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LAPIS Technology Co., Ltd.
October 1, 2020

ROHM GROUP
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20LD-0901-ML62Q1000-Errata-06E

ML62Q1300 Group
ML62Q1500/ML62Q1800 Group
ML62Q1700 Group

Restriction of Function and Performance/Usage Note

Issue date: 16 Sep, 2020

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1. Introduction

This document describes restrictions of function and performance and usage notes for ML62Q1300, ML62Q1500/ML62Q1800 and ML62Q1700 group.

1.1 Restriction list

Table 1. Restriction list

Section	Restriction or note	Reference Section	Issue date
2.1	Do not use SnRFUL bit of Synchronous Serial Port n Status Register (SIOnSTAT) in the serial communication unit.	See “2.1 Synchronous Serial I/O Port”.	2019.2.18
2.2	Corrected FTMn interrupt request bit (FTnIR) number in Functional timer FTMn interrupt clear register (FTnIR). Wrong : bit 15 Correct : bit 7	See “2.2 Functional timer”.	2020.1.24
2.3	Do not enter HALT-H mode when an external interrupt is used in the high-speed clock sampling mode. Also do not change the ENOSC bit.	See “2.3 External interrupt sampling”.	2020.1.24
2.4	Disable the CPU interrupt (MIE=0) when entering the STOP mode.	See “2.4 Interrupt processing while releasing STOP mode”.	2020.1.24
2.5	Corrected description of filtering function for the functional timer trigger and the external clock.	See “2.5 Functional timer filter function “.	2020.1.24
2.6	Unexpected emergency stop may occur at Functional timer Emergency stop setting	See “2.6 Functional timer Emergency stop”.	2020.1.24
2.7	When write to interrupt request register while Expanded External interrupt is used, Expanded external interrupt may not be notified to CPU.	See “2.7” Expanded external interrupt (EXI8INT-EXI11INT)	2020.9.16

2. Details of restriction

2.1 Synchronous Serial I/O Port

If reading Serial Communication Unit n Transmit/Receive Buffer (SDnBUF) at the same time as completion of the data receive, SnRFUL bit of Synchronous Serial Port n Status Register (SIOnSTAT) is not set to "1".

Applicable documents:

Documents Name	Documents No	Chapter	Page
ML62Q1000 Series User’s Manual (Rev1, Rev2)	FEUL62Q1000-01 FEUL62Q1000-02	Chapter 11 Serial Communication Unit	P11-24

Applicable products:

ML62Q1323 / ML62Q1324 / ML62Q1325 : SSOP16 / WQFN16
ML62Q1333 / ML62Q1334 / ML62Q1335 : TSSOP20
ML62Q1345 / ML62Q1346 / ML62Q1347 : WQFN24
ML62Q1365 / ML62Q1366 / ML62Q1367 : TQFP32 / WQFN32
ML62Q1530 / ML62Q1531 / ML62Q1532 / ML62Q1533 / ML62Q1534 : TQFP48
ML62Q1540 / ML62Q1541 / ML62Q1542 / ML62Q1543 / ML62Q1544 : TQFP52
ML62Q1550 / ML62Q1551 / ML62Q1552 / ML62Q1553 / ML62Q1554 / ML62Q1555 / ML62Q1556 / ML62Q1557 / ML62Q1858 / ML62Q1859 : TQFP64 / QFP64

ML62Q1563 / ML62Q1564 / ML62Q1565 / ML62Q1566 / ML62Q1567 / ML62Q1868 / ML62Q1869 : QFP80
ML62Q1573 / ML62Q1574 / ML62Q1575 / ML62Q1576 / ML62Q1577 / ML62Q1878 / ML62Q1879 : TQFP100 / QFP100
ML62Q1700 / ML62Q1701 / ML62Q1702 / ML62Q1703 / ML62Q1704 : TQFP48
ML62Q1710 / ML62Q1711 / ML62Q1712 / ML62Q1713 / ML62Q1714 : TQFP52
ML62Q1720 / ML62Q1721 / ML62Q1722 / ML62Q1723 / ML62Q1724 / ML62Q1725 / ML62Q1726 / ML62Q1727 / ML62Q1728 / ML62Q1729 : QFP64 / TQFP64
ML62Q1733 / ML62Q1734 / ML62Q1735 / ML62Q1736 / ML62Q1737 / ML62Q1738 / ML62Q1739 : QFP80
ML62Q1743 / ML62Q1744 / ML62Q1745 / ML62Q1746 / ML62Q1747 / ML62Q1748 / ML62Q1749 : QFP100 / TQFP100

2.1.1 Restriction

Do not use the SnRFUL bit of Synchronous Serial Port n Status Register (SIOnSTAT) in the serial communication unit.

2.1.2 Improvement plan

No plan to fix the hardware of ML62Q1300, ML62Q1500/ML62Q1800, ML62Q1700.

2.2 Functional timer

A description for bit No. of FTnIR bit in FTMn interrupt clear register (FTnINTC) used for Functional timer is wrong.

Wrong : FTMn interrupt clear register (FTnINTC) FTnIR bit = bit 15
Correct : FTMn interrupt clear register (FTnINTC) FTnIR bit = bit 7

Applicable document:

Documents Name	Documents No	Chapter	Page
ML62Q1000 Series User's Manual (Rev2)	FEUL62Q1000-02	Chapter 9 Functional timer	P9-31

Applicable products:

ML62Q1323 / ML62Q1324 / ML62Q1325 : SSOP16 / WQFN16
ML62Q1333 / ML62Q1334 / ML62Q1335 : TSSOP20
ML62Q1345 / ML62Q1346 / ML62Q1347 : WQFN24
ML62Q1365 / ML62Q1366 / ML62Q1367 : TQFP32 / WQFN32
ML62Q1530 / ML62Q1531 / ML62Q1532 / ML62Q1533 / ML62Q1534 : TQFP48
ML62Q1540 / ML62Q1541 / ML62Q1542 / ML62Q1543 / ML62Q1544 : TQFP52
ML62Q1550 / ML62Q1551 / ML62Q1552 / ML62Q1553 / ML62Q1554 / ML62Q1555 / ML62Q1556 / ML62Q1557 / ML62Q1858 / ML62Q1859 : TQFP64 / QFP64
ML62Q1563 / ML62Q1564 / ML62Q1565 / ML62Q1566 / ML62Q1567 / ML62Q1868 / ML62Q1869 : QFP80
ML62Q1573 / ML62Q1574 / ML62Q1575 / ML62Q1576 / ML62Q1577 / ML62Q1878 / ML62Q1879 : TQFP100 / QFP100
ML62Q1700 / ML62Q1701 / ML62Q1702 / ML62Q1703 / ML62Q1704 : TQFP48
ML62Q1710 / ML62Q1711 / ML62Q1712 / ML62Q1713 / ML62Q1714 : TQFP52
ML62Q1720 / ML62Q1721 / ML62Q1722 / ML62Q1723 / ML62Q1724 / ML62Q1725 / ML62Q1726 / ML62Q1727 / ML62Q1728 / ML62Q1729 : QFP64 / TQFP64
ML62Q1733 / ML62Q1734 / ML62Q1735 / ML62Q1736 / ML62Q1737 / ML62Q1738 / ML62Q1739 : QFP80
ML62Q1743 / ML62Q1744 / ML62Q1745 / ML62Q1746 / ML62Q1747 / ML62Q1748 / ML62Q1749 : QFP100 / TQFP100

2.2.1 Restriction

- Write to the interrupt request bit(FTnIR: bit 7) of Functional timer FTMn interrupt clear register(n=0~7) by word access. The writing to the FTnIR bit by byte access or bit access is disabled.

  - DTU8 debugger cannot write to the FTnIR bit on the SFR window or the watch window.

2.2.2 Improvement plan

No plan to fix the hardware on ML62Q1300, ML62Q1500/ML62Q1800, ML62Q1700.

The bit No. of FTnIR bit is corrected in revised device information file, available in U8/U16 Development Tools Release 2.1.0.

2.3 External interrupt sampling

If an interrupt occurred while the high-speed clock is being stopped in the case of the high-speed clock sampling is selected, the same interrupt may occur again when restarting the high-speed clock.

Note that the following cases are not applicable to the restriction.
1: External interrupt function (interrupt and trigger, and etc.) is not used.
2: High-speed clock sampling is not selected as sampling clock even the external interrupt function is used.

・Conditions
On the presupposition that
- External sampling function is used.
- High-speed clock is selected as sampling clock
(PInSM bit =1 and PG0CS0 bit =1 in the external interrupt mode register 0(EIMOD0))
When the following operations are executed, the unintended interrupt may occur.

1. Shift to HALT-H mode under the state of high-speed clock turns on (ENOSC = 1) .

(The unintended interrupt does not occur in the case of STOP/STOP-D mode because an initialize sequence is executed)

2. Change Frequency control register (FCON) ENOSC bit from 1 → 0 →1.

(0 : turns the high-speed clock off, 1: turns high-speed clock on)

Applicable document:

Documents Name	Documents No	Chapter	Page
ML62Q1000 Series User's Manual (Rev2)	FEUL62Q1000-02	Chapter 18 External Interrupt Function	P18-7, P18-8

Applicable products:

ML62Q1323 / ML62Q1324 / ML62Q1325	: SSOP16 / WQFN16
ML62Q1333 / ML62Q1334 / ML62Q1335	: TSSOP20
ML62Q1345 / ML62Q1346 / ML62Q1347	: WQFN24
ML62Q1365 / ML62Q1366 / ML62Q1367	: TQFP32 / WQFN32
ML62Q1530 / ML62Q1531 / ML62Q1532 / ML62Q1533 / ML62Q1534	: TQFP48
ML62Q1540 / ML62Q1541 / ML62Q1542 / ML62Q1543 / ML62Q1544	: TQFP52
ML62Q1550 / ML62Q1551 / ML62Q1552 / ML62Q1553 / ML62Q1554 / ML62Q1555 / ML62Q1556 / ML62Q1557 / ML62Q1858 / ML62Q1859	: TQFP64 / QFP64
ML62Q1563 / ML62Q1564 / ML62Q1565 / ML62Q1566 / ML62Q1567 / ML62Q1868 / ML62Q1869	: QFP80
ML62Q1573 / ML62Q1574 / ML62Q1575 / ML62Q1576 / ML62Q1577 / ML62Q1878 / ML62Q1879	: TQFP100 / QFP100
ML62Q1700 / ML62Q1701 / ML62Q1702 / ML62Q1703 / ML62Q1704	: TQFP48
ML62Q1710 / ML62Q1711 / ML62Q1712 / ML62Q1713 / ML62Q1714	: TQFP52

ML62Q1720 / ML62Q1721 / ML62Q1722 / ML62Q1723 / ML62Q1724
/ ML62Q1725 / ML62Q1726 / ML62Q1727 / ML62Q1728 / ML62Q1729 : QFP64 / TQFP64
ML62Q1733 / ML62Q1734 / ML62Q1735 / ML62Q1736 / ML62Q1737
/ ML62Q1738 / ML62Q1739 : QFP80
ML62Q1743 / ML62Q1744 / ML62Q1745 / ML62Q1746 / ML62Q1747
/ ML62Q1748 / ML62Q1749 : QFP100 / TQFP100

2.3.1 Restriction

- If shifting to HALT-H mode while using the external interrupt with the high-speed clock sampling mode, change an another mode to " No sampling"
- If changing ENOSC bit while using the external interrupt with the high-speed clock sampling mode, change to an another mode " No sampling" or disable the interrupt during the change of clock.

2.3.2 Improvement plan

No plan to fix the hardware on ML62Q1300, ML62Q1500/ML62Q1800, ML62Q1700.

2.4 Interrupt processing while releasing STOP mode

When waking up from STOP/STOP-D mode with a condition of that the interrupt to the CPU is enabled (MIE="1"), the program operation may shift to an unintended interrupt routine.

Note that the following cases are not applicable to the restriction.
- STOP/STOP-D mode is not used.
- MIE flag is "0" even STOP/STOP-D mode is used.

・Conditions
When CPU is in interrupt enable status (MIE=1) and a wakeup factor is generated under the following timing.

- When an wakeup factor is generated while shifting to the STOP/STOP-D mode (before the LSI completely stopped).
- In the case multiple interrupt are enabled for the wakeup from STOP/STOP-D mode, when it wakes up the CPU and a another interrupt with higher priority is generated at the timing of the CPU restarted.

Applicable document:

Documents Name	Documents No	Chapter	Page
ML62Q1000 Series User's Manual (Rev2)	FEUL62Q1000-02	Chapter 4 Power Management	P4-6 P4-25

Applicable products:
ML62Q1323 / ML62Q1324 / ML62Q1325 : SSOP16 / WQFN16
ML62Q1333 / ML62Q1334 / ML62Q1335 : TSSOP20
ML62Q1345 / ML62Q1346 / ML62Q1347 : WQFN24
ML62Q1365 / ML62Q1366 / ML62Q1367 : TQFP32 / WQFN32
ML62Q1530 / ML62Q1531 / ML62Q1532 / ML62Q1533 / ML62Q1534 : TQFP48
ML62Q1540 / ML62Q1541 / ML62Q1542 / ML62Q1543 / ML62Q1544 : TQFP52
ML62Q1550 / ML62Q1551 / ML62Q1552 / ML62Q1553 / ML62Q1554
/ ML62Q1555 / ML62Q1556 / ML62Q1557 / ML62Q1858 / ML62Q1859 : TQFP64 / QFP64
ML62Q1563 / ML62Q1564 / ML62Q1565 / ML62Q1566 / ML62Q1567
/ ML62Q1868 / ML62Q1869 : QFP80
ML62Q1573 / ML62Q1574 / ML62Q1575 / ML62Q1576 / ML62Q1577
/ ML62Q1878 / ML62Q1879 : TQFP100 / QFP100
ML62Q1700 / ML62Q1701 / ML62Q1702 / ML62Q1703 / ML62Q1704 : TQFP48

ML62Q1710 / ML62Q1711 / ML62Q1712 / ML62Q1713 / ML62Q1714 : TQFP52
ML62Q1720 / ML62Q1721 / ML62Q1722 / ML62Q1723 / ML62Q1724
/ ML62Q1725 / ML62Q1726 / ML62Q1727 / ML62Q1728 / ML62Q1729 : QFP64 / TQFP64
ML62Q1733 / ML62Q1734 / ML62Q1735 / ML62Q1736 / ML62Q1737
/ ML62Q1738 / ML62Q1739 : QFP80
ML62Q1743 / ML62Q1744 / ML62Q1745 / ML62Q1746 / ML62Q1747
/ ML62Q1748 / ML62Q1749 : QFP100 / TQFP100

2.4.1 Restriction and Workaround

- Disable the interrupts to the CPU (Set MIE to “0”) when shifting to the STOP/STOP-D mode
- STOP/STOP-D mode is not available in the case of SYSTEMCLK = 24MHz setting.
- Select 16MHz or lower for SYSTEMCLK when shifting the STOP/STOP-D mode.

See the following example of workaround that changes MIE to “0”.

Example of workaround 1) How to disable the interrupts saving the status of MIE

```
#pragma asm
  PUSH R0             ;R0 (Backup)
  MOV  R0,     #05ah
  ST   R0,     STPACP   ;5A
  MOV  R0,     #0a5h
  ST   R0,     STPACP   ;A5
  MOV  R0,     PSW      ;PSW (Backup)
  DI
  SB   STP             ;STOP mode
  NOP
  NOP
  MOV  PSW, R0         ;PSW rewrite(if MIE=1, shift to interrupt process from here)
  NOP
  NOP
  POP  R0              ;R0 rewrite
#pragma endasm
```

・In this example, SB instruction is used set the STOP bit and “z” flag of PSW is reset to “0”.
・In this example, the program shifts to an interrupt processing routine before rewriting R0. So, note that R0 is changed in the interrupt processing routine.

Example of workaround 2)　How to implement by using the software interrupt

```
int main( void )
{
      :
__asm("swi #0");
__asm("nop¥n");
__asm("nop¥n");
      :
}

#pragma SWI smpl_procSWI0Int 0x0080 1
static void smpl_procSWI0Int( void )
{
/* set the CPU mode to 'Stop mode' */
lp_setStopMode();
}

void lp_setStopMode( void )
{
/* set StopCode Accepter */
write_reg8( STPACP, 0x50 );
write_reg8( STPACP, 0xA0 );

/* The CPU mode is changed to the STOP mode. */
set_bit( STP );
__asm("nop¥n");
__asm("nop¥n");
}
```

Place two NOP instructions because an instruction immediately after the SWI instruction may be executed before an instruction in the interrupt routine.

2.4.2 Improvement plan

No plan to fix the hardware on ML62Q1300, ML62Q1500/ML62Q1800, ML62Q1700.

2.5 Functional timer filter function

The descriptions of functional timer trigger/external clock filtering function are incorrect.
The trigger/the clock may be filtered depending on the pulse width.

Applicable document:

Documents Name	Documents No	Chapter	Page
ML62Q1000 Series User's Manual (Rev2)	FEUL62Q1000-02	Chapter 9 Functional timer	P9-21 P9-24～26

20LD-0901-ML62Q1000-Errata-06E

Applicable products:

ML62Q1323 / ML62Q1324 / ML62Q1325	: SSOP16 / WQFN16
ML62Q1333 / ML62Q1334 / ML62Q1335	: TSSOP20
ML62Q1345 / ML62Q1346 / ML62Q1347	: WQFN24
ML62Q1365 / ML62Q1366 / ML62Q1367	: TQFP32 / WQFN32
ML62Q1530 / ML62Q1531 / ML62Q1532 / ML62Q1533 / ML62Q1534	: TQFP48
ML62Q1540 / ML62Q1541 / ML62Q1542 / ML62Q1543 / ML62Q1544	: TQFP52
ML62Q1550 / ML62Q1551 / ML62Q1552 / ML62Q1553 / ML62Q1554 / ML62Q1555 / ML62Q1556 / ML62Q1557 / ML62Q1858 / ML62Q1859	: TQFP64 / QFP64
ML62Q1563 / ML62Q1564 / ML62Q1565 / ML62Q1566 / ML62Q1567 / ML62Q1868 / ML62Q1869	: QFP80
ML62Q1573 / ML62Q1574 / ML62Q1575 / ML62Q1576 / ML62Q1577 / ML62Q1878 / ML62Q1879	: TQFP100 / QFP100
ML62Q1700 / ML62Q1701 / ML62Q1702 / ML62Q1703 / ML62Q1704	: TQFP48
ML62Q1710 / ML62Q1711 / ML62Q1712 / ML62Q1713 / ML62Q1714	: TQFP52
ML62Q1720 / ML62Q1721 / ML62Q1722 / ML62Q1723 / ML62Q1724 / ML62Q1725 / ML62Q1726 / ML62Q1727 / ML62Q1728 / ML62Q1729	: QFP64 / TQFP64
ML62Q1733 / ML62Q1734 / ML62Q1735 / ML62Q1736 / ML62Q1737 / ML62Q1738 / ML62Q1739	: QFP80
ML62Q1743 / ML62Q1744 / ML62Q1745 / ML62Q1746 / ML62Q1747 / ML62Q1748 / ML62Q1749	: QFP100 / TQFP100

2.5.1 Revised contents in Rev.3

The descriptions of the noise removal width and effective pulse width determined by FTnTRF2~0 bit are incorrect in user's manual revision 2. See the following corrected descriptions.

Wrong: User's Manual Rev.2

Note in section 9.2.9/9.2.10 (Page: 9-21,9-24)	The pulse input to the EXTRG0 to EXTRG7 pin must have "the noise removal width chosen by FTnTRF2 to 0 bits of FTnTRG1 register + two timer clocks" or longer.
Note in section 9.2.11 (Page: 9-26)	The pulse input to the EXTRG0 to EXTRG7 pin must have "the noise removal width chosen by FTnTRF2 to 0 bits of FTnTRG1 register + two timer clocks" or longer.
Description in section 9.3.7.2 (Page: 9-56)	If EXTRG0 to EXTRG7 and CMP0D are chosen as the event trigger source, input the signal with the noise removal width set in FTnTRF2 to FTnTRF0 bits of the FTnTRG1 register or longer.

Description of bit in section 9.2.11 (Page9-25)

Bit No.	Bit symbol name	Description	
10~8	FTnTRF2~ FTnTRF0	000:	Noise filter is disabled (initial value)
		001:	Remove noise for 2 clocks of HSCLK
		010:	Remove noise for 4 clocks of HSCLK
		011:	Remove noise for 8 clocks of HSCLK
		100:	Remove noise for 16 clocks of HSCLK
		101:	Remove noise for 32 clocks of HSCLK
		110:	Remove noise for 64 clocks of HSCLK
		111:	Remove noise for 128 clocks of HSCLK

Correct: User's Manual Rev.3

Bit No.	Bit symbol name	Description

Bit No.	Bit symbol name	Description			
10~8	FTnTRF2~ FTnTRF0	These bits are used to set the noise filter function for the external trigger or the external clock (EXTRG0 to EXTRG7 and CMP0TRG). It is invalid for other event trigger and the emergency stop trigger source. Input signal: EXTRG0 to EXTRG7 or CMP0TRG are sampled by the timer clock. The following shows valid pulse width and invalid pulse width of the input signal. It is uncertain whether the other pulse width can be accepted or removed.			
			Filter function, Filtering clock,	Valid pulse width ,	Invalid pulse width
		000 :	disabled, none,	more than 1 cycle,	none (Initial value)
		001 :	enabled, 1/2 of timer clock,	more than 4 cycles,	less than 2 cycles
		010 :	enabled, 1/4 of timer clock,	more than 8 cycles,	less than 4 cycles
		011 :	enabled, 1/8 of timer clock,	more than 16 cycles,	less than 8 cycles
		100 :	enabled, 1/16 of timer clock,	more than 32 cycles,	less than 16 cycles
		101 :	enabled, 1/32 of timer clock,	more than 64 cycles,	less than 32 cycles
		110 :	enabled, 1/64 of timer clock,	more than 128 cycles,	less than 64 cycles
		111 :	enabled, 1/128 of timer clock,	more than 256 cycles,	less than 128 cycles

2.6 Functional timer emergency stop

Unintended functional timer emergency stop occurs on the following conditions regardless the status of functional timer.

Conditions :
- When changed FTnEMGEN bit from “0” to “1” on the condition of the trigger input status is “H” and the trigger edge is “rise”
- When changed FTnEMGEN bit from “1” to “0” on the condition of the trigger input status is “H” and the trigger edge is “fall”

The emergency stop interrupt status bit (FTnISES) and interrupt request bit(QFTMn) becomes “1”, 3 system clocks + 3 timer clocks after the change of FTnEMGEN bit in FTCCON register.

Applicable document:

Documents Name	Documents No	Chapter	page
ML62Q1000 Series User’s Manual (Rev2)	FEUL62Q1000-02	Chapter 9 Functional timer	P9-58

Applicable products:

ML62Q1323 / ML62Q1324 / ML62Q1325	: SSOP16 / WQFN16
ML62Q1333 / ML62Q1334 / ML62Q1335	: TSSOP20
ML62Q1345 / ML62Q1346 / ML62Q1347	: WQFN24
ML62Q1365 / ML62Q1366 / ML62Q1367	: TQFP32 / WQFN32
ML62Q1530 / ML62Q1531 / ML62Q1532 / ML62Q1533 / ML62Q1534	: TQFP48

ML62Q1540 / ML62Q1541 / ML62Q1542 / ML62Q1543 / ML62Q1544 : TQFP52
ML62Q1550 / ML62Q1551 / ML62Q1552 / ML62Q1553 / ML62Q1554
/ ML62Q1555 / ML62Q1556 / ML62Q1557 / ML62Q1858 / ML62Q1859 : TQFP64 / QFP64
ML62Q1563 / ML62Q1564 / ML62Q1565 / ML62Q1566 / ML62Q1567
/ ML62Q1868 / ML62Q1869 : QFP80
ML62Q1573 / ML62Q1574 / ML62Q1575 / ML62Q1576 / ML62Q1577
/ ML62Q1878 / ML62Q1879 : TQFP100 / QFP100
ML62Q1700 / ML62Q1701 / ML62Q1702 / ML62Q1703 / ML62Q1704 : TQFP48
ML62Q1710 / ML62Q1711 / ML62Q1712 / ML62Q1713 / ML62Q1714 : TQFP52
ML62Q1720 / ML62Q1721 / ML62Q1722 / ML62Q1723 / ML62Q1724
/ ML62Q1725 / ML62Q1726 / ML62Q1727 / ML62Q1728 / ML62Q1729 : QFP64 / TQFP64
ML62Q1733 / ML62Q1734 / ML62Q1735 / ML62Q1736 / ML62Q1737
/ ML62Q1738 / ML62Q1739 : QFP80
ML62Q1743 / ML62Q1744 / ML62Q1745 / ML62Q1746 / ML62Q1747
/ ML62Q1748 / ML62Q1749 : QFP100 / TQFP100

2.6.1 Restriction

Change the FTnRMGEN bit except the condition of that the unintended emergency stop occurs, or need to cancel the emergency stop for running the timer after the unintended emergency stop occurred.

2.6.2 Improvement plan

No plan to fix the hardware on ML62Q1300, ML62Q1500/ML62Q1800, ML62Q1700.

2.7 Expanded external interrupt (EXI8INT-EXI11INT)

In the timing when Expanded external interrupt occurs, when interrupt request registers(IRQ01,IRQ23,IRQ45,IRQ67) are written from a CPU, Expanded external interrupt status register(EEISTAT) is set, but the request bit(QEXTX=IRQ23 register, bit 8) of Expanded external interrupt is not set and the interrupt may not be notified to CPU.

When Expanded external interrupt status register(EEISTAT) is set,
Unless clearing the register or re-requesting interrupt by setting interrupt request bit(EEIR) of Expanded external interrupt clear register(EEINTC) to 1, Expanded external interrupt is not notified afterward.

Applicable document:

Documents Name	Documents No	Chapter	page
ML62Q1000 Series User's Manual (Rev5)	FEUL62Q1000-05	Chapter 5 Interrupt Chapter 18 External Interrupt Function	P5-13～20 P18-9～13

Applicable products:

ML62Q1530 / ML62Q1531 / ML62Q1532 / ML62Q1533 / ML62Q1534 : TQFP48
ML62Q1540 / ML62Q1541 / ML62Q1542 / ML62Q1543 / ML62Q1544 : TQFP52
ML62Q1550 / ML62Q1551 / ML62Q1552 / ML62Q1553 / ML62Q1554
/ ML62Q1555 / ML62Q1556 / ML62Q1557 / ML62Q1858 / ML62Q1859 : TQFP64 / QFP64
ML62Q1563 / ML62Q1564 / ML62Q1565 / ML62Q1566 / ML62Q1567
/ ML62Q1868 / ML62Q1869 : QFP80
ML62Q1573 / ML62Q1574 / ML62Q1575 / ML62Q1576 / ML62Q1577
/ ML62Q1878 / ML62Q1879 : TQFP100 / QFP100
ML62Q1700 / ML62Q1701 / ML62Q1702 / ML62Q1703 / ML62Q1704 : TQFP48
ML62Q1710 / ML62Q1711 / ML62Q1712 / ML62Q1713 / ML62Q1714 : TQFP52

ML62Q1720 / ML62Q1721 / ML62Q1722 / ML62Q1723 / ML62Q1724
/ ML62Q1725 / ML62Q1726 / ML62Q1727 / ML62Q1728 / ML62Q1729 : QFP64 / TQFP64
ML62Q1733 / ML62Q1734 / ML62Q1735 / ML62Q1736 / ML62Q1737
/ ML62Q1738 / ML62Q1739 : QFP80
ML62Q1743 / ML62Q1744 / ML62Q1745 / ML62Q1746 / ML62Q1747
/ ML62Q1748 / ML62Q1749 : QFP100 / TQFP100

2.7.1 Restriction

When interrupt request registers(IRQ01,IRQ23,IRQ45,IRQ67) are written while Expanded External interrupt is enabled(setting except “disable interrupt” by Expanded external interrupt control register 0(EEICON0)), re-request interrupt by setting EEINTC EEIR to 1 after having written the interrupt request register.

2.7.2 Improvement plan

No plan to fix the hardware on ML62Q1500/ML62Q1800, ML62Q1700.

3. Revision History

Document No.	Issue date	Page		Description
		Previous Rev.	Current Rev.	
19LD-0158-ML62Q1300_ML62Q1500_ML62Q1700-Errata-01E	2019.2.18	–	–	First Revision
20LD-0071 -ML62Q1300_ML62Q1500 _ML62Q1700_Errata_04E	2020.1.24	–	–	The 2nd and 3rd Revision are skipped to match the revision number to Japanese errata document.
		2	2	Add section 2.2 to 1.1 list
		–	3,4	Add section 2.2 functional timer
		2	2	Add section 2.3, 2.4 to 1.1 list
		4	4	Updated 2.2.2 Improvement plan
		–	4,5	Add section 2.3 external interrupt sampling
		–	5,6,7	Add section 2.4 interrupt processing while releasing Stop mode
		2	2	Update section 2.4 of 1.1 list Add section 2.5,2.6 to 1.1 list
		7	7	Corrected Example of workaround 2) in section 2.4
		–	8,9	Add section 2.5 Functional timer filtering function
		–	10	Add section 2.6 Functional timer Emergency stop
20LD-0212-ML62Q1000-Errata-05E	2020.3.19	*	*	Corrected typo
20LD-0901-ML62Q1000-Errata-06E	2020.9.16	2	2	Update section 2.7 of 1.1 list
		–	11,12	Add section 2.7 Expanded external interrupt (EXI8INT-EXI11INT)