Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL86640-03
Issue Date: Feb.20.2024

ML86640

NTSC/PAL format compatible　Single power source　P/I conversion function equipped　Compact Digital Video Encoder

■ Preface

ML86640 is a digital video encoder compatible with the NTSC/PAL format. The encoder converts digital image input such as ITU-R BT.656, ITU-R BT.601, etc. to analog image signal. Supported digital image input is RGB 24bit, YCbCr 24bit / 16bit / 8bit, and ITU-R BT.656. Its input scan mode supports both interlace and progressive.
The analog image output is a NTSC/PAL composite signal 1 ch. P/I conversion is equipped to output progressive digital data as interlace signals. An output signal can be used by directly connecting to a image display apparatus. External video amplifiers are not required.

■ Features

○ Supported image format
NTSC/PAL

○ Input scan mode
Interlace /Progressive

○ Input data format
ITU-R BT.656 style : YCbCr 4:2:2 8bit multiplexing Synchronization signal information appending (Interlace/Progressive)
YCbCr 4:2:2 : 8bit multiplexing Each synchronization signal (Interlace/Progressive)
YCbCr 4:2:2 : 16bit non-multiplexing (Interlace/Progressive)
YCbCr 4:4:4 : 24bit non-multiplexing (Interlace/Progressive)
RGB 4:4:4 : 24bit non-multiplexing (Interlace/Progressive)

○ Input CLK frequency
Interlace input
27MHz : BT.656 / 8bit YCbCr
13.5MHz : BT.656 DDR / 8bit YCbCr DDR
13.5MHz : 16bit/24bit YCbCr
13.5MHz : 24bit RGB
Progressive input
54MHz : BT.656 / 8bit YCbCr
27MHz : BT.656 DDR / 8bit YCbCr DDR
27MHz : 16bit/24bit YCbCr
27MHz : 24bit RGB
（※DDR：Double data rate）

○ Output format
Composite (CVBS)

○ Scan type conversion function
Progressive to Interlace

○ Internal color bar output function
○ Luminance level adjustment function
○ Color difference level adjustment function
○ Extended luminance range mode (possible input: 1-254)
○ Extended color difference range mode (possible input: 1-254)
○ Standby mode
○ R/G/B and Y/Cb/Cr input port swapping
○ Input data MSB-LSB swapping
○ Field input function at PI conversion

○ CGMS/WSS information appending function
○ Closed captioning information appending function
○ Serial interface : I^2C Slave, Max400 kHz
Slave address 88 h (1000_100x)

○ Operation ambient temperature (Ta) : -40 to 105 °C

○ Power source voltage : 3.3 V Single (I/O, core, and analog)

○ Package : 48pin TQFP (P-TQFP48-0707-0.50-ZK6)

■ Application

- Car navigation
- Display audio
- In-vehicle camera
- Drive recorder
- Video intercom

■ Line up

Part Number	Shipping form
ML86640TBZ0AX	Tray

■ BLOCK DIAGRAM

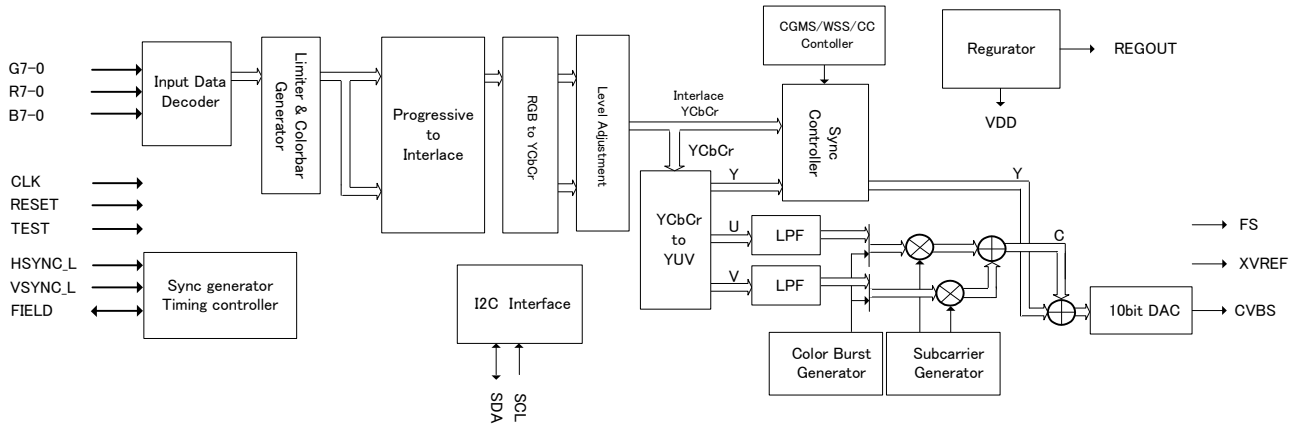
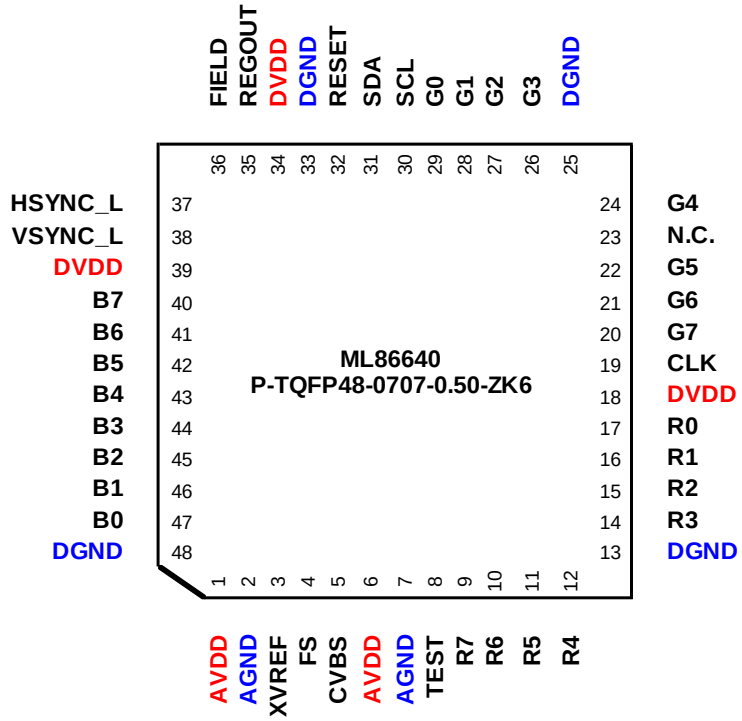


Figure 1: Block diagram

■ PIN CONFIGURATION
(TOP VIEW)



TQFP48

Note:
Make sure non-used input pins are fixed to "L" or "H" level, not to become OPEN.
Fix the TEST pin to "L" level.

■ PIN FUNCTIONS

Pin	Symbol	I/O	Function	Description	Initial State
1	AVDD	—	Analog power supply (3.3V)		-
2	AGND	—	Analog GND		-
3	XVREF	O	Reference voltage pin Connect a 0.01uF capacitor between the XVREF and AGND		output
4	FS	O	Video output full-scale adjustment pin Connect a 150ohm resistor for adjustment between the FS and AGND pins. (Resister is better than +/- 1% accuracy)		output
5	CVBS	O	Composite signal output pin refer to “Example of Application Circuits” (Resister is better than +/- 1% accuracy)		output
6	AVDD	—	Analog power supply (3.3V)		-
7	AGND	—	Analog GND		-
8	TEST	I	Test mode pin Please fix the TEST terminal to the “L” level.	PD	input
9	R7	I	Digital video data input (MSB)		input
10	R6	I	Digital video data input		input
11	R5	I	Digital video data input		input
12	R4	I	Digital video data input		input
13	DGND	—	Digital GND		-
14	R3	I	Digital video data input		input
15	R2	I	Digital video data input		input
16	R1	I	Digital video data input		input
17	R0	I	Digital video data input (LSB)		input
18	DVDD	—	Digital power supply (3.3V)		-
19	CLK	I	Pixel clock input		input
20	G7	I	Digital video data input (MSB)		input
21	G6	I	Digital video data input		input
22	G5	I	Digital video data input		input
23	N.C.	—			-
24	G4	I	Digital video data input		input
25	DGND	—	Digital GND		-
26	G3	I	Digital video data input		input
27	G2	I	Digital video data input		input
28	G1	I	Digital video data input		input
29	G0	I	Digital video data input (LSB)		input
30	SCL	I	I^2C Clock	ST, 5V-tolerant	input
31	SDA	I/O	I^2C Data	ST, 5V-tolerant	input
32	RESET	I	Reset input	ST	input

Pin	Symbol	I/O	Function	Description	Initial State
33	DGND	—	Digital GND		-
34	DVDD	—	Digital power supply (3.3V)		-
35	REGOUT	O	Regulator output Connect a 4.7uF±20% capacitor between the REGOUT and DGND		output
36	FIELD	I/O	Field input		input
37	HSYNC_L	I	Horizontal sync signal input-output pin (In BT.656 mode, connect with “L” level.)		input
38	VSYNC_L	I	Vertical sync signal input-output pin (In BT.656 mode, connect with “L” level.)		input
39	DVDD	—	Digital power supply (3.3V)		-
40	B7	I	Digital video data input (MSB)		input
41	B6	I	Digital video data input		input
42	B5	I	Digital video data input		input
43	B4	I	Digital video data input		input
44	B3	I	Digital video data input		input
45	B2	I	Digital video data input		input
46	B1	I	Digital video data input		input
47	B0	I	Digital video data input (LSB)		input
48	DGND	—	Digital GND		-

PD = pull-down. ST = Schmitt Trigger.

Note) pull-down is about 40Kohm

The nonuse input terminal fixes it to “L” or the “H” level, and prevent it from becoming OPEN.

■ ELECTRICAL CHARACTERISTICS

● ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage (I/O, Core)	DVDD	Ta = 25°C	–0.3 V to +4.6 V	V
Power supply voltage (Analog)	AVDD	Ta = 25°C	–0.3 V to +4.6 V	V
Input voltage	V_I	Ta = 25°C	–0.3 V to +DVDD+0.3V	V
Output short-circuit current	I_{OS}	—	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Storage temperature	T_{stg}	—	–55 to +150	°C

Caution: Product quality may suffer if any of the absolute maximum ratings above is exceeded, even for an instant. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage. Therefore the product must be used under conditions that ensure that no absolute maximum rating will ever be exceeded.

● RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (I/O, Core)	DVDD	3.0	3.3	3.6	V
Power supply voltage (Analog)	AVDD	3.0	3.3	3.6	V
Operating temperature	T_a	-40	+25	+105	°C

● DC Characteristics

Ta = –40 to +105°C, DVDD= 3.3 V ±0.3 V, AVDD = 3.3 V ±0.3 V, DGND, AGND = 0 V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" level input voltage 1	V_{IH1}	LVTTL	2.0	-	DVDD +0.3V	V
"H" level input voltage 2	V_{IH2} *1	5V-tolerant/Schmitt	2.1	-	5.5	V
"H" level input voltage 3	V_{IH3} *2	Schmitt	2.1	-	DVDD +0.3V	V
"L" level input voltage 1	V_{IL1}	LVTTL	-0.3	-	0.8	V
"L" level input voltage 2	V_{IL2} *3	Schmitt	-0.3	-	0.7	V
"H" level output voltage	V_{OH} *4	I_{OH}= -4mA	2.4	-	-	V
"L" level output voltage	V_{OL}	I_{OL}= 4mA	-	-	0.4	V
Input leakage current	I_{IL}	V_{IN}=DVDD or DGND	-10	-	+10	µA
"H" level input current (pull-down resistance)	I_{IHd}	V_{IN}=DVDD	20	-	200	µA
Output leakage current	I_{OL}	V_{OUT}=DVDD or DGND	-10	-	+10	µA
Power supply current (during operation)	I_{DVDD}	RGB 4:4:4 24bit Progressive	-	-	50	mA
	I_{AVDD}	R_L=75 CLK=54MHz	-	-	50	mA
Power supply current (standby)	I_{DDS}	CLK=0MHz V_{IN}=V_{IL} STANDBY:0Fh[0]=1	-	-	1	mA
REGOUT output voltage	V_{REG}	-	-	2.4	2.75	V

*1: VIH2 is applied to the SDA and SCL pins.
*2: VIH3 is applied to the RESET pin.
*3: VIL2 is applied to SDA, SCL, and RESET pins.
*4: VOH is applied to the FIELD pin. (When #02h[7]:FLDEN=1)

● AC Characteristics

Ta = –40 to +105°C, DVDD= 3.3 V ±0.3 V, AVDD = 3.3 V ±0.3 V, DGND, AGND = 0 V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency (CLK frequency)	F_{CLK}	NTSC/PAL ITU-R BT.601	-	13.5	-	MHz
			-	27	-	MHz
			-	54	-	MHz
Clock duty ratio	dt_{CLK}	-	45	-	55	%
Input data setup time	t_{SI}	-	3	-	-	ns
Input data hold time	t_{HI}	-	1	-	-	ns
Reset pulse time (except Power-ON sequence)	t_{RSTP}	-	200	-	-	ns

● I^2C bus AC Characteristics

I^2C Specifications (Normal Mode)

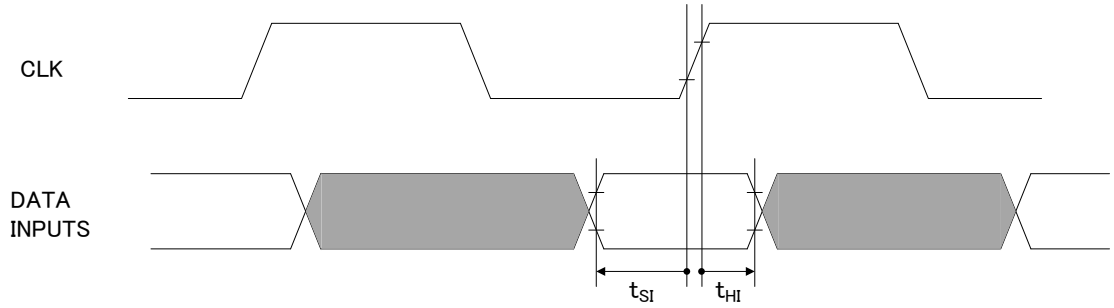
Symbol	Parameter	Min	Typ	Max	Unit
tCCI2C	SCL period	10			μs
tLI2C	Clock LOW period	4.7			μs
tHI2C	Clock HIGH period	4.0			μs
tDHI2C	Data hold time	0			ns
tDSI2C	Data setup time	250			ns

I^2C Specifications (Fast Mode)

Symbol	Parameter	Min	Typ	Max	Unit
tCCI2C	SCL period	2.5			μs
tLI2C	Clock LOW period	1.3			μs
tHI2C	Clock HIGH period	0.6			μs
tDHI2C	Data hold time	0			ns
tDSI2C	Data setup time	100			ns

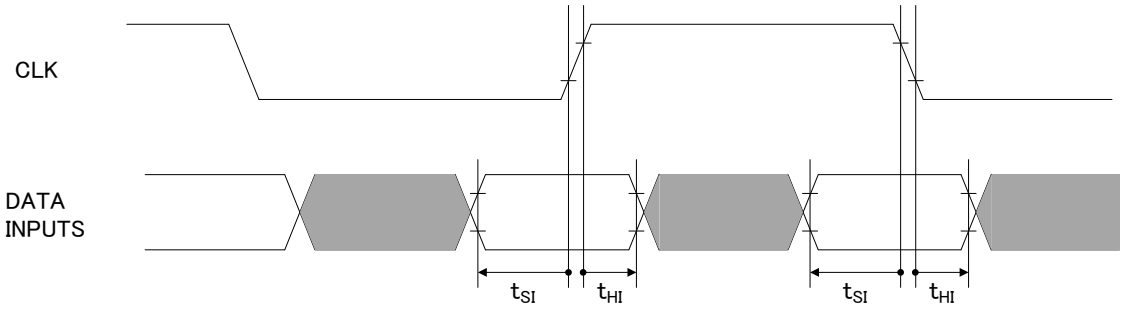
■ Input-output timing

（1）Input timing



Input signal: R7-0, G7-0, B7-0, VSYNC_L, HSYNC_L
(Note: The polarity of loading clock edge of above input signals can be reversed with register setting.)

（2）Input timing(DDR mode)



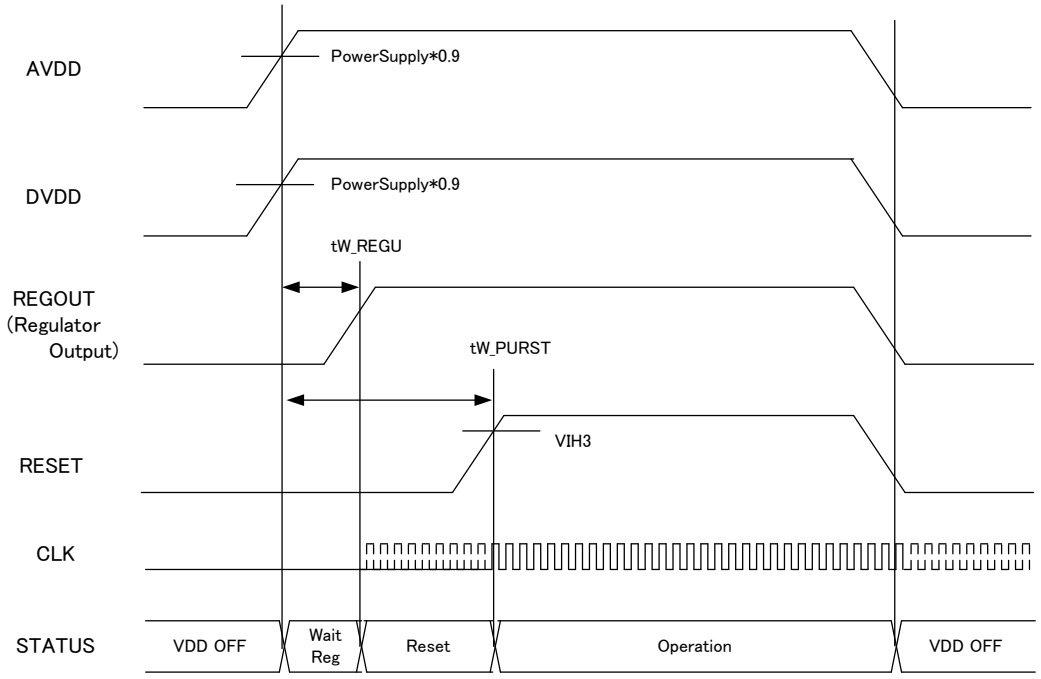
Input signal: R7-0, G7-0, B7-0, VSYNC_L, HSYNC_L
(Note: This mode can be set in the ITU-R BT.656 style or YCbCr 4:2:2 8bit + Synchronization signal input mode).

■ Power ON sequence

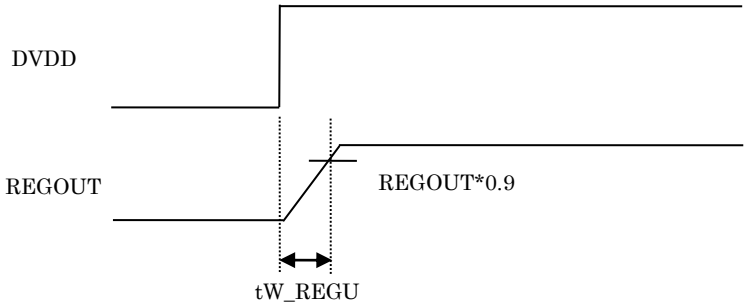
There are no sequence restrictions between each power sources (AVDD and DVDD). It can be used when powered ON and powered OFF from any power sources.
Input "L" for the RESET pin from power application to the reset time (tW_PURST). LSI control is possible after passing the reset time (tW_PURST).
When the power is turned ON again after the power is shut down, start each power source from the 0 V state.

Perform voltage application to the input pin while the regulated voltage is applied to all power sources.

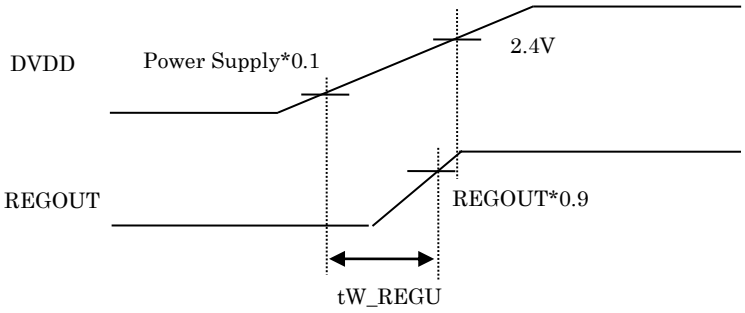
Parameter	Symbol	Min.	Typ.	Max.	Unit	備考
Reset time	tW_PURST	2	—	—	ms	ー
Regulator Start-up time	tW_REGU	—	100	—	us	(*1):When DVDD starts up in rectangular shape(delay 0).
		—	200	—	us	(*2):When DVDD starts up in 300us.



(*1)When DVDD starts up in rectangular shape(delay 0).
tW_REGU is a delay time of Regulator.



(*2) When DVDD starts up in 300us.



■ I²C interface timing

Use the I²C interface to set the internal register values. The I²C bus interface performs the processing by using the clock input to the CLK pin. Be sure to input the clock to the CLK pin. The I²C interface supports the 400 kHz (SCL frequency) high speed mode. Figure 2 shows the basic timing. Make sure that the SDA value does not change while SCL is at a "H" level. For information on timing parameter values refer to the AC characteristics.

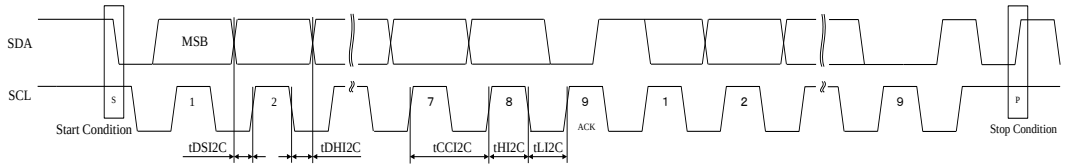


Figure 2: I²C Interface Basic Timing

Figures 3 and 4 show the I²C interface input format.

Write format

S	Slave address (write)	A	Sub address	A	Data 0	A	……..	Data n	A	P

Figure 3: Write Format

Write data to the specified sub address register. If multiple data items are written in succession, the sub address is incremented automatically for each data item.

Read format

S	Slave address (write)	A	Sub address	A	Sr	Slave address (read)	A	Data 0	Am	……..	Data n	Am	P

Figure 4: Read Format

Read data of the register at the specified sub address. If multiple data items are read in succession, the sub address is incremented automatically for each data item.

Table 1: Symbols Used in the Input Formats

Symbol	Meaning
S	Start condition
Sr	Restart condition
Slave address	Slave address "1000_100X" X is the Read/Write identification bit ("1": Read, "0": Write).
A	Acknowledge (slave)
Am	Acknowledge (master)
Sub address	Sub address
Data n	Write and read data at sub address
P	Stop condition

■ Scanning Methods

Table 2 shows the available scanning methods for NTSC and PAL.

Table 2: Scanning Methods

Scanning method	No. of lines	Frequency
NTSC interlaced	262.5	59.94Hz
NTSC progressive	525	59.94Hz
PAL interlaced	312.5	50Hz
PAL progressive	625	50Hz

■ Image Input Timing

Horizontal direction Image signal input timing

(1) ITU-R BT.656 style (NTSC/PAL)

This mode extracts timing information from SAV and EAV of pixel data four words, and perform operation control. Because SAV and EAV contain synchronization timing information, encode processing is possible without connecting HSYNC_L and VSYNC_L signals. Figure 5 shows the interface timing. The number of effective pixels is 720 pixels for both NTSC and PAL. For the DDR mode, the CLK number in Table 3 is divided by 1/2.

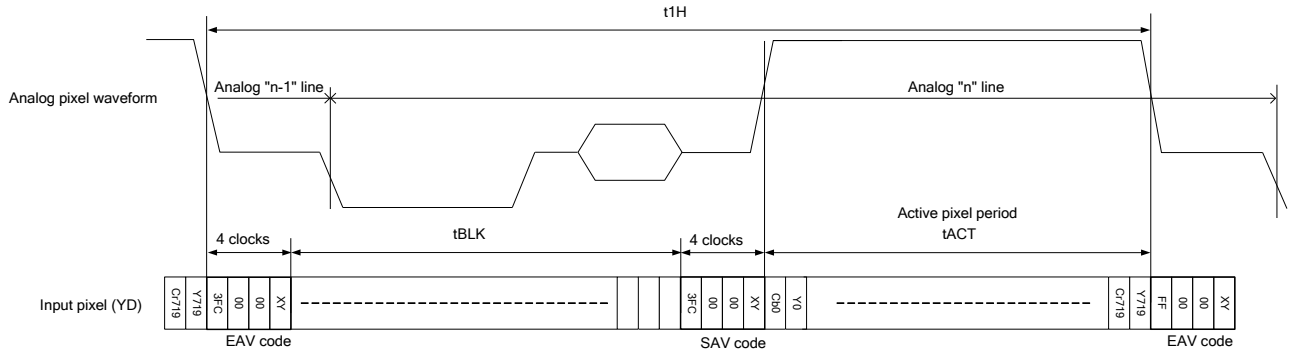


Figure 5: Interface Timing of ITU-R BT.656 Style

Table 3: Specified Values of tBLK, tACT, and t1H (CLK Clock Count)

Video format	tBLK	tACT	t1H
NTSC	268	1440	1716
PAL	280	1440	1728

SAV and EAV information is recognized as 8bit information. Parity information of SAV and EAV is not managed. Make sure the horizontal and vertical synchronization signals, HSYNC_L and VSYNC_L, not to be the OPEN state by conducting "L" level input, etc.

(2) YCbCr 4:2:2 8bit + Synchronization signal Input mode

This mode inputs horizontal and vertical synchronization signals from the HSYNC_L pin and VSYNC_L pin. Input formats supported by this mode are shown in Figure 6. A synchronization signal to input is loaded by synchronizing to the rising edge of CLK. (Note: The CLK polarity of input data loading can be reversed with register setting.)

The valid duration of input pixel data (active video) starts from loading CLK of the horizontal synchronization signal SYNC_L after CLK regulated with tSTA. The valid period is regulated with tACT. tSTA and tACT are regulated for pixel frequencies as shown in Table 4.

For the DDR mode, the CLK number in Table 4 is divided by 1/2.

Table 4: Specified Values of tSTA, tACT, and tFP (CLK Clock Count)

Pixel frequency mode	tSTA	tACT	tFP
NTSC ITU-R BT.601	244	1440	32
PAL ITU-R BT.601	264	1440	24

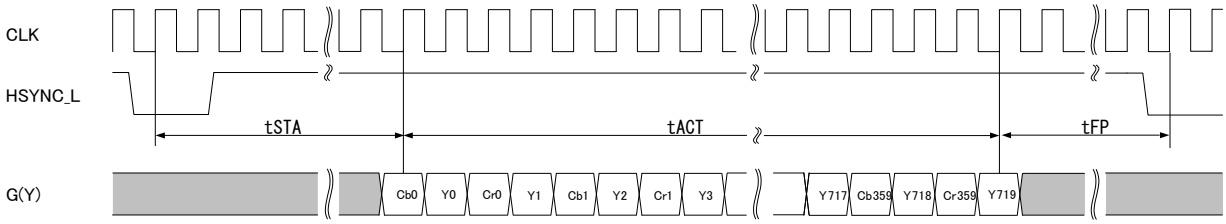


Figure 6: YCbCr 8-bit Multiplex Input

(3) YCbCr 4:2:2 16bit + Synchronization signal / YCbCr 4:4:4 24bit + Synchronization signal / RGB 4:4:4 24bit + Synchronization signal Input mode

This mode inputs horizontal and vertical synchronization signals from the HSYNC_L pin and VSYNC_L pin. Input formats supported by this mode are shown in Figure 7 and 8.

A synchronization signal to input is loaded by synchronizing to the rising edge of CLK. (Note: The CLK polarity of input data loading can be reversed with register setting.)

The valid period of input pixel data (active video period) starts from loading CLK of the horizontal synchronization signal HSYNC_L after CLK regulated with tSTA. The valid period is regulated with tACT. tSTA and tACT are regulated for pixel frequencies as shown in Table 5.

Table 5 : Specified Values of tSTA, tACT and tFP (Clock Count)

Pixel frequency mode	tSTA	tACT	tFP
NTSC ITU-R BT.601	122	720	16
PAL ITU-R BT.601	132	720	12

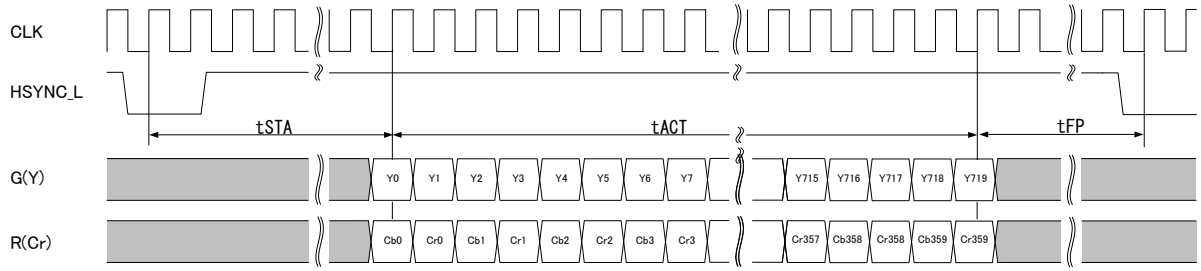


Figure 7：YCbCr 4:2:2 16bit + Synchronization signal Input mode

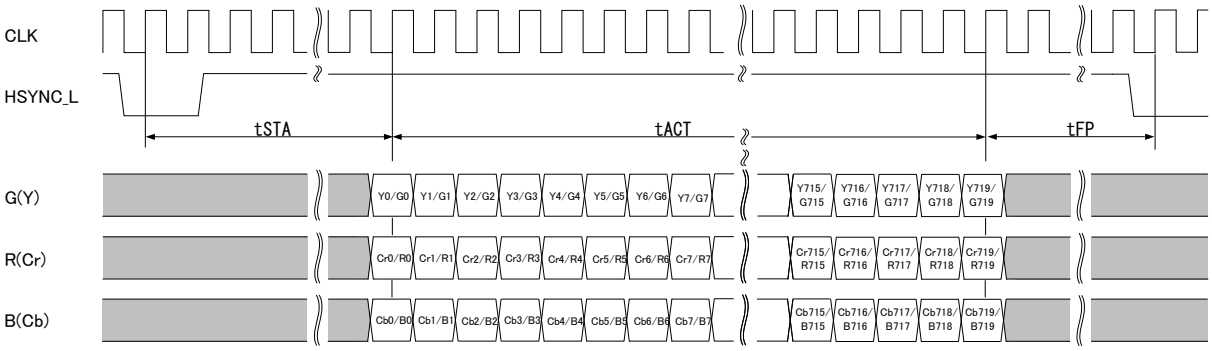


Figure 8：YCbCr 4:4:4 24bit + Synchronization signal / RGB 4:4:4 24bit + Synchronization signal Input mode

Vertical direction Image signal input timing

(1) **Vertical Video Signal Input Timing (NTSC Interlaced)**

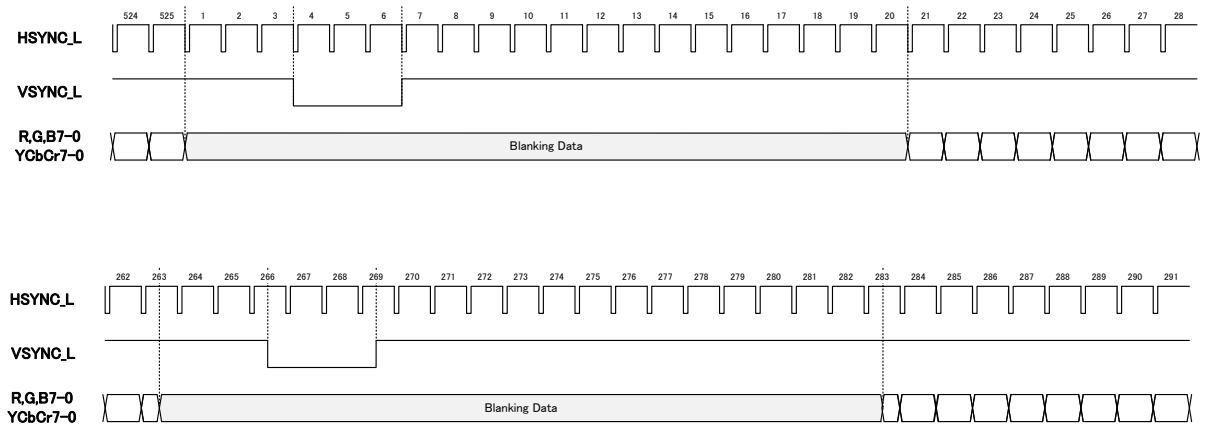


Figure 9: Vertical Video Signal Input Timing (NTSC Interlaced)

(2) Vertical Video Signal Input Timing (PAL Interlaced)

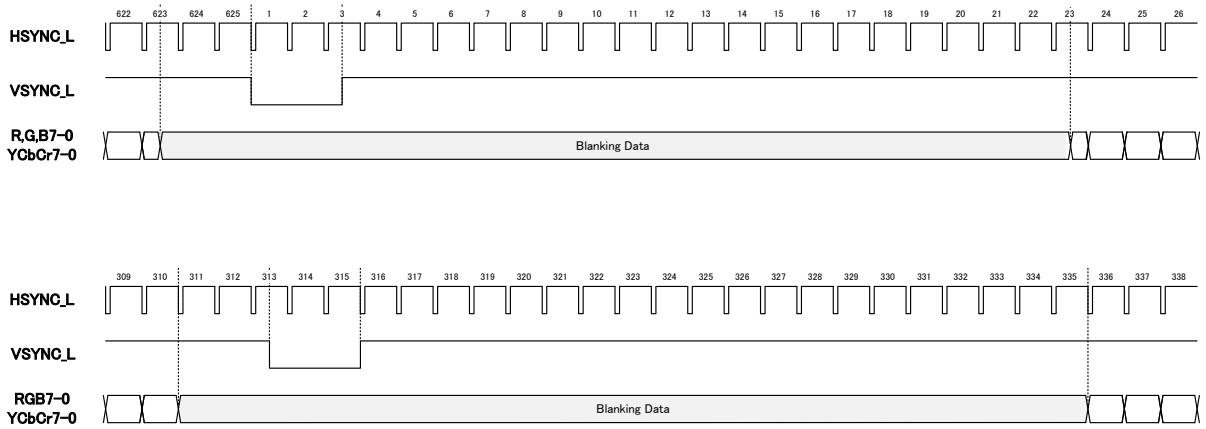


Figure 10: Vertical Video Signal Input Timing (PAL Interlaced)

(3) **Vertical Video Signal Input Timing (NTSC Progressive)**

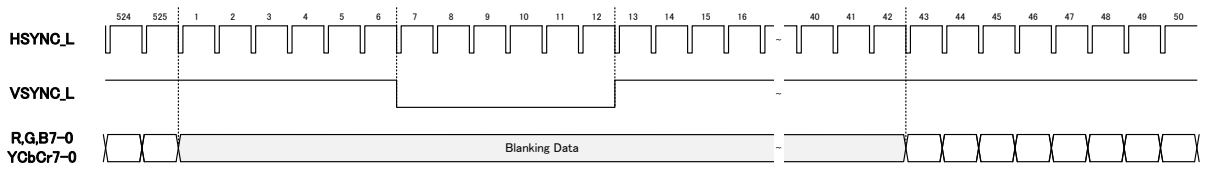


Figure 11: Vertical Video Signal Input Timing (NTSC Progressive)

(4) Vertical Video Signal Input Timing (PAL Progressive)

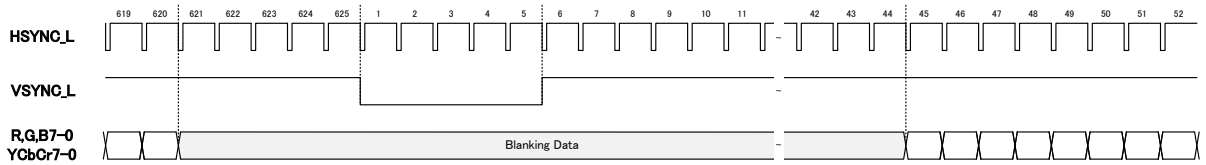


Figure 12: Vertical Video Signal Input Timing (PAL Progressive)

■ Image Input Format Setting

Image input timing described up to the previous section and image input format are set with the internal register. Default setting after resetting is progressive RGB 4:4:4 24bit + synchronization signal input mode. A data input port can be changed from the internal register (PORT_CHG) setting. Fix to "L" or "H" level for the pins not used in each input format. The register setting of each image input timing is shown in Table 6.

Table 6 : Settings of Image Input Format

					#00h[4]	#00h[3]	#00h[2]	#01h[2]	#01h[1]	#01h[0]
Scanning method	Data type	Bit width	Chroma Sampling rate	Input CLK frequency [MHz]	DDRMOD	MLTDAT	IMODSEL2	I444SEL	IRGBSEL	IPRGSEL
Interlace	ITU-R BT.BT.656-4 style	8bit	4:2:2	27MHz	0	0	1	0	0	0
	YCbCr 4:2:2 8bit +sync signal	8bit	4:2:2	27MHz	0	1	1	0	0	0
	ITU-R BT.BT.656-4 style (DDR)	8bit	4:2:2	13.5MHz	1	0	1	0	0	0
	YCbCr 4:2:2 8bit + sync signal (DDR)	8bit	4:2:2	13.5MHz	1	1	1	0	0	0
	YCbCr 4:2:2 16bit + sync signal	16bit	4:2:2	13.5MHz	0	0	0	0	0	0
	YCbCr 4:4:4 24bit + sync signal	24bit	4:4:4	13.5MHz	0	0	0	1	0	0
	RGB 4:4:4 24bit + sync signal	24bit	4:4:4	13.5MHz	0	0	0	1	1	0
Progressive	ITU-R BT.BT.656-4 style	8bit	4:2:2	54MHz	0	0	1	0	0	1
	YCbCr 4:2:2 8bit +sync signal	8bit	4:2:2	54MHz	0	1	1	0	0	1
	ITU-R BT.BT.656-4 style (DDR)	8bit	4:2:2	27MHz	1	0	1	0	0	1
	YCbCr 4:2:2 8bit + sync signal (DDR)	8bit	4:2:2	27MHz	1	1	1	0	0	1
	YCbCr 4:2:2 16bit + sync signal	16bit	4:2:2	27MHz	0	0	0	0	0	1
	YCbCr 4:4:4 24bit + sync signal	24bit	4:4:4	27MHz	0	0	0	1	0	1
	RGB 4:4:4 24bit + sync signal	24bit	4:4:4	27MHz	0	0	0	1	1	1

*Fix to "L" or "H" level for the pins not used in each input format, and make sure they do not become OPEN.

Settings of Changing Data Input Port

#00h[7:6]	Input Terminal		
PORT_CHG	G	R	B
00	G/Y	R/Cr	B/Cb
01	R/Cr	B/Cb	G/Y
10	B/Cb	R/Cr	G/Y
11	R/Cr	G/Y	B/Cb

■ Input Data Level

In this section, selection of the input data level on YCbCr and RGB, and data format of CbCr (complementary number of offset binary, 2) are described.

(1) Data Level of YCbCr Input (ITU-R BT.601)

For the input level, input a level regulated with ITU-R BT.601 in 8-bit. The input level range is shown in Figure 13.

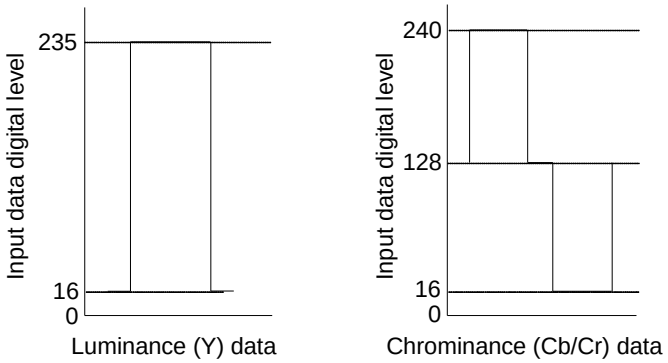


Figure 13: 8-bit YCbCr Input Level Range

Input data are clipped in the value range shown next.

8-bit data

Luminance data: When Y > 235, clip to Y = 235
When Y < 16, clip to Y = 16

Color difference data: When C > 240, clip to C = 240
When C < 16, clip to C = 16

For the color difference data format, the offset binary format and complementary number 2 format can be selected by specifying the internal register IN2S.

Table 7: IN2S Register Functions

#01h[6] IN2S	Function
0	Offset binary format(default)
1	2’s complement format

(2) Data Level of YCbCr Input (Extended Luminance Range Mode)

The extended luminance range mode can manage Y = 1 (8-bit) for the lower limit of luminance data range, and Y = 254 (8-bit) for the upper limit. To set the extended luminance range mode, set the internal register SBON to "1". In the extended luminance range, the clipping range of input data is extended as follows.

8-bit data

Luminance data: When Y > 254, clip to Y = 254
When Y < 1, clip to Y = 1

Color difference data: When C > 240, clip to C = 240
When C < 16, clip to C = 16

Table 8: SBON Register

#03h[4] SBON	Function
0	ITU-R BT.601 renge(default)
1	Extended luminance range

Examples for inputting Y = 1 and Y = 16 as the input luminance signal are shown in Figure 18. When the extended luminance range mode is not applied, the output luminance level is output as black level 0 as shown in Figure 14-A, because the luminance signal is clipped as Y = 16. On the other hand, when the extended luminance range mode is applied, Y = 1 can be output as a signal with the black level or less (super black level) as shown in Figure 14-B.

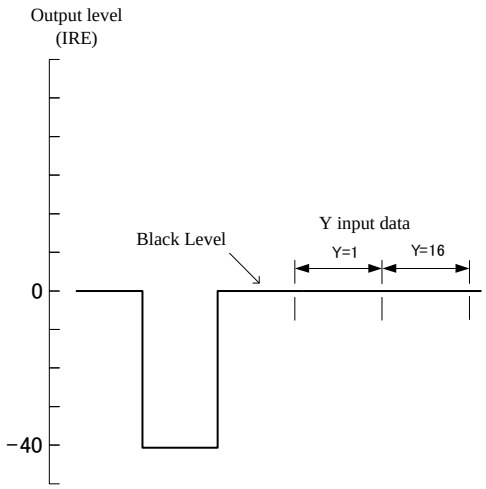


Figure 14-A: Not Applying the Extended Luminance Range

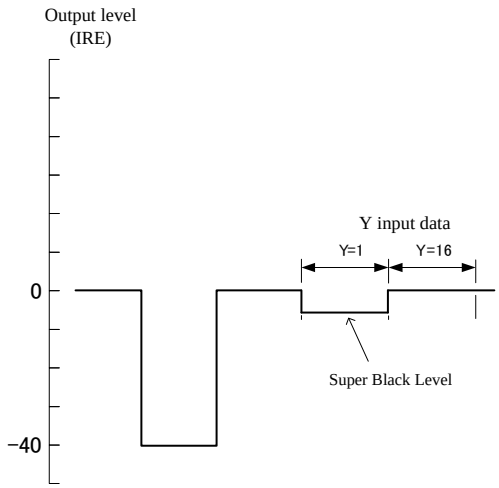


Figure 14-B: Applying the Extended Luminance Range

Next, examples for inputting Y = 254 and Y = 235 as the input luminance signal are shown in Figure 15. When the extended luminance range mode is not applied, the output luminance level is output as black level, because the luminance signal is clipped as Y = 235. On the other hand, when the extended luminance range mode is applied, Y = 254 can be output as a signal with the white level or more (super white level) as shown in Figure 15-B.

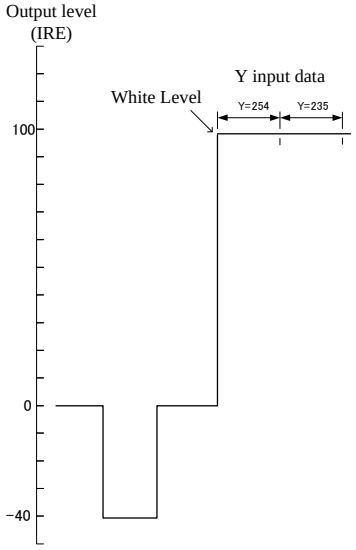


Figure 15-A: Not Applying the Extended Luminance Range

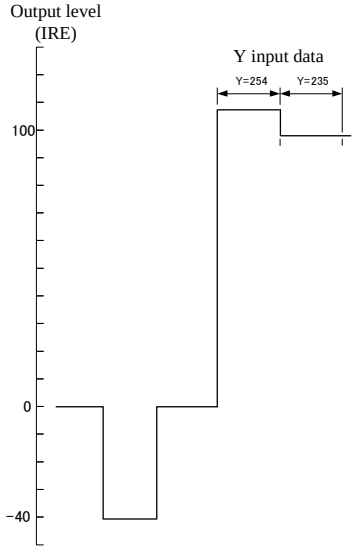


Figure 15-B: Applying the Extended Luminance Range

(3) RGB Input Data Level

The input data level range can be selected from two types of level ranges, the full scale (0 to 255) or level range (16 to 235) regulated with ITU-R BT.601. The level range selection is set with the internal register RGBLEV.

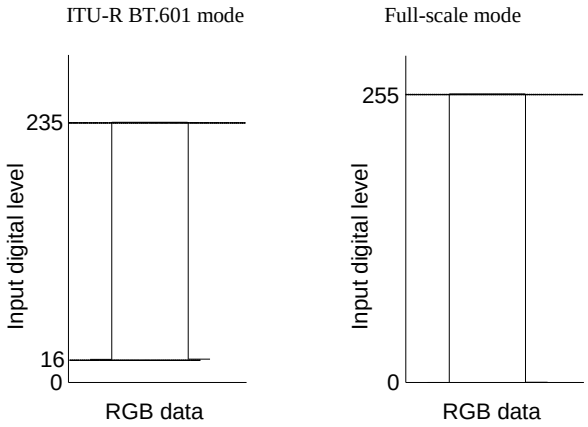


Figure 16: Level range of 8-bit RGB input

Table 9: RGBLEV Register Functions

#03h[3] RGBLEV	Function
0	Full-scale mode(default)
1	ITU-R BT.601 mode

When input data in the ITU-R BT.601 mode are the following values, they are clipped in the range shown next.

8-bit data

When RGB data > 235 Clip to RGB = 235
When RGB data < 16 Clip to RGB = 16

■ Video Output Level

（1）Composite NTSC Setup 0.0IRE

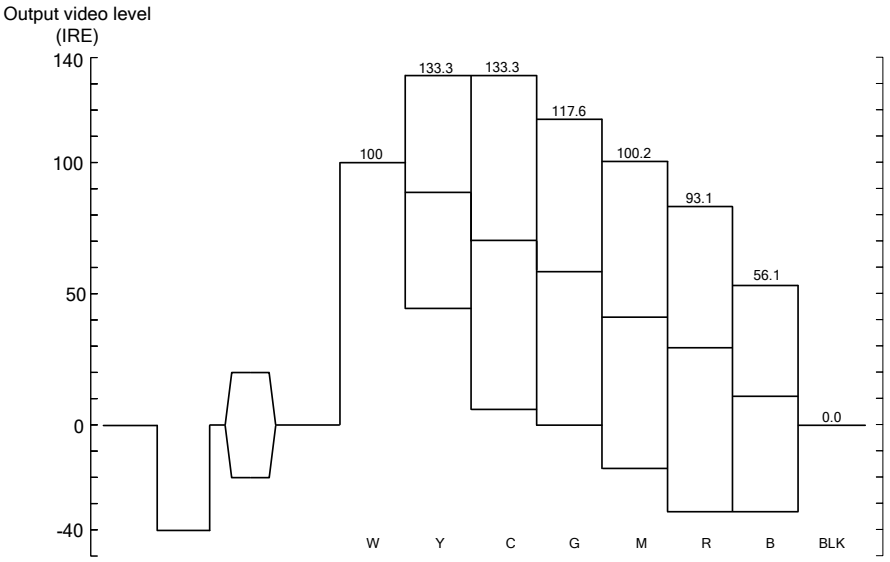


Figure 17: NTSC Composite Video Output Level (Setup 0.0IRE)

（2）Composite NTSC Setup 7.5IRE

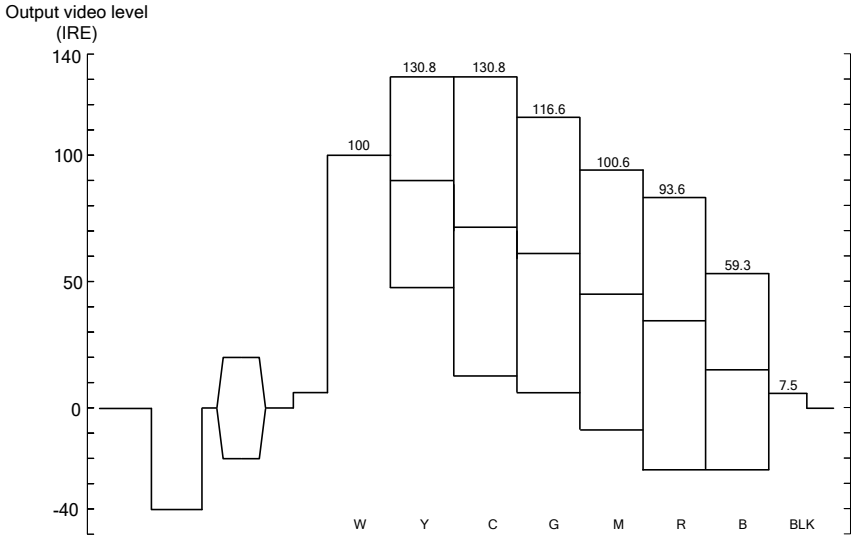


Figure 18: NTSC Composite Video Output Level (Setup 7.5IRE)

（3）Composite PAL

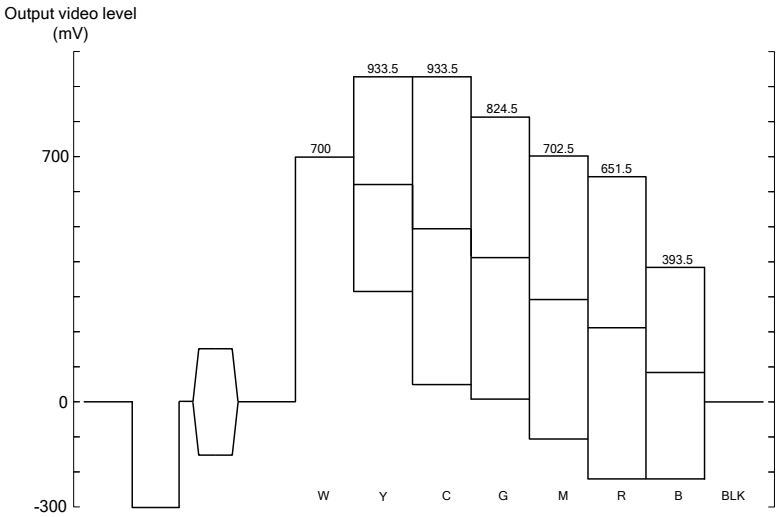
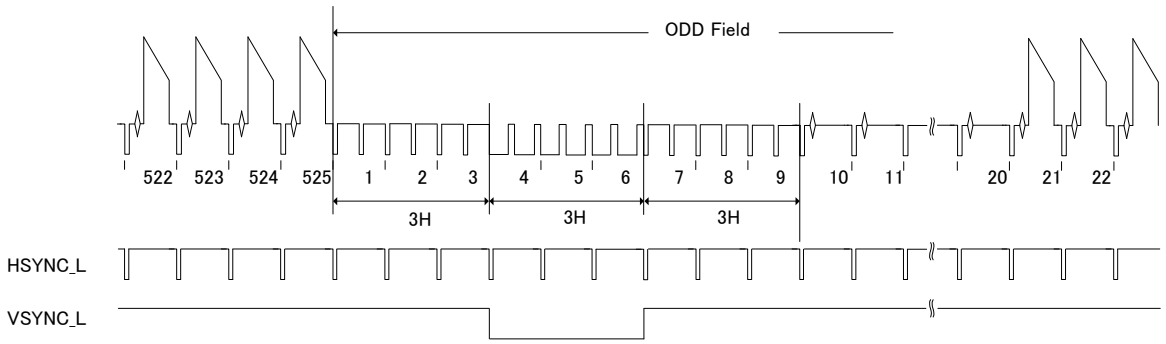


Figure 19: PAL Composite Video Output Level

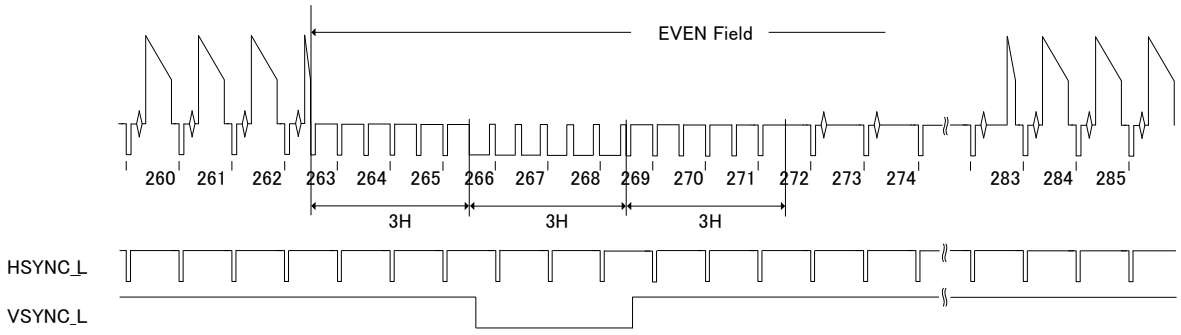
■ Video Interface Timing

Vertical Blanking Period Waveform

（1） Composite NTSC Interlace Output



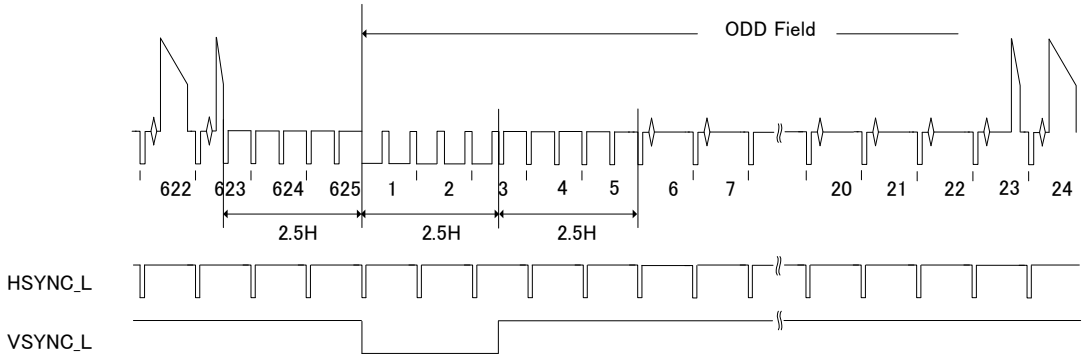
[Even Number Field → Odd Number Field]



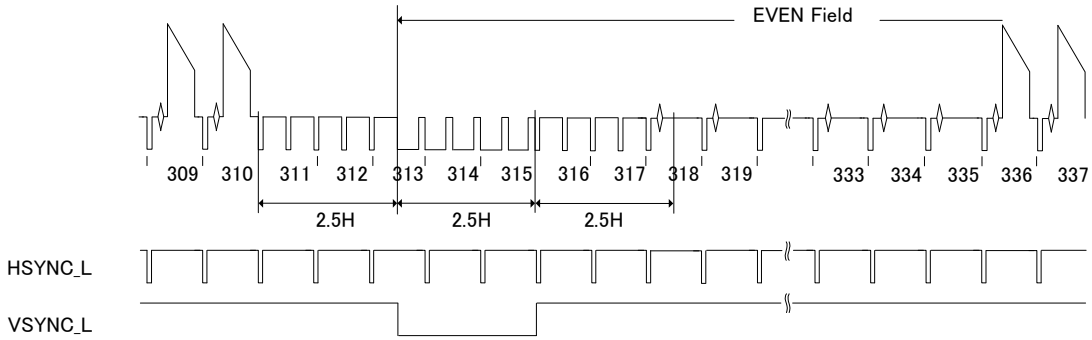
[Odd Number Field → Even Number Field]

Figure 20: Waveforms of a Vertical Blanking Period at Composite NTSC Interlace Output

(2) Composite PAL Interlace Output



[Even Number Field → Odd Number Field]

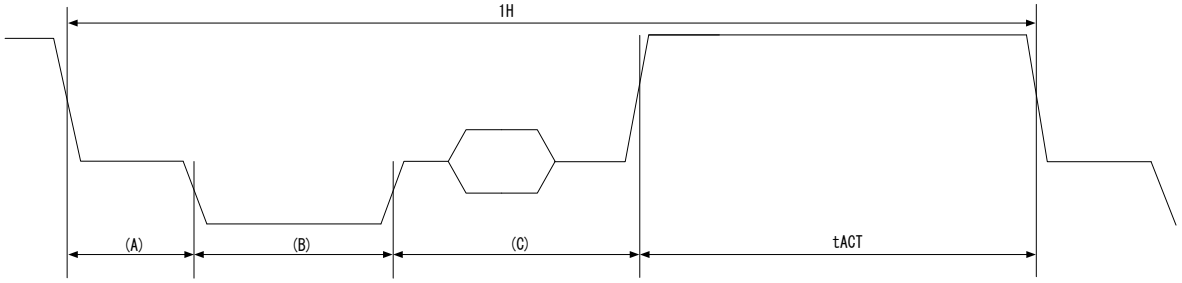


[Odd Number Field → Even Number Field]

Figure 21: Waveforms of a Vertical Blanking Period at Composite PAL Interlace Output

Horizontal Blanking Period Waveform

Figures 22 and Table 10 show the specifications of horizontal blanking waveforms of composite signals.



(A): Front porch (B): H sync (C): Back porch

Figure 22: H Blank Period of Composite Signals

Table 10: Pixel Clock Counts during Horizontal Blank Period

Pixel frequency mode	(A)	(B)	(C)
NTSC ITU-R BT.601	16	63	59
PAL ITU-R BT.601	12	63	69

■ Description of Operation

● P/I Conversion Control
Progressive to Interlace Conversion Function

ML86640 performs P/I conversion on a progressive input signal (YCbCr and RGB), and output as an interlace image. For conversion to an interlace image, an odd number field uses the odd number line of progressive input data, and an even number field uses the even number line of progressive input data.

Table 11: P/I Conversion

#01h[0] IPRGSEL	P/I Conversion
0	Not performed
1	Performed (default)

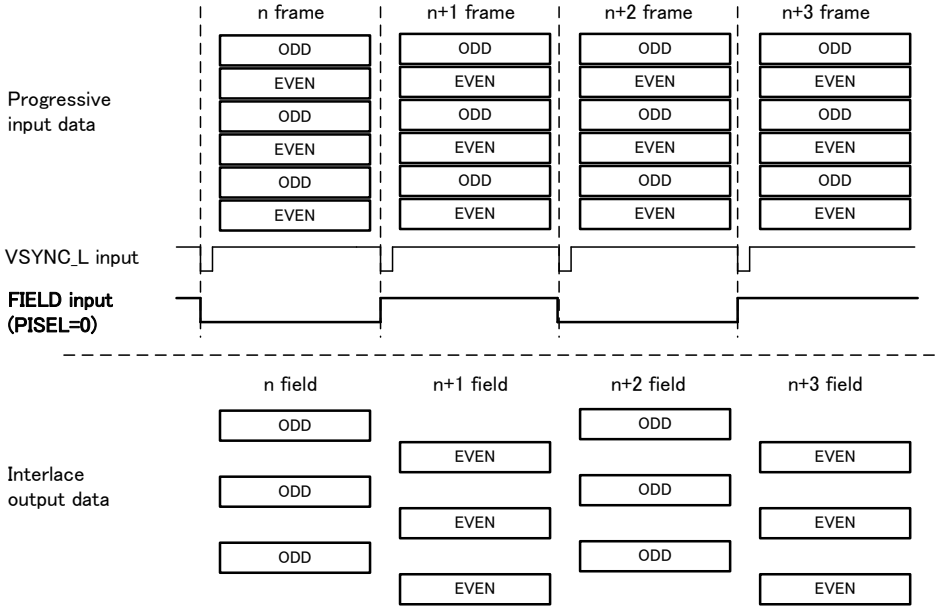
Also, by setting Register #02h/bit[6](PIFLD) = "1", an odd number/even number line of input progressive image used for output interlace signals can be specified from the field information input from the FIELD pin. Output image is generated from the odd number line when the FIELD signal is "L", and from the even number line when the FIELD signal is "H" (From the setting of Register #02h/bit[5](PISEL), logic reversion of the FIELD signal is possible). For the FIELD signal, input by toggling each frame of progressive input.

*Except for the cases of FIELD signal output enabled (#02h/bit[7](FLDEN)=1), input "L" or "H" in the FIELD pin, and make sure it does not become OPEN.

Table 12: FIELD signal input

#02h[6] PIFLD	FIELD signal input
0	Disable(default)
1	Enable

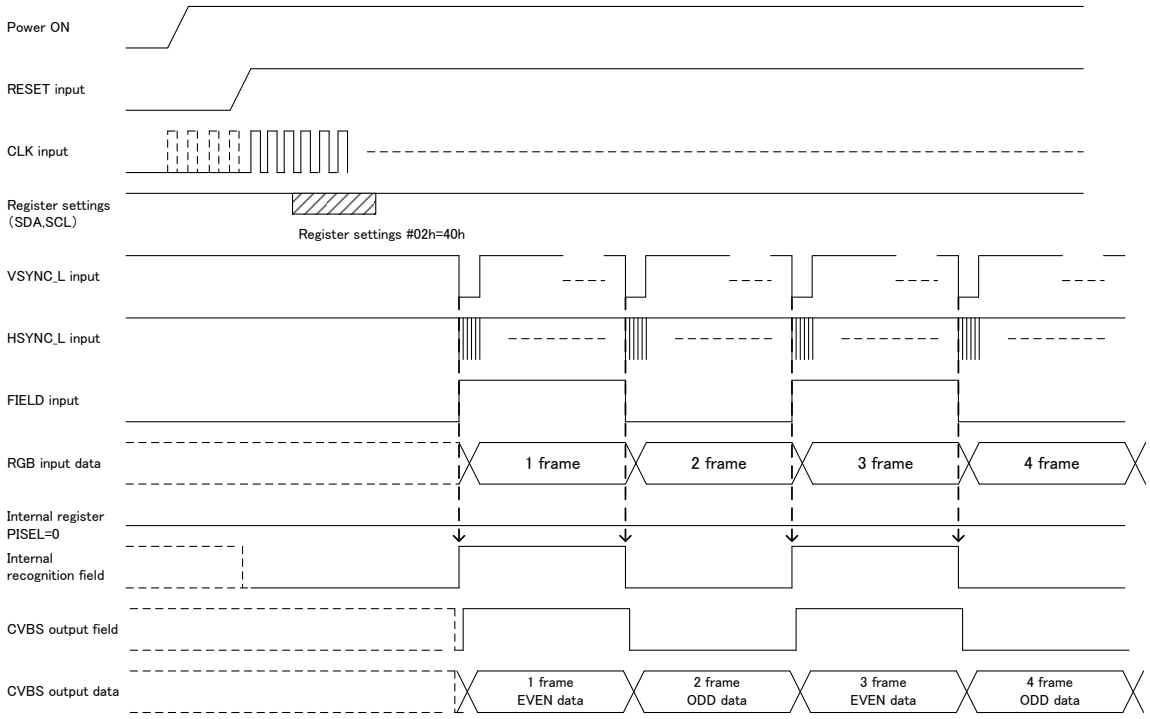
P/I conversion operation figure when the FIELD signal input enabled



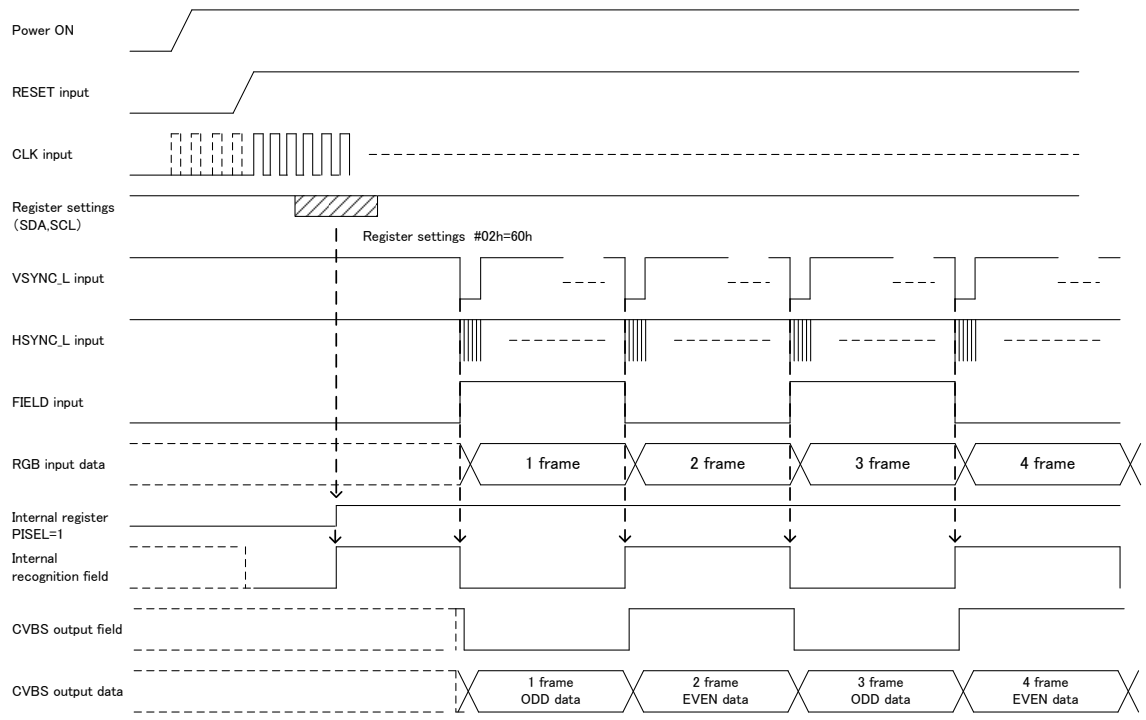
P/I Conversion Operation Start Sequence

P/I conversion operation starts with VSYNC_L falling after releasing reset as standard.

1. PIFLD = 1 and PISEL = 0 (Setting example: NTSC progressive, RGB 4:4:4 24bit + synchronization signal input mode)

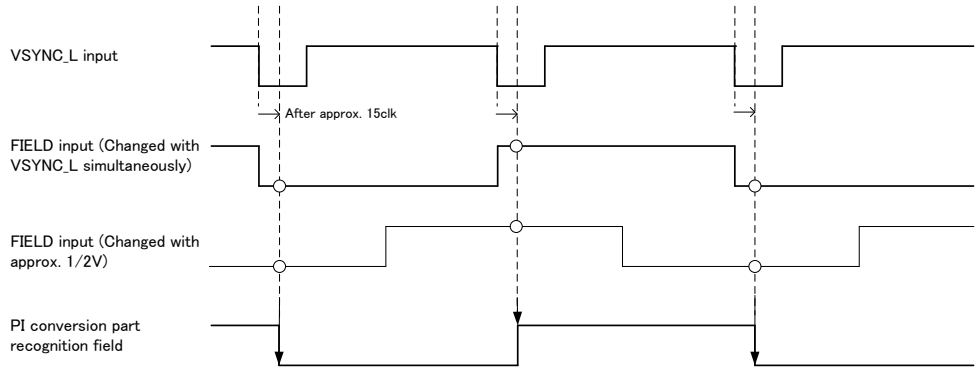


2. PIFLD = 1 and PISEL = 1 (Setting example: NTSC progressive, RGB 4:4:4 24bit + synchronization signal input mode)



FIELD Signal Input Timing

The FIELD signal to reflect on P/I conversion operation loads logic after approx. 15 CLK cycles with the falling edge of VSYNC_L input as the starting point. FIELD signal logic reversion is possible with Register #02h/bit[5](PISEL).

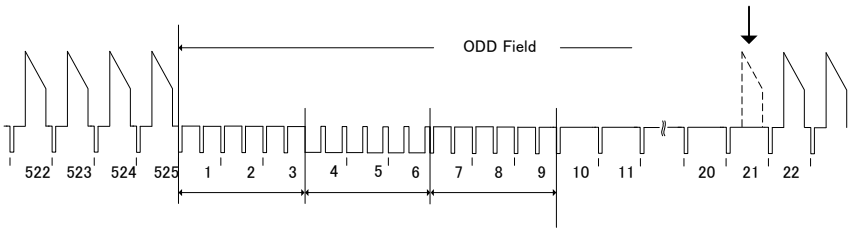


Waveform of a Vertical Blanking Period at NTSC or PAL Interlace Conversion Output

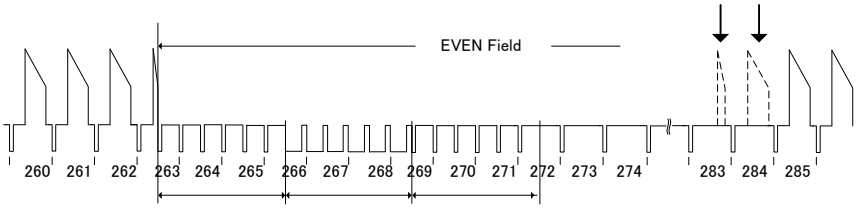
The valid number of lines in interlace scan mode of the ML86640conforms to the Standard [ITU-R BT.601] (NTSC : 242.5H, PAL : 287.5H). However, the valid number of lines decreases from the number defined in the Standard [ITU-R BT.601] as a result of P/I conversion due to the P/I conversion algorithm.

（1） Waveform of a Vertical Blanking Period after NTSC P/I Conversion

In NTSC mode, the valid data that is output includes odd number fields of 241.5H, which are one line less at the top end and even number of fields of 241H, which are 1/2 line + 1 line less at the top end. The valid data that is indicated by the dotted lines in the diagram are deleted.



[Even Number Field → Odd Number Field]

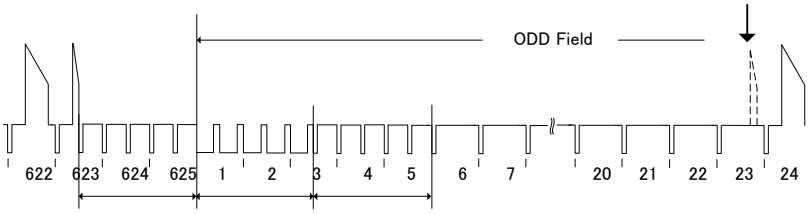


[Odd Number Field → Even Number Field]

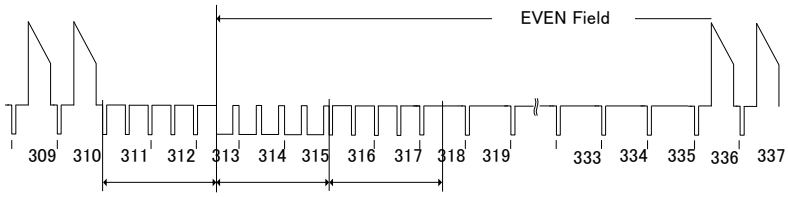
Figure 23: Waveform of an NTCS Interlace Vertical Blanking Period after P/I Conversion

(2) Waveform of a Vertical Blanking Period after PAL P/I Conversion

In PAL, even number of fields of 287H, which is one line less on the top (1/2H line) and even number of fields of 287.5H are output as valid data. The valid data that is indicated by the dotted lines in the diagram is deleted.



[Even Number Field → Odd Number Field]



[Odd Number Field → Even Number Field]

Figure 24: Waveform of a PAL Interlace Vertical Blanking Period after P/I Conversion

● Standby mode

A standby mode is controlled by STANDBY register. During the standby mode, consumption current can be reduced, because internal DAC powers down and DAC output becomes zero output. During the standby mode, internal register can be also accessed.
When setting DAC output to zero output only, set the internal register MUTE.

Table 13: STANDBY register function

#0Fh[0] STANDBY	Function
0	Normal operation (default)
1	Standby operation

● Mute mode

MUTE register is a function to set digital signals to DAC to ALL "0", and perform zero output from DAC.

Table 14: MUTE register function

#0Fh[1] MUTE	Function
0	Normal operation (default)
1	MUTE operation

● Image no-input mode

When an image signal/synchronization signal is not input to the encoder, a synchronization signal is generated inside the encoder to make the encoder itself enable to output an image signal. An image signal that can be output can be selected from blueback, color bar, and black level output.
Note: When #00h/bit[3:2]=01(ITU-R BT.656 style), this setting is not valid.

Table 15: NOSIG register function

#08h[7] NOSIG	Function
0	Normal mode (default)
1	Image no-input mode

● Closed Caption (CC)

The Closed caption (CC) function based on the EIA-608 Standard can be used. Each line caption information is multiplexed as 26-cycle signals that are synchronized with 503 kHz. Each cycle is described below.

1 to 7 cycles
Clock run-in period: Clock signal for caption data to synchronize with caption information
8 to 10 cycles
Start code: Fixed signal of logical level "001"
11 to 26 cycles
Caption information: Two sets (2 bytes) of multiplex information formed by combining an ASCII code of bits 0-6 and an odd number parity bit of bit 7. The first byte is multiplexed by 11 to 18 cycles and the second byte is multiplexed by 19 to 26 cycles with LSB first.

Closed caption encoding function

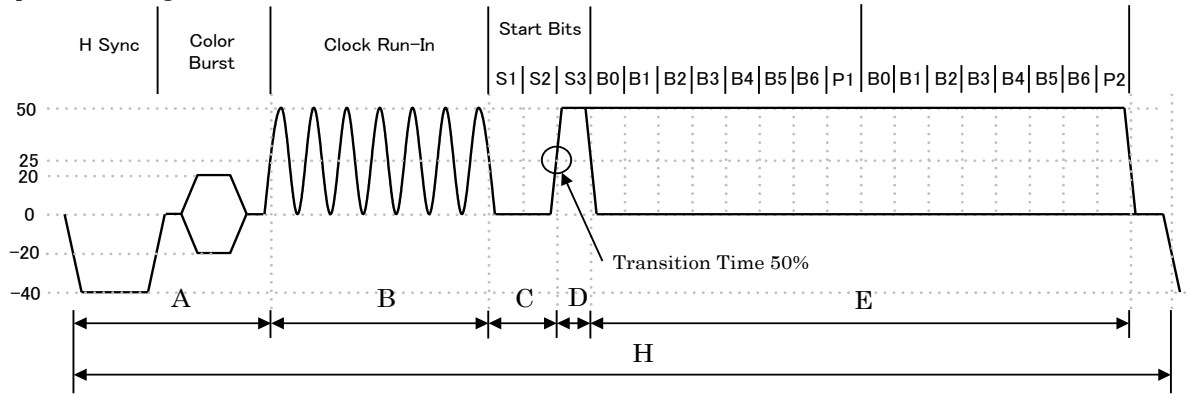


Figure 25: CC Encode Waveform

A: (H Sync To Clock Run-in) …10.500µS
B: (Clock Run-in) …12.910µS
C: (Clock Run-in to Start Bit) … 3.972µS
D: (Data Bit) … 1.986µS
E: (Data Characters) …31.778µS
H :(Horizontal Line) …63.556µS

Data Bit High
Clock Run-in Maximum …50IRE
Data Bit Low
Clock Run-in Minimum …0IRE
Data Bit Differential
Clock Run-in Differential …50IRE

*Signals in PAL are also output in the same timing.

Closed caption control registers

CC function ON/OFF	CCEN[1:0]	
	CCEN[0]	1: Odd number field On, 0: Off
	CCEN[1]	1: Even number filed On, 0: Off
Line select	CCLN[4:0]	4 to 35, 267 to 298 line(NTSC) *Default lines 21,284 5 to 36, 318 to 349 lines (PAL) *Default lines 22,335
Closed caption data	CCODT0[7:0]	Odd first byte data
	CCODT1[7:0]	Odd second byte data
	CCEDT0[7:0]	Even first byte data
	CCEDT1[7:0]	Even second byte data
Caption data status	CCSTAT[1:0]	
(Read only register)	CCSTAT[0]	Odd CC data status
	CCSTAT[1]	Even CC data status 1: Termination of register write operation from external section (CC data enable) 0: End of data encoding (0x80 data output)

Usage:
Updating of closed caption data is assumed when data is written to CCOD0 and CCOD1 in the case of odd number fields and CCED0 and CCED1 in the case of even number fields. When the data is updated (CCSTAT=1), the data is encoded in the specified line that is subsequently forwarded. When the data is not updated (CCSTAT=0), 80h code is output and the parity bit at closed caption data multiplexing is prepared by the host.

● Copy Generation Management System (CGMS)

The copy generation management system corresponds to the encoding function of CGMS information. When the input video signal is in NTSC, information is superimposed on lines 20 and 283 of the vertical blanking period. CGMS data comprises a total of 20 bits, namely, 14-bit data of Word 0 to 2 and 6-bit data of CRCC. Tables 16-1 to 16-2 show the contents of each data bit.
Two modes for setting CRCC data are available, a mode where CRCC data is generated automatically by calculation based on polynomial X6+X+1 and a mode where a CRCC data value is directly specified. To specify a CRCC data value directly, set the internal register CRCON to "1".

Table 16-1: Word0 Infromation (bits 0 to 5)

bit	Value	Function
bit 0	0	Accept ratio 4:3
	1	Accept ratio 16:9
bit 1	0	Display format: Normal
	1	Display format: Letter box
bit 2	Undefined	
bits 5:3	ID signals of video, audio, etc.	

Table 16-2: Word1 and 2 Infromation (bit 6 to 13)

bit	Function
bits 9:6	ID signal associated with Word0
bits 13:7	ID signal and information associated with Word0

To enable the CGMS function, set the following registers.

Table 17: CGMSEN Register Functions

#16h[7] CGMSEN	Function
0	CGMS disabled(default)
1	CGMS enabled

Table 18: CRCON Register Functions

#18h[7] CRCON	Function
0	Automatic generation mode in CRC data (default)
1	User specified mode of CRC data

[Register name]:CRCDATA [Register address]: #18h bit [5:0]
[Function]: Register for storing the CRC data that is specified by the user.
[Initial value]: 0h

Figure 26 shows the CGMS waveform at interlace output.

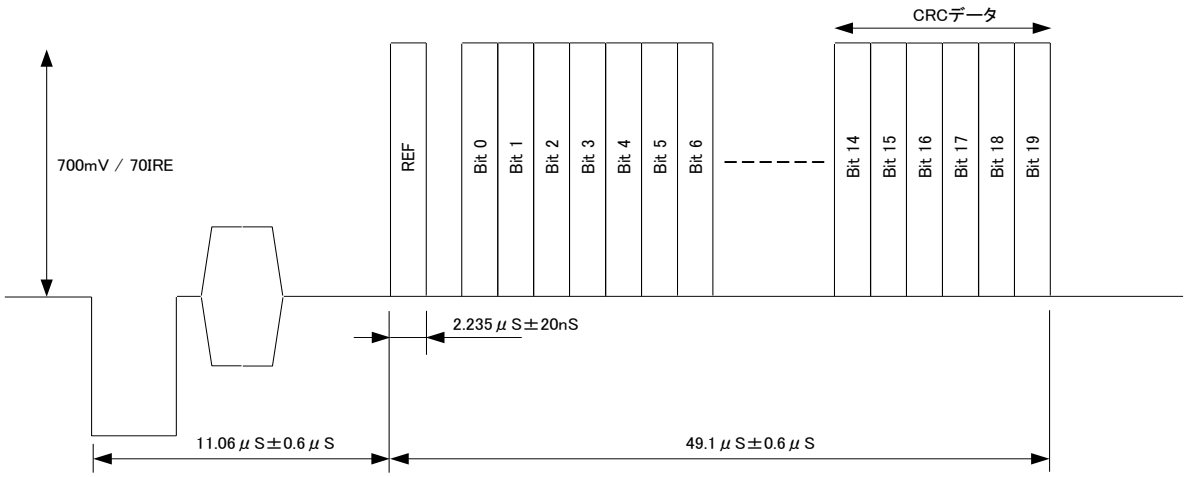


Figure 26: CGMS Waveform at Interlace Output

● Wide Screen Signaling (WSS)

This function corresponds to the encoding function of wide screen signaling (WSS) that superimposes accept ratio determination information and title information. The function superimposes the information on line 23 of the vertical blanking period only when the input video signal is in PAL. The WSS data is 14-bit data. Tables 19-1 to 19-4 show the contents of each data bit.

Table 19-1: Accept Ratio Information (bits 0 to 3)

bit	Value	Function
bit4	0	Camera mode
	1	Film mode
bit 5	0	Standard coding
	1	Movement application type color plus
bit 6	0	No helper
	1	Modulated helper
bit 7	0	Reserved
	1	Reserved

Table 19-2: PALplus Related Information (bits 4 to 7)

bit	Value	Function
bit4	0	Camera mode
	1	Film mode
bit 5	0	Standard coding
	1	Movement application type color plus
bit 6	0	No helper
	1	Modulated helper
bit 7	0	Reserved
	1	Reserved

Table 19-3: Subtitle Information (bits 8 to 10)

bit	Value	Function
bit 8	0	Without TeleText subtitles
	1	With TeleText subtitles
bit 9:10	00	Without subtitles
	10	With subtitles on the screen
	01	With subtitles on the lower side (or upper side) of the screen
	11	Reserved

Table 19-4: Sound Surround Information (bit 11)

bit	Value	Function
bit 11	0	Without sound (surround) information
	1	With sound (surround) information

bits 12 to 13: Reserved

To enable the WSS function, set the WSSEN register to “1”.

Table 20: WSSEN Register Functions

#1Ah[7] WSSEN	Function
0	WSS disabled(default)
1	WSS enabled

Figure 27 shows the WSS waveform.

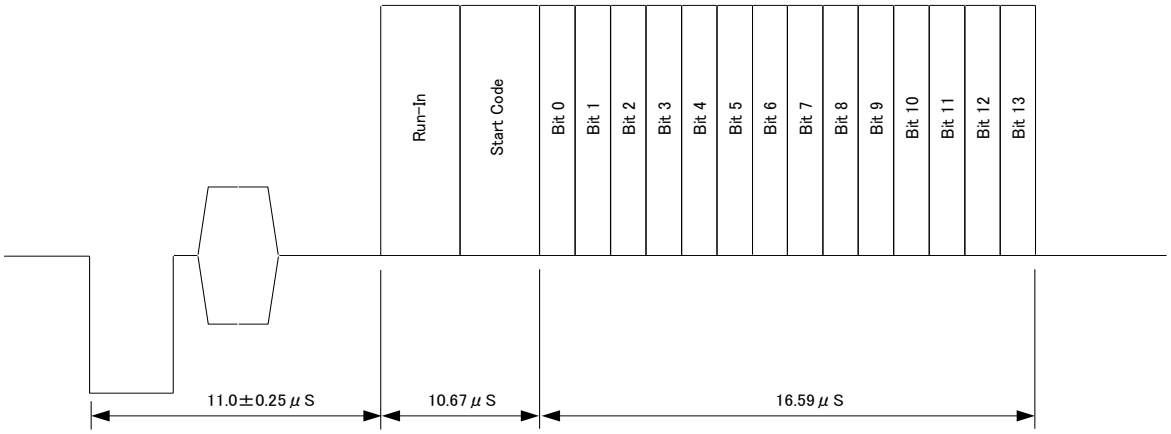


Figure 27: WSS Waveform

■ Function of Registers

Register of ML86640 performs control with I^2C bus. Various function changes such as image quality adjustment, mode switching, etc. are possible by conducting register control.

For the register address, #00-#3F are assigned as the sub-address of I^2C bus. A part of register is Read only.
Do not write data except for the default values for the register address without explanation.

Each register is explained in the order of addresses in the next section.
A register value with "*" or "(default)" denotes a default value.

■ Register Map

Set internal registers using the I^2C interface.

Table 21: Register Map

Sub Adress	W/R	Register Name								Initial Value
		BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
#00h	W/R	PORT_CHG		BIT_CHG	DDRMOD	MLTDAT	IMODSEL2	-		00h
#01h	W/R	-	IN2S	-		NPSEL	I444SEL	IRGBSEL	IPRGSEL	07h
#02h	W/R	FLDEN	PIFLD	PISEL	NEGCK	-				00h
#03h	W/R	CBON	BBON	BLON	SBON	RGBLEV	SETUP	OUTLEV[1:0]		03h
#04h	W/R	-			CLEV	-				00h
#05h	W/R	-								00h
#06h	W/R	-				BLKADJ				08h
#07h	W/R	-								00h
#08h	W/R	NOSIG	-							00h
#09h	W/R	CVBSGAINY								80h
#0Ah	W/R	CVBSGAINC								80h
#0Bh	W/R	-								00h
#0Ch	W/R	-								00h
#0Dh	W/R	-						APEN[1:0]		00h
#0Eh	W/R	-								00h
#0Fh	W/R	-						MUTE	STANDBY	00h
#10h	W/R	CCEN [1:0]		-	CCLN [4:0]					11h
#11h	W/R	CCOD0 [7:0]								00h
#12h	W/R	CCOD1 [7:0]								00h
#13h	W/R	CCED0 [7:0]								00h
#14h	W/R	CCED1 [7:0]								00h
#15h	R Only	-						CCSTAT [1:0]		03h
#16h	W/R	CGMSEN	-	WD01 [5:0]						00h
#17h	W/R	WD02 [7:0]								00h
#18h	W/R	CRCON	-	CRCDATA[5:0]						00h
#19h	W/R	GP12 [7:0]								00h
#1Ah	W/R	WSSEN	-	GP34[5:0]						00h
#1Bh	W/R	reserved								00h
～	W/R									00h
#1Fh	W/R									00h
#20h	R Only									FFh
～	R Only									FFh
#39h	R Only									FFh
#3Ah	R Only									86h
#3Bh	R Only									64h
#3Ch	W/R									x0h
#3Dh	W/R									00h
#3Eh	W/R									80h
#3Fh	W/R									00h

“Reserved” in Sub addresses 1B to 3F indicates the reserved registers for the system. Do not use these registers.

Function of Registers

● **Sub Address #00h / Input Mode Control1 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial Value
#00h	PORT_CHG		BIT_CHG	DDRMOD	MLTDAT	IMOD SEL2	-		00h

#00h/bit[7:6] PORT_CHG
Selects the digital video input port.

"00" : G pin : Y/G, R pin : Cr/R, B pin : Cb/B (default)
"01" : G pin : Cr/R, R pin : Cb/B, B pin : Y/G
"10" : G pin : Cb/B, R pin : Cr/R, B pin : Y/G
"11" : G pin : Cr/R, R pin : Y/G, B pin : Cb/B

#00h/bit[5] BIT_CHG
Swaps MSB-LSB of the digital video input port.

"0" : Normal (default)
"1" : Swap MSB-LSB

#00h/bit[4] DDRMOD
Enables double data rate input. The supported modes are ITU-R BT.656 or YCbCr 4:2:2 8bit + Synchronization signal input mode.

"0" : Single data rate (default)
"1" : Double data rate

#00h/bit[3], MLTDAT
When input data are 8bit, select ITU-R BT.656 input or YCbCr 4:2:2 8bit + Synchronization signal input mode.
For the setting list of image input formats, refer to Table 22.

0 : Selects the ITU-R BT.656 style input (default)
1 : Selects the YCbCr 4:2:2 8bit + Synchronization signal input

#00h/bit[2], IMODSEL2
Input interface setting register.
For the setting list of image input formats, refer to Table 22.

0 : YCbCr 4:2:2 16bit + Synchronization signal or YCbCr/RGB 4:4:4 24bit + Synchronization signal (default)
1 : YCbCr BT.656 or YCbCr 4:2:2 8bit + Synchronization signal

#00h/bit[1:0]
Set to “00”.

Table 22 : Settings of Image Input Format

Scanning method	Data type	Bit width	Chroma Sampling rate	Input CLK frequency [MHz]	#00h[4] DDRMOD	#00h[3] MLTDAT	#00h[2] IMODSEL2	#01h[2] I444SEL	#01h[1] IRGBSEL	#01h[0] IPRGSEL
Interlace	ITU-R BT.BT.656-4 style	8bit	4:2:2	27MHz	0	0	1	0	0	0
	YCbCr 4:2:2 8bit +sync signal	8bit	4:2:2	27MHz	0	1	1	0	0	0
	ITU-R BT.BT.656-4 style (DDR)	8bit	4:2:2	13.5MHz	1	0	1	0	0	0
	YCbCr 4:2:2 8bit + sync signal (DDR)	8bit	4:2:2	13.5MHz	1	1	1	0	0	0
	YCbCr 4:2:2 16bit + sync signal	16bit	4:2:2	13.5MHz	0	0	0	0	0	0
	YCbCr 4:4:4 24bit + sync signal	24bit	4:4:4	13.5MHz	0	0	0	1	0	0
	RGB 4:4:4 24bit + sync signal	24bit	4:4:4	13.5MHz	0	0	0	1	1	0
Progressive	ITU-R BT.BT.656-4 style	8bit	4:2:2	54MHz	0	0	1	0	0	1
	YCbCr 4:2:2 8bit +sync signal	8bit	4:2:2	54MHz	0	1	1	0	0	1
	ITU-R BT.BT.656-4 style (DDR)	8bit	4:2:2	27MHz	1	0	1	0	0	1
	YCbCr 4:2:2 8bit + sync signal (DDR)	8bit	4:2:2	27MHz	1	1	1	0	0	1
	YCbCr 4:2:2 16bit + sync signal	16bit	4:2:2	27MHz	0	0	0	0	0	1
	YCbCr 4:4:4 24bit + sync signal	24bit	4:4:4	27MHz	0	0	0	1	0	1
	RGB 4:4:4 24bit + sync signal	24bit	4:4:4	27MHz	0	0	0	1	1	1

● **Sub Address #01h / Input Mode Control2 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial Value
#01h	-	IN2S	-	-	NPSEL	I444SEL	IRGBSEL	IPRGSEL	07h

#01h/bit[7]
Set to “0”.

#01h/bit[6] IN2S
Selects a numeric format of the input chrominance signal (Cb/Cr).

0 : Offset binary format (default)
1 : 2’s complement format

#01h/bit[5:4]
Set to “00”.

#01h/bit[3] NPSEL
Selects Video Signal mode (NTSC/PAL)

0 : NTSC (default)
1 : PAL

#01h/bit[2] I444SEL
Selects a chrominance sampling rate of input images.
See Table 22 for the settings of image input format.

0 : 4:2:2
1 : 4:4:4 (default)

#01h/bit[1] IRGBSEL
Selects YCbCr or RGB of input video signal.
See Table 22 for the settings of image input format.

0 : YCbCr input
1 : RGB input (default)

#01h/bit[0] IPRGSEL
Selects a scan mode (interlace/progressive) of the input video signal.
See Table 22 for the settings of image input format.

0 : Interlace input
1 : Progressive input(default)

● **Sub Address #02h / Input Mode Control3 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#02h	FLDEN	PIFLD	PISEL	NEGCK	-	-	-	-	00h

#02h/bit[7] FLDEN
Outputs field information of CVBS output signal from the FIELD pin.
(Odd number field: FIELD output = "L", Even number field: FIELD output = "H")
Note: Because it is an identical pin with the FIELD signal input pin, the FIELD input function cannot be used when the FIELD signal output is enabled.

0 : OFF (default)
1 : FIELD signal output enabled

#02h/bit[6] PIFLD
In P/I conversion operation, the odd number line/even number line of input progressive image used for output interlace signal is specified by inputting field information from the FIELD pin.
(Odd number line: FIELD input = "L", Even number line: FIELD input = "H")
FIELD input logic reversion is possible by setting #02h/bit[5] PISEL.

0 : OFF (default)
1 : FIELD signal input enabled

#02h/bit[5] PISEL
In P/I conversion, FIELD input logic is reversed when the FIELD signal input is enabled (#02h/bit[6](PIFLD)=1).

0 : FIELD input = "L" : "Odd number line, FIELD input = "H" : Even number line (default)
1 : FIELD input = "H" : "Odd number line, FIELD input = "L" : Even number line

Selects the starting field of P/I conversion when the FIELD signal input is disabled (#02h/bit[6](PIFLD)=0).
A starting field is generated from the frame on the initial VSYNC_L falling after releasing reset as the starting point.

0 : An interlace signal is generated in the order of Even, Odd, Even, Odd field....(default)
1 : An interlace signal is generated in the order of Odd, Even, Odd, Even field....

#02h/bit[4] NEGCK
Selects a loading clock edge of input signal.

0 : CLK rising (default)
1 : CLK falling

#02h/bit[3:0]
Set to “000”.

● **Sub Address #03h / Output Data Control1 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#03h	CBON	BBON	BLON	SBON	RGBLEV	SETUP	OUTLEV		03h

#03h/bit[7] CBON
Outputs Color-Bar function.

0 : Off (default)
1 : Color-Bar signal output

#03h/bit[6] BBON
Outputs blue back signals.

0 : Off (default)
1 : Output blue back signals

#03h/bit[5] BLON
Outputs black level signals.

0 : Off (default)
1 : Output black level signals

#03h/bit[4] SBON
Selects the luminance value range of YCbCr input data.
SBON is a register to select the quantization range of a luminance signal. In addition to the range (16 to 235) regulated by the normal ITU-R BT.601,
a luminance signal can manage the data from 1 to 254 range as the luminance extended range mode. By using this mode, black on pedestal or less can be output.

0 : ITU-R BT.601 range mode (default)
1 : Extended luminance range mode

#03h/bit[3] RGBLEV
Selects an RGB input data range.

0 : Full-scale（0 to 255）(default)
1 : ITU-R BT.601 （16 to 235）

#03h/bit[2] SETUP
Selects whether 7.5IRE setup of NTSC output signals (composite signals and S-Video luminance signals) is provided.

0 : 7.5IRE setup is not provided. (default)
1 : 7.5IRE setup is provided.

#03h/bit[1:0] OUTLEV
Selects an output level of the built-in color bar.

00 : 25% color bar
01 : 50% color bar
10 : 75% color bar
11 : 100% color bar (default)

● **Sub Address #04h / Output Data Control2 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#04h	-	-	-	CLEV	-	-	-	-	00h

#04h/bit[7:5]
Set to “000”.

#04h/bit[4] CLEV
Selects the color difference range of YCbCr input data.
CLEV is a register to select the quantization range of a color difference signal. In addition to the range (16 to 240) regulated by the normal ITU-R BT.601,
a color difference signal can manage the data from 1 to 254 range as the extended color difference range mode.

0 : ITU-R BT.601range mode (default)
1 : Extended color difference range mode

#04h/bit[3:0]
Set to “0000”.

● **Sub Address #06h / Output Data Control3 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#06h	-	-	-	-	BLKADJ				08h

#06h/bit[7:4]
Set to “0000”.

#06h/bit[3:0] BLKADJ
Shifts the BLANK_L signal timing (rise and fall simultaneously) of the LSI internal section in pixel units within the range from –8 pixels to +7 pixels.

0h to 7h : Changes to the range from –8 pixels to –1 pixel.
8h : BLANK_L position is in default state.（default）
9h to 15h : Changes the range from +1 pixel to +7 pixels.

● **Sub Address #08h / Output Data Control4 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#08h	NOSIG	-	-	-	-	-	-	-	00h

#08h/bit[7] NOSIG
When an image signal/synchronization signal is not input to the encoder, an image signal can be output by generating a synchronization signal inside the encoder.

An image signal that can be output can be selected from blueback, color bar, and black level output. (Related register #03h)
Note: When #00h/bit[3:2]=01(ITU-R BT.656 style), this setting is not valid.

0 : Normal mode (default)
1 : Image no-input mode

#08h/bit[6:0]
Set to “000_0000”.

● **Sub Address #09h / Output Data Control5 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#09h	CVBSGAINY								80h

#09h/bit[7:0] CVBSGAINY
Adjusts the luminance signal level of CVBS output.

Bit	7	6	5	4	3	2	1	0
	Integer	Decimal part						

Setting is possible with 0 to approx. 1.9922 times (in units of 1/128).

● **Sub Address #0Ah / Output Data Control6 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Ah	CVBSGAINC								80h

#0Ah/bit[7:0] CVBSGAINC
Adjusts the color signal level of CVBS output.

Bit	7	6	5	4	3	2	1	0
	Integer	Decimal part						

Setting is possible with 0 to approx. 1.9922 times (in units of 1/128).

● **Sub Address #0Dh / Luminance Signal Filter Control （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Dh	-	-	-	-	-	-	APEN		00h

#0Dh/bit[7:2]
Set to “000000”.

#0Dh/bit[1:0] APEN
A mode selection signal of the aperture filter for a luminance signal. Emphasizes the high range frequency element.
The correction amount can be adjusted in three levels. MODE1 is the smallest correction amount, and MODE3 is the largest correction amount.

00: Aperture correction OFF (default)
01: Aperture correction ON MODE1
10: Aperture correction ON MODE2
11: Aperture correction ON MODE3

● **Sub Address #0Fh / Standby Control （R/W）**

Address	bit[7]	bit[6]	Bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Fh	-	-	-	-	-	-	MUTE	STANDBY	00h

#0Fh/bit[7:2]
Set to “000000”.

#0Fh/bit[1] MUTE
Sets the MUTE mode.
Digital signals to DAC are set to ALL "0", and perform zero output from DAC.

0 : Normal mode (default)
1 : MUTE mode

#0Fh/bit[0] STANDBY
The STANDBY register controls standby operation of a device. During the standby mode, consumption current can be reduced, because internal DAC powers down and DAC output becomes zero output.
During the standby mode, internal register can be also accessed.

0 : Normal mode (default)
1 : STANDBY mode

● **Sub Address #10h / CC Data Control （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#10h	CCEN		-	CCLN					11h

#10h/bit[7:6] CCEN

This register is the on-off control of the closed caption data.

00 :The C.C. data no addition (default)
01 :The CC data add to the odd fields.
10 :The CC data add to the even fields.
11 :The CC data add to the odd and the even fields.

#10h/bit[5]

Set to “0”.

#10h/bit[4:0] CCLN

This register specifies the addition line of the closed caption data.
The C.C. data is added to the line which is shown in table 23 by the register set value.

Table 23 :CCLN Register

CCLN	Function	
	NTSC	PAL
00000	Setting prohibited	Setting prohibited
00001	Setting prohibited	Odd 6、Even 319 Line
00010	Setting prohibited	Odd 7、Even 320 Line
00011	Setting prohibited	Odd 8、Even 321 Line
00100	Setting prohibited	Odd 9、Even 322 Line
00101	Setting prohibited	Odd 10、Even 323 Line
00110	Odd 10、Even 273 Line	Odd 11、Even 324 Line
00111	Odd 11、Even 274 Line	Odd 12、Even 325 Line
01000	Odd 12、Even 275 Line	Odd 13、Even 326 Line
01001	Odd 13、Even 276 Line	Odd 14、Even 327 Line
01010	Odd 14、Even 277 Line	Odd 15、Even 328 Line
01011	Odd 15、Even 278 Line	Odd 16、Even 329 Line
01100	Odd 16、Even 279 Line	Odd 17、Even 330 Line
01101	Odd 17、Even 280 Line	Odd 18、Even 331 Line
01110	Odd 18、Even 281 Line	Odd 19、Even 332 Line
01111	Odd 19、Even 282 Line	Odd 20、Even 333 Line
10000	Odd 20、Even 283 Line	Odd 21、Even 334 Line
10001*	**Odd 21、Even 284 Line**	**Odd 22、Even 335 Line**
10010	Odd 22、Even 285 Line	Odd 23、Even 336 Line
10011	Odd 23、Even 286 Line	Odd 24、Even 337 Line
10100	Odd 24、Even 287 Line	Odd 25、Even 338 Line
10101	Odd 25、Even 288 Line	Odd 26、Even 339 Line
10110	Odd 26、Even 289 Line	Odd 27、Even 340 Line
10111	Odd 27、Even 290 Line	Odd 28、Even 341 Line
11000	Odd 28、Even 291 Line	Odd 29、Even 342 Line
11001	Odd 29、Even 292 Line	Odd 30、Even 343 Line
11010	Odd 30、Even 293 Line	Odd 31、Even 344 Line
11011	Odd 31、Even 294 Line	Odd 32、Even 345 Line
11100	Odd 32、Even 295 Line	Odd 33、Even 346 Line
11101	Odd 33、Even 296 Line	Odd 34、Even 347 Line
11110	Odd 34、Even 297 Line	Odd 35、Even 348 Line
11111	Odd 35、Even 298 Line	Odd 36、Even 349 Line

NTSC Odd : 4+CCLN [Line]
NTSC Even : 267+CCLN [Line]
PAL Odd : 5+CCLN [Line]
PAL Even : 318+CCLN [Line]

● **Sub Address #11h / CC Odd Data0 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#11h	CCOD0								00h

#11h/bit[7:0] CCOD0
This register specifies the Odd 1st Byte Data of the C.C. data.

Table 24 : Sets to the Odd 1st Byte Data (Bit0,Bit1,Bit2,Bit3,Bit4,Bit5,Bit6 and Pty1 data)of the C.C. data.

CCOD0[7]	CCOD0[6]	CCOD0[5]	CCOD0[4]	CCOD0[3]	CCOD0[2]	CCOD0[1]	CCOD0[0]
Pty1	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

● **Sub Address #12h / CC Odd Data1 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#12h	CCOD1								00h

#12h/bit[7:0] CCOD1
This register specifies the Odd 2nd Byte Data of the C.C. data.

Table 25 : Sets to the Odd 2nd Byte Data (Bit0,Bit1,Bit2,Bit3,Bit4,Bit5,Bit6 and Pty2 data)of the C.C. data.

CCOD1[7]	CCOD1[6]	CCOD1[5]	CCOD1[4]	CCOD1[3]	CCOD1[2]	CCOD1[1]	CCOD1[0]
Pty2	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

● **Sub Address #13h / CC Even Data0 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#13h	CCED0								00h

#13h/bit[7:0] CCED0
This register specifies the Even 1st Byte Data of the C.C. data.

Table 26 : Sets to the Even 1st Byte Data (Bit0,Bit1,Bit2,Bit3,Bit4,Bit5,Bit6 and Pty1 data)of the C.C. data.

CCED0[7]	CCED0[6]	CCED0[5]	CCED0[4]	CCED0[3]	CCED0[2]	CCED0[1]	CCED0[0]
Pty1	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

● **Sub Address #14h / CC Even Data1 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#14h	CCED1								00h

#14h/bit[7:0] CCED1
This register specifies the Even 2nd Byte Data of the C.C. data.

Table 27 : Sets to the Even 2nd Byte Data (Bit0,Bit1,Bit2,Bit3,Bit4,Bit5,Bit6 and Pty2 data)of the C.C. data.

CCED1[7]	CCED1[6]	CCED1[5]	CCED1[4]	CCED1[3]	CCED1[2]	CCED1[1]	CCED1[0]
Pty2	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

● **Sub Address #15h / CC Data Status （R）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#15h	-						CCSTAT1	CCSTAT2	03h

#15h/bit[7:2]
Set to “0000_00”.

#15h/bit[1] CCSTAT1
This register shows the status of the C.C. data of even field(Address #13h, #14h).
This register is lead clear and read-only.

0 : The encoding end of the CC data
1 : The register writing is finished of C.C. data.

#15h/bit[0] CCSTAT2
This register shows the status of the C.C. data of odd field(Address #11h, #12h).
This register is lead clear and read-only.

0 : The encoding end of the CC data
1 : The register writing is finished of C.C. data.

● **Sub Address #16h / CGMS Control1 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#16h	CGMSEN	-	WDO1						00h

#16h/bit[7] CGMSEN
This register chooses the CGMS function enable or disable.

0 : CGMS disable (default)
1 : CGMS enable

#16h/bit[6]
Set to “0”.

#16h/bit[5:0] WDO1
This register specifies CGMS data.

Table 28: Sets to the CGMS data (Bit1,Bit2,Bit3,Bit4,Bit5 and Bit6 data)

WDO1[5]	WDO1[4]	WDO1[3]	WDO1[2]	WDO1[1]	WDO1[0]
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

● **Sub Address #17h / CGMS Control2 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#17h	WDO2								00h

#17h/bit[7:0] WDO2
This register specifies CGMS data.

Table 29: Sets to the CGMS data (Bit7,Bit8,Bit9,Bit10,Bit11,Bit12,Bit13 and Bit14 data)

WDO2[7]	WDO2[6]	WDO2[5]	WDO2[4]	WDO2[3]	WDO2[2]	WDO2[1]	WDO2[0]
Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6

● **Sub Address #18h / CGMS Control3 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#18h	CRCON	-	CRCDATA						00h

#18h/bit[7] CRCON
This register chooses a way of specifying the CRC dater of CGMS. (the auto-generation mode or the user specification mode.)

0 : The auto-generation mode of the CRC data. (default)
1 : The user specification mode of the CRC data,

#18h/bit[6]
Set to “0”.

#18h/bit[5:0] CRCDATA
This register stores the CRC data which the user specifies.

Table 30: Sets to the CGMS data (Bit15,Bit16,Bit17,Bit18,Bit19 and Bit20 data)

CRCDATA[5]	CRCDATA[4]	CRCDATA[3]	CRCDATA[2]	CRCDATA[1]	CRCDATA[0]
Bit19	Bit18	Bit17	Bit16	Bit15	Bit14

● **Sub Address #19h / WSS Control1 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#19h	GP12								00h

#19h/bit[7:0] GP12
This register specifies WSS data of PAL.

Table 31: Sets to the WSS data (Bit0,Bit1,Bit2,Bit3,Bit4,Bit5,Bit6 and Bit7 data)

GP12[7]	GP12[6]	GP12[5]	GP12[4]	GP12[3]	GP12[2]	GP12[1]	GP12[0]
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

● **Sub Address #1Ah / WSS Control2 （R/W）**

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#1Ah	WSSEN	-	GP34						00h

#1Ah/bit[7] WSSEN
This register chooses the WSS function enable or disable.

0 : WSS disable (default)
1 : WSS enable

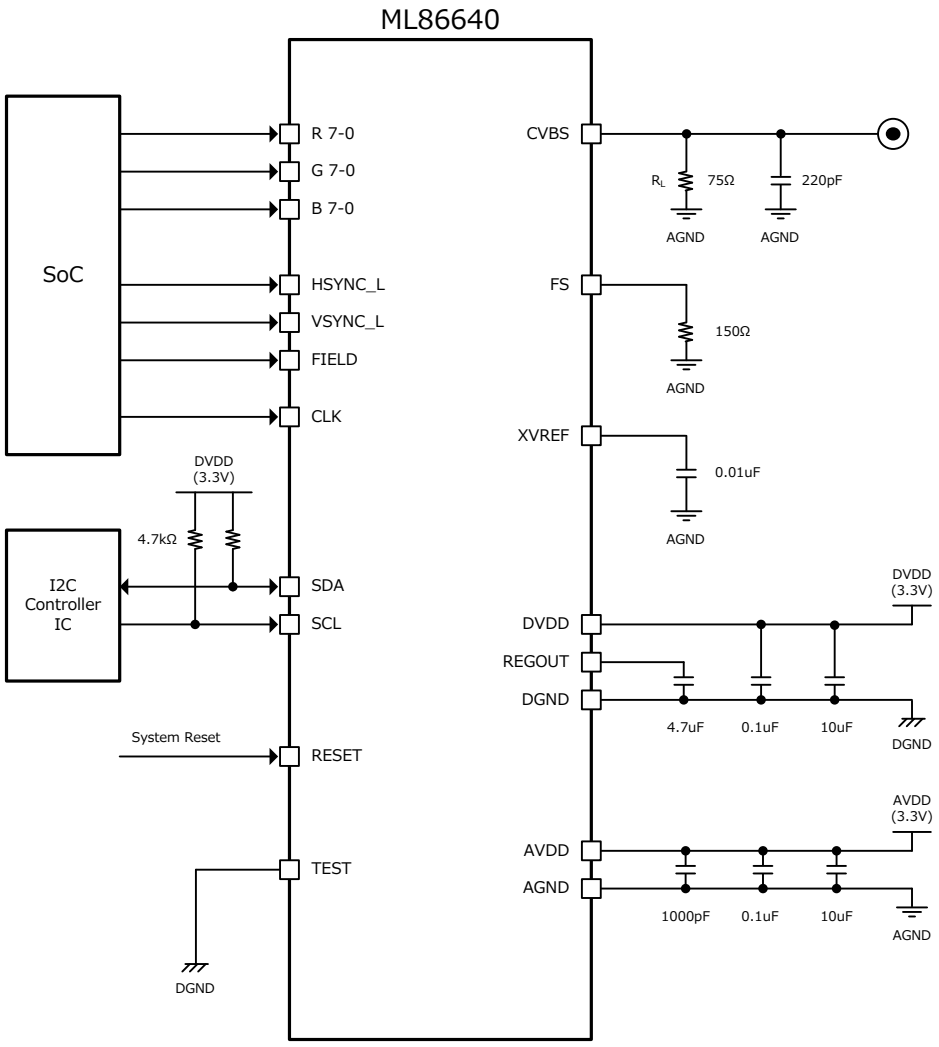
#1Ah/bit[6]
Set to “0”.

#1Ah/bit[5:0] GP34
This register specifies WSS data of PAL.

Table 32: Sets to the WSS data (Bit8,Bit9,Bit10,Bit11,Bit12 and Bit13 data)

GP34[5]	GP34[4]	GP34[3]	GP34[2]	GP34[1]	GP34[0]
Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

■ An Expample of Circuit Connection



The applied circuit example shown above shows a representative example for usage reference.

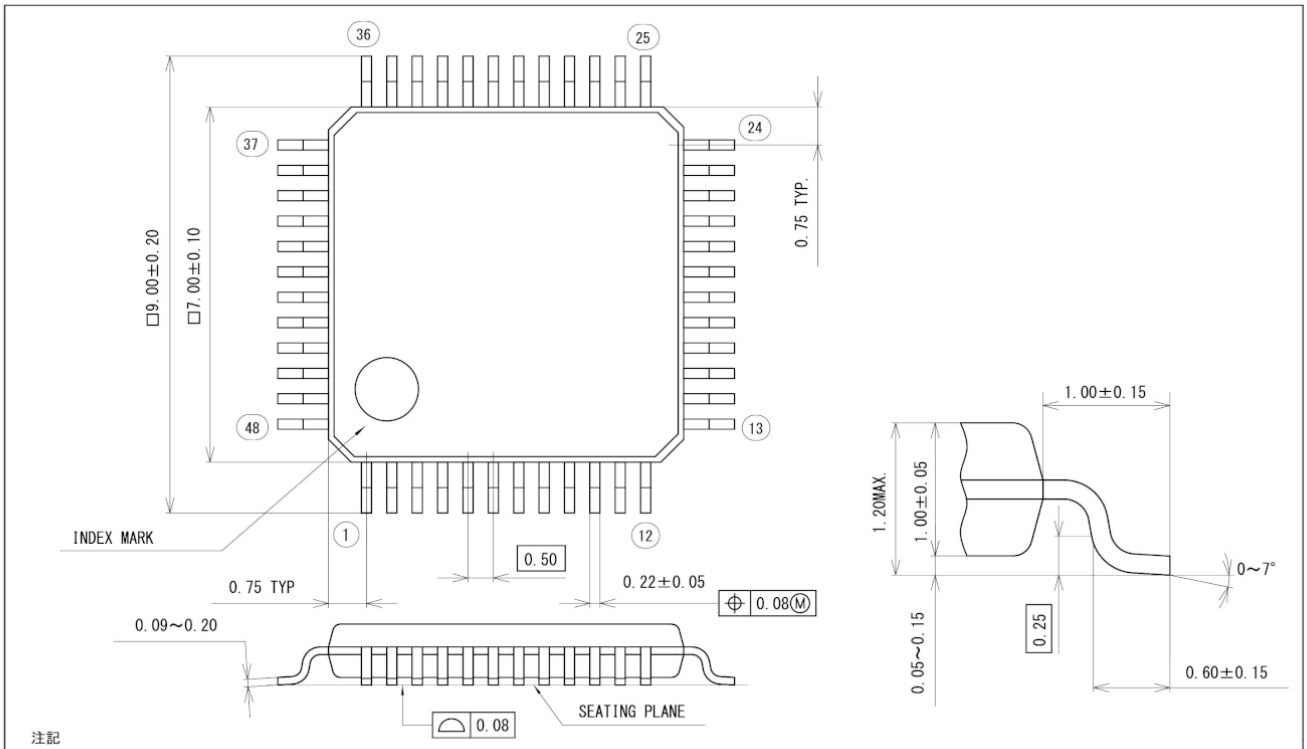
When using with the ITU-R BT.656 style, fix the HSYNC_L and VSYNC_L pins to "L" level to make sure they do not be in the OPEN state.

For the load resistor to connect to the CVBS pin, and load resistor to connect to the FS pin, ± 1 % or less is recommended.
Connect a ceramic capacitor with 4.7 uF ± 20 % or more to the regulator output pin (REGOUT).

The circuit example shown here is an applied example, and does not guarantee its performance.
When using this LSI, perform operation verification on circuit element and circuit configuration optimized to your system.

■ PACKAGE DIMENSIONS

TQFP48



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69142
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.13TYP	REVISED	Oct/12/2020

■ Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEDL86640-01	2017.3.23	—	56	first edition issued
FEDL86640-02	2018.3.19	56	56	2nd edition issued
FEDL86640-03	2024.2.20	56	56	p.3: Added applications and “Line up” p.51, p52: Correct table28,29,30 p.56: Updated “Notice”

Notes

1) When using LAPIS Technology Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings*1, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
   *1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples, etc.). Therefore, LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) LAPIS Technology intends our Products to be used in a way indicated in this document. Please be sure to contact a ROHM sales office if you consider the use of our Products in different way from original use indicated in this document. For use of our Products in medical systems, please be sure to contact a LAPIS Technology representative and must obtain written agreement. Do not use our Products in applications which may directly cause injuries to human life, and which require extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us without our prior written consent.

6) All information contained in this document is subject to change for the purpose of improvement, etc. without any prior notice. Before purchasing or using LAPIS Technology Products, please confirm the latest information with a ROHM sales office. LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document, however, LAPIS Technology shall have no responsibility for any damages, expenses or losses arising from inaccuracy or errors of such information.

7) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

8) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

9) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.

10) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) “LAPIS Technology” as used in this document means LAPIS Technology Co., Ltd.

LAPIS Technology Co.,Ltd.
2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/

LTSZ08023・01・002