Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL7344C/E/J-08
Issue Date: Jan 10, 2024

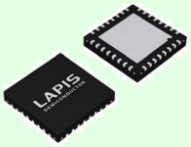
ML7344C/E/J

Sub-GHz(160MHz to 510MHz) band short range wireless transceiver IC

■Overview

ML7344C/E/J is a narrow band sub-GHz IC that integrates RF part, IF part, MODEM part and HOST interface part in single-chip. It supports various frequency band from 160MHz to 510MHz. ML7344C can output 100mW (20dBm) transimittion power and it suits for the smart-meter in Chinese market. ML7344E is suitable for Fmode (434MHz) or N mode (169MHz) of Wireless M-Bus system. ML7344J is suitable for security radio system type III or IV of the RCR STD-30 and specified low-power radio station in 426 MHz operation of the ARIB STD-T67.

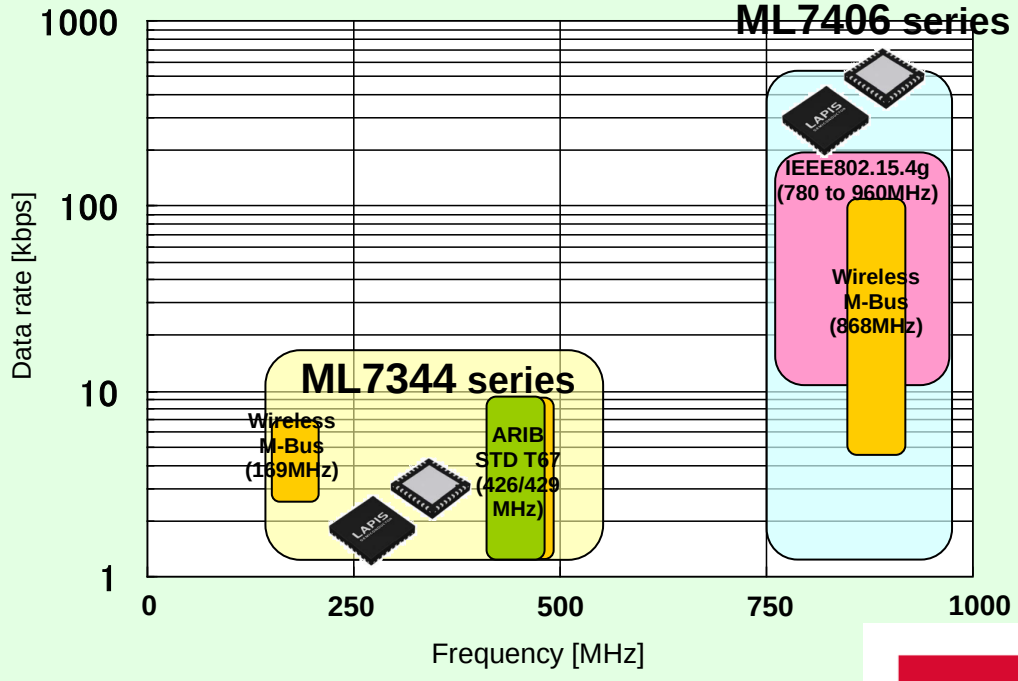
ML7406 and ML7344 have the same package, pins assignment and major registers.



(32pin WQFN)

ML7344 series
RF: 160MHz to 510MHz
Rate: 1.2kbps to 15kbps (FSK/GFSK)
Channel Spacing: 25 kHz
Wireless M-Bus
ARIB STD-T67

ML7406 series
RF: 750MHz to 960MHz
Rate: 1.2kbps to 500kbps (FSK/GFSK)
Channel Spacing: 100 kHz to 1.6MHz
Wireless M-Bus
IEEE802.15.4g (FEC not supported)
ARIB STD-T108



●Product Name ML7344JCGD ML7344JTGD

●Application Remote control
Home, Building Security
Sensor Network
Smart Meters

■Features

- Frequency Range: 160 – 510MHz
- ML7344C is able to use as communication unit of Q_GDW374.3 (China)
  ML7344E is able to use as F mode or N mode of the wirelss M-bus system.
  ML7344J is able to use as type III or IV security radio of RCR STD-30 and ARIB STD-T67 in 426 MHz operation. (Japan)
- High accurate modulation implemented by direct modulation scheme using fractional-N PLL.
- Multiple modulation scheme : GFSK/GMSK, FSK/MSK
- Configurable data ratres from 1.2kbps to 15 kbps
- Supports NRZ code, Manchester code and 3 out of 6 code.
- Programmable modulation frequency deviation
- Polarity conversion for TX and RX data bits
- On chip 26MHz oscillation circuit implemented (ML7344xC x=C, E or J)
  Supports 26MHz TCXO input. (ML7344xT, x=C, E or J)
  Note: The ordering product name is different from supporting clock source.
- On chip low speed RC oscillation circuit.
- Oscillation frequecy tuning function implemented. (ML7344xC x=C, E or J)
- Frequency tuning function (frequency fine tuning by oscillation circuit and fractional-N PLL)
- Built in Power Amp (PA) and power control function
  Programmable from 100mW, 20mW and 10mW (ML7344C)
  Programable from 20mW,10mW and 1mW (ML7344E/J)
- Fine output power tuning function implemented. (Tune ±0.2dB)
- TX ramp control function implemented
- High speed carrier checking function
- Support external PA
- Receive Signal Strength Indicator (RSSI) reporting function and threshold comparison function
- Built-in AFC function
- Synchronous serial peripheral interface (SPI)
- Auto wake-up and auto sleep function are implemented
- 2 genral purpose timers are implemented
- Test Pattern generation (PN9, CW, 0/1, all-1, all-0 pattern)

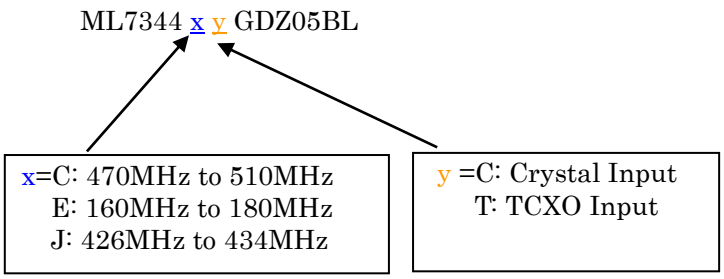
- Packet mode function
    - Support 2 wireless M-bus packet format. (Format A and B)
    - Support general packet format (Format C)
    - Max packet length 255 bytes (Format A and B)and 2047 bytes (Format C)
    - 64 byte TX and RX buffer are implemented
    - Preamble pattern detection function (Preamble length can be prgrammable between 1 to 4 Byte)
    - Programmable TX preamble length (Max 16383 Byte)
    - ID code or SFD detection function (Max 4 Byte x 2codes, available for TX and RX)
    - Progrmable CRC generate function for CRC32, CRC16 and CRC8
    - Whitenning function
    - Address filtering function
      Checking C-Fieled, M-Field and A field of wireless M-bus packet (EN13575-4:2011)

- Supply voltage
  1.8V to 3.6V Outpur power is set at 1mW
  2.1V to 3.6V Output power is set at 10mW
  2.6V to 3.6V Output power is set at 20mW
  3.3V to 3.6V Output power is set at 100mW
- Operating temperature -40 to +85 ˚C
- Current consumption (operation at 400MHz band)

Deep Sleep Mode:		0.1 uA (Typ)
Sleep Mode1		0.4 uA (Typ) (Maintain Register values)
Sleep Mode2		0.53 uA (Typ) (Maintain Register values and FIFO data)
Idle Mode		0.6 mA (Typ)
TX	100mW	90 mA (Typ.)
	20mW	28 mA (Typ.) (ML7344E/J)
		45 mA (Typ.) (ML7344C)
	10mW	22 mA (Typ.)
	1mW	8.8 mA (Typ.)
RX		6.2 mA (Typ.)

- Package
  32 pin WQFN 5.0mm x 5.0mm x 0.8mm
  Pb free, RoHS compliant

■Ordering Guide



■Description Convention

1) Numbers description
'0xnn' indicates hexadecimal and '0bnn' indicates binary

Example: 0x11=17 (decimal), 0b11=3 (decimal)

2) Register description
[<register name>: B<Bank No.> <register address>] register

Example: [RF_STATUS: B0 0x0B] register
Register name: RF_STATUS
Bank No.: 0
Register address: 0x0B

3) Bit name description
<bit name> ([<register name>: B<Bank No.> <register address> (<bit location>)])

Example: SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)])
Bit name: SET_TRX
Register name: RF_STATUS
Bank No.: 0
Register address: 0x0B
Bit location: bit3 to bit0

4) In this documet
"TX" stands for transmittion.
"RX" stands for reception.

■Block Diagram

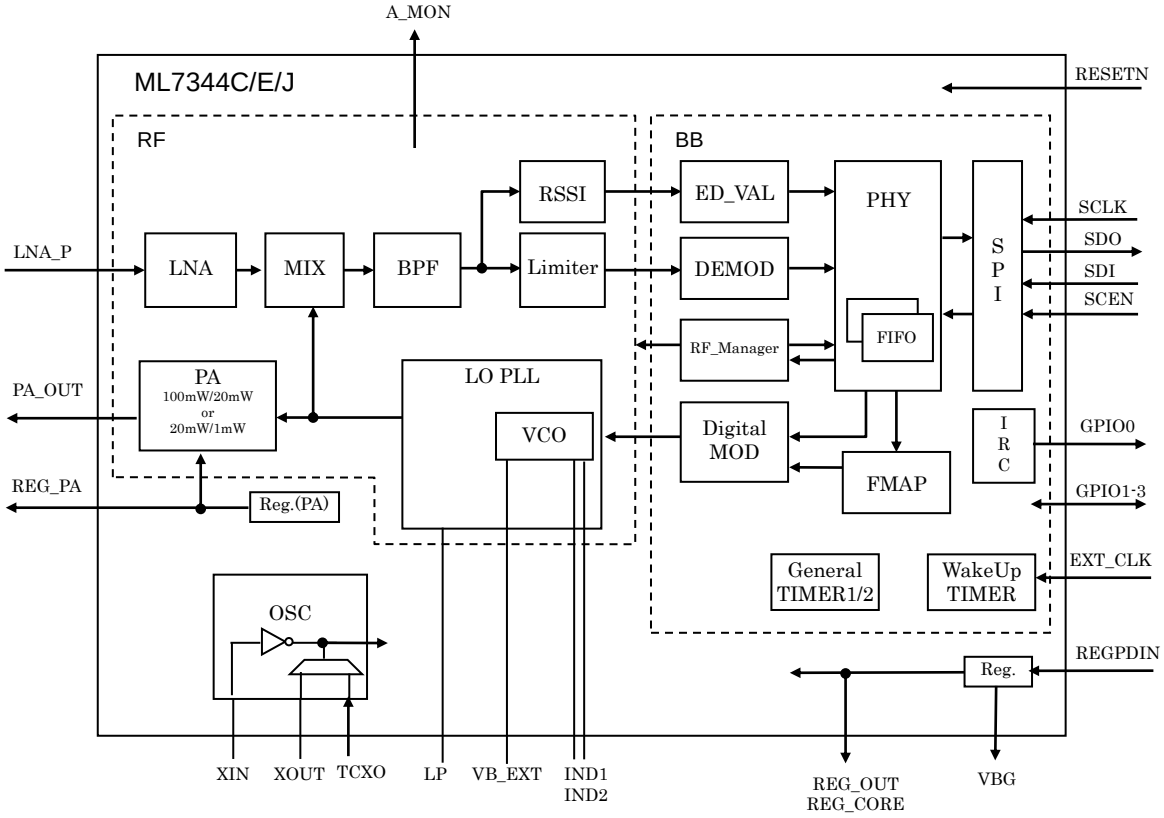


Fig.1 Block diagram

■PIN Configuration

Package: 32pin WQFN

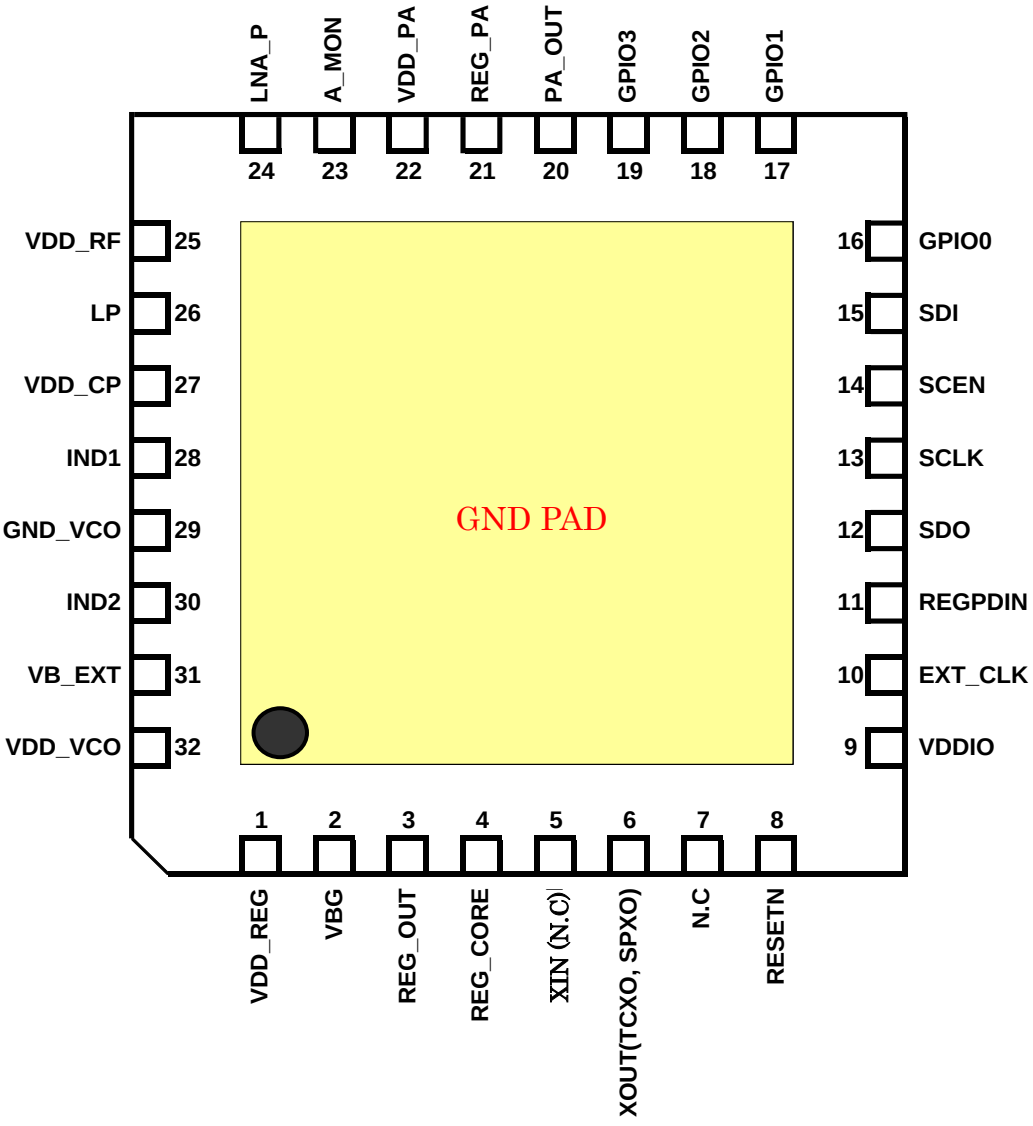


Fig.2 Pin Assignment

NOTE: Pattern shown in the centre of the chip is located at bottom side of the chip (GND PAD)

■PIN Definitions

Definiion of Symbols

I/O			Reset state			Active Level		
I	:	Digital input	I	:	Digital Input	H	:	High Level
O	:	Digital output	O	:	Digital Ouput	L	:	Low Level
IS	:	Shmidt Trigger input	Hi-Z	:	High-Impedance	OD	:	Open Drain
IO	:	Digital input/output				P	:	Positive Edge
IA	:	Analog input				N	:	Negative Edge
OA	:	Analog output 1						
OAH	:	Analog output 2						
IOA	:	Analog input/output						
IRF	:	RF input						
ORF	:	RF output						
VDDIO	:	I/O power supply						
VDDRF	:	RF power supply						
GND	:	Ground						

●RF and Analog pins

Pin	Pin name	Reset state	I/O	Active Level	function
20	PA_OUT	−	O_{RF}	−	RF antenna output
23	A_MON	−	O_A	−	Temperature information output (*1)
24	LNA_P	−	I_A	−	RF antenna input
26	LP	−	IO_A	−	Pin for loop filter
28	IND1	−	IO_A	−	Pin for VCO tankl inductor
30	IND2	−	IO_A	−	Pin for VCO tank inductor
31	VB_EXT	−	IO_A	−	Pin for smothing capacitor for internal bias

*1 This pin can be configured by [MON_CTRL:B0 0x4D] register, no signal assigned as default setting.

●SPI Interface pins

Pin	Pin name	Reset state	I/O	Active Level	function
12	SDO	Hi-Z	O	H or L	SPI data output or DCLK (*1)
13	SCLK	Hi-Z	I_S	P or N	SPI clock input
14	SCEN	Hi-Z	I_S	L	SPI chip enable L: enable H: disable
15	SDI	Hi-Z	I_S	H or L	SPI data input or DIO (*1)

*1 Please refer to “DIO function”

●Regulator pins

Pin	Pin name	Reset state	I/O	Active Level	function
2	VBG	−	O_{AH}	−	Pin for decouppling capacitor
3	REG_OUT	−	O_{AH}	−	Requlator1 ouput (typ. 1.5V)
4	REG_CORE	−	O_A	−	Requlator2 ouput (typ. 1.5V)
11	REGPDIN	I	I	H	Power down control pin for regulator Fix to ‘L’ for nomal use. “H” is for deep sleep mode.
21	REG_PA	−	O_{AH}	−	Regulator output for PA block

●Miscellaneous pins

Pin	Pin name	Reset state	I/O	Active Level	function
5	XIN N.C.(*2)	I –	I_A –	P or N –	26MHz crystal pin1 (Note) In case of TCXO, it must be open.
6	XOUT TCXO(*2)	O	O_A I_A I	P or N	26MHz crystal pin 2 or TCXO input
8	RESETN	I	I_S	L	Reset L: Hardware reset enable (Forcing reset state) H: Normal operation
10	EXT_CLK	Hi-Z	IO	P or N	Digital I/O (*3) Reset state: External RTC (32kHz) input. [ML7344E/J] External PA control signal output. [ML7344C]
16	GPIO0	Hi-Z	IO or OD(*1)	H or L	Digital GPIO (*4) Reset state: interrupt indication signal output
17	GPIO1	Hi-Z	IO or OD(*1)	H or L	Digital GPIO (*5) Reset state: clock output
18	ANT_SW/ GPIO2	Hi-Z	IO or OD(*1)	H or L	Digital GPIO (*6) Reset state: Antenna diversity selection control signal
19	TRX_SW/ GPIO3	Hi-Z	IO or OD(*1)	H or L	Digital GPIO (*7) Reset state: TX –RX selection signal control

(Note)

*1 OD is open drain output.

*2 The following pin names are different depend on products.

Pin No.	ML7344C	ML7344T
5	XIN	N.C.
6	XOUT	TCXO

(Note)

*1 In case of using TCXO, set TCXO_EN=0b1. Please make sure only one of the register TCXO_EN, XTAL_EN is set to 0b1.

*2 For ML7344Jy, the initial value of the register TCXO_EN is 0b1. In case of using ML7344JC, the register XTAL_EN([CLK_SET2: B0 0x03(4)])=0b1 must be programmed first.

*3 For ML7344Cy, the initial value of the register XTAL_EN is 0b1. In case of using ML7344CT, the register TCXO_EN([CLK_SET2: B0 0x03(6)])=0b1 must be programmed first.

*4 Please refer to [EXTCLK_CTR: B0 0x52] register.

*5 Please refer to [GPIO0_CTRL: B0 0x4E] register

*6 Please refer to [GPIO1_CTRL: B0 0x4F] register

*7 Please refer to [GPIO2_CTRL: B0 0x50] register

*8 Please refer to [GPIO3_CTRL: B0 0x51] register

●Power supply/GND pins

Pin	Pin name	Reset state	I/O	Active Level	function
1	VDD_REG	−	V_{DDIO}	−	Power supply pin for Regulator (input voltage: 1.8V to 3.3V)
9	VDDIO	−	V_{DDIO}	−	Power supply for digital I/O (input voltage: 1.8 to 3.6V)
22	VDD_PA	−	V_{DDIO}	−	Power supply for PA block (input voltage: 18 to 3.6V, depending on TX mode)
25	VDD_RF	−	V_{DDRF}	−	Power supply for RF blocks (REG-OUT is connected, typ.1.5V)
27	VDD_CP	−	V_{DDRF}	−	Power supply for charge pump (REG-OUT is connected, typ.1.5V)
32	VDD_VCO	−	V_{DDRF}	−	Power supply for VCO (REG_OUT is connected, typ.1.5V)
29	GND_VCO	−	GND	−	GND for VCO

●Unused pins treatment

Unused pins treatments are as follows:

Unused pins treatment

Pin name	Pins number	Recommended treatment
N.C.	5	Open
N.C.	7	GND or Open
EXT_CLK	10	GND
A_MON	23	GND
GPIO0	16	Open
GPIO1	17	Open
GPIO2	18	Open
GPIO3	19	Open

(Note)

*1 If input pins are high-impedence state and leave open, excess current could be drawn. Care must be taken that unused input pins and unused I/O pins should not be left open.

*2 After reset, GPIO1 pin is CLK_OUT function. If this function is not used, the clock must to be disabled by setting 0b000 to GPIO1_IO_CFG[2:0] ([GPIO1_CTRL: B0 0x4F (2-0)]). If this pin is left open while outputing clock signal, it may affect RX sensitivity.

■Electrical Characteristics

●Absolute Maximum Ratings

Ta=-40˚C to +85˚C and GND=0V is the typical conditoin if not defined specific condition.

item	symbol	condition	Rating	unit
I/O Power supply	V_{DDIO}		-0.3 to +4.6	V
RF Power supply	V_{DDRF}		-0.3 to +2.0	V
RF input power	P_{RFI}	Antenna input in RX	0	dBm
RF output Voltage	V_{RFO}	PA_OUT(#20)	-0.3 to +4.6	V
RF output Voltage[ML7344C]	V_{RFO}	PA_OUT(#20) Duty Cycle of transmission at +20dBm output <1 %	-0.3 to +7.7	V
Voltage on Analog Pins 1	V_A		-0.3 to +2.0	V
Voltage on Analog Pins 2	V_{AH}		-1.0 to +4.6	V
Voltage on Digital Pins	V_D		-0.3 to +4.6	V
Digital Input Current	IDI		-10 to +10	mA
Digital Output Current	IDO		-8 to +8	mA
Power Dissipation	Pd	Ta= +25˚C	1.2	W
Storage Temperature	Tstg	−	-55 to +150	˚C

●Recommended Operating Conditions

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Power Supply (I/O)	V_{DDIO}	VDD_IO, VDD_REG pins	1.8	3.3	3.6	V
Power Supply (PA)	V_{DDPA}	VDD_PA pin TX power = 1mW	1.8	3.3	3.6	V
		VDD_PA pin TX power = 10mW	2.1	3.3	3.6	V
		VDD_PA pin TX power = 20mW	2.6	3.3	3.6	V
		VDD_PA pin TX power = 100mW	3.3	-	3.6	V
Ambient Temperature	T_a	-	-40	+25	+85	ºC
Digital input rising time	T_{IR}	Digital input pins (*1)	-	-	20	ns
Digital input falling time	T_{IF}	Digital Input pins (*1)	-	-	20	ns
Digital output loads	C_{DL}	All Digital Output pins	-	-	20	pF
Master clock frequency	F_{MCK1}	(*2)	-	26	-	MHz
Master clock accuracy	A_{CMCK}	(*3)	-10		+10	ppm
TCXO Input voltage	V_{TCXO}	DC cut (ML7344xT)	0.8	-	1.5	Vpp
SPI clock frequency	F_{SCLK}	SCLK pin	0.032	2	16	MHz
SPI clock duty ratio	D_{SCLK}	SCLK pin	45	50	55	%
RF channel frequency	F_{RF}	ML7344C ML7344E ML7344J	470 160 315	- - -	510 180 450	MHz

(*1) Those pins with symbol I, Is at pin definition section
(*2) XIN and XOUT pin (ML7344xC), TCXO pin (ML7344xT)
(*3) This difinition is the specification of RF communication availability, not the system requirement.
Use the appropriate frequency accuracy under each specificaton requirement as below.

Specification	Required accuracy
RCR STD-30 type III (Japan)	±10 ppm
RCR STD-30 type IV (Japan)	±4 ppm
Wireless M-bus N mode	±1.5kHz (±8.5 ppm, 4.8kbps) ±2.0kHz (±11.803 ppm, 2.4kbps)
Wireless M-bus F mode	±16 ppm

●Power Consumption

Item	Symbol	Conditions		Min	Typ. (*2)	Max(*3)	Unit
Power Consumption (*1)	I_{DD_DSLP}	Deep Sleep mode		-	0.1	11 (0.8)	µA
	I_{DD_SLP1}	Sleep mode 1 (*4)		-	0.4	23 (1.6)	µA
	I_{DD_SLP2}	Sleep mode 2 (*4)		-	0.53	25.8 (1.9)	µA
	I_{DD_SLP3}	Sleep mode 3 (*4)		-	0.7	26 (2.1)	µA
	I_{DD_SLP4}	Sleep mode 4 (*4)		-	2.14	28 (4.1)	µA
	I_{DD_IDLE}	Idle mode(*5)		-	0.6	-	mA
	I_{DD_RX}	RF RX mode (*6)(*7) LOW_RATE_EN([CLK_SET2:		-	5.9	-	mA
	I_{DD_TX1}	RF TX mode (1mW) (*6) For ML7344E/J		-	8.8	-	mA
	I_{DD_TX10}	RF TX mode (10mW) (*6)		-	22.0	-	mA
	I_{DD_TX20}	RF TX mode (20mW)	For ML7344E/J (*6)	-	28.0	-	mA
			For ML7344C (*7)	-	45.0	-	mA
	I_{DD_TX100}	RF TX mode (100mW) (*7) For ML7344C		-	90	-	mA
	I_{DD_XTAL}	X'tal Oscillator Circuit (*8)		-	0.3	-	mA

(*1) Power consumption is sum of current consumption of all power supply pins
(*2) "Typ" value is centre value under condition of VDDIO=3.3V, 25˚C.
(*3) () is a reference maximum value under condition of 25˚C
(*4) The definition od each sleep mode is shown in following table.

Mode.	Register	FIFO	RC Osc. (32kHz)	Low clock timer
Sleep mode 1	Not retain	Not retain	OFF	-
Sleep mode 2	Retain	Retain	OFF	-
Sleep mode 3	Retain	Retain	External Input	ON
Sleep mode 4	Retain	Retain	ON	ON

(*5) Under condition of using TCXO.
(*6) Under condition of data receiving speed at 9.6 kbps and 426 MHz operation.
(*7) Under condition of data receiving speed at 9.6 kbps and 490 MHz operation.

(*8) When using ML7344xC, power consumptions of each mode exluded Deep Sleep and Sleep are added I_{DD_XTAL}.

●DC characteristics

Item	Symbol	Conditions	Min	Typ. (*2)	Max	Unit
Voltage Input High	VIH1	Digital input/inout pins	V_{DDIO} *0.75	-	V_{DDIO}	V
	VIH2	XIN pin	1.35	-	1.5	V
Voltage Input Low	VIL1	Digital input/inout pins	0	-	V_{DDIO} *0.18	V
	VIL2	XIN pin	0	-	0.15	V
Schmit Trigger Threshold High level	VT+	Digital pins with shmitt trigger gate	-	1.2	V_{DDIO} *0.75	V
Schmit Trigger Threshold Low level	VT-	Digital pins with shmitt trigger gate	V_{DDIO} *0.18	0.8	-	V
Input leakage current	IIH1	Digital input pins	-1	-	1	µA
	IIL1	Digital input pins	-1	-	1	µA
	IIL2	XIN pin	-0.3	-	0.3	µA
Tri-state output leakage current	IOZH	EXT_CLK, GPIO0-3 pins	-1	-	1	µA
	IOZL	EXT_CLK, GPIO0-3 pins	-1	-	1	µA
Voltage ouput level H	VOH	IOH=-4mA	V_{DDIO} *0.8	-	V_{DDIO}	V
Voltage ouput evel L	VOL	IOL=4mA	0	-	0.3	V
Regulator output voltage	MAIN_REG	REG_CORE and REG_OUTpin When in mode other than	1.4	1.5	1.6	V
	SUB_REG	REG_CORE pin When in sleep mode	0.95	1.5	1.65	V
Pin capacitance	CIN	Input pins	-	6	-	pF
	COUT	Output pins	-	9	-	pF
	CRFIO	RF inout pins	-	9	-	pF
	CAI	Analog input pins	-	9	-	pF

●RF characteristics

Data Rate : 1.2 kbps to 15 kbps
Modulation scheme : 2-GFSK/ 2-FSK
Channel spacing : 25kHz
Definisiton Point : ANT connector of ML7344 RF board.

[RF frequency]

Item	Condition	Min	Typ.	Max	Unit
ML7344C	LNA_P,PA_OUT pins	470	-	510	MHz
ML7344E		160	-	180	MHz
ML7344J		315	-	450	MHz

NOTE:1) Support 160 MHz to 510 MHz by changing L and C components between IND1 and IND2 pins
2) Integer multiples of the master clock frequency and its around frequency can not be used. Please refer section of “Programing Channel Frequency ”

[TX characteristics]

170MHz and 426MHz Band (160MHz to 180MHz, 315MHz to 450MHz) [ML7344E/J]

Item	Condition	Min	Typ.	Max	Unit
TX Power	20mW(13dBm) mode	10	13	13.8	dBm
	10mW(10dBm) mode	7	10	10.8	dBm
	1mW(0dBm) mode	-3	0	0.8	dBm
Frequency deviation setting range [Fdev]		0.025	-	400	kHz
Occupied bandwidth 9600 bps (PN9), Fdev=3 kHz	Band including 99% power	8.5	-	11.8	kHz
Adjacent Channel Power 9600bps (PN9), Fdev=3 kHz	Offset:25 kHz ±8 kHz band	-	-	-40	dB
Spurious emission level	+10dBm output 9600 bps (PN9). Fdev = 3 kHz Total power from 62.5 kHz to 162.5kHz offset	-	-	-26	dBm
	Harmonics +10dBm output with LC trap filter 9600 bps (PN9). Fdev = 3 kHz	-	-	-26	dBm

470MHz BAND(470MHz to 510MHz) [ML7344C]

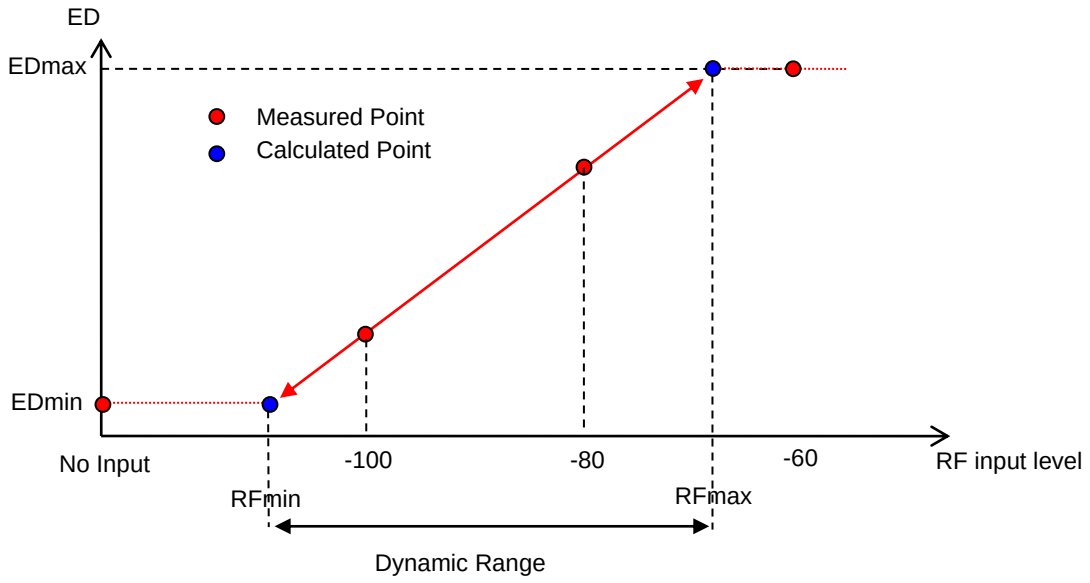
Item	Condition	Min	Typ.	Max	Unit
TX Power	100mW(20dBm) mode	18.5	20	23	dBm
	20mW(13dBm) mode	10	13	16	dBm
Frequency Deviation (Fdev) Range		0.025	-	400	kHz
Occupied bandwidth 9600 bps (PN9), Fdev=3 kHz	Band including 99% power	8.5	-	11.8	kHz
Spurious emission level	Harmonics +20dBm output with LC trap filter	-	-	-36	dBm

[RX characteristics]

426MHz Band (315MHz to 450MHz) [ML7344J]

Item	Condition		Min	Typ.	Max	Unit
Minimum RX sensitivity BER<0.1%	4.8 kbps, Fdev=3kHz		-	-115	-108	dBm
	9.6 kbps, Fdev=3kHz		-	-114	-107	dBm
	4.8 kbps, Fdev=3kHz High Gain Mode		-	-118	-111	dBm
	9.6 kbps, Fdev=3kHz High Gain Mode		-	-117	-110	dBm
Adjacent channel rejection	±12.5 kHz		-	3	-	dB
	±25 kHz		30	33	-	dB
	±50 kHz		-	36	-	dB
Blocking (426MHz operation)	1 MHz offset		-	69	-	dB
	2 MHz offset		-	72	-	dB
	6 MHz offset		-	75	-	dB
	10 MHz offset		-	80	-	dB
	-400kHz offset (image frequency), Ta=25 ºC After I/Q adjustment		30	40	-	dB
Minimum power detection level	RFmin in Figure of RSSI characteristics*1		-	-115	-	dBm
		High Gain Mode	-	-120	-	dBm
Power detection range	Dynamic Range in Figure of RSSI characteristics*1		-	40	-	dB
		High Gain Mode	-	35	-	dB
Spurious Emission level	Compliant with FCC, ARIB, ETSI standard		-	-	-54	dBm

*1. RSSI characteristics as shown follow.



470MHz BAND(470MHz to 510MHz) [ML7344C] High Gain Mode

Item	Condition	Min	Typ.	Max	Unit
Minimum RX sensitivity	4.8 kbps, Fdev=3kHz (BER<0.1%)	-	-116	-	dBm
	9.6 kbps, Fdev=3kHz (BER<0.1%)	-	-115	-	dBm
	4.8 kbps, Fdev=3kHz (BER<1%)	-	-118	-	dBm
	9.6 kbps, Fdev=3kHz (BER<1%)	-	-117	-	dBm
Adjacent channel rejection	±200kHz	-	55	-	dB
Blocking	1 MHz offset	-	65	-	dB
	2 MHz offset	-	66	-	dB
	6 MHz offset	-	71	-	dB
	10 MHz offset	-	73	-	dB
	-400kHz offset (image frequency), Ta=25 ºC After I/Q adjustment	-	40	-	dB
Minimum power detection level	RFmin in Figure of RSSI characteristics*1	-	-120	-	dBm
Power detection range	Dynamic Range in Figure of RSSI characteristics*1	-	35	-	dB
Spurious Emission level	Compliant with FCC, ARIB, ETSI standard	-	-	-54	dBm

170MHz Band [ML7344E]

Item	Condition		Min	Typ.	Max	Unit
Minimum RX sensitivity BER<0.1%	4.8 kbps, Fdev=3kHz		-	-115	-	dBm
	9.6 kbps, Fdev=3kHz		-	-114	-	dBm
	4.8 kbps, Fdev=3kHz High Gain Mode		-	-118	-	dBm
	9.6 kbps, Fdev=3kHz High Gain Mode		-	-117	-	dBm
Adjacent channel rejection	±12.5 kHz		-	3	-	dB
	±25 kHz		-	33	-	dB
	±50 kHz		-	36	-	dB
Blocking (426MHz operation)	1 MHz offset		-	69	-	dB
	2 MHz offset		-	72	-	dB
	6 MHz offset		-	75	-	dB
	10 MHz offset		-	80	-	dB
	-400kHz offset (image frequency), Ta=25 ºC After I/Q adjustment		-	40	-	dB
Minimum power detection level	RFmin in Figure of RSSI characteristics*1		-	-115	-	dBm
		High Gain Mode	-	-120	-	dBm
Power detection range	Dynamic Range in Figure of RSSI characteristics*1		-	40	-	dB
		High Gain Mode	-	35	-	dB
Spurious Emission level	Compliant with FCC, ARIB, ETSI standard		-	-	-54	dBm

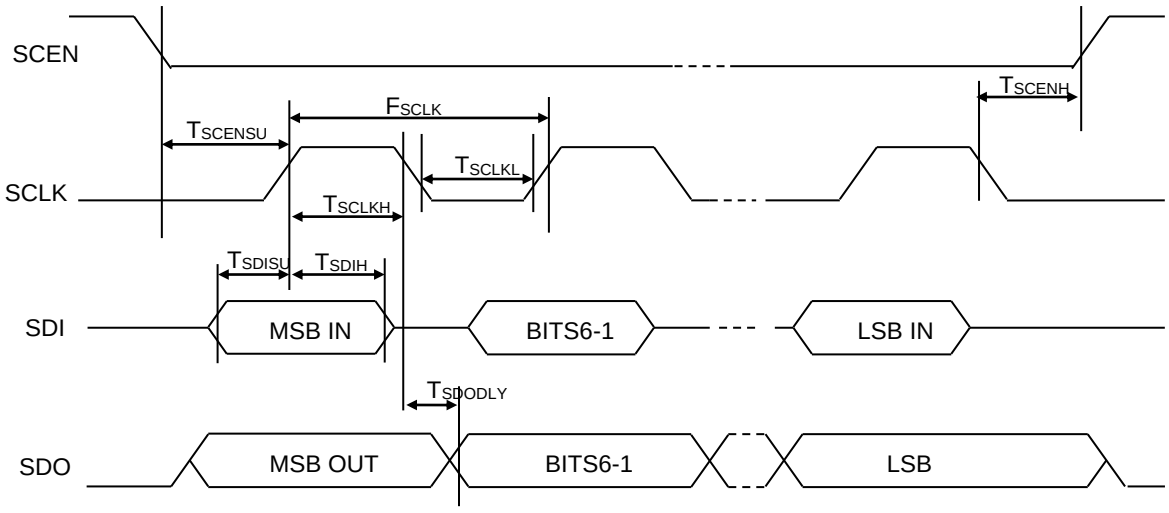
●RC oscillator circuit characteristics

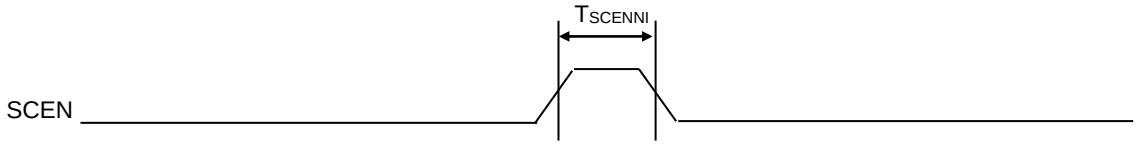
Item	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation Frequency	F_{RCOSC}		-	44	-	kHz

●SPI interface characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
SCLK clock frequency	FSCLK	Load capacitance CL=20pF	0.032	2	16	MHz
SCEN input setup time	TSCENSU		30	−	−	ns
SCEN input hold time	TSCENH		30	−	−	ns
SCLK high pulse width	TSCLKH		28	−	−	ns
SCLK low pulse width	TSCLKL		28	−	−	ns
SDI input setup time	TSDISU		5	−	−	ns
SDI input hold time	TSDIH		15	−	−	ns
SCEN negate time	TSCENNI		200	−	−	ns
SDO output delay time	TSDODLY		−	−	22	ns

NOTE: All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%.



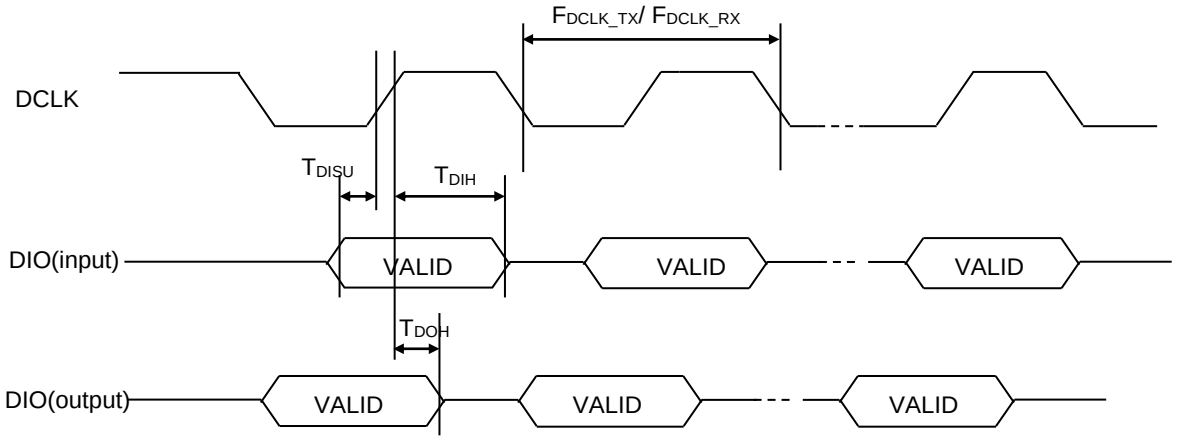


●DIO interface characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
DIO Input setup time	T_{DISU}	Load capacitance CL=20pF	1	-	-	µs
DIO Input hold time	T_{DIH}		0	-	-	ns
DIO Output hold time	T_{DOH}		20	-	-	ns
DCLK frequency accuracy in TX (*1)	F_{DCLK_TX}		(*3)	-	(*3)	kHz
DCLK frequency accuracy in RX (*2)	F_{DCLK_RX}		-30	-	+30	%
DCLK output duty ratio (TX)	D_{DCLK_TX}		45	-	55	%
DCLK output duty ratio (RX)	D_{DCLK_RX}		30	-	70	%

(*1) DCLK clock frequency in TX mode will be varied depending on the variance of master clock frequency.
(*2) DCLK clock frequency in RX mode will be varied by reproduced clock and its jitter.
(*3) These values are equal to the accuracy of the master clock frequency

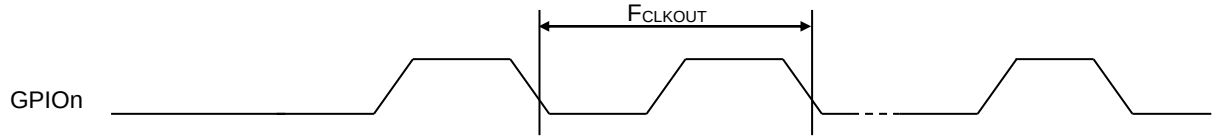
NOTE: All timing parameter is defined at voltage level of V_{DDIO} * 20% and V_{DDIO} * 80%.



●Clock output characteristics

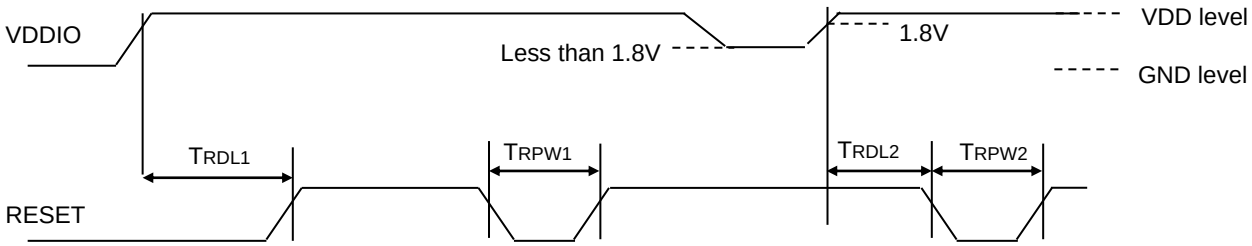
ML7344x has configurable clock output function. It is controlled by [MON_CNTRL: B0 0x4D] register and [GPIOn_CTRL: B0 0x4E-0x51)] registers (n=0 to 3),. Default settign is the 3.33MHz clock is output from GPIO1.

Item	Symbol	Condition		Min	Typ.	Max	Unit
Clock output frequency	F_{CLKOUT}	Load capacitance CL=20pF		0.0064	3.33	26	MHz
Clock output duty ratio	D_{CLKOUT}		8.66 MHz	33	-	67	%
			Other than 8.66 MHz	48	50	52	%



●Reset characteristics

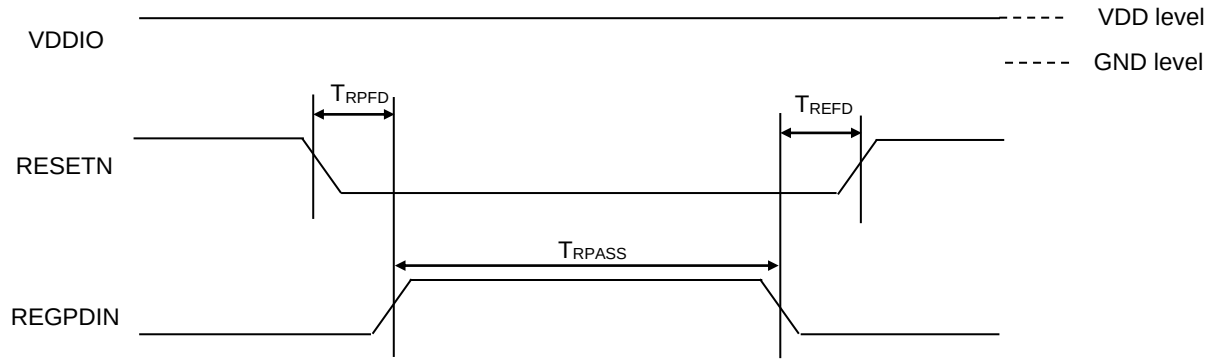
Item	Symbo	Condition	Min	Typ.	Max	Unit
RESETN delay time (Power on)	T_{RDL1}	All power supply pins (After power on)	0.5	-	-	ms
RESETN pulse period When starting from VDDIO=0V	T_{RPW1}		200	-	-	ns
RESETN pulse period 2 When starting from VDDIO≠0V	T_{RPW2}	VDDIO > 1.8V should be required.	1.5	-	-	ms
RESETN input delay time (When ML7344 start up from VDDIO≠0V)	T_{RDL2}	VDDIO > 1.8V	1	-	-	µs



NOTE: When ML7344 start up from VDDIO≠0V, RESETN pulse should be asserted after VDDIO becomes over 1.8V.

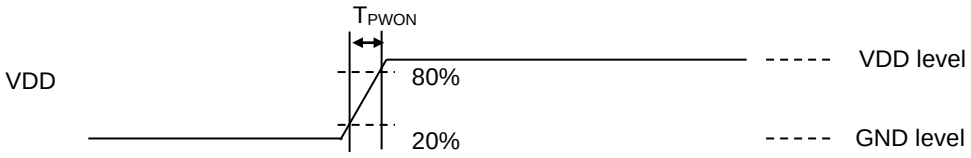
●Deep Sleep mode characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
REGPDIN assert delay time	T_{RPFD}	VDDIO = "H"	0	-	-	µs
REGPDIN assert time	T_{RPASS}		1.2	-	-	ms
RESETN release delay time	T_{REFD}		0.5	-	-	ms



●Power-on characteristics

Item	Symbol	Condition	Min	Typ.	Max	Unit
Power on time	T_{PWON}	Power on state (All power supply pins)	-	-	5	ms



■Function description

●HOST Interface

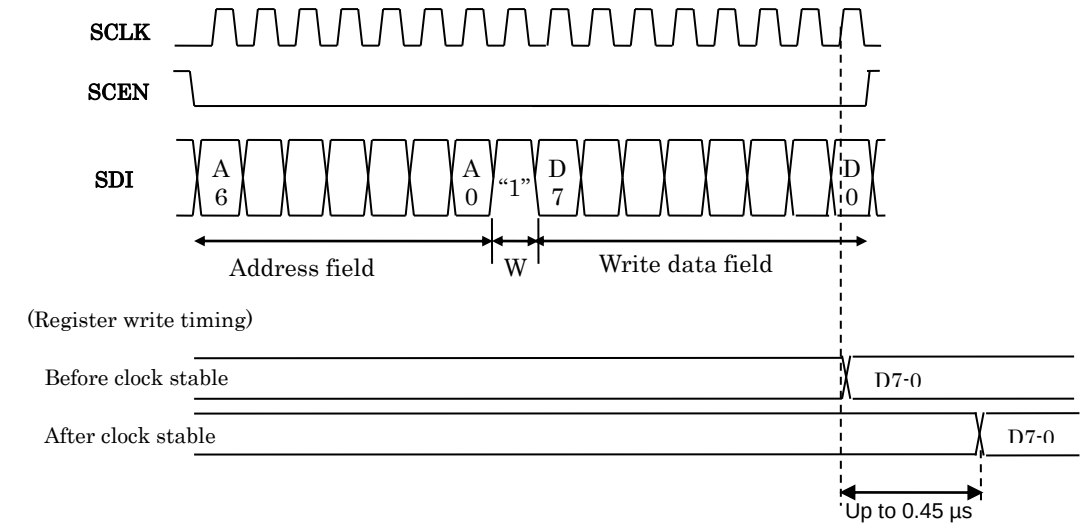
●Serial Peripheral Interface (SPI)

ML7344 has a SPI, which supports slave mode. Host MCU can read/write to the ML7344 registers and on-chip FIFO using MCU clock. Single access and burst access are also supported.

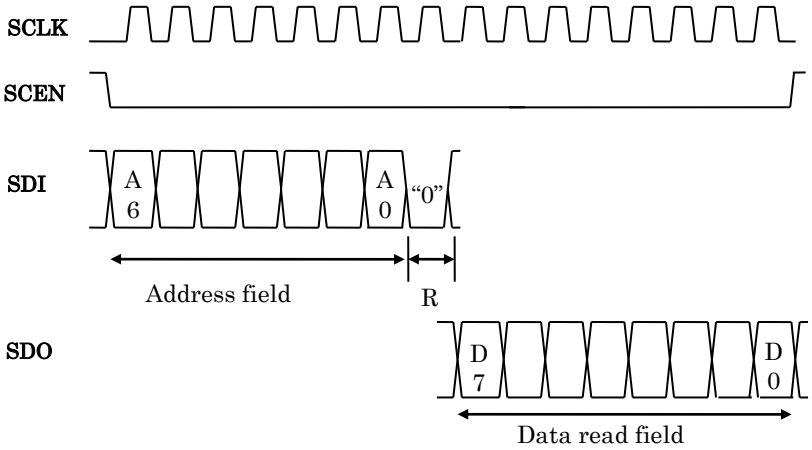
[Single Access Mode Timing Chart]

In write operation, data will be stored into internal register at rising edge of clock which is capturing D0 data. During write operation, if setting SCEN line to "H", the data will not be stored into register. For more details of SCEN negate timing, please refer to the "SPI interface characteristics". Afetr the internal clock is stabilized, data will be written into the register in syncrohonization with the internal clock.

[Write]



[Read]



[Burst Access Mode Timing Chart]

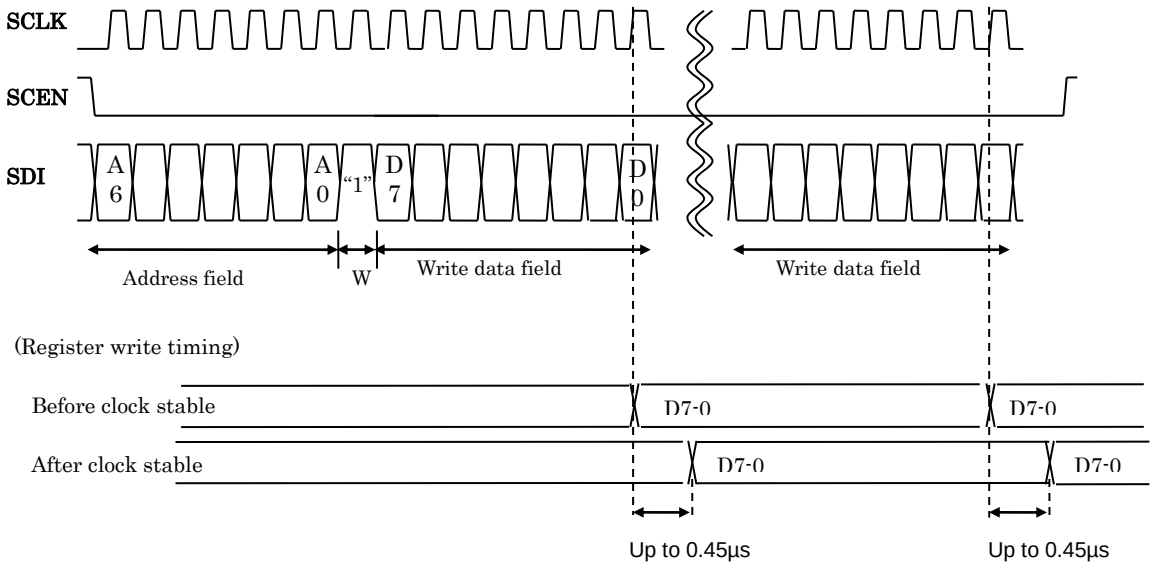
By maintaining SCEN line as “L”, burst access mode will be active. By setting SCEN line to “H”, exiting from the burst access mode. During burst access mode, address will be automatically incremented.

When SCEN line becomes “H” before Clock for D0 is input, data transaction will be aborted.

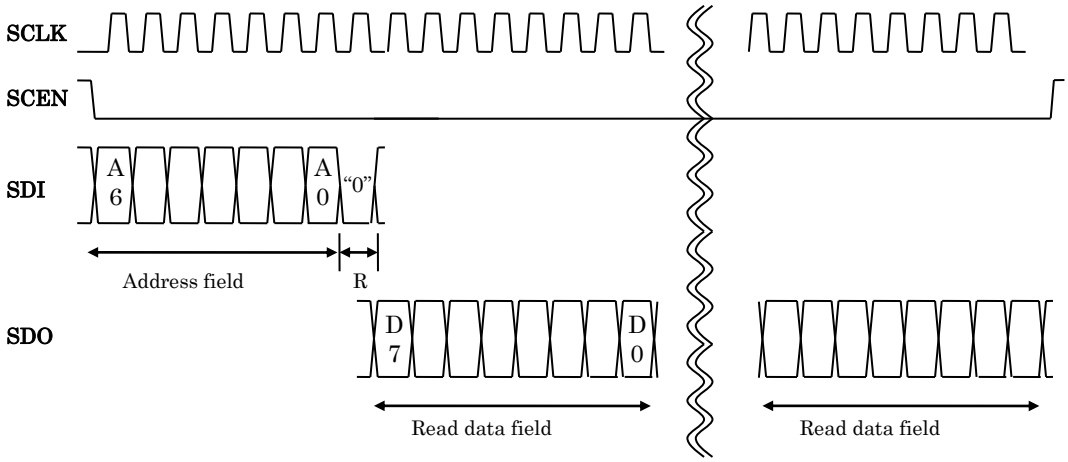
NOTE:

If destination is [WR_TX_FIFO:B0 0x7C] or [RD_FIFO:B0 0x7F], address will not be increment. And continuous FIFO access is possible.

[Write]



[Read]



●LSI state transition control

●LSI State transition instruction

State can be controlled from MCU by setting registers below.

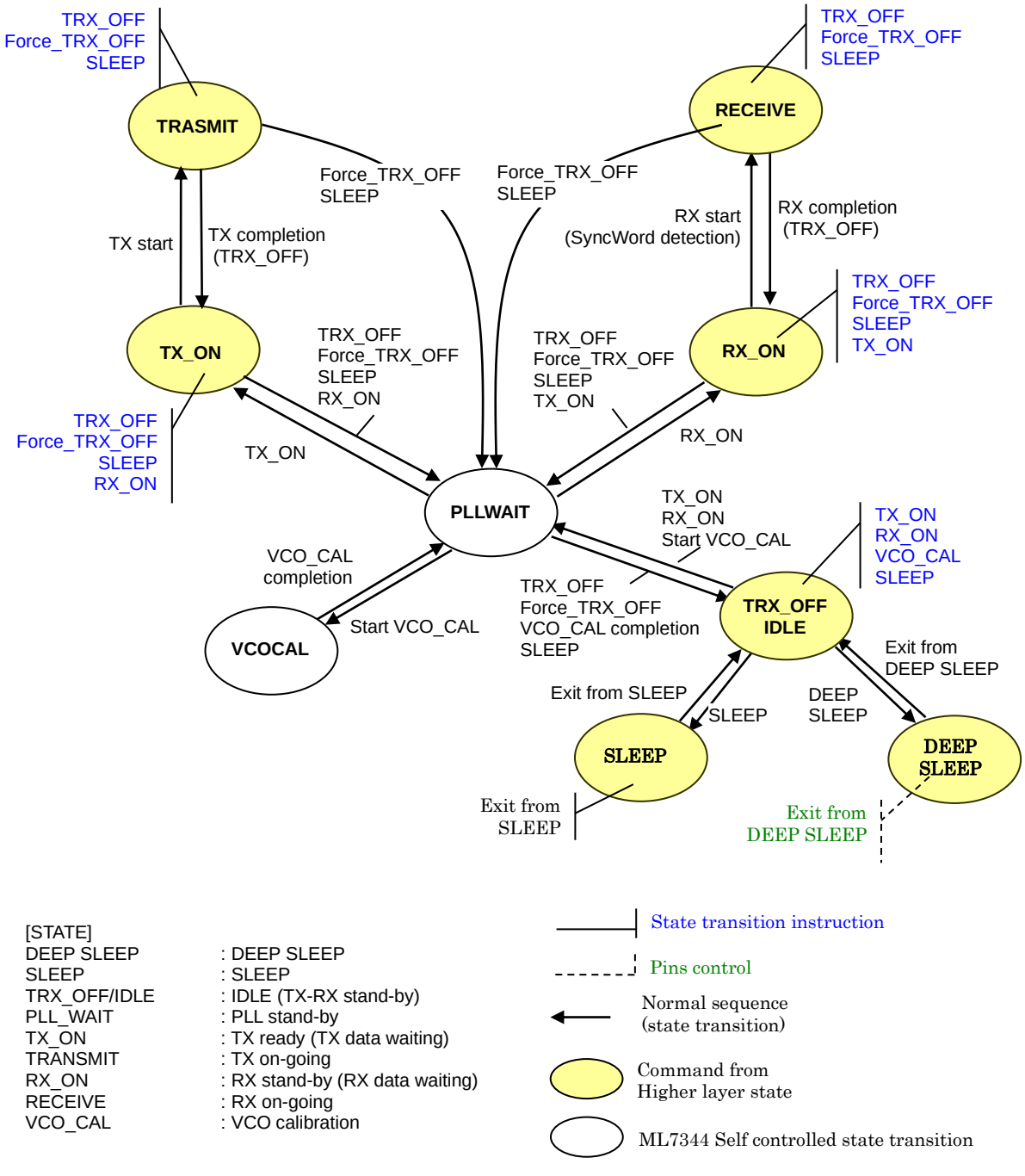
State transition command	Instruction
TX_ON	SET_TRX([RF_STATUS:B0 0x0B(3-0)])=0b1001
RX_ON	SET_TRX([RF_STATUS:B0 0x0B(3-0)])=0b0110
TRX_OFF	SET_TRX([RF_STATUS:B0 0x0B(3-0)])=0b1000
Force_TRX_OFF	SET_TRX([RF_STATUS:B0 0x0B(3-0)])=0b0011
SLEEP_EN	SLEEP_EN([SLEEP/WU_SET:B0 0x2D(0)])=0b1
VCO_CAL_EN	VCO_CAL_START([VCO_CAL_START:B0 0x6F(0)])=0b1

State can be changed without command from MCU. If one of the following condition is met, state is changed automatically according to the following table. In order to enable these functions, the following registers must be programmed.

Function	Control bit name
Automatic TX_ON after FIFO write completion (AUTO_TX)	AUTO_TX_EN([RF_STATUS_CTRL:B0 0x0A(4)])
Automatic TX_ON during FIFO write (FAST_TX)	FAST_TX_EN([RF_STATUS_CTRL:B0 0x0A(5)])
RF state setting after packet transmission completion	TXDONE_MODE[1:0]([RF_STATUS_CTRL:B0 0x0A(1-0)])
RF state setting after packet reception completion	RXDONE_MODE[1:0]([RF_STATUS_CTRL:B0 0x0A(3-2)])
Automatic RX_ON/TX_ON by Wake-up timer	WAKEUP_MODE([SLEEP/WU_SET:B0 0x2D(6)]) WAKEUP_EN([SLEEP/WU_SET:B0 0x2D(4)])
Automatic VCO calibration after exit from SLEEP	AUTO_VCOCAL_EN([VCO_CAL_START:B0 0x6F(4)])
Automatic SLEEP by timer	WU_DURATION_EN([SLEEP/WU_SET:B0 0x2D(5)])
Automatic SLEEP by high speed carrier checking mode	FAST_DET_MODE_EN([CCA_CTRL:B0 0x39(3)])
Force_TRX_OFF after PLL unlock detection during TX	PLL_LD_EN([PLL_LOCK_DETECT:B1 0x0B(7)])

●State Diagram

Each state transition control is described in the following state diagram.



[STATE]

DEEP SLEEP	: DEEP SLEEP
SLEEP	: SLEEP
TRX_OFF/IDLE	: IDLE (TX-RX stand-by)
PLL_WAIT	: PLL stand-by
TX_ON	: TX ready (TX data waiting)
TRANSMIT	: TX on-going
RX_ON	: RX stand-by (RX data waiting)
RECEIVE	: RX on-going
VCO_CAL	: VCO calibration

Fig.3 LSI state diagram

●SLEEP setting

Deep SLEEP mode: Powers for all blocks except for IO pins are turned off.
SLEEP mode: Main regulator and 26MHz oscillation circuits are turned off. But sub-regulator is turned-on.
The following registers can be programmed to control SLEEP state

Function	Control bit name
Power control	PDN_EN([SLEEP?WU_SET:B0 0x2D(1)])
Wake-up setting	WAKEUP_EN([SLEEP/WU_SET:B0 0x2D(4)])
Wake-up timer clock source setting	WUT_CLK_SOURCE([SLEEP/WU_SET:B0 0x2D(2)])
Internal RC oscillator control	RC32K_EN([CLK_SET2:B0 0x03(3)])

Setting method and internal state for DEEP_SLEEP and various SLEEP modes are as follows:

SLEEP mode	Setting method	main regulator	Sub regulator	26MHz oscillator	RC oscilator	Low clock timer	FIFO
DEEP_SLEEP	RESETN pin="L" REGPDIN pin="H"	OFF	OFF	OFF	OFF	OFF	OFF
SLEEP1	[SLEEP/WU_SET: B0 0x2D(4-0)] = 0b0_1011 (*2) [CLK_SET2: B0 0x03(3)] = 0b0 (default)	OFF	ON	OFF	OFF	OFF	OFF
SLEEP2	[SLEEP/WU_SET: B0 0x2D(4-0)] = 0b0_1001 (*2) [CLK_SET2: B0 0x03(3)] = 0b0 (default)	OFF	ON	OFF	OFF (*1)	OFF	ON
SLEEP3	[SLEEP/WU_SET: B0 0x2D(4-0)] = 0b1_1001 (*2) [CLK_SET2: B0 0x03(3)] = 0b0 (default)	OFF	ON	OFF	OFF	ON	ON
SLEEP4	[SLEEP/WU_SET: B0 0x2D(4-0)] = 0b1_1101 (*2) [CLK_SET2: B0 0x03(3)] = 0b1	OFF	ON	OFF	ON	ON	ON

(*1) Low speed clock is supplied from EXT_CLK pin.
(*2) Please set proper value to [SLEEP/WU_SET: B0 0x2D(3)].

NOTE: Contents of registers are not kept during DEEP_SLEEP. Contents of registers are kept during SLEEP1, SLEEP2, SLEEP3 and SLEEP4.
However, in SLEEP1 mode, contents of TX FIFO and RX FIFO are not kept, because power to FIFO is turned off.

●Notes to set RF state

ML7344 is able to change the internal RF state transition autonomously (without commands from MCU) as well as RF state change commands from MCU. (please refer to "LSI state transition instruction"). If both timing of operation (autonomous state and state change from MCU command) overlapped, unintentional RF state may occur. Timing of autonomous state RF change is described in the following table.
Care must be taken not to overlap the conditions.

Function	RF state change (before → after)	RF state transition timing (not from Host MCU command)	Recommended process
Automatic TX	TRX_OFF/RX_ON →TX_ON	After TX data transfer completion interrupt occurs, {value [TX_RATE_H/L: B1 0x02/03)] × 2 / 26}[µs] period	Write access to [RF_STATUS:B0 0x0B] is possible after RF state transition completion interrupt (INT[3] group1), or move to the state defined by GET_TRX ([RF_STATUS:B0 0x0B(7-4)]).
FAST_TX mode		When FIFO write access exceed trigger level +1, {value [RX_RATE1_H/L:B1 0x04/05] × 5 / 26}[µs] period.	
RF state setting after TX completion	TX_ON→TRX_OFF	After TX completion interrupt (INT[16] group3), {value [TX_RATE_H/L:B1 0x02/03] × 2 / 26} [µs] period	
	TX_ON→RX_ON		
	TX_ON→SLEEP		
RF state setting after RX completion	RX_ON→TRX_OFF	After RX completion interrupt (INT[8] group2), {value [RX_RATE1_H/L:B1 0x04/05] × 2 / 26}[µs] period	
	RX_ON→TX_ON		
	RX_ON→SLEEP		
Wake-up timer	SLEEP→TX_ON	After wake-up timer completion interrupt (INT[6] group1), 1 clock cycle period defined by WUT_CLK_SET[3:0] ([WUT_CLK_SET: B0 0x2E(3-0)]).	
	SLEEP→RX_ON		
	SLEEP→VCO_CAL →TX_ON	After wake-up timer completion interrupt (INT[6] group1), before VCO calibration completion interrupt (INT[1] group1).	Write access to [RF_STATUS:B0 0x0B] and BANK2 is possible after VCO calibration completion interrupt (INT[1] group1).
	SLEEP→VCO_CAL →RX_ON		
Continuous operation timer	TX_ON→SLEEP	After continuous operation timer completion, 1 clock cycle period defined by WUT_CLK_SET [3:0] ([WUT_CLK_SET: B0 0x2E(3-0)]).	Write access to [RF_STATUS:B0 0x0B] is possible after RF state transition completion interrupt (INT[3] group1), or move to the state defined by GET_TRX ([RF_STATUS:B0 0x0B(7-4)]).
	RX_ON→SLEEP		
High speed carrier checking	RX_ON→SLEEP	After CCA completion interrupt (INT[18] group3), duration 6.3[µs].	
PLL unlock detection	TX_ON→TRX_OFF	After PLL unlock detection interrupt (INT[2] group1) occurs, duration 147[µs].	Write access to [RF_STATUS:B0 0x0B] is possible 147µs after PLL unlock interrupt (INT[2] group1) detected.

●Packet Handling Function

●Packet format

ML7344 supports Wireless M-BUS frame FormatA/B, and Format C which is non Wireless M-BUS universal format. The following packet handling are supported in FIFO mode or DIO mode

1) Preamble and SyncWord automatic insertion (TX) --- DIO/FIFO mode
2) Preamble and SyncWord automatic detection (RX) --- DIO/FIFOmode
3) Preamble and SyncWord automatic deletion (RX) --- DIO/FIFO mode
4) CRC data insertion (TX) --- FIFO mode
5) CRC check and error notification (RX) --- DIO/FIFO mode

The following table shows the control bit relating with Packet format function.

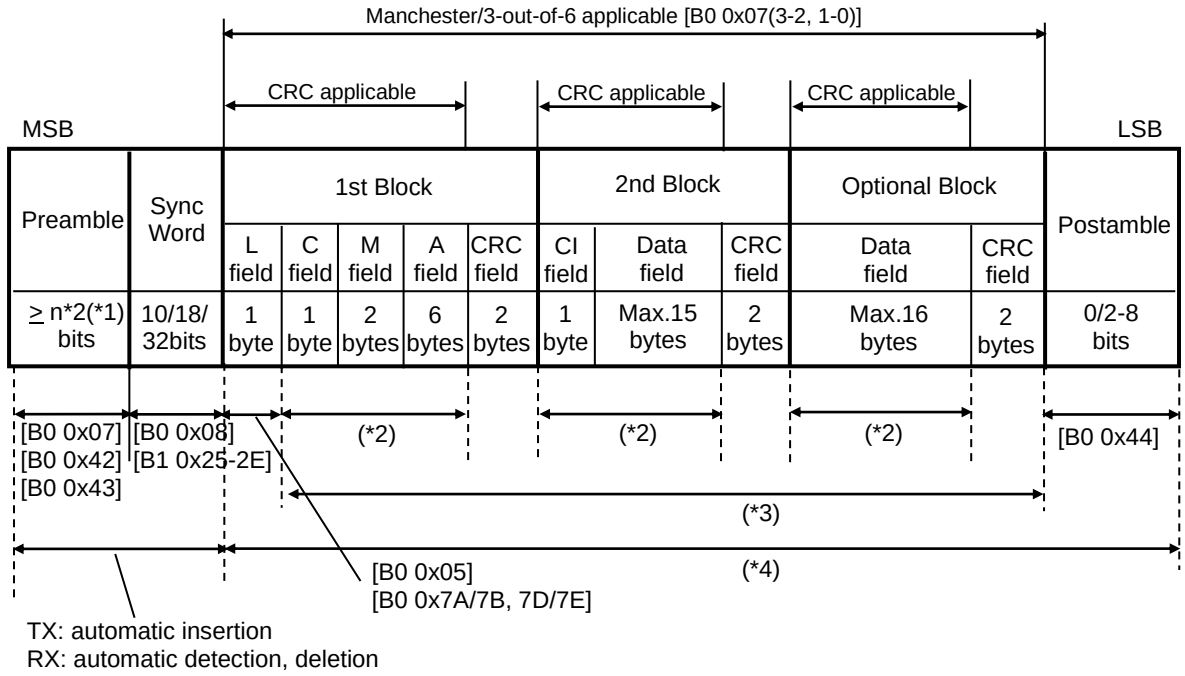
Function	Control bit name
Packet format setting	PKT_FORMAT[1:0] ([PKT_CTRL1: B0 0x04(1-0)])
RX extended link layer mode disable	RX_EXTPKT_OFF ([PKT_CTRL1: B0 0x04(3)])
Data area bit order setting	DAT_LF_EN ([PKT_CTRL1: B0 0x04(4)])
Length area bit order setting	LEN_LF_EN ([PKT_CTRL1: B0 0x04(5)])
Extended link layer mode setting	EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])
Length field setting	LENGTH_MODE ([PKT_CTRL2: B0 0x05(0)])

(1) Format A (Wireless M-BUS)

By setting PKT_FORMAT[1:0] ([PKT_CTRL1: B0 0x04(1-0)])=0b00, Wireless M-BUS Format A is selected.

Format A consists of 1st Block, 2nd Block and Optional Block(s). Each block has 2 bytes of CRC. "L-field" (1st byte of 1st Block) indicates packet length, which includes subsequenct user data bytes from "C-field". However, CRC bytes and postanble are excluded. Depending on "L-field" value, 2nd Block and Optional Block(s) are added.

The following [] indicates register address [bank #, address].



*1: Each mode has different minimum value of n.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

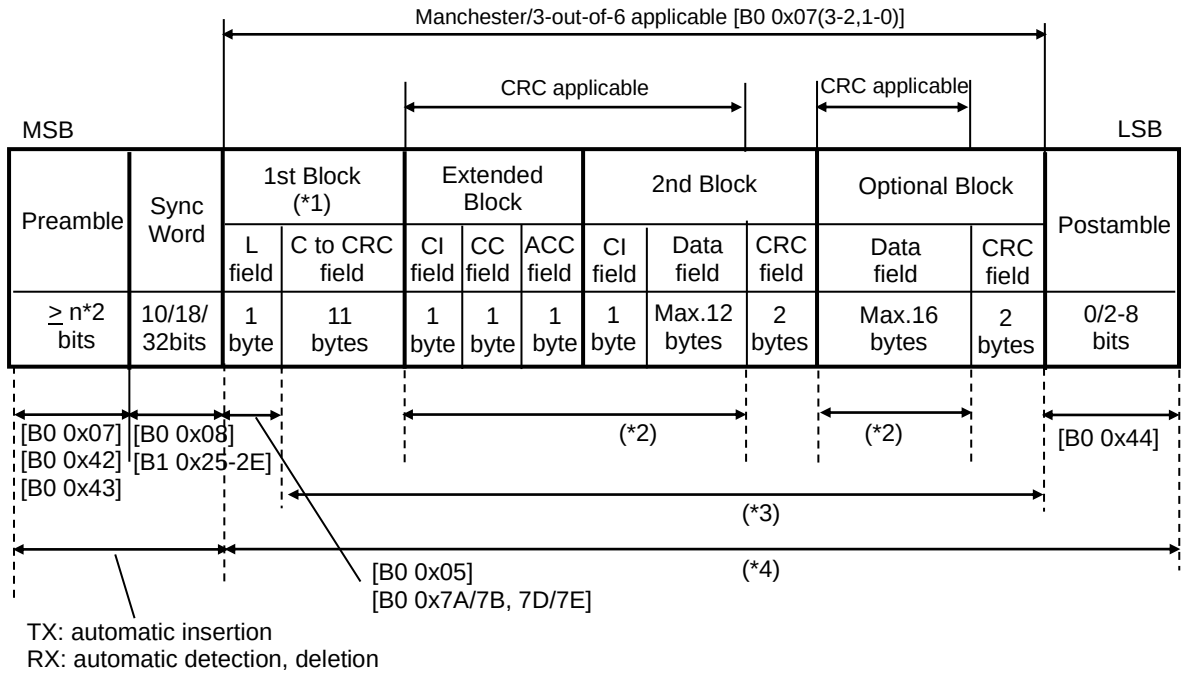
Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block)=0x8C or 0x8D, Extended Link Layer is applied. The packet format is as follows:

(1) CI-field = 0x8C

For TX, if 2 bytes extention format is used, set EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])=0b01.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7344 recognizes "CI-field" and RX operation is processed.

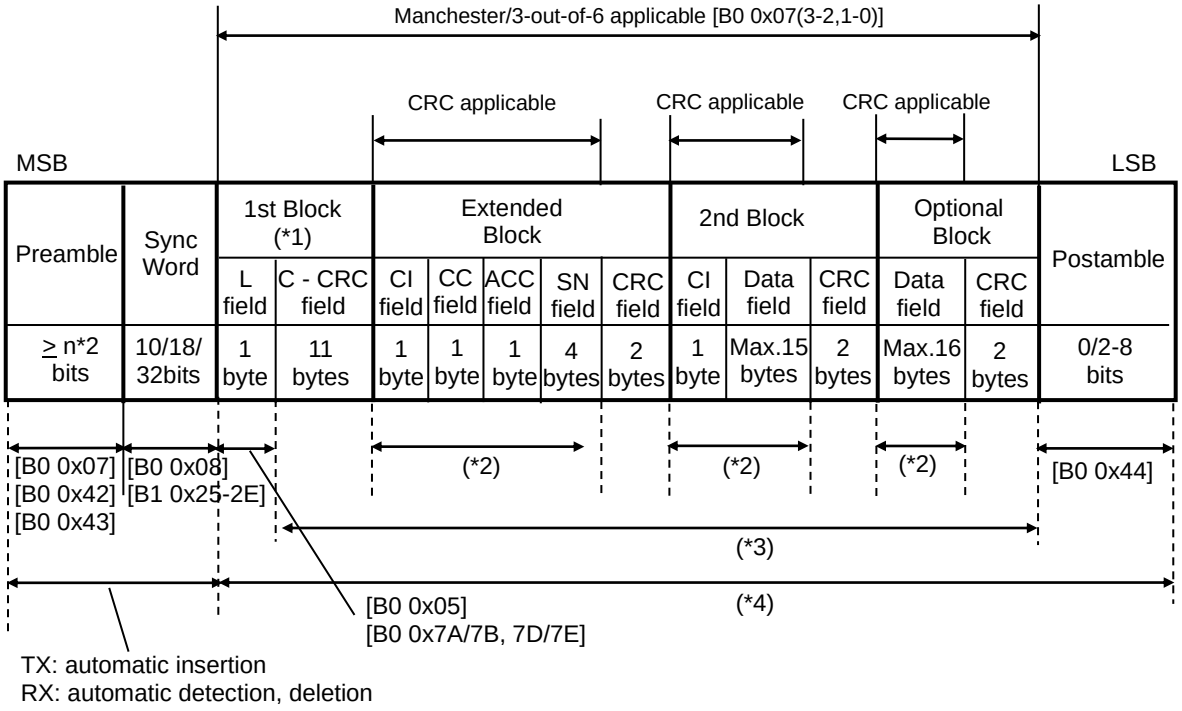


*1: 1st Block is identical to normal Format A.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

(2) CI-field = 0x8D

For TX, if 8 bytes extention format is used, set EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])=0b10.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7344 recognizes "CI-field" and RX operation is processed.



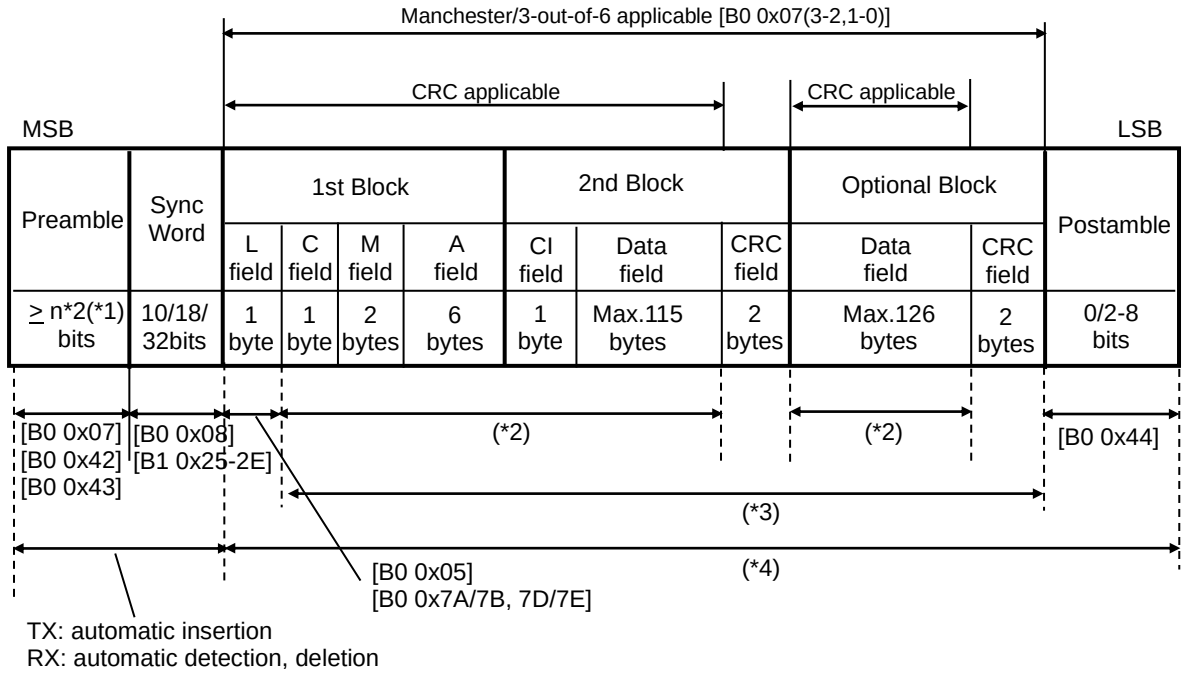
*1: 1st Block is identical to normal Format A.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

(2) Format B (Wireless M-BUS)

By setting PKT_FORMAT[1:0] ([PKT_CTRL1: B0 0x04(1-0)])=0b00, Wireless M-BUS Format B is selected.

Format B consists of 1st Block, 2nd Block and Optional Block(s). Each block has 2 bytes of CRC. "L-field" (1st byte of 1st Block) indicates packet length, which includes subsequenct user data bytes from "C-field". However, unlike Format A, CRC bytes are included. (postanble are excluded.) Depending on "L-field" value, 2nd Block and Optional Block(s) are added.

The following [] indicates register address [bank #, address].



*1: Each mode has different minimum value of n.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

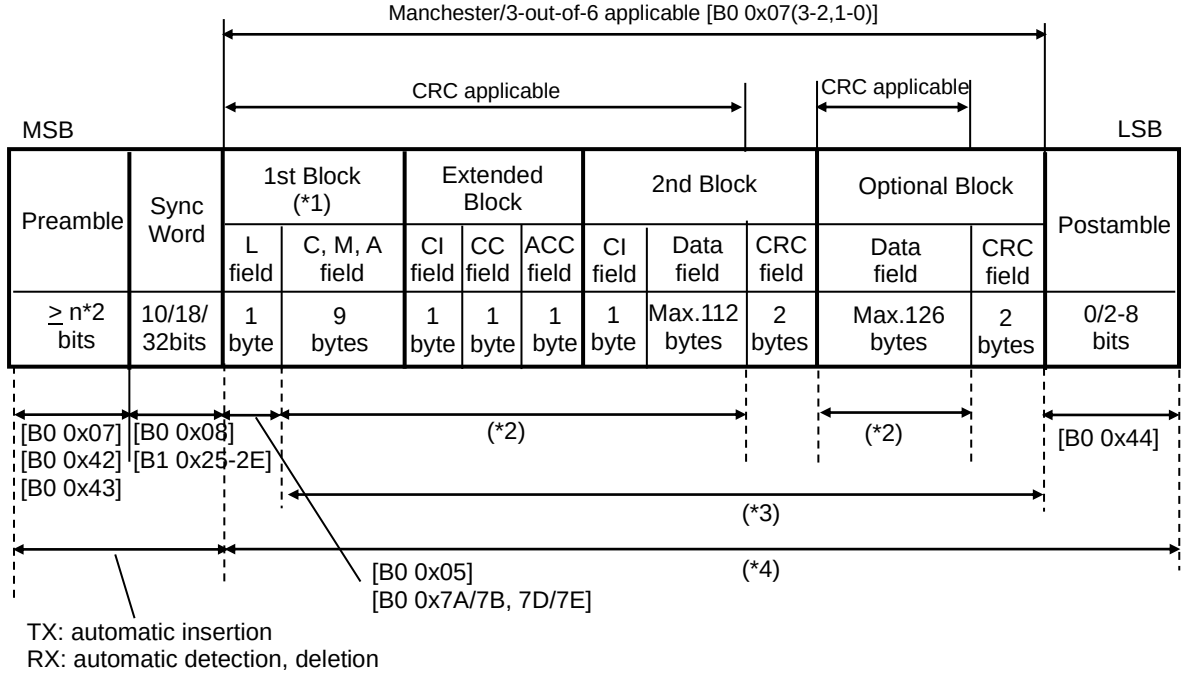
Extended Link Layer Format

If "CI-field" (1st byte of 2nd Block)=0x8C or 0x8D, Extended Link Layer is applied. The packet format is as follows:

(1) CI-field = 0x8C

For TX, if 2 bytes extention format is used, set EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])=0b01.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7344 recognizes "CI-field" and RX operation is processed.

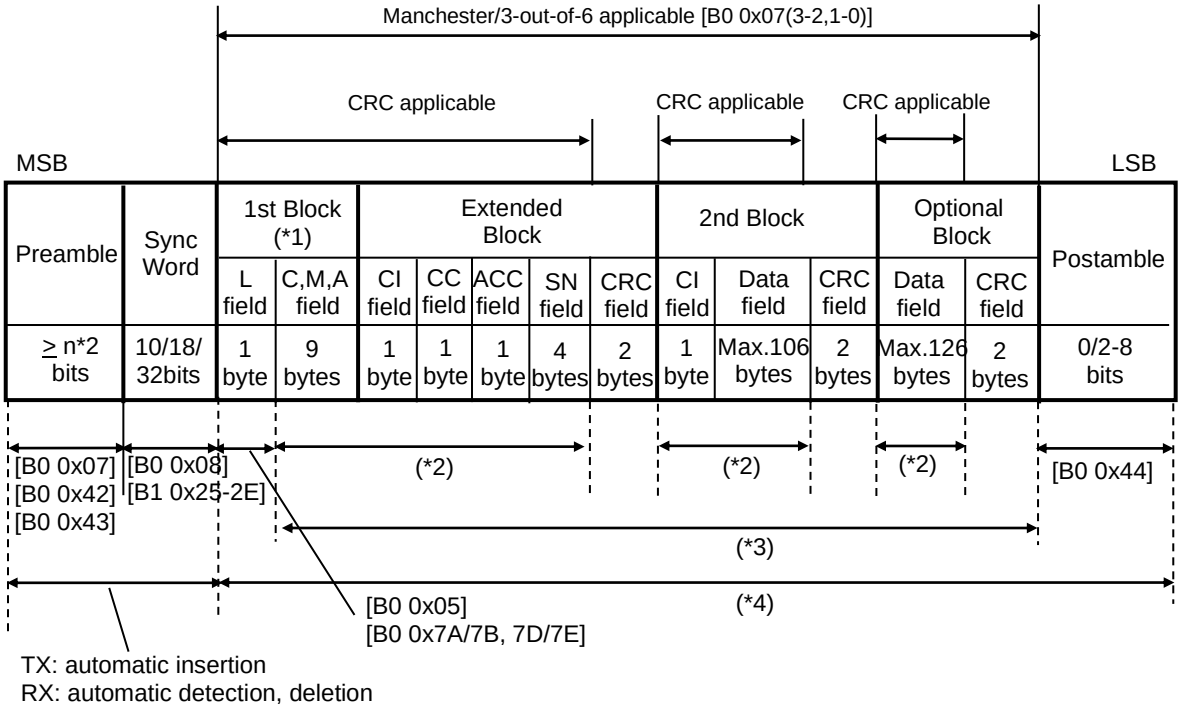


*1: 1st Block is identical to normal Format B.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

(2) CI-field = 0x8D

For TX, if 8 bytes extention format is used, set EXT_PKT_MODE[1:0] ([PKT_CTRL1: B0 0x04(7-6)])=0b10.

For RX, if RX_EXTPKT_OFF([PKT_CTRL1: B0 0x04(3)])=0b0, ML7344 recognizes "CI-field" and RX operation is processed.

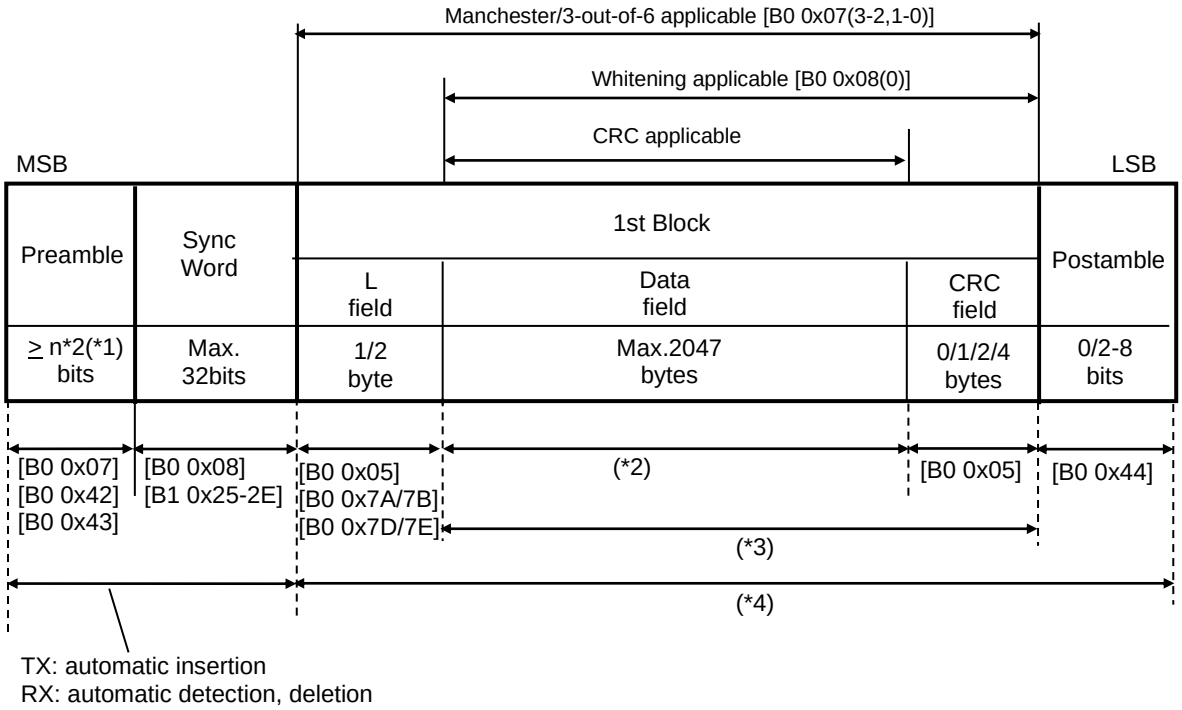


*1: 1st Block is identical to normal Format B.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

(3) Format C (non Wireless M-BUS, general purpose format)

By setting PKT_FORMAT([PKT_CTRL1: B0 0x04(1-0)])=0b10, Format C, which is non Wireless M-BUS format, is selected. Format C consists of 1st Block only, which has 2 bytes of CRC. "L-field" indicates packet length, which includes subsequent user data bytes, including CRC bytes. The length of "L-field" is defined by LENGTH_MODE ([PKT_CTRL2:B0 0x5(0]). Data Whitening function is supported.

The following [] indicates register address [bank #, address].



*1: Preamble length (n) is programable by [TXPR_LEN_H/L: B0 0x42/43] registers.
*2: Indicates TX FIFO data storage area size.
*3: Indicates RX FIFO data storage area size.
*4: When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10, indicates DCLK/DIO output area.

●CRC function

ML7344 has CRC32,CRC16 and CRC8 function. CRC is calculated and appended to TX data. CRC is checked for RX data. The following modes are used for automatic CRC function.

●FIFO mode: RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b00
●DIO mode: RXDIO_CTRL ([DIO_SET: B0 0x0C(7-6)]) = 0b11

Function	Control bit name / Register
TX CRC setting	TX_CRC_EN([PKT_CTRL2: B0 0x05(2)])
RX CRC setting	RX_CRC_EN([PKT_CTRL2: B0 0x05(3)])
CRC length setting	CRC_LEN([PKT_CTRL2: B0 0x05(5-4)])
CRC complement value OFF setting	CRC_COMP_OFF([PKT_CTRL2: B0 0x05(6)])
CRC polynomial setting	[CRC_POLY3/2/1/0: B1 0x16/17/18/19] registers
CRC error status	[CRC_ERR_H/M/L: B0 0x13/14/15] registers

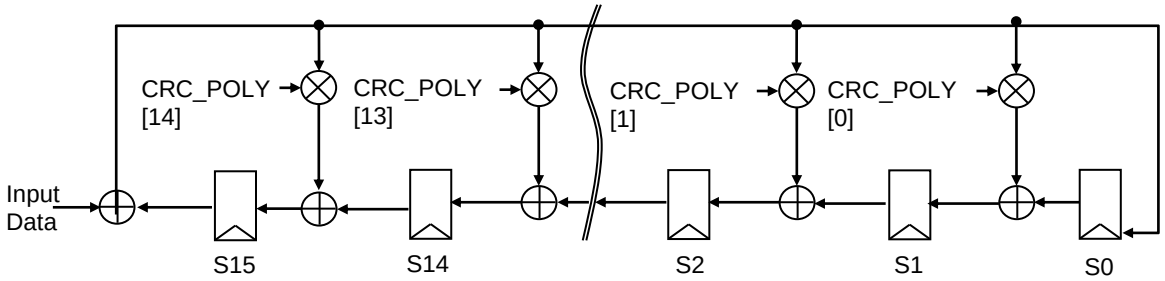
Any CRC polynomials for CRC32/CRC16/CRC8 can be specified. Reset value is as follows:

CRC16 polynomial = $x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$ (reset value)

NOTE: CRC result data can be inverted by CRC complement value OFF setting,

CRC data will be generated by the following circuits. By programming [CRC_POLY3/2/1/0] registers, any CRC polynomials can be supported. Generated CRC will be transfer from the most left bit (S15). If data length is shorter than CRC length (3 bytes of CRC32 only), data "0"s will be added for CRC calculation. CRC check result is stored in [CRC_ERR_H/M/L] registers.

Unlike Format C, Format A/B can include multiple CRC fields in one packet. For multiple CRCs check results, CRC value closest to L-field will be stored in CRC_ERR[0] ([CRC_ERR_L:B0 0x15(0)]). Subsequent bit will be stored in CRC_ERR from MSB order.



NOTE: ⊕ exclusive OR

Fig.4 CRC16 polynomial circuits

General CRC polynomial can be programmed by below [CRC_POLY3/2/1/0] register setting.
CRC length can be set by CRC_LEN.

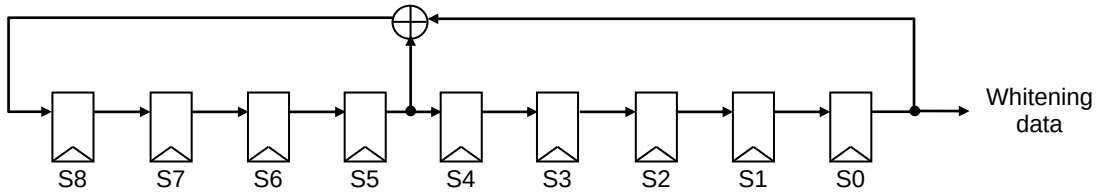
CRC polynomial		[CRC_POLY3/2/1/0]			
		(B1 0x16)	(B1 0x17)	(B1 0x18)	(B1 0x19)
CRC8	$x^8 + x^2 + x + 1$	0x00	0x00	0x00	0x03
CRC16	$x^{16} + x^{12} + x^5 + 1$	0x00	0x00	0x08	0x10
	$x^{16} + x^{15} + x^2 + 1$	0x00	0x00	0x40	0x02
	$x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^8 + x^6 + x^5 + x^2 + 1$	0x00	0x00	0x1E	0xB2
CRC32	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$	0x02	0x60	0x8E	0xDB

●Data whitening function (non Wireless M-BUS standard)

ML7344 supports Data whitening function. In packet format A/B, subsequent data followed by C-field can be processed data whitening. In packet format C, data Whitening is applied from data field. Data generated by the following 9 bit pseudo random sequence (PN9) will be "XOR" with TX data (encoded data if Manchester or 3-out-of 6 coding is selected) before transmission. Intialization value of the PN9 generation shift register can be defined by [WHT_INIT_H/L: B1 0x64/65] registers. PN9 polynomial can be programmed with [WHT_CFG: B1 0x66] register.

Function	Control bit name
Data whitening setting enable	WHT_SET ([DATA_SET2: B0 0x08(0)])
Data whitening initialization value	WHT_INIT[8:0] ([WHT_INIT_H/L: B1 0x64(0)/65(7-0)])
Whitening polynomial	WHT_CFG[7:0] ([WHT_CFG: B1 0x66(7-0)])

In order to make feedback from S1 register, setting 0b1 to WHT_CFG0 ([WHT_CFG: B1 0x66(0)]). Similaly in order to make feedback from S2 register, setting 0b1 to WHT_CFG1 ([WHT_CFG: B1 0x66(1)]). Other bits of [WHT_CFG: B1 0x66] register has same function. Two or more bits can be also set to 0b1. Therefore any type of PN9 polinominal can be programmed.



NOTE: ⊕ exclusive OR

Fig.5 Whitening data generation circuits
(generator polynomial: $x^9 + x^5 + 1$)

General PN9 polynomial can be defined by WHT_CFG[7:0].

PN9 polynomial	WHT_CFG[7:0] [WHT_CFG: B1 0x66]
$x^9 + x^4 + 1$	0x08
$x^9 + x^5 + 1$	0x10

●SyncWord detection function

ML7344 supports automatic SyncWord recognition function. By having two sets of SyncWord pattern storage area, it is possible to detect two different packet format (Format A/B) which are defined by Wireless M-Bus. (For details, please refer to Wireless M-BUS standard) Receiving packet format is indicated by SW_DET_RSLT([STM_STATE:B0 0x77(5)]). In Format C, it is possible to search for two SyncWords but detected result is not indicated.

1) TX

SyncWord pattern defined by SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) will be selected. SyncWord length for TX is defined by SYNC_WORD_LEN[5:0] ([SYNC_WORD_LEN: B1 0x25(5-0)]). From high bit of each SyncWord pattern will be transmitted.

SYNCWORD_SEL	TX SyncWord pattern
0	SYNC_WORD1[31:0] ([SYNCWORD1_SET3/2/1/0: B1 0x27/28/29/2A])
1	SYNC_WORD2[31:0] ([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E])

[Example] SyncWord patten and SyncWord length

If the follwing registers are programmed, from higher bit of SYNC_WORD1[17:0] will be transmitted sequencially.

[SYNC_WORD_LEN: B1 0x25]=0x12

SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b0

If the following registers are programmed, from higher bit of SYNC_WORD2[23:0] will be transmitted sequencially.

[SYNC_WORD_LEN: B1 0x25]=0x18

SYNCWORD_SEL ([DATA_SET2: B0 0x08(4)]) = 0b1

2) RX

By setting SYNCWORD_SEL and 2SW_DET_EN ([DATA_SET2: B0 0x08(4,3)]), One SyncWord pattern waiting or two SyncWord patterns waiting can be selected as follows: Packet format automatic detection is valid if 2SW_DET_EN=0b1 and Format A or Fromat B is selected by PKT_FORMAT[1:0] ([PKT_CTRL1:B0 0x04(1-0)]).

2SW_ DET_EN	SYNCWORD _SEL	SyncWord pattern During Sync Detection	SyncWord Detection operation	Automatic packet format detection	Data process after SyncWord
0	0	SYNC_WORD1[31:0]	Waiting for 1 pattern	no	Process according to each Format setting
0	1	SYNC_WORD2[31:0]	Waiting for 1 pattern	no	Process according to each Format setting
1	–	SYNC_WORD1[31:0] SYNC_WORD2[31:0]	Waiting for 2 patterns	yes	[Format A or Format B setting] If matched with SYNC_WORD1, then process as Format A. If matched with SYNC_WORD2, then process as Format B. [Format C setting] Process as Format C

Length of SyncWord pattern can be defined by SYNC_WORD_LEN[5:0] ([SYNC_WORD_LEN: B1 0x25(5-0)]). In this case, SyncWord pattern defined by the length from low bit of SYNC_WORD1[31:0] or SYNC_WORD2[31:0] will be the pattern for checking.

[Example] SyncWord length

If the following registers are set, 18 bit of SYNC_WORD1[17:0] or SYNC_WORD2[17:0] will be reference pattern for the SyncWord detection. Higher bits (bit31-18) are not checked.

[SYNC_WORD_LEN: B1 0x25]=0x12

[SYNC_WORD_EN: B1 0x26]=0x0F

32bit SyncWord pattern can be controlled by enabling/disabling by each 8bit, when receiving SyncWord. The following table describes enable/disable control and SyncWord pattern.

[SYNC_WORD_EN] (B1 0x26)	SYNC_WORD*				SyncWord detection operation
	[31:24]	[23:16]	[15:8]	[7:0]	
0000					No SyncWord detection
0001	D.C.(*1)			ON	Only [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0010	D.C.		ON	D.C.	Only [15:8] are valid. Upon [7:0] detection, SyncWord detection.
0011	D.C.		ON	ON	[15:0] are valid. Upon [7:0] detection, SyncWord detection.
0100	D.C.	ON	D.C.		Only [23:16] are valid. Upon [7:0] detection, SyncWord detection.
0101	D.C.	ON	D.C.	ON	[23:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
0110	D.C.	ON	ON	D.C.	[23:8] are valid. Upon [7:0] detection, SyncWord detection.
0111	D.C.	ON	ON	ON	[23:0] are valid. Upon [7:0] detection, SyncWord detection.
1000	ON	D.C.			Only [31:24] are valid. Upon [7:0] detection, SyncWord detection.
1001	ON	D.C.		ON	[31:24] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1010	ON	D.C.	ON	D.C.	[31:24] and [15:8] are valid. Upon [7:0] detection, SyncWord detection.
1011	ON	D.C.	ON	ON	[31:24] and [15:0] are valid. Upon [7:0] detection, SyncWord detection.
1100	ON	ON	D.C.		[31:16] are valid. Upon [7:0] detection, SyncWord detection.
1101	ON	ON	D.C.	ON	[31:16] and [7:0] are valid. Upon [7:0] detection, SyncWord detection.
1110	ON	ON	ON	D.C.	[31:8] are valid. Upon [7:0] detection, SyncWord detection.
1111	ON	ON	ON	ON	Whole [31:0] are valid. Upon [7:0] detection, SyncWord detection.

(*1) D.C. stands for Don't Care.

(*2) Preamble pattern can be added to the SyncWord detection conditions by RXPR_LEN[5:0] ([SYNC_CONDITION1 :B0 0x45(5-0)]).

●Field check function

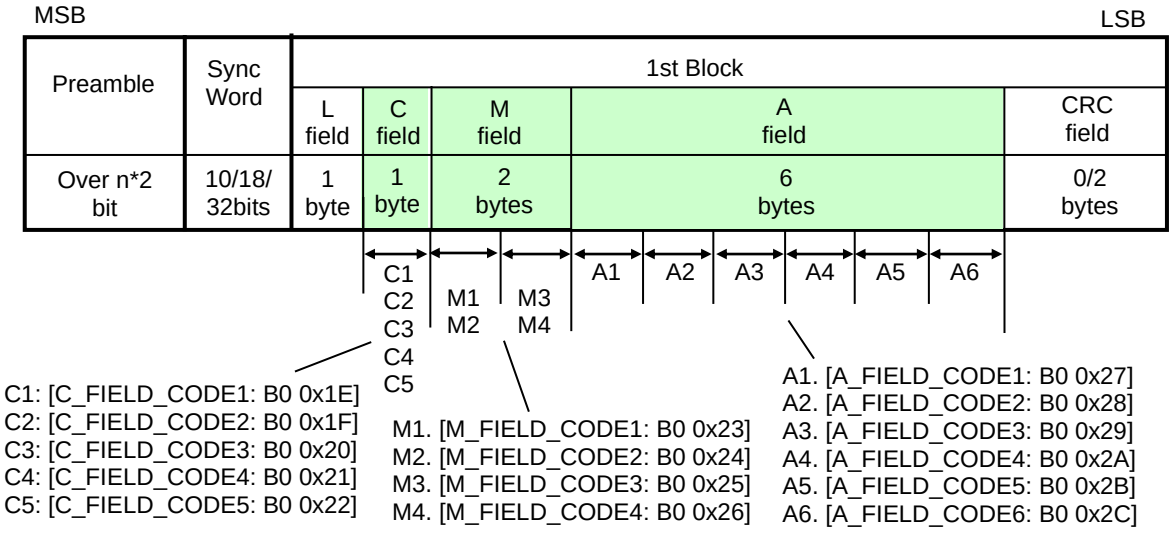
ML7344 has the function of comparing the 9 bytes following L-field (Format A/B: start from C-field, Format C: start from Data-field) in a receiving packet. Based on comparison with the expected data, possible to generate interrupts (Field check function). Field check can be possible with the following register setting. When using this function, RXDIO_CTRL [1:0] ([DIO_SET:B0 0x0C(7-6)]) = 0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required.

Function	Register
RX data process setting when Field check unmatched	[C_CHECK_CTRL: B0 0x1B(7)]
Field check interrupt setting	[C_CHECK_CTRL: B0 0x1B(6)]
C-field detection enable setting	[C_CHECK_CTRL: B0 0x1B(4-0)]
M-field detection enable setting	[M_CHECK_CTRL: B0 0x1C(3-0)]
A-field detection enable setting	[A_CHECK_CTRL: B0 0x1D(5-0)]
C-field code setting	[C_FIELD_CODE1: B0 0x1E] [C_FIELD_CODE2: B0 0x1F] [C_FIELD_CODE3: B0 0x20] [C_FIELD_CODE4: B0 0x21] [C_FIELD_CODE5: B0 0x22]
M-field code setting	[M_FIELD_CODE1: B0 0x23] [M_FIELD_CODE2: B0 0x24] [M_FIELD_CODE3: B0 0x25] [M_FIELD_CODE4: B0 0x26]
A-field code setting	[A_FIELD_CODE1: B0 0x27] [A_FIELD_CODE2: B0 0x28] [A_FIELD_CODE3: B0 0x29] [A_FIELD_CODE4: B0 0x2A] [A_FIELD_CODE5: B0 0x2B] [A_FIELD_CODE6: B0 0x2C]

The following describes the relation between each comparison code and incoming RX data.

[Format A/B(Wireless M-Bus)]

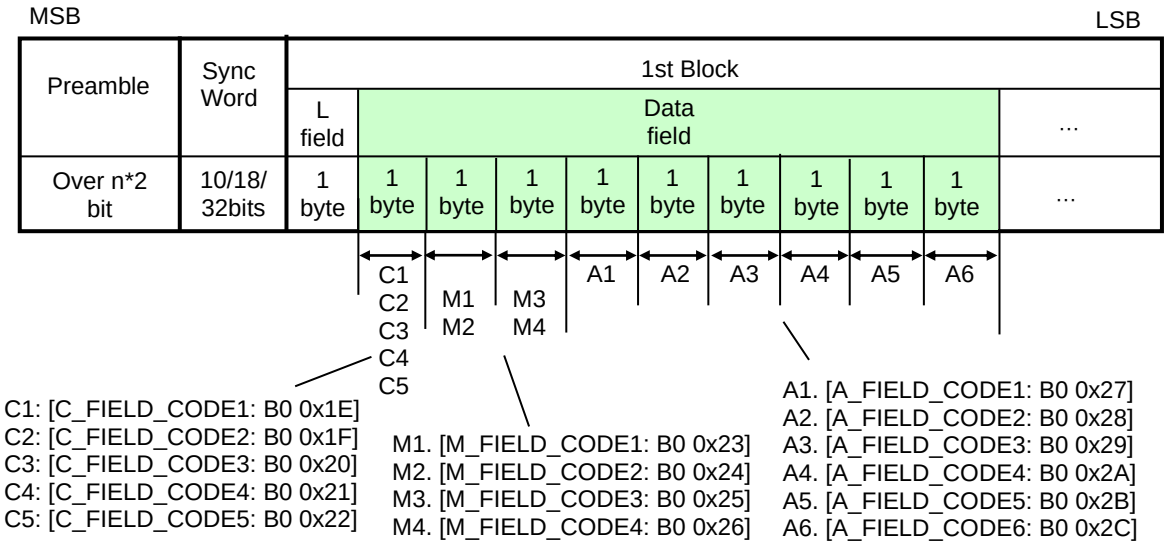
Field check can be controlled by setting disabled/enabled for each comparison code (1 byte). If all specified Field data (C-field/M-field/A-field) are matched, Field checking matching will be notified. However, if C-field data and C_FIELD_CODE5 are matched, even if other Field data (M-field/A-field) are not matched, Field check result will be notified as ”match”.



Check Field	Comparison Code	Conditions for match
C-field	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	If one of the 5 comparison code is matched
M-field 1st byte	M_FIELD_CODE1 or M_FIELD_CODE2	If one of the 2 comparison code is matched.
M-field 2nd byte	M_FIELD_CODE3 or M_FIELD_CODE4	If one of the 2 reference pattern is matched.
A-field	A_FIELD_CODE1/2/3/4/5/6	If comparison codes are matched.

[Format C]

Field check can be controlled by setting disabled/enabled for each comarison code (1 byte). If all specified Field data (specified table below) are matched, Field checking matching will be notified. However, if 1st byte of Data field and C_FIELD_CODE5 are matched, even if other Field data(from 2nd byte to 9th byte) are not matched, Field check result will be notified as "match".



Check Field	Comparison Code	Conditions for match
Data-field 1st byte	C_FIELD_CODE1 or C_FIELD_CODE2 or C_FIELD_CODE3 or C_FIELD_CODE4 or C_FIELD_CODE5	If one of the 5 comparison code is matched
Data-field 2nd byte	M_FIELD_CODE1 or M_FIELD_CODE2	If one of the 2 comparison code is matched.
Data-field 3rd byte	M_FIELD_CODE3 or M_FIELD_CODE4	If one of the 2 comparison code is matched.
Data-field 4th byte	A_FIELD_CODE1	If comparison code is matched.
Data-field 5th byte	A_FIELD_CODE2	If comparison code is matched.
Data-field 6th byte	A_FIELD_CODE3	If comparison code is matched.
Data-field 7th byte	A_FIELD_CODE4	If comparison code is matched.
Data-field 8th byte	A_FIELD_CODE5	If comparison code is matched.
Data-field 9th byte	A_FIELD_CODE6	If comparison code is matched.

●Packet processing as a result of Field checking

By setting CA_RXD_CLR ([C_CHECK_CTRL: B0 0x1B(7)])=0b1, if the result of Field check is unmatch, data packet will be aborted and wait for next packet data.

●Storing number of unmatched packets

Unmatched packets can be counted up to max. 2047 packets and result are stored in [ADDR_CHK_CTR_H: B1 0x62] and[ADDR_CHK_CTR_L: B1 0x63]. This count value can be cleared by STATE_CLR4 ([STATE_CLR: B0 0x16(4)]).

●FIFO control function

ML7344 has on-chip TX_FIFO(64Byte) and RX_FIFO(64Byte). As TX/RX_FIFO do not support multiple packets, packet should be processed one by one. If RX_FIFO keeps RX packet and next RX packet is received, RX_FIFO will be overwritten. It applies to TX_FIFO as well. However TX FIFO access error interrupt (INT[20] group3) will be generated. When receiving, RX data is stored in FIFO (byte by byte) and the host MCU will read RX data through SPI. When transmitting, host MCU write TX data to TX_FIFO through SPI and transmitting through RF.

Writing or reading to FIFO is through SPI with burst access. TX data is written to [WR_TX_FIFO: B0 0x7C] register. RX data is read from [RD_FIFO: B0 0x7F] register. Continuous access increments internal FIFO counter automatically. If FIFO access is suspended during write or read operation, address will be kept until the packet will be process again. Therefore, when resuming FIFO access, next data will be resumed from the suspended address.

FIFO control register are as follows:

Function	Register
TX FIFO Full level setting	[TXFIFO_THRH: B0 0x17]
TX FIFO Empty level setting	[TXFIFO_THRL: B0 0x18]
RX FIFO Full level setting	[RXFIFO_THRH: B0 0x19]
RX FIFO Empty level setting	[RXFIFO_THRL: B0 0x1A]
FIFO readout setting	[FIFO_SET: B0 0x78]
RX FIFO data usage status indication	[RX_FIFO_LAST: B0 0x79]
TX packet Length setting	[TX_PKT_LEN_H/L: B0 0x7A/7B]
RX packet Length setting	[RX_PKT_LEN_H/L: B0 0x7D/7E]
TX FIFO	[WR_TX_FIFO: B0 0x7C]
FIFO read	[RD_FIFO: B0 0x7F]

[TX]

i) TX data L-field value is set to [TX_PKT_LEN_H: B0 0x7A], [TX_PKT_LEN_L: B0 0x7B] register. If Length is 1 byte, [TX_PKT_LEN_L] register will be transmitted.
Length can be set to LENGTH_MODE([PKT_CTRL2: B0 0x05(0)]).

ii) TX data is written to [WR_TX_FIFO:B0 0x7C] register.

NOTE:

1. If TX_FIFO write sequence is aborted during transmission, STATE_CLR0 [STATE_CLR:B0 0x16(0)] (TX FIFO pointer clear) must be issued. Otherwise data pointer is kept in the LSI and the next packet is not processed properly.
   For example, TX FIFO access error interrupt (INT[20] group3) is generated. This interrupt can be generated when the next packet data is writren to the TX_FIFO before transmitting previous packet data or FIFO overrun (FIFO is written when no TX_FIFO space) or underrun (attempt to transmit when TX_FIFO is empty)
2. Depending on the packet format, TX data Length value is different.
   Format A: Length includs data area excluding L-field and CRC data.
   Format B: Length includes data area excluding L-field.
   Format C: Length includes data area excluding L-field.

[RX]

i) L-field (Length) is read from [RX_PKT_LEN_H: B0 0x7D], [RX_PKT_LEN_L: B0 0x7E] registers.

ii) Reading RX data from FIFO. When reading from RX_FIFO, set FIFO_R_SEL([FIFO_SET: B0 0x78(0)])= 0b0. If FIFO_R_SEL=0b1 , TX_FIFO will be selected. Data usage value of RX_FIFO is indicated by [RX_FIFO_LAST: B0 0x79] register.

NOTE:

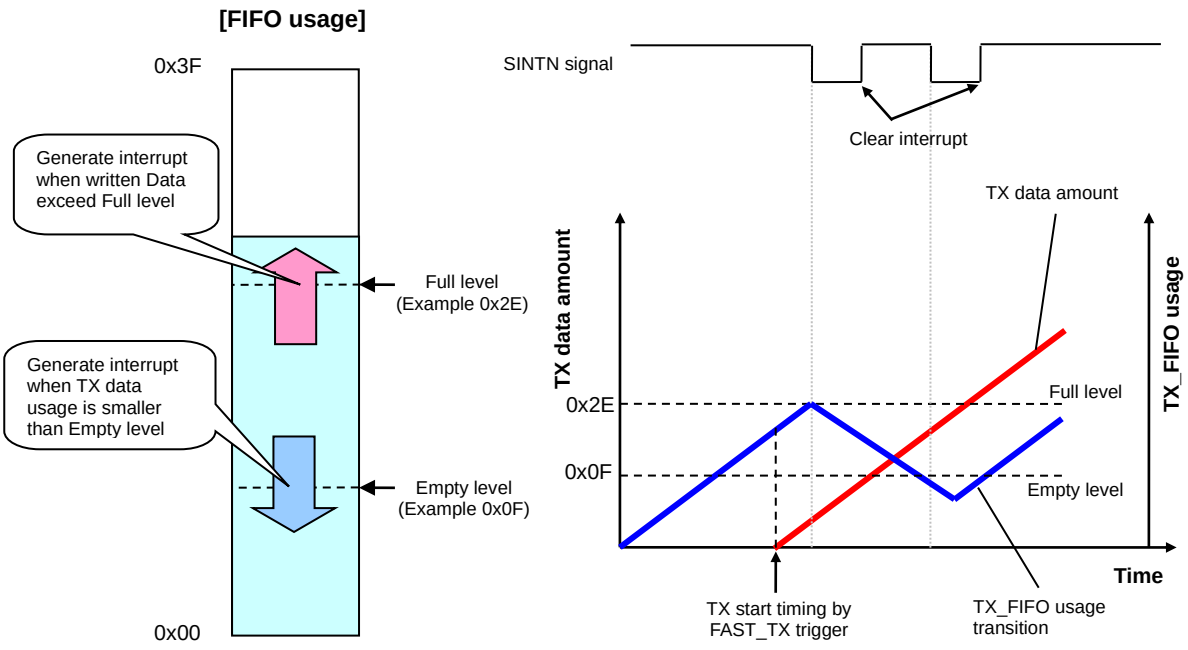
1. If reading FIFO data is terminated before reading all data, STATE_CLR1 [STATE_CLR: B0 0x16(1)] (RX FIFO pointer clear) must be issued. Otherwise If RX_FIFO is not cleared, the pointer controlling FIFO data keeps the same status. Next RX data will not be processed in the FIFO properly.
   For example, when RX_FIFO access error interrupt (INT[12] group2) is generated. This interrupt occurs when RX_FIFO overrun (data received when no space in RX_FIFO) or underrun (reading empty RX_FIFO).
2. If 1 packet data is kept in the RX_FIFO, next RX data will be overwritten.

IF TX/RX pack is larger than FIFO size, FIFO access can be controlled by FIFO-Full trigger or FIFO-Empty trigger.

(1) TX_FIFO usage notification function

This function is to notice TX_FIFO usage to the MCU using interrupt (SINTN). If TX_FIFO usage (un-transmitted data in TX_FIFO) exceed the Full level threshold set by [TXFIFO_THRH: B0 0x17] register, interrupt will generate as FIFO-full interrupt (INT[5] group1). If TX_FIFO usage is smaller than Empty level threshold set by [TXFIFO_THRL: B0 0x18] register, FIFO-Empty interrupt will generate as FIFO-Empty interrout (INT[4] grou1). Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK pin.

For output setting, please refer to [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52] registers for output setting.



[Reference Sequence]:

1. Set Full level threshold and Empy level threshold..Each threshold should set as TXFIFO_THRH[5:0] ([TXFIFO_THRH:B0 0x17(5-0)]) > TXFIFO_THRL[5:0] ([TXFIFO_THRL:B0 0x18(5-0)]). And enabling Full level threshold by TXFIFO_THRH_EN([TXFIFO_THRH:B0 0x17(7)=0b1.
2. Enabling FAST_TX mode by FAST_TX_EN([RF_STATUS_CTRL:B0 0x0A(5)])=0b1 and start writing TX data to the TX_FIFO[WR_TX_FIFO:B0 0x7C] until FIFO-Full interrupt (INT[5] group1) occurs.
3. After FIFO-Full interrupt is generated, Clear the interupt. Then disabling Full level threshold (TXFIFO_THRH_EN= 0b0) and enabling Empty level threshold (TXFIFO_THRL_EN ([TXFIFO_THRL:B0 0x18(7)])=0b1).
4. After FIFO-Empty interrupt (INT[4] group1) is generated, Clear the interupt. Then disabling Empty level threshold (TXFIFO_THRL_EN=0b0) and enabling Full level threshold (TXFIFO_THRH_ EN=0b1). Then resume writing TX data to the TX_FIFO until next FIFO-Full interrupt occurs.
5. Repeat 3.-4. until completion of TX.

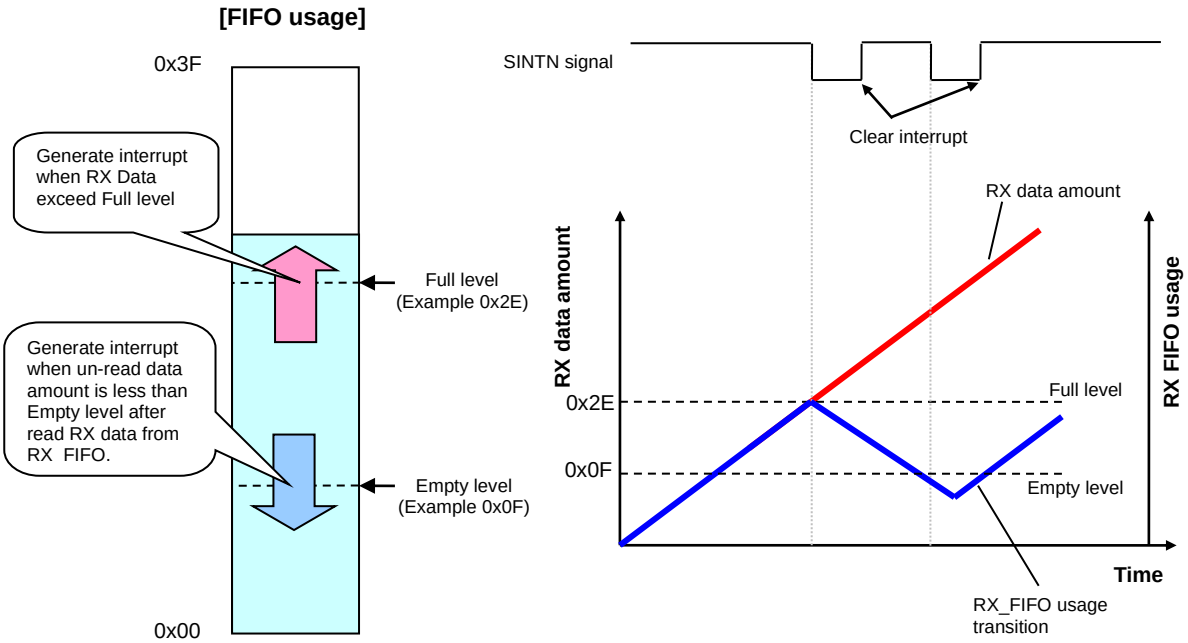
NOTE:

When skip disabling threshold level at sequece 3. or 4., depending on TX data read (PHY block) and TX_FIFO write timing through SPI, in the middle of TX_FIFO writing, unwiilling FIFO-Full interrupt or FIFO-Empty interrupt may occurs.

(2) RX_FIFO usage notification function

This function is to notify remaining RX_FIFO by using interrupt (SINTN) to the MCU. If RX_FIFO usage (un-read data in RX_FIFO) exceed Full level threshold defined by [RXFIFO_THRH: B0 0x19] register, interrupt will generate as FIFO-Full interrupt (INT[5] group1). After MCU read RX data from RX_FIFO, un-read amount become smaller than Empty level threshold defined by [RXFIFO_THRL: B0 0x1A] register, interrupt will generated as FIFO-Empty (INT[4] group1). Interrupt signal (SINTN) can be output from GPIO* or EXT_CLK.

For output setting, please refer to [GPIO0_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51], [EXTCLK_CTRL: B0 0x52] registers.



[Reference Sequence]:

1. Set Full level threshold and Empy level threshold..Each threshold should set as RXFIFO_THRH[5:0] ([RXFIFO_THRH:B0 0x19(5-0)]) > RXFIFO_THRL[5:0] ([RXFIFO_THRL:B0 0x1A(5-0)]). And enabling Full level threshold by RXFIFO_THRH_EN([RXFIFO_THRH:B0 0x19(7)=0b1.
2. After issuing RX_ON, wait FIFO-Full interrupt (INT[5] group1) generation.
3. After FIFO-Full interrupt is generated, Clear the interupt. Then disabling Full level threshold (RXFIFO_THRH_EN= 0b0) and enabling Empty level threshold (RXFIFO_THRL_EN ([RXFIFO_THRL:B0 0x1A(7)])=0b1). And start reading RX data from RX_FIFO [RD_FIFO:B0 0x7F].
4. After FIFO-Empty interrupt (INT[4] group1) is generated, Clear the interupt. Then disabling Empty level threshold (TXFIFO_THRL_EN=0b0) and enabling Full level threshold (TXFIFO_THRH_EN=0b1). Then resume writing TX data to the TX_FIFO until next FIFO-Full interrupt occurs.
5. Repeat 3.-4. until completion of RX data read out.

NOTE:

1. When skip disabling threshold level at sequece 3. or 4., depending on RX data write (PHY block) and RX_FIFO read timing through SPI, in the middle of RX_FIFO reading, unwiilling FIFO-Full interrupt or FIFO-Empty interrupt may occurs.
2. This function is valid during data receiving. FIFO-Empty interrupt does not occur after RX completion.

●DIO function

Using GPIO0-3, EXT_CLK or SDI/SDO pins, TX/RX data can be input/output. Pins can be configured by [GPIO*_CTRL: B0 0x4E/0x4F/0x50/0x51], [EXTCLK_CTRL: B0 0x52] and [SPI/EXT_PA_CTRL: B0 0x53] registers.
Data format for TX/RX are as follows:
TX --- TX data (NRZ or Manchester/3-out-of-6coding) will be input.
RX --- pre-decoded RX data or decoded RX data will be output. (selectable by [DIO_SET: B0 0x0C] register)

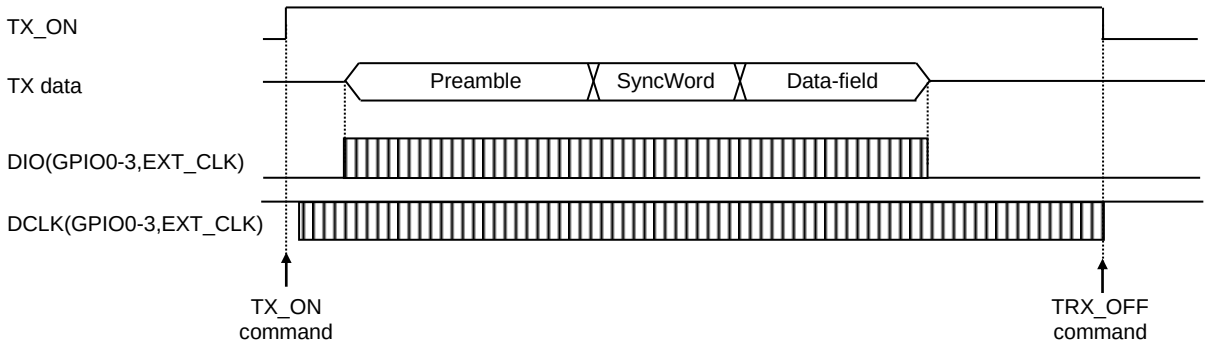
DIO function registers are as follows:

Function	Registers
DIO RX data output start setting	[DIO_SET: B0 0x0C(0)]
DIO RX completion setting	[DIO_SET: B0 0x0C(2)]
TX DIO mode setting	[DIO_SET: B0 0x0C(5-4)]
RX DIO mode setting	[DIO_SET: B0 0x0C(7-6)]

(1)In case of using GPIO*, EXT_CLK pins

If GPIO0-3 or EXT_CLK pins are used as DCLK/DIO, DCLK/DIO should be controlled as follow. (below DIO/DCLK vertical line part indicate output or input period)

[TX]
i) Continuous input mode (from host)
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) =0b01.
After TX_ON(SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)])=0x9), DCLK is output continuously. At falling edge of DCLK, TX data is input from DIO pin. TX data must be encoded data.

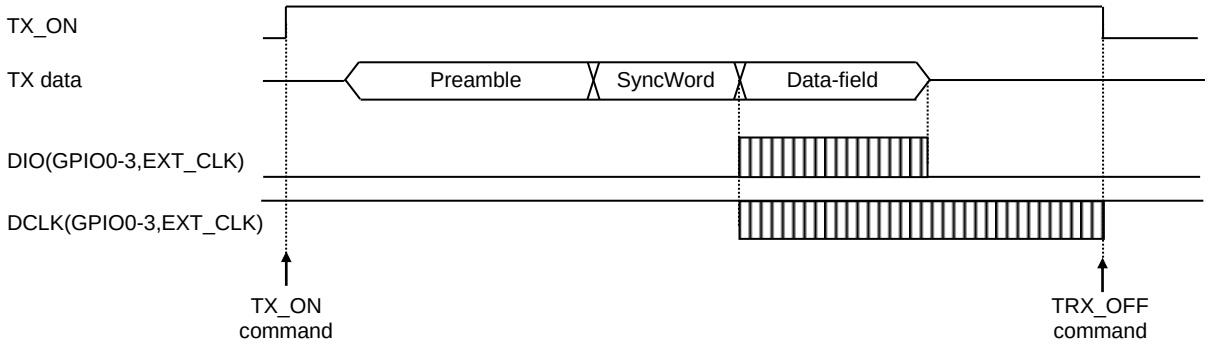


NOTE: For details of timing, please refer to the “TX” in the “Timing Chart”.

ii) Data input mode (from host)

Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) =0b10.

After TX_ON, DCLK is output during data input period after SyncWord. TX data is input at falling edge of DCLK through DIO input. Encoded TX data must be transferred from the host. Preamble and SyncWordis generated automatically according to the registers setting.



NOTE:.

Preamble can be set by PB_PAT([DATA_SET1: B0 0x07(7)] and TXPR_LEN[15:0] ([TXPR_LEN_H/L:B0 0x42/43]).

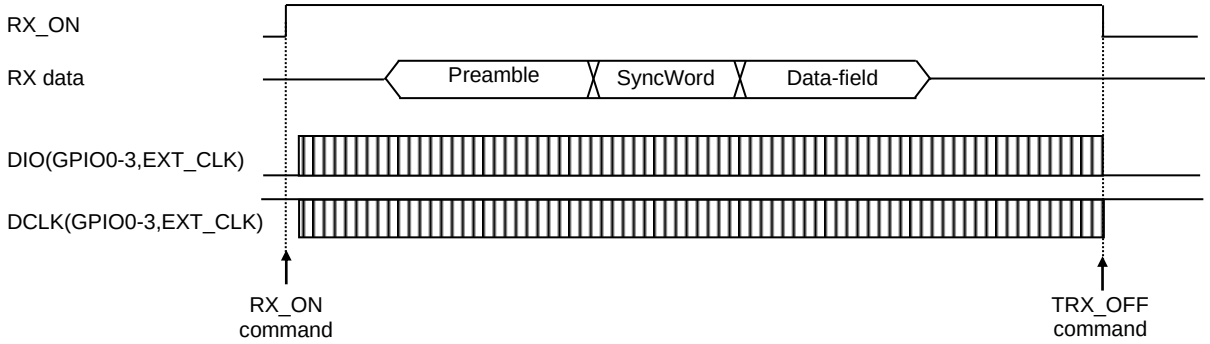
SyncWord can be set by SYNCWORD_SEL([DATA_SET2: B0 0x08(4)), SYNCWORD_LEN[5:0] ([SYNC_WORD_ LEN: B1 0x25(5-0)]), SYNC_WORD_EN* ([SYNC_WORD_EN: B1 0x26(3-0)]), SYNC_WORD1[31:0] ([SYNCWORD1_ SET3/2/1/0: B1 0x27/28/29/2A]) and SYNC_WORD2[31:0] ([SYNCWORD2_SET3/2/1/0: B1 0x2B/2C/2D/2E]).

[RX]

i) Continuous output mode (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) =0b01.

After RX_ON(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x6), DCLK is output continuously. RX data (demodulated data) is output from DIO pin at falling edge of DCLK. RX data is not stored into RX_FIRO.

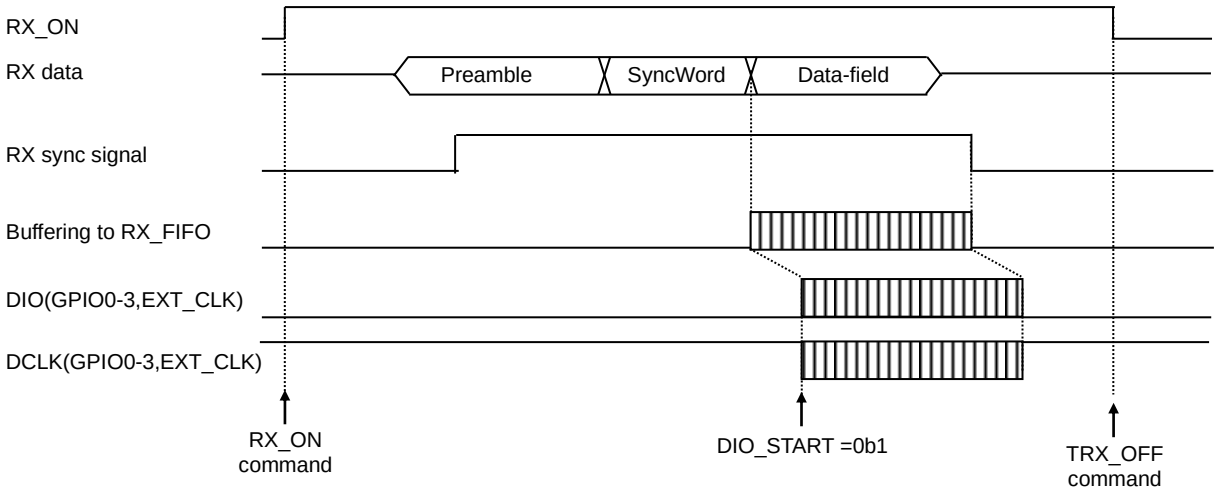


NOTE: For details of timing, please refer to the “RX” in the “Timing Chart”.

ii) Data output mode 1 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) =0b10.

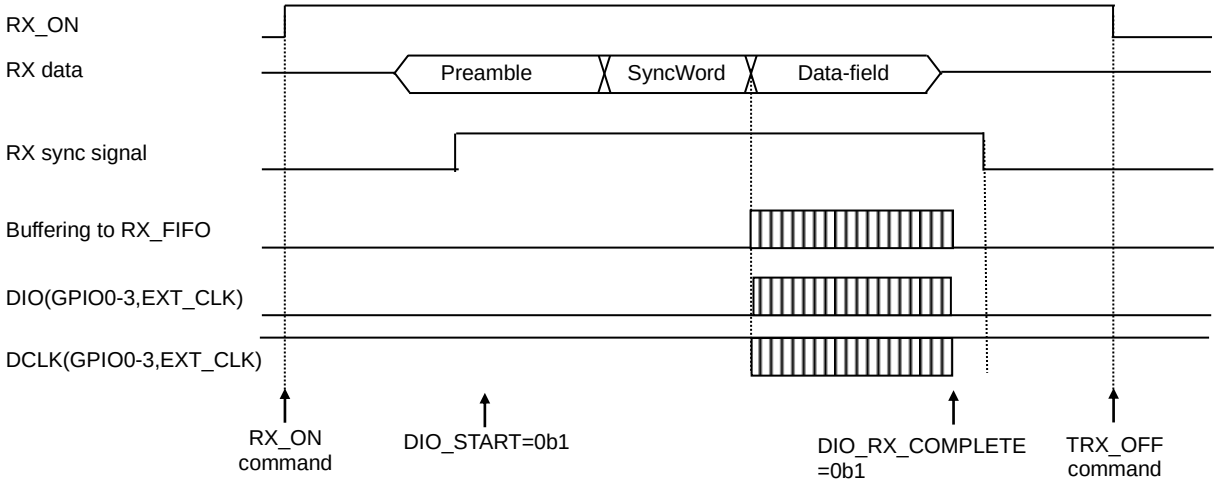
After SyncWord detection, RX data is buffered in RX_FIFO. RX data buffering will continue until RX sync signal (SYNC) becomes ”L”. By setting DIO_START ([DIO_SET: B0 0x0C(0)])=0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK). However, if DIO_START setting is done after 64 byte timing, the top byte will be over written. If all buffered data is output until SYNC becomes ”L”, RX completion interrupt (INT[8] group 2) will be generated. After RX completion, ready to receive next packet.



NOTE:

1. RX data buffering in RX_FIFO is accessed byte by byte. DIO_START should be issued after 1 byte access cycle upon SyncWord detection.
2. This mode does not process L-field. Field checking function is not supported.

If DIO_START is issued before SyncWord detection, data is not buffered in RX_FIFO and RX data after SyncWord detection will be output at falling edge of DCLK . In order to complete RX before SYNC becomes "L", DIO RX completion setting (DIO_RX_COMPLETE([DIO_SET: B0 0x0C(2)]=0b1) is necessary. After DIO_RX_COMPLETE setting, ready to receive the next packet.

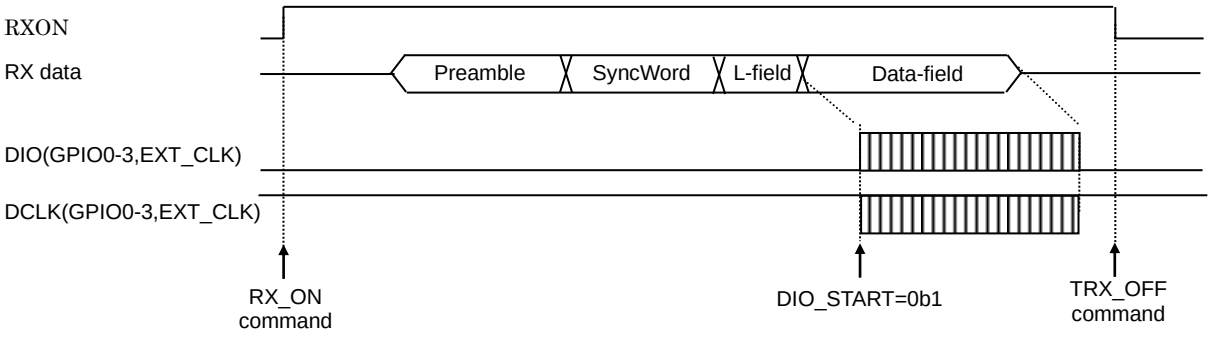


iii) Data output mode 2 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b11.

Only Data-field of RX data is buffered in RX_FIFO. RX data indicated by L-field is stored in RX_FIFO. By DIO_START([DIO_SET: B0 0x0C(0)])=0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK).

However, if DIO_START setting is done after 64 byte timing, the top byte will be overwritten. If all data indicated by L-field is output, RX completion interrupt (INT[8] group2) will be generated. After RX completion, ready to receive next packet. Length information is stored in [RX_PKT_LEN_H/L: B0 0x7D/7E] registers. This mode support fileld check function.



NOTE:

RX data buffering in RX_FIFO is byte by byte access. DIO_START should be issued after elapsed time from SyncWord detection to L-field length + over 1byte access time.

(2)In case of using SDI/SDO pins (sharing with SPI interface)

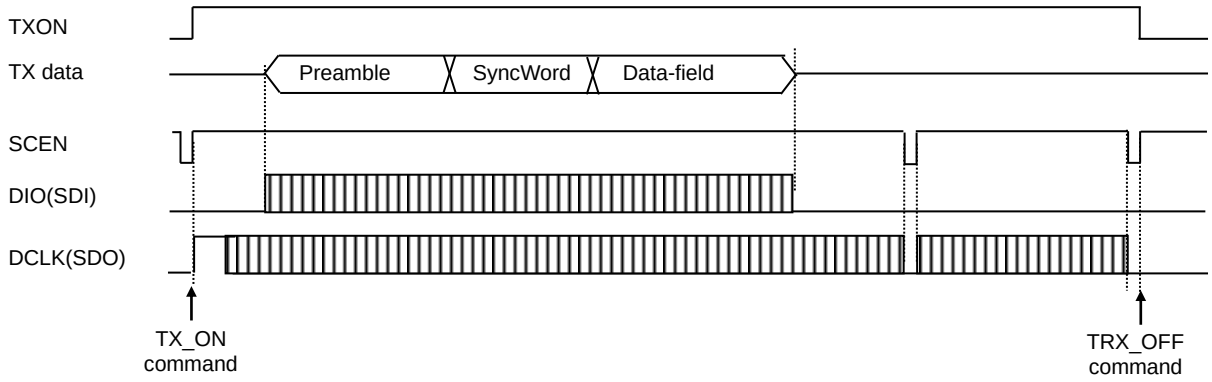
If SDI and SDO pins are used as DCLK/DIO, DCLK/DIO should be controlled as follow. (below DIO/DCLK vertical line part indicate output or input period) Both SDO_CFG and SDI_CFG ([SDI/EXT_PA_CTRL:B0 0x53(5,4)]) should be set 0b1

[TX]

i) Continuous input mode (from host)

Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)]) =0b01.

After TX_ON(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x9), during SCEN pin is "H", DCLK is output from SDO pin., TX data can be input from DIO pin at falling edge of DCLK. TX data must be encoded data. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), DCLK output will stop. During DCLK output, if SCEN pin becomes "L", DCLK output will stop. (SPI access has priority)



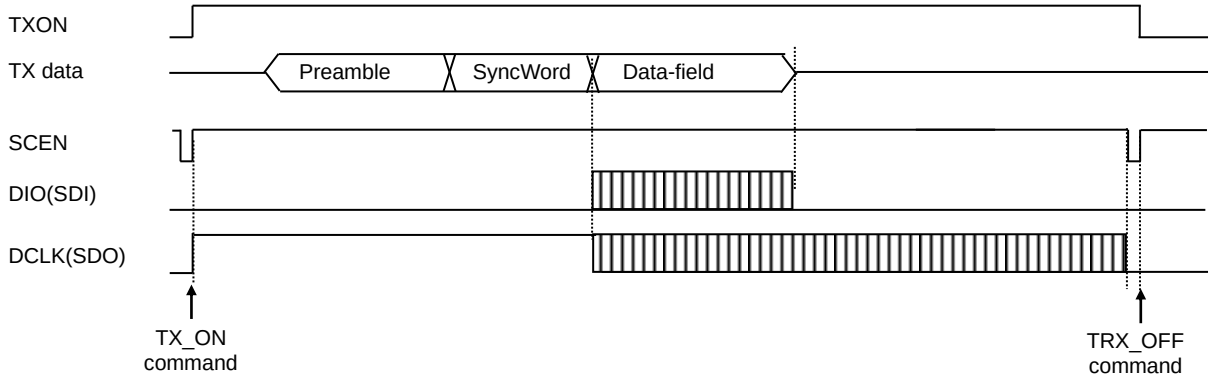
NOTE:

Not to access SPI until TX completion. During packet transmission, if SPI access is attempted by the host, TX data error can be expected.

ii) Data input mode (from host)

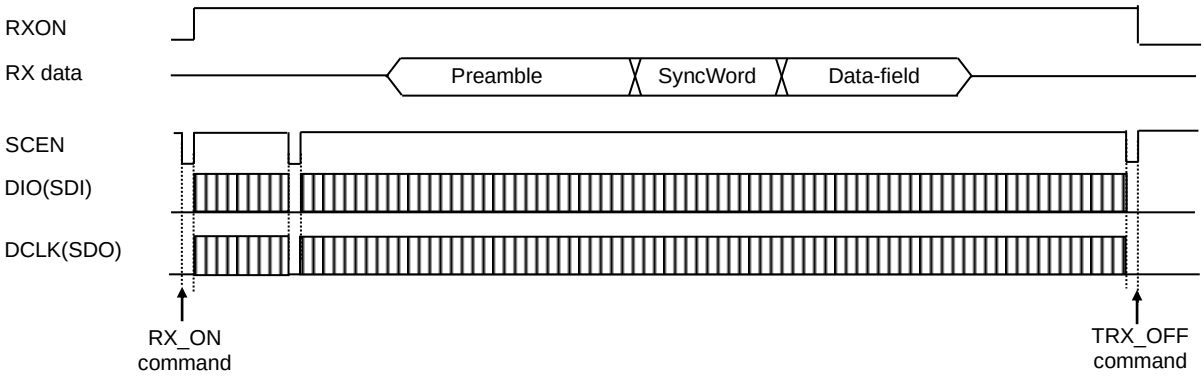
Set TXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(5-4)])=0b10.

After TX_ON, when SCEN is "H", DCLK is output from SDO pin during data input period after SyncWord. At falling edge of DCLK, TX data should be input to SDI from the host. After TRX_OFF is issued (SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), DCLK output will stop. During DCLK output period, if SCEN becomes "L", DCLK output will stop. (SPI access has a priority)



NOTE:
Not to access SPI until TX completion. During packet transmission, if SPI access is attempted by the host, TX data error can be expected.

[RX]
i) Continuous output mode (to host)
Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b01.
After RX_ON (SET_TRX[3:0]([RF_STATUS: B0 0x0B(3-0)])=0x6) issued, during SCEN is "H" period, DCLK is output from SDO pin, RX data is output from SDI pin at falling edge of DCLK. After TRX_OFF issuing(SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)])=0x8), DCLK/DIO output will stop. Even if DCLK/DIO are output, when SCEN becomes "L", DCLK/DIO will stop. (SPI access has a higher priority)



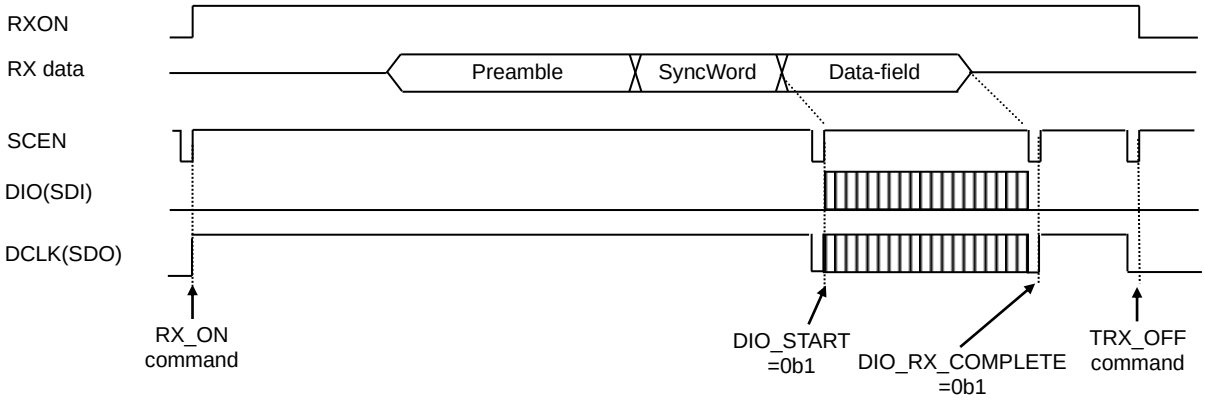
NOTE:
Not to access SPI until RX completion. During packet transmission, if SPI access is attempted by the host, RX data error can be expected.

ii) Data ouput mode 1 or data output mode 2 (to host)

Set RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)])=0b10/11

After RX_ON, RX data upon SyncWord (output mode 1) or RX data upon L-fileld (output mode 2) is buffered in RX_FIFO. During SCEN is "H", by DIO_START([DIO_SET: B0 0x0C(0)])=0b1, top data of buffered data will be output through DIO interface (DIO/DCLK). (RX data is output at falling edge of DCLK). Other output condition is same as the case of using GPIO:/ECT_CLK pins. After TRX_OFF isuing, DCLK/DIO output will stop. Even during DCLK/DIO are output period, if SCEN becomes "L", DCLK/DIO output will stop. (SPI access has a priority)

(In case of data output mode1)



NOTE:

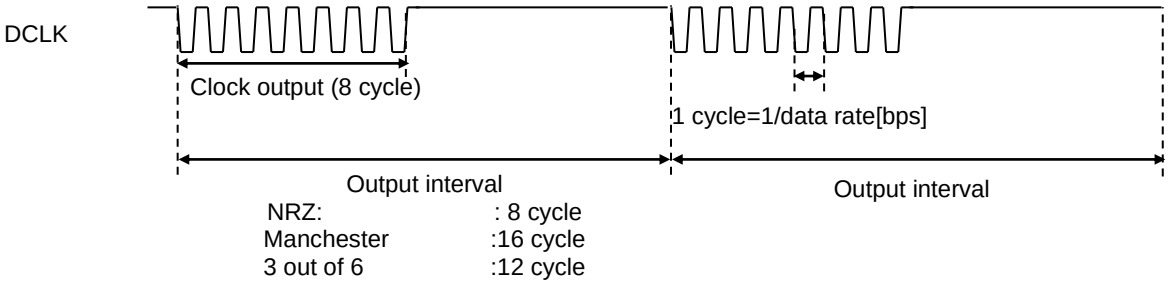
Not to access SPI until RX completion. During packet transmission, if SPI access is attempted by the host, RX data error can be expected.

(3)DCLK output method

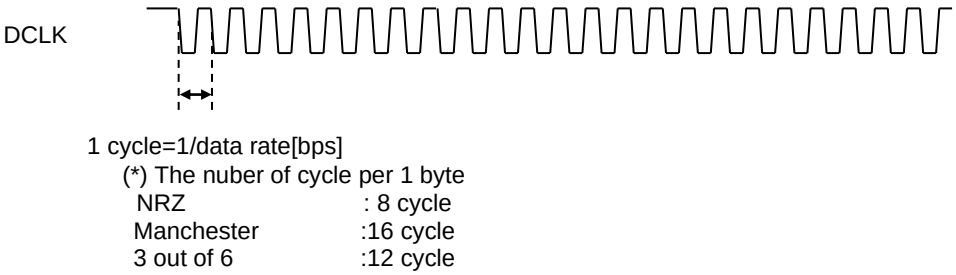
In Data output mode 2, decoded data is output. Therefore, The DCLK output section in a output interval changes with the coding method. DCLK output section is as follows.

In othe modes, undecoded data is input or output. DCLK is output continuously. Then, it is not depend on the coding method.

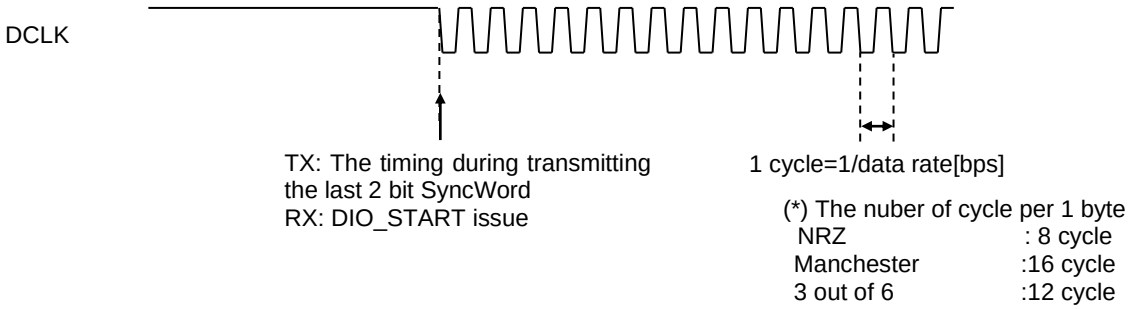
i) Data output mode 2



ii) TX continuous input mode or RX continuous mode



iii) TX Data input mode / RX Data output mode1



●Timer Function

●Wake-up timer

ML7344 has automatic wake-up function using wake-up timer. The following operations are possible by using wake-up timer.

- Upon timer completion, automatically wake-up from SLEEP state. After wake-up operation can be selected as RX_ON state or TX_ON state by WAKEUP_MODE ([SLEEP/WU_SET: B0 0x2D(6)]).
- By setting WUT_1SHOT_MODE ([SLEEP/WU_SET: B0 0x2D(7)]), continuous wake-up operation (interval operation) or one shot operation can be selected
- In interval operation, if RX_ON/TX_ON state is caused by wake-up timer, continuous operation timer is in operation.
- After moving to RX_ON state by wake-up timer, when continuous operation timer completed, move to SLEEP state automatically. However, if SYncWord is detected before timer completion, RX_ON state will be maintained. In this case, ML7344 does not go back to SLEEP state automatically. SLEEP setting (SLEEP_EN ([SLEEP/WU_SET: B0 0x2D(0)])=0b1) is necessary to go back to SLEEP state. However, if RXDONE_ MODE[1:0] ([RF_STATUS_CTRL:B0 0x0A(3-2)])=0b11, after RX completion, move to SLEEP state automatically.
  For ML7344C, when continuous operation timer completed, the condition for continuing reception is selected from Sync Word detection or Field check result by RCV_CONT_SEL([C_CHECK_CTRL: B0 0x1B(5)]).
- After moving to TX_ON state by wake-up timer, when continuous operation timer completed, move to SLEEP state automatically.
- After wake-up by combining with high speed carrier checking mode, CCA is automatically performed, if IDLE is detected, able to move to SLEEP state immediately. For details, please refer to the "(3) high speede carrier detection mode".
- By setting WUT_CLK_SOURCE ([SLEEP/WU_SET:B0 0x2D(2)]), clock source for wake-up timer are selectable from EXT_CLK pin or on-chip RC OSC.

Wake-up interval, wake-up timer interval and continuous operation timer can be calculated in the following formula.

Wake-up interval [s] = Wake-up timer interval [s] + Continuous operation timer [s]

Wake-uptimer interval [s] = Wake-up timer clock cycle *
Division setting ([WUT_CLK_SET: B0 0x2E(3-0)]) *
Wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30])

Continuous operation timer [s] = Wake-up timer clock cycle *
Division setting([WUT_CLK_SET: B0 0x2E(7-4)]) *
Continuous operation timer setting ([WU_DURATION: B0 0x31])

NOTE:

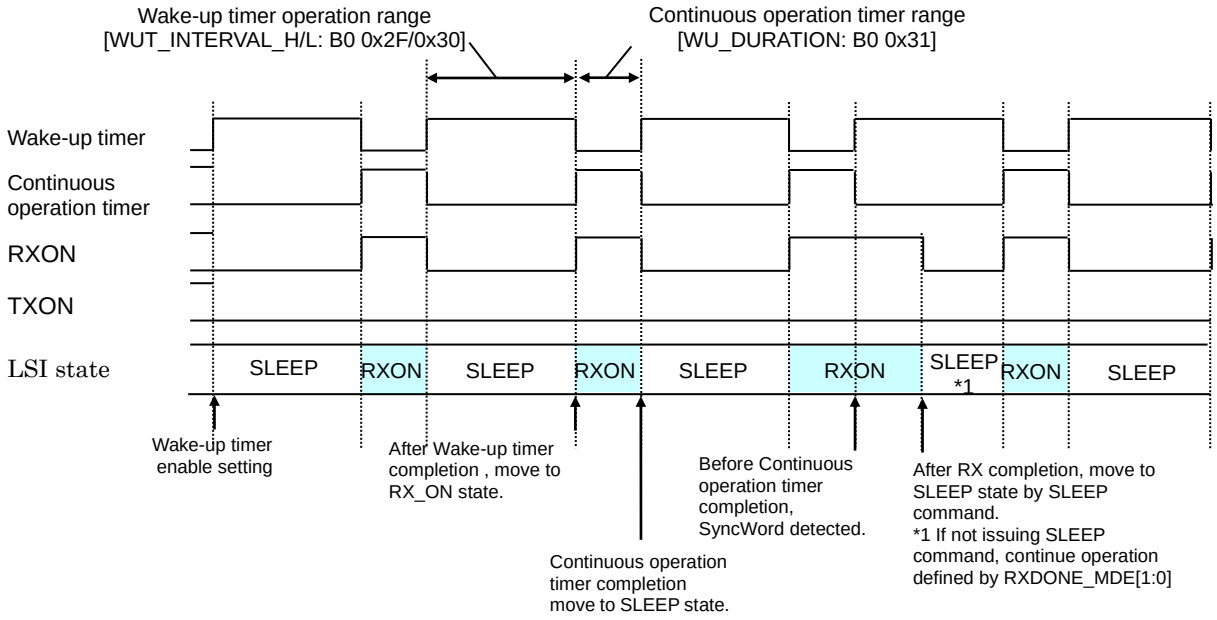
- In case of moving to TX_ON state after wake-up, move to SLEEP state when timer completed even in the middle of transmission. Continuous oeration timer should be set in such manner that timer completing after TX completion.
- WUDT_CLK_SET[3:0] ([WUT_CLK_SET: B0 0x2E(7-4)]) and WUT_CLK_SET[3:0] ([WUT_CLK_ SET: B0 0x2E (3-0)]) can be set independently. In case of using continuous operation timer, please set the same value as WUDT_CLK_SET as WUT_CLK_SET.
- Minimum value for wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) is 0x02. And minimum value for continuous operation timer setting ([WU_DURATION: B0 0x31]) is 0x01.
- Be noted that the SyncWord detection is not issued when in DIO mode with RXDIO_CTRL([DIO_SET: B0 0x0C(7-6)])=0b01. Therefore, when continuous operation timer completed, forcibly move to SLEEP state.

(1) Interval operation

[RX]

After wake-up, RX_ON state. If continuous operation timer completed before SyncWord detection, automatically move to SLEEP state. If SyncWord detected, continue RX_ON. After RX completion, conitune operation defined by RXDONE_MODE[1:0] ([RF_STATUS_CTRL:B0 0x0A(3-2)]).

[SLEEPWU_SET: B0 0x2D(6-4)]=0b011

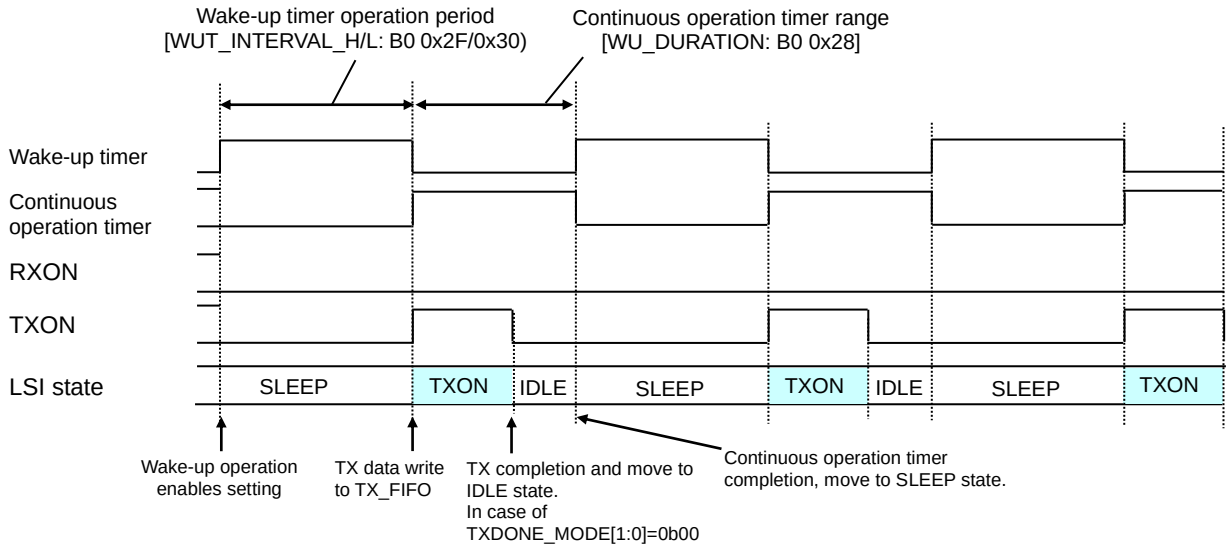


[TX]

After wake-up, TX_ON state. After TX completion, continue operation defined by TXDONE_MODE[1:0] ([RF_STATUS_CTRL: B0 0x08(1-0)]) .

If continuous operation timer completed, automatically return to SLEEP state. So continuous operation timer has to be set so that timer completion occur after TX completion.

[SLEEP/WU_SET: B0 0x2D(6-4)]=0b111



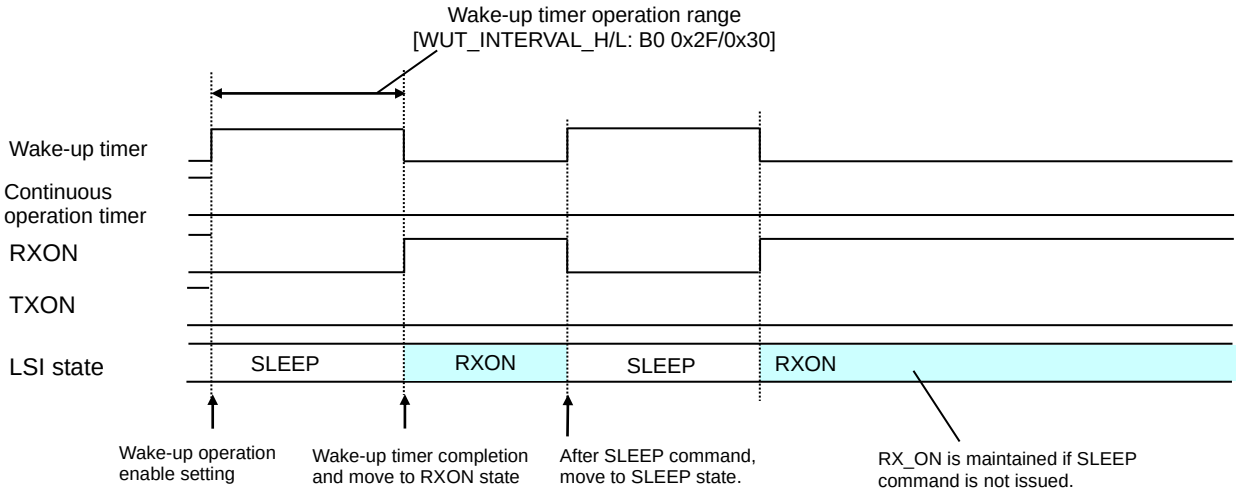
(2) 1 shot operation

[RX]

After wake-up timer completion, move to RX_ON state. And continue RX_ON state. Move to SLEEP state by SLEEP command. If wake-up timer interval setting ([WUT_INTERVAL_H/L:B0 0x2F/0x30]) is maintained, after re-issuing SLEEP command, 1 shot operation will be activated again.

If RX completed during RX_ON, continue operation defined by RXDONE_ MODE[1:0] ([RF_STATUS_ CTRL: B0 0x0A(3-2)]) . Same manner in TX_ON state.

[SLEEPWU_SET: B0 0x2D(7-4)]=0b1011

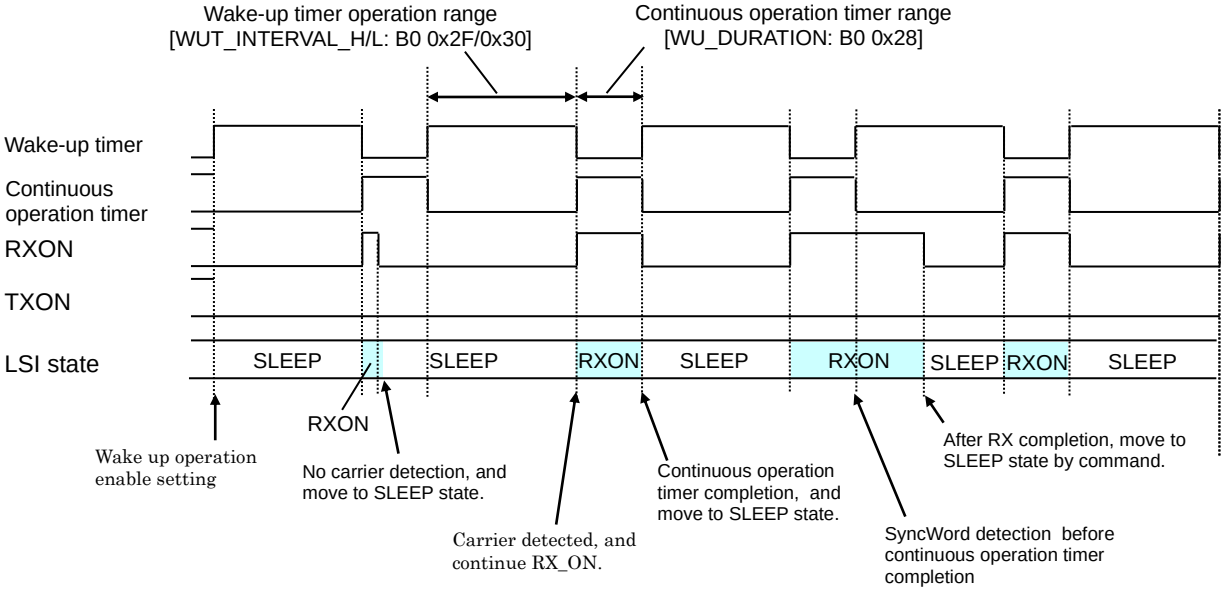


(3) Combination with high speed carrier detection

[Intetval operation]

After wake-up timer completion, move to RX_ON state. Then perform CCA. If no carrier detected, automatically move to SLEEP state. If carrier detected, maintaining RX_ON state and perform SuncWord detection. If continuous operation timer completed before SyncWord detection, automatically move to SLEEP state. And If SyncWord detected, continue RX_ON state.

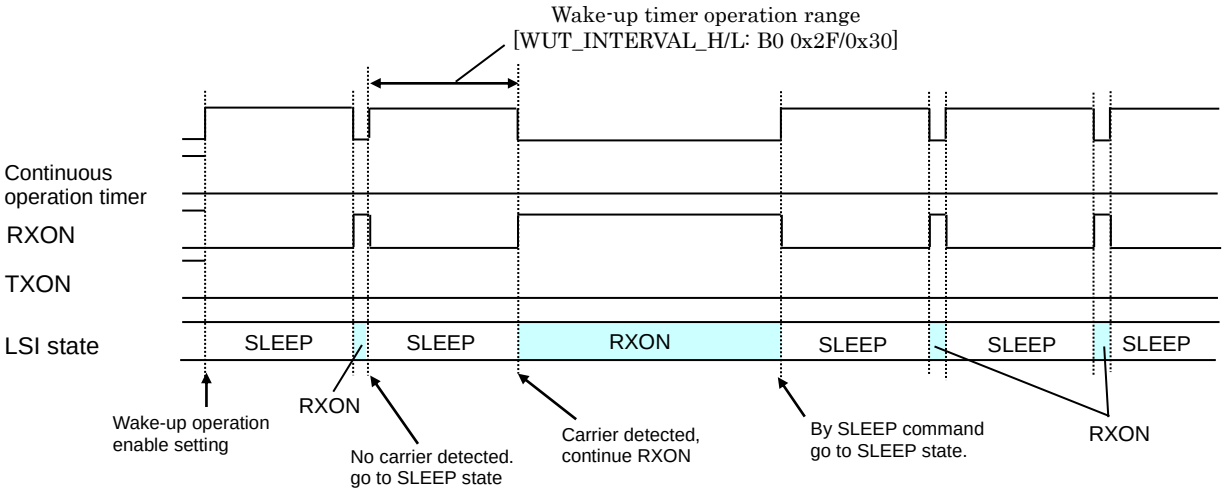
[SLEEP/WU_SET: B0 0x2D(7-4)]=0b0011
FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)])=0b1



[1 shot operation]

After wake-up timer completion, move to RX_ON state. And perform CCA to check carrier. If no carrier detected, go back to SLEEP state automatically. After wake-up timer completion, wake-up to check the carrier again. If carrier is detected, continue RX state. Able to go back to SLEEP by setting SLEEP parameters.

[SLEEPWU_SET: B0 0x2D(7-4)]=0b1011
FAST_DET_MODE_EN([CCA_CTRL: B0 0x39(3)])=0b1



●General purpose timer

ML7344 has general purpose timer. 2 channel of timer are able to function independently. Clock sources, timer setting can be programmed independently. When timer is completed, General purpose timer 1 interrupt (INT[22] group3) or General purpose timer 2 interrupt (INT[23] group3)will be generated.

General timer interval can be programmed as the following formula.

General purpose timer interval[s] = general purpose timer clock cycle *
Division setting ([GT_CLK_SET: B0 0x33]) *
General purpose timer interval setting
([GT1_TIMER: B0 0x34] or [GT2_TIMER: B0 0x35])

By setting GT2/1_CLK_SOURCE ([GT_SET: B0 0x32(5,1)]), clock sources for general purpose timer can be selectable from wake-up timer clock or 2MHz.

●Frequency Setting Function

●Channel frequency setting

Maximum 256 channels can be selected (CH#0 -CH#255) by the following resisters.

Frequency		Register
CH#0 frequency	TX	[TXFREQ_I: B1 0x1B], [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E]
	RX	[RXFREQ_I: B1 0x1F], [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22]
Channel space	-	[CH_SPACE_H: B1 0x23] and [CH_SPACE_L: B1 0x24]
Channel setting	-	[CH_SET: B0 0x09]

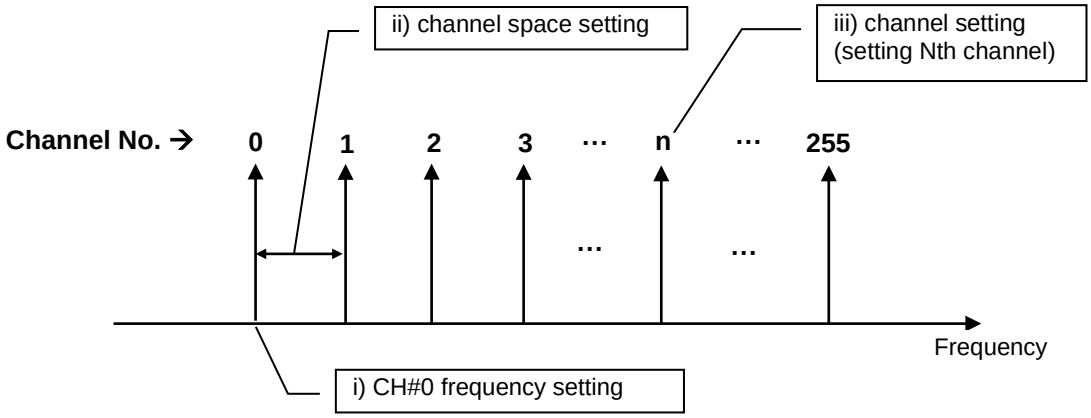
(1) Channel frequency setting overview

[Channel frequency setting]

Using above registers, channel frequency is defined as following formula.

Channel frequency = i) CH#0 frequency + ii) channel space * iii) channel setting

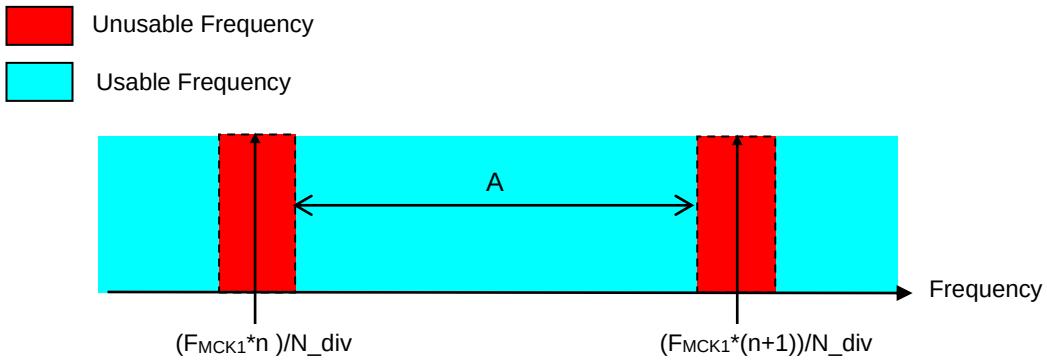
[Channel frequency allocation image]



NOTE:
The channel frequency to be selected must meet the following conditions. If the following conditions cannot be met, please change channel #0 frequency or use other channels. If this formula cannot be met, expected frequency is not functional or PLL may not be locked.

(F_{MCK1}*n + 1MHz) / N_div ≤ channel frequency ≤ (F_{MCK1}*(n+1) – 1MHz) / N_div

F_{MCK1}: Master clock frequency
N_div = 1 (PLL_MODE ([PLL_DIV_SET: B1 0x1A (4)])=0b0)
2 (PLL_MODE ([PLL_DIV_SET: B1 0x1A (4)])=0b1)
n = integer



[Calculation example above "A" range]
Condition: Master clock 26MHz, N_div=1(PLL_MODE=0b0), n=16

(26*16+1)MHz ≤ channel frequency to be used ≤ (26*(16+1)-1)
→ 417 MHz ≤ channel frequency to be used ≤ 441MHz

NOTE:
"CH#0 frequency (Hz)" and "channle space (Hz)" may have error (Hz). Then the "channel frequency error (Hz)" is defined as following formula.

Channel frequency error (Hz) =
CH#0 frequency error (Hz) + channel space error (Hz)* channel setting

When changing "channel frequency" by setting "channel setting" without "CH#0 frequency" change, the "channel frequency error" will become larger than by setting both "CH#0 frequency" and "channel setting". If the "channle frequency error" is larger than expection, please consider to change "CH#0 frequency".

(2) Channel #0 frequency setting

TX frequency can be set by [TXFREQ_I: B1 0x1B], [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D] and [TXFREQ_FL: B1 0x1E]. RX frequency can be set by [RXFREQ_I: B1 0x1F], [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21] and [RXFREQ_FL: B1 0x22]. When enabling PLL 1/2 division mode by setting PLL_MODE([PLL_DIV_SET:B1 0x1A(4)])=0b1, calcurated with fref =F_{MCK1}/2 in the following formula.

Channel #0 frequency setting can be caluculated using the following formula.

$$I = \frac{f_{rf}}{f_{ref}} \text{ (Integer part)}$$

$$F = \left\{ \frac{f_{rf}}{f_{ref}} - I \right\} \cdot 2^{20} \text{ (Integer part)}$$

Here

f_{rf} :Channel #0 frequency

f_{ref} :PLL reference frequency (=master clock frequency: F_{MCK1})

I :Integer part of frequency setting

F :Fractional part of frequency setting

I (Hex) is set to [TXFREQ_I: B1 0x1B], [RXFREQ_I: B1 0x1F] registers.

F (Hex.) is set to the following registers.

For TX, from MSB, set in order of [TXFREQ_FH: B1 0x1C], [TXFREQ_FM: B1 0x1D], [TXFREQ_FL: B1 0x1E] registers.

For RX, from MSB, set in order of [RXFREQ_FH: B1 0x20], [RXFREQ_FM: B1 0x21], [RXFREQ_FL: B1 0x22] registers.

Frequency error (f_{err}) is calculated as follows :

$$f_{err} = \left\{ I + \frac{F}{2^{20}} \right\} \cdot f_{ref} - f_{rf}$$

[Example]

When set TX channel #0 frequency to 426MHz (master clock 26MHz), the calculations are as follows.

$$I = \frac{426MHz}{26MHz} \text{ (Integer part) =16(0x10)}$$

$$F = \left\{ \frac{426MHz}{26MHz} - I \right\} \cdot 2^{20} \text{ (Integer part)=403298(0x062762)}$$

[TXFREQ_I: B1 0x1B] = 0x10
[TXFREQ _FH: B1 0x1C] = 0x06
[TXFREQ _FM: B1 0x1D] = 0x27
[TXFREQ _FL: B1 0x1E] = 0x62

Frequency error f_{err} is as follows:

$$f_{err} = \left\{ 16 + \frac{403298}{2^{20}} \right\} \cdot 26MHz - 426MHz = -11.45Hz$$

(3) Channel space setting

Channel space can be set by [CH_SPACE_H: B1 0x23], [CH_SPACE_L: B1 0x24] registers. Hexadecimal values calculated in the following formula should be set to [CH_SPACE_H: B1 0x23], [CH_SPACE_L: B1 0x24] registers. (MSB->LSB order) When enabling PLL 1/2 division mode by setting PLL_MODE ([PLL_DIV_SET:B1 0x1A(4)])=0b1, calcurated with fref =F_{MCK1}/2 in the following formula.
Channel space is from the center frequency of given channel to adjacent channel center frequency.

Channel space setting value can be calculated using the following formula:

$$CH\_SPACE = \left\{ \frac{f_{sp}}{f_{ref}} \right\} \cdot 2^{20} \quad \text{(Integer part)}$$

Here

CH_SPACE : Channel space setting

f_{sp} : Channel space [Hz]

f_{ref} : PLL reference frequency (=master clock frequency : F_{MCK1})

[Example]
When set channle space to 25kHz (master clock 26MHz), the calculation is as follows.

$$CH\_SPACE = \left\{ \frac{0.025MHz}{26MHz} \right\} \cdot 2^{20} \quad \text{(Integer part)} = 1008 \text{ (0x03F0)}$$

[CH_SPACE_H: B1 0x23] = 0x03
[CH_SPACE_L: B1 0x24] = 0xF0

●IF frequency setting

IF frequency is 200kHz. IF frequency corresponds to each oepration frquency must be selected as below.

	Operating Frequency		
	169MHz (ML7344E)	315 to 450MHz (ML7344J)	470 t0 510MHz (ML7344C)
PLL division setting [PLL_DIV_SET:B1 0x1A]	0x10	0x00	
IF frequency setting [IF_FREQ_H/L:B0 0x54-55]	0x1F81	0x0FC0	

IF frequency setting value can be calculated using the following formula:

$$IF\_FREQ = \left\{ \frac{(f_{IF} / 2)}{f_{ref}} \right\} \cdot 2^{20} \text{ (Integer part)}$$

Here

IF_FREQ : IF frequency setting

f_{IF} : IF frequency [Hz]

f_{ref} : PLL reference frequency (=master clock frequency: F_{MCK1})

[Example] ML7344C/J

IF_FREQ= {(0. 2MHz / 2) / 26MHz} * 2^{20} (Integer part) = 4032 (0x0FC0)

[IF_FREQ_H: B0 0x54] = 0x0F
[IF_FREQ_L: B0 0x55] = 0xC0

[Example] ML7344E

IF_FREQ= {(0. 2MHz / 2) / (26/2)MHz} * 2^{20} (Integer part) = 8065 (0x1F81)

[IF_FREQ_H: B0 0x54] = 0x1F
[IF_FREQ_L: B0 0x55] = 0x81

●Modulation setting

ML7344 supports GFSK modulation and FSK modulation.

(1) GFSK modulation setting

By setting GFSK_EN([DATA_SET1: B0 0x07(4)])=0b1, GFSK mode can be selected. In GFSK modulation, frequency deviation can be set by [GFSK_DEV_H: B1 0x30] and [GFSK_DEV_L: B1 0x31] registers and Gaussian filter can be set by [FSK_DEV0_H/GFIL0: B1 0x32] to [FSK_DEV3_H/GFIL6: B1 0x38] registers.
When enabling PLL 1/2 division mode by setting PLL_MODE ([PLL_DIV_SET:B1 0x1A(4)])=0b1, calcurated with fref =F_{MCK1}/2 in the following formula.

i) GFSK frequency deviation setting

F_DEV value can be calculated as the following formula:

$$F\_DEV = \left\{ \frac{f_{dev}}{f_{ref}} \right\} \cdot 2^{20} \text{ (Integer part)}$$

Here

F_DEV : Frequency deviation setting

f_{dev} : Frequency deviation [Hz]

f_{ref} : PLL reference frequency (= master clock frequency: F_{MCK1})

[Example]

When set frequency deviation to 50kH (master clock 26MHz), the calculation is as follows.

F_DEV = {0.05MHz ÷ 26MHz} $\times 2^{20}$ (Integer value) = 2016 (0x07E0)

[GFSK_DEV_H: B1 0x30] = 0x07
[GFSK_DEV_L: B1 0x31] = 0xE0

ii) Gaussian filter setting

BT value of Gaussian filter and setting value to related registers are shown in the below table.

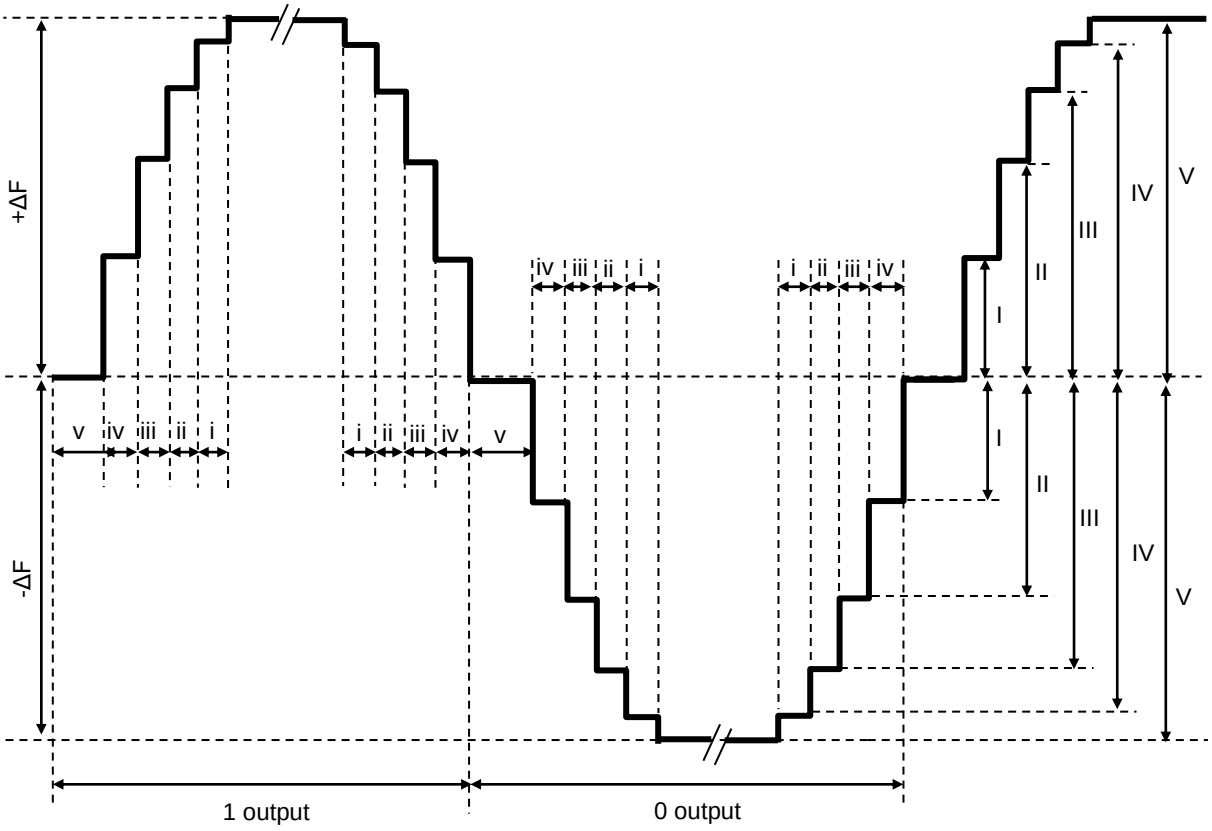
Register	BT value	
	0.5	1.0
[FSK_DEV0_H/GFIL0: B1 0x32]	0x49	0x00
[FSK_DEV0_L/GFIL1: B1 0x33]	0xA7	0x10
[FSK_DEV1_H/GFIL2: B1 0x34]	0x0F	0x04
[FSK_DEV1_L/GFIL3: B1 0x35]	0x14	0x0D
[FSK_DEV2_H/GFIL4: B1 0x36]	0x19	0x1E
[FSK_DEV2_L/GFIL5: B1 0x37]	0x1D	0x32
[FSK_DEV3_H/GFIL6: B1 0x38]	0x1E	0x3C

NOTE:

GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

(2) FSK modulation setting

By setting GFSK_EN([DATA_SET1: B0 0x07(4)])=0b0, FSK mode can be selected. Fine frequency deviation can be set by [FSK_DEV0_H/GFIL0: B1 0x32] to [FSK_DEV4_L: B1 0x3B] registers. By adjusting [FSK_TIM_ADJ4-0: B1 0x3C-40] registers, FSK timing can be fine tuned.



TX_FSK_POL ([DATA_SET1:B0 0x07(6)]) = 0b0 setting

Frequency deviation setting				Timing setting			
symbol	**Register name**	**address**	**function**	**symbol**	**Register name**	**address**	**function**
I	FSK_FDEV0_H/GFIL0 FSK_FDEV0_L/GFIL1	B1 0x32/33	Frequency deviation Resolution: Approx.25 Hz	i	FSK_TIM_ADJ4	B1 0x3C	Modulation timing 4.3MHz/13 MHz counter value (*1)
II	FSK_FDEV1_H/GFIL2 FSK_FDEV1_L/GFIL3	B1 0x34/35		ii	FSK_TIM_ADJ3	B1 0x3D	
III	FSK_FDEV2_H/GFIL4 FSK_FDEV2_L/GFIL5	B1 0x36/37		iii	FSK_TIM_ADJ2	B1 0x3E	
IV	FSK_FDEV3_H/GFIL6 FSK_FDEV3_L	B1 0x38/39		iv	FSK_TIM_ADJ1	B1 0x3F	
V	FSK_FDEV4_H FSK_FDEV4_L	B1 0x3A/3B		v	FSK_TIM_ADJ0	B1 0x40	

(*1) Modulation timing resolution can be changed by FSK_CLK_SET ([FSK_CTRL: B1 0x2F(0)]).

NOTE:
GFSK filter coefficient setting register and FSK frequency deviation setting register are common. In GFSK mode, filter coefficient applies to this register. In FSK mode, frequency deviation applies to this register.

●RX Related Function

●AFC function

ML7344 supports AFC function. Master clock Frequency accuracy (max. ±10ppm) between transmitter and receiver can be compensated by this function. Using this function, stable RX sensitivity and interference blocking performance can be achieved. This function can be enabled by setting AFC_EN([AFC/GC_CTRL: B1 0x15(7)])=0b1. AFC range is defined by AFC_LIM_OFF ([DEMOD_SET0:B1 0x56(2)]. When setting 0b0 (limit ON), AFC range is ±9ppm. When setting 0b1 (limit OFF), ±10ppm AFC range is avilable.

●Energy detection value (ED value) acquisition function

ML7344 supports calculating Energy detection value (ED value) based on Received signal strength indicator (RSSI). ED value acquisition can be enabled by setting ED_CALC_EN ([ED_CTRL: B0 0x41(7)])=0b1 and as soon as transition to RX_ON state, automatically start acquiring ED value. During RX_ON state, ED value constantly updated.

ED value is not RSSI value at given timing, but average values. Number of average times can be specified by ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)]). After acquiring specified average ED value, ED_DONE ([ED_CTRL: B0 0x41(4)]) becomes ”0b1” and ED_VALUE[7:0] ([ED_RSLT: B0 0x3A]) is updated.

ED_DONE bit will be cleared if one of the following conditions are met.

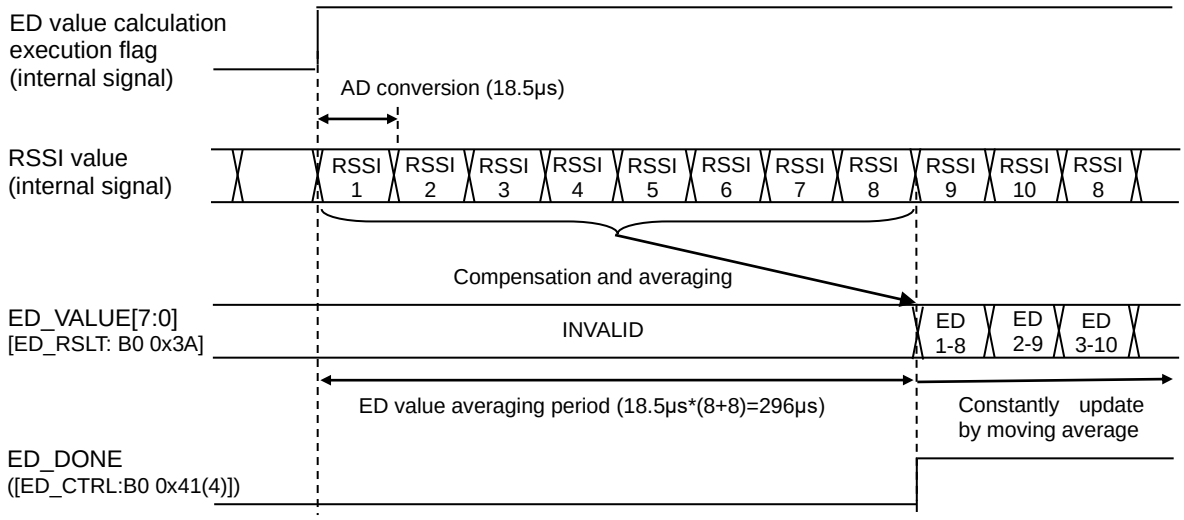
1. Gain is switched..
2. Once stopping ED value acquisition and then resume it

Timing from ED value starting point to ED value acquisition is calculated as below formula.

ED value average time = AD conversion time (18.5µs/14.7µs) * (Number of average times + 8(Deley)).

NOTE: AD conversion time can be slected by ADC_CLK_SEL([ADC_CLK_SET: B1 0x08(4)]).
Reset value is 1.73MHz and AD conversion time is 18.5µs.
Digital filter delay is “AD conversion time * 8”.

The timing example is as follows:
Set ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]) =0b1. (1.73 MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011. (8 times averaging)



●CCA (Clear Channel Assessment) function

ML7344 supports CCA function. CCA function is to make a judment wheher the specified frequency channel is in-use or available. Normal mode, continuous mode and IDLE detection mode are supported as following table.

[CCA mode setting]

	[CCA_CTRL: B0 0x39]		
	Bit4 (CCA_EN)	**Bit5 (CCA_CPU_EN)**	**Bit6 (CCA_IDLE_EN)**
Normal mode	0b1	0b0	0b0
Continuous mode	0b1	0b1	0b0
IDLE detection mode	0b1	0b0	0b1

(1) Normal mode

Normal mode determines IDLE or BUSY. CCA (Normal mode) will be executed when RX_ON is issued whille CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN (CCA_CTRL: B0 0x39(5)])=0b0 and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b0 are set.

CCA judgement is determined by average ED value in [ED_RSLT: B0 0x3A] register and CCA threshold value defined by [CCA_LVL: B0 0x37] register. IF average ED value exceeds the CCA threshold value, it is considered as “BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) =0b01 is set

If average ED value is smaller than CCA threshold value and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3B], [IDLE_WAIT_H: B0 0x3C] registers, it is considered as “IDLE”. And CCA_RSLT[1:0] =0b00 is set. For details operation of CCA_IDLE_WAIT[9:0], please refer to ”IDLE detection for long time period”

If “BUSY” or “IDLE” state is detected, CCA completion interrupt (INT[18] group3) is generated, CCA_EN bit is cleared to 0b0 automatically.

Upon clearing CCA completion interrupt, CCA_RSLT[1:0] are reset to 0b00. Therefore CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

If an ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36] register, and a given ED value is included in the averaging target of ED value calculation, IDLE judgement is not performed. In this case if average ED value exceed CCA threshold value, it is considered as “BUSY” and CCA operation is terminated.

If average ED value is smaller than CCA threshold value, IDLE judgement is not determined. And CCA_RSLT[1:0] indicates 0b11. CCA operation continues until “BUSY” is determined or the gievn ED value is out of averaging target and “IDLE” is determined. For details operation of ED value exeeceding [CCA_IGNORE_LVL: B0 0x36] register, please refer to ”IDLE determination exclusion under strong signal input”.

Time from CCA command issue to CCA completion is in the formula below.

[IDLE detection]

CCA execution time = (ED value average times + Dgital filter delay + IDLE_WAIT setting) * AD conversion time

[BUSY detection]

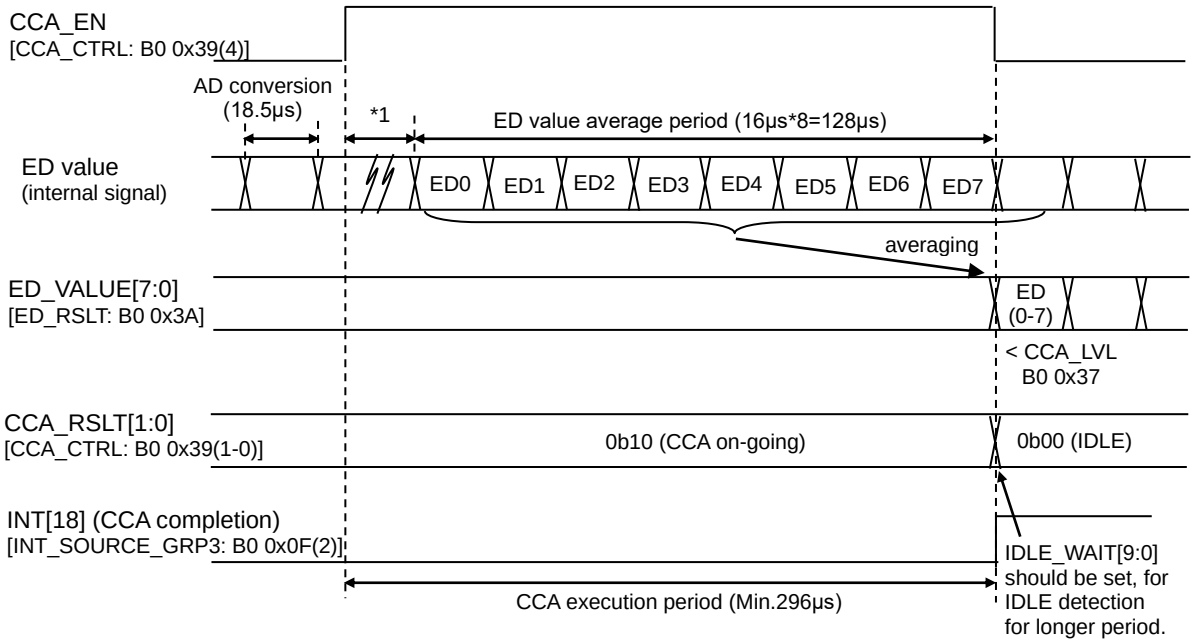
CCA execution time = (ED value average times + Digtal filter delay)* AD conversion time

NOTE:

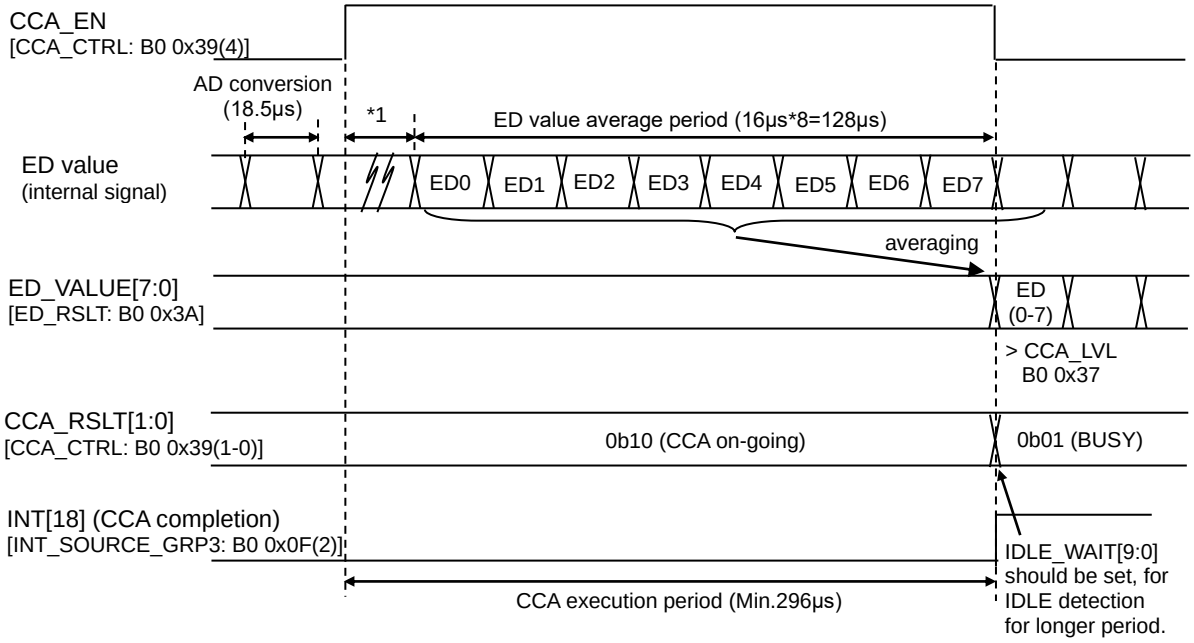
1. Above formula does not consider IDLE judgement exclusion based on [CCA_IGNORE_LVL: B0 0x36] register. For details, please refer to ”IDLE detection exclusion under strong signal input”.
2. AD conversion time can be slected by ADC_CLK_SEL([ADC_CLK_SET: B1 0x08(4)]). ADC_CLK_SEL=0b0:14.7µs , 0b1:18.5µs (default)
3. Digital filter delay is “AD conversion time * 8”.

The following is timing chart for normal mode.
Set ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]) =0b1. (1.73 MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011. (8 times average)
Set IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)])=0b00 0000 0000 (IDLE detection 0µs)

[IDLE detection case]



[BUSY detection case]



NOTE:
*1 Digital filter delay is “AD conversion time * 8”. AD conversion time can be slected by ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]). Reset value is 1.73MHz and AD conversion time is 18.5μs.

(2) Continuous mode

Continuous mode continues CCA untill terminated by the host MCU. CCA continuous mode will be executed when RX_ON is issued while CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b1 and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b0 are set.

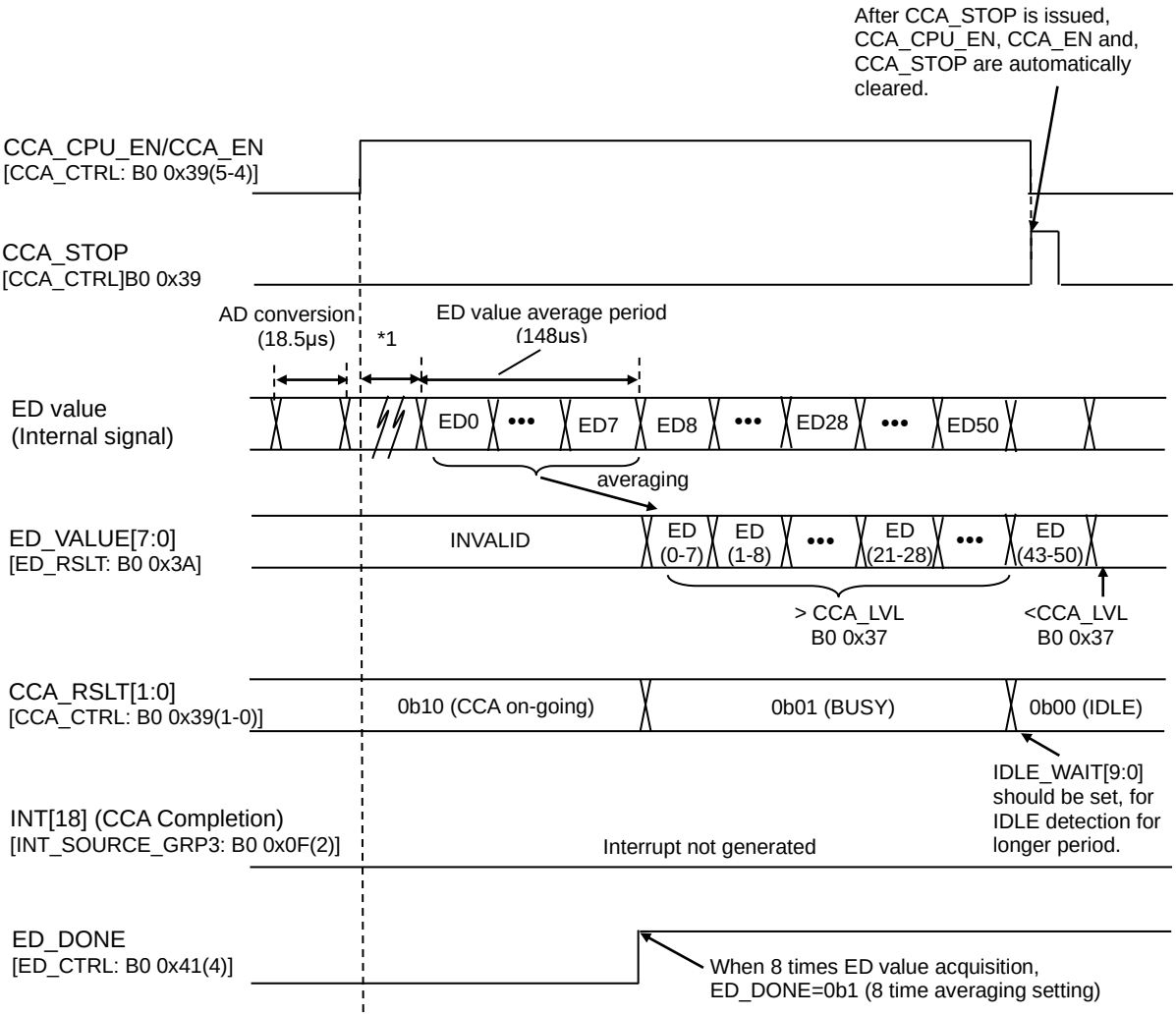
Like normal mode, CCA judgement is determined by average ED value in [ED_RSLT: B0 0x3A] register and CCA threshold defined by [CCA_LVL: B0 0x37] register. IF average ED value exceeds the CCA threshold value, it is considered as “BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) = 0b01 is set.
If average ED value is smaller than CCA threshold value and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3B], [IDLE_WAIT_H: B0 0x3C] registers, it is considered as “IDLE”. And CCA_RSLT[1:0] =0b00 is set. For details operation of CCA_IDLE_WAIT[9:0], please refer to ”IDLE detection for long time period”.

If an ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36] register, a given ED value is included in the averaging target of ED value calculation, IDLE judgement is not performed. In this case if average ED value exceeds CCA threshold level, it is considered as “BUSY” and CCA_RSLT[1:0] indicates 0b01. If average ED value is smaller than CCA threshold level, IDLE judgement is not determined. And CCA_RSLT[1:0] indicates 0b11. For details operation of ED value exeeceding [CCA_IGNORE_LVL: B0 0x36] register, please refer to ”IDLE determination exclusion under strong signal input”.

Continuous mode does not stop when “BUSY” or “IDLE” is detected. CCA operation continues until 0b1 is set to CCA_STOP([CCA_CTRL: B0 0x39(7)]). Result is updated every time ED value is acquired. CCA completion interrup (INT[18] group3) will not be generated.

The following is timing chart for continuous mode.
Set ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]) =0b1. (1.73 MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011. (8 times average)
Set IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)])=0b00 0000 0000 (IDLE detection 0µs)

[BUSY to IDLE transition, terminated with CCA_STOP]



NOTE:
*1 Digital filter delay is “AD conversion time * 8”. AD conversion time can be slected by ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]). Reset value is 1.73MHz and AD conversion time is 18.5µs.

(3) IDLE detection mode

IDLE detection mode continues CCA untill IDLE detection. Idle detectin CCA will be executed when RX_ON is issued while CCA_EN(CCA_CTRL: B0 0x39(4)])=0b1, CCA_CPU_EN(CCA_CTRL: B0 0x39(5)])=0b0 and CCA_IDLE_EN(CCA_CTRL: B0 0x39(6)])=0b1 are set.

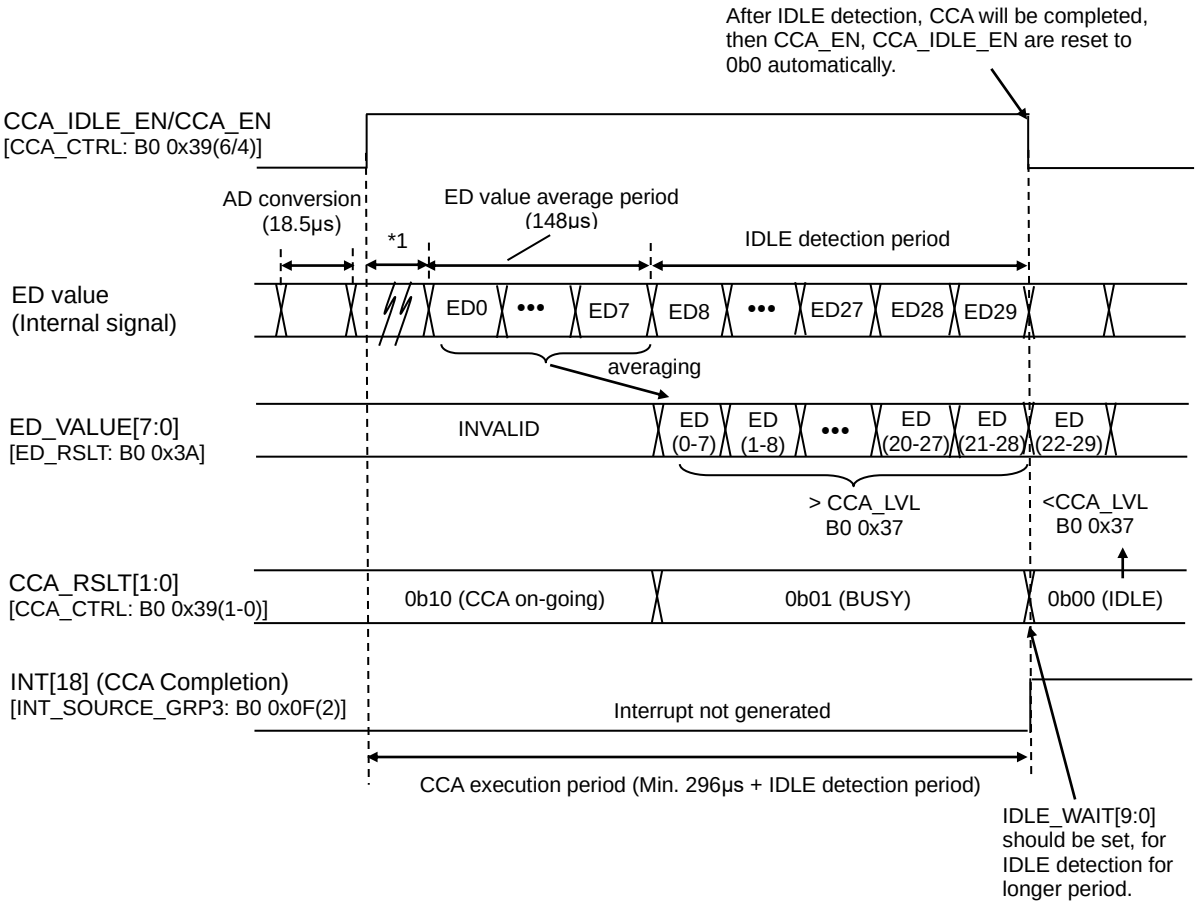
Like normal mode, CCA judgement is determined by average ED value in [ED_RSLT: B0 0x3A] register and CCA threshold defined by [CCA_LVL: B0 0x37] register. IF average ED value exceeds the CCA threshold value, it is considered as “BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)]) =0b01 is set.
If average ED value is smaller than CCA threshold value and maintains IDLE detection period which is defined by IDLE_WAIT[9:0] of the [IDLE_WAIT_L: B0 0x3B], [IDLE_WAIT_H: B0 0x3C] registers. it is considered as “IDLE”. And CCA_RSLT[1:0] =0b00 is set. For details operation of CCA_IDLE_WAIT[9:0], please refer to ”IDLE detection for longer period”.

In IDLE detection mode, only when IDLE is detected, CCA completion interrupt (INT[18] group3) is generated. After IDLE detection, CCA_EN and CCA_IDLE_EN are reset to 0b0.
Upon clearing CCA completion interrupt, CCA_RSLT[1:0] are reset to 0b00. Therefore CCA_RSLT[1:0] should be read before clearing CCA completion interrupt.

If an ED value exceeds the value defined by [CCA_IGNORE_LVL: B0 0x36] register, as long as a given ED value is included in the averaging target of ED value calculation, IDLE judgement is not performed. In this case, if average ED value is smaller than CCA threshold level, IDLE determination is not performed and CCA_RSLT[1:0] indicates 0b11. CCA operation continues until given ED value is out of averaging target and “IDLE” is determined. For details of ED value exceeding [CCA_IGNORE_LVL: B0 0x36] register, please refer to ”IDLE determination exclusion under strong signal input”.

The following is timing chart for IDLE detection mode.
Set ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]) =0b1. (1.73 MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011. (8 times average)
Set IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)])=0b00 0000 0000 (IDLE detection 0µs)

[Upon BUSY detection, continue CCA and IDLE detection case]



NOTE:
*1 Digital filter delay is “AD conversion time * 8”. AD conversion time can be slected by ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]). Reset value is 1.73MHz and AD conversion time is 18.5µs.

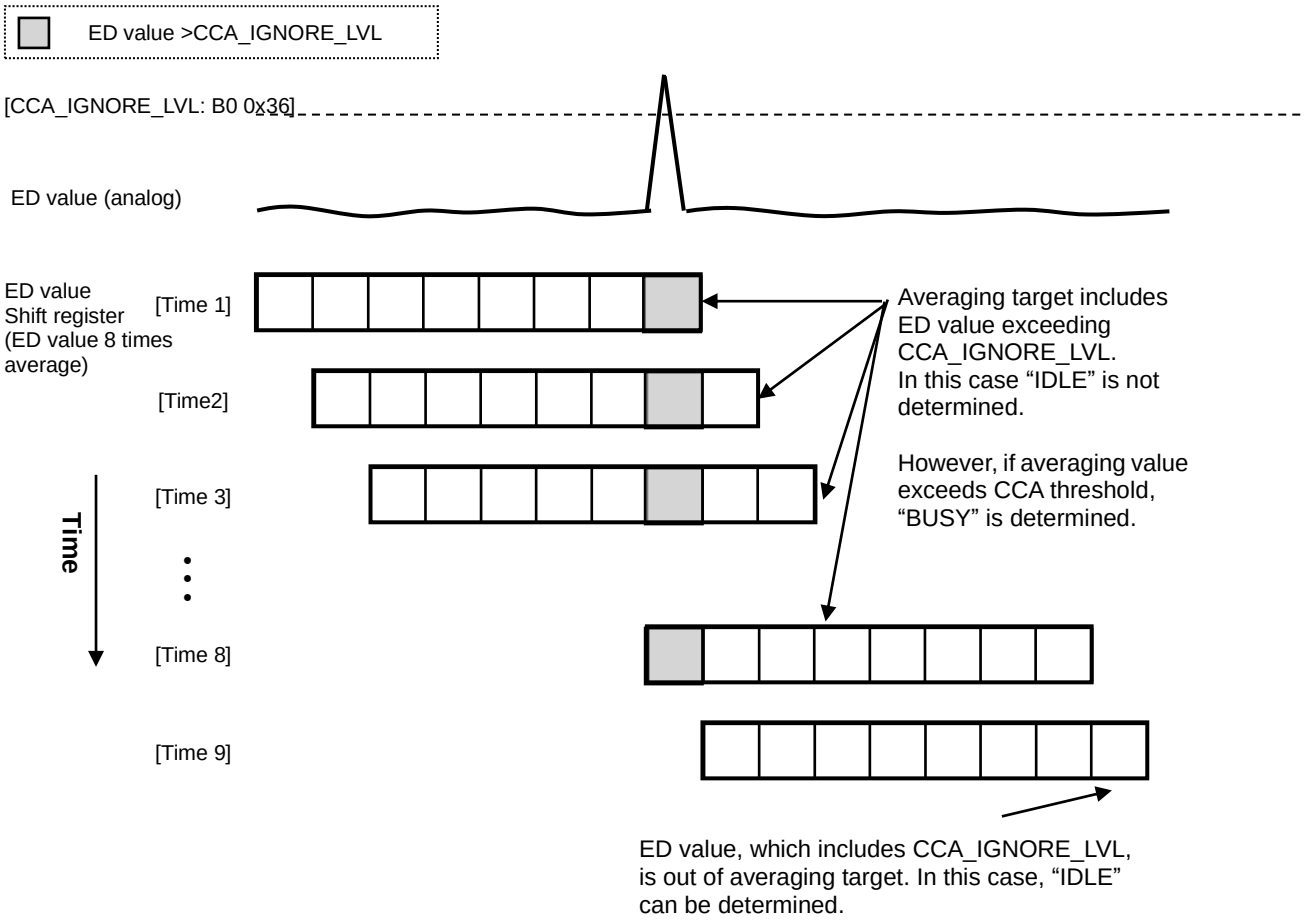
(4) IDLE determination exclusion under strong signal input

If acquired ED value exceeds [CCA_IGNORE_LVL: B0 0x36] register, IDLE dertermination is not performed as lon as a given ED value is included in the averaging target range. If average ED value including this strong ED value indicated in [ED_RSLT: B0 0x39] rehgiser exceeds the CCA threshold value defined by [CCA_LVL: B0 0x37] register, it is considered as ”BUSY”. And CCA_RSLT[1:0]([CCA_CTRL: B0 0x39(1-0)])=0b01 is set.

If average ED value is smaller than CCA threshold value, IDLE determination is not performed and CCA_RSLT[1:0] indicates 0b11 ”CCA evaluation on-going (ED value excluding CCA judgement acquisition)”. CCA will continue until “IDLE” or “BUSY” determination (in case of IDLE detection mode, “IDLE” is determined. In case of continuous mode, CCA_STOP([CCA_CTRL: B0 0x39(7)]) is issued.)

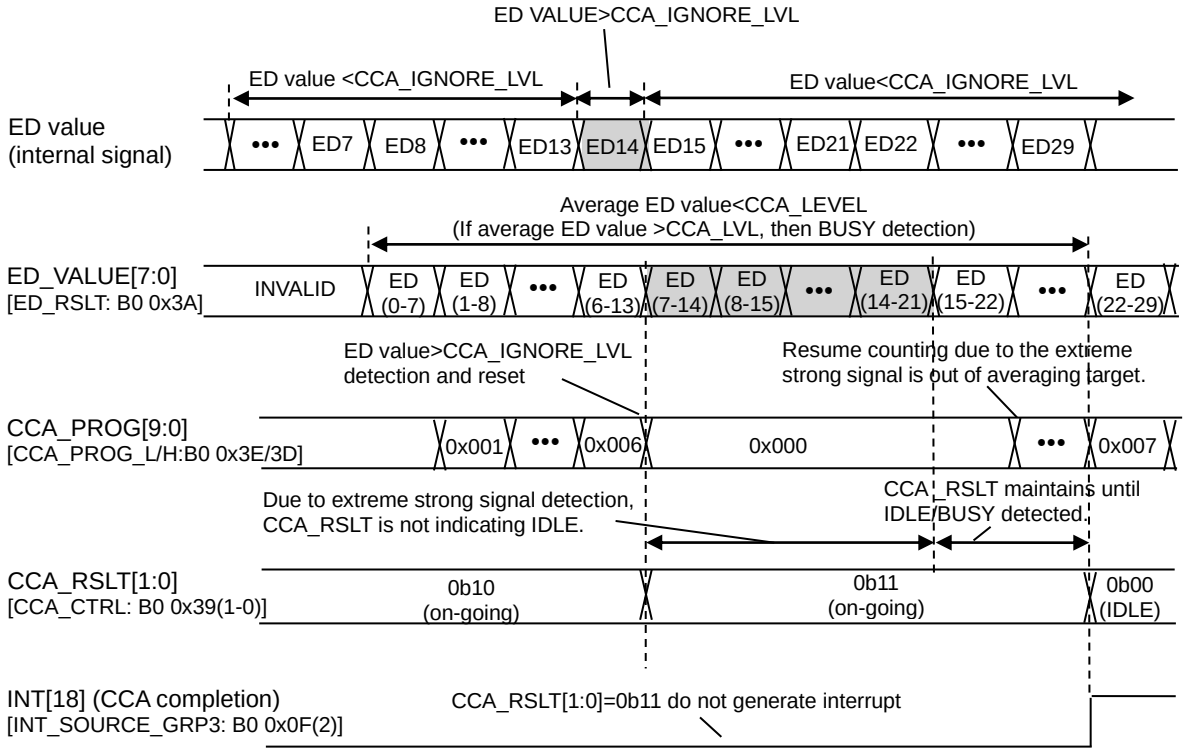
NOTE:
CCA completion interrupt (INT[18] group3) is generated only when “IDLE” or “BUSY” is determined. Therefore, if data whose ED value exceeds CCA_IGNORE_LVL are input intermittently, neither “IDLE” or “BUSY” can be determined and CCA may continues.

[ED value acquisition under extrem strong signal]



The following is timing chart for IDLE detemination exclusion under strong signal.
Set ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]) =0b1. (1.73 MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011. (8 times average)
Set IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)])=0b00 0000 0111 (IDLE detection 129.5µs)

[During IDLE_WAIT counting, detected extremly strong signal. After the given signal is out of averaging target, IDLE detection case]



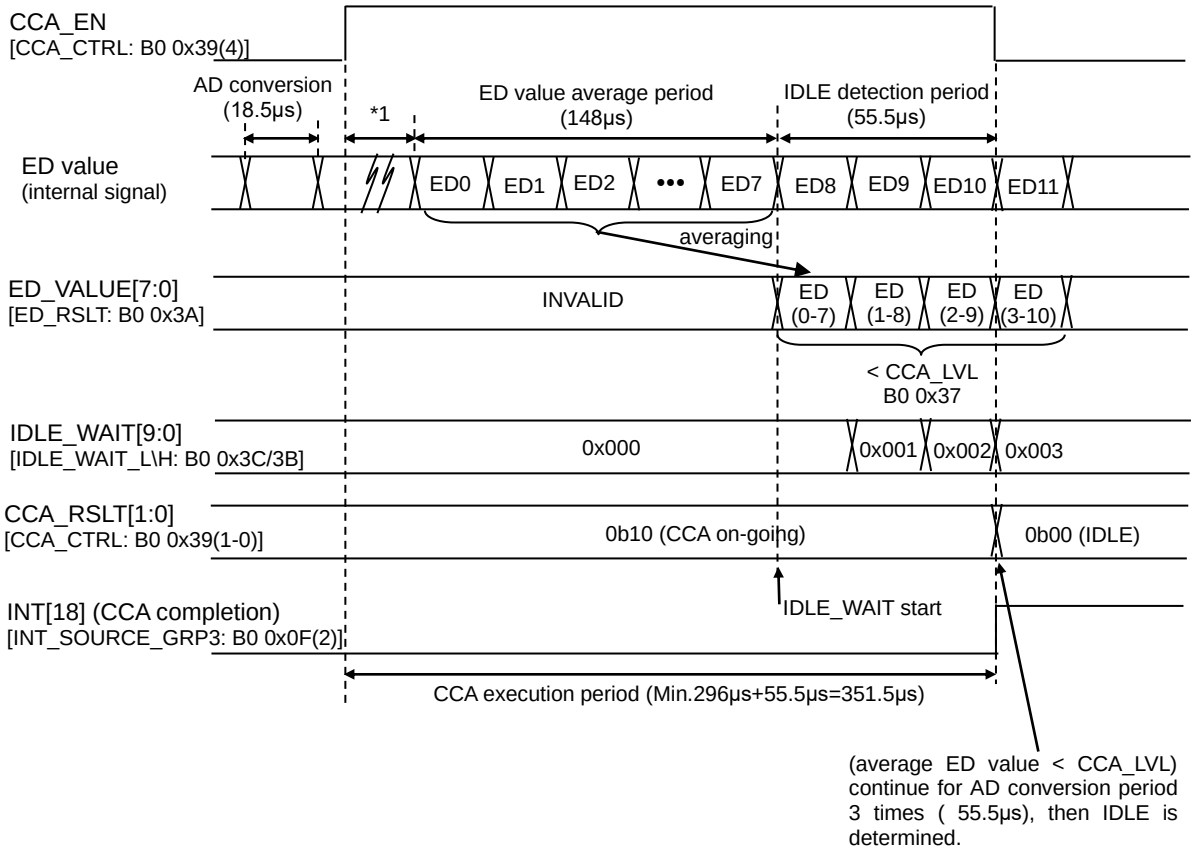
(5) IDLE detection for longer period

When CCA IDLE detection is performed for longer time period, IDLE_WAIT[9:0]([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)] can be used. By setting IDLE_WAIT [9:0], averaging period longer than the period (for example, AD conversion16µs, 8 times average setting 128µs) can be possible.

This function can be used for IDLE determination – by counting times when average ED value becomes smaller than CCA threshold defined by [CCA_LVL: B0 0x37] register. When counting exceed IDLE_WAIT [9:0], IDLE is determined. If average ED value exceeds CCA threshold level, imemediately "Busy" is determined without wait for IDLE_WAIT [9:0] period.

The following timing chart is IDLE detection setting IDLE_WAIT[9:0].
Set ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]) =0b1. (1.73 MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b011. (8 times average)
Set IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)])=0b00 0000 0011 (IDLE detection 55.5µs)

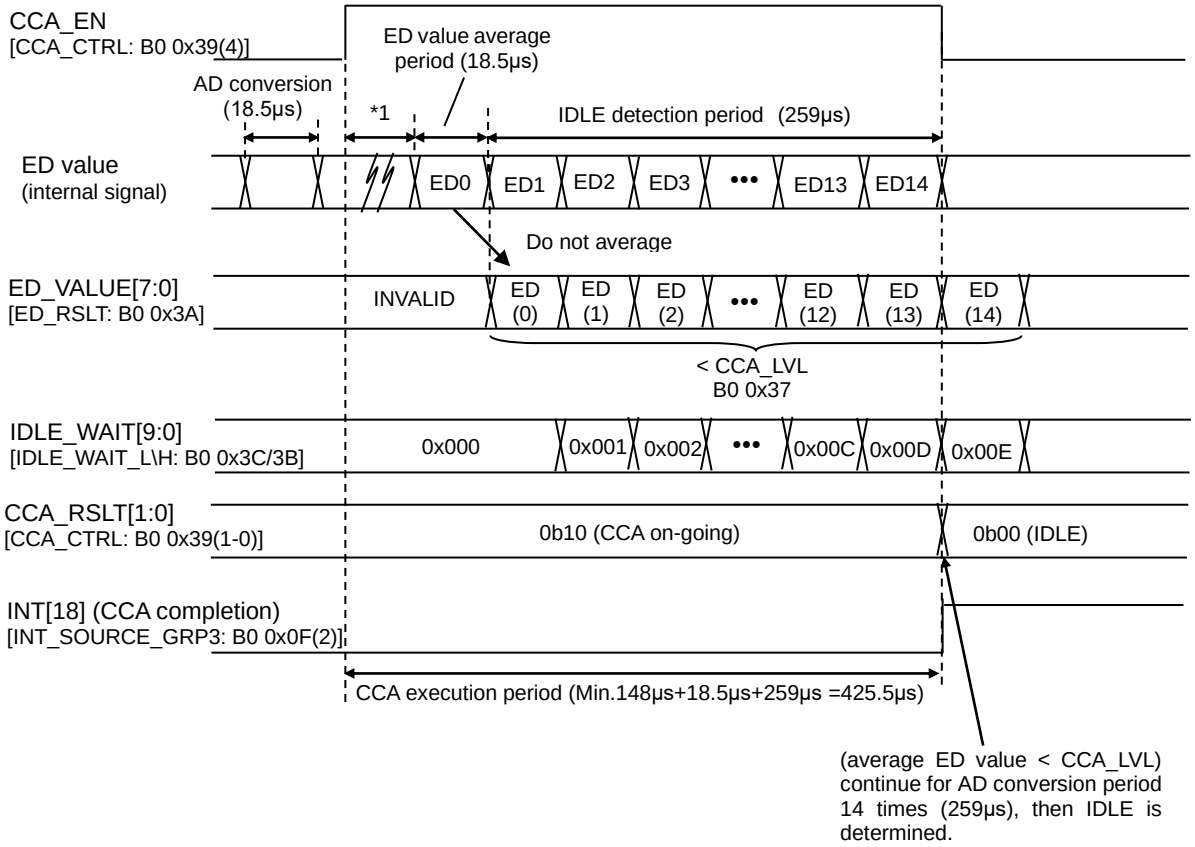
[ED value 8 timesv average IDLE detection case]



NOTE:

*1 Digital filter delay is "AD conversion time * 8". AD conversion time can be slected by ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]). Reset value is 1.73MHz and AD conversion time is 18.5µs.

[ED value 1time IDLE detection case]
Set ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]) =0b1. (1.73 MHz)
Set ED_AVG[2:0] ([ED_CTRL: B0 0x41(2-0)])=0b000. (1 time average)
Set IDLE_WAIT[9:0] ([IDLE_WAIT_L/H:B0 0x3C/3B(1-0)])=0b00 0000 1110 (IDLE detection 259µs)



NOTE:
*1 Digital filter delay is “AD conversion time * 8”. AD conversion time can be slected by ADC_CLK_SEL ([ADC_CLK_SET: B1 0x08(4)]). Reset value is 1.73MHz and AD conversion time is 18.5µs.

(6) CCA threshold setting

CCA threshold value defined by [CCA_LVL: B0 0x37] register, should be considered desired input leve (ED value), components variation, temperature fluctuation, loss at antenna and matching circuits. Input level and ED value are described in the follow table.

RSSI value = 1.35 * (input level[dBm] – variations[dBm] – other losses[dBm]) + offset
ED value (CCA threshold) = (RSSI value + RSSI_ADJ) * RSSI_MAG_ADJ

Item	Value	
	High Sensitivity Mode	High Linearity Mode
offset	164.5	156
Variation (individual, temp.)[dBm]	10	7
Other loss[dBm]	Antenna, matching circuits loss	
RSSI_ADJ	The setting of [RSSI_VAL:B1 0x14]	
RSSI_MAG_ADJ	The setting of [RSSI_ADJ: B0 0x66]	

Example) When input level threshold is set to -85dBm
conditions: High Linearity Mode, other loss = 1dB, RSSI_ADJ=0, RSSI_MAG_ADJ=4.5

RSSI value = 1.35 * (-85 - 7 – 1) + 156
= 30.45
CCA threshold = (30.45 + 0) * 4.5
= 137.025
~ 0x89

In order to validate whether CCA threshold is optimised or not, CCA should be executed and confirmimg level changing from IDLE to BUSY, every time input level is changed,

●Other Functions

●Data rate setting function

(1) Data rate change setting

ML73444 supports various TX/RX data rate setting defined by the following registers.
TX: [TX_RATE_H: B1 0x02] and [TX_RATE_L: B1 0x03] registers
RX: [RX_RATE1_H: B1 0x04], [RX_RATE1_L: B1 0x05] and [RX_RATE2: B1 0x06] registers
TX/RX data rate can be defined in the following formula.

[TX]

TX data rate [bps] = round (26MHz / 13/ TX_RATE[11:0])

Recommended values for each data rate are in the table below. Registers value below are automatically set to [TX_RATE_H],[TX_RATE_L] registers by setting TX_DRATE[3:0] ([DRATE_SET: B0 0x06(3-0)]).

TX data rate [kbps]	[TX_RATE_H][TX_RATE_L] register setting value	Data rate deviation [%] *1
1.2	1667d	-0.02
2.4	833d	0.04
4.8	417d	-0.08
9.6	208d	0.16
10.0	200d	0.00
11.52	174d	-0.22
15	133d	0.25

*1 Data rate deviation is assumption that frequency deviation of master clock(26MHz crystal oscillator or TCXO) is 0ppm.

[RX]

RX data rate [bps] = round (26MHz / {RX_RATE1[11:0] ×[RX_RATE2[6:0]})

Recommended values for each data rate are in the table below. Registers value below are automatically set to [RX_RATE1_H][RX_RATE1_L] [RX_RATE2] registers by setting RX_DRATE[3:0]([DRATE_SET:B0 0x06(7-4)]).

RX dta rate [kbps]	[RX_RATE1_H][RX_RATE1_L] register setting value	[RX_RATE2] register setting
1.2	169d	0d
2.4	85d	0d
4.8	42d	0d
9.6	21d	0d
10		
11.52		
15		

NOTE:
When LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1, [RX_RATE1_H/L] and [RX_RATE2] registers are not set automatically by setting RX_DRATE[3:0]. Please calcurate appropriate values by replacing the 8.66MHz to 26MHz in the above formula and set them to each register.

(2) Other register setting associate with data rate change

Data rate can be cahnged by RX_DRATE[3:0] ([DRATE_SET(7-4)]) and TX_DRATE[3:0] ([DRATE_SET(3-0)]), below registers may have to be changed.

NOTE:
Depending on data rate, the following chage may not be necessary. For details, please refer to each register description.

Parameters	Registers	
	Name	Address
Data rate	DRATE_SET	B0 0x06
Channel space	CH_SPACE_H	B1 0x23
	CH_SPACE_L	B1 0x24
Frequency deviation(GFSK)	GFSK_DEV_H	B1 0x30
	GFSK_DEV_L	B1 0x31
Frequencydeviation (FSK)	FSK_DEV0_H/GFIL0	B1 0x32
	FSK_DEV0_L/GFIL1	B1 0x33
	FSK_DEV1_H/GFIL2	B1 0x34
	FSK_DEV1_L/GFIL3	B1 0x35
	FSK_DEV2_H/GFIL4	B1 0x36
	FSK_DEV2_L/GFIL5	B1 0x37
	FSK_DEV3_H/GFIL6	B1 0x38
	FSK_DEV3_L	B1 0x39
	FSK_DEV4_H	B1 0x3A
	FSK_DEV4_L	B1 0x3B
Frequency deviation time(FSK)	FSK_TIM_ADJ4	B1 0x3C
	FSK_TIM_ADJ3	B1 0x3D
	FSK_TIM_ADJ2	B1 0x3E
	FSK_TIM_ADJ1	B1 0x3F
	FSK_TIM_ADJ0	B1 0x40
IF adjustment	IFF_ADJ_H	B0 0x5E
	IFF_ADJ_L	B0 0x5F
Demodulator adjustment1	DEMOD_SET1	B1 0x57
Demodulator adjustment2	DEMOD_SET2	B1 0x58
Demodulator adjustment3	DEMOD_SET3	B1 0x59
Demodulator adjustment4	DEMOD_SET4	B1 0x5A
Demodulator adjustment5	DEMOD_SET5	B1 0x5B
Demodulator adjustment6	DEMOD_SET6	B1 0x5C
Demodulator adjustment7	DEMOD_SET7	B1 0x5D
Demodulator adjustment8	DEMOD_SET8	B1 0x5E
Demodulator adjustment9	DEMOD_SET9	B1 0x5F

●Interrupt generation function

ML7344 support interrupt generation function. When interrupt occurs, interrupt notification signal (SINTN) become “L” to notify interrupt to the host MCU. Interrupt elements are divided into the 3 groups, [INT_SOURCE_GRP1: B0 0x0D], [INT_SOURCE_GRP2: B0 0x0E] and [INT_SOURCE_GRP3: B0 0x0F]. Each interrupt element can be maskalable using [INT_EN_GRP1: B0 0x10], [INT_EN_GRP2: B0 0x11] and [INT_EN_GRP3: B0 0x12] registers. Interrupt notification signal (SINTN) can be output from GPIO* or EXT_CLK. For output setting, please refer to [GPIO1_CTRL: B0 0x4E], [GPIO1_CTRL: B0 0x4F], [GPIO2_CTRL: B0 0x50], [GPIO3_CTRL: B0 0x51] and [EXTCLK_CTRL: B0 0x52] registers.

NOTE: In one of unmask interrupt event occurs, SINTN maintains Low.

(1) Interrupt events table

Each interrupt event is described below table.

Register	Interrupt name	Description
INT_SOURCE_GRP1	INT[0]	Clock stabilization completion interrupt
	INT[1]	VCO calibration completion interrupt/
	INT[2]	PLL unlock interrupt or VCO CAL request interrupt
	INT[3]	RF state transition completion interrupt
	INT[4]	FIFO-Empty interrupt
	INT[5]	FIFO-Full interrupt
	INT[6]	Wake-up timer completion interrupt
	INT[7]	Clock calibration completion interrupt
INT_SOURCE_GRP2	INT[8]	RX completion interrupt
	INT[9]	CRC error interrupt
	INT[10]	Reserved
	INT[11]	RX Length error interrupt
	INT[12]	RX FIFO access error interrupt
	INT[13]	SyncWord detection interrupt
	INT[14]	Field checking interrupt
	INT[15]	Sync error interrupt
INT_SOURCE_GRP3	INT[16]	TX completion interrupt
	INT[17]	TX Data request accept completion interrupt
	INT[18]	CCA completion interrupt
	INT[19]	TX Length error interrupt
	INT[20]	TX FIFO access error interrupt
	INT[21]	Reserved
	INT[22]	General purpose timer 1 interrupt
	INT[23]	General purpose timer 2 interrupt

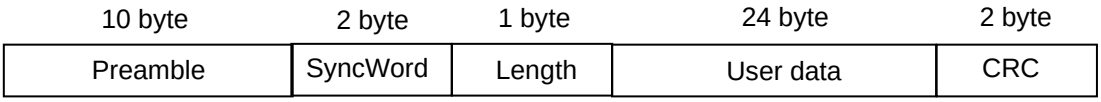
(2) Interrupt generation timing

In each interrupt generation, timing from reference point to interrupt generation (notification) are described in the following table. Timeout procedure for interrupt notification waiting are also described below.

NOTE:

(1)The values are described in units of "bit cycle" in the below table is the value at 100kbps. If using other data rate, please esitimate with appropriate "bit cycle".

(2)Below table uses the following format for TX/RX data.



(3)Even if each interrupt notification is masked, in case of interrupt occurence, interrupt elements are stored internally. Therefore, as soon as interrupt notification is unmasked, interrupt will generate.

Interrupt notice		Reference point	Timing from reference point to interrupt generation or interrupt generation timing
INT[0]	CLK stabilization completion	RESETN release (upon power-up)	50µs
		SLEEP release (recovered from SLEEP)	50µs
INT[1]	VCO calibration completion	VCO calibration start	2.6ms to 8.8ms
INT[2]	PLL unlock detection	-	(TX) during TX after PA enable. (RX) during RX after RX enable.
	VCO CAL request	-	(TX) rising edge of PA_ON signal. (RX) rising edge of RX enable signal.
INT[3]	RF state transition completion	TX_ON command	(IDLE) 1406µs (RX) 1188µs
		RX_ON command	(IDLE) µs (TX) 244µs
		TRX_OFF command	(TX) 147µs (RX) 4µs
		Force_TRX_OFF Command	(TX) 147µs (RX) 4µs
INT[4]	FIFO-Empty detection	(TX) TX_ON command (*1)	NRZ coding, Empty trigger level is set to 0x02 RF wake-up(1406µs)+ 35 byte (preamble to 22nd Data byte) * 8bit *10(bit cycle) =4206µs
		(RX) -	By FIFO read, remaining FIFO data is under trigger level
INT[5]	FIFO-FULL detection	(TX) -	By FIFO write, FIFO usage exceed trigger level
		(RX) SyncWord detection	NRZ coding, Full trigger level is set to 0x05 6byte (Length to 5th Data byte) * 8bit * 10µs(bit cycle) = 480µs
INT[6]	Wake-up timer completion	SLEEP setting	Wake-up timer is completed. For details, please refer to "wake-up timer"
INT[7]	Clock calibration completion	Calibration start	Calibration timer is completed. For details, please refer to "low speed clock shift detection function".

(*1) Before issuing TX_ON, writing full-length TX data to the TX_FIFO.

Interrupt notice		Reference point	Timing From reference point to interrupt generation or interrupt generation timing
INT[8]	RX completion	SyncWord detection	NRZ coding, Full trigger level is set to 0x05 27byte (Length to CRC) * 8bit * 10µs(bit cycle) = 2160µs
INT[9]	CRC error detection	SyncWord detection	(Format A/B) each RX CRC block calculation completion (Format C) RX completion
INT[10]	Reserved	-	-
INT[11]	RX Length error detection	SyncWord detection	80µs (L-field 1byte) 160µs (L-field 2byte)
INT[12]	RX FIFO access error detection	-	(1)overflow occurs because FIFO read is too slow. (2)underflow occurs because too many FIFO data is read
INT[13]	SyncWord detection	-	SyncWord detection
INT[14]	Field check completion	-	Match or mismatch detected in Field check
INT[15]	Sync error detection	-	During RX after SyncWord detection, out-of-sync detected. (When RXDIO_CTRL[1:0] ([DIO_SET: B0 0x0C(7-6)]) =0b00 or 0b11.)
INT[16]	TX completion	TX_ON command (*1)	RF wake-up+[TX data+3](bit) after =1406µs+(39byte ×10 +3)bit * 10µs (bit cycle)=4556µs
INT[17]	TX Data request accept completion	-	After full length data are written to the TX FIFO.
INT[18]	CCA completion	CCA execution start	(1)Normal mode (ED value calculation averaging time + IDLE_WAIT setting [IDLE_WAIT_H/L:B0 0x3B,3C]) * AD conversion time (2) IDLE detection mode ○IDLE judgment case (ED value calculation averaging time + IDLE_WAIT setting [IDLE_WAIT_H/L:B0 0x3B,3C]) * AD conversion time ○BUSY judgment case (ED value calculation averaging time) * AD conversion time AD conversion time can be changed by ADC_CLK_SEL ([ADC_CLK_SET:B1 0x08(4)]). ADC conversion time = 14.8µs at 2.17MHz 18.5µs at 1.73MHz For details, please refer to the “CCA (Clear Channel Assessment) function”.
INT[19]	TX Length error detection	-	After set length value to [TX_PKT_LEN_H/L: B0 0x7A/7B] register
INT[20]	TX FIFO access error detection	-	(1) When the next packet data is written to the TX_FIFO before transmitting previous packet data. (2) FIFO overflow when writing (3) FIFO underflow (no data) when transmitting
INT[21]	Reserved	-	

(*1) Before issuing TX_ON, writing full-length TX data to the TX_FIFO.

Interrupt notice		Reference point	Timing From reference point to interrupt generation or interrupt generation timing
INT[22]	General purpose timer 1 completion	Timer start	General purpose timer 1 completion General purpose timer clock cycle * Division setting [GT_CLK_SET: B0 0x33] * general purpose timer interval setting [GT1_TIMER:B0 0x34] For details, please refer to the “General purpose timer”.
INT[23]	General purpose timer 2 completion	Timer start	General purpose timer 2 completion General purpose timer clock cycle * Division setting [GT_CLK_SET: B0 0x33] * general purpose timer interval setting [GT2_TIMER:B0 0x35] For details, please refer to the “General purpose timer”.

(3) Clearing interrupt condition

The following table shows the condition of clearing each intereupt. As a procedure to clear the interrup, it is recommended that the interrupt to be cleared after masking the interrupt.

Interrupt notification		Conditions for clearing interrupts
INT[0]	CLK stabilization completion	After interrupt generated
INT[1]	VCO calibration completion	After interrupt generated
INT[2]	PLL unlock or VCO CAL request	After interrupt generated
INT[3]	RF state transition completion	After interrupt generated
INT[4]	FIFO-Empty	After interrupt generated (must clear before next FIFO-Empty trigger timing)
INT[5]	FIFO-Full	After interrupt generated (must clear before next FIFO-Full trigger timing)
INT[6]	Wake-up timer completion	After interrupt generated
INT[7]	Clock calibration completion	After interrupt generated
INT[8]	RX completion	After interrupt generated
INT[9]	CRC error	After interrupt generated
INT[10]	Reserved	-
INT[11]	RX Length error	After interrupt generated
INT[12]	RX FIFO access error	After interrupt generated
INT[13]	SyncWord detection	After interrupt generated
INT[14]	Field checking	After interrupt generated
INT[15]	Sync error	After interrupt generated
INT[16/]	TX completion	After interrupt generated
INT[17]	TX Data request accept completion	After interrupt generated
INT[18]	CCA completion	After interrupt generated Note: Clearing interrupt erase CCA result as well.
INT[19]	TX Length error	After interrupt generated
INT[20]	TX FIFO access error	After interrupt generated
INT[21]	Reserved	-
INT[22]	General purpose timer 1	After interrupt generated
INT[23]	General purpose timer 2	After interrupt generated

●Low speed clock shift detection function

ML7344 has low spleed frequency shift detection function to compensate inaccurate clock generated by RC oscillator (external clock or internal RC oscillation circuits). By detecting frequency shift of the wake up timer, host can set wake-up timer parameters which taking frequency shift into consideration. More accurate timer operation is possible by adjusting wake-up timer interval setting ([WUT_INTERVAL_H/L: B0 0x2F/0x30]) or continuous operation timer interval ([WU_DURATION: B0 0x31]).

Setting	Register
Frequency shift detection clock frequency setting	[CLK_CAL_SET: B0 0x70]
Clock calibration time	[CLK_CAL_TIME: B0 0x71]
Clock calibration result value	[CLK_CAL_H: B0 0x72], [CLK_CAL_L: B0 0x73]

This function is to measure low speed wake-up timer cycle by using accurate high speed internal clock and count result will be stored in [CLK_CAL_H/L: B0 0x72/0x73] registers. Above setting and count numbers are as follows:

High speed clock counter = {Wakeup timer clock cycle[SLEEP/WU_SET:B0 0x2D(2)] *
Clcok calibration time setting ([CLK_CAL_TIME:B0 0x71(5-0)]) /
{master clock cycle (26MHz) / clock division setting value ([CLK_CAL_SET: B0 0x70(7-4)])}

Clock calibration time is as follows:

Clock calibration time[s] = Wakeup timer clock cycle * Clock calibration time setting

[Example]
Assuming no division in the internal high speed clock, calibration time is set as 10 cycle and set 1,000 to the Wake-up interval timer value.

condition: Wakeup timer clock frequency = 44kHz
Detection clock division setting CLK_CAL_DIV[3:0][CLK_CAL_SET: B0 0x70(7-4)] = 0b0000
Clock calibration time setting [CLK_CAL_TIME] = 0x0A
Wake-up interval timert setting [WUT_INTERVAL_H/L:B0 0x2F,30] = 0x03E8

Theoretical high speed clock count = (1/44kHz) ***** 10 / (1/(26/1)MHz)
= 5909(0x1715)

If getting [CLK_CAL_H/L:B0 0x72,73] = 0x162E (5678)
Counter difference = 5678-5909 = -231
Frequency shift = 1/{1/44kHz + (-231) / 10 * 1 / 26MHz} – 44kHz = 1.79 kHz
Then finding wake-up timer clock frequency accuracy is +4.1% higher. And the compensation vale (C) is calcurared as below:

C = Wake-up timer interval([WUT_INTERVAL_H/L:B0 0x2F,30]) ***** frequecy shift / 44kHz
= 1000 ***** 1.79kHz / 44kHz =41

Therefore, setting [WUT_INTERVAL_H/L:B0 0x2F,30] = 1000+41 =0x0411 to achive more accurate inteval timinig.

NOTE:
If calibration time is too short or if high speed counter is divided into low speed clock, calibration may not be accurate.

●Antenna switching function

(1) Antenna switching function

By using [2DIV_CTRL: B0 0x48], [ANT_CTRL: B0 0x4C], [SPI/EXT_PA_CTRL: B0 0x53] registers, TX-RX signal selection (TRX_SW), antenna switching signal (ANT_SW) can be controlled.

ML7344 can support both SPDT antena swith control. ANT_SW signal and TRX_SW signal output considion for each antenna switch are explained below.

ANT_SW, TRX_SW output condition of each Idle, TX, RX state are as follow. (default setting) If INV_TRX_SW([2DIV_CTRL: B0 0x48(2)])=0b1, polarity of TRX_SW is reversed.

TX/RX condition	INV_TRX_SW=0b0 (default setting)		INV_TRX_SW=0b1 (polarity reverse)		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	L	H	Idle state
TX	L	H	L	L	TX state
RX	L	L	L	H	RX state

In the above setting, If INV_ANT_SW([2DIV_CTRL: B0 0x48(3)])=0b1, ANT_CTRL1([2DIV_CTRL: B0 0x48(5)])=0b1 are set, polarity of ANT_SW pin is reversed.

TX/RX state	INV_ANT_SW=0b0 ANT_CTRL1=any (default setting)		INV_ANT_SW=0b1 ANT_CTRL1=0b1		Description
	ANT_SW	TRX_SW	ANT_SW	TRX_SW	
Idle	L	L	H	L	Idle state
TX	L	H	H	H	TX state
RX	L	L	H	L	RX state

(2) Antenna switch forced setting

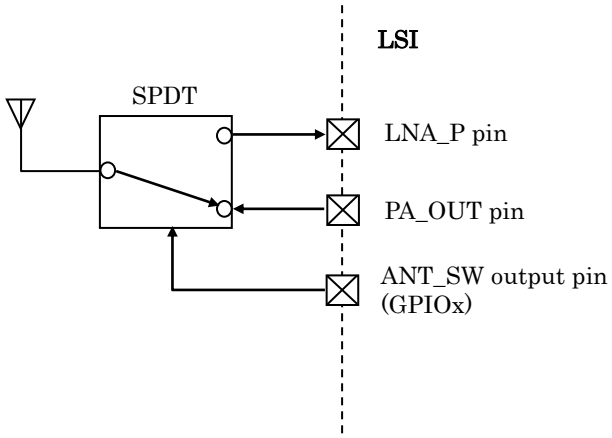
By [ANT_CTRL: B0 0x4C] register, ANT_SW pin output conditions can be set to fix.

TX: By TX_ANT_EN([ANT_CTRL: B0 0x4C(0)])=0b1, TX_ANT([ANT_CTRL: B0 0x4C(1)]) condition will be output.
RX: By RX_ANT_EN([ANT_CTRL: B0 0x4C(4)])=0b1, RX_ANT([ANT_CTRL: B0 0x4C(5)]) condition will be output.

However, output is defined by [GPIIO*_CTRL: B0 0x4E - 0x51] register , [GPIIO*_CTRL:B0 0x4E - 0x51] registers setting has higer priority.

Antenna switching control signals can be also used as below.

Example 1) using SPDT switches



(Note) altenate external PA control signal exsits. (GPIOx or EXT_CLK pin)
(Note) external circuits around LNA_P pin, PA_OUTpin and antenna switch(SPDT) are omitted in this example.

■LSI adjustment items and adjustment method

●PA adjustment

ML7344E/J have output circuits for 1mW and 20mW (10mW as well) and ML7344C has output circuit for 20mW and 100mW. Output circuits can be selected by PA_MODE[1:0] ([PA_MODE: B0 0x67(5-4)]).

PA_MODE[1:0]	Output circuit	
	ML7344E/J	ML7344C
0b00	1mW	Not allowed
0b01	10mW	20mW
0b10	20mW	100mW
0b11	Not allowed	

Output power can be adjusted by the following 3 registers.
Coarse adjustment 1 PA_REG[3:0] ([PA_MODE: B0 0x67(3-0)]) 16 resolutions
Coarse adjustment 2 PA_ ADJ[3:0] ([PA_ADJ: B0 0x69(3-0)]) 16 resolutions
Fine adjustment PA REG_FINE_ADJ[4:0] ([PA_REG_FINE_ADJ: B0 0x68(4-0)]) 32 resolutions

Coarse adjustment 1: PA regulator adjustment
Setting regulator voltage according to the desired output level.
However, please set PA regulator voltage to less than [VDD_PA(pin#22) – 0.3V].

PA_REG[3:0] [PA_MODE:B0 0x67]	PA regulator Voltage [V]
0b0000	1.20
0b0001	1.32
0b0010	1.44
0b0011	1.56
0b0100	1.68
0b0101	1.80
0b0110	1.92
0b0111	2.04
0b1000	2.16
0b1001	2.28
0b1010	2.40
0b1011	2.52
0b1100	2.64
0b1101	2.76
0b1110	2.88
0b1111	3.00

Coarse adjustment 2: PA output gain adjustment

Controlling output power by adjusting PA gain. The typical PA output for PA_ADJ at 10mW is as follows.

10mW	Power [dBm]					
[PA_ADJ: B0 0x69(3-0)]	PA_REG[3:0] =0	PA_REG[3:0] =1	PA_REG[3:0] =2	PA_REG[3:0] =3	PA_REG[3:0] =4	PA_REG[3:0] =5
0	3.8	5.0	5.9	6.3	6.8	7.0
1	4.8	6.2	7.1	7.6	8.2	8.4
2	5.5	6.9	8.0	8.6	9.1	9.5
3	6.1	7.5	8.7	9.4	10.0	10.4
4	6.5	8.0	9.1	9.8	10.5	11.0
5	6.9	8.5	9.6	10.4	11.0	11.5
6	7.2	8.8	9.9	10.8	11.4	12.0
7	7.5	9.1	10.2	11.0	11.8	12.3
8	7.6	9.2	10.3	11.2	11.9	12.4
9	7.8	9.4	10.6	11.4	12.1	12.7
10	8.0	9.6	10.8	11.6	12.5	12.9
11	8.2	9.7	10.9	11.8	12.6	13.1
12	8.3	9.8	11.0	11.9	12.7	13.2
13	8.4	9.9	11.2	12.0	12.8	13.4
14	8.4	10.1	11.3	12.1	13.0	13.5
15	8.6	10.1	11.4	12.3	13.0	13.6

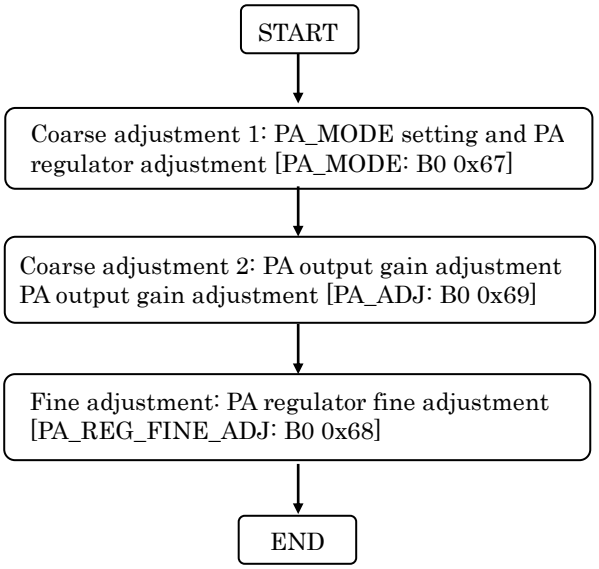
Fine adjustment: PA regulator voltage fine adjustment

Fine tuning output power by adjusting PA regulator voltage. Adjustment step is less than 0.2dB. However, please set PA regulator voltage to less than [VDD_PA(pin#22) – 0.3V].

PA_REG_FINE_ADJ[4:0] [PA_REG_FINE_ADJ:B0 0x68]	PA regulator Voltage [V]
0b0_0000	89.5%
0b0_0001	90.1%
0b0_0010	90.7%
0b0_0011	91.3%
0b0_0100	91.9%
0b0_0101	92.5%
0b0_0110	93.2%
0b0_0111	93.8%
0b0_1000	94.4%
0b0_1001	95.1%
0b0_1010	95.8%
0b0_1011	96.5%
0b0_1100	97.1%
0b0_1101	97.8%
0b0_1110	98.6%
0b0_1111	99.3%
0b1_0000	100.0%
0b1_0001	100.7%
0b1_0010	101.5%
0b1_0011	102.3%
0b1_0100	103.0%
0b1_0101	103.8%
0b1_0110	104.6%
0b1_0111	105.4%
0b1_1000	106.3%
0b1_1001	107.1%
0b1_1010	107.9%
0b1_1011	108.8%
0b1_1100	109.7%
0b1_1101	110.6%
0b1_1110	111.5%
0b1_1111	112.4%

NOTE:
In order to achieve the most optimized result, Matching circuits may vary depending on the output mode.

●PA output adjustment flow



●I/Q adjustment

Image rejection ratio can be adjusted by tuning IQ signal balance. The adjustment procedure is as follows:

1. From SG, image frequency signal is input to ANT pin (#24).
   Input signal: no modulation wave
   Input frequency: channel frequency - (2 * IF frequency)
   IF frequency = 200kHz:
   Input level: -70dBm

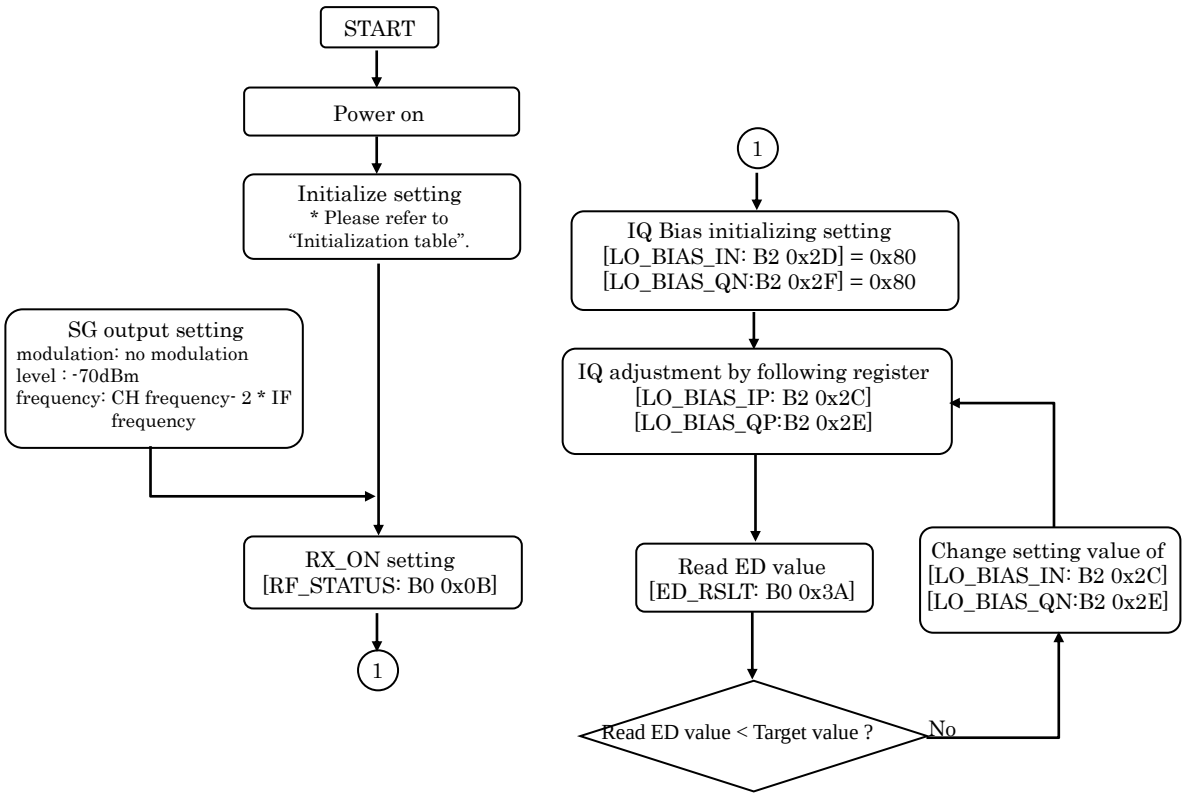
2. Isuuing RX_ON by [RF_STATUS:B0 0x0b] register, by adjusting
- [LO_BIAS_IP: B2 0x2C]、From 0x50 To 0xD0 Step 0x04
- [LO_BIAS_IN: B2 0x2D]、From 0x60 To 0xA0 Step 0x10
- [LO_BIAS_QP: B2 0x2E]、From 0x50 To 0xD0 Step 0x04
- [LO_BIAS_QN: B2 0x2F]、From 0x60 To 0xA0 Step 0x10

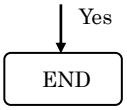
, finding setting value so that ED value [ED_RSLT: B0 0x3A] is minimum.

3. It is possible to choice the adjusted value and break the above search flow at halfway.
   To obtain minimum 30dB blocking characteristic for image frequency, ML7344 requires more than 40dB attenuation for image frequency (IMRR: IMage Rejection Ratio). The 10dB differ is caused by co-channel blocking characteristic of ML7344. Because input -70dBm signal during IQ adjustment, IMRR is more than 40dB if ML7344 indicates less than -110dBm by ED value. It is possible to break adjustment flow at halfway by using the ED value as “Target value” in the IQ adjustment flow.

●IQ adjustment flow

For IQ adjustment, using Bank2 (closed Bank) registers. Any other register access is inhibited.





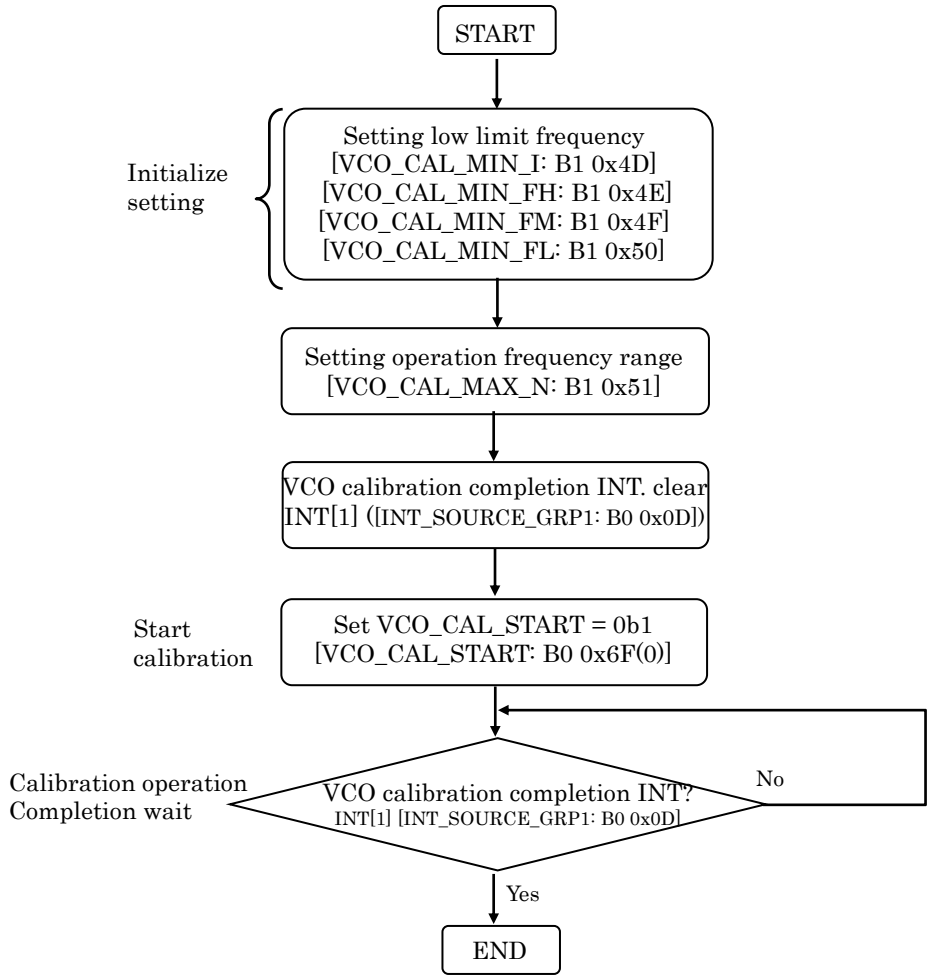
●VCO adjustment

In order to compensate VCO operation margin, optimized capacitance compensation value should be set in each TX/RX operation and frequency. This capacitance compensation value can be acquired by VCO calibration.

By performing VCO calibration when power-up or reset, acquired capacitance compensation values for upper limit and lower limit of operation frequency range (for both TX/RX), based on this value optimised capacitance value is applied during TX/RX operation.

●VCO adjustment flow

The following flow is the procedure for acquiring capacitance compensation value when power-up or reset.



NOTE:1) VCO calibration should be performed only during IDLE state.

VCO calibration is necessary every 2.6ms to 8.8ms.
After completion, capacitance compensation values are stored in the following registers.
Capacitance compensation value at TX low limit frequency: [TXVCAL_MIN: B1 0x52]
Capacitance compensation value at TX upper limit frequency: [TXVCAL_MAX: B1 0x53]
Capacitance compensation value at RX low limit frequency: [RXVCAL_MIN: B1 0x54]
Capacitance compensation value at RX upper limit frequency: [RXVCAL_MAX: B1 0x55]

In actual operation, based on the 2 compensation values for each TX/RX, the most optimized capacitance value for the frequency is calculated and applied. The calculated value is stored in [VCO_CAL: B0 0x6E].

By evaluation stage, if below values are stored in the MCU memory and uses these values upon reset or power-up, calibration operation can be omitted.

Registers to be saved in the MCU memory.
[VCO_CAL_MIN_I: B1 0x4D]
[VCO_CAL_MIN_FH: B1 0x4E]
[VCO_CAL_MIN_FM: B1 0x4F]
[VCO_CAL_MIN_FL: B1 0x50]
[VCO_CAL_MAX_N: B1 0x51]
[TXVCAL_MIN: B1 0x52]
[TXVCAL_MAX: B1 0x53]
[RXVCAL_MIN: B1 0x54]
[RXVCAL_MAX: B1 0x55]

After issuing VCO calibration, VCO tuning voltage may be out of control range by the temperature difference between operating timing and VCO calibration timing. If activating RF when VCO tuninng voltage is out of control range, the margine of VCO operation will be lost and it may cause the PLL unlock. When detecting VCO tuning voltage is out of control range, VCO calibration should be re-issued or set VCO caluibration value which has operating margine at that temperature.
The ML7344 has the function of comparing the VCO tunign voltage with upper and lower limit voltages and determining it is in the control range or not and indiacting the result. After detecting VCO tuning voltage is out of contol range, it can be notified by INT[2] (group1: VCO CAL request interrupt). This function is valid by setting VTUNE_COMP_ON([VTUNE_COMP_ON: B2 0x40(5)])=0b1.

[Relative controlo bit]
The comparison result with maximum threshold: VTUNE_COMP_H ([VCO_VTRSLT:B0 0x40(1)])
The comparison result with minimum threshold: VTUNE_COMP_L ([VCO_VTRSLT:B0 0x40(0)])
VCO CAL request interrupt enable setting: VTUNE_INT_ENB ([VCO_VTRSLT:B0 0x40(2)])
State control after PLL unlock detection: PLL_LD_EN ([PLL_LOCK_DETECT:B1 0x0B(7)]

[VCO voltage condition]

VTUNE_COMP_L [VCO_VTRSLT:B0 0x40(0)]	VTUNE_COMP_H [VCO_VTRSLT:B0 0x40(1)]	Condition
0b0	0b0	Ordinary
0b0	0b1	Out of control range (beyond upper level)
0b1	0b0	Out of control range (below lower level)
0b1	0b1	Extra ordinary

NOTE:
1. For low limit frequency, please use frequency at least 400kHz lower than operation frequency
2. For upper limit frequency should be selected so that operation frequency is in the frequency range.
3. In case of like a channel change, if the setting frequency is outside of calibration frequency range, calibration process has to be performed again with proper frequency.
4. INT[2] (group1) will generate by detecting PLL unlock or VCO CAL request (when VTUNE_INT_ENB ([VCO_VTRSLT:B0 0x40(2)])=0b1). The following shows the ML7344 opereation related with LSI state and PLL_LD_EN([PLL_LOCK_DETECT:B1 0x0B(7)]) setting, after interrupt generation.

[In case of PLL unlock interrupt]

LSI state	check timig of PLL unlock detection	PLL lock detection control setting and ML7344 operation after interrupt generation	
		PLL_LD_EN=0b1 [PLL_LOCK_DETECT:B1 0x0B(7)]	PLL_LD_EN=0b0 [PLL_LOCK_DETECT:B1 0x0B(7)]
TX	PA_ON ="H"	interrupt occurs and TX stops forcibly	interrupt occurs and TX is continued
RX	RX enable ="H"	interrupt occurs and RX is continued	interrupt occurs and RX is continued

[In case of VCO CAL request interrupt]

LSI state	check timig of PLL unlock detection	PLL lock detection control setting and ML7344 operation after interrupt generation	
		PLL_LD_EN=0b1 [PLL_LOCK_DETECT:B1 0x0B(7)]	PLL_LD_EN=0b0 [PLL_LOCK_DETECT:B1 0x0B(7)]
TX	Rising edge of PA_ON signal	interrupt occurs and TX stops forcibly	interrupt occurs and TX is continued
RX	Rising edhe of RX enable signal	interrupt occurs and RX is continued	interrupt occurs and RX is continued

●VCO low limit frequency setting

VCO low limit frequency can be set as described in the "channel frequency setting". I is set to [VCO_CAL_MIN_I:B1 0x4D] register, F is set to [VCO_CAL_MIN_FH:B1 0x4E], [VCO_CAL_MIN_FM:B1 0x4F], [VCO_CAL_MIN_FL:B1 0x50] in MSB – LSB order.

example) If operation low limit frequency is 426.6MHz, setting value should be lower than 400kHz. Then in following example, low limit frequency is set to 426.MHz, master clock frequency is 26MHz.

I = 426MHz/26MHz (Integer part) = 16(0x10)
F =(426MHz/26MHz-16) * 2^{20} (Integer part) = 403298 (0x062762)

Setting values for each register is as follows:

[VCO_CAL_MIN_I] = 0x10
[VCO_CAL_MIN_FH] = 0x06
[VCO_CAL_MIN_FM] = 0x27
[VCO_CAL_MIN_FL] = 0x62

●VCO upper limit frequency setting

VCO upper limit frequency is calculated as following formula, based on low limit frequency values and [VCO_CAL_MAX_N:B1 0x51] register.

VCO calibration upper limit frequency =
VCO calibration low limit frequency (B1 0x4D-0x50) + ΔF(B1 0x51)

ΔF is defined in the table below

VCO_CAL_MAX_N[3:0]	ΔF[MHz]
0b0000	0
0b0001	0.8125
0b0010	1.625
0b0011	3.25
0b0100	6.5
0b0101	13
0b0110	26
0b0111	52
Other than above	prohibited

●Energy detection value (ED value) adjustment

ED value is calculated by RSSI signal (analog signal) from RF part, By performing the following adjustment, it is possible to correct the variation in LSIs.

[ED value]

ED value is calculated as following formula,

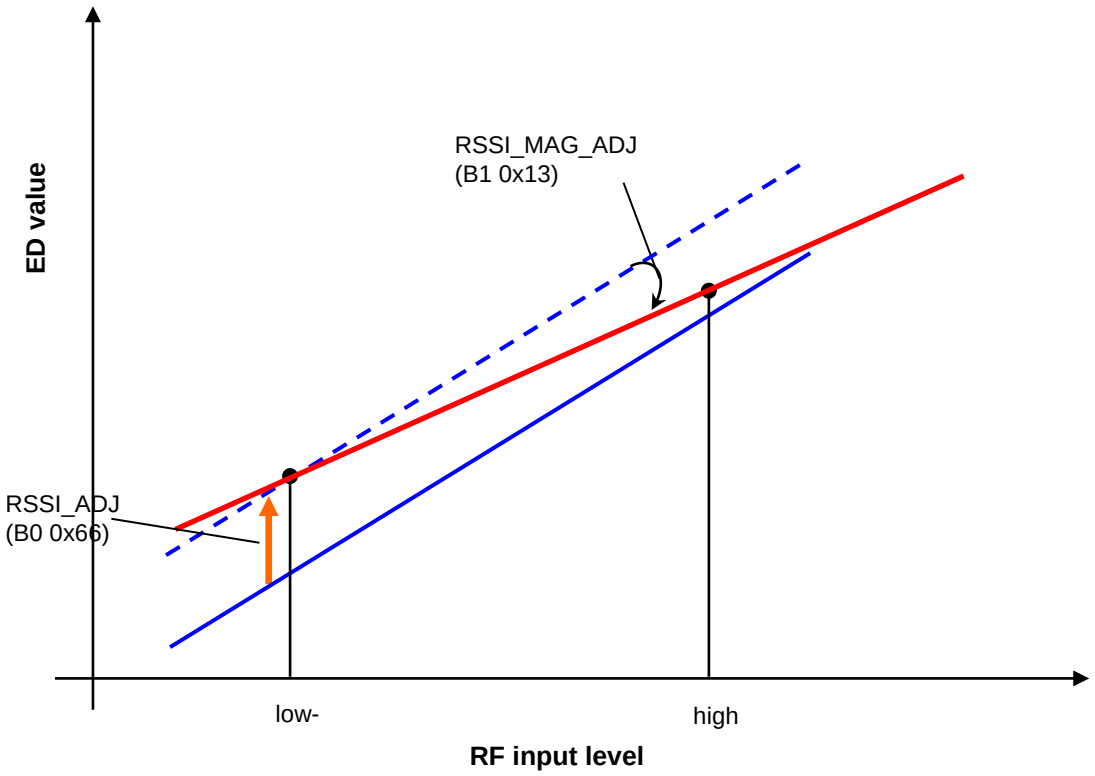
RSSI value = 1.35 * (input level[dBm] – variations[dBm] – other losses[dBm]) + offset

ED value (CCA threshold) = (RSSI value + RSSI_ADJ) * RSSI_MAG_ADJ

Item	Value	
	High Sensitivity Mode	High Linearity Mode
offset	164.5	156
Variation (individual, temp.)[dBm]	10	7
Other loss[dBm]	Antenna, matching circuits loss	
RSSI_ADJ	The setting of [RSSI_VAL:B1 0x14]	
RSSI_MAG_ADJ	The setting of [RSSI_ADJ: B0 0x66]	

[ED value asjustment]

At first, inputting the low-level signal to ANT terminal. Adjusting the RSSI_ADJ value so that ED_VALUE [ED_RSLT:B0 0x3A(7-0)] indicates the target value of the low-level signal.. Next inputting the high-level signal and adjusting the RSSI_MAG_ADJ value so that ED_VALUE indicates the target value of the high-level signal. Repeat several times in accordance with the required accuracy.



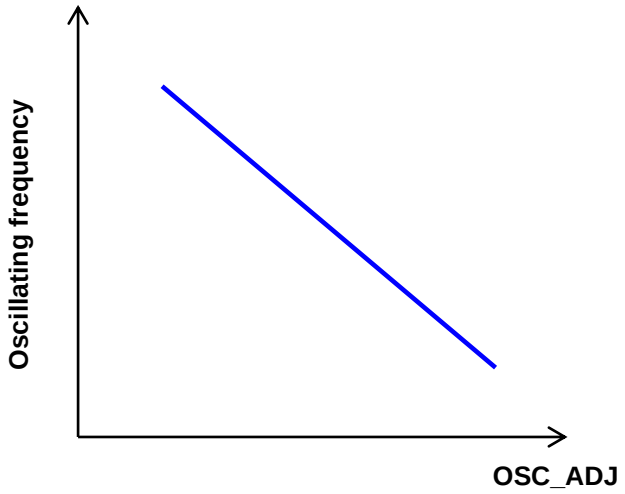
●Oscillation circuit adjustment

In case of using a crystal oscillator (ML7344xC), crystal oscillator frequency deviation can be tuned by adjusting load capacitance of XIN pin (pin#5) and XOUT pin (pin #6). Load capacitance can be adjusted by [OSC_ADJ1: B0 0x62] and [OSC_ADJ2: B0 0x63].

Adjustable capacitance is as follows:

[OSC_ADJ1] Coarse adjustment of load capacitance: **0.7pF/step (setting range: 0x00 to 0x0F)**

[OSC_ADJ2] Fine adjustment of load capacitance: **0.02pF/step (setting range: 0x00 to 0x77)**



■Resister setting

●Initialization table

ML7344 needs initilaization. For the value to each register, please refer to the "ML7344 Initilaization Table" document.

●RX mode setting

ML7344 has two RX modes. One is "High sensitivity mode" that is tuned for minimum RX sensitivity. It achieves -118dBm under condition of BER<0.1%, 4.8kbps and Fdev=3kHz. The other is "High linearity mode" that improves linearity about 6dB, so characteristics of blocking and power detection rang are grown instead of sensitivity degradation about 3dB. For swtiching RX mode, set the register [LNA_GAIN1:B2 0x28] as below.

RX mode	[LNA_GAIN1:B2 0x28]
High sensitivity mode	0xF7
High linearity mode	0x07

●BER measurement setting

The following registers setting are necessary for RX side when measuring BER.

[DIO_SET: B0 0x0C] = 0x40
[MON_CTRL: B0 0x4D] = 0x80
[GPIO0_CTRL: B0 0x4F] to [GPIO3_CTRL: B0 0x52] for setting DCLK/DIO output pins.
[GAIN_HTOM: B1 0x0E] = 0x1E

When termiate BER measurement and reurn from RX state, Force TRX_OFF should be issued by SET_TRX[3:0] ([RF_STATUS:B0 0x0b(3-0]) =0b0011.

●Wireless M-bus setting

The following parameter tables are example for programing each Wireless M-Bus mode (N/F).

●Mode N

(Channel frequency: 169.4125MHz, Modulation: GFSK, Data Rate: 4800bps)

Parameter	Register		Setting Value
	Name	Address	
TX frequency	TXFREQ_I	B1 0x1B	0x0D
	TXFREQ_FH	B1 0x1C	0x00
	TXFREQ_FM	B1 0x1D	0x81
	TXFREQ_FL	B1 0x1E	0xF8
RX frequency	RXFREQ_I	B1 0x1F	0x0D
	RXFREQ_FH	B1 0x20	0x00
	RXFREQ_FM	B1 0x21	0x81
	RXFREQ_FL	B1 0x22	0xF8
Channel space	CH_SPACE_H	B1 0x23	0x07
	CH_SPACE_L	B1 0x24	0xE0
PLL frequency division	PLL_DIV_SET	B1 0x1A	0x10

Data rate	DRATE_SET	B0 0x06	0x22
TX\RX data configulation	DATA_SET1	B0 0x07	0x10
	DATA_SET2	B0 0x08	0x00
Frequency deviation (GFSK)	GFSK_DEV_H	B1 0x30	0x00
	GFSK_DEV_L	B1 0x31	0x60

Mode N setting (continued)

Parameter	Register		Setting Value
	Name	Address	
Frequency deviation (FSK)	FSK_DEV0_H/GFIL0	B1 0x32	0x49
	FSK_DEV0_L/GFIL1	B1 0x33	0xA7
	FSK_DEV1_H/GFIL2	B1 0x34	0x0F
	FSK_DEV1_L/GFIL3	B1 0x35	0x14
	FSK_DEV2_H/GFIL4	B1 0x36	0x19
	FSK_DEV2_L/GFIL5	B1 0x37	0x1D
	FSK_DEV3_H/GFIL6	B1 0x38	0x1E
	FSK_DEV3_L	B1 0x39	-
	FSK_DEV4_H	B1 0x3A	-
	FSK_DEV4_L	B1 0x3B	-
Frequency deviation time	FSK_TIM_ADJ0	B1 0x3C	-
	FSK_TIM_ADJ1	B1 0x3D	-
	FSK_TIM_ADJ2	B1 0x3E	-
	FSK_TIM_ADJ3	B1 0x3F	-
	FSK_TIM_ADJ4	B1 0x40	-
Preamble length	TXPR_LEN_H	B0 0x42	0x00
	TXPR_LEN_L	B0 0x43	0x08
SyncWord length	SYNC_WORD_LEN	B1 0x25	0x10
SyncWord pattern 1	SYNC_WORD1_SET0	B1 0x27	0x00
	SYNC_WORD1_SET1	B1 0x28	0x00
	SYNC_WORD1_SET2	B1 0x29	0xF6
	SYNC_WORD1_SET3	B1 0x2A	0x8D
SyncWord pattern 2	SYNC_WORD2_SET0	B1 0x2B	-
	SYNC_WORD2_SET1	B1 0x2C	-
	SYNC_WORD2_SET2	B1 0x2D	-
	SYNC_WORD2_SET3	B1 0x2E	-
Postamble setting	POSTAMBLE_SET	B0 0x44	0x00
Demodulator DC level	IFF_ADJ_H	B0 0x5E	0x00
	IFF_ADJ_L	B0 0x5F	0x00
Demodulator adjustment 1	DEMOD_SET1	B1 0x57	T.B.D.
Demodulator adjustment 2	DEMOD_SET2	B1 0x58	T.B.D.
Demodulator adjustment 3	DEMOD_SET3	B1 0x59	T.B.D.
Demodulator adjustment 4	DEMOD_SET4	B1 0x5A	T.B.D.
Demodulator adjustment 5	DEMOD_SET5	B1 0x5B	T.B.D.
Demodulator adjustment 6	DEMOD_SET6	B1 0x5C	T.B.D.
Demodulator adjustment 7	DEMOD_SET7	B1 0x5D	T.B.D.
Demodulator adjustment 8	DEMOD_SET8	B1 0x5E	T.B.D.
Demodulator adjustment 9	DEMOD_SET9	B1 0x5F	T.B.D.

●Mode F

Parameter	Register		Setting Value
	Name	Address	
TX frequency	TXFREQ_I	B1 0x1B	0x10
	TXFREQ_FH	B1 0x1C	0x0A
	TXFREQ_FM	B1 0x1D	0xF7
	TXFREQ_FL	B1 0x1E	0x55
RX frequency	RXFREQ_I	B1 0x1F	0x10
	RXFREQ_FH	B1 0x20	0x0A
	RXFREQ_FM	B1 0x21	0xF7
	RXFREQ_FL	B1 0x22	0x55
Channel space	CH_SPACE_H	B1 0x23	-
	CH_SPACE_L	B1 0x24	-
PLL frequency division	PLL_DIV_SET	B1 0x1A	0x00
Data rate	DRATE_SET	B0 0x06	0x11
TX\RX data configulation	DATA_SET1	B0 0x07	0x00
	DATA_SET2	B0 0x08	0x00
Frequency deviation (GFSK)	GFSK_DEV_H	B1 0x30	-
	GFSK_DEV_L	B1 0x31	-
Frequency deviation (FSK)	FSK_DEV0_H/GFIL0	B1 0x32	0x00
	FSK_DEV0_L/GFIL1	B1 0x33	0x44
	FSK_DEV1_H/GFIL2	B1 0x34	0x00
	FSK_DEV1_L/GFIL3	B1 0x35	0x82
	FSK_DEV2_H/GFIL4	B1 0x36	0x00
	FSK_DEV2_L/GFIL5	B1 0x37	0xB3
	FSK_DEV3_H/GFIL6	B1 0x38	0x00
	FSK_DEV3_L	B1 0x39	0xD2
	FSK_DEV4_H	B1 0x3A	0x00
	FSK_DEV4_L	B1 0x3B	0xD0
Frequency deviation time	FSK_TIM_ADJ0	B1 0x3C	0x7F
	FSK_TIM_ADJ1	B1 0x3D	0x7F
	FSK_TIM_ADJ2	B1 0x3E	0x7F
	FSK_TIM_ADJ3	B1 0x3F	0x7F
	FSK_TIM_ADJ4	B1 0x40	0x7f
Preamble length	TXPR_LEN_H	B0 0x42	0x00
	TXPR_LEN_L	B0 0x43	0x27
SyncWord length	SYNC_WORD_LEN	B1 0x25	0x10
SyncWord pattern 1	SYNC_WORD1_SET0	B1 0x27	0x00
	SYNC_WORD1_SET1	B1 0x28	0x00
	SYNC_WORD1_SET2	B1 0x29	0xF6
	SYNC_WORD1_SET3	B1 0x2A	0x8D
SyncWord pattern 2	SYNC_WORD2_SET0	B1 0x2B	0x00
	SYNC_WORD2_SET1	B1 0x2C	0x00
	SYNC_WORD2_SET2	B1 0x2D	0xF6
	SYNC_WORD2_SET3	B1 0x2E	0x72
Postamble setting	POSTAMBLE_SET	B0 0x44	0x00

Mode F setting (continued)

Parameter	Register		Setting Value
	Name	Address	
Demodulator DC level	IFF_ADJ_H	B0 0x5E	0x00
	IFF_ADJ_L	B0 0x5F	0x00
Demodulator adjustment 1	DEMOD_SET1	B1 0x57	T.B.D.
Demodulator adjustment 2	DEMOD_SET2	B1 0x58	T.B.D.
Demodulator adjustment 3	DEMOD_SET3	B1 0x59	T.B.D.
Demodulator adjustment 4	DEMOD_SET4	B1 0x5A	T.B.D.
Demodulator adjustment 5	DEMOD_SET5	B1 0x5B	T.B.D.
Demodulator adjustment 6	DEMOD_SET6	B1 0x5C	T.B.D.
Demodulator adjustment 7	DEMOD_SET7	B1 0x5D	T.B.D.
Demodulator adjustment 8	DEMOD_SET8	B1 0x5E	T.B.D.
Demodulator adjustment 9	DEMOD_SET9	B1 0x5F	T.B.D.

■Flowcharts

Category	Condition 1	Condition 2	Name of flow
Turn on Sequence	-	-	(1) Initialization flow
TX/RX common Sequence	-	-	(1) RF state transition wait
TX Sequence	DIO mode	-	TX (1) DIO mode
	FIFO mode	Under 64 byte	TX (2) FIFO mode
		65 byte or more (FAST_TX)	TX (3) FIFO mode
	Automatic TX	-	TX (4) automatic TX
RX Sequence	DIO mode	-	RX (1) DIO mode
	FIFO mode	Under 64 byte	RX (2) FIFO mode
		65 byte or mode	RX (3) FIFO mode
	ACK transmission	-	RX (4) ACK transmission
	Field check	-	RX (5) Field checking
	CCA	Normal mode	RX (6) CCA normal mode
		Continuous execution mode	RX (6) CCA continuous execution mode
		IDLE detection mode	RX (6) CCA IDLE detection mode
	High speed carrier checking	-	RX (7) high speed carrier checking
	ED-SCAN	-	RX (8) ED-SCAN
SLEEP Sequence	SLEEP	-	(1) SLEEP
	Wake-up timer	-	(2) Wake-up timer
Error Process	Sync error	-	(1) Sync error
	TX FIFO access error	-	(2) TX FIFO access error
	RX FIFO access error	-	(3) RX FIFO access error
	PLL unlock	-	(4) PLL unlock
Data Rate Change Process	-	-	(1) Change Data Rate

●Turn on Sequence

(1) Initialization flow

In initialization status, interrupt process, registers setting, VCO calibration are necessary.

(1) Interrupt process

Upon reset, all interrupt notification settings ([INT_EN_GRP1-3: B0 0x10-0x12]) are disabled.
After hard reset is released, INT[0] (group 1: Clock stabilization completion interrupt) will be detected. INT[0] should be enabled by [INT_EN_GRP1:B0 0x10] register.

In use of ML7344JC, after hard reset is released, set 0b1 to XTAL_EN [CLK_SET2:B0 0x03(4)] at first.

(2) Registers setting

(ML7344JT)

After hard reset is released, all registers in BANK0 and BANK1 except FIFO access registers ([WR_TX_FIFO: B0 0x7C] and [RD_FIFO: B0 0x7F]), are accessible before INT[0] notification.

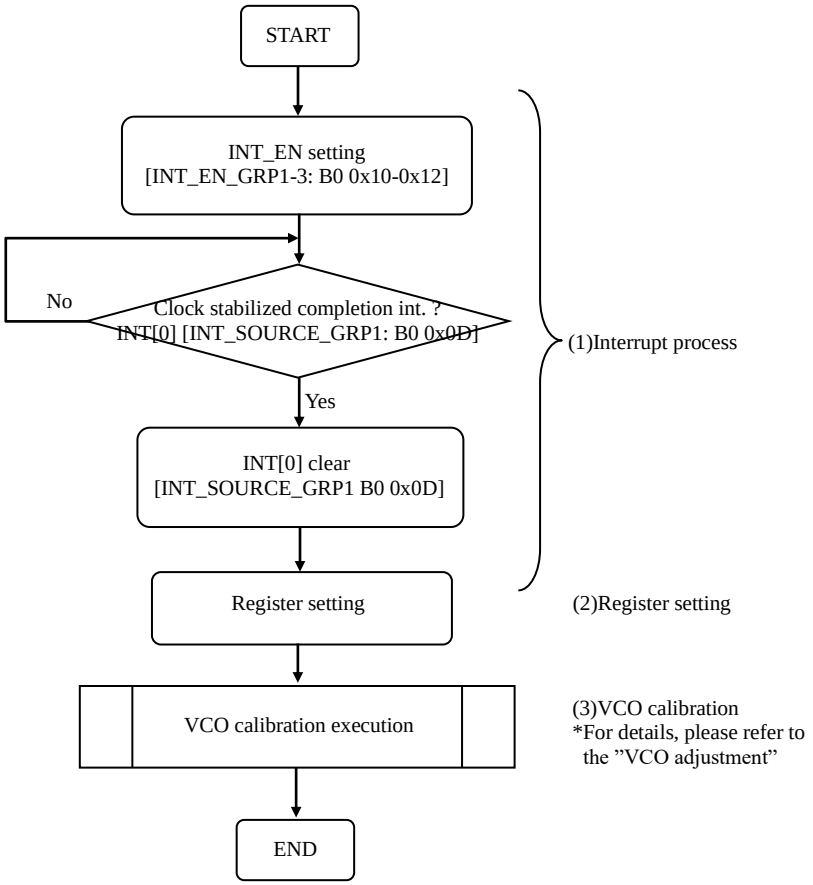
(ML7344JC/ML7344CC)

After hard reset is released, all register access and FIFO access (**) is prohibited until INT[0] occurrence.

(**) FIFO access: Accessing [WR_TX_FIFO: B0 0x7C] and [RD_FIFO: B0 0x7F] registers.

(3) VCO calibration

VCO calibration is executed after setting upper and low limit of the operation frequency.
For details, please refer to the “VCO adjustment”.



●TX/RX Common Sequence

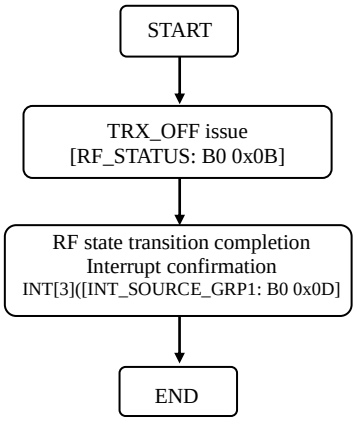
(1) RF state transition wait

If below setting for RF state change is selected, please confirm the completion of RF state transtion by INT[3] (group1: RF state transtion completion interrupt).

○RF state transition by [RF_STATUS: B0 0x0B] register
○RF state transition by [RF_STATUS_CTRL: B0 0x0A] resgister
●FAST_TX mode setting
●automatic TX setting
●RF state setting after TX completion
●RF state setting after RX completion
○RF state modification by wake-up timer setting

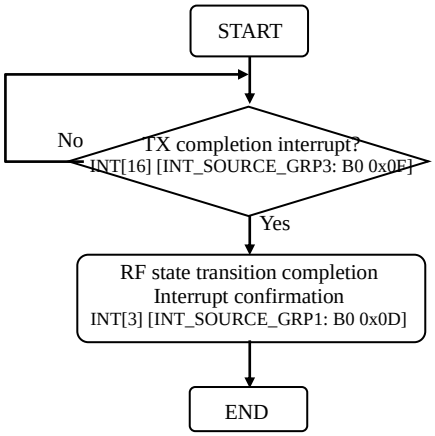
i) TRX_OFF flow
RF state change by [RF_STATUS: B0 0x0B]

SET_TRX[3:0]=0b1000

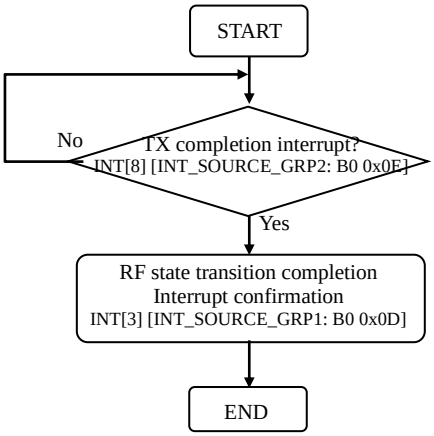


RF state change by [RF_STATUS_CTRL: B0 0x0A]

TXDONE_MODE[1:0=0b00

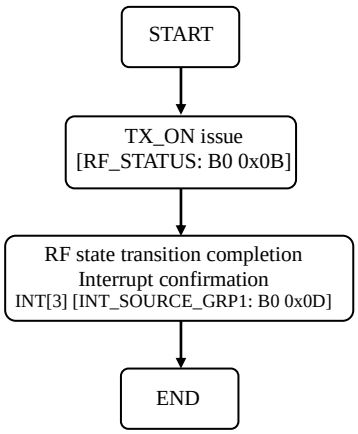


RXDONE_MODE[1:0]=0b00



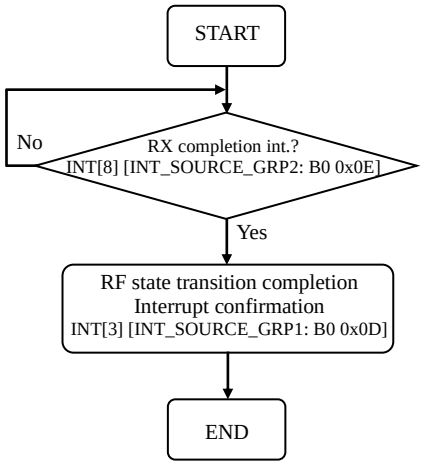
ii) TX_ON flow
RF state transition change by [RF_STATUS: B0 0x0B]

SET_TRX[3:0]=0b1001

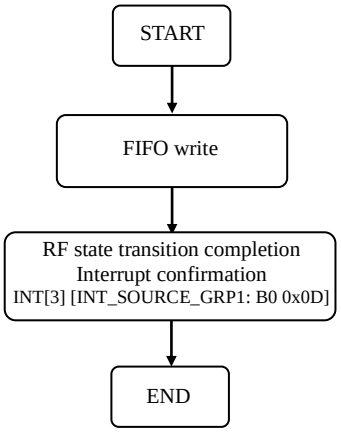


RF state transition by [RF_STATUS_CTRL]register(B0 0x0A)

RXDONE_MODE[1:0]=0b10



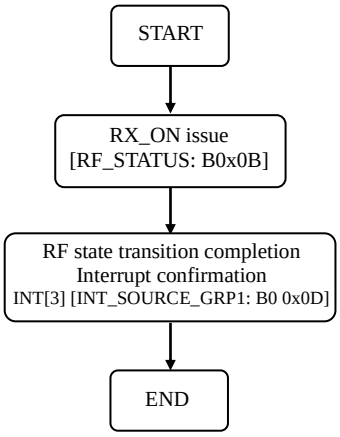
FAST_TX_EN=0b1 and
AUTO_TX_EN=0b1



iii) RX_ON flow

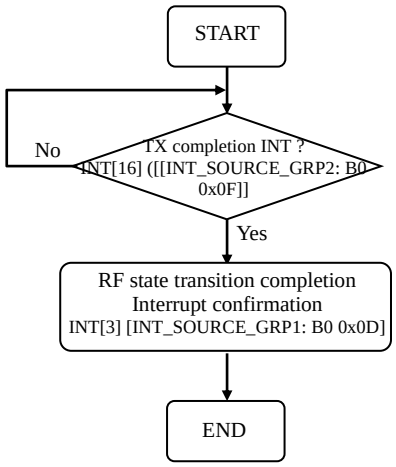
RF state change by [RF_STATUS: B0 0x0B]

SET_TRX[3:0]=0b0110



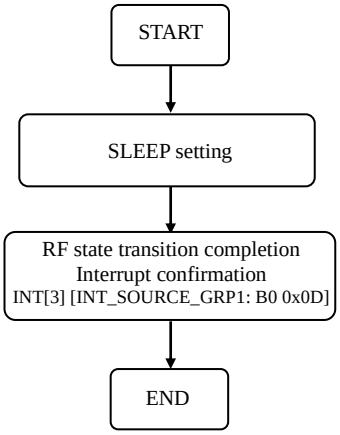
RF state change by [RF_STATUS_CTRL: B0 0x0A]

TXDONE_MODE[1:0]=0b10



iv) Wake-up flow

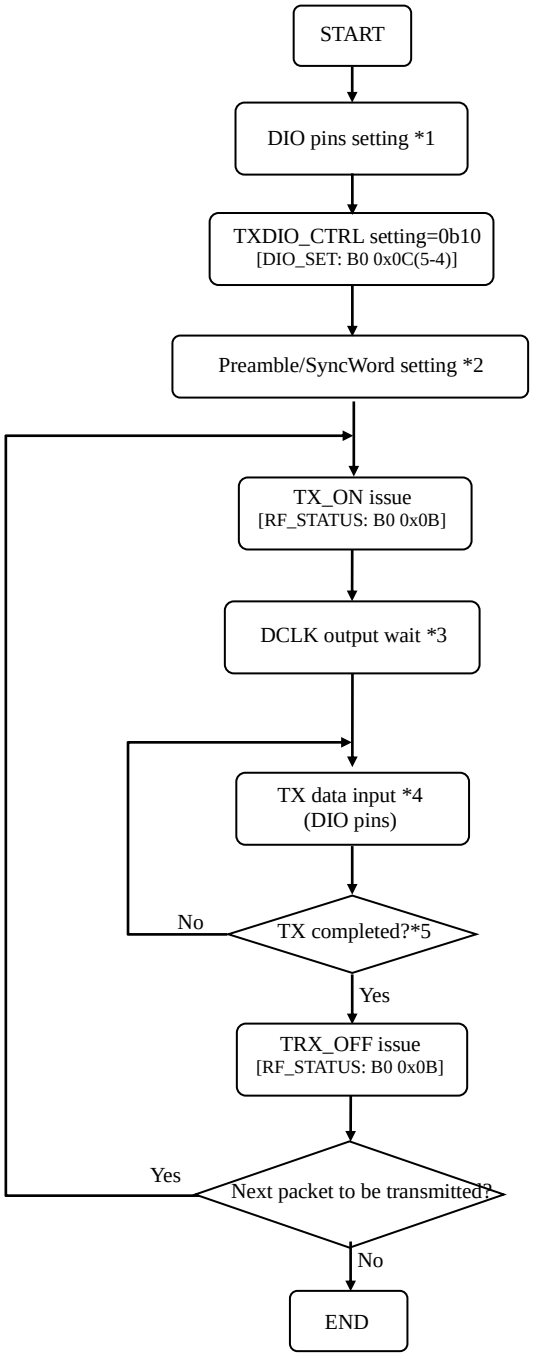
The following flow doses not apply to the case when waiting for INT[14] (group 1: Field checking interrupt) after wake-up.



●TX Sequence

(1) DIO mode

DIO(TX) mode can be selected by setting TXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(5-4)])=0b01 or 0b10. In DIO mode, when TX_ON is issued, data input on the pin related DIO will be transimitted to the air. After TX completion, TRX_OFF should be issued.



*1 DIO/DCLK pins are defined as follows:
[GPIO0_CTRL: B0 0x4E]
[GPIO1_CTRL: B0 0x4F]
[GPIO2_CTRL: B0 0x50]
[GPIO3_CTRL: B0 0x51]
[EXT_CLK_CTRL: B0 0x52]
[SPI/EXT_PA_CTRL: B0 0x53]

*2: preamble/SyncWord is transmitted based on the following registers.
Preamble [DATA_SET1: B0 0x07]
[TXPR_LEN_H/L: B0 0x42-43]
SyncWord [SYNCWORD1_SET0-3: B1 0x27-2A]
[SYNCWORD2_SET0-3: B1 0x2B-2E]
[SYNC_WORD_LEN: B1 0x25]
[DATA_SET2: B0 0x08]

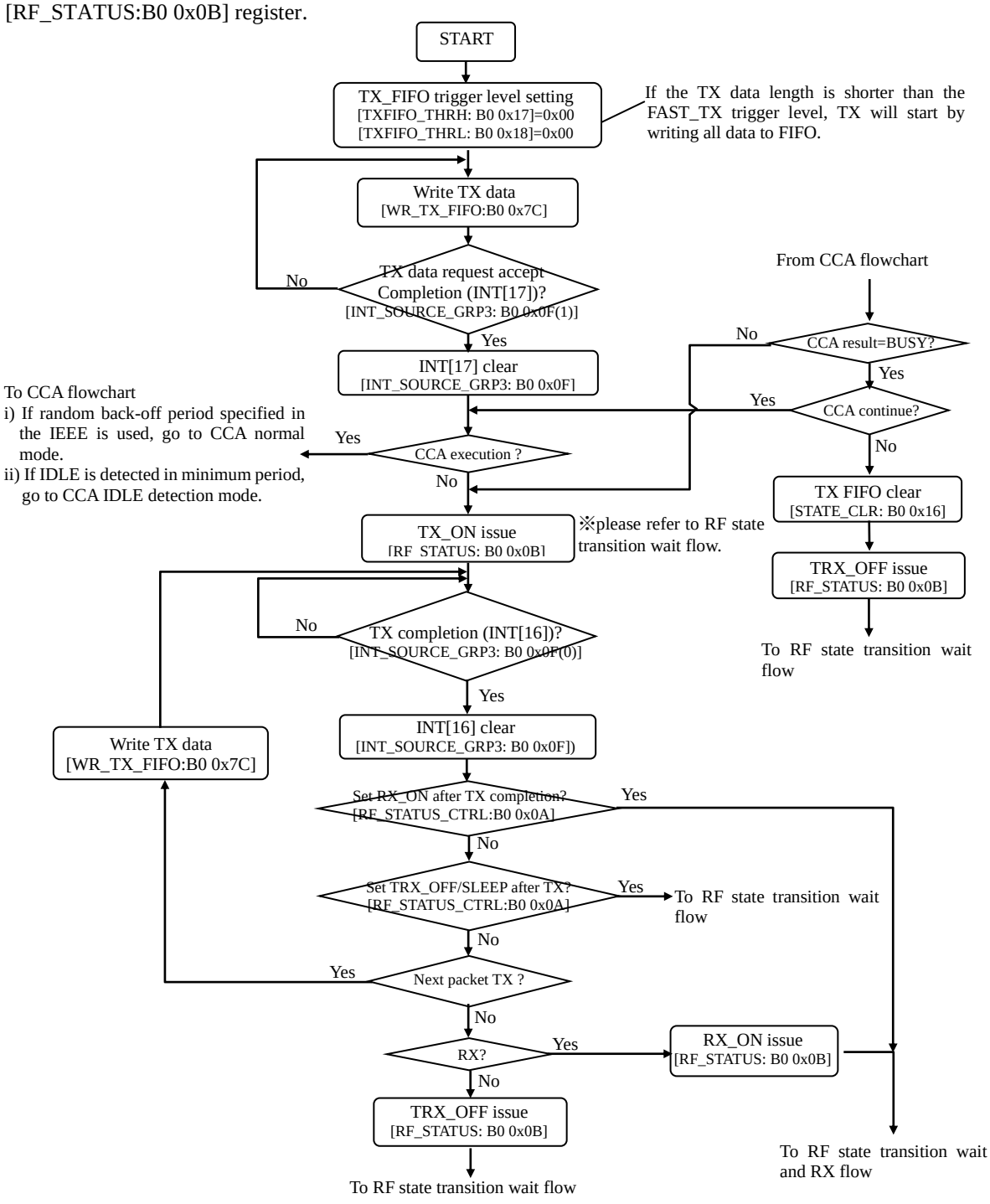
*3: Timing up to DCLK output varies depending on TX preamble, SFC, data rate.

*4: TX data must be input at falling edge of DCLK.

*5: Please refer to RF state transition wait flow.

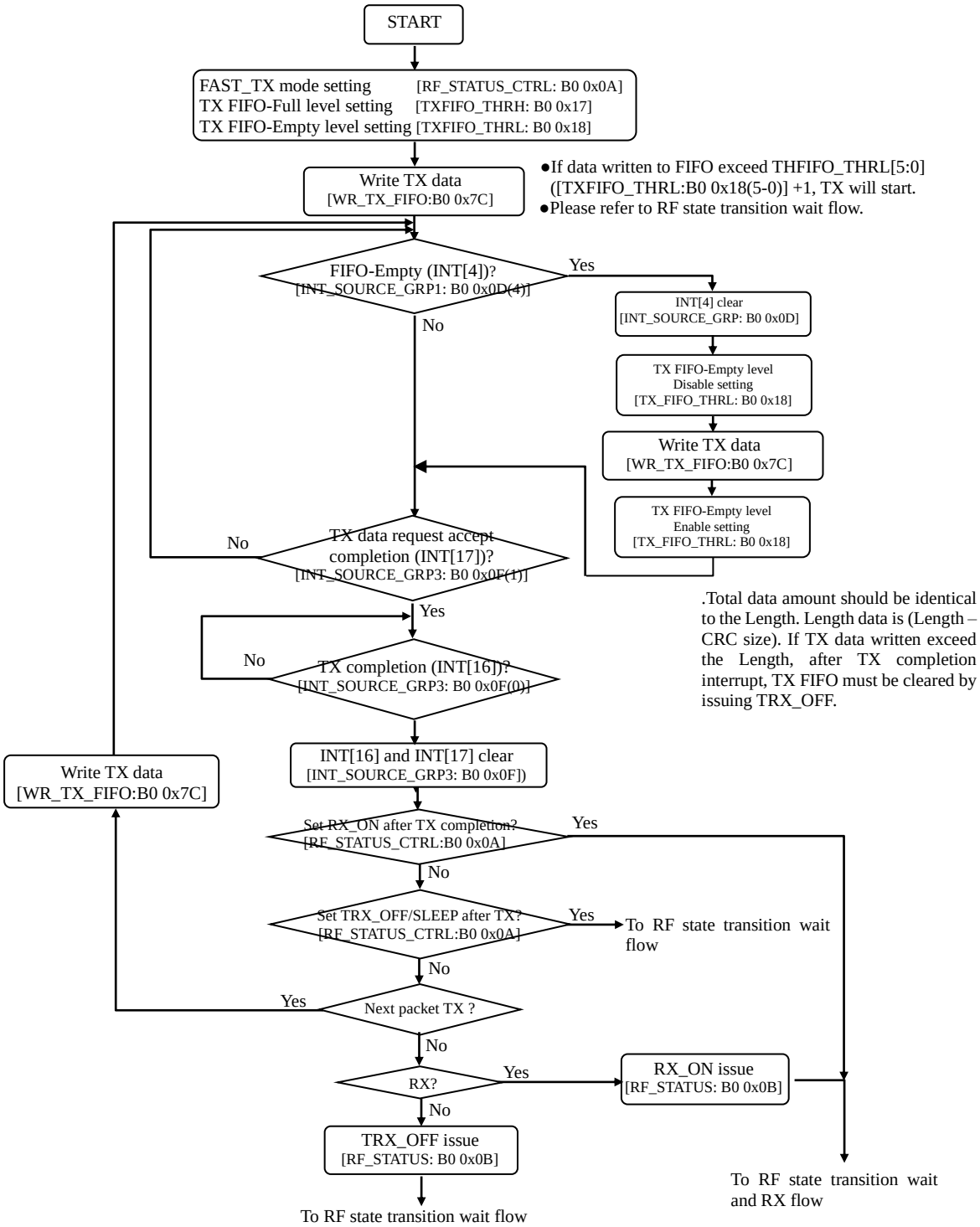
(2) FIFO mode (less than 64 byte)

FIFO mode (packet mode) can be selected by setting TXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(5-4)])=0b00. In FIFO mode, data is written to the TX_FIFO by [WR_TX_FIFO:B0 0x7C] register. After writing full data of a packet, issuing TX_ON by [RF_STATUS:B0 0x0B] resister. Following preamble/SyncWord, TX_FIFO data is transmitted to the air. Upon TX completion interrupt (INT[16] group 3) occurs, interrupt must be cleared. If the next TX packet is sent, the next TX packet data is written to the TX_FIFO. If RX is expected after TX, RX_ON should be issued by [RF_STATUS: B0 0x0B] resister. TX can be terminated by issuing TRX_OFF by [RF_STATUS:B0 0x0B] register.



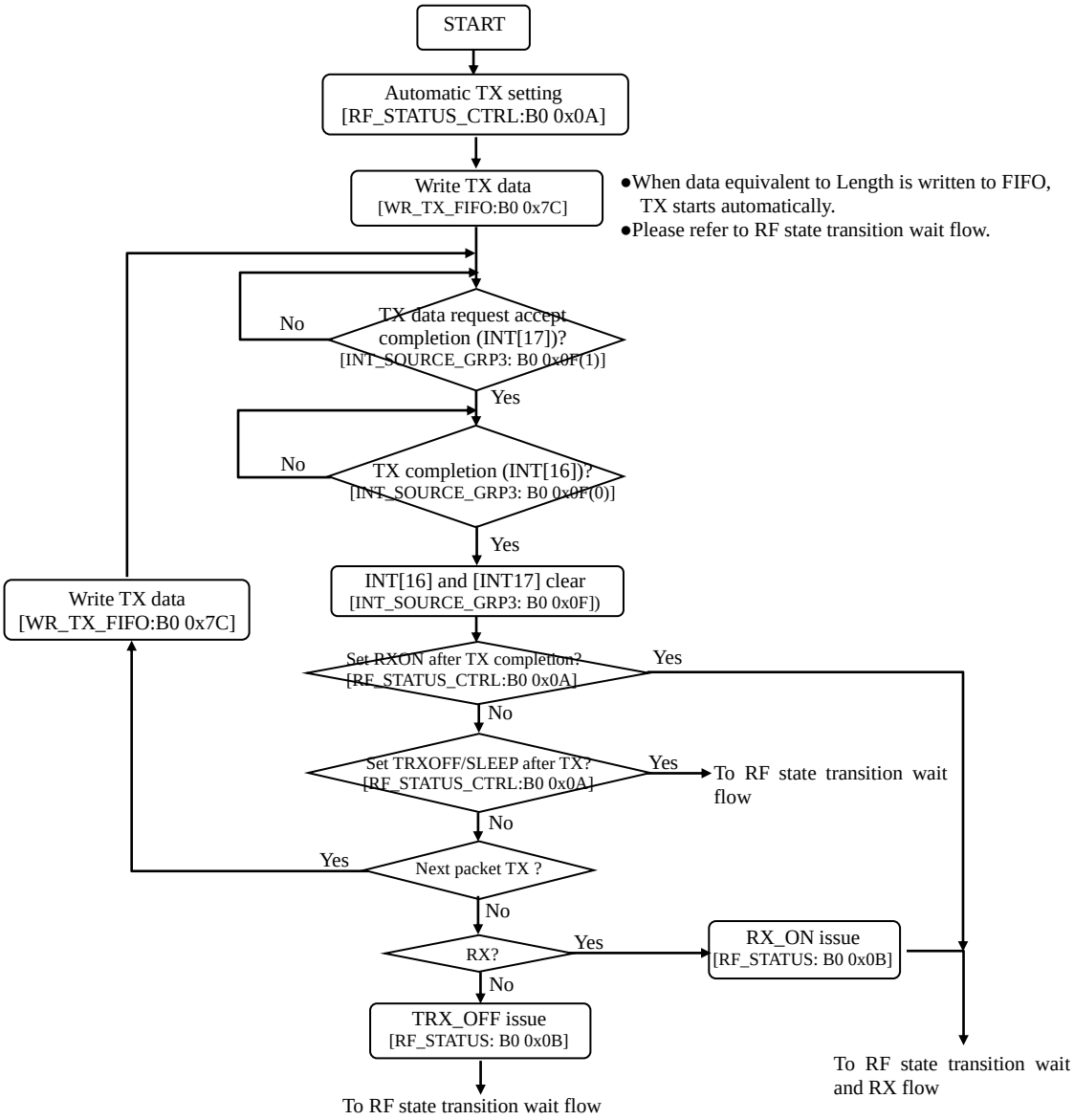
(3) FIFO mode (65 byte or more)

The Host must write TX data to the TX_FIFO while checking INT[5] (group1: FIFO-Full interrupt) and INT[4] (group1: FIFO-Empty interrupt) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operations are identical to the FIFO mode (less than 64byte). Enabling FAST_TX mode by FAST_TX_EN ([RF_STATUS_CTRL: B0 0x0A(5)] =0b1, TX will start when data amount written to the FIFO exceeds the bytes+1 in the [TXFIFO_THRL: B0 0x18].



(4) Automatic TX (less than 64 byte)

If AUTO_TX_EN([RF_STATUS_CTRL: B0 0x0A(4)]=0b1, TX starts automatically when FIFO is filled with data equivalent to the Langth. Afer TX completion, RFstate transition setting is by TXDONE_MODE ([RF_STATUS_CTRL: B0 0x0A(1-0)]).



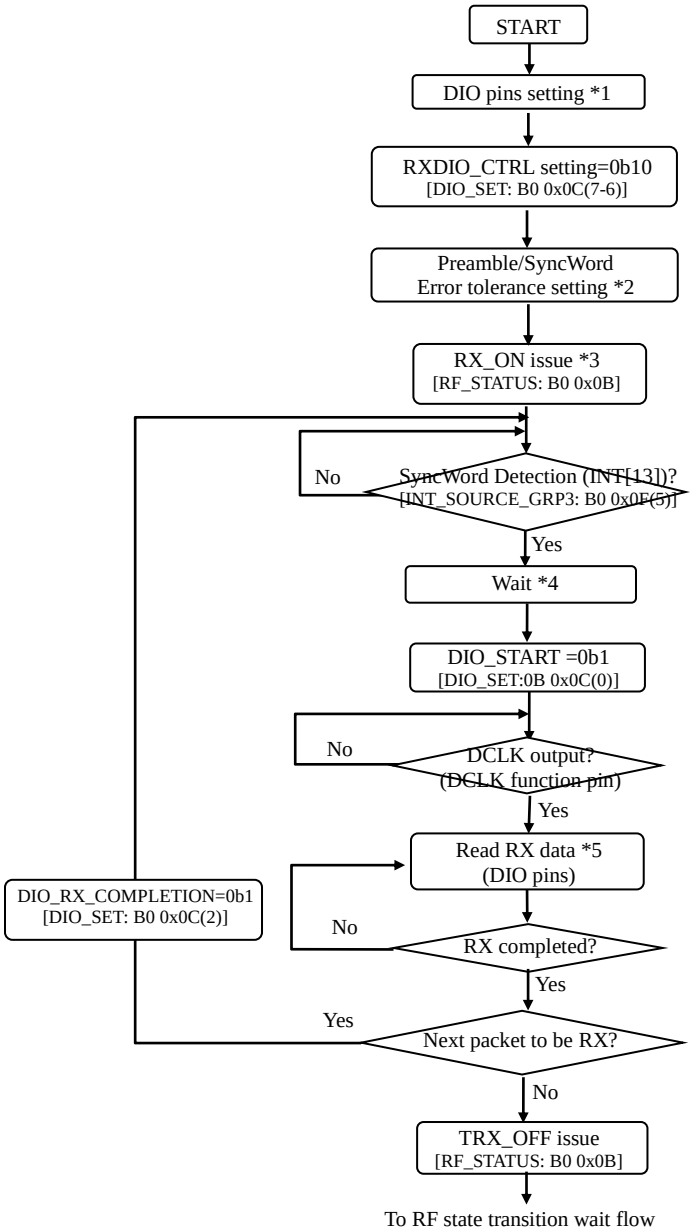
●RX Sequence

(1) DIO mode

DIO mode can be selected by setting RXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(7-6)])=0b10/0b11. Upon setting DIO mode and issuing RX_ON by [RF_STATUS:B0 0x0B] register, SyncWord detection will be started.

○DIO output mode 1 operation

When RXDIO_CTRL[1:0]=0b10 setting, after SyncWord pattern detection, RX data will be strored into the RX_FIFO. RX data stored in the RX_FIFO is output through DIO pins, if setting DIO_START ([DIO_SET: B0 0x0C(0)])=0b1. After RX completion, if more data is to be received, by setting DIO_RX_COMPLETE ([DIO_SET: B0 0x0C(2)]) =0b1 (DIO RX Completion), the next packet will be ready to receive. In case of TRX_OFF, issuing TRX_OFF by [RF_STATUS:B0 0x0B] register.



*1 DIO/DCLK pins are defined as follows:
[GPIO0_CTRL: B0 0x4E]
[GPIO1_CTRL: B0 0x4F]
[GPIO2_CTRL: B0 0x50]
[GPIO3_CTRL: B0 0x51]
[EXT_CLK_CTRL: B0 0x52]
[SPI/EXT_PA_CTRL: B0 0x53]

*2: Preamble, SyncWord and Error tolerance are set by following registers.
Preamble [DATA_SET1: B0 0x07]
[SYNC_CONDITION1-3: B0 0x45-47]
SyncWord [SYNCWORD1_SET0-3: B1 0x27-2A]
[SYNCWORD2_SET0-3: B1 0x2B-2E]
[SYNC_WORD_LEN: B1 0x25]
[DATA_SET2: B0 0x08]

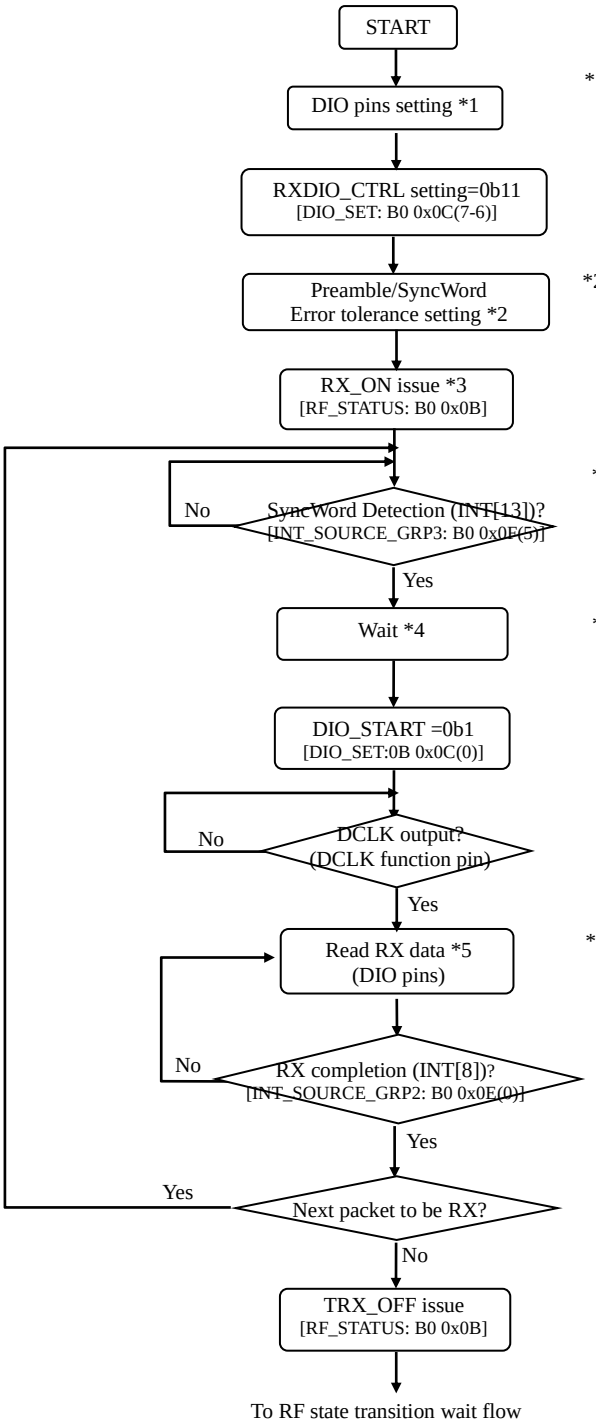
*3: Please refer to RF state transition wait flow

*4 Wait time should be more than 1 byte data receiving period

*5 RX data must be transferred to the HOST at rising edge of DCLK.

○DIO output mode 2 operation

While RXDIO_CTRL[1:0]=0b11, RX data (after L-field) will be stored into the RX_FIFO. RX data stored in the RX_FIFO is output through DIO pins, if setting DIO_START ([DIO_SET: B0 0x0C(0)])=0b1. Upon outputting RX data defined by L-field, RX is completed and generate RF completion interrupt (INT[8] group2). In case of TRX_OFF, issuing TRX_OFF by [RF_STATUS:B0 0x0B] register.



*1 DIO/DCLK pins are defined as follows:
[GPIO0_CTRL: B0 0x4E]
[GPIO1_CTRL: B0 0x4F]
[GPIO2_CTRL: B0 0x50]
[GPIO3_CTRL: B0 0x51]
[EXT_CLK_CTRL: B0 0x52]
[SPI/EXT_PA_CTRL: B0 0x53]

*2: Preamble, SyncWord and Error tolerance are set by following registers.
Preamble [DATA_SET1: B0 0x07]
[SYNC_CONDITION1-3: B0 0x45-47]
SyncWord [SYNCWORD1_SET0-3: B1 0x27-2A]
[SYNCWORD2_SET0-3: B1 0x2B-2E]
[SYNC_WORD_LEN: B1 0x25]
[DATA_SET2: B0 0x08]

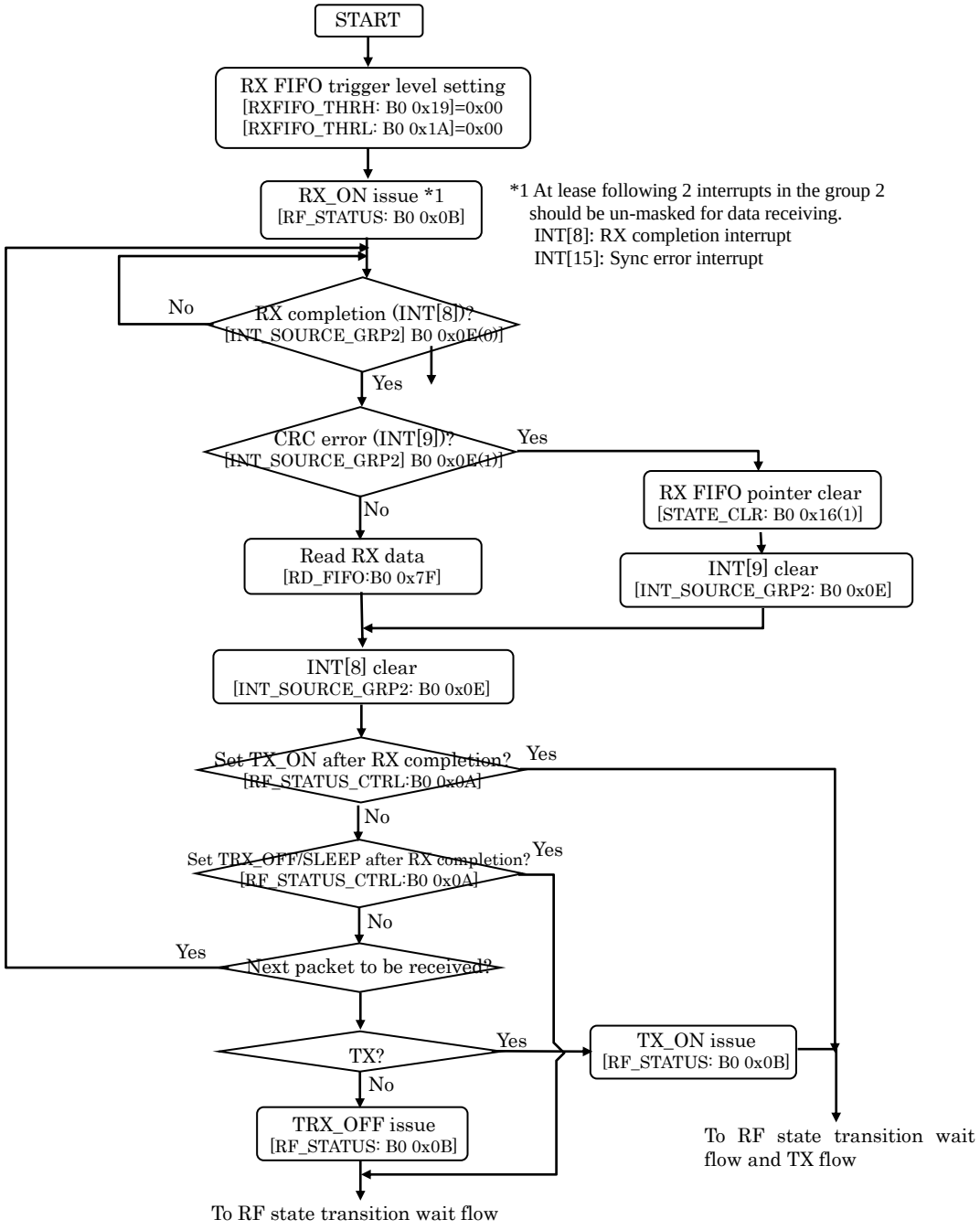
*3: Please refer to RF state transition wait flow

*4 Wait time should be more than Length field + 1 byte data receiving period.
1 byte data is decoded 8 bit data. If using Manchester code, 1 byte period becomes 160µs (@ 100kbps).

*5 RX data must be transferred to the HOST at rising edge of DCLK.

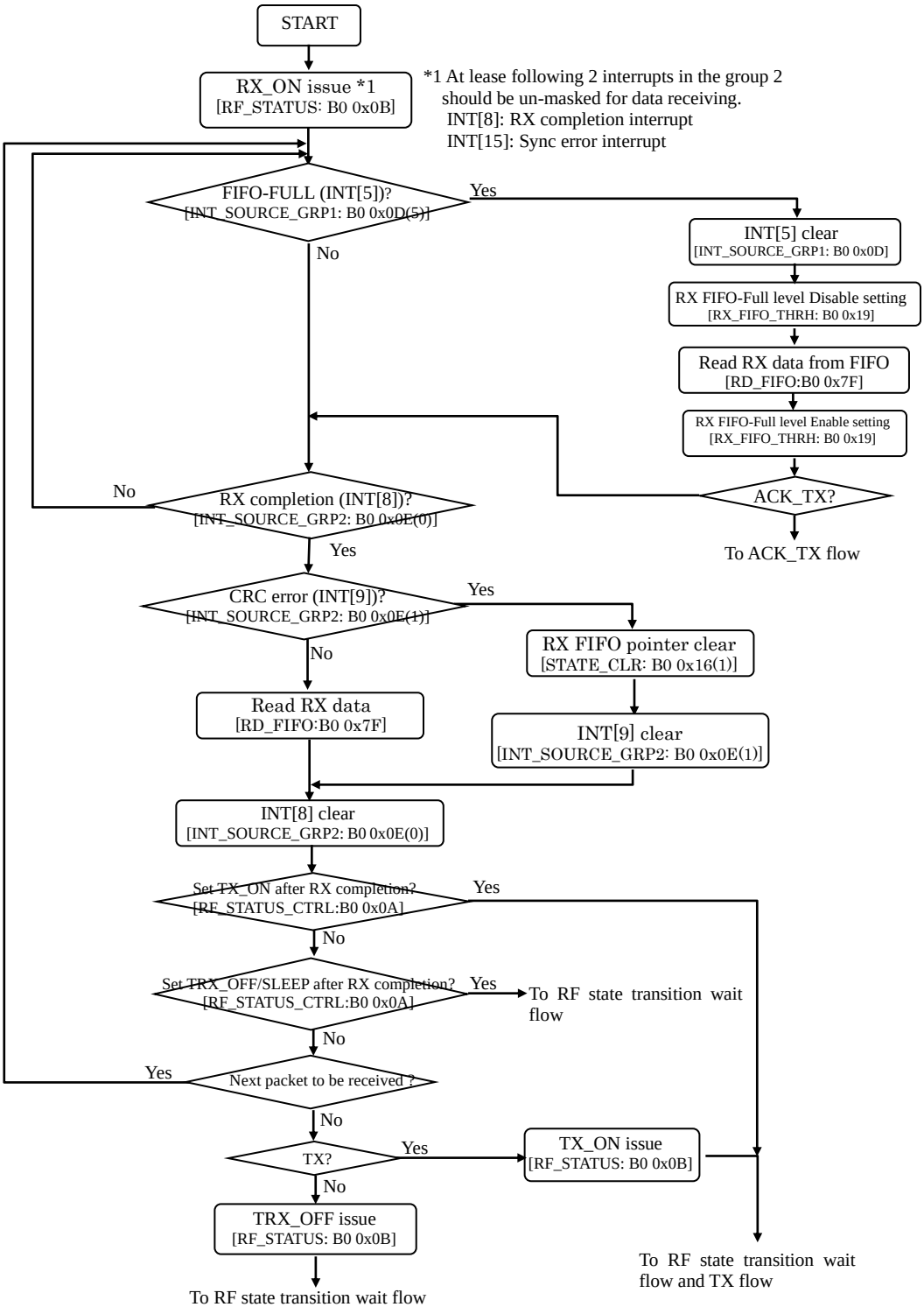
(2) FIFO mode (less than 64 byte)

FIFO mode can be selected by RXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(7-6)])=0b00. After SyncWord detection, RX data will be stored into the RX_FIFO. Upon Data RX completion interrupt (INT[8] group2) occurs, the host will read RX data from [RD_FIFO:B0 0x7F] registers. If CRC errors interrupt (INT[9] group2) is generated, the next packet can be ready to receive without reading all current RX data by setting STATE_CLR1 [STATE_CLR: B0 0x16(1)](RX FIFO pointer clear). If FIFO-Full trigger and FIFO-Empty trigger are not used, please set 0b0 to both RXFIFO_THRH_EN([RXFIFO_THRH: B0 0x19(7)]) and RXFIFO_THRL_EN([RXFIFO_THRH: B0 0x1A(7)]) .



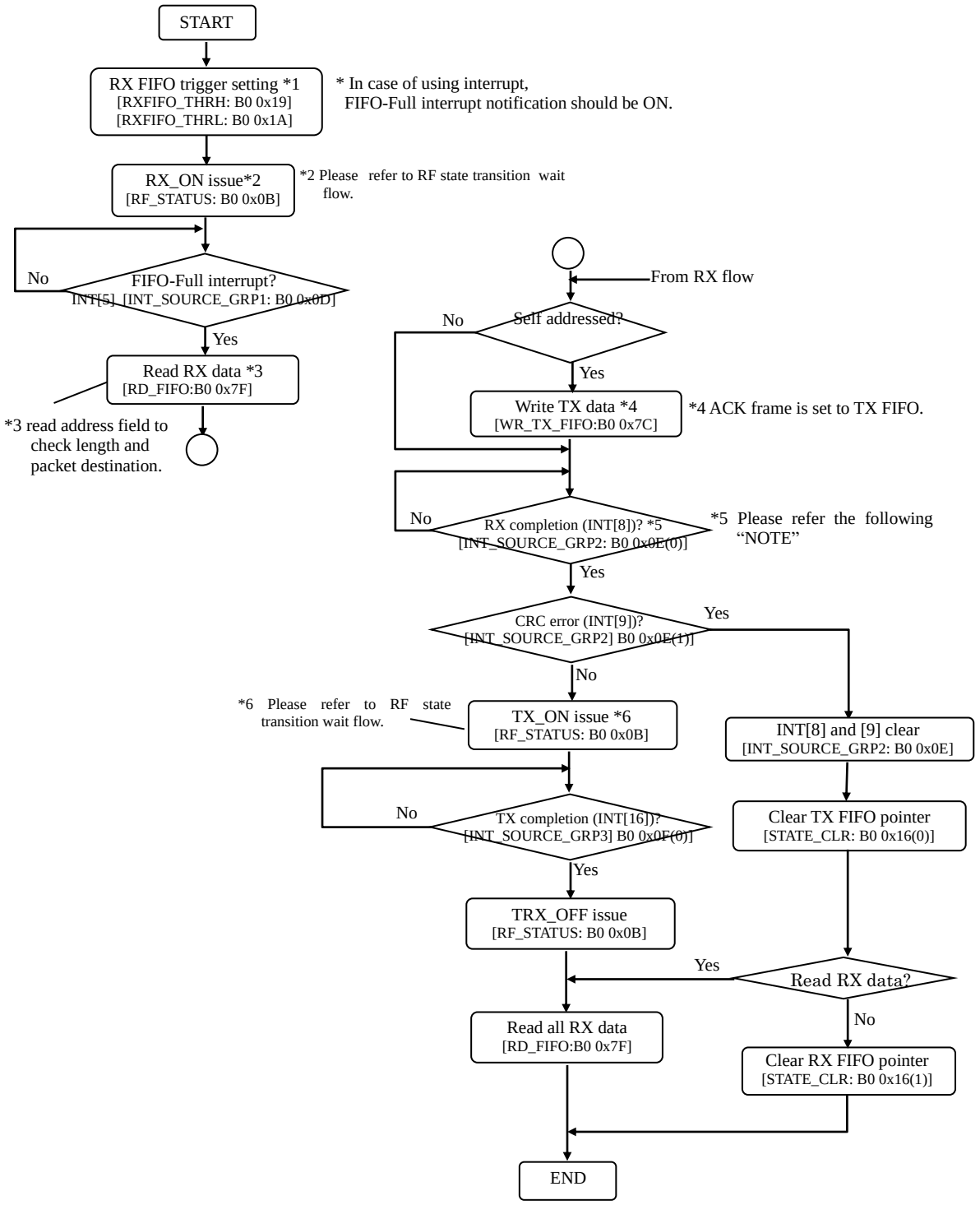
(3) FIFO mode (65 byte or more)

The Host must read RX data from the RX_FIFO while checking INT[5] (group1: FIFO-Full interrupt) and INT[4] (group1: FIFO-Empty interrupt) in order to avoid FIFO-Overrun or FIFO-Underrun. Other operations are identical to the FIFO mode (less than 64byte).



(4) ACK transmission

ACK TX flow is as follows. During RX, ACK frame can be set in the TX FIFO.



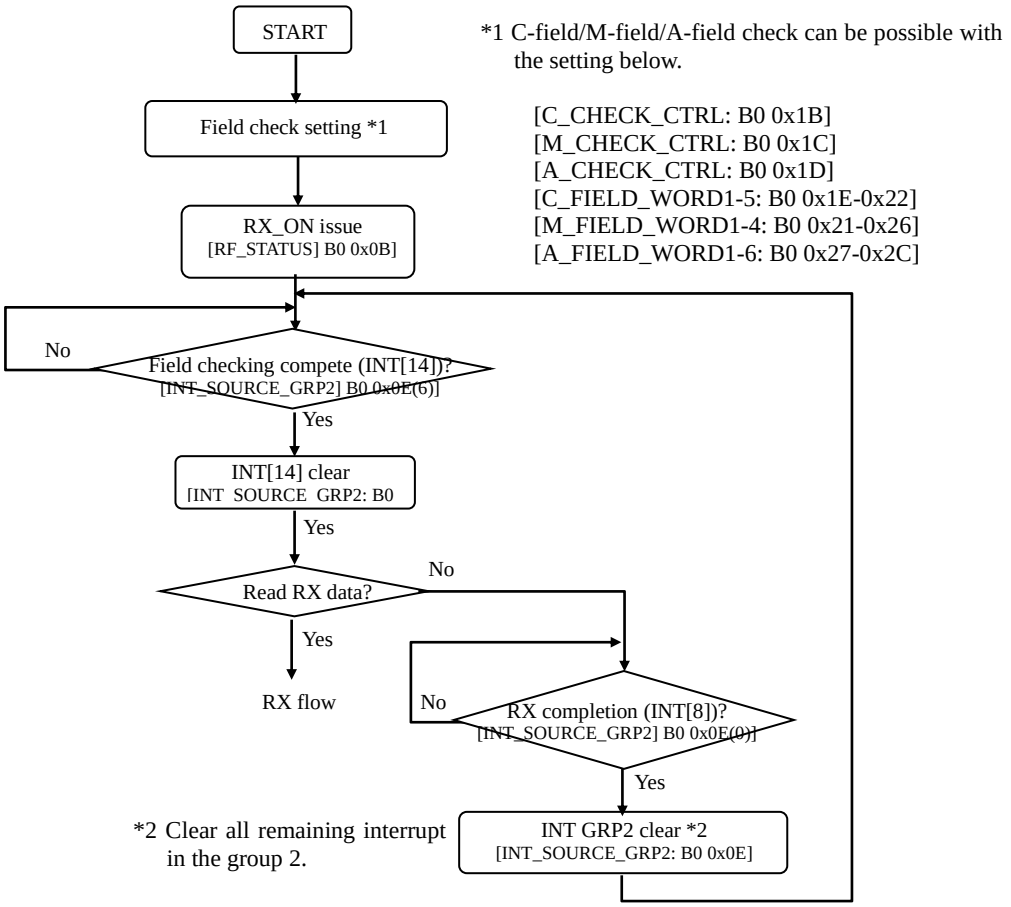
NOTE:

If setting “FAST_TX_EB=0b1” or “AUTO_TX_EN=0b1 or “RXDONE_MODE[1:0]=0b01 (move to TX state)” at the [RF_STATUS:CTRL:B0 0x0A] register, moving to TX_ON state automatically after RX completion in above flowchart.

Even if CRC error occurs, moving to TX_ON state. Since CRC errors interrupt (INT[9] group2) and RX completion interrupt (INT[8] group2) occur almost same timeing, Therefore in case of CRC error interrupt occurs, Force_TRX_OFF should be issued by [RF_STATUS:B0 0x0B] register withing the transition time from RX state to TX state(1.188msec), and clear TX FIFO pointer by [STATE_CLR:B0 0x16] register. When it is hard to issue Force_TRX_OFF during the trasition time due to MCU performance, “FAST_TX”, “AUTO_TX” and “move to TX state after RX completion” should be disabled. (In “FAST_TX”, trnasmitting conditoin depends on [TXFIFO_THRL:B0 0x18] register.)

(5) Field check transmission

After enabling Filedcheck functions, issuing RX_ON by [RF_STATUS:B0 0x0B] register. According to the setting of CA_INT_CTRL([C_CHECK_CTRL:B0 0x1B(6)]), filed checking result (match or no match) can be notified by the INT[14](group2: Field checking interrupt). Numbers of unmatched packets can be counted and stored into [ADDR_CHK_CTR_H/L: B1 0x62/0x63]) registers. This counter can be cleared by STATE_CLR4 [STATE_CLR: B0 0x16(4)](Address check counter clear).

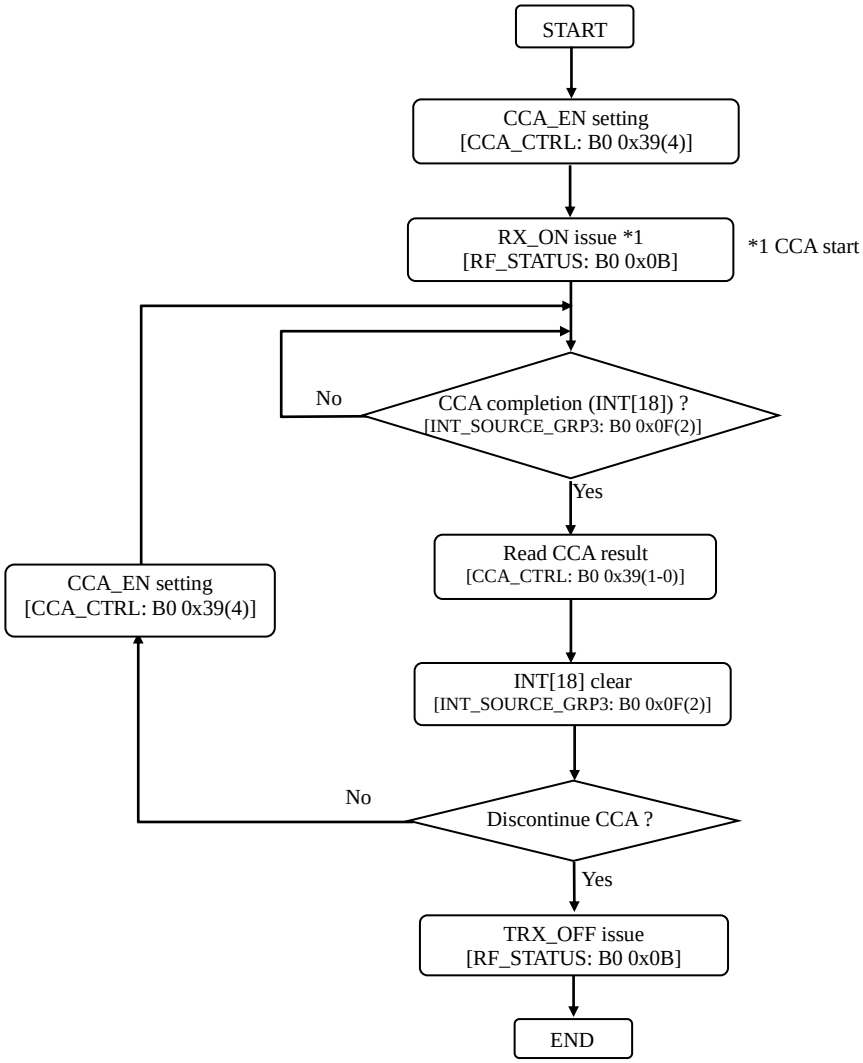


(6) CCA

○Normal mode

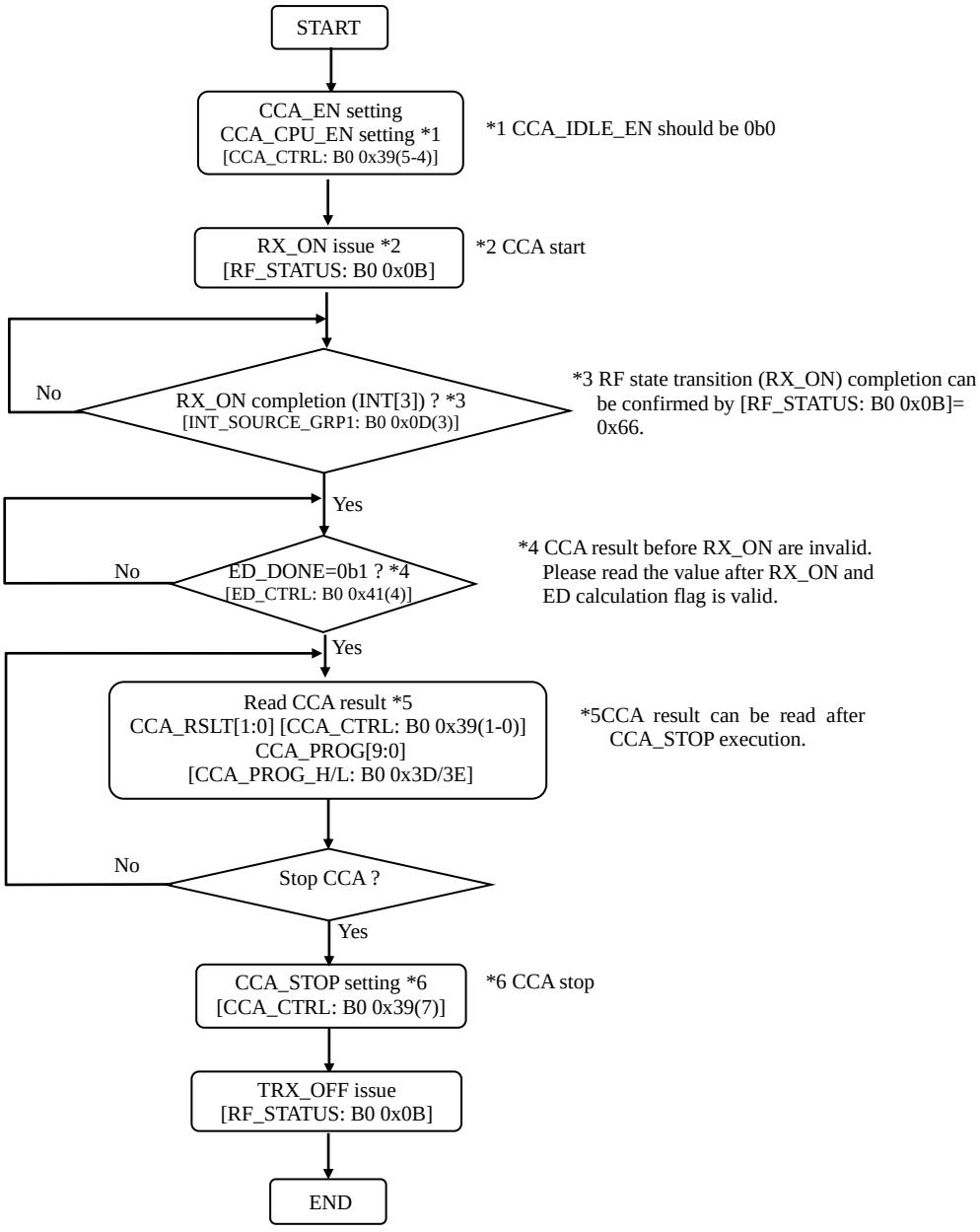
After setting CCA_EN([CCA_CTRL: B0 0x39(4)])=0b1, issuing RX_ON by [RF_STATUS:B0 0x0B] register. Comparing aquired ED average value with CCA threshold value in [CCA_LVL: B0 0x37] register and noitce the result. After CCA execution, CCA_EN([CCA_CTRL: B0 0x39(4)]) is disabled and RF maintains RX_ON state.

Even if set CCA_EN=0b1 in the RX_ON state, CCA execution is possible.



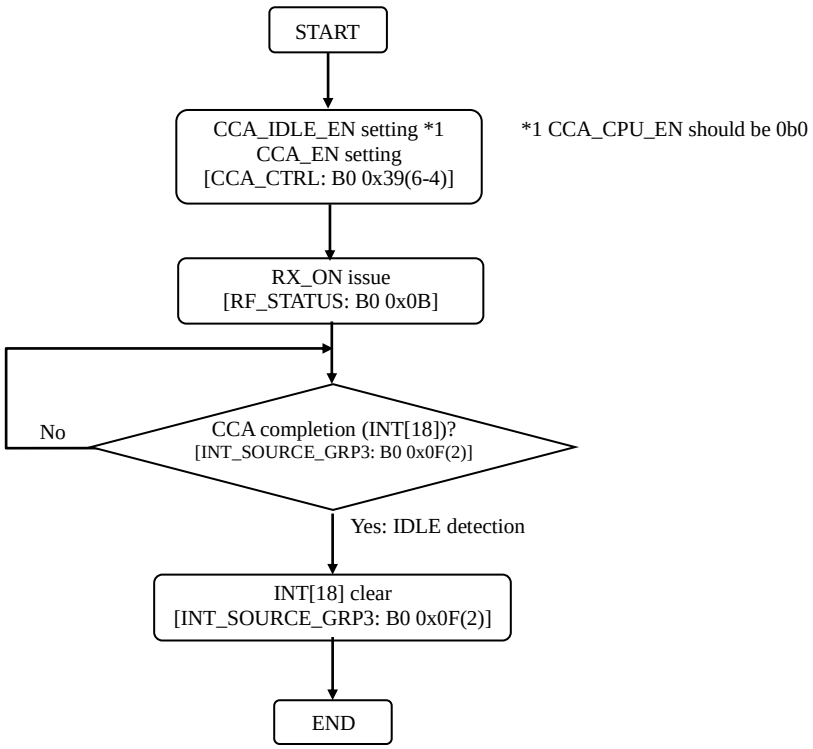
○Continuous mode

Continuous CCA mode is executed by issuing RX_ON by [RF_STATU:B0 0x0B] register after setting CCA_EN([CCA_CTRL: B0 0x39(4)])=0b1 and CCA_CPU_EN([CCA_CTRL: B0 0x39(5)])=0b1. In this mode, CCA continues until CCA_STOP([CCA_CTRL: B0 0x39(7)])=0b1 is set. CCA completion interupt (INT[18]: group3) is not generated. During CCA execution, CCA_RSLT([CCA_CTRL: B0 0x39(1-0)]), [CCA_PROG_L: B0 0x3E], [CCA_PROG_H: B0 0x3D] are constantly updated. The value will be kept by setting CCA_STOP([CCA_CTRL: B0 0x39(7)])=0b1.



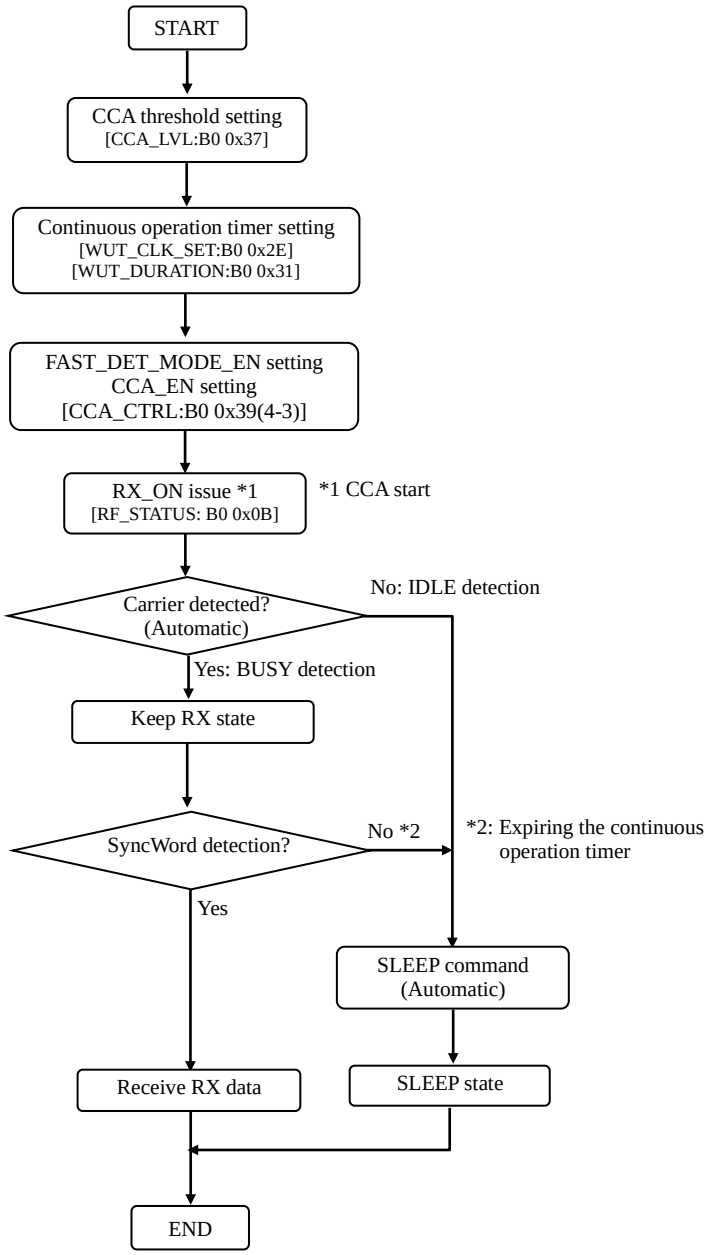
○IDLE detection mode

CCA is continuously executed untill IDLE is detected. CCA (IDLE detection mode) will be executing by . issuing RX_ON by [RF_STATU:B0 0x0B] register after setting CCA_EN([CCA_CTRL: B0 0x39(4)])=0b1, CCA_IDLE_EN ([CCA_CTRL: B0 0x39(6)])=0b1.



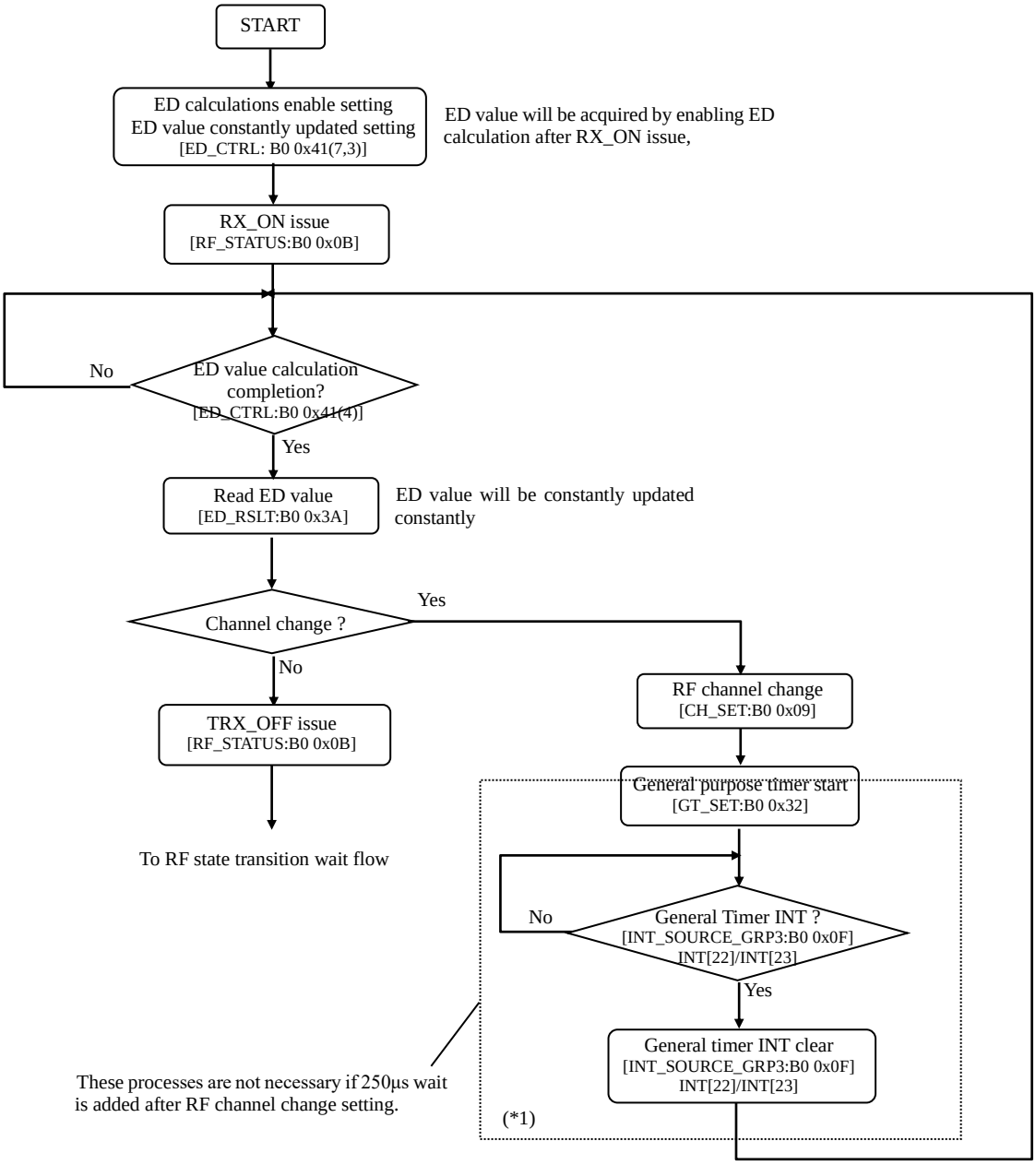
(7) High speed carrier checking mode

This mode is used for deciding whether continuing RX state or stoping RX state during RX state, based on RSSI level and SyncWord detection time. The value set in the [CCA_LVL:B0 0x37] register is used for RSSI level decision, continuous operation timer is used for SyncWord detection time decision. After decision, operation will automaticall switch to – either SLEEP state or RX state.



(8) ED scan

ED value will be automatically acquired by issuing RX_ON by [RF_STATU:B0 0x0B] register after setting ED_CALC_EN ([ED_CTRL: B0 0x41(7)])=0b1. ED value is constanty updated when ED_RSLT_SET ([ED_CTRL:B0 0x41(3)])=0b0.



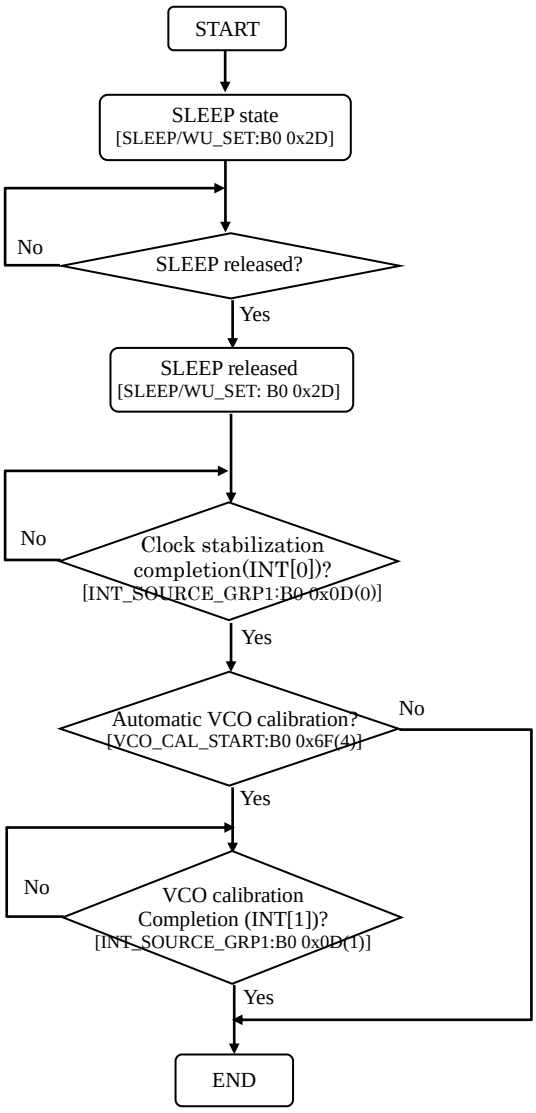
(*1) general purpose timer setting example
If 250µs wait is programmed using general purpose timer 1,
The following registers can be used.

[GT_CLK_SET:B0 0x33]	0x01(128 division)
[GT_INTERVAL1:B0 0x34]	0x04(timer setting)
[GT_SET:B0 0x32]	0x03(2MHz clock, timer start)

●SLEEP Sequence

(1) SLEEP

SLEEP can be executed by setting SLEEP_EN([SLEEP/WU_SET:B0 0x2D(0)])=0b1. SLEEP can be released by setting SLEEP_EN=0b0. If VCO calibration automatic execution setting AUTO_VCOCAL_EN ([VCO_CAL_START:B0 0x6F (4)])=0b1, VCO calibration is performed after clock stabilization completion interrupt (INT[0] group1) from SLEEP release.



(2) Wake-up timer

By setting the following registers, after SLEEP, automatically wake-up to RX_ON state.

If SyncWord is detected before continuous operation timer-up, RX_ON will be continued to receive a packet. After receiving RX completion interrupt(INT[8]: group2), by reading INT group2, MCU can determine read RX data or not. In order to re-enter SLEEP state, executing SLEEP command after clearing all interrupts in INT group2. If generating Sync error interrupt(INT[15]: group2), executing SLEEP command after clearing RX_FIFO and INT group2.

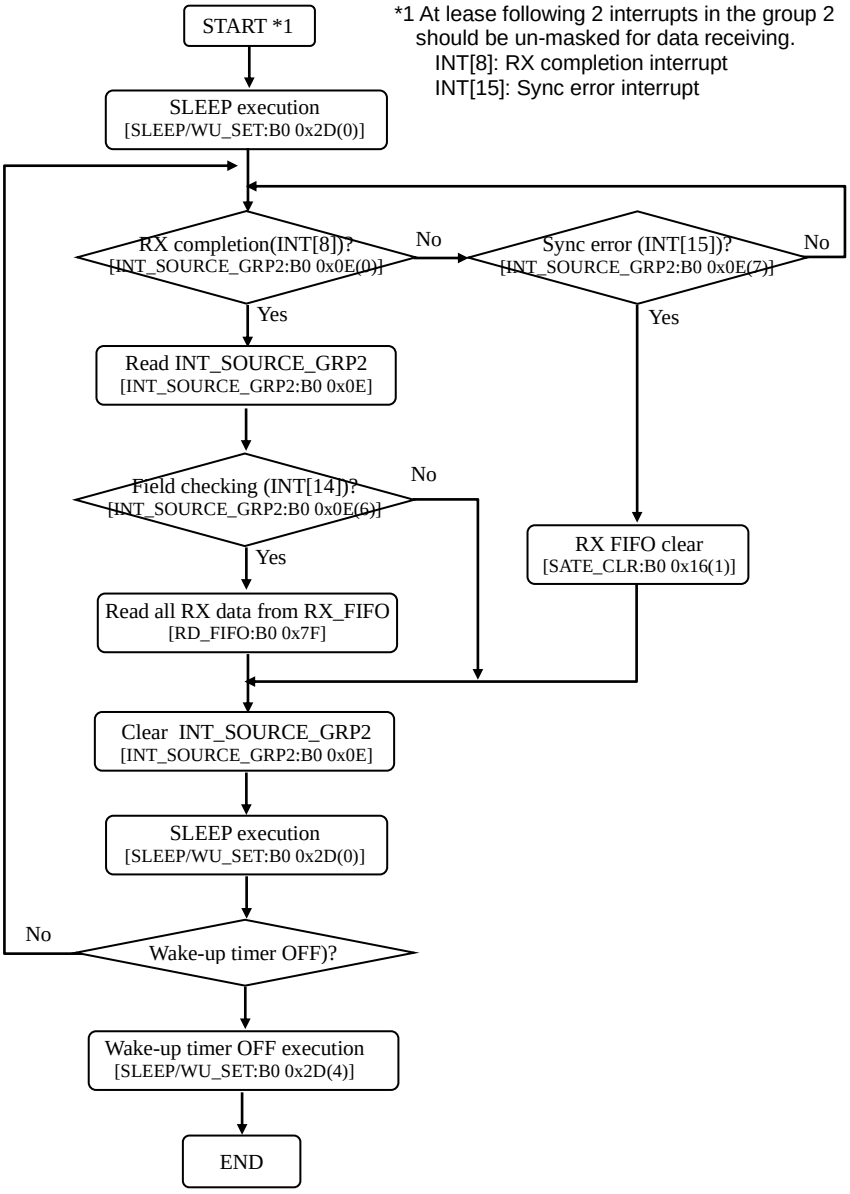
If SyncWord cannot be detected, automatically go back to SLEEP state after continuous operation timer-up.

[Wake-up timer setting]

WAKEUP_EN([SLEEP_SET:B0 0x2D(4)]) =0b1
RX_DURATION_EN([SLEEP_SET:B0 0x2D(5)])=0b1
WAKEUP_MODE([SLEEP_SET:B0 0x2D(6)])=0b0
[WUT_CLK_SET:B0 0x2E]
[WUT_INTERVAL_H:B0 0x2F]
[WUT_INTERVAL_L:B0 0x30]
[RX_DURATION:B0 0x31]

[Field check function setting]

[C_CHECK_CTR:B0 0x1B]
[M_CHECK_CTRL:B0 0x1C]
[A_CHECK_CTRL:B0 0x1D]
[C_FIELD_WORD1:B0 0x1E] to
[C_FIELD_WORD5:B0 0x22]
[M_FIELD_WORD1:B0 0x23] to
[M_FIELD_WORD4:B0 0x26]
[A_FIELD_WORD1:B0 0x27] to
[A_FIELD_WORD6:B0 0x2C]

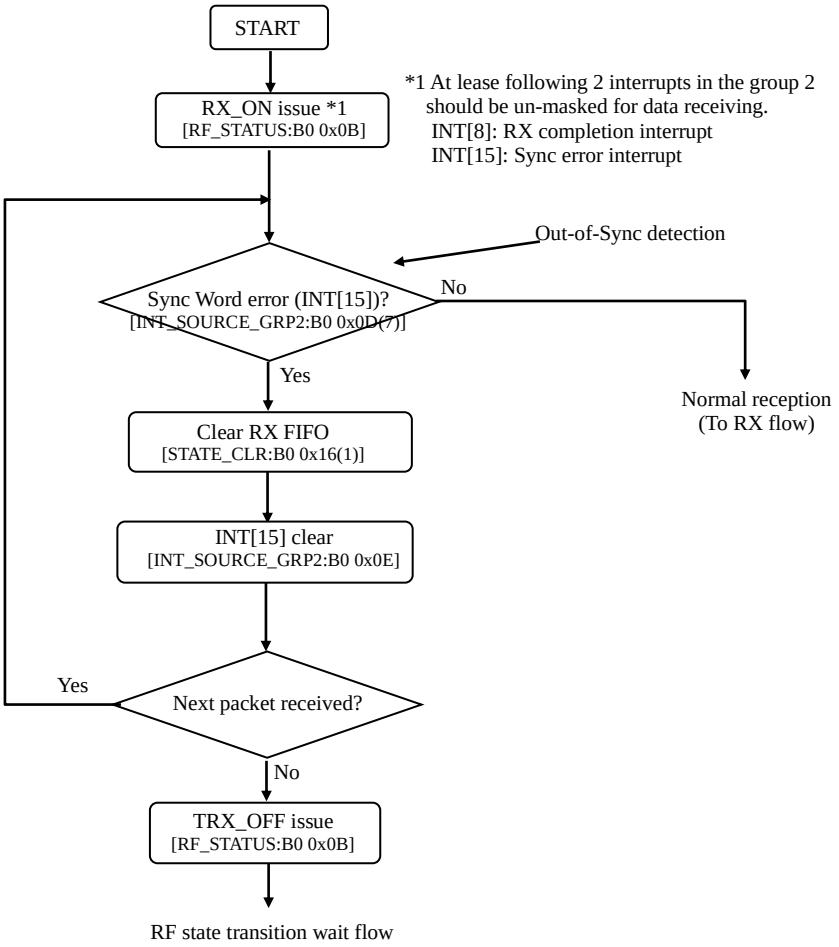


●Error Process

(1) Sync error

When out-of-sync is detected during data reception after SyncWord detection, Sync error interrupt (INT[15] group2) will be generated, RX completion interrupt (INT[8]: group2) will not be generated. If Sync error interrupt occurs, issuing STATE_CLR1 [STATE_CLR: B0 0x16(1)](RX FIFO pointer clear) without read RX_FIFO data and clear Sync error interrupt.

”data reception” indicates receiving data (L-field, data, CRC). after SyncWord detection.



[Note]

When ML7344 detects a sync error in FIFO mode, ML7344 judges that packet is invalid and stops storing the received data in the FIFO. And ML7344 clears the FIFO control information for reception. When FIFO is read in this state, since there is no receive data, invalid FIFO usage and RX FIFO access error interrupt are indicated. To receive the next packet, please clear the RX FIFO ([STATE_CLR:B0 0x16]) and RX FIFO access error interrupt(INT[12]) before starting reception.

When a sync error occurs, ML7344 continues the reception status(RX_ON) and waits for a sync word detection in preparation for the next packet reception immediately after the sync error. To receive the next packet correctly, clear the RX FIFO ([STATE_CLR:B0 0x16]) and all receive related interrupts([INT_SOURCE_GRP2:B0 0x0E]).

The internal state at the occurrence of the sync error and the processing necessary for receiving the next pacekt are as follows.

FIFO processing after sync error	FIFO processing from SyncWord detection to sync error	Internal state	processing necessary for receiving the next pacekt
No FIFO read	No FIFO read	If the FIFO read is not performed before the sync error occurs, the FIFO read pointer is maintained in the initial state.	The next packet data can be normally read without clearing the RX FIFO. Please clear all receive related interrupts([INT_SOURCE_GRP2:B0 0x0E]) in order to notify interrupts necessary for reception.
	FIFO Read	If the FIFO is read before sync error occurs, the FIFO read pointer is not cleared.	It is necessary to initialize the RX FIFO pointer in order to read the next packet data normally. Please surely clear the RX FIFO ([STATE_CLR:B0 0x16]) and clear all receive related interrupts([INT_SOURCE_GRP2:B0 0x0E]) in order to notify interrupts necessary for reception.
FIFO Read	FIFO Read / No FIFO read	FIFO will be read out with no receive data.Then, invalid FIFO usage and RX FIFO access error interrupt are indicated. RX FIFO read pointer is not cleared.	

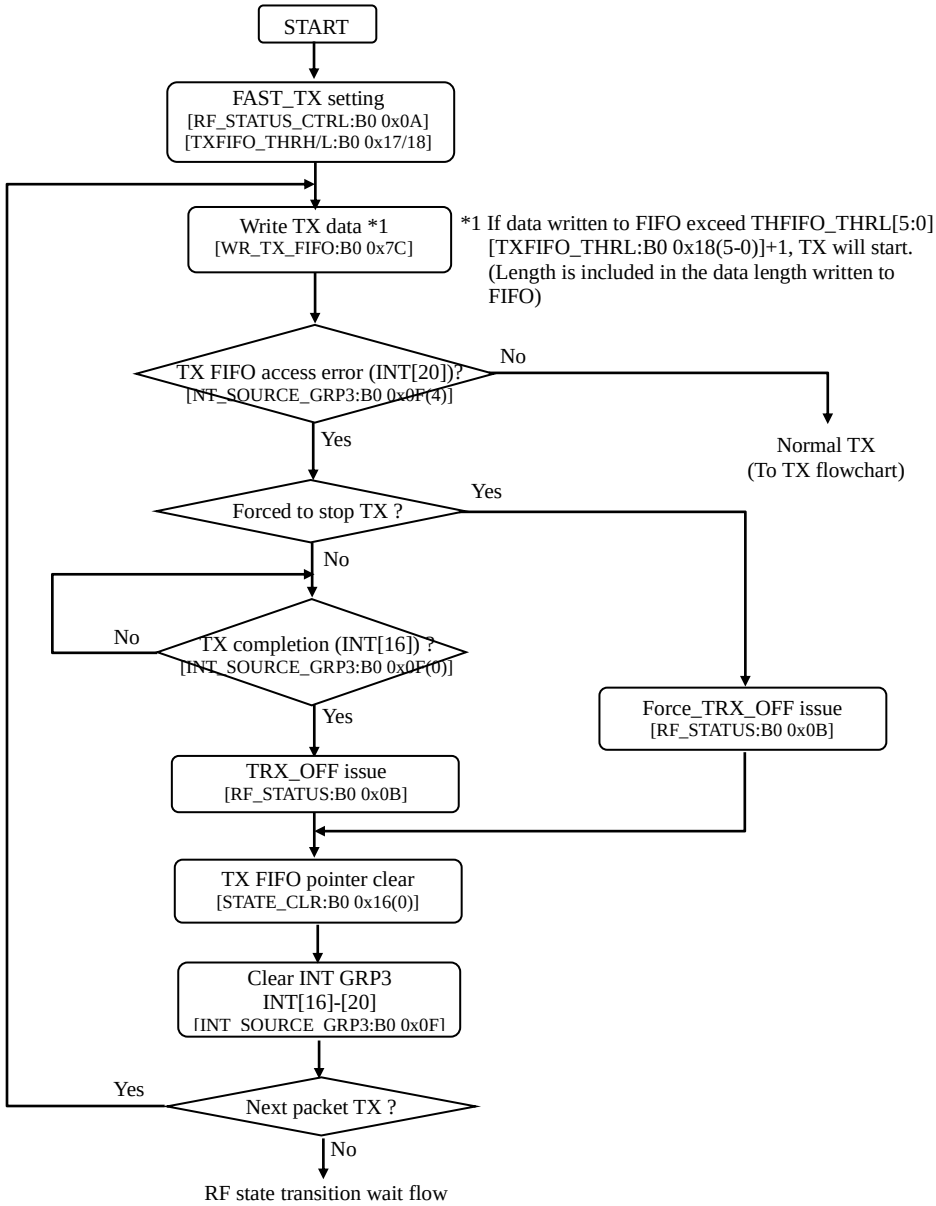
(2) TX FIFO access error

If one of the following conditions is met, TX FIFO access error interrupt (INT[20]: group3) will be generated.

- ●After TX Data request accept completion interrupt (INT[17]: group3] was generated, next packet is written to the TX_FIFO without transmiting the current TX data.
- ●Data write overflow occurs to the TX_FIFO.
- ●No TX data in the TX_FIFO during TX data transimission.

When TX FIFO acccess error interrupt occurs, issuing TRX_OFF after TX completion interrupt (INT[16]: group3) is recognized, or issueing Force_TRX_OFF by [RF_STATUS:B0 0x0A] register without waiting for TX completion interrupt. After that, issuing TX FIFO pointer clear by [STATE_CLR:B0 0x16] register and clear remaining interrupts relative with TX in the [INT_SOURCE_GRP3:B0 0x0F] register.

If TX FIFO access error occurs, subquent TX data will be inverted. CRC error should be detected at rexeiver side even if TRX_OFF is issued when TX completion interrupt detected.

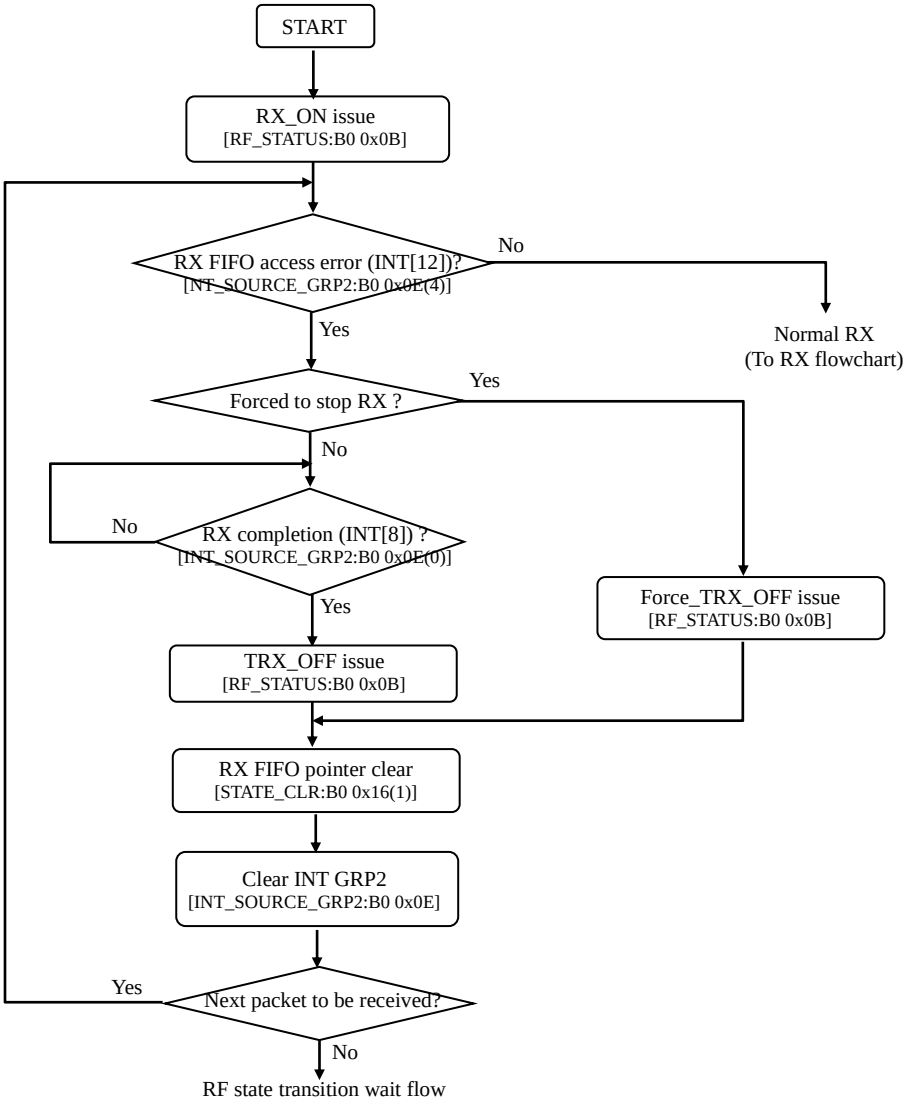


(3) RX FIFO access error

If one of the following conditions is met, RX FIFO access error interrupt (INT[12]: group2) will be generated.

- ●RX data overflow occurs to RX_FIFO
- ●Read RX_FIFO during no data in the RX_FIFO

When RX FIFO acccess error interrupt occurs, issuing TRX_OFF after RX completion interrupt (INT[8]: group2) is recognized, or issueing Force_TRX_OFF by [RF_STATUS:B0 0x0B] register without waiting for RX completion interrupt. After that, issuing RX FIFO pointer clear by [STATE_CLR:B0 0x16] register and clear remaining interrupts in the [INT_SOURCE_GRP2:B0 0x0E] register.

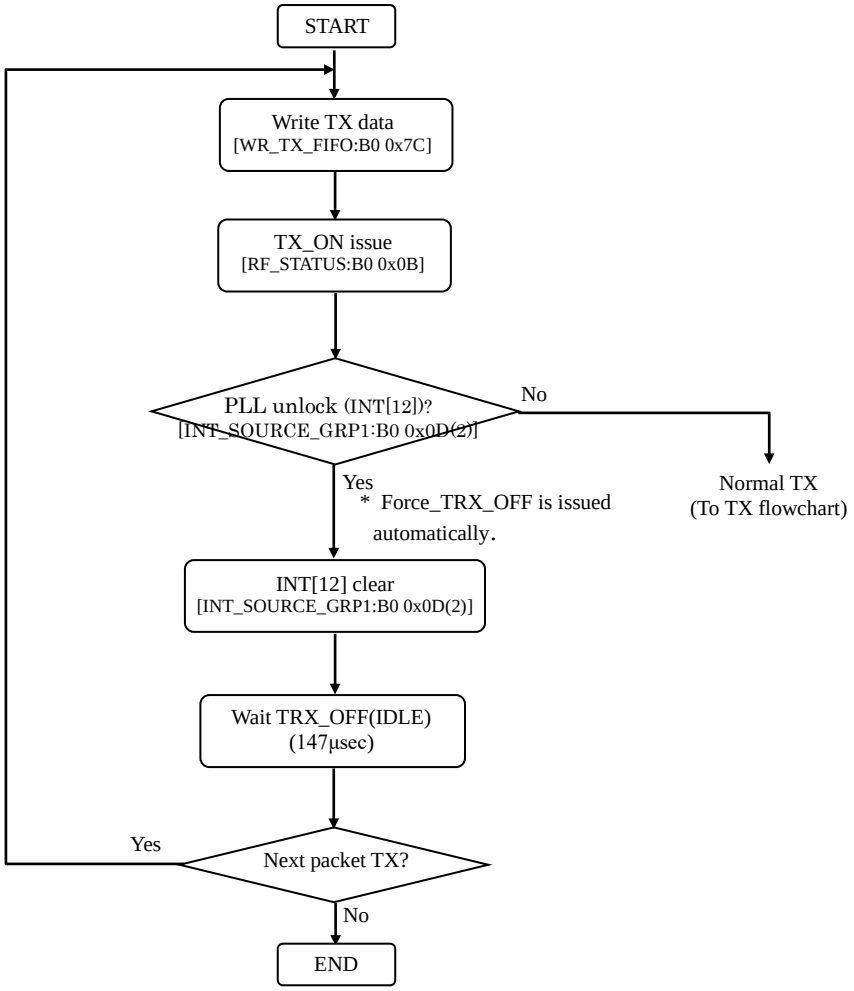


(4) PLL unlock detection

○TX

During TX, if PLL unlock is detected, PLL unlock interrupt (INT[2] group1) will be generated. When PLL unlock interrupt occurs, Force_TRX_OFF is automaticcally issued and move to IDLE state. SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)]) will be written to 0b0011(Force_TRX_OFF). PLL unlock might be occurred when VCO calibration value is not correct. Please confirm VCO calibration or perform VCOcalibration again.

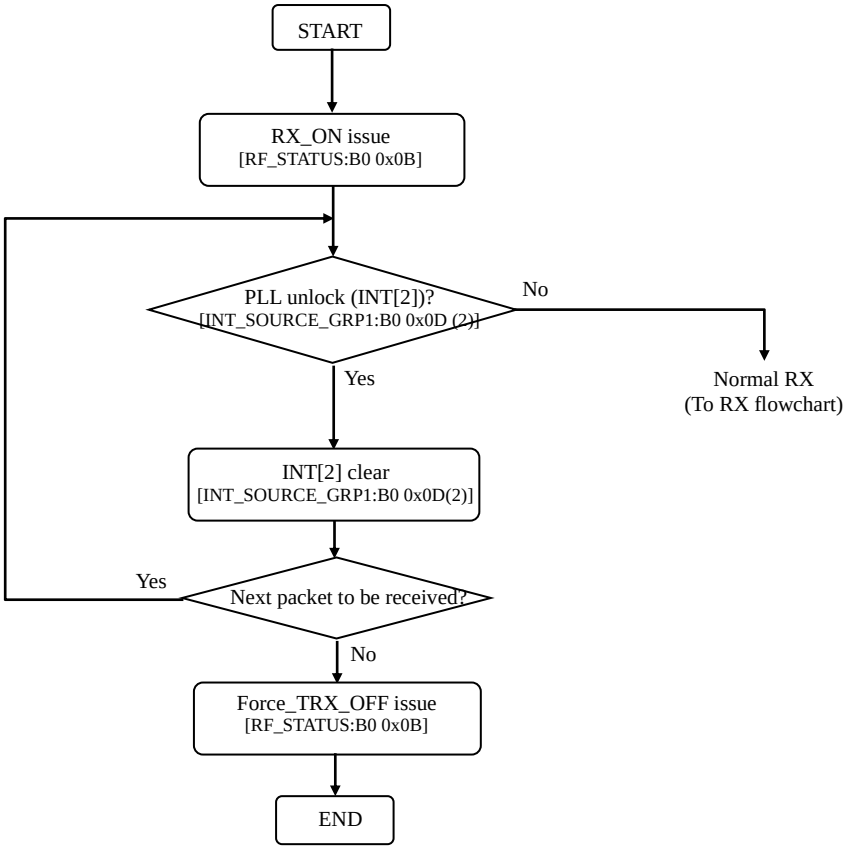
After PLL unlock interrupt occurs, max. 147 μs is necessary to move to IDLE state. Please wait for at least 147μs before next TX, RX or VCO calibration is performed.



○RX

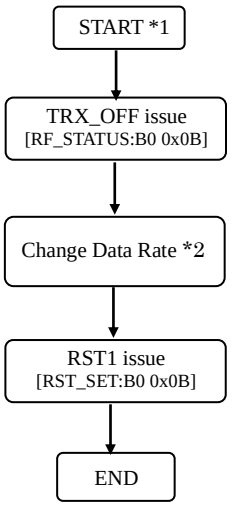
During RX, if PLL unlock is detected, PLL unlock interrupt (INT[2] group1) will be generated. During RX, even if PLL unlock is detected, RX state is maintained (do not move to IDLE state). Please receive next packet after clearing PLL unlock interrupt.

When PLL unlock interrupt occurs frequently, PLL unlock cause mitgh be due to the mismatch of the VCO circuit and using frequency band. Please use after removing the cause by circuit verification.



●Data Rate Change Sequence

When changing data rate during operation, registers relative data rate should be set in TRX_OFF state and issuing RST1([RST_SET: B0 0x01(1)])(MODEM reset) after register setting. If not issuing RST1, ML7344 can not transmit or receive correctlly.



*1 TX_ON or RX_ON state

*2 Relating registers
refer to “Data rate setting function”

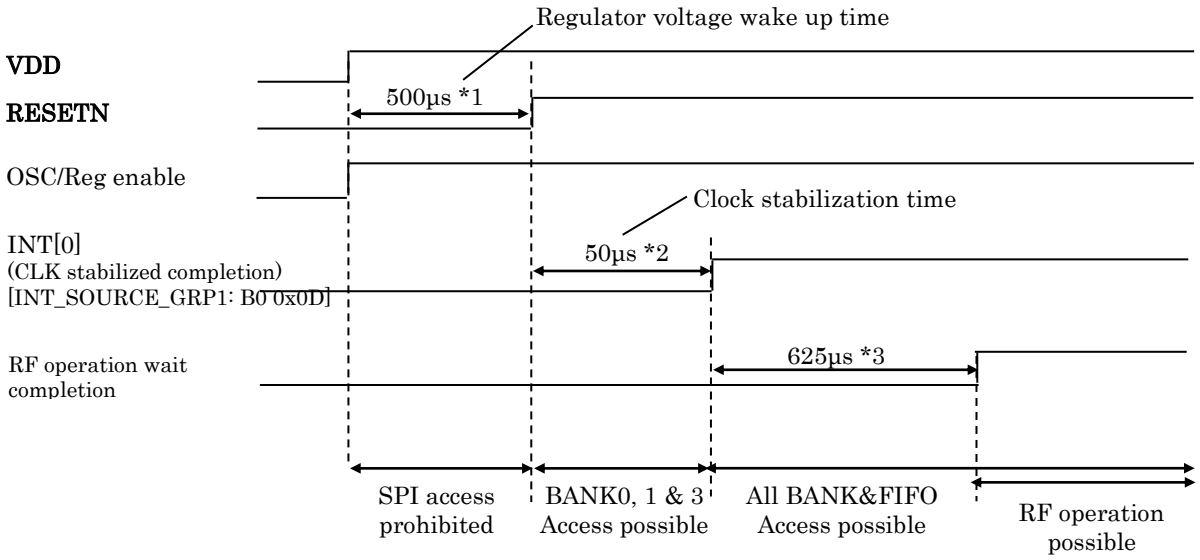
■Timing Chart

The followings are operation timing for major functions.

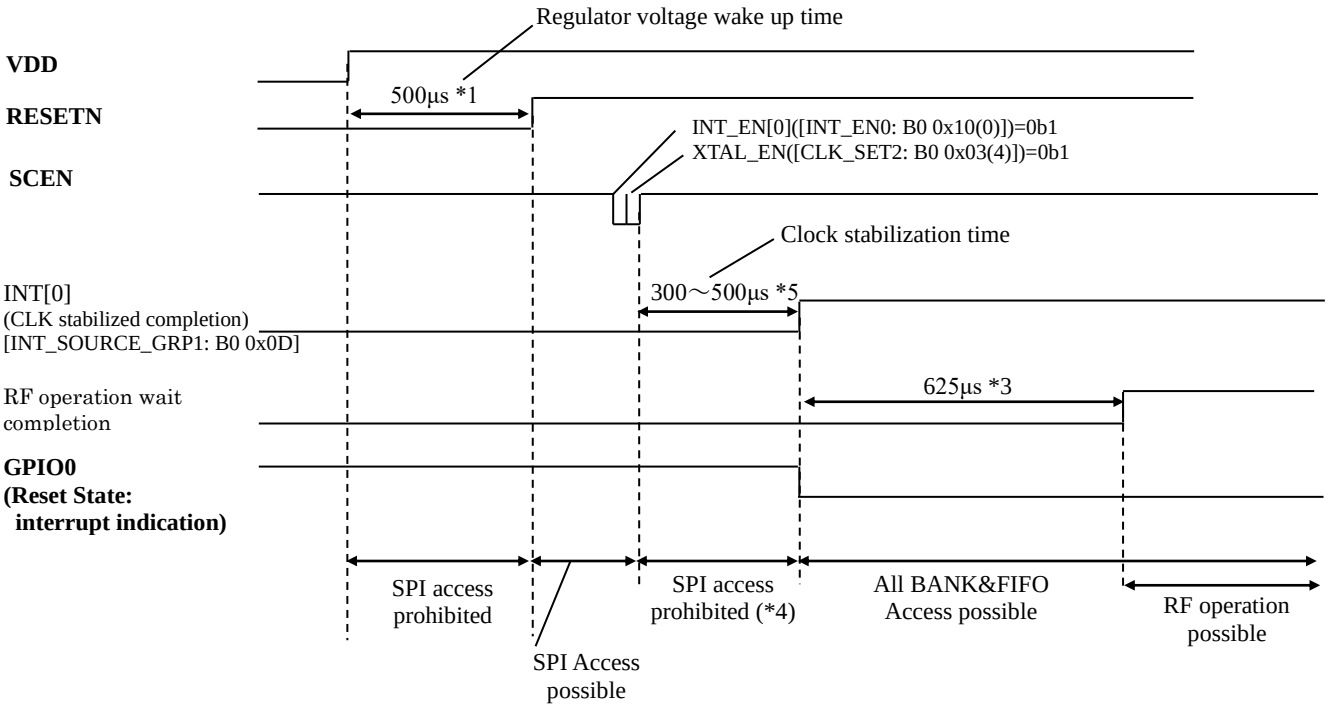
NOTE: Bold characters indicate pins related signals. Non bold characters indicate internal signals.

●Start-up

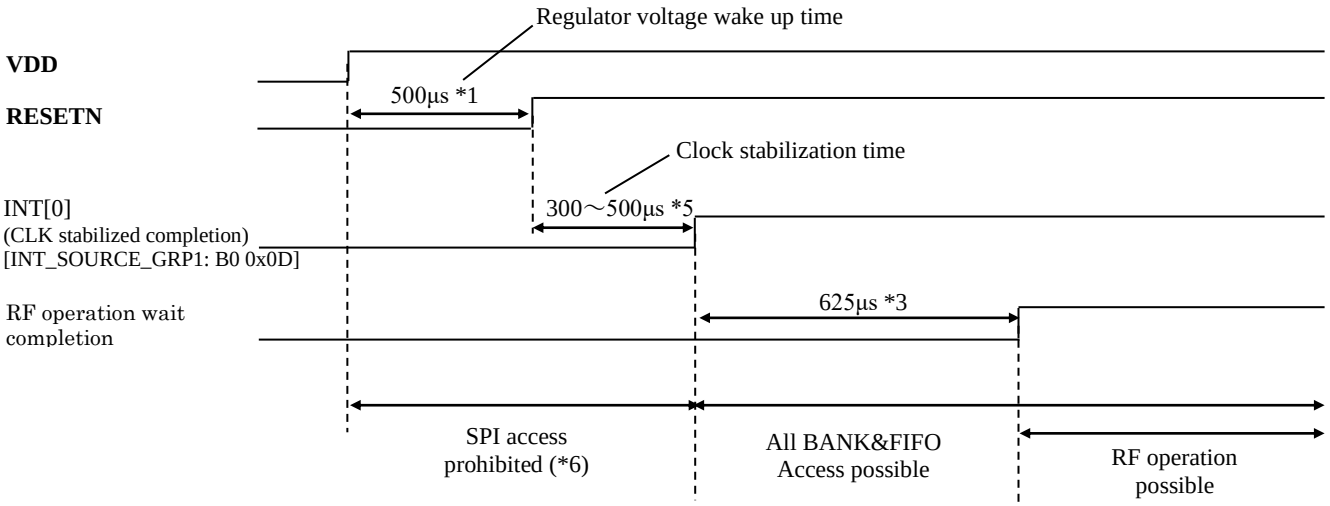
[ML7344JT]



[ML7344JC]



[ML7344CC]



*1 : For wake-up timing of VDD and RESETN, please refer to the “Reset characteristics”.

*2 : When setting XTAL_EN(CLK_SET2:B0 0x03(4)))=0b1, it is possible to adjust to 10/50/250/500 µs, by setting OSC_W_SEL[1:0]([ADC_CLK_SET: B1 0x08(6-5)]).
When using TCXO (TCXO_EN([CLK_SET2:B0 0x03(6)])=0b1), clock stabilization time is 5.5µs.

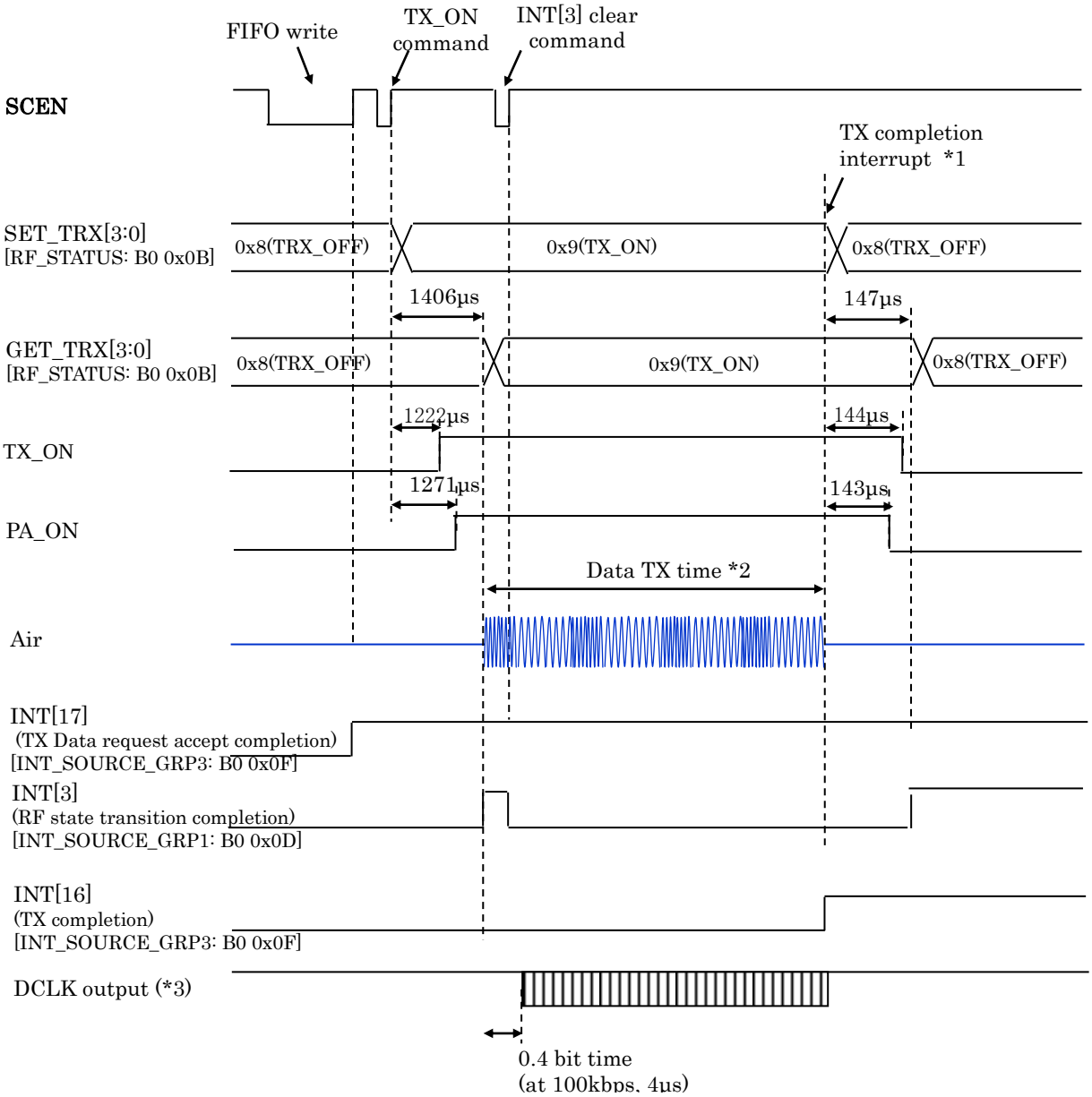
*3 : [VCO_CAL_START:B0 0x6F] and [RF_STATUS:B0 0x0B] resister access is possible, but process is pending until RF operation wait completion signal is asserted.

*4: In use of crystal oscillator circuit, clock stabilization time is about 300 to 500µs. This time changes by the matching condition(component values, etc) for crystal oscillator circuit.

*5: In use of ML7344JC, after hard reset is released, set 0b1 to XTAL_EN [CLK_SET2:B0 0x03(4)] at first. After crystal oscillator circuit was enabled, all register access and FIFO access (**) is prohibited until INT[0] occurrence.
(**) FIFO access: Accessing [WR_TX_FIFO: B0 0x7C] and [RD_FIFO: B0 0x7F] registers.

*6: In use of ML7344CC, after hardware reset is released, all register access and FIFO access (**) is prohibited until INT[0] occurrence.
(**) FIFO access: Accessing [WR_TX_FIFO: B0 0x7C] and [RD_FIFO: B0 0x7F] registers.

●TX



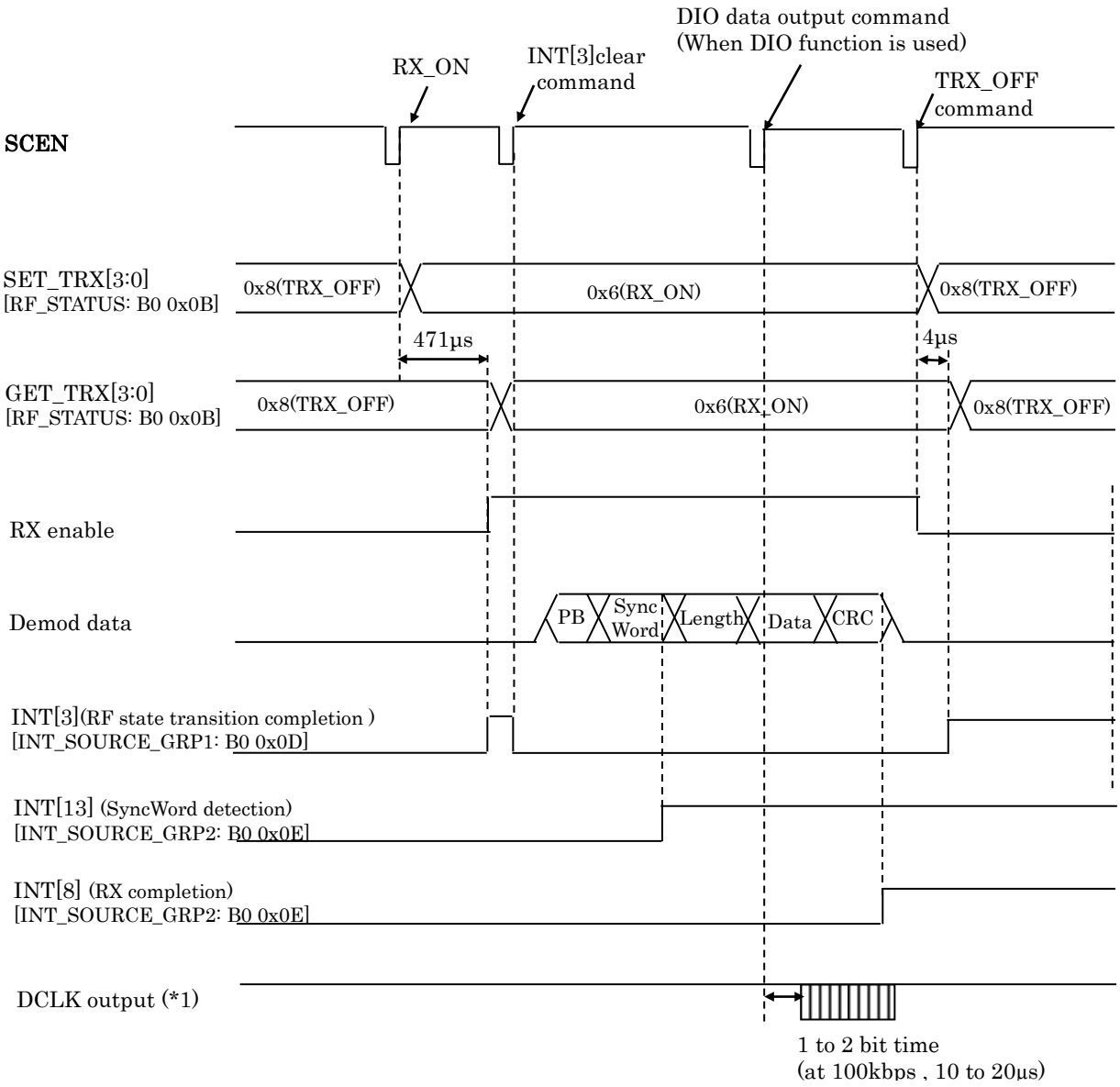
*1 : When TXDONE_MODE[1:0]([RF_STATUS_CTRL: B0 0x0A(1-0)]) = 0b00(default), SET_TRX[3:0] ([RF_STATUS: B0 0x0B(3-0)]) will be set to 0x8(TRX_OFF) automatically, upon detection of TX completion.

*2 : Data TX time calculation is as follows:

Data TX time [sec] = (number of TX bits+3)×1bit TX duration time[sec]
1bit TX duration time [sec] = 1/data rate [bps]

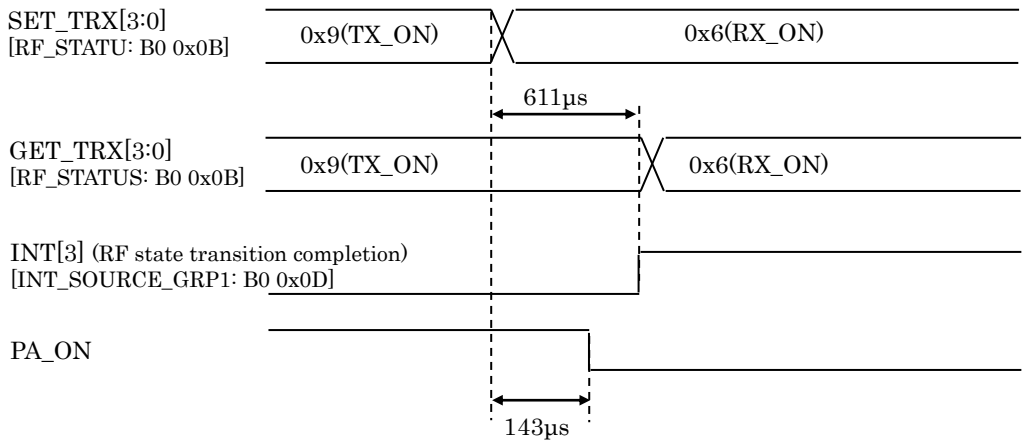
*3 : When setting TXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(5-4)])=0b01.

●RX

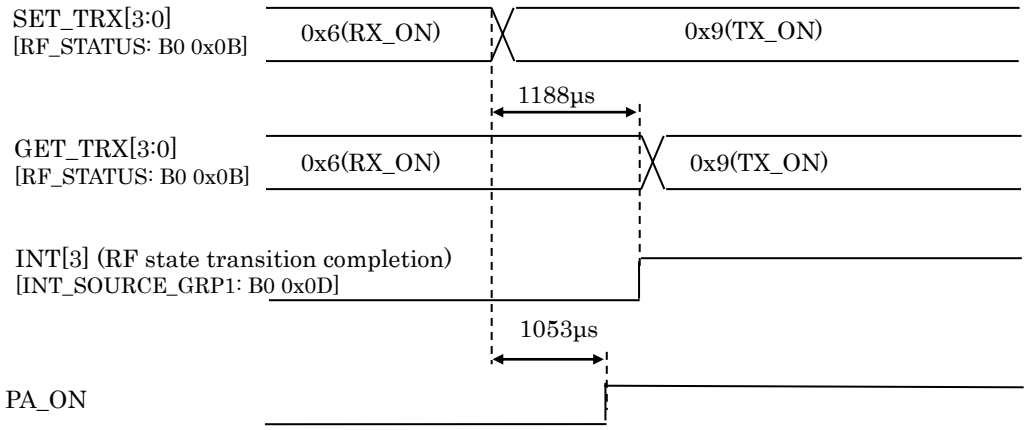


*1 : When setting RXDIO_CTRL[1:0]([DIO_SET: B0 0x0C(7-6)])=0b10 or 0b11.

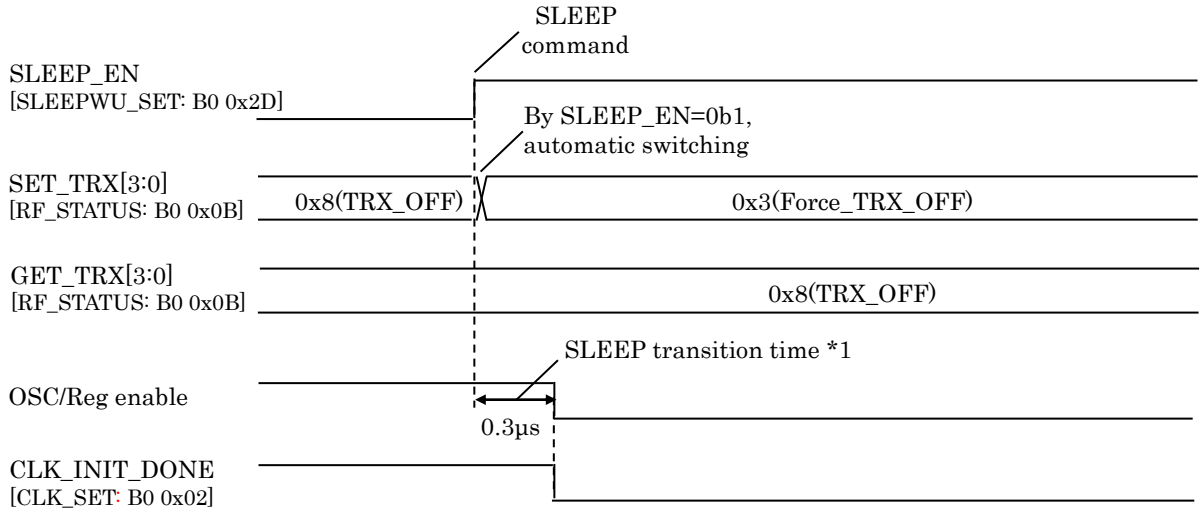
●Transition from TX to RX



●Transition from RX to TX

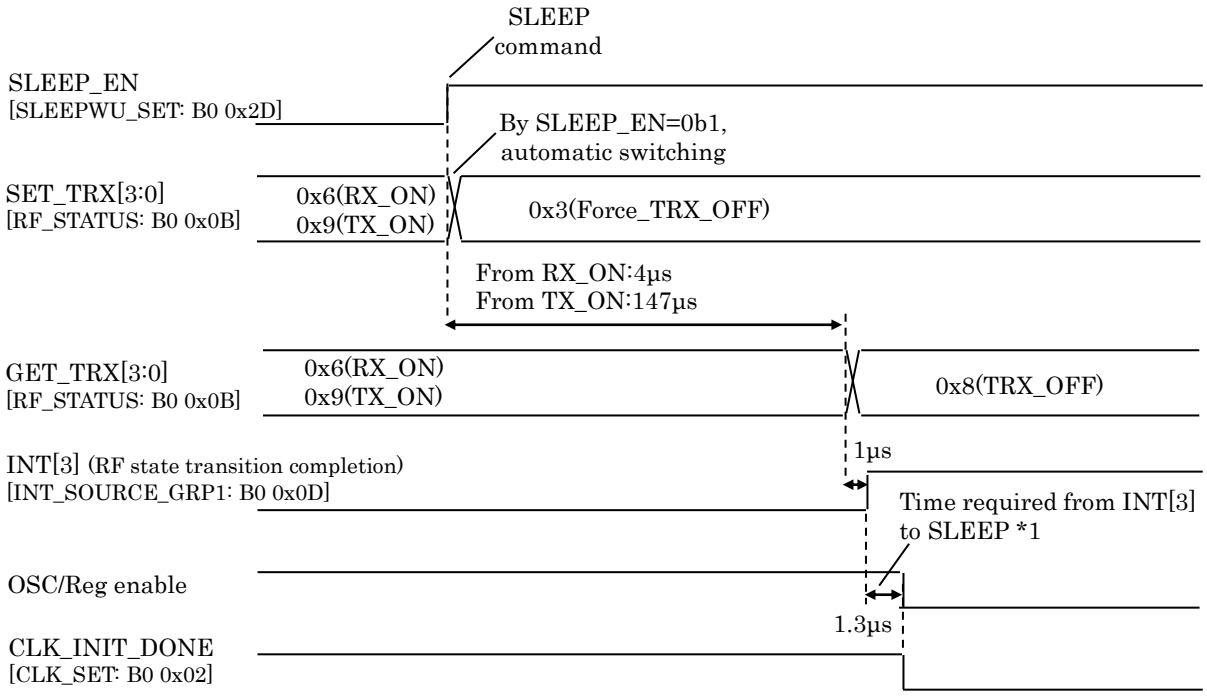


●Transition from IDLE to SLEEP



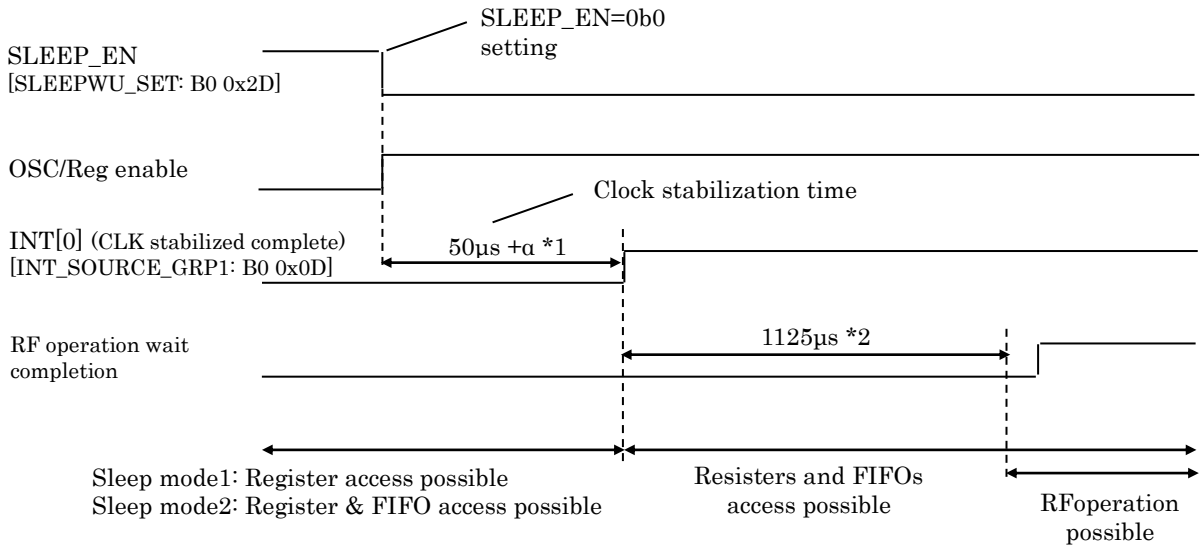
*1 : Clock input should be required for SLEEP transition. If TCXO is stopped during SLEEP stae, please wait 0.3µs after SLEEP command issued (SLEEP_EN([SLEEP/WU_SET: B0 0x2D(0)])=0b1) and then stop TCXO.

●Transition from TX/RX to SLEEP



*1 : If TCXO is used, please stop TCXO(clock) input after 1.3µs from INT[3] notification. by setting SLEEP command (SLEEP_EN ([SLEEP/WU_SET: B0 0x2D(0)])=0b1).

●Transition from SLEEP to IDLE

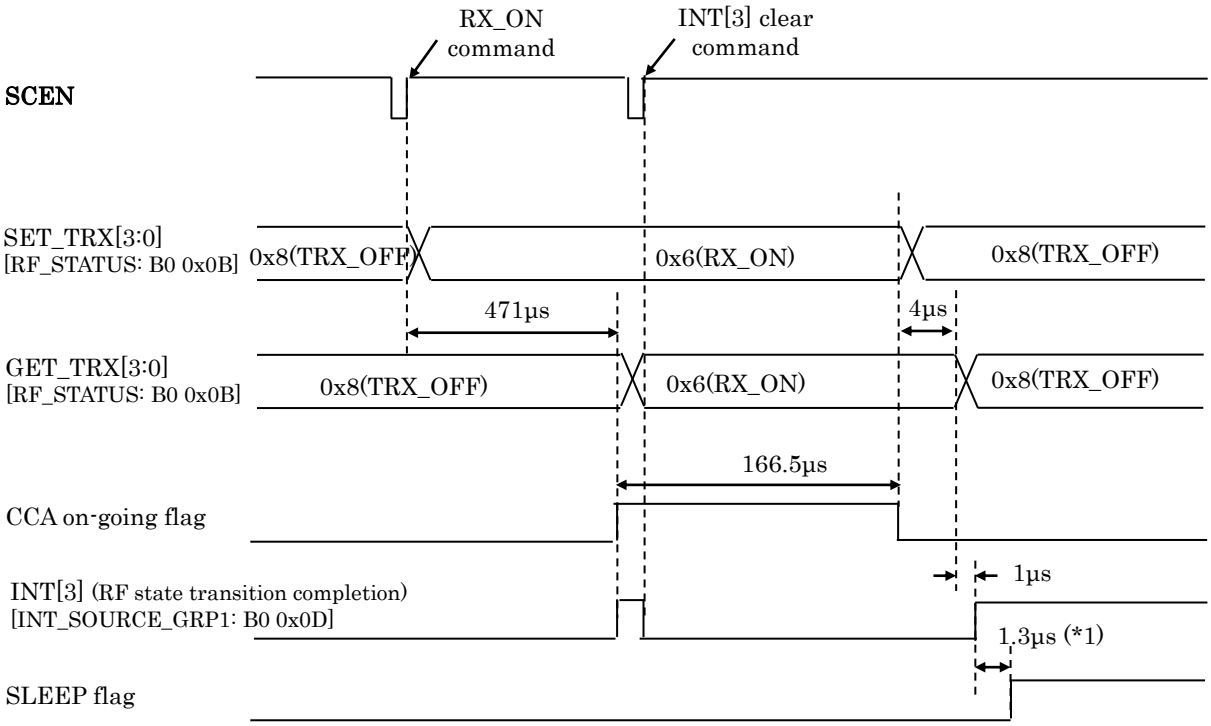


*1: When setting XTAL_EN([CLK_SET2: B0 0x03(4)])=0b1, it is possible to adjust to 10/50/250/500µs , by setting [ADC_CLK_SET: B1 0x08(6-5)]. α is oscillation cuircuits start-up time, and max. is 500µs.
When using TCXO (TCXO_EN([CLK_SET2:B0 0x03(6)])=0b1), clock stabilization time is 5µs.

*2: [VCO_CAL_START:B0 0x6F] and [SET_TRX:B0 0x0B] registers access is possible, but process is pending until RF operation wait completion signal is asserted.

●High speed carrier checking mode

Condition)
Use TCXO
ED averaging: 1 time



*1: Clock input should be required for SLEEP transition. If TCXO is stopped during SLEEP state, please wait 1.3µs from INT[3] and then stop TCXO.

■Registers

●Register map

It is consist of 4 banks, BANK0, BANK1, BANK2 and BANK3. Each BANK has address space of 0x00 to 0x7F, 128 byte in total.

The space shown as gray highlighted part is not implemented in LSI or reserved bits. Reserved bits may be assigned closed function. Please use default values to reserved bits, when write a register which contains reserved bits. Regarding reserved register, access is inhibited. BANK3 is closed BANK, then access is limited..

Transition between banks can be controlled by bit 3-0 (BANK[3:0]) of [BANK_SEL] register.

□ : Implemented as functionable register ▨ : Impelemted as reserved bits

BANK0

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access bank selection
0x01	RST_SET									Software reset setting
0x02	CLK_SET1		▨	▨						Clock configuration 1
0x03	CLK_SET2						▨			Clock configuration 2
0x04	PKT_CTRL1						▨			Packet configuration 1
0x05	PKT_CTRL2							▨		Packet configuration 2
0x06	DRATE_SET									Data rate setting
0x07	DATA_SET1									TX/RX data configuration 1
0x08	DATA_SET2	▨	▨	▨						TX/RX data configuration 2
0x09	CH_SET									RF channel setting
0x0A	RF_STATUS_CTRL	▨	▨							RF auto status transition control
0x0B	RF_STATUS									RF state setting and status indication
0x0C	DIO_SET					▨		▨		DIO mode configuration
0x0D	INT_SOURCE_GRP1									Interrupt status for INT0 to INT7
0x0E	INT_SOURCE_GRP2							▨		Interrupt status for INT8 to INT15 (RX)
0x0F	INT_SOURCE_GRP3			▨						Interrupt status for INT16 to INT23 (TX)
0x10	INT_EN_GRP1									Interrupt mask for INT0 to INT7
0x11	INT_EN_GRP2									Interrupt mask for INT8 to INT15
0x12	INT_EN_GRP3									Interrupt mask for INT16 to INT23
0x13	CRC_ERR_H	▨	▨	▨	▨	▨	▨	▨		CRC error status (high byte)
0x14	CRC_ERR_M									CRC error status (middle byte)
0x15	CRC_ERR_L									CRC error status (low byte)
0x16	STATE_CLR		▨	▨		▨				State clear control
0x17	TXFIFO_THRH		▨							TX FIFO-Full level setting
0x18	TXFIFO_THRL		▨							TX FIFO-Empty level setting and TX trigger level setting in FAST_TX mode
0x19	RXFIFO_THRH		▨							RX FIFO-Full level setting
0x1A	RXFIFO_THRL		▨							RX FIFO-Empty level setting
0x1B	C_CHECK_CTRL			▨						Control field (C-field) detection setting
0x1C	M_CHECK_CTRL	▨	▨	▨	▨					Manufacture ID field (M-field) detection setting
0x1D	A_CHECK_CTRL	▨	▨							Address field (A-Field) detection setting
0x1E	C_FIELD_CODE1									C-field setting code #1
0x1F	C_FIELD_CODE2									C-field setting code #2

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x20	C_FIELD_CODE3									C-field setting code #3
0x21	C_FIELD_CODE4									C-field setting code #4
0x22	C_FIELD_CODE5									C-field setting code #5
0x23	M_FIELD_CODE1									M-field 1st byte setting code #1
0x24	M_FIELD_CODE2									M-field 1st byte setting code #2
0x25	M_FIELD_CODE3									M-field 2nd byte setting code #1
0x26	M_FIELD_CODE4									M-field 2nd byte setting code #2
0x27	A_FIELD_CODE1									A-field 1st byte setting
0x28	A_FIELD_CODE2									A-field 2nd byte setting
0x29	A_FIELD_CODE3									A-field 3rd byte setting
0x2A	A_FIELD_CODE4									A-field 4th byte setting
0x2B	A_FIELD_CODE5									A-field 5th byte setting
0x2C	A_FIELD_CODE6									A-field 6th byte setting
0x2D	SLEEP/WU_SET									SLEEP execution and Wake-up operation setting
0x2E	WUT_CLK_SET									Wake-up timer clock division setting
0x2F	WUT_INTERVAL_H									Wake-up timer interval setting (high byte)
0x30	WUT_INTERVAL_L									Wake-up timer interval setting (low byte)
0x31	WU_DURATION									Continue operation timer (after Wake-up) setting
0x32	GT_SET									General purpose timer configuration
0x33	GT_CLK_SET									General purpose timer clock division setting
0x34	GT1_TIMER									General purpose timer #1 setting
0x35	GT2_TIMER									General purpose timer #2 setting
0x36	CCA_IGNORE_LVL									ED threshold level setting for excluding CCA judgement
0x37	CCA_LVL									CCA threshold level setting
0x38	CCA_ABORT									Timing setting for forced termination of CCA operation
0x39	CCA_CTRL									CCA control setting and result indication
0x3A	ED_RSLT									ED value indication
0x3B	IDLE_WAIT_H									IDLE detection period setting during CCA (high 2bits)
0x3C	IDLE_WAIT_L									IDLE detection period setting during CCA (low byte)
0x3D	CCA_PROG_H									IDLE judgement elapsed time indication during CCA (high 2 bits)
0x3E	CCA_PROG_L									DLE judgement elapsed time indication during CCA (low byte)
0x3F	Reserved									Reserved
0x40	VCO_VTRSLT									VCO voltage adjustment result indication
0x41	ED_CTRL									ED detection control setting
0x42	TXPR_LEN_H									TX preamble length setting (high byte)
0x43	TXPR_LEN_L									TX preamble length setting (low byte)
0x44	POSTAMBLE_SET									Postamble length and pattern setting
0x45	SYNC_CONDITION1									RX preamble setting and ED threshold check setting
0x46	SYNC_CONDITION2									ED threshold setting during synchronization
0x47	SYNC_CONDITION3									Bit error tolerance setting in RX preamble and SyncWord detection
0x48-4C	Reserved									Reserved
0x4D	MON_CTRL									Monitor function setting
0x4E	GPIO0_CTRL									GPIO0 pin (pin #16) configuration setting
0x4F	GPIO1_CTRL									GPIO1 pin (pin #17) configuration setting

BANK0 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x50	GPIO2_CTRL									GPIO2 pin (pin #18) configuration setting
0x51	GPIO3_CTRL									GPIO3 pin (pin #19) configuration setting
0x52	EXTCLK_CTRL									EXT_CLK pin (pin #10) configuration setting
0x53	SPI/EX_PA_CTRL									SPI interface IO configuration/external PA control setting
0x54	IF_FREQ_H									IF frequency setting (high byte)
0x55	IF_FREQ_L									IF frequency setting (low byte)
0x56-61	Reserved									Reserved
0x62	OSC_ADJ1									Coarse adjustment of load capacitance for oscillation circuit
0x63	OSC_ADJ2									Fine adjustment of load capacitance for oscillation circuit
0x64-65	Reserved									Reserved
0x66	RSSI_ADJ									RSSI value adjustment
0x67	PA_MODE									PA mode setting / PA regulator coarse adjustment
0x68	PA_REG_FINE_ADJ									PA regulator fine adjustment
0x69	PA_ADJ									PA gain adjustment
0x6A-6D	Reserved									Reserved
0x6E	VCO_CAL									VCO calibration setting or status indication
0x6F	VCO_CAL_START									VCO calibration execution
0x70	CLK_CAL_SET									Low speed clock calibration control
0x71	CLK_CAL_TIME									Low speed clock calibration time setting
0x72	CLK_CAL_H									Low speed clock calibration result indication (high byte)
0x73	CLK_CAL_L									Low speed clock calibration result indication (low byte)
0x74	Reserved									
0x75	SLEEP_INT_CLR									Interruption clear setting during SLEEP state
0x76	RF_TEST_MODE									TX test pattern setting
0x77	STM_STATE									State machine status / synchronization status indication
0x78	FIFO_SET									FIFO readout setting
0x79	RX_FIFO_LAST									RX FIFO data usage status indication
0x7A	TX_PKT_LEN_H									Tx packet length setting (high byte)
0x7B	TX_PKT_LEN_L									Tx packet length setting (low byte)
0x7C	WR_TX_FIFO									TX_FIFO
0x7D	RX_PKT_LEN_H									Rx packet length indication (high byte)
0x7E	RX_PKT_LEN_L									Rx packet length indication (low byte)
0x7F	RD_FIFO									FIFO read

BANK1

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access bank select
0x01	CLK_OUT									CLK_OUT (GPIOn) output frequency setting
0x02	TX_RATE_H									TX data rate conversion setting (high 4 bits)
0x03	TX_RATE_L									TX data rate conversion setting (low byte)
0x04	RX_RATE1_H									RX data rate conversion setting 1 (high 4 bits)
0x05	RX_RATE1_L									RX data rate conversion setting 1 (low byte)
0x06	RX_RATE2									RX data rate conversion setting 2
0x07	Reserved									Reserved
0x08	ADC_CLK_SET									RSSI ADC clock frequency setting
0x09-0A	Reserved									Reserved
0x0B	PLL_LOCK_DETECT									PLL lock detection setting
0x0C-0x12	Reserved									Reserved
0x13	RSSI_MAG_ADJ									Scale factor setting for ED value conversion
0x14	RSSI_VAL									RSSI value indication
0x15	AFC_CTRL									AFC control setting
0x16	CRC_POLY3									CRC Polynomial setting 3
0x17	CRC_POLY2									CRC Polynomial setting 2
0x18	CRC_POLY1									CRC Polynomial setting 1
0x19	CRC_POLY0									CRC Polynomial setting 0
0x1A	PLL_DIV_SET									PLL frequency division setting
0x1B	TXFREQ_I									TX frequency setting (I counter)
0x1C	TXFREQ_FH									TX frequency setting (F counter high 4 bits)
0x1D	TXFREQ_FM									TX frequency setting (F counter middle byte)
0x1E	TXFREQ_FL									TX frequency setting (F counter low byte)
0x1F	RXFREQ_I									RX frequency setting (I counter)
0x20	RXFREQ_FH									RX frequency setting (F counter high 4 bits)
0x21	RXFREQ_FM									RX frequency setting (F counter middle byte)
0x22	RXFREQ_FL									RX frequency setting (F counter low byte)
0x23	CH_SPACE_H									Channel space setting (high byte)
0x24	CH_SPACE_L									Channel space setting (low byte)
0x25	SYNC_WORD_LEN									SyncWord length setting
0x26	SYNC_WORD_EN									SyncWord enable setting
0x27	SYNC_WORD1_SET0									SyncWord #1 setting (bit24 to 31)
0x28	SYNC_WORD1_SET1									SyncWord #1 setting (bit16 to 23)
0x29	SYNC_WORD1_SET2									SyncWord #1 setting (bit8 to 15)
0x2A	SYNC_WORD1_SET3									SyncWord #1 setting (bit0 to 7)
0x2B	SYNC_WORD2_SET0									SyncWord #2 setting (bit24 to 31)
0x2C	SYNC_WORD2_SET1									SyncWord #2 setting (bit16 to 23)
0x2D	SYNC_WORD2_SET2									SyncWord #2 setting (bit8 to 15)
0x2E	SYNC_WORD2_SET3									SyncWord #2 setting (bit0 to 7)
0x2F	FSK_CTRL									GFSK/FSK modulation timing resolution setting

BANK1 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x30	GFSK_DEV_H									GFSK frequency deviation setting (high 6 bits)
0x31	GFSK_DEV_L									GFSK frequency deviation setting (low byte)
0x32	FSK_DEV0_H/GFIL0									FSJ 1st frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 0
0x33	FSK_DEV0_L/GFIL1									FSJ 1st frequency deviation setting (low byte) / Gaussian filter coefficient setting 1
0x34	FSK_DEV1_H/GFIL2									FSJ 2nd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 2
0x35	FSK_DEV1_L/GFIL3									FSJ 2nd frequency deviation setting (low byte) / Gaussian filter coefficient setting 3
0x36	FSK_DEV2_H/GFIL4									FSJ 3rd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 4
0x37	FSK_DEV2_L/GFIL5									FSJ 3rd frequency deviation setting (low byte) / Gaussian filter coefficient setting 5
0x38	FSK_DEV3_H/GFIL6									FSJ 4th frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 6
0x39	FSK_DEV3_L									FSJ 4th frequency deviation setting (low byte)
0x3A	FSK_DEV4_H									FSJ 5th frequency deviation setting (high 6 bits)
0x3B	FSK_DEV4_L									FSJ 5th frequency deviation setting (low byte)
0x3C	FSK_TIM_ADJ4									FSK 4th frequency deviation hold timing setting
0x3D	FSK_TIM_ADJ3									FSK 3rd frequency deviation hold timing setting
0x3E	FSK_TIM_ADJ2									FSK 2nd frequency deviation hold timing setting
0x3F	FSK_TIM_ADJ1									FSK 1st frequency deviation hold timing setting
0x40	FSK_TIM_ADJ0									FSK no-deviation frequency (carrier frequency) hold timing setting
0x41-4C	Reserved									Reserved
0x4D	VCO_CAL_MIN_I									VCO calibration low limit frequency setting (I counter)
0x4E	VCO_CAL_MIN_FH									VCO calibration low limit frequency setting (F counter high 4 bits)
0x4F	VCO_CAL_MIN_FM									VCO calibration low limit frequency setting (F counter middle byte)

BANK1 (continued)

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x50	VCO_CAL_MIN_FL									VCO calibration low limit frequency setting (F counter low byte)
0x51	VCO_CAL_MAX_N									VCO calibration upper limit frequency setting
0x52	TXVCAL_MIN									TX VCO calibration low limit value indication and setting
0x53	TXVCAL_MAX									TX VCO calibration upper limit value indication and setting
0x54	RXVCAL_MIN									RX VCO calibration low limit value indication and setting
0x55	RXVCAL_MAX									RX VCO calibration upper limit value indication and setting
0x56	DEMOD_SET0									Demodulator configuration #0
0x57	DEMOD_SET1									Demodulator configuration #1
0x58	DEMOD_SET2									Demodulator configuration #2
0x59	DEMOD_SET3									Demodulator configuration #3
0x5A	DEMOD_SET4									Demodulator configuration #4
0x5B	DEMOD_SET5									Demodulator configuration #5
0x5C	DEMOD_SET6									Demodulator configuration #6
0x5D	DEMOD_SET7									Demodulator configuration #7
0x5E	DEMOD_SET8									Demodulator configuration #8
0x5F	DEMOD_SET9									Demodulator configuration #9
0x60	DEMOD_SET10									Demodulator configuration #10
0x61	Reserved									
0x62	ADDR_CHK_CTR_H									Address check counter indication (high 3 bits)
0x63	ADDR_CHK_CTR_L									Address check counter indication (low byte)
0x64	WHT_INIT_H									Whitening initialized state setting (high 1 bit)
0x65	WHT_INIT_L									Whitening initialized state setting (low byte)
0x66	WHT_CFG									Whitening polynomial setting
0x67-7E	Reserved									Reserved
0x7F	ID_CODE									ID code

BANK2

Address	Symbol (# test register)	Bit								Description
		7	6	5	4	3	2	1	0	
0x00	BANK_SEL									Register access bank select
0x01-2B	Reserved									Closed register
0x2C	LO_BIAS_IP									Local bias adjustment (I-Phase Positive)
0x2D	LO_BIAS_IN									Local bias adjustment (I-Phase Negative)
0x2E	LO_BIAS_QP									Local bias adjustment (Q-Phase Positive)
0x2F	LO_BIAS_QN									Local bias adjustment (Q-Phase Negative)
0x30-3F	Reserved									Closed register
40	VTUNE_COMP_ON									VCO adjustment voltage comparison result display enable
0x41-7F	Reserved									Closed register

●Register Bank0

0x00[BANK_SEL]

Function: Register access bank selection
Address: 0x00 (BANK0)
Defalut value: 0x11

Bit	Bit name	Reset Value	R/W	Description
7	B3_ACEN	0	R/W	BANK3 register access enable 0: Access disable 1: Access enable
6	B2_ACEN	0	R/W	BANK2 register access enable 0: Access disable 1: Access enable
5	B1_ACEN	0	R/W	BANK1 register access enable 0: Access disable 1: Access enable
4	B0_ACEN	1	R/W	BANK0 register access enable 0: Access disable 1: Access enable
3-0	BANK[3:0]	0001	R/W	BANK selection 0b0001: BANK0 access 0b0010: BANK1 access 0b0100: BANK2 access 0b1000: BANK3 access Other setting: prohibit

NOTE:

1. During VCO calibration operation, do not access BANK1 registers
2. Register access can be done when CLK_INT_DONE([CLK_SET: B0 0x02(7)])=0b0.
   But the registers related to RF status has to be accessed after CLK_INT_DONE=0b1

0x01[RST_SET]

Function: Software reset setting
Address: 0x01 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	RST3_EN	0	R/W	Reser3 enabling setting 0: reset disable 1: reset enable (after reset automatically written to 0b0)
6	RST2_EN	0	R/W	Reser2 enabling setting 0: reset disable 1: reset enable (after reset automatically written to 0b0)
5	RST1_EN	0	R/W	Reser1 enabling setting 0: reset disable 1: reset enable (after reset automatically written to 0b0)
4	RST0_EN	0	R/W	Reser0 enabling setting 0: reset disable 1: reset enable (after reset automatically written to 0b0)
3	RST3	0	R/W	PHY function reset bit7(RST3_EN)=0b1, reset can be executed 0: not reset 1: reset execution (after reset automatically written to 0b0)
2	RST2	0	R/W	RF control function reset bit6(RST2_EN)=0b1, reset can be executed 0: not reset 1: reset execution (after reset automatically written to 0b0)
1	RST1	0	R/W	MODEM function reset bit5(RST1_EN)=0b1, reset can be executed 0: not reset 1: reset execution (after reset automatically written to 0b0)
0	RST0	0	R/W	Configuration function reset bit5(RST1_EN)=0b1, reset can be executed 0: not reset 1: reset execution (after reset automatically written to 0b0) Note: All register, except [CLK_SET2:B0 0x03] bit 6-4, are reset to the initial value. Note: After reset, FIFO data are not guaranteed.

Description:

1. Please set enable bit (bit7 to bit4) and execution bit (bit3 to bit0) at the same time. After reset, status are not retained and automatically written to 0b0.
2. 2μs after writing to the execution bit (bit3 to bit0), reset operation will complete. However, if executing reset in SLEEP state (while SLEEP_EN ([SLEEP/WU_SET:B0 0x2D(0)]) =0b1), reset will be executed at Clock stabilizzation completion interrupt (INT[0] group1) from SLEEP release and each bit turned to 0b0. If chnaging set value before reset execution, last setting is valid.

0x02[CLK_SET1]

Function: Clock configuration 1
Address: 0x02 (BANK0)
Defalut value: 0x1F

Bit	Bit name	Reset Value	R/W	Description
7	CLK_INT_DONE	0	R	Clock stabilization completion flag
6:5	Reserved	00	R/W	
4	CLK4_EN	1	R/W	ADC clock control 0: clock stop 1: clock enable
3	CLK3_EN	1	R/W	RF function (RF state control) clock control 0: clock stop 1: clock enable
2	CLK2_EN	1	R/W	TX function (MOD) clock control 0: clock stop 1: clock enable
1	CLK1_EN	1	R/W	RX function (DEMOD) clock control 0: clock stop 1: clock enable
0	CLK0_EN	1	R/W	PHY function clock control 0: clock stop 1: clock enable

0x03[CLK_SET2]

Function: Clock configuration 2
Address: 0x03 (BANK0)
Defalut value: 0xC3 (ML7344J) / 0x93(ML7344C)

Bit	Bit name	Reset Value	R/W	Description
7	MSTR_CLK_EN	1	R/W	Logic block clock enable control 0: disable 1: enable
6	TCXO_EN	1	R/W	TCXO input control (1) (2) (3) 0: disable 1: enable
5	Reserved	0	R/W	
4	XTAL_EN	0	R/W	Crystal oscillator circuit control (1) (2) (3) 0: disable 1: enable
3	RC32K_EN	0	R/W	On chip Low speed RC oscillator circuits enable control 0: disable 1: enable
2	Reserved	0	R/W	
1	REG_PA_EN	1	R/W	PA regulator control 0: continuously turned-on 1: Turned-off during RX
0	LOW_RATE_EN	1	R/W	RX low rate clock mode control 0: disable 1: enable Note: If enable, achievable the consumption current defined in the "Power Consumption".

NOTE:

(1) In case of using TCXO, set 0b1 to either TCXO_EN. And one of TCXO_EN, XTAL_EN has to be 0b1.

(2) RST0([RST_SET: B0 0x02(0)]) cannot clear these bits. In order to clear, hard reset (RESETN="L") or clear these bits through the SPI interface from HOST MCU.

(3) In case of using TCXO, this register must be programmed first. If other registers are set before programming this register, values set to other registers are not valid.

(4) In use of ML7344JC, after hardware reset is released, set 0b1 to XTAL_EN [CLK_SET2:B0 0x03(4)] at first. After crystal oscillator circuit was enabled, all register access and FIFO access (**) is prohibited until INT[0] occurrence.
**: FIFO access: Accessing [WR_TX_FIFO: B0 0x7C] and [RD_FIFO: B0 0x7F] registers.

(5) In use of ML7344CC, after hardware reset is released, all register access and FIFO access (**) is prohibited until INT[0] occurrence.
**: FIFO access: Accessing [WR_TX_FIFO: B0 0x7C] and [RD_FIFO: B0 0x7F] registers.

0x04[PKT_CTRL1]

Function: Packet configuration 1
Address: 0x04 (BANK0)
Defalut value: 0x00(ML7344J) / 0x02(ML7344C)

Bit	Bit name	Reset Value	R/W	Description
7:6	EXT_PKT_MODE[1:0]	00	R/W	Extended Link Layer mode setting (Wireless M-bus) 00: no Extended Link Layer 01: 2 byte extension (Extended Link Layer CI=0x8C) 10: 8 byte extension (Extended Link Layer CI=0x8D) 11: Reserved Please refer to the “Packet Format”. (note) When packet format setting is Format A and packet expansion mode is set by 0b10, it cannot transmit and receive data properly with the Length value meeting the following condition. So please use the Length value where the following condition is not met. (condition) a surplus of "(length -15)/16" becomes "0"
5	LEN_LF_EN	0	R/W	Length area bit order setting 0: MSB first 1: LSB first (1)
4	DATA_LF_EN	0	R/W	DATA area bit order setting 0: MSB first 1: LSB first
3	RX_EXTPKT_EN	0	R/W	RX Extended Link Layer mode setting (Wireless M-bus) 0: Automatically detecting “Extended Link Layer”. 1: HW does not check “Extended Link Layer” automatically.
2	Reserved	0	R/W	
1:0	PKT_FORMAT[1:0]	00	R/W	Extended Link Layer mode setting (Wireless M-bus) 00: Format A (Wireless M-bus) (2) 01: Format B (Wireless M-bus) 10: Format C (non Wireless M-bus, general purpose format) 11: Reserved Please refer to the “Packet Format”.

NOTE:

1. If setting LSB first (LEN_LF_EN=0b1), the length value should be 63 bytes or less. If the length value is 64byte or more, TX/RX operation is not possible. [ML7344J]
2. If PKT_FORMAT=0b00, the length value should be 13 bytes or more. If the length value is 12 bytes or less, TX/RX operation is not possible [ML7344J]

0x05[PKT_CTRL2]

Function: Packet configuration 2
Address: 0x05 (BANK0)
Defalut value: 0x1C

Bit	Bit name	Reset Value	R/W	Description
7	CRC_INT_SEL	0	R/W	CRC initialized state setting 0: all "0" setting 1: all "1" setting
6	CRC_COMP_OFF	0	R/W	CRC complement value OFF setting 0: Complement value 1: no complement value
5:4	CRC_LEN[1:0]	01	R/W	CRC length setting 00: CRC8 01: CRC16 10: CRC32 11: Reserved Note: 0b00(CRC8) and 0b01(CRC16) are valid for Format C only. For details, please refer to the "CRC Function".
3	RX_CRC_EN	1	R/W	RX CRC setting 0: disable 1: enable (CRC calculation) Note: If enable, CRC results are stored in [CRC_ERR_H/M/L:B0 0x13/14/15] registers.
2	TX_CRC_EN	1	R/W	TX CRC setting 0: disable 1: enable (CRC calculation) Note: If enable, CRC(s) are automatically appended to the TX data. If meet the floowing conditons, TX FIFO access error interrupt is set. You contorol size of last wirte data to TX FIFO to avoid this interrupt is set. TX_CRC_EN = 0b0 and CRC_LEC = 0b00 and size of a last wirte data to TX FIFO is 1byte TX_CRC_EN = 0b0 and CRC_LEC = 0b01 and size of a last wirte data to TX FIFO is equal to or less than 2bytes. TX_CRC_EN = 0b0 and CRC_LEC = 0b10 and size of a last wirte data to TX FIFO is equal to or less than 4bytes.
1	Reserved	0	R/W	
0	LENGTH_MODE	0	R/W	Length field setting 0: 1 byte mode 1: 2 byte mode (length extended upper 3 bits) Other setting: prohibit

Description:

1. In transmission (TX), based on the length from [TX_PKT_LEN_H/L:B0 0x7A/7B] registers, total data lenth will be calculated. Upon transmitting all data, TX complete.
2. In receiving (RX), based on the the length from RX data, total data lenth will be calculated. Upon reception of all data, RX complete.
3. For details, please refer to the "Packet Format".

0x06[DRATE_SET]

Function: Data rate setting
Address: 0x06 (BANK0)
Defalut value: 0x33

<table>
<tr><th>Bit</th><th>Bit name</th><th>Reset Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>7:4</td><td>RX_DRATE[3:0]</td><td>0011</td><td>R/W</td><td>RX data rate setting
<table><tr><th>Setting</th><th>Data rate</th></tr><tr><td>0000</td><td>1.2 kbps</td></tr><tr><td>0001</td><td>2.4 kbps</td></tr><tr><td>0010</td><td>4.8 kbps</td></tr><tr><td>0011</td><td>9.6 kbps</td></tr><tr><td>0100</td><td>10 kbps</td></tr><tr><td>0101</td><td>11.52 kbps (1)</td></tr><tr><td>0110</td><td>15 kbps</td></tr><tr><td>Other setting</td><td>reserved</td></tr></table>Note: If LOW_RATE_EN ([CLK_SET2:B0 0x03(0)])=0b0, by setting this field, optimal values automatically set to the [RX_LATE1_H/L:B1 0x04/05] and [RX_LATE2:B1 0x06] registers.
Note: If LOW_RATE_EN=0b1, optimal values are not set. It is need to set specified values directly to the [RX_LATE1_H/L:B1 0x04/05] and [RX_LATE2:B1 0x06] registers according to the “Initialization table”.
Note: If RXDIO_CTRL[1:0]([DIO_SET:B0 0x0C(7-6)])=0b10 (enabling DIO mode), less than or equal 9.6kbps can not be used by setting this register. It is need to set specified values directly to the [RX_LATE1_H/L:B1 0x04/05] and [RX_LATE2:B1 0x06] registers according to the “Initialization table”.</td></tr>
<tr><td>3:0</td><td>TX_DRATE[3:0]</td><td>0011</td><td>R/W</td><td>TX data rate setting
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</table>

NOTE:

(1) 11.52kbps data rate can not beRx low rate clock mode (LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1) cannot be used with this data rate..

0x07[DATA_SET1]

Function: TX/RX data configuration 1
Address: 0x07 (BANK0)
Defalut value: 0x15

Bit	Bit name	Reset Value	R/W	Description
7	TX_PAT	0	R/W	TX preamble pattern setting 0: “01” pattern 1: “10” pattern
6	TX_FSK_POL	0	R/W	TX data polarity setting 0: data “1”= deviated to high frequency data “0” = deviated to low frequency 1: data ”1”= deviated to low frequency data “0”= deviated to high frequency
5	RX_FSK_POL	0	R/W	TX data polarity setting 0: data “1”= deviated to high frequency data “0” = deviated to low frequency 1: data ”1”= deviated to low frequency data “0”= deviated to high frequency
4	GFSK_EN	1	R/W	GFSK mode setting 0: GFSK disable (FSK mode) 1: GFSK enable For details, please refer to the “Modulation setting)
3:2	RX_DEC_SCHEME[1:0]	01	R/W	RX data coding mode setting 00: Manchester coding 01: NRZ coding 10: 3-out-of-6 coding 11: reserved
1:0	TX_DEC_SCHEME[1:0]	01	R/W	TX data coding mode setting 00: Manchester coding 01: NRZ coding 10: 3-out-of-6 coding 11: reserved

0x08[DATA_SET2]

Function: TX/RX data configuration 2
Address: 0x08 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:5	Reserved	000	R/W	
4	SYNCWORD_SEL	0	R/W	SyncWord pattern selection setting 0: SyncWord pattern 1 1: SyncWord pattern 2 For details, please refer to the “SyncWord detection function”.
3	2SW_DET_EN	0	R/W	Two SyncWord search setting 0: 2 SyncWords searching disable 1: 2 SyncWords searching enable
2	2PB_DET_EN	0	R/W	Two RX preamble search setting 0: 2 preamble pattern searching disable (distinguish between “01” pattern and “10” pattern.) 1: 2 preamble pattern searching enable (do not distinguish between “01” pattern and “10” pattern.)
1	MAN_POL	0	R/W	Manchester polarity setting 0: do not inverse polarity 1: inverse polarity
0	WHT_SET	0	R/W	Whitening setting 0: disable whitening 1: enable whitening

0x09[CH_SET]

Function: RF channel setting
Address: 0x09 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	RF_CH[7:0]	0000_0000	R/W	RF channel setting (setting range 0 to 255) For details. Please refer to the “Channel frequency setting”.

0x0A[RF_STATUS_CTRL]

Function: RF suto status transition control
Address: 0x0A (BANK0)
Defalut value: 0x08

Bit	Bit name	Reset Value	R/W	Description
7-6	Reserved	00	R/W	
5	FAST_TX_EN	0	R/W	FAST_TX mode setting 0: disable FAST_TX mode 1: enable FAST_TX mode Note: If enable, move to the TX state after the data bytes written into the TX_FIFO becomes greater than the value specified by TXFIFO_THRL[5:0] ([TXFIFO_THRL: B0 0x18 (5–0)]).
4	AUTO_TX_EN	0	R/W	Automatic TX mode setting 0: disable automatic TX mode 1: enable automatic TX mode Note: If enable, TX data specified by the length are written to the TX FIFO, move to the TX state.
3:2	RXDONE_MODE[1:0]	10	R/W	RF state setting after packet reception completion. 00: move to IDLE state (TRX_OFF) 01: move to TX state 10: continue RX state 11: move to SLEEP state
1:0	TXDONE_MODE[1:0]	00	R/W	RF state setting after packet transmission completion. 00: move to IDLE state (TRX_OFF) 01: continue TX state 10: move to RX state 11: move to SLEEP state

Description:

1. For details, please refer to the “LSI state transition control”.

0x0B[RF_STATUS]

Function: RF state setting and status indication
Address: 0x0B (BANK0)
Defalut value: 0x88

Bit	Bit name	Reset Value	R/W	Description
7:4	GET_TRX[3:0]	1000	R	RF status indication 0110: RX_ON (RX state) 1000: TRX_OFF (RF_OFF state) 1001: TX_ON (TX State) Other setting: reserved
3:0	SET_TRX[3:0]	1000	R/W	RF state setting 0011: Force_TRX_OFF (Force RF_OFF setting) 0110: RX_ON (RX setting) (*1) 1000: TRX_OFF (RF_OFF setting) (*3) 1001: TX_ON (TX setting) (*2) Other setting: prohibit (no state change) (*1) During TX operation, setting RX_ON is possible. In this case, after TX completion, move to RX_ON state automatically. (*2) During RX operation, setting TX_ON is possible. In this case, after RX completion, move to TX_ON state automatically. (*3) If TRX_OFF is selected during TX or RX operation, after TX or RX completion, move to TRX_OFF state automatically. If Force_TRX_OFF is selected during TX or RX operation, move to TRX_OFF state immediately.

Description:

1. For details, please refer to the “LSI state transition control”.

0x0C[DIO_SET]

Function: DIO mode configuration
Address: 0x0C (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	RXDIO_CTRL[1:0]	00	R/W	RF status indication 00: disable DIO mode (FIFO mode) 01: continuous output mode DIO (demodulated data) and DCLK are constantly output 10: data output mode 1 DIO (undecoded data) and DCLK are output after SyncWord detection. 11: data output mode 2 DIO (decoded data) and DCLK are output after L-field detection. Note: When measurement BER, set to 0b01. Note: If 0b10, as FIFO is used for storing undecoded RX data. By setting bit0 (DIO_START)=0b1, DIO and DCLK are output. Data after SyncWord is stored into FIFO. Note: If 0b11, as FIFO is used for storing decoded RX data. By setting bit0 (DIO_START)=0b1, DIO and DCLK are output. Upon completion of data (specified by the Length) transferring, DIO and DCK output are stop. Data after Length field is stored into FIFO.
5:4	TXDIO_CTRL[1:0]	00	R/W	TX DIO mode setting 00: disable DIO mode (FIFO mode) 01: DCLK is constantly output 10: DCLK is output after SyncWord detection 11: Reserved Note: When setting 0b01 or 0b10. FIFO cannot be used. Encoded data must be sent to ML7344 at the falling edge of DCLK.
3	Reserved	0	R/W	
2	DIO_RX_COMPLETE	0	R/W	DIO RX completion setting 0: RX not finished 1: RX completion Note: After RX completion, reset to “0b0” automatically.
1	Reserved	0	R/W	
0	DIO_START	0	R/W	DIO RX data output start setting 0: no OUTPUT (NOT stop output) 1: start OUTPUT Note: Upon out of synchronization, reset to “0b0”.

Description:

1. For details, please refer to the “DIO function”.

0x0D[INT_SOURCE_GRP1]

Function: Interrupt status for INT0 to INT7
Address: 0x0D (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	INT[7]	0	R/W	Clock calibration completion interrupt 0: no interrupt 1: interrupt
6	INT[6]	0	R/W	Wake-up timer completion interrupt 0: no interrupt 1: interrupt Note: if this interrupt is cleared during SLEEP state, interrupt by wake-up timer completion will not generate.
5	INT[5]	0	R/W	FIFO-Full interrupt 0: no interrupt 1: interrupt Note: Interrupt will generate, if FIFO usage becomes threshold defined by TXFIFO_THRH[5:0] ([TXFIFO_THRH: B0 0x17(5-0)]) in TX or RXFIFO_THRH[5:0] ([RXFIFO_ THRH: B0 0x19(5-0)]) in RX.
4	INT[4]	0	R/W	FIFO-Empty interrupt 0: no interrupt 1: interrupt Note: Interrupt will generate, if FIFO usage is above threshold defined by TXFIFO_THRL[5:0]([TXFIFO_THRL: B0 0x18(5-0)]) in TX or RXFIFO_THRH[5:0] ([RXFIFO_ THRL: B0 0x1A(5-0)]) in RX.
3	INT[3]	0	R/W	RF state transition completion interrupt 0: no interrupt 1: interrupt
2	INT[2]	0	R/W	PLL unlock interrupt or VCO CAL request interrupt 0: no interrupt 1: interrupt (unlock) Note: when VTUNE_INT_ENB([VCO_VTRSLT:B0 0x40(2)]) =0b1, VCO CAL request interrupt is activated.
1	INT[1]	0	R/W	VCO calibration completion interrupt 0: no interrupt 1: interrupt (VCO calibration completed)
0	INT[0]	0	R/W	Clock stabilization completion interrupt 0: no interrupt 1: interrupt (Clock is stabilized)

Note:

1. Regardless of [INT_EN_GRP1: B0 0x10] register setting, this register value reflect internal status. For writing only 0b0 is valid, writing 0b1 is ignored.
2. If one of unmasked interrupt element occur, interrupt pin keeps output “Low”.
3. During SLEEP state, interupts are not cleared immediately by this register. In this case, interrupts are cleared at the clock stabilizzation completion timing after return from the SLEEP state.
   If need to clear interrupts during SLEEP state, please use [SLEEP_INT_CLR:B0 0x75] register.

0x0E[INT_SOURCE_GRP2]

Function: Interrupt status for INT8 to INT15 (RX)
Address: 0x0E (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	INT[15]	0	R/W	Sync error interrupt 0: no interrupt 1: interrupt
6	INT[14]	0	R/W	Field checking interrupt 0: no interrupt 1: interrupt
5	INT[13]	0	R/W	SyncWord detection interrupt 0: no interrupt 1: interrupt
4	INT[12]	0	R/W	RX FIFO access error interrupt 0: no interrupt 1: interrupt Note: During RX using FIFO mode, if the FIFO overrun or under-run detected, interrupt will generate.
3	INT[11]	0	R/W	RX Length error interrupt 0: no interrupt 1: interrupt
2	INT[10]	0	R/W	Reserved
1	INT[9]	0	R/W	CRC error interrupt 0: no interrupt 1: interrupt Note: Interrupt will generate when detecting CRC error. As Format A and B have multiple CRC field, error CRC block is indicated by [CRC_ERR_H/M/L: B0 0x13/14/15] registers. Format C has only one CRC field. Therefore MCU can detect CRC error with this interruption.
0	INT[8]	0	R/W	RX completion interrupt 0: no interrupt 1: interrupt Note: Interrupt will generate when RX data, specified by the L-field, received

Description:

(1) If the following L-field data is received, RX Length error interruption will generate

Packet format [PKT_CTRL1: B0 0x04]	Extension format [PKT_CTRL1: B0 0x04]	Length Indicating RX Length error
Format A	No extension	Under 8 byte
	2 byte extension	Under 12 byte
	8 byte extension	Under 16 byte
Format B	No extension	Under 10 byte, 128 to 129 byte
	2 byte extension	
	8 byte extension	Under 17 byte, 19 to 20 byte, 128 to 129 byte
Format C	-	0 byte (CRC8) 1 byte (CRC16) 2 byte (CRC32)

Note:

1. Regardless of [INT_EN_GRP2: B0 0x11], this register value reflect internal status. For writing only 0b0 is, writing 0b1 is ignored.
2. If one of unmasked interrupt event occur, interrupt pin keeps output “Low”.
3. During SLEEP state, interupts are not cleared immediately by this register. In this case, interrupts are cleared at the clock stabilizzation completion timing after return from the SLEEP state.
   If need to clear interrupts during SLEEP state, please use [SLEEP_INT_CLR:B0 0x75] register.

0x0F[INT_SOURCE_GRP3]

Function: Interrupy status for INT16 to INT23 (TX)
Address: 0x0F (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	INT[23]	0	R/W	General purpose timer 2 interrupt 0: no interrupt 1: interrupt
6	INT[22]	0	R/W	General purpose timer 1 interrupt 0: no interrupt 1: interrupt
5	INT[21]	0	R/W	Reserved
4	INT[20]	0	R/W	TX FIFO access error interrupt 0: no interrupt 1: interrupt Note: interrupt will generate at following cases during TX using FIFO mode. 1) FIFO overrun or underrun detected 2) The next packet data is written to the FIFO before transmitting.
3	INT[19]	0	R/W	TX Length error interrupt (1) 0: no interrupt 1: interrupt
2	INT[18]	0	R/W	CCA completion interrupt 0: no interrupt 1: interrupt
1	INT[17]	0	R/W	TX Data request accept completion interrupt 0: no interrupt 1: interrupt Note: Interrupt will generated when TX data, whose length specified by the [TX_PKT_LEN_H/L: B0 0x7A/7B] registers, written to the FIFO.
0	INT[16]	0	R/W	TX completion interrupt 0: no interrupt 1: interrupt Note: Interrupt will generated when TX data, whose length specified by the [TX_PKT_LEN_H/L: B0 0x7A/7B] registers, transmitted.

Description:

(1) If the following L-field data is written to the [TX_PKT_LEN_H/L: B0 0x7A/7B] registers, TX Length error interruption will generate.

Packet format [PKT_CTRL1: B0 0x04]	Extension format [PKT_CTRL1: B0 0x04]	Length Indicating RX Length error
Format A	No extension	Under 8 byte
	2 byte extension	Under 12 byte
	8 byte extension	Under 16 byte
Format B	No extension	Under 10 byte, 128 to 129 byte
	2 byte extension	
	8 byte extension	Under 17 byte, 19 to 20 byte, 128 to 129 byte
Format C	-	0 byte (CRC8) 1 byte (CRC16) 2 byte (CRC32)

Note:

1. Regardless of [INT_EN_GRP3: B0 0x12], this register value reflect internal status. For writing only 0b0 is, writing 0b1 is ignored.
2. If one of unmasked interrupt event occur, interrupt pin keeps output “Low”.
3. During SLEEP state, interupts are not cleared immediately by this register. In this case, interrupts are cleared at the clock stabilizzation completion timing after return from the SLEEP state.
   If need to clear interrupts during SLEEP state, please use [SLEEP_INT_CLR:B0 0x75] register.

0x10[INT_EN_GRP1]

Function: Interrrupt mask for INT0 to INT7
Address: 0x10 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	INT_EN[7:0]	0000_0000	R/W	Enabling from interrupt 0 event to interrupt 7 event 0: masking interrupt 1: generate interrupt

Note:

1. Please refer to the “interrupt events tabkle”.
2. For event details, please refer to the [INT_SOURCE_GRP1: B0 0x0D] register.

0x11[INT_EN_GRP2]

Function: Interrrupt mask for INT8 to INT15
Address: 0x11 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	INT_EN[15:8]	0000_0000	R/W	Enabling from interrupt 8 event to interrupt 15 event 0: masking interrupt 1: generate interrupt

Note:
1. Please refer to the "interrupt events tabkle".
2. For event details, please refer to the [INT_SOURCE_GRP2: B0 0x0E] register.

0x12[INT_EN_GRP3]

Function: Interrrupt mask for INT16 to INT23
Address: 0x12 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	INT_EN[23:16]	0000_0000	R/W	Enabling from interrupt 16 event to interrupt 23 event 0: masking interrupt 1: generate interrupt

Note:
1. Please refer to the "interrupt events tabkle".
2. For event details, please refer to the [INT_SOURCE_GRP3: B0 0x0F] register.

0x13[CRC_ERR_H]

Function: CRC error status (high byte)
Address: 0x13 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:1	Reserved	0000_000	R/W	
0	CRC_ERR[16]	0	R	17^{th} CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)

Description:
1. Please refer to the the "CRC function".

0x14[CRC_ERR_M]

Function: CRC error status (middle byte)
Address: 0x14 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	CRC_ERR[15]	0	R	16th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
6	CRC_ERR[14]	0	R	15th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
5	CRC_ERR[13]	0	R	14th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
4	CRC_ERR[12]	0	R	13th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
3	CRC_ERR[11]	0	R	12th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
2	CRC_ERR[10]	0	R	11th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
1	CRC_ERR[9]	0	R	10th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
0	CRC_ERR[14]	0	R	9th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)

Description:

1. Please refer to the the “CRC function”.

0x15[CRC_ERR_L]

Function: CRC error status (low byte)
Address: 0x15 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	CRC_ERR[7]	0	R	8th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
6	CRC_ERR[6]	0	R	7th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
5	CRC_ERR[5]	0	R	6th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
4	CRC_ERR[4]	0	R	5th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
3	CRC_ERR[3]	0	R	4th CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A (Wireless M-Bus)
2	CRC_ERR[2]	0	R	3rd CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A or B (Wireless M-Bus)
1	CRC_ERR[1]	0	R	2nd CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A or B (Wireless M-Bus)
0	CRC_ERR[0]	0	R	1st CRC error status 0: CRC OK or no CRC calculation 1: CRC error Note: for Format A or B (Wireless M-Bus)

Description:

1. Please refer to the the “CRC function”.

0x16[SATE_CLR]

Function: State clear control
Address: 0x16 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	STATE_CLR_EN	0	R/W	State clear enable setting 0: disable State clear 1: enable State clear Note: State clear bit0-4 can be enabled depending on this bit.
6-5	Reserved	0	R/W	
4	STATE_CLR4	0	R/W	Address check counter clear 1: Clear address check counter Note: [ADDR_CHK_CTR_H/L:B1 0x62,63] registers will be cleared. Note: bit78STATE_CLR_EN)=0b1 is required. After clear operation and then automatically return to 0b0
3	STATE_CLR3	0	R/W	Reserved
2	STATE_CLR2	0	R/W	PHY state clear 1: Clear PHY state Note: bit78STATE_CLR_EN)=0b1 is required. After clear operation and then automatically return to 0b0
1	STATE_CLR1	0	R/W	RX FIFO pointer clear 1: Clear write pointer and read pointer of RX FIFO. Note: bit78STATE_CLR_EN)=0b1 is required. After clear operation and then automatically return to 0b0
0	STATE_CLR0	0	R/W	TX FIFO pointer clear 1: Clear write pointer and read pointer of TX FIFO. Note: bit78STATE_CLR_EN)=0b1 is required. After clear operation and then automatically return to 0b0

Description:

1. Please set enable bit (bit7) and execution bits (bit4-0) at the same time. After completing a clearing operation, automatically 0b0 will be written to eacj bit.
2. After writing to the execution bits (bit4-0), clearing will be completed within the following time.
   Clearing time = master clock period (26MHz) * [RX_RATE1_H/L: B1 0x04/05] * 2 [us]

0x17[TXFIFO_THRH]

Function: TX FIFO-Full level setting
Address: 0x17 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	TXFIFO_THRH_EN	0	R/W	TX FIFO Full level enable setting 0: disable 1: enable
6	Reserved	0	R/W	
5-0	TXFIFO_THRH[5:0]	0	R/W	TX FIFO Full level setting Note: valid, if bit 7 (TXFIFO_THRH_EN)=0b1

Description:

1. For details, please refer to the “TX FIFO usage notification function”.
2. When TX FIFO data size exceeds the full level, INT[5] (group 1) will generate.

0x18[TXFIFO_THRL]

Function: TX FIFO-Empty level setting and TX trigger level setting in FST_TX mode
Address: 0x18 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	TXFIFO_THRL_EN	0	R/W	TX FIFO Empty level enable setting 0: disable 1: enable
6	Reserved	0	R/W	
5-0	TXFIFO_THRL[5:0]	0	R/W	TX FIFO Empty level setting and TX trigger level setting in FAST_TX mode Note: valid, if bit 7 (TXFIFO_THRL_EN)=0b1. Note: Empty level should be set greater or equal 1. Note: If using FAST_TX mode, please set 0b1 to the FAST_TX_EN ([RF_STATUS_CTRL: B0 0x0A(5)]). Empty level should be set less than or equal [FIFO write size(byte) -3(byte)].

Description:

1. For details, please refer to the “TX FIFO usage notification function”.
2. When TRX FIFO data size becomes below the empty level, INT[4] (group 1) will generate.

[Note]

1. For TX trigger level setting in FAST TX mode, please control so that the FIFO write amount has the relationship shown in the below table. If the following relationship is not satisfied, there is a possibility of unintentional transmission.

FAST_TX trigger level[Bytes]	FIFO write amount [Bytes]
1～2	1
3～6	1～3
7～14	1～7
15～30	1～15
31～62	1～31
63	1～63

0x19[RXFIFO_THRH]

Function: RX FIFO-Full level setting
Address: 0x19 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	RXFIFO_THRH_EN	0	R/W	RX FIFO Full level enable setting 0: disable 1: enable
6	Reserved	0	R/W	
5-0	RXFIFO_THRH[5:0]	0	R/W	RX FIFO Full level setting Note: valid, if bit 7 (RXFIFO_THRH_EN)=0b1

Description:

1. For details, please refer to the “RX FIFO usage notification function”.
2. When RX FIFO data size exceeds the full level, INT[5] (group 1) will generate.

0x1A[RXFIFO_THRL]

Function: RX FIFO-Empty level setting
Address: 0x1A (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	RXFIFO_THRL_EN	0	R/W	RX FIFO Empty level enable setting 0: disable 1: enable
6	Reserved	0	R/W	
5-0	RXFIFO_THRL[5:0]	0	R/W	RX FIFO Empty level setting Note: valid, if bit 7 (TXFIFO_THRH_EN)=0b1 Empty level should be set greater than 2.

Description:

1. For details, please refer to the “RX FIFO usage notification function”.
2. When RX FIFO data size becomes below the empty level, INT[4] (group 1) will generate.

0x1B[C_CHECK_CTRL]

Function: Control field detection setting
Address: 0x1B (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	CA_RXD_CLR	0	R/W	Data processing if Field mismatch 0: continue receiving RX data 1: RX data abort Note: if 0b0 is set, immediately abort RX data and wait for the next RX packet.
6	CA_INT_CTRL	0	R/W	Field check interrupt setting 0: generate interrupt if Field match 1: generate interrupt if Field mismatch Note: selected interrupt will become INT[14] (group 2).
5	ML7344J Reserved	0	R/W	
	ML7344C RCV_CONT_SEL			Reception continuation condition setting 0: Continue receiving by interrupt of Sync Word detection 1: Continue receiving by interrupt of Field checking
4	C_FIELD_CODE5_EN	0	R/W	Control field code #5 check enable 0: disable 1: enable Note: The pattern 5 has specific function. If received Control field data matches with the pattern 5, immediately generate interrupt and following M-field and A-field check do not proceed. Field mismatch interrupt will not generate.
3	C_FIELD_CODE4_EN	0	R/W	Control field code #4 check enable 0: disable 1: enable
2	C_FIELD_CODE3_EN	0	R/W	Control field code #3 check enable 0: disable 1: enable
1	C_FIELD_CODE2_EN	0	R/W	Control field code #2 check enable 0: disable 1: enable
0	C_FIELD_CODE1_EN	0	R/W	Control field code #1 check enable 0: disable 1: enable

Description:

1. For details, please refer to the “Field check function”.
2. When using field check function, RXDIO_CTRL[1:0] ([DIO_SET:B0 0x0C(7-6)]) =0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required.

0x1C[M_CHECK_CTRL]

Function: Manufacture ID field detection setting
Address: 0x1C (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-4	Reserved	0000	R/W	
3	M_FIELD_CODE4_EN	0	R/W	Manufacture ID field 2nd byte of code #2 check enable 0: disable 1: enable
2	M_FIELD_CODE3_EN	0	R/W	Manufacture ID field 2nd byte of code #1 check enable 0: disable 1: enable
1	M_FIELD_CODE2_EN	0	R/W	Manufacture ID field 1st byte of code #2 check enable 0: disable 1: enable
0	M_FIELD_CODE1_EN	0	R/W	Manufacture ID field 1st byte of code #1 check enable 0: disable 1: enable

Description:

1. For details, please refer to the “Field check function”.
2. When using field check function, RXDIO_CTRL[1:0] ([DIO_SET:B0 0x0C(7-6)]) =0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required.

0x1D[A_CHECK_CTRL]

Function: Address field detection setting
Address: 0x1D (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-6	Reserved	00	R/W	
5	A_FIELD_CODE6_EN	0	R/W	Address field 6th byte check enable 0: disable 1: enable
4	A_FIELD_CODE5_EN	0	R/W	Address field 5th byte check enable 0: disable 1: enable
3	A_FIELD_CODE4_EN	0	R/W	Address field 4th byte check enable 0: disable 1: enable
2	A_FIELD_CODE3_EN	0	R/W	Address field 3rd byte check enable 0: disable 1: enable
1	A_FIELD_CODE2_EN	0	R/W	Address field 2nd byte check enable 0: disable 1: enable
0	A_FIELD_CODE1_EN	0	R/W	Address field 1st byte check enable 0: disable 1: enable

Description:

1. For details, please refer to the “Field check function”.
2. When using field check function, RXDIO_CTRL[1:0] ([DIO_SET:B0 0x0C(7-6)]) =0b00 (FIFO mode) or 0b11 (data output mode 2) setting is required.

0x1E[C_FIELD_CODE1]

Function: Contor field setting (code #1)
Address: 0x1E (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	C_FIELD_CODE1[7:0]	0000_0000	R/W	C-field setting code #1

Description:

1. For details, please refer to the “Field check function”.

0x1F[C_FIELD_CODE2]

Function: Contor field setting (code #2)
Address: 0x1F (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	C_FIELD_CODE1[7:0]	0000_0000	R/W	C-field setting code #2

Description:

1. For details, please refer to the “Field check function”.

0x20[C_FIELD_CODE3]

Function: Contor field setting (code #3)
Address: 0x20 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	C_FIELD_CODE1[7:0]	0000_0000	R/W	C-field setting code #3

Description:

1. For details, please refer to the “Field check function”.

0x21[C_FIELD_CODE4]

Function: Contor field setting (code #4)
Address: 0x21 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	C_FIELD_CODE1[7:0]	0000_0000	R/W	C-field setting code #4

Description:

1. For details, please refer to the “Field check function”.

0x22[C_FIELD_CODE5]

Function: Contor field setting (code #5)
Address: 0x22 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	C_FIELD_CODE1[7:0]	0000_0000	R/W	C-field setting code #5

Description:

1. For details, please refer to the “Field check function”.

0x23[M_FIELD_CODE1]

Function: Manufacture ID 1st byte setting (code #1)
Address: 0x23 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	M_FIELD_CODE1[7:0]	0000_0000	R/W	M-field 1st byte setting code #1

Description:
1. For details, please refer to the “Field check function”.

0x24[M_FIELD_CODE2]

Function: Manufacture ID 1st byte setting (code #2)
Address: 0x24 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	M_FIELD_CODE2[7:0]	0000_0000	R/W	M-field 1st byte setting code #2

Description:
1. For details, please refer to the “Field check function”.

0x25[M_FIELD_CODE3]

Function: Manufacture ID 2nd byte setting (code #1)
Address: 0x25 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	M_FIELD_CODE3[7:0]	0000_0000	R/W	M-field 2nd byte setting code #1

Description:
1. For details, please refer to the “Field check function”.

0x26[M_FIELD_CODE4]

Function: Manufacture ID 2nd byte setting (code #2)
Address: 0x26 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	M_FIELD_CODE4[7:0]	0000_0000	R/W	M-field 2nd byte setting code #2

Description:
1. For details, please refer to the “Field check function”.

0x27[A_FIELD_CODE1]

Function: Address field 1st byte setting
Address: 0x27 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	A_FIELD_CODE1[7:0]	0000_0000	R/W	A-field setting (1st byte)

Description:

1. For details, please refer to the “Field check function”.

0x28[A_FIELD_CODE2]

Function: Address field 2nd byte setting
Address: 0x28 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	A_FIELD_CODE2[7:0]	0000_0000	R/W	A-field setting (2nd byte)

Description:

1. For details, please refer to the “Field check function”.

0x29[A_FIELD_CODE3]

Function: Address field 3rd byte setting
Address: 0x29 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	A_FIELD_CODE3[7:0]	0000_0000	R/W	A-field setting (3rd byte)

Description:

1. For details, please refer to the “Field check function”.

0x2A[A_FIELD_CODE4]

Function: Address field 4th byte setting
Address: 0x2A (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	A_FIELD_CODE4[7:0]	0000_0000	R/W	A-field setting (4th byte)

Description:

1. For details, please refer to the “Field check function”.

0x2B[A_FIELD_CODE5]

Function: Address field 5th byte setting
Address: 0x2B (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	A_FIELD_CODE5[7:0]	0000_0000	R/W	A-field setting (5th byte)

Description:

1. For details, please refer to the “Field check function”.

0x2C[A_FIELD_CODE6]

Function: Address field 6th byte setting
Address: 0x2C (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-0	A_FIELD_CODE6[7:0]	0000_0000	R/W	A-field setting (6th byte)

Description:

1. For details, please refer to the “Field check function”.

0x2D[SLEEP/WU_SET]

Function: SLEEP execution and Wake-up operation setting
Address: 0x2D (BANK0)
Defalut value: 0x08(ML7344J) / 0x0C(ML7344C)

Bit	Bit name	Reset Value	R/W	Description
7	WUT_1SHOT_MODE	0	R/W	Wake-up timer operation mode setting 0: continue interval operation 1: after 1-SHOT operation, stop the Wake-up timer
6	WAKEUP_MODE	0	R/W	After Wake-up operation setting 0: move to RX_ON 1: move to TX_ON Note: When the continue operation timer is time-out, move to the SLEEP state. Note: if TX FIFO is writen in the SLEEP state, TX Data request accept completion interrupt (INT[17] group 3) will generate after return from the SLEEP state. Note: When 0b1 is set, TX Data should be transmitted before time out of continue operation timer.
5	WU_DURATION_EN	0	R/W	Continue operation timer enable setting after Wake-up. 0: After Wake-up, do not start continue operation timer. [keep the state specified by WAKEIP_MODE (bit 6).] 1: After Wake-up, start continue operation timer. Note: When 0b1 is set and WAKEUP_MODE=0b0, if SyncWord or specified fields are not detected until continue operation time-out, automatically move to the SLEEP state.
4	WAKEUP_EN	0	R/W	Wake-up enable setting 0: disable Wake-up 1: enable Wake-up Note: When 0b1 is set, after wake-up timer is time-out, automatically recover from the SLEEP state. Move to the state specified by bit 6 (WAKEUP_MODE).
3	RCOSC_MODE	1	R/W	RC oscillation circuit operation mode setting 0: continuous operation 1: operation when in the SLEEP state Note: Please refer to the “SLEEP setting” Note: If 0b1 is set when continuous operation timer is used, continuous operation timer doesn’t work. Please set 0b0.
2	WUT_CLK_SOURCE	0	R/W	Wake-up timer clock setting 0: external clock source (EXT_CLK pin #10) 1: on-chip RC oscillation circuit Note: Please refer to the “SLEEP setting”
1	PDN_EN	0	R/W	Power supply control during the SLEEP state 0: all logic block power on 1: PHY/demodulator/FIFO block is power OFF Note: Please refer to the “SLEEP setting”.
0	SLEEP_EN	0	R/W	SLEEP mode setting 0: recover from the SLEEP state. (normal operation) 1: move to the SLEEP state Note: Please refer to the “SLEEP setting”,

Description: For details, please refer to the “Wake-up function”.

0x2E[WUT_CLK_SET]

Function: Wake-up timer clock division setting
Address: 0x2E (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:4	WUDT_CLK_SET[3:0]	0000	R/W	Continuous operation timer clock setting 0000: no division (ML7344xC prohibits this setting) 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 Other setting: divided by 16384 Note: The source clock is specified by WUT_CLK_SOURCE ([SLEEP/WU_SET: B0 0x2D(2)]) . Note: In case of using continuous operation timer, please set the same value as WUDT_CLK_SET as WUT_CLK_SET.
3:0	WUT_CLK_SET[3:0]	0000	R/W	Wake-up timer clock setting 0000: no division 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 Other setting: divided by 16384 Note: The source clock is specified by WUT_CLK_SOURCE ([SLEEP/WU_SET: B0 0x2D(2)]) .

Description:

1. For details, please refer to the “Wake-up function”.

0x2F[WUT_INTERVAL_H]

Function: Wake-up timer interval setting (high byte)
Address: 0x2F (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	WUT_INTERVAL[15:8]	0000_0000	R/W	Wake-up timer interval setting (high byte) Note: combined together with [WUT_INTERVAL_L:B0 0x30] register. Timer interval is programmed as follows: Wake-up timer interval = Wake-up timer cycle ([SLEEP/WU_SET:B0 0x2D(2)]) * Division setting ([WUT_CLK_SET]:B0 0x2E(3:0)]) * Wake-up timer interval [WUT_INTERVAL_H/L:B0 0x2F/30] Note: WUT_INTERVAL[15:0] should be set larger than or equal 2 .

Description:

1. For details, please refer to the “Wake-up function”.

0x30[WUT_INTERVAL_L]

Function: Wake-up timer interval setting (low byte)
Address: 0x30 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	WUT_INTERVAL[15:8]	0000_0000	R/W	Wake-up timer interval setting (high byte) For details, please refer to [WUT_INTERVAL_H:B0 0x2F] register

Description:

1. For details, please refer to the “Wake-up function”.

0x31[WU_DURATION]

Function: Continue operation timer (after Wake-up) setting
Address: 0x31 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	WU_DURATION[7:0]	0000_0000	R/W	Continuous operation timer (after wake-up setting Operation timer period is programmed as follows: Operation timer period = Wake-up timer clock cycle ([SLEEP/WU_SET:B0 0x2D(2)]) * Division setting ([WUT_CLK_SET]:B0 0x2E(7:4)]) * Continuous operation timer setting (WU_DURATION[7:0]) Note: WU_DURATION[7:0] should be set larger than or equal 1.

Description:

1. For details, please refer to the “Wake-up function”.

0x32[GT_SET]

Function: General purpose timer configuration
Address: 0x32 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7-6	Reserved	00	R/W	
5	GT2_CLK_SOURCE	0	R/W	General purpose timer #2 clock source setting 0: Wake-up timer clock 1: 2 MHz clock
4	GT2_START	0	R/W	General purpose timer #2 execution setting 0: pause timer counting 1: start or resume timer counting Note: After time-out, reset to 0b0 automatically.
3-2	Reserved	00	R/W	
1	GT1_CLK_SOURCE	0	R/W	General purpose timer #1 clock source setting 0: Wake-up timer clock 1: 2 MHz clock
0	GT1_START	0	R/W	General purpose timer #1 execution setting 0: pause timer counting 1: start or resume timer counting Note: After time-out, reset to 0b0 automatically.

Description:

1. For details, please refer to the “Genral purpose timer”.

0x33[GT_CLK_SET]

Function: General purpose timer clock division setting
Address: 0x33 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:4	GT2_CLK_SET[3:0]	0000	R/W	General purpose timer #2 clock setting 0000: no division 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 1000: divided by 16384 1001: divided by 32768 Other setting: divided by 65536 Note : The source clock is specified by GT2_CLK_SOURCE ([GT_SET: B0 0x32(5)]) .
3:0	GT1_CLK_SET[3:0]	0000	R/W	General purpose timer #1 clock setting 0000: no division 0001: divided by 128 0010: divided by 256 0011: divided by 512 0100: divided by 1024 0101: divided by 2048 0110: divided by 4096 0111: divided by 8192 1000: divided by 16384 1001: divided by 32768 Other setting: divided by 65536 Note : The source clock is specified by GT1_CLK_SOURCE ([GT_SET: B0 0x32(1)])

Description:

1. For details, please refer to the “Genral purpose timer”.

0x34[GT1_TIMER]

Function: General purpose timer #1 setting
Address: 0x34 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	GT1_TIMER[7:0]	0000_0000	R/W	General purpose timer #1 period setting General purpose timer #1 period is programmed as follows: General purpose timer #1 period = GT1 clock cycle ([GT_SET:B0 0x32(1)]) * Division setting ([WUT_CLK_SET]:B0 0x2E(3-0)]) * GT1 timer period (GT1_TIMER[7:0])

Description:

1. For details, please refer to the “Genral purpose timer”.

0x35[GT2_TIMER]

Function: General purpose timer #2 setting
Address: 0x35 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	GT2_TIMER[7:0]	0000_0000	R/W	General purpose timer #2 period setting General purpose timer #2 period is programmed as follows: General purpose timer #2 period = GT2 clock cycle ([GT_SET:B0 0x32(5)]) * Division setting ([WUT_CLK_SET]:B0 0x2E(7-4)]) * GT2 timer period (GT2_TIMER[7:0])

Description:

1. For details, please refer to the “Genral purpose timer”.

0x36[CCA_IGNORE_LVL]

Function: ED threshold level setting for excluding CCA judgement
Address: 0x36 (BANK0)
Defalut value: 0xFE

Bit	Bit name	Reset Value	R/W	Description
7:0	CCA_IGNORE_LVL[7:0]	1111_1110	R/W	ED threshold level setting for excluding CCA running average Note: An ED value exceeding this threshold, is not used for averaging defined by ED_AVG ([ED_CTRL:B0 0x41 (2-0)]). CCA result will not be judged until acquiring ED values reached averaging number. CCA_RST ([CCA_CTRL:B0 0x39(1-0)]) indicates 0b11 (evaluation on going)

Description:

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x37[CCA_LVL]

Function: CCA threshold level setting
Address: 0x37 (BANK0)
Defalut value: 0x18

Bit	Bit name	Reset Value	R/W	Description
7:0	CCA_LVL[7:0]	0001_1000	R/W	CCA threshold level setting (setting range: 0 to 255) Note: If an ED value exceeds this threshold, CCA_RST ([CCA_CTRL:B0 0x39(1-0)]) indicates 0b01 (carrier detected)

Description:

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x38[CCA_ABORT]

Function: Timing setting for forced termination of CCA operation
Address: 0x38 (BANK0)
Defalut value: 0xFF

Bit	Bit name	Reset Value	R/W	Description
7:0	CCA_ABORT[7:0]	1111_1111	R/W	CCA forced termination timing setting (setting range: 0 to 255) Note: If set b0000_0000, this function becomes invalid. Note: 1 but resolution is 128 μs Note: Time out function for avoiding the incompletion of CCA operation by carrier detection. If CCA operated period becomes the value defined by this register values * RSSI ADC clock setting (default: 18.5 μs). IDLE detection is terminated and packet is aborted, RF state become TRX_OFF Note: 18.5 μs is in case of ADC clock = 1.73MHz, If 2.17MHz is selected, register value * 14.8μs. Please refer [ADC_CLK_SET:B1 0x08] register.

Description:

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x39[CCA_CTRL]

Function: CCA control setting and result indication
Address: 0x39 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	CCA_STOP	0	R/W	CCA continuous mode termination setting (terminate by set 0b1) Note: If CCA_CPU_EN is executed, CCA will continuously perform until this bit is set to 0b1.
6	CCA_IDLE_EN	0	R/W	CCA IDLE detection mode enable setting 0: disable 1: enable
5	CCA_CPU_EN	0	R/W	CCA continuous mode enable setting 0: disable 1: enable Note: CCA will continue until terminated by CCA_STOP bit.
4	CCA_EN	0	R/W	CCA execution setting 0: not perform CCA 1: perform CCA Note: After completion of CCA, reset to 0b0 automatically
3	FAST_DET_MODE_EN	0	R/W	High speed carrier checking mode setting 0: during RX_ON, not perform CCA 1: during RX_ON, perform CCA Note: As a result of CCA, if no carrier found, automatically move to SLEEP state. Timer function can be combined together as well. For details, please refer to the “Wake-up timer”
2	CCA_ABORT_EN	0	R/W	CCA forced termination setting 0: do not terminate CCA 1: terminate CCA Note: valid if bit6(CCA_IDLE_EN)=0b1
1:0	CCA_RSLT[1:0]	00	R/W	CCA result indication 00: no carrier 01: carrier detected 10: CCA evaluation on-going (evaluating IDLE) 11: CCA evaluation on-going (ED value excluding CCA judgement acquisition.) Please refer [CCA_IGNORE_LVL:B0 0x36] register. Note: These bits are not cleared automatically. Every time CCA detects carrier, 0b00 should be set to clear these bits. Only 0b00 is valid for writing. CCA completion is indicated by INT[18] (group 3).

Description:

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”
2. Plase do not set 0b1 to both bit6(CCA_IDLE_EN) and bit5(CCA_CPU_EN) at the same time.

0x3A[ED_RSLT]

Function: ED value indication
Address: 0x3A (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	ED_VALUE[7:0]	0000_0000	R/W	ED value indication Note: If ED_RSLT_SET ([ED_CTRL:B0 0x41(3)])=0b0, ED value is updated constantly during RX_ON. If ED_RSLT_SET =0b1, ED value is acquired at SyncWord detection timing. The value updated by reading RX_FIFO.

Description:

1. For details of ED value auquisition operation, please refer to the "Energy detection value (ED value) acquisition function".

0x3B[IDLE_WAIT_H]

Function: IDLE detection period setting during CCA (high 2 bits)
Address: 0x3B (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:2	Reserved	0000_00	R/W	
1:0	IDLE_WAIT[9:8]	00	R/W	IDLE judgement max. wait time setting (high 2 bits) Note: In CCA IDLE judgement, it is used for detecting long IDLE (no carrier) period. Note: Combined together with [IDLE_WAIT_L:B0 0x3C] register IDLE detection period is programmed as follows: IDLE detection period = ED value averaging period (default 8 times = 148μs:) + (IDLE_WAIT [9:0] * 18.5 μs) Note: Above example is in case of ADC clock = 1.73MHz, If 2.17MHz is selected, IDLE_WAIT [9:0] * 14.8 μs and ED value averaging period becomes 118.4μs. Regarding ADC clock, please refer [ADC_CLK_SET:B1 0x08] register.

Description:

1. For details operation of CCA, please refer to the "CCA(Clear Channel Asessment) function".

0x3C[IDLE_WAIT_L]

Function: IDLE detection period setting during CCA (low byte)
Address: 0x3C (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	IDLE_WAIT[7:0]	0000_0000	R/W	IDLE judgement max. wait time setting (low byte) For details, please refer to [IDLE_WAIT_H:B0 0x3B] register.

Description:

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x3D[CCA_PROG_H]

Function: IDLE judgement elapsed time indication during CCA (high 2 bits)
Address: 0x3D (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:2	Reserved	0000_00	R/W	).
1:0	CCA_PROG[9:8]	00	R/W	IDLE judgement elapsed time indication (high 2 bits) Note: Combined together with [CCA_PROG_L:B0 0x3E] register. IDLE judgement elapsed time is calculated as follows: IDLE judgement elapsed time = ED value averaging period (default 8 times = 148μs:) + (CCA_PROG [9:0] * 18.5 μs) Note: Above example is in case of ADC clock = 1.73MHz, If 2.17MHz is selected, CCA_PROG [9:0] * 14.8 μs and ED value averaging period becomes 118.4μs. Regarding ADC clock, please refer [ADC_CLK_SET:B1 0x08] register.

Description:

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x3E[CCA_PROG_L]

Function: IDLE judgement elapsed time indication during CCA (low byte)
Address: 0x3E (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	IDLE_WAIT[7:0]	0000_0000	R/W	IDLE judgement max. wait time setting (low byte) For details, please refer to [CCA_PROG_H:B0 0x3D] register.

Description:

1. For details operation of CCA, please refer to the “CCA(Clear Channel Asessment) function”.

0x3F[Reserved]

Function:
Address: 0x3F (BANK0)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x40[VCO_VTRSLT]

Function: VCO voltage adjustment result indication
Address: 0x40 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:3	Reserved	0000_0	R/W	
2	VTUNE_INT_EN	0	R/W	VCO CAL(calibration) request interrupt enable setting 0: enable interrupt by INT[2] 1: disable interrupt Note: If enable, INT[2] will generate when PLL unlock occurs or VCO CAL request occurs by detecting VCO tuning voltage is out of control range.
1	VTUNE_COMP_H	0	R/W	VCO tuning voltage comparison result with maximum threshold 0: less than maximum threshold 1: more than or equal maximum threshold
0	VTUNE_COMP_L	0	R/W	VCO tuning voltage comparison result with minimum threshold 0: more than or equal minimum threshold 1: less than minimum threshold

0x41[ED_CTRL]

Function: ED detection control setting
Address: 0x41 (BANK0)
Defalut value: 0x80

Bit	Bit name	Reset Value	R/W	Description
7	ED_CAL_EN	1	R/W	ED value calculation enable setting 0: disable ED value calculation 1: enable ED value calculation
6:5	Reserved	00	R/W	
4	ED_DONE	0	R/W	ED value calculation completion flag 0: calculation on-going (not completed) 1: calculation completion
3	ED_RSLT_SET	0	R/W	ED indication setting in [ED_RSLT:B0 0x3A] register. 0: ED value constantly updated 1: ED value acquired at SyncWord detection timing Note: if 0b1 is set, the ED value is updated at reading RX_FIFO. Please read [ED_RSLT:B0 0x3A] register after reading RX_FIFO.
2:0	ED_AVG[2:0]	000	R/W	ED value calculation average times setting 000: 1 time 001: 2 times average 010: 4 times average 011: 8 times average 100: 16 times average 101: 32 :times average Other setting : 16 times average Note: ED_AVG[2:0] must be set when ED value calculation stop (TRX_OFF state or TX_ON state or bit7(ED_CAL_EN)=0b0),

Description:

1. For details of ED value auquisition operation, please refer to the “Energy detection value (ED value) acquisition function”.

0x42[TXPR_LEN_H]

Function: TX preamble length setting (high byte)
Address: 0x42 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	TXPR_LEN [15:8]	0000_0000	R/W	TX preamble length setting (high byte) TX preamble length = (specified value * 2) bits Note: combined together with [TXPR_LEN_L:B0 0x43] register. Note: Do not set value less than 0x0010 to TXPR_LEN[15:0]. ML7344 requires more than or equal 0x0010 preambles for synchronization. Note: if diversity is used, this parameter may have to change according to the data rate. Please refer to the “initialization table”.

0x43[TXPR_LEN_L]

Function: TX preamble length setting (low byte)
Address: 0x43 (BANK0)
Defalut value: 0x10

Bit	Bit name	Reset Value	R/W	Description
7:0	TXPR_LEN[7:0]	0001_0000	R/W	TX preamble length setting (low byte) For details, please refer to [TXPR_LEN_H:B0 0x42] register.

0x44[POSTAMBLE_SET]

Function: TX preamble length setting (high byte)
Address: 0x44 (BANK0)
Defalut value: 0x12

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:4	POSTAMBLE_LEN[2:0]	001	R/W	Postamble length setting (high byte) Postamble length = (specified value * 2) bits
3	Reserved	0	R/W	
2:1	POSTAMBLE_PAT[1:0]	01	R/W	Postamble pattern setting 00: “01” pattern repetition 01: “10” pattern repetition 10: repetition of the last CRC pattern and its inversion 11: reserved
0	POSTAMBLE_EN	0	R/W	Postamble enable setting 0: no postamble addition 1: postamble addition

0x45[SYNC_CONDITION1]

Function: RX preamble setting and ED threshold check setting
Address: 0x45 (BANK0)
Defalut value: 0x08

Bit	Bit name	Reset Value	R/W	Description
7	SYNC_ED_EN	0	R/W	ED threshold check enable setting during synchronization 0: disable ED threshold check during synchronization 1: enable ED threshold check during synchronization Note: ED threshold value is set to the [SYNC_CONDITION2:B0 0x46] register.
6	Reserved	0	R/W	
5:0	RXPR_LEN[5:0]	00_1000	R/W	RX preamble length setting (setting range: 0 to 32, unit: bit) Note: if larger than 0b10_0000, interpret as 0b10_0000 Note: when 1 or more value is set to this register, for syncword detection, syncword detection is performed with the pattern added to syncword pattern for the number of preambles set. If the false detection probability is high only with the syncword length, this function can reduce the probability by adding a preamble. Note: ML7344 requires AFC convergence time(Max 24 bits). If the preamble comparison length set in RXPR_LEN[5:0] overlaps the AFC convergence time, syncword can not be detected. Therefore, please set this register to a value equal to or less than the number of bytes obtained by subtracting the AFC convergence time from the transmission preamble.

0x46[SYNC_CONDITION2]

Function: ED threshold setting during synchronization
Address: 0x46 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_ED_TH[7:0]	0000_0000	R/W	ED threshold value setting during synchronization Note: if SYNC_ED_EN ([SYNC_CONDITION1:B0 0x45(7)])=0b1, ED threshold value becomes valid. Note: if acquired ED value does not exceed this threshold, synchronization is not detected.

0x47[SYNC_CONDITION3]

Function: Bit error tolerance setting during RX preamble and SyncWord detection
Address: 0x47 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:4	SW_RCV[3:0]	0000	R/W	Error tolerance value (bits) in the SyncWord (setting range: 0 to 15)
3:0	PB_RCV[3:0]	0000	R/W	Error tolerance value (bits) in RX preamble (setting range: 0 to 15)

0x48[2DIV_CTRL]

Function:Antenna diversity setting
Address:0x48 (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R/W	
5	ANT_CTRL1	0	R/W	ANT control bit 1
4	Reserved	0	R/W	
3	INV_ANT_SW	0	R/W	ANT_SW polarity setting
2	INV_TRX_SW	0	R/W	TRX_SW polarity setting
1:0	Reserved	00	R/W	

[Description]

1. For details, please refer to “antenna switching function”

0x49-0x4B[Reserved]

Function:
Address: 0x49-0x4B (BANK0)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x4C[ANT_CTRL]

Function:TX/RX antenna control setting
Address:0x4C (BANK0)
Reset value:0x00

Bit	Bit name	Reset value	R/W	Description
7:6	Reserved	00	R/W	
5	RX_ANT	0	R/W	Antenna setting for RX 0: antenna 1 1: antenna 2 (Note) Valid if bit4(RX_ANT_EN)=0b01. This bit defines antenna during RX_ON.
4	RX_ANT_EN	0	R/W	Antenna settinge enable for RX 0: disable 1: enable
3:2	Reserved	00	R/W	
1	TX_ANT	0	R/W	Antenna setting for TX 0: antenna 1 1: antenna 2 (Note) Valid If bit0(TX_ANT_EN)=0b01. This bit defines antenna during TX_ON.
0	TX_ANT_EN	0	R/W	Antenna settinge enable for TX 0: disable 1: enable

[Description]

1. For details, please refer to “antenna switching function”

0x4D[MON_CTRL]

Function: Monitor function setting
Address: 0x4D (BANK0)
Defalut value: 0x01

Bit	Bit name	Reset Value	R/W	Description
7	BER_MODE	0	R/W	BER measurement mode setting 0: normal operation mode 1: BER measurement mode Note: by setting BER measurement mode, demodulated data and clock output from DIO/DCLK pins. For details, please refer to the “BER measurement setting”
6	FIFOMODE_MON	0	R/W	FIFO mode monitor setting 0: FIFO mode and DIO/DCLK not out put 1: FIFO mode and DIO/DCLK output Note: Demodulate data and clock are output from DIO/DCLK pins.
5:4	Reserved	00	R/W	
3:0	DMON_SET	0001	R/W	Digital monitor output setting 0000: “L” output 0001: CLK_OUT output 0010: PLL lock detection signal output if PLL is locked, digital monitor signal outputs “H” 0011: Synchronization detection signal output if synchronization is completed, digital monitor signal outputs “H” Other setting: reserved

0x4E[GPIO0_CTRL]

Function: GPIO0 pin (pin #16) configuration setting
Address: 0x4E (BANK0)
Defalut value: 0x07

Bit	Bit name	Reset Value	R/W	Description
7	GPIO0_INV	0	R/W	GPIO0 output signal polarity setting
6	GPIO0_OD	0	R/W	GPIO0 output signal polarity setting
5	GPIO0_FORCEOUT	0	R/W	GPIO0 forced output value setting 0: "L" output 1: "H" output Note: the setting of bit7(GPIO0_INV) does not affect on this output value
4	GPIO0_FORCEOUTEN	0	R/W	GPIO0 forced output enable setting 0: disable 1: enable (output the value according to bit5 (GPIO0_FORCEOUT) setting.)
3	Reserved	0	R/W	
2:0	GPIO0_IO_CFG[2:0]	111	R/W	GPIO0 input-output signal setting 000: [output] "L" level 001: [output] antenna switch control signal 1 (TX-RX switch signal: TRX_SW) 010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 011: [output] external PA control signal 100: [input-output] data (DIO) 101: [output] data clock (DCLK) 110: [output] digital monitor signal Please refer DMON_SET[3:0] ([MON_CTRL:B0 0x4D(3-0)]). 111: [output] interrupt notification signal (SINT)

0x4F[GPIO1_CTRL]

Function: GPIO0 pin (pin #17) configuration setting
Address: 0x4F (BANK0)
Defalut value: 0x06

Bit	Bit name	Reset Value	R/W	Description
7	GPIO1_INV	0	R/W	GPIO1 output signal polarity setting
6	GPIO1_OD	0	R/W	GPIO1 output signal polarity setting
5	GPIO1_FORCEOUT	0	R/W	GPIO1 forced output value setting 0: "L" output 1: "H" output Note: the setting of bit7(GPIO1_INV) does not affect on this output value
4	GPIO1_FORCEOUTEN	0	R/W	GPIO1 forced output enable setting 0: disable 1: enable (output the value according to bit5 (GPIO1_FORCEOUT) setting.)
3	Reserved	0	R/W	
2:0	GPIO1_IO_CFG[2:0]	110	R/W	GPIO1 input-output signal setting 000: [output] "L" level 001: [output] antenna switch control signal 1 (TX-RX switch signal: TRX_SW) 010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 011: [output] external PA control signal 100: [input-output] data (DIO) 101: [output] data clock (DCLK) 110: [output] digital monitor signal Please refer DMON_SET[3:0] ([MON_CTRL:B0 0x4D(3-0)]). 111: [output] interrupt notification signal (SINT)

0x50[GPIO2_CTRL]

Function: GPIO2 pin (pin #18) configuration setting
Address: 0x50 (BANK0)
Defalut value: 0x02

Bit	Bit name	Reset Value	R/W	Description
7	GPIO2_INV	0	R/W	GPIO2 output signal polarity setting
6	GPIO2_OD	0	R/W	GPIO2 output signal polarity setting
5	GPIO2_FORCEOUT	0	R/W	GPIO2 forced output value setting 0: "L" output 1: "H" output Note: the setting of bit7(GPIO2_INV) does not affect on this output value
4	GPIO2_FORCEOUTEN	0	R/W	GPIO2 forced output enable setting 0: disable 1: enable (output the value according to bit5 (GPIO2_FORCEOUT) setting.)
3	Reserved	0	R/W	
2:0	GPIO2_IO_CFG[2:0]	010	R/W	GPIO2 input-output signal setting 000: [output] "L" level 001: [output] antenna switch control signal 1 (TX-RX switch signal: TRX_SW) 010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 011: [output] external PA control signal 100: [input-output] data (DIO) 101: [output] data clock (DCLK) 110: [output] digital monitor signal Please refer DMON_SET[3:0] ([MON_CTRL:B0 0x4D(3-0)]). 111: [output] interrupt notification signal (SINT)

0x51[GPIO3_CTRL]

Function: GPIO3 pin (pin #19) configuration setting
Address: 0x51 (BANK0)
Defalut value: 0x01

Bit	Bit name	Reset Value	R/W	Description
7	GPIO3_INV	0	R/W	GPIO3 output signal polarity setting
6	GPIO3_OD	0	R/W	GPIO3 output signal polarity setting
5	GPIO3_FORCEOUT	0	R/W	GPIO3 forced output value setting 0: "L" output 1: "H" output Note: the setting of bit7(GPIO3_INV) does not affect on this output value
4	GPIO3_FORCEOUTEN	0	R/W	GPIO3 forced output enable setting 0: disable 1: enable (output the value according to bit5 (GPIO3_FORCEOUT) setting.)
3	Reserved	0	R/W	
2:0	GPIO3_IO_CFG[2:0]	001	R/W	GPIO3 input-output signal setting 000: [output] "L" level 001: [output] antenna switch control signal 1 (TX-RX switch signal: TRX_SW) 010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 011: [output] external PA control signal 100: [input-output] data (DIO) 101: [output] data clock (DCLK) 110: [output] digital monitor signal Please refer DMON_SET[3:0] ([MON_CTRL:B0 0x4D(3-0)]). 111: [output] interrupt notification signal (SINT)

0x52[EXTCLK_CTRL]

Function: EXT_CLK pin (pin #10) configuration setting
Address: 0x52 (BANK0)
Defalut value: 0x00(ML7344J) / 0x03(ML7344C)

Bit	Bit name	Reset Value	R/W	Description
7	EXTCLK_INV	0	R/W	EXT_CLK output signal polarity setting
6	EXTCLK_OD	0	R/W	EXT_CLK output signal polarity setting
5	EXTCLK_FORCEOUT	0	R/W	EXT_CLK forced output value setting 0: "L" output 1: "H" output Note: the setting of bit7(EXTCLK_INV) does not affect on this output value
4	EXTCLK_FORCEOUTEN	0	R/W	EXT_CLK forced output enable setting 0: disable 1: enable (output the value according to bit5 (EXTCLK_ FORCEOUT) setting.)
3	Reserved	0	R/W	
2:0	EXTCLK_IO_CFG[2:0]	000	R/W	EXT_CLK input-output signal setting 000: [input] external clock (32 kHz) 001: [output] antenna switch control signal 1 (TX-RX switch signal: TRX_SW) 010: [output] antenna switch control signal 2 (antenna switch signal: ANT_SW) 011: [output] external PA control signal 100: Reserved 101: [output] data clock (DCLK) 110: [output] digital monitor signal Please refer DMON_SET[3:0] ([MON_CTRL:B0 0x4D (3-0)]). 111: [output] interrupt notification signal (SINT)

0x53[SPI/EXT_PA_CTRL]

Function: SPI interface IO (SDI/SDO) configuration / external PA control setting
Address: 0x53 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5	SDO_CFG	0	R/W	SDO pin (pin #12) input-output signal setting 0: [output] SDO (SPI interface) 1: [output] SDO (when SCEN pin (pin #14) = "L") DCLK (when SCEN pin = "H") For details, please refer to the "DIO function".
4	SDI_CFG	0	R/W	SDI pin (pin #15) input-output signal setting 0: [input] SDI (SPI interface) 1: [input] SDI (when SCEN pin (pin #14) = "L") [input-output] DIO (when SCEN pin = "H") For details, please refer to the "DIO function".
3:2	Reserved	00	R/W	
1	EXT_PA_CNT	0	R/W	External PA control signal control timing setting 0: TX_ON signal output. 1: PA_ON signal output. For details of each signal timing , please refer to " TX" in "Timing Chart"
0	EXT_PA_EN	0	R/W	External PA control timing enable setting 0: disable ("L" output) 1: enable (valid bit1(EXT_PA_CNT) setting)

0x54[IF_FREQ_H]

Function: IF frequency setting (high byte)
Address: 0x54 (BANK0)
Defalut value: 0x0F

Bit	Bit name	Reset Value	R/W	Description
7:0	IF_FREQ[15:8]	0000_1111	R/W	IF frequency setting (high byte) Note: combined together with [IF_FREQ_L:B0 0x55] register.

Description:

1. For details, please refer to the "IF frequency setting".

0x55[IF_FREQ_L]

Function: IF frequency setting (high byte)
Address: 0x55 (BANK0)
Defalut value: 0xC0

Bit	Bit name	Reset Value	R/W	Description
7:0	IF_FREQ[7:0]	1100_0000	R/W	IF frequency setting (low byte) For details, please refer to [IF_FREQ_H:B0 0x54] register

Description:

1. For details, please refer to the “IF frequency setting”.

0x56-0x61[Reserved]

Function:
Address: 0x56-0x61 (BANK0)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x62[OSC_ADJ1]

Function: Coarse adjustment of load capacitance for oscillation circuits
Address: 0x62 (BANK0)
Defalut value: 0x08

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	OSC_ADJ_ROUGH[3:0]	1000	R/W	Load capacitance coarse adjustment – approximately 0.7 pF/step

Description:

1. For details, please refer to the “Oscillation circuits adjustment”.

0x63[OSC_ADJ2]

Function: Fine adjustment of load capacitance for oscillation circuits
Address: 0x63 (BANK0)
Defalut value: 0x40

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	OSC_ADJ_FINE[6:0]	100_0000	R/W	Load capacitance fine adjustment – approximately 0.02 pF/step (adjustment range: 0x00 to 0x77)

Description:

1. For details, please refer to the “Oscillation circuits adjustment”.

0x64-0x65[Reserved]

Function:
Address: 0x64-0x65 (BANK0)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x66[RSSI_ADJ]

Function: RSSI value adjustment
Address: 0x66 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	RSSI_ADD	0	R/W	Adjustment direction setting 0: decrease (set -) 1: increase (set +)
6:5	Reserved	00	R/W	
4:0	RSSI_ADJ[4:0]	0_0000	R/W	RSSI adjustment value setting

Description:

1. For details, please refer to the “Energy detection value (ED value) adjustment”.

0x67[PA_MODE]

Function: PA mode setting / PA regulator carse adjustment
Address: 0x67 (BANK0)
Defalut value: 0x15

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:4	PA_MODE[1:0]	01	R/W	PA mode setting [ML7344C] 00: (not allowed) 01: 13 dBm mode 10: 20 dBm mode 11: (not allowed) [ML7344E/J] 00: 0 dBm mode 01: 10 dBm mode 10: 13 dBm mode 11: (not allowed)
3:0	PA_REG[3:0]	0101	R/W	PA regulator output voltage coarse adjustment setting

Description:
1. For details, please refer to the “PA adjustment”.

0x68[PA_REG_FINE_ADJ]

Function: PA regulator fine adjustment
Address: 0x68 (BANK0)
Defalut value: 0x0D

Bit	Bit name	Reset Value	R/W	Description
7:5	Reserved	000	R/W	
4:0	PA_REG_FINE_ADJ[4:0]	0_1101	R/W	PA regulator output voltage fine adjustment setting Note: PA output power can be adjusted in steps of less than 0.2dB.

Description:
1. For details, please refer to the “PA adjustment”.

0x69[PA_ADJ]

Function: PA gain adjustment
Address: 0x69 (BANK0)
Defalut value: 0x04

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	PA_ADJ[3:0]	0100	R/W	PA output gain adjustment setting.

Description:
1. For details, please refer to the “PA adjustment”.

0x6A-0x6D[Reserved]

Function:
Address: 0x6B-0x6D (BANK0)
Defalut value:-

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x6E[VCO_CAL]

Function: VCO calibration setting or status indication
Address: 0x6E (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	CAL_WR_EN	0	R/W	VCO calibration mode setting 0: automatic setting mode 1: forced writing mode
6:0	VCO_CAL[6:0]	000_0000	R/W	Current VCO calibration value Note: in automatic setting mode, current calibration value is indicated. Note: in forced writing mode, the value set to VCO_CAL[6:0] will be applied as the calibration value. (if CAL_WR_EN=0b0, the set value is ignored.) Note: After completion of clock stabilization, the value will be 0b100_0000.

Description:

1. For details, please refer to the “VCO adjustment”.

0x6F[VCO_CAL_START]

Function: VCO calibration execution
Address: 0x6F (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:5	Reserved	000	R/W	
4	AUTO_VCOCAL_EN	0	R/W	Automatic VCO calibration execution enable 0: disable automatic VCO calibration 1: execute automatic VCO calibration when recovering from the SLEEP state.
3:1	Reserved	000	R/W	
0	VCO_CAL_START	0	R/W	Execute VCO calibration 0: execution completion 1: execution start

Description:

1. For details, please refer to the “VCO adjustment”.

0x70[CLK_CAL_SET]

Function: Low speed clock caliblation control
Address: 0x70 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:4	CLK_CAL_DIV[3:0]	0000	R/W	Clock division control for low speed clock calibration 0000: no division 0001: no division Other setting: division setting.
3:1	Reserved	000	R/W	
0	CLK_CAL_START	0	R/W	Execute low speed clock calibration 0: execution completion 1: execution start

Description:

1. Please use the value specified in the "Low speed clock shift detection function".

0x71[CLK_CAL_TIME]

Function: Low speed clock caliblation time setting
Address: 0x71 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	CLK_CAL_TIME[5:0]	00_0000	R/W	Low speed clock calibration time setting Calibration time = Wake-up timer clock cycle ([SLEEP/WU_SET:B0 0x2D(2)]) * [set value]

Description:

1. Please use the value specified in the "Low speed clock shift detection function".

0x72[CLK_CAL_H]

Function: Low speed clock caliblation result indication (high byte)
Address: 0x72 (BANK0)
Defalut value: 0xFF

Bit	Bit name	Reset Value	R/W	Description
7:0	CLK_CAL[15:8]	1111_1111	R	Low speed clock calibration result (high byte)

Description:

1. Please use the value specified in the "Low speed clock shift detection function".

0x73[CLK_CAL_L]

Function: Low speed clock caliblation result indication (low byte)
Address: 0x73 (BANK0)
Defalut value: 0xFF

Bit	Bit name	Reset Value	R/W	Description
7:0	CLK_CAL[7:0]	1111_1111	R	Low speed clock calibration result (Low byte)

Description:

1. Please use the value specified in the "Low speed clock shift detection function".

0x74[Reserved]

Function:
Address: 0x74 (BANK0)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x75[SLEEP_INT_CLR]

Function: Interrupt clear setting during SLEEP state
Address: 0x75 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:1	Reserved	0000_000	R/W	
0	SLEEP_INT_CLR	0	R/W	Interrupt clear setting during SLEEP state 0: not clear interrupt 1: clear interrupt Note: During SLEEP state interrupt can not be cleared by [INT_SOURCE_GRP*: B0 0x0D/0E/0F] registers. By setting this bit to 0b1, interrupt can be cleared. This register can be written only during SLEEP state. After return from SLEEP state, this bit becomes 0b0. Note: Clear is applicable to whole interrupts. [INT_SOURCE_GRP*: B0 0x0D/0E/0F]

0x76[RF_TEST_MODE]

Function: TX test pattern setting
Address: 0x76 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5	TEST5	0	R/W	CW output
4	TEST4	0	R/W	“01” pattern output
3	TEST3	0	R/W	All “0” pattern output
2	TEST2	0	R/W	All “1” pattern output
1	TEST2	0	R/W	PN9 output
0	TEST_EN	0	R/W	Test mode enable 0: disable test mode 1: enable test mode

Description:

1. During normal operation, all bits have to be 0b0.
2. More than one bits are enable at the same time, lowest bit is valid.
3. Data rate is value in the TX_DRATE[3:0] ([DRATE_SET:B0 0x06(3-0)]).
4. During PN 9 output setting, any PN9 polynomial can be specified by [WHT_CFG:B1 0x66] register

   Most of the commercial Bit error meter use PN9’s polinomial as X^9+X^4+1, which is equivalent to [WHT_CFG:B1 0x66] = 0x08.

0x77[STM_STATE]

Function: State machine status / synchronization status indication
Address: 0x77 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6	SYNC_STATE	0	R	RX synchronization detection status 0: not synchronized 1: synchronization detected
5	SW_DET_RSLT	0	R	Receiving format indication 0: detect SyncWord #1 (Format A) 1: detect SyncWord #2 (Format B) Note: Indication is valid when packet format A or B is selected. PKT_FORMAT[1:0]([PKT_CTRL1:B0 0x04(1-0)])=0b00 or 0b01. Note: Updated at every SyncWord detection timing.
4:0	PHY_STATE	0_0000	R	State machine status 0_0000: IDLE state 0_0001: Preamble transmission state 0_0010: SyncWord transmission state 0_0011: L-field transmission state 0_0100: Data area transmission state 0_0101: Postamble transmission state 0_0110: TX delay waiting state 0_0111: DIO TX state 1_0010: SyncWord detection state 1_0011: L-field receiving state 1_0100: Data area receiving state 1_0111: DIO RX state

0x78[FIFO_SET]

Function: FIFO readout setting
Address: 0x78 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:1	Reserved	0000_000	R/W	
0	FIFO_R_SEL	0	R/W	FIFO readout setting 0: read RX FIFO 1: read TX FIFO Note: [RD_FIFO] register is used for reading both RX FIFO and TX FIFO. If 0b1 is set in order to read TX FIFO, please readout data length specified by [TX_PKT_LEN_H/L: B0 0x7A/7B] registers or set STATE_CLR1 ([STATE_CLR:B0 0x16(1)]) = 0b1. (RX FIFO pointer clear). If FIFO read is aborted without RX FIFO pointer clear and then change to read RX FIFO, reading starts from the interrupting pointer. Therefore RX FIFO could not be read correctly.

0x79[RX_FIFO_LAST]

Function: RX FIFO data usage status indication
Address: 0x79 (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	RX_FIFO_LAST [5:0]	00_0000	R	RX FIFO data usage status (range: 0 to 63) For details, please refer to the “FIFO control function”.

0x7A[TX_PKT_LEN_H]

Function: TX packet length setting (hihg byte)
Address: 0x7A (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	TX_PKT_LEN [15:8]	0000_0000	R/W	TX packet length setting Note: setting TX data length Format A: length excluded L-field and CRC field Format B/C: length excluded L-field Note: combined together with [TX_PKT_LEN_L:B0 0x7B] register. High byte is valid when LENGTH_MODE([PKT_CTRL: B0 0x05(0)=0b1 For details, please refer to the “FIFO control function”

NOTE:

1. If LEN_LF_EN ([PKT_CTRL1: B0 0x04(5)]) =0b1, the length value should be 63 bytes or less. If the length value is 64 bytes or more, TX/RX operation is not possible.[ML7344J]
2. If PKT_FORMAT=0b00, the length value should be 13 bytes or more. If the length value is 12 bytes or less, TX/RX operation is not possible [ML7344J]

0x7B[TX_PKT_LEN_L]

Function: TX packet length setting (low byte)
Address: 0x7B (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	TX_PKT_LEN [7:0]	0000_0000	R/W	TX packet length setting For details, please refer to [TX_PKT_LEN_H:B0 0x7A] register.

0x7C[WR_TX_FIFO]

Function: TX FIFO
Address: 0x7C (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	TX_PKT_LEN [7:0]	0000_0000	W	TX FIFO Note: TX data stored in the TX FIFO is one packet, regardless of packet length. If one packet data is stored and next packet is received, the FIFO will be over-written. And TX FIFO access error interrupt, INT[20] (group 3) will be generated. In case of TX FIFO access error occurs, set STATE_CLR0 ([STATE_CLR]B0 0x16(0)))=0b1. (TX FIFO pointer clear). For details, please refer to the “FIFO control function”.

0x7D[RX_PKT_LEN_H]

Function: RX packet length setting (hihg byte)
Address: 0x7D (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	RX_PKT_LEN [15:8]	0000_0000	R	RX packet length value (high byte) Note: combined together with [RX_PKT_LEN_L:B0 0x7E] register. Note: Format A/B/C: indicating packet length excluding L-field.

0x7E[RX_PKT_LEN_L]

Function: RX packet length setting (low byte)
Address: 0x7E (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	RX_PKT_LEN [7:0]	0000_0000	R	RX packet length value For details, please refer to [RX_PKT_LEN_H:B0 0x7D] register.

0x7F[RD_FIFO]

Function: FIFO read
Address: 0x7F (BANK0)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	RD_FIFO [7:0]	0000_0000	R	FIFO read Note: read FIFO specified by FIFO_R_SEL([FIFO_SET:B0 0x78(0)]). Note: When RX operation, RX data can be stored up to one packet, regardless of packet length. If one packet is stored and the next packet is received, the FIFO will be over-written. Note: If FIFO read is aborted, set STATE_CLR1 ([STATE_CLR]B0 0x16(1)))=0b1. (RX FIFO pointer clear). For details, please refer to the “FIFO control function”.

●Register Bank1

0x00[BANK_SEL]

Function: Register access bank selection
Address: 0x00 (BANK1)
Defalut value: 0x11

Bit	Bit name	Reset Value	R/W	Description
7	B3_ACEN	0	R/W	BANK3 register access enable 0: Access disable 1: Access enable
6	B2_ACEN	0	R/W	BANK2 register access enable 0: Access disable 1: Access enable
5	B1_ACEN	0	R/W	BANK1 register access enable 0: Access disable 1: Access enable
4	B0_ACEN	1	R/W	BANK0 register access enable 0: Access disable 1: Access enable
3-0	BANK[3:0]	0001	R/W	BANK selection 0b0001: BANK0 access 0b0010: BANK1 access 0b0100: BANK2 access b1000: BANK3 access Other setting: prohibit

NOTE:

1. Do not access BANK1 registers during VCO calibration operation
2. Register access can be done when CLK_INT_DONE([CLK_SET: B0 0x02(7)])=0b0.
   But the registers related to RF status has to be accessed after CLK_INT_DONE=0b1

0x01[CLK_OUT]

Function: CLK_OUT (GPIOn) output frequency setting
Address: 0x01 (BANK1)
Defalut value: 0x05

Bit	Bit name	Reset Value	R/W	Description
7:0	CLK_DIV[7:0]	0000_0101	R/W	Output frequency setting 0000_0000: 26MHz (LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b0) 8.66MHz (LOW_RATE_EN=0b1) 0000_0001: 13MHz 0000_0010: 8.66MHz (duty ratio: High:Low=1:2 0000_0011: 6.5MHz 0000_0100: 4.3MHz 0000_0101: 3.3MHz 0000_0110: 2.6MHz 0000_0111: 0.86MHz 0000_1000: 0.43MHz Other setting: The following formula is used to define output frequency. Output frequency = 26 / (16*[set value]+2) MHz For example; if set 0x09 Output frequency = 26 / (16*9+2) = 0.178MHz =178KHz

NOTE:
Due to default value of [CLK_SET2: B0 0x03] register, For ML7344JC/ML7344JS/ML7344CT/ML7344CS/ ML7344Ey, the CLK_OUT is not output after initiailzation. When using CLK_OUT with above LSIs, proper clock source should be set at first, [CLK_SET2: B0 0x03] register.

0x02[TX_RATE_H]

Function: TX data rate conversion setting (high 4 bits)
Address: 0x02 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	TX_RATE[11:8]	0000	R/W	TX data conversion setting (high 4bits) Note: combined together with [TX_RATE_L:B1 x03] register When a given data rate is set, following formula is used Setting value = round (26MHz / 13 / [a given data rate]) For details, please refer to the “Data rate setting function”.

0x03[TX_RATE_L]

Function: TX data rate conversion setting (Low byte)
Address: 0x03 (BANK1)
Defalut value: 0xD0

Bit	Bit name	Reset Value	R/W	Description
7:0	TX_RATE[7:0]	1101_0000	R/W	TX data conversion setting (high 4bits) For details, please refer to [TX_RATE_H:B1 0x02] register.

0x04[RX_RATE1_H]

Function: RX data rate conversion setting 1 (high 4 bits)
Address: 0x04 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	RX_RATE1[11:8]	0000	R/W	RX data conversion setting 1 (high 4bits) Note: combined together with [RX_RATE1_L:B1 x05] register When a given data rate is set, following formula is used Setting value = round (26MHz / ([a given data rate]*RX_RATE2] register)) For details, please refer to the “Data rate setting function”.

0x05[RX_RATE1_L]

Function: RX data rate conversion setting 1 (Low byte)
Address: 0x05 (BANK1)
Defalut value: 0x08(ES2)

Bit	Bit name	Reset Value	R/W	Description
7:0	RX_RATE1[7:0]	0000_1000	R/W	RX data conversion setting 1 (low byte) For details, please refer to [RX_RATE1_H:B1 0x04] register.

0x06[RX_RATE2]

Function: RX data rate conversion setting 2
Address: 0x06 (BANK1)
Defalut value: 0x71

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	RX_RATE2 [6:0]	111_0001	R/W	RX data conversion setting 2 (setting range: 30 to 127) Note: using together with RX_RATE1_H/L:B1 0x04/05] registers. Note: Do not set value below 0x1D to this register. For details, please refer to [RX_RATE1_H:B1 0x04] register.

0x07[Reserved]

Function:
Address: 0x07 (BANK1)
Defalut value: 0xFE

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	1111_1110	R/W	

0x08[ADC_CLK_SET]

Function: RSSI ADC clock frequency setting
Address: 0x08(BANK1)
Defalut value: 0xD3

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	1	R/W	Access is limited
6:5	OSC_W_SEL [1:0]	10	R/W	Clock stabilization waiting time setting 00: 500 µs 01: 250 µs 10: 50 µs 11: 10 µs Note: when start-up or return from the SLEEP state. The waiting time for clock stabilization is set by this register. For details, please refer to the “Start-up time” in the “Timing Chart”.
4	ADC_CLK_SEL	1	R/W	RSSI ADC clock setting When LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b0 0: 1.73MHz 1: 2.0MHz When LOW_RATE_EN([CLK_SET2:B0 0x03(0)])=0b1 0: 2.17MHz 1: 1.73MHz
3:0	Reserved	0011	R/W	Access is limited

0x09-0x0A[Reserved]

Function:
Address: 0x09-0x0A (BANK1)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x0B[PLL_LOCK_DETECT]

Function: RX data rate conversion setting 2
Address: 0x0B (BANK1)
Defalut value: 0x81

Bit	Bit name	Reset Value	R/W	Description
7	PLL_LD_EN	1	R/W	State control after PLL unlock detection when TX operation 0: keep TX state 1: Stop TX state forcibly by Force_TRX_OFF Note: after PLL unlock detection, generate INT2 (group 1) and then move to selected state. Note: during RX operation, after PLL unlock detection, generate INT2 and keep RX state.
6:0	RX_RATE2 [6:0]	000_0001	R/W	PLL lock detection time adjustment Detection time = [set value]* 8μs +1μs (default: 9 μs) Note: If PLL lock detection signal ="H" period exceeds the detection time, determined as PLL Lock. If PLL lock detection signal = “L”, determined as PLL unlock immediately.

NOTE:

1. When move to IDLE state due to PLL unlock detection, please clear PLL unlock interrupt (INT[2] group 1) before transmitting or reciving next data and [RF_STATUS:B0 0x0B] register write access must be after 5 μs.
2. For details about PLL unlock condition and timing, please refer to the “VCO adjustment”.

0x0C-0x12[Reserved]

Function:
Address: 0x0C-0x12 (BANK1)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x13[RSSI_MAG_ADJ]

Function: Scale factor setting for ED value conversion
Address: 0x13 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:4	RSSI_MAG_M[3:0]	0000	R/W	RSSI multiply value setting (setting range: 1 to 15)
3	RSSI_MAG_D3	0	R/W	RSSI division value 1/8 setting 0: do not apply 1: apply
2	RSSI_MAG_D2	0	R/W	RSSI division value 1/4 setting 0: do not apply 1: apply
1	RSSI_MAG_D2	0	R/W	RSSI division value 1/2 setting 0: do not apply 1: apply
0	RSSI_MAG_D1	0	R/W	RSSI division value 1/1 setting 0: do not apply 1: apply

NOTE:

1. For details, please refer to the “Energy detection value (ED value) adjustment”.
2. Please use the value specified in the “initialization table”.
3. Division setting can be selected one bit from bit 3 to bit0. If more than one bit are set, only MSB is valid. (i.e. If both bit3 and bit2 are set 0b1, 1/8 setting is valid.)
4. If both multiplication and division are set, complex calculation is performed. However, if bit[3:0] = 0b0000, 1/1 setting will be set.
   (i.e. If bit[7:4] = 0b0100 (* 4) and bit1 = 0b1 (1/2) are set, result will be *2.)
5. If 0x00 is written to this register, *1 setting.

0x14[RSSI_VAL]

Function: RSSI value indication
Address: 0x14 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	RSSI[5:0]	00_0000	R	RSSI AD conversion value Note: data update cycle is 18.5 μs. Note: Above example is in case of ADC clock = 1.73MHz, If 2.17MHz is selected, update cycle will be 14.8 μs. Regarding ADC clock, please refer [ADC_CLK_SET:B1 0x08] register.

0x15[AFC_CTRL]

Function: AFC control setting
Address: 0x15 (BANK1)
Defalut value: 0x82

Bit	Bit name	Reset Value	R/W	Description
7	AFC_EN	1	R/W	AFC enable setting 0: disable AFC 1: enable AFC
6:0	Reserved	000_0000	R/W	Access is limited

0x16[CRC_POLY3]

Function: CRC polynomial setting 3
Address: 0x16 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	CRC_POLY[30:24]	000_0000	R/W	CRC polynomial setting 3

Description:

1. For details, please refer to the “CRC function”.

0x17[CRC_POLY2]

Function: CRC polynomial setting 2
Address: 0x17 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	CRC_POLY[23:16]	0000_0000	R/W	CRC polynomial setting 2

Description:

1. For details, please refer to the “CRC function”.

0x18[CRC_POLY1]

Function: CRC polynomial setting 1
Address: 0x18(BANK1)
Defalut value: 0x1E

Bit	Bit name	Reset Value	R/W	Description
7:0	CRC_POLY[15:8]	0001_1110	R/W	CRC polynomial setting 1

Description:
1. For details, please refer to the “CRC function”.

0x19[CRC_POLY0]

Function: CRC polynomial setting 0
Address: 0x19 (BANK1)
Defalut value: 0xB2

Bit	Bit name	Reset Value	R/W	Description
7:0	CRC_POLY[7:0]	1011_0010	R/W	CRC polynomial setting 0

Description:
1. For details, please refer to the “CRC function”.

0x1A[PLL_DIV_SET]

Function: PLL frequency division setting
Address: 0x1A (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:5	Reserved	000	R/W	
4	PLL_MODE	0	R/W	PLL 1/2 division enable setting 0: disable 1: enable Note: if 0b1 is set, in the setting for the relevant PLL frequency, need to set value of twice the value of the desired frequency For details, please refer to the “Frequency Setting Function”.
3:0	Reserved	0000	R/W	

0x1B[TXFREQ_I]

Function: TX frequency setting (I counter)
Address: 0x1B (BANK1)
Defalut value: 0x10

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	TX_FREQ_I[5:0]	01_0000	R/W	TX frequency setting – I counter Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x1C[TXFREQ_FH]

Function: TX frequency setting (F counter high 4 bits)
Address: 0x1C (BANK1)
Defalut value: 0x06

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	TX_FREQ_F[19:16]	0110	R/W	TX frequency setting – F counter high 4 bits Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x1D[TXFREQ_FM]

Function: TX frequency setting (F counter middle byte)
Address: 0x1D (BANK1)
Defalut value: 0x8F

Bit	Bit name	Reset Value	R/W	Description
7:0	TX_FREQ_F[15:8]	1000_1111	R/W	TX frequency setting – F counter middle byte Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x1E[TXFREQ_FL]

Function: TX frequency setting (F counter low byte)
Address: 0x1E (BANK1)
Defalut value: 0xC0

Bit	Bit name	Reset Value	R/W	Description
7:0	TX_FREQ_F[7:0]	1100_0000	R/W	TX frequency setting – F counter low byte Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x1F[RXFREQ_I]

Function: RX frequency setting (I counter)
Address: 0x1F (BANK1)
Defalut value: 0x10

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	RX_FREQ_I[5:0]	01_0000	R/W	RX frequency setting – I counter Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x20[RXFREQ_FH]

Function: RX frequency setting (F counter high 4 bits)
Address: 0x20 (BANK1)
Defalut value: 0x06

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	RX_FREQ_F[19:16]	0110	R/W	RX frequency setting – F counter high 4 bits Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x21[RXFREQ_FM]

Function: RX frequency setting (F counter middle byte)
Address: 0x21 (BANK1)
Defalut value: 0x8F

Bit	Bit name	Reset Value	R/W	Description
7:0	RX_FREQ_F[15:8]	1000_1111	R/W	RX frequency setting – F counter middle byte Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x22[RXFREQ_FL]

Function: RX frequency setting (F counter low byte)
Address: 0x22 (BANK1)
Defalut value: 0xC0

Bit	Bit name	Reset Value	R/W	Description
7:0	RX_FREQ_F[7:0]	1100_0000	R/W	RX frequency setting – F counter low byte Note: default value is 426.6625MHz

Description:

1. For details, please refer to the “Channel #0 frequecny setting”.

0x23[CH_SPACE_H]

Function: Channel space setting (high byte)
Address: 0x23 (BANK1)
Defalut value: 0x03

Bit	Bit name	Reset Value	R/W	Description
7:0	CH_SPACE[15:8]	0000_0011	R/W	Channel space setting (high byte) Note: default value is 25 kHz

Description:

1. For details, please refer to the “Channel space setting”.

0x24[CH_SPACE_L]

Function: Channel space setting (low byte)
Address: 0x24 (BANK1)
Defalut value: 0xF0

Bit	Bit name	Reset Value	R/W	Description
7:0	CH_SPACE[7:0]	1111_0000	R/W	Channel space setting (low byte) Note: default value is 25 kHz

Description:

1. For details, please refer to the “Channel space setting”.

0x25[SYNC_WORD_LEN]

Function: SyncWord length setting
Address: 0x25 (BANK1)
Defalut value: 0x20

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	SYNC_WORD_LEN[5:0]	10_0000	R/W	SyncWord length setting (setting range: 8 to 32, unit: bit) Note: if setting is smaller than 0b00_0111, operate as 0b00_1000. Note: if setting is larger than 0b10_0000, operate as 0b10_0000

Description:

1. For details, please refer to the “SyncWord detection function”.

0x26[SYNC_WORD_EN]

Function: SyncWord enable setting
Address: 0x26 (BANK1)
Defalut value: 0x0F

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3	SYNC_WORD_EN3	1	R/W	SyncWord [31:24] checking enable 0: disable 1: enable
2	SYNC_WORD_EN2	1	R/W	SyncWord [23:16] checking enable 0: disable 1: enable
1	SYNC_WORD_EN1	1	R/W	SyncWord [15:8] checking enable 0: disable 1: enable
0	SYNC_WORD_EN0	1	R/W	SyncWord [7:0] checking enable 0: disable 1: enable

Description:

1. For details, please refer to the “SyncWord detection function”.

0x27[SYNCWORD1_SET0]

Function: SyncWord #1 setting (bit24 to 31)
Address: 0x27 (BANK1)
Defalut value: 0x54

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD1[31:24]	0101_0100	R/W	SyncWord parameter #1 setting (bit24 to 31)

Description:

1. For details, please refer to the “SyncWord detection function”.

0x28[SYNCWORD1_SET1]

Function: SyncWord #1 setting (bit16 to 23)
Address: 0x28 (BANK1)
Defalut value: 0x3D

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD1[23:16]	0011_1101	R/W	SyncWord parameter #1 setting (bit16 to 23)

Description:

1. For details, please refer to the “SyncWord detection function”.

0x29[SYNCWORD1_SET2]

Function: SyncWord #1 setting (bit8 to 15)
Address: 0x29 (BANK1)
Defalut value: 0x54

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD1[15:8]	0101_0100	R/W	SyncWord parameter #1 setting (bit8 to 15)

Description:
1. For details, please refer to the “SyncWord detection function”.

0x2A[SYNCWORD1_SET3]

Function: SyncWord #1 setting (bit0 to 7)
Address: 0x2A (BANK1)
Defalut value: 0xCD

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD1[7:0]	1100_1101	R/W	SyncWord parameter #1 setting (bit0 to 7)

Description:
1. For details, please refer to the “SyncWord detection function”.

0x2B[SYNCWORD2_SET0]

Function: SyncWord #2 setting (bit24 to 31)
Address: 0x2B (BANK1)
Defalut value: 0x54

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD2[31:24]	0101_0100	R/W	SyncWord parameter #2 setting (bit24 to 31)

Description:
1. For details, please refer to the “SyncWord detection function”.

0x2C[SYNCWORD2_SET1]

Function: SyncWord #2 setting (bit16 to 23)
Address: 0x2C (BANK1)
Defalut value: 0x3D

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD2[23:16]	0011_1101	R/W	SyncWord parameter #2 setting (bit16 to 23)

Description:
1. For details, please refer to the “SyncWord detection function”.

0x2D[SYNCWORD2_SET2]

Function: SyncWord #2 setting (bit8 to 15)
Address: 0x2D (BANK1)
Defalut value: 0x54

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD2[15:8]	0101_0100	R/W	SyncWord parameter #2 setting (bit8 to 15)

Description:
1. For details, please refer to the “SyncWord detection function”.

0x2E[SYNCWORD2_SET3]

Function: SyncWord #1 setting (bit0 to 7)
Address: 0x2E (BANK1)
Defalut value: 0x3D

Bit	Bit name	Reset Value	R/W	Description
7:0	SYNC_WORD3[7:0]	0011_1101	R/W	SyncWord parameter #3 setting (bit0 to 7)

Description:
1. For details, please refer to the “SyncWord detection function”.

0x2F[FSK_CTRL]

Function: GFSK/FSK clcok setting
Address: 0x2F (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:1	Reserved	0000_000	R/W	
0	FSK_CLK_SET	0	R/W	GFSK/FSK modulation timing resolution setting 0: 4.33 MHz resolution 1: 13 MHz resolution (inhibited) Note: ML7344 need to set 0b0.

Description:
1. For details, please refer to the “Modulation setting”.

0x30[GFSK_DEV_H]

Function: GFSK frequency deviation setting (high 6 bits)
Address: 0x30 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	GFSK_DEV[13:8]	00_0000	R/W	GFSK frequency deviation setting (high 6bits) Note: combined together with [GFSK_DEV_L:B1 x31] register. Note: default value is 3 kHz.

Description:

1. For details, please refer to the “Modulation setting”.

0x31[GFSK_DEV_L]

Function: GFSK frequency deviation setting (low byte)
Address: 0x31 (BANK1)
Defalut value: 0x78

Bit	Bit name	Reset Value	R/W	Description
7:0	GFSK_DEV[7:0]	0111_1000	R/W	GFSK frequency deviation setting (low byte) Note: combined together with [GFSK_DEV_H:B1 x30] register. Note: default value is 3 kHz.

Description:

1. For details, please refer to the “Modulation setting”.

0x32[FSK_DEV0_H/GFIL0]

Function: FSK 1st frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 0
Address: 0x32 (BANK1)
Defalut value: 0x49

Bit	Bit name	Reset Value	R/W	Description
7:6	GFIL0[7:6]	01	R/W	Gaussian filter coefficient setting 0 Note: Gaussian filter coefficient but range is bit7-0.
5:0	FSK_DEV0[13:8] / GFIL0[5:0]	00_1001	R/W	FSK 1st frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 0 Note: FSK 1st deviation frequency can be set combined with [FSK_DEV0_L/GFIL1:B1 x33] register. Default value is 0.9 kHz.

Description:

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x33[FSK_DEV0_L/GFIL1]

Function: FSK 1st frequency deviation setting (low byte) / Gaussian filter coefficient setting 1
Address: 0x33 (BANK1)
Defalut value: 0xA7

Bit	Bit name	Reset Value	R/W	Description
7:0	FSK_DEV0[7:0] / GFIL1[7:0]	1010_0111	R/W	FSK 1st frequency deviation setting (low byte) / Gaussian filter coefficient setting 1 Note: FSK 1st deviation frequency can be set combined with [FSK_DEV0_H/GFIL0:B1 x32] register. Default value is 0.9 kHz.

Description:
1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x34[FSK_DEV1_H/GFIL2]

Function: FSK 2nd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 2
Address: 0x34 (BANK1)
Defalut value: 0x0F

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	FSK_DEV1[13:8] / GFIL2[5:0]	00_1111	R/W	FSK 2nd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 2 Note: FSK 2nd deviation frequency can be set combined with [FSK_DEV1_L/GFIL3:B1 x35] register. Default value is 1.8 kHz.

Description:
1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x35[FSK_DEV1_L/GFIL3]

Function: FSK 2nd frequency deviation setting (low byte) / Gaussian filter coefficient setting 3
Address: 0x35 (BANK1)
Defalut value: 0x14

Bit	Bit name	Reset Value	R/W	Description
7:0	FSK_DEV1[7:0] / GFIL3[7:0]	0001_0100	R/W	FSK 2nd frequency deviation setting (low byte) / Gaussian filter coefficient setting 3 Note: FSK 2nd deviation frequency can be set combined with [FSK_DEV1_H/GFIL2:B1 x34] register. Default value is 1.8 kHz.

Description:
1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x36[FSK_DEV2_H/GFIL4]

Function: FSK 3rd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 4
Address: 0x36 (BANK1)
Defalut value: 0x19

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	FSK_DEV2[13:8] / GFIL4[5:0]	01_1001	R/W	FSK 3rd frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 4 Note: FSK 3rd deviation frequency can be set combined with [FSK_DEV2_L/GFIL5:B1 x37] register. Default value is 2.4 kHz.

Description:

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x37[FSK_DEV2_L/GFIL5]

Function: FSK 3rd frequency deviation setting (low byte) / Gaussian filter coefficient setting 5
Address: 0x37 (BANK1)
Defalut value: 0x1D

Bit	Bit name	Reset Value	R/W	Description
7:0	FSK_DEV2[7:0] / GFIL5[7:0]	0001_1101	R/W	FSK 3rd frequency deviation setting (low byte) / Gaussian filter coefficient setting 5 Note: FSK 3rd deviation frequency can be set combined with [FSK_DEV2_H/GFIL4:B1 x36] register. Default value is 2.4 kHz.

Description:

1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x38[FSK_DEV3_H/GFIL6]

Function: FSK 4th frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 4
Address: 0x38 (BANK1)
Defalut value: 0x1E)

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	0	R/W	
6	GFIL6[6]	0	R/W	Gaussian filter coefficient setting 6 Note: Gaussian filter coefficient but range is bit7-0.
5:0	FSK_DEV3[13:8] / GFIL6[5:0]	01_1110	R/W	FSK 4th frequency deviation setting (high 6 bits) / Gaussian filter coefficient setting 6 Note: FSK 4th deviation frequency can be set combined with [FSK_DEV3_L:B1 x39] register. Default value is 2.9 kHz.

Description:
1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x39[FSK_DEV3_L]

Function: FSK 4th frequency deviation setting (low byte)
Address: 0x39 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	FSK_DEV3[7:0]	0000_0000	R/W	FSK 4th frequency deviation setting (low byte) Note: FSK 4th deviation frequency can be set combined with [FSK_DEV3_H/GFIL6:B1 x38] register. Default value is 2.9 kHz.

Description:
1. For details, please refer to the “Modulation setting”.
2. Gaussian filter coefficient and FSK frequency deviation setting functions are shared in this register.

0x3A[FSK_DEV4_H]

Function: FSK 5th frequency deviation setting (high 6 bits)
Address: 0x3A (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	FSK_DEV4[13:8]	00_0000	R/W	FSK 5th frequency deviation setting (high 6 bits) Note: FSK 5th deviation frequency can be set combined with [FSK_DEV4_L:B1 x3B] register. Default value is 3 kHz.

Description:
1. For details, please refer to the “Modulation setting”.

0x3B[FSK_DEV4_L]

Function: FSK 5th frequency deviation setting (low byte)
Address: 0x3B (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	FSK_DEV4[7:0]	0000_0000	R/W	FSK 5th frequency deviation setting (low byte) Note: FSK 5th deviation frequency can be set combined with [FSK_DEV4_H:B1 x3A] register. Default value is 3 kHz.

Description:
1. For details, please refer to the “Modulation setting”.

0x3C[FSK_TIM_ADJ4]

Function: FSK 4th frequency deviation hold time setting
Address: 0x3C (BANK1)
Defalut value: 0x2D

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	FSK_TIM_ADJ4[6:0]	010_1101	R/W	FSK 4th frequency deviation hold time

Description:

1. For details, please refer to the “Modulation setting”.

0x3D[FSK_TIM_ADJ3]

Function: FSK 3rd frequency deviation hold time setting
Address: 0x3D (BANK1)
Defalut value: 0x2D

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	FSK_TIM_ADJ3[6:0]	010_1101	R/W	FSK 3rd frequency deviation hold time

Description:

1. For details, please refer to the “Modulation setting”.

0x3E[FSK_TIM_ADJ2]

Function: FSK 2nd frequency deviation hold time setting
Address: 0x3E (BANK1)
Defalut value: 0xx2D

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	FSK_TIM_ADJ2[6:0]	010_1101	R/W	FSK 2nd frequency deviation hold time

Description:

1. For details, please refer to the “Modulation setting”.

0x3F[FSK_TIM_ADJ1]

Function: FSK 1st frequency deviation hold time setting
Address: 0x3F (BANK1)
Defalut value: 0x2D

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	FSK_TIM_ADJ1[6:0]	010_1101	R/W	FSK 1st frequency deviation hold time

Description:

1. For details, please refer to the “Modulation setting”.

0x40[FSK_TIM_ADJ0]

Function: FSK no-deviation frequency (carrier frequency) hold time setting
Address: 0x40 (BANK1)
Defalut value: 0x2D

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	FSK_TIM_ADJ0[6:0]	010_1101	R/W	FSK no-deviation frequency hold time

Description:

1. For details, please refer to the “Modulation setting”.

0x41-0x4C[Reserved]

Function:
Address: 0x41-0x4C (BANK1)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x4D[VCO_CAL_MIN_I]

Function: VCO calibration low limit frequency setting (I counter)
Address: 0x4D (BANK1)
Defalut value: 0x10

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:0	VCO_CAL_MIN_I[5:0]	01_0000	R/W	VCO calibration low limit frequency setting – I counter

Description:

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”
2. For frequency setting method, please refer to the “VCO low limit frequency setting”.

Note:

1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x4E[VCO_CAL_MIN_FH]

Function: VCO calibration low limit frequency setting (F counter high 4 bits)
Address: 0x4E (BANK1)
Defalut value: 0x06

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	VCO_CAL_MIN_F[19:16]	0110	R/W	VCO calibration low limit frequency setting – F counter high 4 bits

Description:
1. For details information of VCO calibration usage, please refer to the “VCO adjustment”
2. For frequency setting method, please refer to the “VCO low limit frequency setting”.

Note:
1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x4F[VCO_CAL_MIN_FM]

Function: VCO calibration low limit frequency setting (F counter middle byte)
Address: 0x4F (BANK1)
Defalut value: 0x27

Bit	Bit name	Reset Value	R/W	Description
7:0	VCO_CAL_MIN_F[15:8]	0010_0111	R/W	VCO calibration low limit frequency setting – F counter middle byte

Description:
1. For details information of VCO calibration usage, please refer to the “VCO adjustment”
2. For frequency setting method, please refer to the “VCO low limit frequency setting”.

Note:
1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x50[VCO_CAL_MIN_FL]

Function: VCO calibration low limit frequency setting (F counter low byte)
Address: 0x50 (BANK1)
Defalut value: 0x62

Bit	Bit name	Reset Value	R/W	Description
7:0	VCO_CAL_MIN_F[7:0]	0110_0010	R/W	VCO calibration low limit frequency setting – F counter low byte

Description:
1. For details information of VCO calibration usage, please refer to the “VCO adjustment”
2. For frequency setting method, please refer to the “VCO low limit frequency setting”.

Note:
1. For low limit frequency, please set the frequency 400kHz lower than frequency used.

0x51[VCO_CAL_MAX_N]

Function: VCO calibration upper limit frequency setting
Address: 0x51 (BANK1)
Defalut value: 0x02

Bit	Bit name	Reset Value	R/W	Description
7:4	Reserved	0000	R/W	
3:0	VCO_CAL_MAX_N[3:0]	0010	R/W	VCO calibration upper limit frequency range setting (ΔF from the low limit frequency) 0000: 0 MHz 0001: 0.8125 MHz 0010: 1.625 MHz 0011: 3.25 MHz 0100: 6.5 MHz 0101: 13 MHz 0110: 26 MHz 0111: 52 MHz Other setting: prohibit

Description:

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”
2. For frequency setting method, please refer to the “VCO low limit frequency setting”.

Note:

1. For upper limit frequency, please set the frequency range that includes the frequency used.

0x52[TXVCAL_MIN]

Function: TX VCO calibration low limit value indication and setting
Address: 0x52 (BANK1)
Defalut value: 0x40

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	TXVCAL_MIN[6:0]	100_0000	R/W	TX VCO calibration low limit value Note: after calibration by [VCO_CAL_START:B0 0x6F], value will be saved automatically.

Description:

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”

0x53[TXVCAL_MAX]

Function: TX VCO calibration upper limit value indication and setting
Address: 0x53 (BANK1)
Defalut value: 0x40

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	TXVCAL_MAX[6:0]	100_0000	R/W	TX VCO calibration upper limit value Note: after calibration by [VCO_CAL_START:B0 0x6F], value will be saved automatically.

Description:

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”

0x54[RXVCAL_MIN]

Function: RX VCO calibration low limit value indication and setting
Address: 0x54 (BANK1)
Defalut value: 0x40

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	RXVCAL_MIN[6:0]	100_0000	R/W	RX VCO calibration low limit value Note: after calibration by [VCO_CAL_START:B0 0x6F], value will be saved automatically.

Description:

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”

0x55[RXVCAL_MAX]

Function: RX VCO calibration upper limit value indication and setting
Address: 0x55 (BANK1)
Defalut value: 0x40

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	RXVCAL_MAX[6:0]	100_0000	R/W	RX VCO calibration upper limit value Note: after calibration by [VCO_CAL_START:B0 0x6F], value will be saved automatically.

Description:

1. For details information of VCO calibration usage, please refer to the “VCO adjustment”

0x56[DEMOD_SET0]

Function: Demodulator configulation 0
Address: 0x56 (BANK1)
Defalut value: 0x10

Bit	Bit name	Reset Value	R/W	Description
7:5	Reserved	000	R/W	
4	STR_LIM_ON	1	R/W	Symbol timing recovery limiter setting 0: turn off limiter 1: turn on limiter
3	STR_HOLD_ON	0	R/W	Symbol timing recovery setting 0: constantly tacking symbol timing 1: after SyncWord detection, keeping symbol timing
2	AFC_LIM_OFF	0	R/W	AFC limiter setting 0: turn on AFC limiter 1: turn off AFC limiter
1	AFC_HOLD_ON	0	R/W	AFC mode setting 0: constantly performing AFC 1: after SyncWord detection, keeping AFC
0	AFC_OFF_EN	0	R/W	AFC OFF enable setting 0: disable (performing AFC) 1: enable (not performing AFC)

Description:

1. Please use the value specified in the "Initialization table".

0x57[DEMOD_SET1]

Function: Demodulator configulation 1
Address: 0x57 (BANK1)
Defalut value: 0x23

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5:4	IFEDGE_SEL[1:0]	10	R/W	IF edge width setting 00: 1 cycle width 01: 2 cycle width 10: 3 cycle width 11: 4 cycle width
3:0	DEMOD_DIV[3:0]	0011	R/W	Modulation divisor setting 0000: no division 0001: no division Other setting: divisor value setting (default: 1/4)

Description:

1. Please use the value specified in the "Initialization table".

0x58[DEMOD_SET2]

Function: Demodulator configulation 2
Address: 0x58 (BANK1)
Defalut value: 0x53

Bit	Bit name	Reset Value	R/W	Description
7	Reserved	0	R/W	
6:0	FDET_LPF1_SUB[6:0]	101_0011	R/W	Demodulator LPF 1 zero adjustment

Description:

1. Please use the value specified in the "Initialization table".

0x59[DEMOD_SET3]

Function: Demodulator configulation 3
Address: 0x59 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:5	FDET_LPF3_SUB[2:0]	000	R/W	Demodulator LPF3 zero adjustment
4:0	FDET_LPF2_SUB[4:0]	0_0000	R/W	Demodulator LPF2 zero adjustment

Description:

1. Please use the value specified in the "Initialization table".

0x5A[DEMOD_SET4]

Function: Demodulator configulation 4
Address: 0x5A (BANK1)
Defalut value: 0x7F

Bit	Bit name	Reset Value	R/W	Description
7:4	LPF2_SEL[3:0]	0111	R/W	Demodulator LPF2 cut-off frequency setting
3:0	LPF1_SEL[3:0]	1111	R/W	Demodulator LPF1 cut-off frequency setting

Description:

1. Please use the value specified in the "Initialization table".

0x5B[DEMOD_SET5]

Function: Demodulator configulation 5
Address: 0x5B (BANK1)
Defalut value: 0xB4

Bit	Bit name	Reset Value	R/W	Description
7:6	LPF3_GAIN[1:0]	10	R/W	Demodulator LPF3 gain setting
5:3	LPF2_GAIN[2:0]	110	R/W	Demodulator LPF2 gain setting
2:0	LPF3_GAIN[2:0]	100	R/W	Demodulator LPF3 cut-off frequency setting

Description:

1. Please use the value specified in the "Initialization table".

0x5C[DEMOD_SET6]

Function: Demodulator configulation 6
Address: 0x5C (BANK1)
Defalut value: 0x30

Bit	Bit name	Reset Value	R/W	Description
7:0	RXDEV_RANGE[7:0]	0011_0000	R/W	RX frequency deviation range setting setting value = frequency deviation range[Hz]*6.58 Note: this equation is valid only when master clock frequency is 26MHz.

Description:

1. Please use the value specified in the "Initialization table". If adjustment is needed, the target of setting value is "used frequency deviation * 1.5".

0x5D[DEMOD_SET7]

Function: Demodulator configulation 7
Address: 0x5D (BANK1)
Defalut value: 0x4F

Bit	Bit name	Reset Value	R/W	Description
7:0	AFC_LIM[7:0]	0100_1111	R/W	AFC tacking range setting

Description:

1. Please use the value specified in the "Initialization table".

0x5E[DEMOD_SET8]

Function: Demodulator configulation 8
Address: 0x5E (BANK1)
Defalut value: 0x26

Bit	Bit name	Reset Value	R/W	Description
7:6	LPF1_ADJ[1:0]	00	R/W	Demodulator LPF1 adjustment
5	LPF2_CLK_SEL	1	R/W	Demodulator LPF2 clock setting 0: using over 15 kbps (inhibited) 1: using less than or equal 15 kbps Note: ML7344 need to set 0b1.
4:3	Reserved	00	R/W	
2:0	PLL_AFC_SHIFT[2:0]	110	R/W	PLL-AFC magnification adjustment 1

Description:

1. Please use the value specified in the "Initialization table".

0x5F[DEMOD_SET9]

Function: Demodulator configulation 9
Address: 0x5F (BANK1)
Defalut value: 0x8B

Bit	Bit name	Reset Value	R/W	Description
7:0	PLL_AFC_CO[7:0]	1000_1011	R/W	PLL-AFC magnification adjustment 2

Description:
1. Please use the value specified in the "Initialization table".

0x60[DEMOD_SET10]

Function: Demodulator configulation 10
Address: 0x60 (BANK1)
Defalut value: 0x10

Bit	Bit name	Reset Value	R/W	Description
7:5	Reserved	000	R/W	
4:0	STR_PB_LEN[4:0]	1_0000	R/W	Demodulator preamble detection threshold value setting

Description:
1. Please use the value specified in the "Initialization table".

0x61[Reserved]

Function:
Address: 0x61 (BANK1)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x62[ADDR_CHK_CTR_H]

Function: Address check counter indication (high 3 bits)
Address: 0x62 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:3	Reserved	0000_0	R/W	
2:0	ADDR_CHK_CTR[10:8]	000	R/W	Indicating the number of packets mismatch during Field checking (high 3 bits) Note: combined together with [ADDR_CHK_CTR_L:B1 x63] register Note: Max. count is 2047. Count vale. Count value can be cleared by STATE_CLR4([STATE_CLR:B0 0x16(4)]).

Description:
1. Please use the value specified in the "Field checking function".

0x63[ADDR_CHK_CTR_L]

Function: Address check counter indication (low byte)
Address: 0x63 (BANK1)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:0	ADDR_CHK_CTR[7:0]	0000_0000	R/W	Indicating the number of packets mismatch during Field checking (low bytes) For details, please refer to [ADDR_CHK_CTR_H:B1 0x62] register.

Description:

1. Please use the value specified in the "Field checking function".

0x64[WHT_INIT_H]

Function: Whitening initialized state setting (high 1 bit)
Address: 0x64 (BANK1)
Defalut value: 0x01

Bit	Bit name	Reset Value	R/W	Description
7:1	Reserved	0000_000	R/W	
0	WHT_INIT[8]	1	R/W	Whitening initialized state setting (high 1 bit)

Description:

1. Please use the value specified in the "Data Whitening function".

0x65[WHT_INIT_L]

Function: Whitening initialized state setting (low byte)
Address: 0x65 (BANK1)
Defalut value: 0xFF

Bit	Bit name	Reset Value	R/W	Description
7:0	WHT_INIT[7:0]	1111_1111	R/W	Whitening initialized state setting (low byte)

Description:

1. Please use the value specified in the "Data Whitening function".

0x66[WHT_CFG]

Function: Whitening polynomial setting
Address: 0x66 (BANK1)
Defalut value: 0x08

Bit	Bit name	Reset Value	R/W	Description
7:0	WHT_CFG[7:0]	0000_1000	R/W	Whitening polynomial setting

Description:

1. Please use the value specified in the "Data Whitening function".

0x67-0x7E[Reserved]

Function:
Address: 0x67-0x7E (BANK1)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	

0x7F[ID_CODE]

Function: ID code indication
Address: 0x7F (BANK1)
Defalut value: depends on the version

Bit	Bit name	Reset Value	R/W	Description
7:0	ID_CODE[7:0]	-	R	ID code 0x02: ML7344J 0x40: ML7344C

●Register Bank2

0x00[BANK_SEL]

Function: Register access bank selection
Address: 0x00 (BANK2)
Defalut value: 0x11

Bit	Bit name	Reset Value	R/W	Description
7	B3_ACEN	0	R/W	BANK3 register access enable 0: Access disable 1: Access enable
6	B2_ACEN	0	R/W	BANK2 register access enable 0: Access disable 1: Access enable
5	B1_ACEN	0	R/W	BANK1 register access enable 0: Access disable 1: Access enable
4	B0_ACEN	1	R/W	BANK0 register access enable 0: Access disable 1: Access enable
3-0	BANK[3:0]	0001	R/W	BANK selection 0b0001: BANK0 access 0b0010: BANK1 access 0b0100: BANK2 access 0b1000: BANK3 access Other setting: prohibit

NOTE:
1. Do not access BANK1 registers during VCO calibration operation
2. Register access can be done when CLK_INT_DONE([CLK_SET: B0 0x02(7)])=0b0.
   But the registers related to RF status has to be accessed after CLK_INT_DONE=0b1

0x01-0x2B[Reserved]

Function:
Address: 0x01-0x2B (BANK2)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	Access is limited

NOTE:
1. These registers are closed register and acceess is limited. Accessible registers are written in the “initialization table”.

0x2C[LO_BIAS_IP]

Function: Local bias adjustment (I-phase, Positive)
Address: 0x2C (BANK2)
Defalut value: 0x80

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	1000_0000	R/W	Local bias adjustment (I-Phase, Positive)

NOTE:
1. For details, please refer to the “IQ adjustment”.

0x2D[LO_BIAS_IN]

Function: Local bias adjustment (I-phase, Negative)
Address: 0x2D (BANK2)
Defalut value: 0x80

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	1000_0000	R/W	Local bias adjustment (I-Phase, Negative)

NOTE:
1. For details, please refer to the “IQ adjustment”.

0x2E[LO_BIAS_QP]

Function: Local bias adjustment (Q-phase, Positive)
Address: 0x2E (BANK2)
Defalut value: 0x80

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	1000_0000	R/W	Local bias adjustment (Q-Phase, Positive)

NOTE:
1. For details, please refer to the “IQ adjustment”.

0x2F[LO_BIAS_QN]

Function: Local bias adjustment (Q-phase, Negative)
Address: 0x2F (BANK2)
Defalut value: 0x80

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	1000_0000	R/W	Local bias adjustment (Q-Phase, Negative)

NOTE:
1. For details, please refer to the “IQ adjustment”.

0x30-3F[Reserved]

Function:
Address: 0x30-0x3F (BANK2)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	Access is limited

NOTE:
1. These registers are closed register and acceess is limited. Accessible registers are written in the "initialization table".

0x40[VTUNE_COMP_ON]

Function: VCO adjustment voltage comparison result display enable
Address: 0x40 (BANK2)
Defalut value: 0x00

Bit	Bit name	Reset Value	R/W	Description
7:6	Reserved	00	R/W	
5	VTUNE_COMP_ON	0	R/W	VCO adjustment voltage comparison result display enable 0: disable 1: enable
4:0	Reserved	0_0000	R/W	

NOTE:
1. For details, please refer to the "IQ adjustment".

0x41-7F[Reserved]

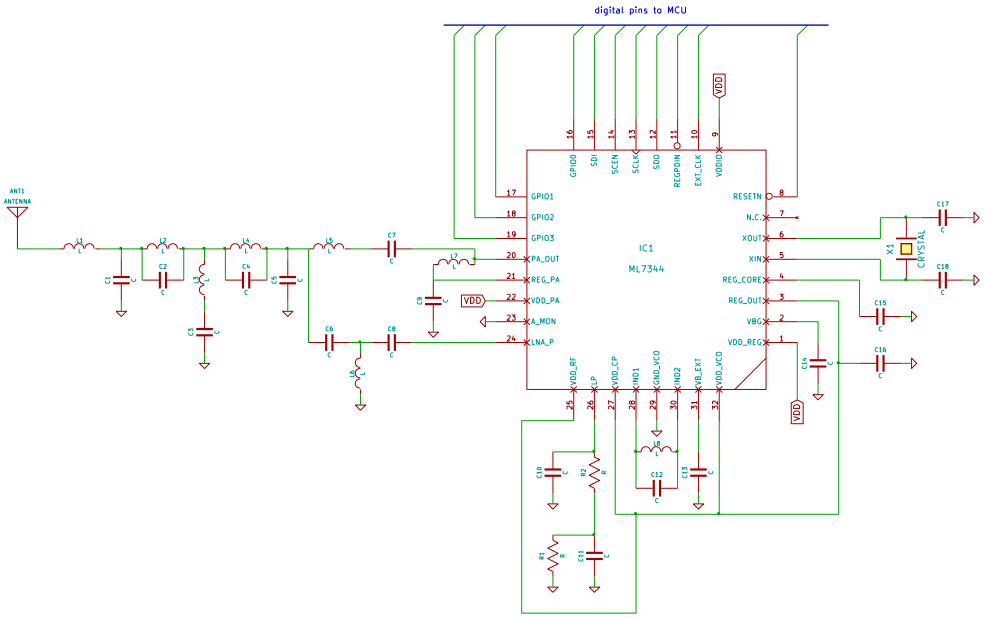
Function:
Address: 0x41-0x7F (BANK2)
Defalut value: -

Bit	Bit name	Reset Value	R/W	Description
7:0	Reserved	-	R/W	Access is limited

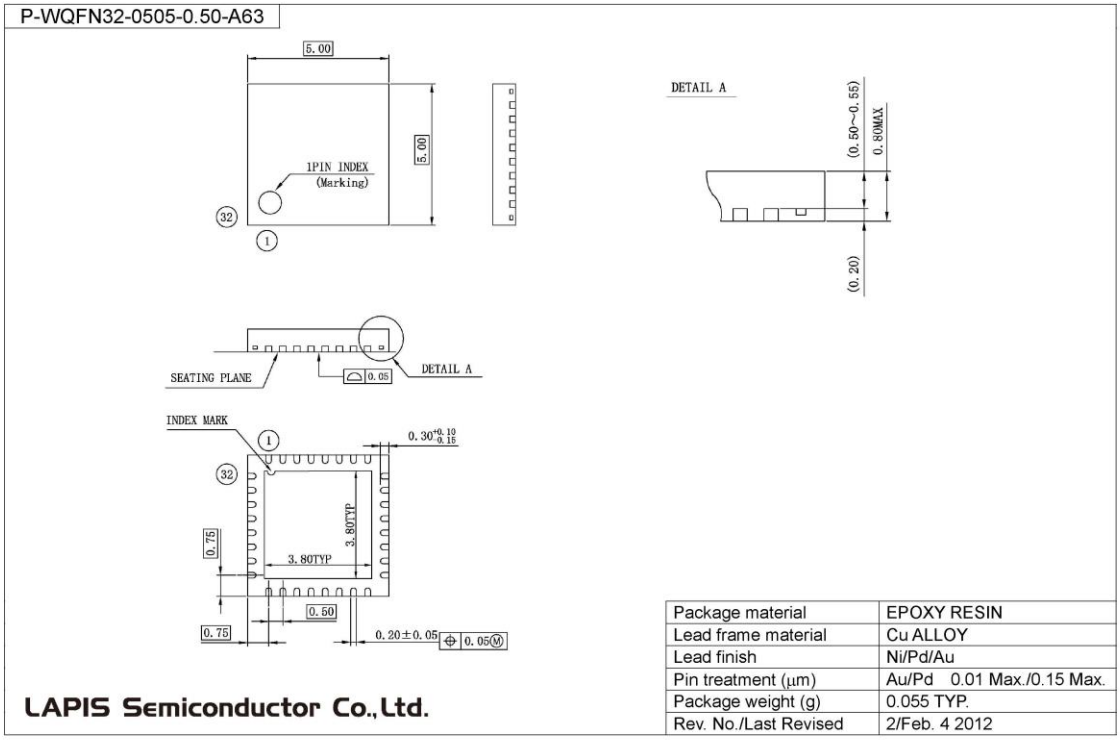
NOTE:
1. These registers are closed register and acceess is limited. Accessible registers are written in the "initialization table".

■Application circuit example

The below diagram does not show decoupling capacitors for LSI power pins.
10uF decoupling capacitor should be placed to common 3.3V power pins .
MURATA LQW15series inductors are recommended.



■Package dimensions



Package material	EPOXY RESIN
Lead frame material	Cu ALLOY
Lead finish	Ni/Pd/Au
Pin treatment (μm)	Au/Pd 0.01 Max./0.15 Max.
Package weight (g)	0.055 TYP.
Rev. No./Last Revised	2/Feb. 4 2012

Remarks for surface mount type package

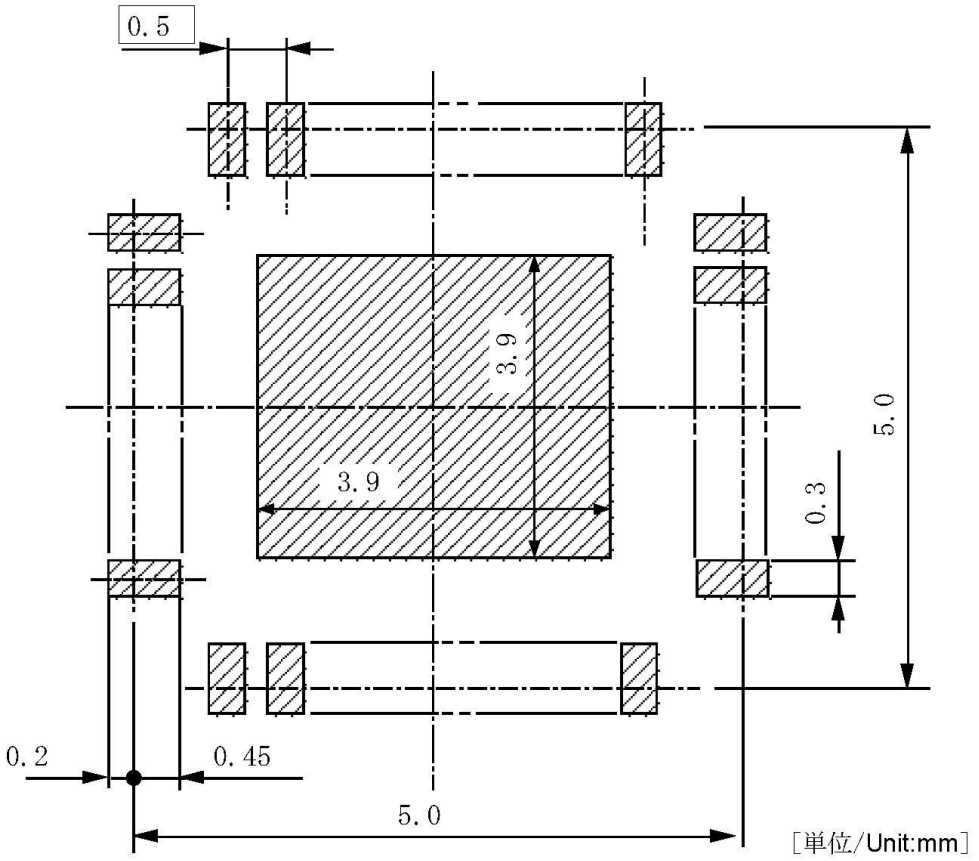
Surface mount type package is very sensitive affected by heating from reflow process, humidity during storaging Therefore, in case of reflow mouting process, please contact sales representative about product name, package name, number of pin, package code and required reflow process condition (reflow method, temperature, number of reflow process), storage condition.

■Footprint Pattern (Recommendation)

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts, reliability, wiring, and elimination of slder bridges.

The optimum design for the foot pattern varies with the materials of the substrate, the sort and thichness of used soldering paste, and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering PC boards.

P-WQFN32-0505-0.50-A63



■Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7344C/E/J-01	July 8, 2013	–	–	Initial release
FEDL7344C/E/J-02	July 9, 2013	3	3	Correct mistype(100mW TX power consumption)
		13	13	Add RX power consumption of ML7344xC.
		21	21	Change figure in DIO interface characteristics. Initial level of DCLK is modified from L to H.
FEDL7344C/E/J-03	Apr 15, 2014	15	15	Added min. / max. value for TX power
		17	17	Added max. value for minimum RX sensitivity.
		58	58	Corrected formula of Wake-up timer interval and continuous operation timer.
		81, 96	81, 96	Updated a formula for calculating the ED value.
			89, 90	Added typical values for PA adjustments.
		98	98	Removed “BPF adjustment”. This is no longer necessary.
		99	98	Added “RX mode setting.”
		132	134	Added TX_ON signal in “TX Timing-chart”
		148	150	Added note of LEN_LF_EN[PKT_CTRL1: B0 0x04(5)] and PKT_FORMAT[PKT_CTRL1: B0 0x04(1-0)].
		176	178	Corrected formula of wake-up timer interval in function description.
		176	178	Corrected formula of continuous operation timer interval in function description.
		193	195	Corrected function description of EXT_CLK pin configuration setting (EXTCLK_IO_CFG [EXTCLK_CTRL: B0 0x52 (2-0)])
		194	196	Corrected function description of external setting EXT_PA_CNT[SPI/EXT_PA_CTRL: B0 0x53(1)] and EXT_PA_EN[SPI/EXT_PA_CTRL: B0 0x53(0)]
		204	207	Added note of LEN_LF_EN[PKT_CTRL1: B0 0x04(5)] and PKT_FORMAT[PKT_CTRL1: B0 0x04(1-0)].
		208	211	Added note of CLK_OUT function
		144, 239	143, 238	Removed a register [BPF_ADJ: B2 0x10]. BPF adjustment is no longer necessary.

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7344C/E/J-04	Oct 2, 2014	-	-	Removed SPXO support
		12	12	Removed Master Clock Accuracy(ACMCK2)
		14	14	Corrected Regulator voltage output when sleep mode(SUB_REG)
		15	15	Corrected Typ. value of TX Power.
		18	18	Corrected typ. value of blocking (470MHz BAND).
		70	70	Corrected compensation range of AFC
		198	-	Removed a register [IFF_ADJ_H: B0 0x5E]
		198	-	Removed a register [IFF_ADJ_L: B0 0x5F]
		216	215	Removed registers bit6-4 of [AFC_CTRL: B1 0x15]
FEDL7344C/E/J-05	Jan 20, 2015	9	9	Added description of EXT_CLK pin
		88	88	Changed frequency from 32.768kHz to 44kHz in the example.
		-	89-90	Added antenna switching function.
		97	97	Modified registers
		135	138	Corrected TX-RX transition time in Timing chart
		136	139	Corrected RX start-up time in Timing chart
		139	142	Corrected RX start-up time and CCA time in Timing chart
		176	179	Added note of RCOSC_MODE[SLEEP/WU_SET: B0 0x2D(3)]
		177	180	Added note of WUDT_CLK_SET[WUT_CLK_SET: B0 0x2E(7-4)]
		-	195	added [2DIV_CTRL: B0 0x48] and [ANT_CTRL: B0 0x4C]
		234	238	added equation for setting value and note of [DEMOD_SET6: B1 0x5C]

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7344C/E/J-06	Apr 1st, 2019	7-9	7-9	[Pin-definition] correct definition in reset state of pins (EJDL7344C_E_J-05_errata_rev3_0)
		8	8	[Pin-definition]-[Regulator Pins] delete detail (*1)
		23	23	[Electrical Characteristics]-[Reset Characteristics] delete RESETN rising time.
		49	49	[Function Description]-[Packet Handling Function]-[FIFO control function] add note(2)
		85	85	[Function Description]-[Other Function]-[Interrupt generation function] (2)Interrupt generation timing Correct VCO Calibration time (EJDL7344C_E_J-05_errata_rev3_0)
		98	98	[LSI Adjustment items and Adjustment Method]-[VCO adjustment] add description about activation of VTUNE_COMP_ON)
		100	100	[LSI Adjustment items and Adjustment Method]-[VCO adjustment] Correct VCO calibration range setting(delete 82.875, 104MHz)
		109	109	[Flowchart]-[Turn On Sequence] Correct SPI access prohibited section (FJDL7344C_E_J-05_errata_rev3_0)
		130	130-131	[Flowchart]-[Error Process] (1)Sync Error Add note (FJDL7344C_E_J-05_errata_rev3_0)
		136	137-138	[Time Chart]-[Start-up] Correct SPI access prohibited section(ML7344JC/ML7344CC) (EJDL7344C_E_J-05_errata_rev3_0)
		152	154	[CLK_SET2: B0 0x03] add note 4,5 (EJDL7344C_E_J-05_errata_rev3_0)
		153	155	[PKT_CTRL1: B0 0x04] add note of Extended Link Layer mode setting (Wireless M-Bus) (FJDL7344C_E_J-05_errata_rev3_0)
		154	156	[PKT_CTRL2: B0 0x05] add note for CRC disabling setting (EJDL7344C_E_J-05_errata_rev3_0)
		170	172	[TXFIFO_THRL: B0 0x18] add note for TX trigger level setting (EJDL7344C_E_J-05_errata_rev3_0)
		192	194	[SYNC_CONDITION1: B0 0x45] add register description
		234	236	[VCO_CAL_MAX_N: B1 0x51] Correct VCO calibration range setting(delete 82.875, 104MHz) (EJDL7344C_E_J-05_errata_rev3_0)
		-	246	[VTUNE_COMP_ON: B2 0x40] add register description
FEDL7344C/E/J-07	Nov.1 2023	2	2	Add application
		253	253	The description of [Note] has been updated.
		2	2	Add Product Name
FEDL7344C/E/J-08	Jan.10 2024	253	253	The description of [Note] has been updated.

Notes

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LTSZ08023・01・002