Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL62Q1500C-05
Issue Date: Mar 26, 2024

ML62Q1500C Group

16-bit micro controller

GENERAL DESCRIPTION

ML62Q1500C Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory (Flash memory), data memory (RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC generator, DMA controller, Clock generator, Simplified RTC, Timer, General Purpose Ports, UART, Synchronous serial port, I^2C bus interface unit (Master, Slave), Buzzer, Voltage Level Supervisor (VLS), Successive approximation type A/D converter, D/A converter, Analog comparator, Safety function (IEC60730/60335 Class B), and so on.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP (In-System Programming) function supports the Flash programming in production line.

- Applications

Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

Note:
This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems. Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

- Product list

The ML62Q1500C Group has five packages (52pin - 80pin) and ten kinds of memory sizes (96Kbyte - 128Kbyte).

Table 1 ML62Q1500C Group Product List

Program memory	Data memory (RAM)	Data Flash	52pin TQFP52	64pin QFP64 TQFP64	80pin QFP80
128Kbyte	8Kbyte	4KByte	ML62Q1544C	ML62Q1554C	ML62Q1564C
96Kbyte			ML62Q1543C	ML62Q1553C	ML62Q1563C

Please see the last 2 pages “Notes for product usage” and “Notes” in this document on use with this ML62Q1500C group.

FEATURES

- CPU
  - 16-bit RISC CPU: nX-U16/100 (A35 core)
  - Instruction system: 16-bit length instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Built-in On-chip debug function
  - Built-in ISP (In-System Programming) function
  - Minimum instruction execution time
    Approximately 30.5µs (at 32.768 kHz system clock)
    Approximately 62.5ns/41.6ns (at 16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Multiplication : 16bit × 16bit (operation time: 4 cycles)
  - Division : 32bit ÷ 16bit (operation time: 8 cycles)
  - Division : 32bit ÷ 32bit (operation time: 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time: 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time: 4 cycles)
  - Signed or Unsigned is selectable

- Operating voltage and temperature
  - Operating voltage: VDD = 1.6 to 5.5V (V_{DD} should be 1.8V or over at Power-on)
  - Operating temperature: -40°C to +105°C

- Internal memory
  - Program memory area
    Rewrite count: 100 cycles
    Write unit: 32bit (4byte)
    Erase unit: 16Kbyte/1Kbyte
    Erase/Write temperature: 0°C to +40°C

  - Data Flash memory area
    Rewrite count 10,000 cycles
    Write unit: 8bit (1byte)
    Erase unit: all area/128byte
    Erase/Write temperature: -40°C to +85°C
    Back Ground Operation (CPU can work while erasing and rewriting)

    This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
    Super Flash® is a registered trademark of Silicon Storage Technology, Inc.
  - Data RAM area
    Rewrite unit: 8bit/16bit (1byte/2byte)
    Parity check function is available (interrupt / reset are generatable at Parity error)

- Clock generation circuit
  - Low-speed clock (LSCLK)
    Internal low-speed RC oscillation: Approximately 32.768kHz
    External low-speed clock input: Approximately 32.768kHz
    External low-speed crystal oscillation: 32.768kHz crystal resonator is connectable
    3 selectable crystal oscillation mode (Tough, Normal, and Low current consumption)
    - Tough mode: Largest oscillation allowance to make highest resistance against leakage between the pins
    - Normal mode: Normal oscillation allowance and current consumption
    - Low current consumption mode: Smallest oscillation allowance to make lower current consumption
  - High-speed clock (HSCLK)
    PLL oscillation: 2 selectable oscillation frequency (24MHz and 16MHz) by code option
  - Watch Dog Timer (WDT): built-in independent clock for WDT (RC1K: Approximately 1kHz)

- Reset
  - Reset by reset input pin
  - Reset by Power-On Reset

- Reset by WDT overflow
- Reset by WDT invalid clear
- Reset by RAM parity error
- Reset by unused ROM area access (instruction access)
- Reset by voltage level supervisor (VLS)
- Software reset by BRK instruction (reset CPU only)
- Reset the peripherals individually
- Collective reset to the all control pins and peripheral circuits

- Power management
  - HALT mode: CPU stops executing instruction, peripheral circuits continue working
  - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits continue working with low-speed clock
  - HALT-C mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits working with low-speed clock remain previous states. Peripheral circuits can work only watchdog timer, external interrupt, low-speed time base counter, 16-bit timers, and crystal oscillation circuit.
  - STOP mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop.
  - STOP-D mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop. The internal logic voltage (VDDL) goes down to reduce the current consumption (RAM data is retained).
  - Clock gear: High-speed system clock frequency can be changed (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of HSCLK)
  - Block Control Function: Powers down the unused function blocks (reset the block or stop supplying the clock)

- Interrupt controller
  - External interrupt ports: max. 12
  - Non-maskable interrupt source: 1 (Internal sources: WDT)
  - Maskable interrupt sources: max. 43
  - Four step interrupt levels

- Watchdog timer (WDT)
  - Selectable Operating clock: select RC1K or LSCLK by code option
  - Overflow period: 8selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2s and 8s)
  - Selectable window function (enable or disable): configurable clear enable period (50% or 75% of overflow period)
  - Selectable WDT operation: select Enable or Disable by code option
  - Readable WDT counter: WDT counter monitor function

- DMA (Direct Memory Access) controller
  - Channel: 2channel
  - Transfer unit: 8bit/16bit
  - Transfer count: 1 to 1024
  - Transfer cycle: 2 cycle transfer
  - Transfer address: Fixed addressing mode, inclement addressing mode, and decrement addressing mode
  - Transfer target: Special Function Register (SFR)/RAM → SFR/RAM (Transfer from/to Flash is not supported)
  - Transfer request: External pins, Serial communication unit, Successive approximation type A/D converter, 16bit timer, and Functional timer

- Low-speed Time base counter
  - Generate 8 frequency (128Hz to1Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
  - Selectable 3 interrupts from eight frequency internal pulse signals
  - 1Hz or 2Hz output from general purpose port
  - Built-in Frequency adjust function: Adjust range: Approximately -488ppm to +488ppm, adjust resolution: Approximately 0.119ppm

- Simplified RTC
  - Channel: 1channel
  - Count by a unit for one second from "00min. 00sec" to "59min. 59sec"
  - Selectable Periodical interrupt request from four periods (0.5s, 1s, 30s or 60s)
  - Built-in minute and second writing error protraction function

- Functional timer
  - Channel: 6channel
  - Built-in timer, capture, and PWM function by 16bit counter
  - One shot mode is available
  - Two types of PWM output with the same period and different duties, and complementary PWM output with the dead time
  - Monitor input signal duty and the period by capture function
  - Generate periodical interrupts, duty interrupts, and interrupts coincided with set value
  - Counter Start, Stop, Counter clear triggered by an external inputs or Timer
  - Generate Emergency stop and emergency stop interrupt triggered by an external input
  - Same start/stop among different channels of the functional timer
  - Selectable counter clock (external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channel

- 16-bit General timers
  - Channel: 6channel
  - 8 bits timer mode and 16bit timer mode
  - Same start/stop among different channels of 16bit (8bit) timer
  - Timer output (toggled by overflow)
  - Selectable counter clock (external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channel

- Serial communication unit
  - Synchronous Serial Port (SSIO) mode or UART mode is selectable
  - Channel: Max. 4channel

  < Synchronous Serial Port mode>
  - Selectable from Master and Slave
  - Selectable from LSB first or MSB first
  - Selectable 8-bit length or 16-bit length

  < UART mode>
  - Full-duplex communication mode and half-duplex communication mode
  - 5 to 8bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits
  - Selectable from Positive logic or Negative logic
  - Selectable from LSB first or MSB first
  - Configurable wide range communication speed
    32.768kHz operation clock: 1bit/s to 4,800bit/s
    24MHz operation clock: 600bit/s to 3Mbit/s
    16MHz operation clock: 300bit/s to 2Mbit/s
  - Built-in baud rate generator

- I^2C bus unit (Master / Slave)
  - Selectable from Master mode or Slave mode
  - Channel: 1channel

  < Master function >
  - Standard mode (100kbit/s), fast mode (400kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock synchronization)
  - 7bit address format (10bit address format is supported)

  < Slave function >
  - Standard mode (100kbit/s), fast mode (400kbit/s) and 1Mbps mode(1Mbit/s)
  - Clock stretch function
  - 7bit address format

- I^2C bus Master
  - Channel: 2channel
  - Standard mode (100kbit/s), fast mode (400kbit/s) and 1Mbps mode(1Mbit/s)
  - Handshake (Clock synchronization)
  - 7bit address format (10bit address format is supported)

- General-purpose ports (GPIO)
  - I/O port: Max. 74 (Including one pin for on-chip debug and pins for other shared functions)
  - Input port: Max. 2 (Including a shared function)
  - External interrupt port: Max. 12
  - LED driver port: Max. 73
  - Carrier frequency output function (for IR communication)

- Successive approximation type A/D converter (SA-ADC)
  - Channel: Max.12channel
  - Resolution: 10bit
  - Conversion time: Min. 2.25µs / channel (When the conversion clock is 8MHz)
  - Reference voltages are selectable
    (V_{DD} pin / Internal reference voltage (V_{REFI} = Approximately 1.55V) / External reference voltage (V_{REF} pin))
    – Selected channel repeat conversion
  - dedicated result register for each channel
  - Interrupt determining by upper limit or lower limit threshold of conversion result

- Voltage Level Supervisor (VLS)
  - Accuracy: ±4%
  - Threshold voltage: 12 selectable (from 1.85V to 4.00V)
  - Functional Voltage level detection reset (VLS reset)
  - Functional Voltage level detection interrupt (VLS0 interrupt)

- Analog comparator
  - Channel: 2channel
  - Selectable interrupt from the comparator output (rising edge or falling edge)
  - Selectable from sampling or without sampling
  - Comparable with external 2 inputs
  - Comparable with external input and internal reference voltage (0.8V)

- D/A converter
  - Channel: 1channel
  - Resolution: 8bit
  - Output impedance: 6k ohm (Typ.)
  - R-2R ladder type

- Buzzer
  - 4 buzzer mode (Continuous sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
  - 8frequencies (4.096kHz to 293Hz)
  - 15 step duty (1/16 to 15/16)
  - Selectable from positive logic buzzer output or negative logic buzzer output

- CRC (Cyclic Redundancy Check) generator
  - Generation equation: $X^{16}+X^{12}+X^{5}+1$
  - Selectable from LSB first or MSB first
  - Built-in Automatic program memory CRC calculation mode in HALT mode

- Safety Function (IEC60730/60335 Class B)
  - Automatic switching to the internal low-speed RC oscillation in case the low-speed crystal oscillation stopped
  - RAM/SFR guard
  - Automatic program memory CRC calculation
  - RAM parity error detection
  - ROM unused area access reset (instruction access)
  - Clock mutual monitoring
  - WDT counter monitoring
  - SA-ADC test
  - UART test
  - Synchronous serial I/O test
  - I^2C bus test
  - GPIO test

- Shipping package

Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Packing form and Product name	
			Tray	Tape & Reel
52 pin plastic TQFP	10.0 × 10.0 (12.0 × 12.0)	0.65	ML62Q1543C-NNNTBZWAX ML62Q1544C-NNNTBZWAX	ML62Q1543C-NNNTBZWBX ML62Q1544C-NNNTBZWBX
64 pin plastic TQFP	10.0 × 10.0 (12.0 × 12.0)	0.50	ML62Q1553C-NNNTBZWAX ML62Q1554C-NNNTBZWAX	ML62Q1553C-NNNTBZWBX ML62Q1554C-NNNTBZWBX
64 pin plastic QFP	14.0 × 14.0 (16.0 × 16.0)	0.80	ML62Q1553C-NNNGAZWAX ML62Q1554C-NNNGAZWAX	-
80 pin plastic QFP	14.0 × 14.0 (16.0 × 16.0)	0.65	ML62Q1563C-NNNGAZWAX ML62Q1564C-NNNGAZWAX	-

xxx: ROM code number

ML62Q1500C Group how to read the part number

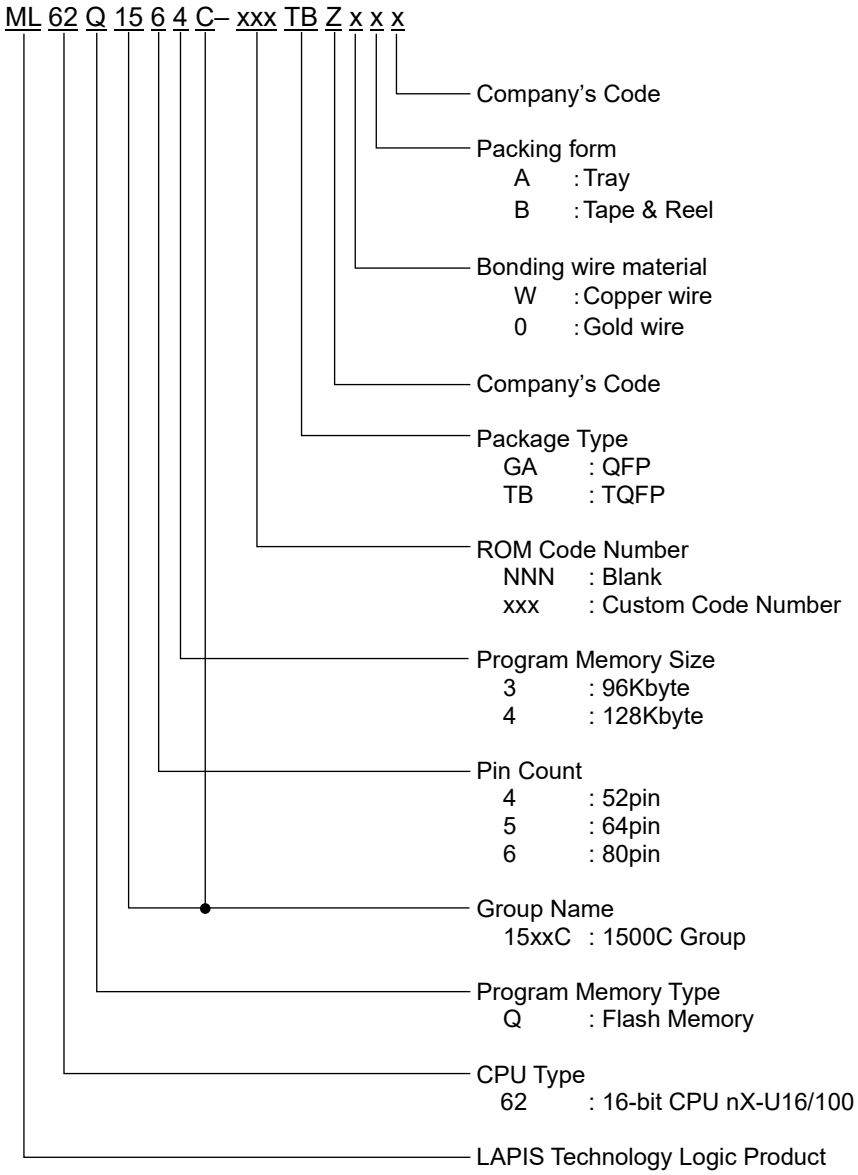


Figure 1 ML62Q1500C Group Part Number

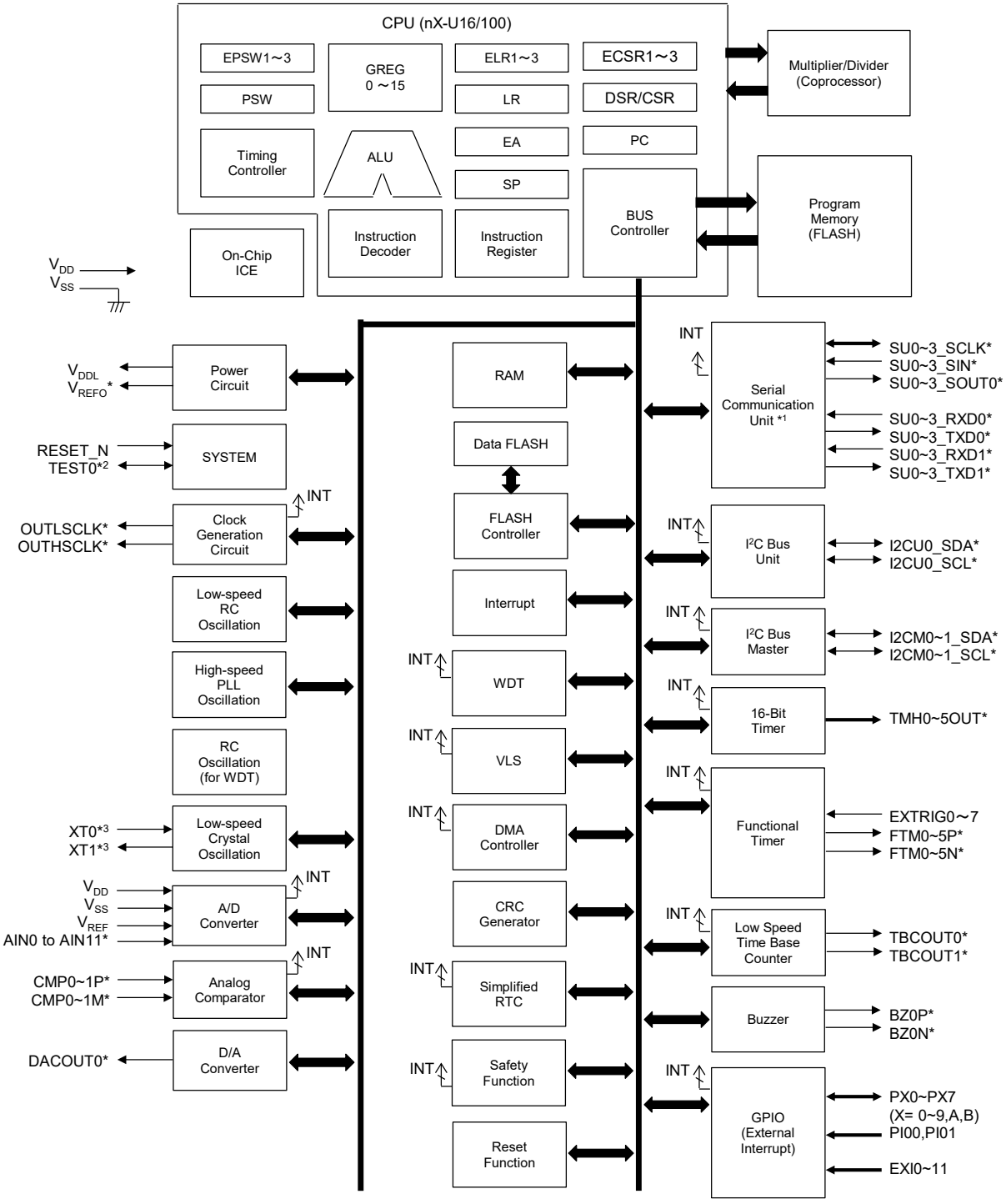
ML62Q1500C Group Main Function List

Table 2 ML62Q1500C Group Main Function List

Part number	Pin						Interrupt		Timer			Serial			Analog			
	Total pin-counts	Power pin counts	Reset Input pin	Input port *3	I/O port	LED drive port	Internal interrupt [source]	External interrupt [port]	Functional Timer [ch]	16-bit Timer [ch] *1	Simplified RTC [ch]	Serial communication unit (Full-duplex UART or Synchronous serial) [ch] *2	I²C bus unit (Master/Slave) [ch]	I²C bus interface (Master only) [ch]	10bit Successive approximation type A/D converter [ch]	Analog comparator [ch]	Analog comparator [input pin]	8bit D/A converter [ch]
ML62Q1543C	52	3	1	2	46	45	33	10	6	6	1	3	1	2	12	2	4	1
ML62Q1544C																		
ML62Q1553C	64				58	57	35					4						
ML62Q1554C																		
ML62Q1563C	80				74	73		12										
ML62Q1564C																		

*1: One 16-bit timer is configurable as two 8bit timers
*2: Full-duplex UART and Synchronous Serial Port cannot be used simultaneously in the same channel. One Full-duplex UART is configurable as two half-duplex UARTs.
*3: Shared with pins for crystal oscillation

BLOCK DIAGRAM



* : Indicates the shared function of general ports.

*1 : Shared UART and Synchronous Serial Port.

*2 : Not available as the input port when connecting to the on-chip debug emulator.

*3 : Not available as the input port when connecting to the crystal resonator.

Figure 2 ML62Q1500C Group Block Diagram

PIN CONFIGURATION

The port names in the pin-layout indicate 1st-function. Refer to Table-3 or Table-4 about other functions.

Pin Layout of 52pin TQFP Package

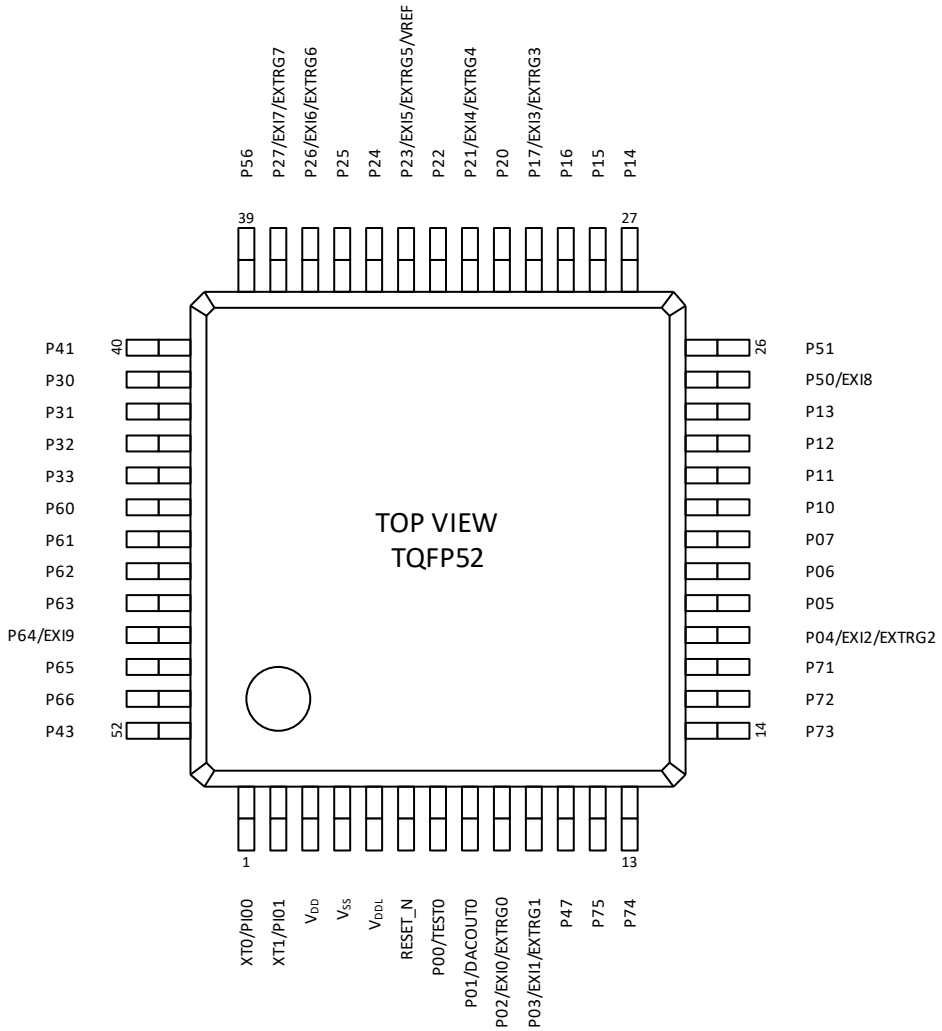


Figure 3 Pin Layout of 52pin TQFP52 Package

Pin Layout of 64pin TQFP/QFP Package

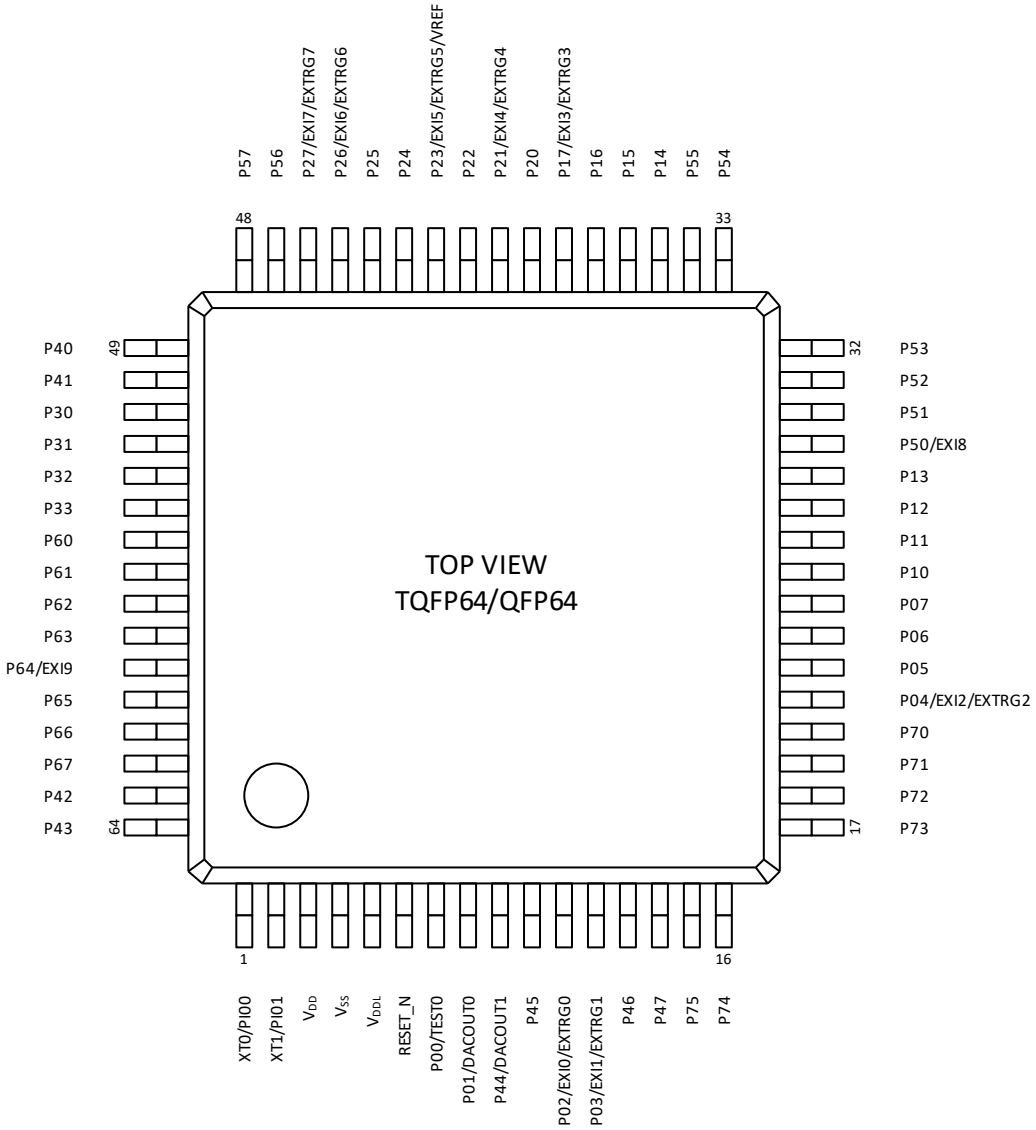


Figure 4 Pin Layout of 64pin TQFP/QFP Package

Pin Layout of 80pin QFP Package

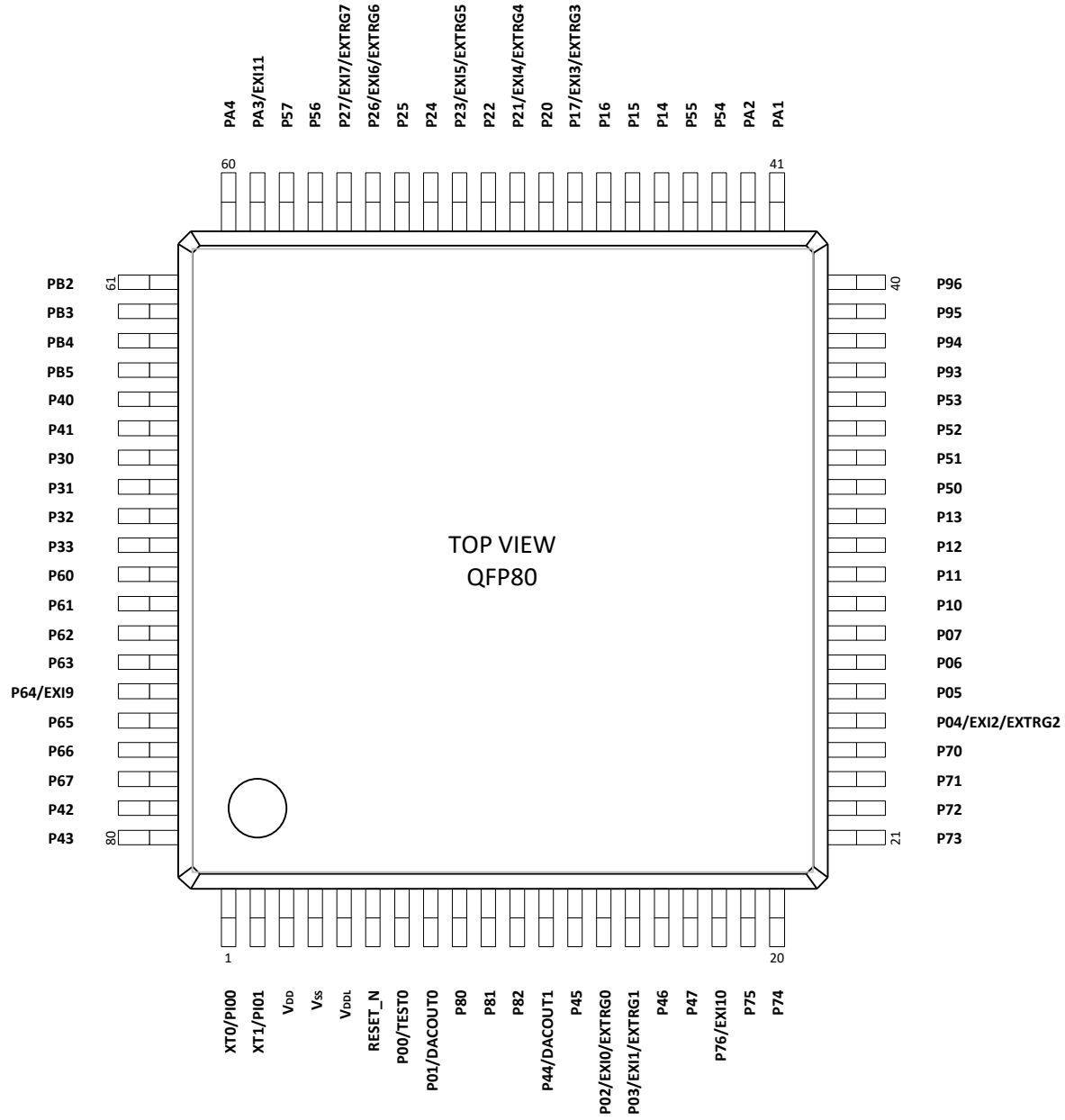


Figure 5 Pin Layout of 80pin QFP Package

PIN LIST

Table 3 Pin List (1/3)

Pin No.			Pin name (1st function)	1st function others	2nd function SIU	3rd function SIU	4th function I2C	5th function Timer	6th function others	7th function others	8th function ADC
52 Pin	64 Pin	80 Pin									
3	3	3	V_{DD}	-	-	-	-	-	-	-	-
4	4	4	V_{SS}	-	-	-	-	-	-	-	-
5	5	5	V_{DDL}	-	-	-	-	-	-	-	-
1	1	1	XT0	PI00	-	-	-	-	-	-	-
2	2	2	XT1	PI01	-	-	-	-	-	-	-
6	6	6	RESET_N	RESET_N	-	-	-	-	-	-	-
7	7	7	P00	TEST0	-	-	-	-	-	-	-
8	8	8	P01	DACOUT0	-	-	-	FTM3P	TBCOUT0	TBCOUT1	-
9	11	14	P02	EXI0 EXTRG0	SU0_RXD0 SU0_SIN	-	I2CU0_SCL	FTM0P	OUTLSCLK	CMP0M	-
10	12	15	P03	EXI1 EXTRG1	SU0_TXD0 SU0_SOUT	SU0_TXD1	I2CU0_SDA	FTM0N	OUTHSCLK	CMP0P	AIN11
17	21	25	P04	EXI2 EXTRG2	SU0_SCLK	-	I2CU0_SCL	TMH0OUT	-	-	-
18	22	26	P05	-	-	-	-	-	-	-	-
19	23	27	P06	-	-	-	I2CM0_SDA	-	-	-	-
20	24	28	P07	-	SU0_RXD1	SU0_RXD0	I2CM0_SCL	-	-	-	-
21	25	29	P10	-	SU0_TXD1		-	-	-	-	-
22	26	30	P11	-	SU0_SCLK		-	-	-	-	-
23	27	31	P12	-	SU0_RXD0 SU0_SIN		-	TMH4OUT	-	-	-
24	28	32	P13	-	SU0_TXD0 SU0_SOUT	SU0_TXD1	-	TMH1OUT	-	TMH3OUT	-
27	35	45	P14	-	-	-	-	-	-	-	-
28	36	46	P15	-	-	-	I2CU0_SDA		-	-	-
29	37	47	P16	-	SU1_SCLK	-	I2CU0_SCL	TMH5OUT	-	-	-
30	38	48	P17	EXI3 EXTRG3	SU0_RXD1	SU0_RXD0	-	FTM1P	TBCOUT0	BZ0P	AIN0
31	39	49	P20	-	SU0_TXD1	-	-	FTM1N	TBCOUT1	BZ0N	AIN1
32	40	50	P21	EXI4 EXTRG4	SU1_RXD0 SU1_SIN	-	-	FTM2P	OUTLSCLK	-	AIN2
33	41	51	P22	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	I2CM0_SDA	FTM2N	OUTHSCLK	-	AIN3
34	42	52	P23	EXI5 EXTRG5 V_{REF}	SU1_SCLK	-	I2CM0_SCL	TMH2OUT	-	-	V_{REFO}
35	43	53	P24	-	SU1_RXD0 SU1_SIN	-	-	-	-	-	AIN4
36	44	54	P25	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	-	-	-	-	AIN5
37	45	55	P26	EXI6 EXTRG6	SU1_RXD1	SU1_RXD0	I2CU0_SDA	FTM3P	TBCOUT0	BZ0P	AIN6
38	46	56	P27	EXI7 EXTRG7	SU1_TXD1	SU2_SCLK *1	I2CU0_SCL	FTM3N	TBCOUT1	BZ0N	AIN7

*1: No assignment to products of 52 PIN-and 80 PIN package.

Table 3 Pin List (2/3)

Pin No.			Pin name (1st function)	1st function others	2nd function SIU	3rd function SIU	4th function I2C	5th function Timer	6th function others	7th function others	8th function ADC
52 Pin	64 Pin	80 Pin									
41	51	67	P30	-	-	-	-	-	-	-	-
42	52	68	P31	-	-	-	-	-	TBCOUT0	TBCOUT1	-
43	53	69	P32	-	SU1_RXD1	SU1_RXD0	-	-	-	-	-
44	54	70	P33	-	SU1_TXD1	-	-	TMH3OUT	-	-	-
-	49	65	P40	-	-	-	-	-	-	-	-
40	50	66	P41	-	-	-	-	-	-	-	-
-	63	79	P42	-	SU3_TXD1 *1	-	-	-	-	-	-
52	64	80	P43	-	-	-	-	-	TBCOUT0	TBCOUT1	AIN10
-	9	12	P44	-	-	-	-	FTM3N	-	-	-
-	10	13	P45	-	-		-	-	-	-	-
-	13	16	P46	-	-	-	I2CU0_SDA	FTM1N	-	-	-
11	14	17	P47	-	SU0_SCLK	-	I2CU0_SCL *1	FTM1P	-	-	-
25	29	33	P50	EXI8	-	-	-	-	-	-	-
26	30	34	P51	-	-	-	-	-	-	-	-
-	31	35	P52	-	-	-	-	-	-	-	-
-	32	36	P53	-	-	-	-	-	-	-	-
-	33	43	P54	-	SU2_RXD1 *1	SU2_RXD0 *1	-	-	-	-	-
-	34	44	P55	-	SU2_TXD1 *1	-	-	-	-	-	-
39	47	57	P56	-	SU2_RXD0 SU2_SIN *1	-	-	-	-	-	-
-	48	58	P57	-	SU2_TXD0 SU2_SOUT *1	SU2_TXD1 *1	-	-	-	-	-
45	55	71	P60	-	-	-	I2CM1_SCL	-	-	-	-
46	56	72	P61	-	-	-	I2CM1_SDA	-	-	-	-
47	57	73	P62	-	-	-	-	FTM4N	-	CMP1P	-
48	58	74	P63	-	-	-	-	FTM4P	-	CMP1M	-
49	59	75	P64	EXI9	SU3_RXD0 SU3_SIN	-	-	FTM5P	-	-	-
50	60	76	P65	-	SU3_TXD0 SU3_SOUT	SU3_TXD1	-	FTM5N	-	-	AIN8
51	61	77	P66	-	SU3_SCLK	-	-	-	-	-	AIN9
-	62	78	P67	-	SU3_RXD1 *1	SU3_RXD0 *1	-	-	-	-	-
-	20	24	P70	-	-	-	-	-	-	-	-
16	19	23	P71	-	-	-	-	-	-	-	-
15	18	22	P72	-	-	-	-	-	-	-	-
14	17	21	P73	-	-	-	-	-	-	-	-
13	16	20	P74	-	-	-	-	-	-	-	-
12	15	19	P75	-	-	-	-	-	-	-	-
-	-	18	P76	EXI10	-	-	-	-	-	-	-

*1: No assignment to products of 52 PIN-package.

Table 3 Pin List (3/3)

Pin No.			Pin name (1st function)	1st function others	2nd function SIU	3rd function SIU	4th function I2C	5th function Timer	6th function others	7th function others	8th function ADC
52 Pin	64 Pin	80 Pin									
-	-	9	P80	-	-	-	-	-	-	-	-
-	-	10	P81	-	-	-	-	-	-	-	-
-	-	11	P82	-	-	-	-	-	-	-	-
-	-	37	P93	-	-	-	-	-	-	-	-
-	-	38	P94	-	-	-	-	-	-	-	-
-	-	39	P95	-	-	-	-	-	-	-	-
-	-	40	P96	-	-	-	-	-	-	-	-
-	-	41	PA1	-	-	-	-	-	-	-	-
-	-	42	PA2	-	-	-	-	-	-	-	-
-	-	59	PA3	EXI11	SU2_SCLK *1	-	-	-	-	-	-
-	-	60	PA4	-	-	-	-	-	-	-	-
-	-	61	PB2	-	-	-	-	-	-	-	-
-	-	62	PB3	-	-	-	-	-	-	-	-
-	-	63	PB4	-	-	-	-	-	-	-	-
-	-	64	PB5	-	-	-	-	-	-	-	-

*1: No assignment to products of 52 PIN and 64 PIN-packages.

PIN DESCRIPTION

Table 4 Pin Description (1/5)

Function	Signal name	Pin name	I/O	Description	Logic
Power	-	V_{SS}	-	Negative power supply pin (-)	-
	-	V_{DD}	-	Positive power supply pin (+). Connect a capacitor C_V between this pin and V_{SS}.	-
	-	V_{DDL}	-	Power supply pin for internal logic (internal regulator's output). Connect a capacitor C_V (1µF) between this pin and V_{SS}.	-
Test	TEST0	P00	I/O	Input pin for testing. Also, used for on-chip debug interface or ISP function. P00 is initialized as pull-up input mode by the system reset.	-
System	V_{REFO}	P23	-	Reference voltage output.	-
	RESET_N	RESET_N	I	Reset input. Applying "L" level shifts the MCU in system reset mode. Applying "H" level shifts the CPU in program running mode. Used for on-chip debug interface and ISP function. No pull-up resistor is installed.	Negative
	XT0	XT0	I	Low-speed crystal oscillation pins Connect 32.768kHz crystal resonator and have capacitors between the pin and V_{SS}.	-
	XT1	XT1	O		-
	OUTLSCLK	P02	O	Low-speed clock output.	-
		P21			
	OUTHSCLK	P03	O	High-speed clock output.	-
		P22			
General input port (GPI)	PI00, PI01	XT0, XT1	I	General purpose input. Not available as general inputs when using the crystal resonator.	Positive
General port (GPIO)	P00	P00	I/O	General purpose I/O port - High impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output Not available to use as I/O pin when using for on-chip debug interface or ISP function.	Positive
	P01 – P07	P01 – P07	I/O	General I/O port - High impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output	Positive
	P10 – P17	P10 – P17			
	P20 – P27	P20 – P27			
	P30 – P33	P30 – P33			
	P40 – P47	P40 – P47			
	P50 – P57	P50 – P57			
	P60 – P67	P60 – P67			
	P70 – P76	P70 – P76			
	P80 – P82	P80 – P82			
	P93 – P96	P93 – P96			
	PA1 – PA4	PA1 – PA4			
	PB2 – PB5	PB2 – PB5			

Table 4 Pin Description (2/5)

Function	Signal name	Pin name	I/O	Description	Logic
UART	SU0_TXD0	P03	O	Serial communication unit0 UART0 data output	Positive
		P13			
	SU0_RXD0	P02	I	Serial communication unit0 Full-duplex data input Serial communication unit0 UART0 data input	Positive
		P07			
		P12			
		P17			
	SU0_TXD1	P03	O	Serial communication unit0 Full-duplex data output Serial communication unit0 UART1 data output	Positive
		P10			
		P13			
		P20			
	SU0_RXD1	P07	I	Serial communication unit0 UART1 data input	Positive
		P17			
	SU1_TXD0	P22	O	Serial communication unit1 UART0 data output	Positive
		P25			
	SU1_RXD0	P21	I	Serial communication unit1 Full-duplex data input Serial communication unit1 UART0 data input	Positive
		P24			
		P26			
		P32			
	SU1_TXD1	P22	O	Serial communication unit1 Full-duplex data output Serial communication unit1 UART1 data output	Positive
		P25			
		P27			
		P33			
	SU1_RXD1	P26	I	Serial communication unit1 UART1 data input	Positive
		P32			
	SU2_TXD0	P57	O	Serial communication unit2 UART0 data output	Positive
	SU2_RXD0	P54	I	Serial communication unit2 Full-duplex data input Serial communication unit2 UART0 data input	Positive
		P56			
	SU2_TXD1	P55	O	Serial communication unit2 Full-duplex data output Serial communication unit2 UART1 data output	Positive
		P57			
	SU2_RXD1	P54	I	Serial communication unit2 UART1 data input	Positive
	SU3_TXD0	P65	O	Serial communication unit3 UART0 data output	Positive
	SU3_RXD0	P64	I	Serial communication unit3 Full-duplex data input Serial communication unit3 UART0 data input	Positive
		P67			
	SU3_TXD1	P42	O	Serial communication unit3 Full-duplex data output Serial communication unit3 UART1 data output	Positive
		P65			
	SU3_RXD1	P67	I	Serial communication unit3 UART1 data input	Positive

Table 4 Pin Description (3/5)

Function	Signal name	Pin name	I/O	Description	Logic
Synchronous Serial Port	SU0_SIN	P02	I	Serial communication unit0 Synchronous serial data input	Positive
		P12			
	SU0_SCK	P04	I/O	Serial communication unit0 Synchronous serial clock I/O	Positive
		P11			
		P47			
	SU0_SOUT	P03	O	Serial communication unit0 Synchronous serial data output	Positive
		P13			
	SU1_SIN	P21	I	Serial communication unit1 Synchronous serial data input	Positive
		P24			
	SU1_SCK	P16	I/O	Serial communication unit1 Synchronous serial clock I/O	Positive
		P23			
	SU1_SOUT	P22	O	Serial communication unit1 Synchronous serial data output	Positive
		P25			
	SU2_SIN	P56	I	Serial communication unit2 Synchronous serial data	Positive
	SU2_SCLK	P27	I/O	Serial communication unit2 Synchronous serial clock I/O	Positive
		PA3			
	SU2_SOUT	P57	O	Serial communication unit2 Synchronous serial data output	Positive
	SU3_SIN	P64	I	Serial communication unit3 Synchronous serial data input	Positive
	SU3_SCLK	P66	I/O	Serial communication unit3 Synchronous serial clock I/O	Positive
	SU3_SOUT	P65	O	Serial communication unit3 Synchronous serial data output	Positive
I^2C Bus	I2CU0_SDA	P03	I/O	I^2C Unit0 (Master and Salve) Data I/O N-channel open drain Connect a pull-up resistor externally	Positive
		P15			
		P26			
		P46			
	I2CU0_SCL	P02	I/O	I^2C Unit0 (Master and Salve) Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive
		P04			
		P16			
		P27			
		P47			
	I2CM0_SDA	P06	I/O	I^2C Master0 Data I/O pin N-channel open drain output Connect a pull-up resistor externally	Positive
		P22			
	I2CM0_SCL	P07	I/O	I^2C Master0 Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive
		P23			
	I2CM1_SDA	P61	I/O	I^2C Master1 Data I/O N-channel open drain output Connect a pull-up resistor externally	Positive
	I2CM1_SCL	P60	I/O	I^2C Master1 Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive

Table 4 Pin Description (4/5)

Function	Signal name	Pin name	I/O	Description	Logic
Functional Timer (FTM)	FTM0P	P02	O	Functional Timer0 P output	Positive
	FTM0N	P03	O	Functional Timer0 N output	Negative
	FTM1P	P17	O	Functional Timer1 P output	Positive
		P47			
	FTM1N	P20	O	Functional Timer1 N output	Negative
		P46			
	FTM2P	P21	O	Functional Timer2 P output	Positive
	FTM2N	P22	O	Functional Timer2 N output	Negative
	FTM3P	P01	O	Functional Timer3 P output	Positive
		P26			
	FTM3N	P27	O	Functional Timer3 N output	Negative
		P44			
	FTM4P	P63	O	Functional Timer4 P output	Positive
	FTM4N	P62	O	Functional Timer4 N output	Negative
	FTM5P	P64	O	Functional Timer5 P output	Positive
	FTM5N	P65	O	Functional Timer5 N output	Negative
	EXTRG0	P02	I	Functional Timer event trigger input	-
	EXTRG1	P03	I	Functional Timer event trigger input	-
	EXTRG2	P04	I	Functional Timer event trigger input	-
	EXTRG3	P17	I	Functional Timer event trigger input	-
	EXTRG4	P21	I	Functional Timer event trigger input	-
	EXTRG5	P23	I	Functional Timer event trigger input	-
	EXTRG6	P26	I	Functional Timer event trigger input	-
	EXTRG7	P27	I	Functional Timer event trigger input	-
16-bit Timer	TMH0OUT	P04	O	16bit General Timer 0 output	Positive
	TMH1OUT	P13	O	16bit General Timer 1 output	Positive
	TMH2OUT	P23	O	16bit General Timer 2 output	Positive
	TMH3OUT	P13	O	16bit General Timer 3 output	Positive
		P33			
	TMH4OUT	P12	O	16bit General Timer 4 output	Positive
	TMH5OUT	P16	O	16bit General Timer 5 output	Positive
	EXTRG0	P02	I	16bit Timer trigger input	-
	EXTRG1	P03	I	16bit Timer trigger input	-
Low-speed Time Base Counter (LTBC)	TBCOUT0	P01	O	The virtual frequency adjustment signal output or The low speed time base counter output signal	Positive
		P17			
		P26			
		P31			
		P43			
	TBCOUT1	P01	O	1Hz/2Hz clock output for the Simplified RTC	Positive
		P20			
		P27			
		P31			
		P43			
Buzzer	BZ0P	P17	O	Buzzer output (positive phase)	Positive
		P26			
	BZ0N	P20	O	Buzzer output (negative phase)	Negative
		P27			

Table 4 Pin Description (5/5)

Function	Signal name	Pin name	I/O	Description	Logic
External Interrupt	EXI0	P02	I	External Interrupt 0 Input	-
	EXI1	P03	I	External Interrupt 1 Input	-
	EXI2	P04	I	External Interrupt 2 Input	-
	EXI3	P17	I	External Interrupt 3 Input	-
	EXI4	P21	I	External Interrupt 4 Input	-
	EXI5	P23	I	External Interrupt 5 Input	-
	EXI6	P26	I	External Interrupt 6 Input	-
	EXI7	P27	I	External Interrupt 7 Input	-
	EXI8	P50	I	External Interrupt 8 Input	-
	EXI9	P64	I	External Interrupt 9 Input	-
	EXI10	P76	I	External Interrupt 10 Input	-
	EXI11	PA3	I	External Interrupt 11 Input	-
Successive approximation type A/D converter	V_{REF}	P23	-	SA-ADC external reference voltage input	-
	AIN0	P17	I	SA-ADC channel 0 input	-
	AIN1	P20	I	SA-ADC channel 1 input	-
	AIN2	P21	I	SA-ADC channel 2 input	-
	AIN3	P22	I	SA-ADC channel 3 input	-
	AIN4	P24	I	SA-ADC channel 4 input	-
	AIN5	P25	I	SA-ADC channel 5 input	-
	AIN6	P26	I	SA-ADC channel 6 input	-
	AIN7	P27	I	SA-ADC channel 7 input	-
	AIN8	P65	I	SA-ADC channel 8 input	-
	AIN9	P66	I	SA-ADC channel 9 input	-
	AIN10	P43	I	SA-ADC channel 10 input	-
	AIN11	P03	I	SA-ADC channel 11 input	-
Analog comparator	CMP0P	P03	I	Comparator input 0 (noninverting input)	-
	CMP0M	P02	I	Comparator input 0 (inverting input)	-
	CMP1P	P62	I	Comparator input 1 (noninverting input)	-
	CMP1M	P63	I	Comparator input 1 (inverting input)	-
D/A converter	DACOUT	P01	O	D/A converter 0 output	-

TERMINATION OF UNUSED PINS

Table 5 Termination of unused pins

Pin	Recommended pin termination
RESET_N	Connect to V_{DD}.
P00/TEST0	Connect to V_{DD} with initial state (pulled-up input mode)
XT0/PI00, XT1/PI01	Open the pins with the internal initial condition of High impedance mode (input/output is disable).
P01 to P07	
P10 to P17	
P20 to P27	
P30 to P33	
P40 to P47	
P50 to P57	
P60 to P67	
P70 to P76	
P80 to P82	
P93 to P96	
PA1 to PA4	
PB2 to PB5	

[Note]

- **Terminate unused input pins according to the table 5 in order to avoid unexpected through-current in the pins.**

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V_{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta = +25°C		-0.3 to +2.0	V
Input voltage	V_{IN}	Ta = +25°C		-0.3 to V_{DD}+0.3*1	V
Output voltage	V_{OUT}	Ta = +25°C		-0.3 to V_{DD}+0.3*1	V
"H" level output current	I_{OUTH}	Ta = +25°C	1pin	-40*2	mA
			Total	-180*2	
"L" level output current	I_{OUTL}	Ta = +25°C	1pin	+40	mA
			Total	+180	
Power dissipation	PD	Ta = +25°C		1	W
Storage temperature	T_{STG}	-		-55 to +150	°C

*1 6.5V or lower
*2 The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

[Note]
- **Use the product within absolute maximum ratings. The absolute maximum ratings are conditions which may physically deteriorate the quality of product.**

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambient)	Ta	-	-40 to +105	°C
Operating temperature (Chip-Junction)	Tj	-	-40 to +115	
Operating voltage 1	V_{DD}	-	1.6 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.6 to 5.5V	30k to 4M	Hz
		V_{DD} = 1.8 to 5.5V	30k to 25M	
V_{DDL} pin external capacitance	C_L	-	1.0 ±30%	µF

Thermal characteristics

The maximum chip-junction temperature, T_{jmax}, may be calculated using the following equation.

$T_{j\ max} = T_{a\ max} + P_{D\ max} \times \theta_{ja}$
$T_{a\ max}$: maximum ambient temperature
$P_{D\ max}$: LSI maximum power dissipation
θ_{ja} : Package junction to ambient thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

Parameter	Symbol	Package type	Value		Unit
			L1	L2	
Thermal resistance	θ_{ja}	TQFP52	61.7	56.7	°C/W
		TQFP64	63.2	58.2	
		QFP64	47.2	43.3	
		QFP80	55.5	51.6	

PCB conditions:

PCB name	L1	L2	Unit
PCB size（L / W / T）	114.3 / 76.2 / 1.6	114.3 / 76.2 / 1.6	mm
Number of layers	1	2	layer
Wiring density	60% (top layer)	60% (top and bottom layer)	-
Wind condition	No wind (0m/s)		-

Current Consumption

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.*3	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. All oscillations are stopped.	Ta = -40 to +85°C	-	0.8	34	µA	1
			Ta = -40 to +105°C	-		68		
Supply current 1	IDD1	CPU is in STOP state. All oscillations are stopped.	Ta = -40 to +85°C	-	1.2	38		
			Ta = -40 to +105°C	-		74		
Supply current 2-1	IDD2-1	Low-speed RC32K Oscillating.*1 CPU is in HALT state. PLL oscillation is stopped.	Ta = -40 to +85°C	-	4.0	42		
			Ta = -40 to +105°C	-		80		
Supply current 2-2	IDD2-2	Low-speed Crystal Oscillating.*1*4 CPU is in HALT state. PLL oscillation is stopped.	Ta = -40 to +85°C	-	3.0	42		
			Ta = -40 to +105°C	-		80		
Supply current 2-3	IDD2-3	Low-speed Crystal Oscillating.*1*4 CPU is in HALT-C state. PLL oscillation is stopped.	Ta = -40 to +85°C	-	2.2	40		
			Ta = -40 to +105°C	-		76		
Supply current 3	IDD3	CPU: Running with low-speed RC32K oscillation clock*1*2 PLL oscillation is stopped.	Ta = -40 to +105°C	-	17	104		
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock*1*2 PLL 16MHz is oscillating. V_{DD} = 1.8~5.5V	Ta = -40 to +105°C	-	3.2	4.0	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock*1*2 PLL 24MHz is oscillating. V_{DD} = 1.8~5.5V	Ta = -40 to +105°C	-	4.5	5.2		

*1 LTBC and WDT is operating, Significant bits of BCKCON0-3 and BRECON0-3 registers are all "1"
*2 CPU running in wait mode
*3 On the condition of V_{DD} = 3.0V, Ta = +25 °C
*4 When the noise filter is not used in the low power consumption mode

Low-speed Crystal Oscillation

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105ºC, unless otherwise specified)

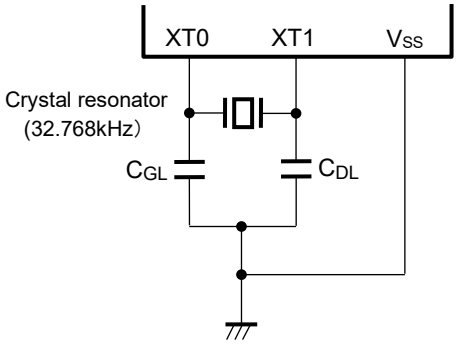
Parameter	Symbol	Condition	Range			Unit
			Min.	Typ.	Max.	
Crystal oscillation frequency *1 *2	f_{XTL}	-	-	32.768	-	kHz
Crystal oscillation start time	T_{XTL}	-	-	-	2	s

*1: The oscillation frequency is determined by the oscillation circuit, crystal resonator and the external capacitance (C_{GL}/C_{DL}). As those parameters changes depending the crystal resonator, it requires evaluation on the actual PCB circuit for matching. Ask crystal resonator makers for matching and confirm the oscillation characteristics.

*2: The quality of oscillation characteristics might be lost, depending on material of PCB, condition of wiring capacitance or parasitic capacitance on the external circuits. Note for designing the external circuit.

- Make the wires on the external circuit as short as possible.
- Place the crystal resonator and oscillation circuit as close to the MCU as possible and make the wires between the external capacitance and crystal resonator as short as possible.
- Ensure no signal line flowing big current runs near the oscillation circuit.
- Ensure no signal line runs under and near the oscillation circuit.
- Make ground of external capacitance the same as MCU ground V_{SS} pin and connect them to the ground that has low variation of current and voltage.
- The quality of oscillation characteristics might be lost depending on operating environment due to moisture absorption of PCB and condensation of PCB surface, recommended to have measures such as covering the oscillation circuit with resin.

Low-speed Crystal Oscillation external circuit example



External Clock Input

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105ºC, unless otherwise specified)

Parameter	Symbol	Condition	Range			Unit
			Min.	Typ.	Max.	
Input Frequency	f_{EXCK}	-	Typ. -1.0%	32.768	Typ. +1.0%	kHz
Input pulse width	t_{EXCKW}	-	1/fEXCK x 0.4	-	1/fEXCK x 0.6	s

On-chip Oscillator

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed RC oscillator frequency accuracy 1 Without software adjustment	f_{RCL1}	Ta = +25°C V_{DD} = 1.8 to 5.5V	Typ. -1.0%	32.768	Typ. +1.0%	kHz	1
		Ta = -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ. -2.5%	32.768	Typ. +2.5%		
		Ta = -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ. -3.0%	32.768	Typ. +3.0%		
		V_{DD} = 1.6 to 1.8V	Typ. -3.5%	32.768	Typ. +3.5%		
Low-speed RC oscillator frequency accuracy 2 With software adjustment	f_{RCL2}	Ta = -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ. -1.0%	32.768	Typ. +1.0%		
		Ta = -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ. -1.5%	32.768	Typ. +1.5%		
PLL oscillation frequency accuracy 1 Without software adjustment	f_{PLL1}	Ta = -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ. -2.5%	16/24	Typ. +2.5%	MHz	
		Ta = -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ. -3.0%	16/24	Typ. +3.0%		
		V_{DD} = 1.6 to 5.5V	Typ. -3.5%	16/24	Typ. +3.5%		
PLL oscillation frequency accuracy 2 With software adjustment	f_{PLL2}	Ta = -40 to +85°C V_{DD} = 1.8 to 5.5V	Typ. -1.0%	16/24	Typ. +1.0%		
		Ta = -40 to +105°C V_{DD} = 1.8 to 5.5V	Typ. -1.5%	16/24	Typ. +1.5%		
PLL oscillation start time	T_{PLL}	V_{DD} = 1.6 to 5.5V	-	-	2	ms	
1kHz Low-speed RC oscillator (for WDT) frequency accuracy	f_{RC1K}	Ta = -40 to +105°C V_{DD} = 1.6 to 5.5V	0.5	1	2.5	kHz	

Input / Output pin 1

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage1 "H"/"L" level (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P76) (P80-P82) (P93-P96) (PA1-PA4) (PB2-PB5)	VOH1	IOH1 = -10mA V_{DD} ≥ 4.5V		V_{DD} -1.5	-	-	V	2
		IOH1 = -1mA V_{DD} ≥ 1.6V		V_{DD} -0.5	-	-		
	VOL1	IOL1 = +10mA V_{DD} ≥ 4.5V		-	-	1.5		
		IOL1 = +1mA V_{DD} ≥ 1.6V		-	-	0.5		
Output voltage2 "L" level (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P76) (P80-P82) (P93-P96) (PA1-PA4) (PB2-PB5)	VOL2	When N-ch open drain output mode is selected	IOL2 = +15mA V_{DD} ≥ 4.5V	-	-	0.7		
			IOL2 = +8mA V_{DD} ≥ 3.0V	-	-	0.5		
			IOL2 = +3mA V_{DD} ≥ 2.0V	-	-	0.4		
			IOL2 = +2mA V_{DD} ≥ 1.6V	-	-	0.4		

Input / Output pin 2

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	V_{DD} ≥ 4.5V	-10*3*5	-	-	mA	3
			V_{DD} ≥ 1.6V	-1*3*5	-	-		
"H" level output total current *1*4	IOH3	Total of 'P00-P07, P10-P13, P44-P47, P50-P53, P70-P76, P80-P82, P93-P96' or Total of 'P14-P17, P20-P27, P30-P33, P40-P43, P54-P57 P60-P67, PA1-PA4, PB2-PB5' (duty ≤ 50%)	V_{DD} ≥ 4.5V	-90*5	-	-		
			V_{DD} ≥ 1.6V	-20*5	-	-		
		All pin totals (duty ≤ 50%)	V_{DD} ≥ 4.5V	-180*5	-	-		
			V_{DD} ≥ 1.6V	-40*5	-	-		
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	V_{DD} ≥ 4.5V	-	-	10*3		
			V_{DD} ≥ 1.6V	-	-	1*3		
"L" level output current2 *6	IOL2	1pin (N-ch open drain output mode)	V_{DD} ≥ 4.5V	-	-	15*3		
			V_{DD} ≥ 3.0V	-	-	8*3		
			V_{DD} ≥ 2.0V	-	-	3*3		
			V_{DD} ≥ 1.6V	-	-	2*3		
"L" level output total current *2*4	IOL3	Total of 'P00-P07, P10-P13, P44-P47, P50-P53, P70-P76, P80-P82, P93-P96' or Total of 'P14-P17, P20-P27, P30-P33, P40-P43, P54-P57 P60-P67, PA1-PA4, PB2-PB5' (N-ch open drain output mode, duty ≤ 50%)	V_{DD} ≥ 4.5V	-	-	90		
			V_{DD} ≥ 3.0V	-	-	40		
			V_{DD} ≥ 2.0V	-	-	15		
			V_{DD} ≥ 1.6V	-	-	10		
		All pin totals (N-ch open drain output mode, duty ≤ 50%)	V_{DD} ≥ 4.5V	-	-	180		
			V_{DD} ≥ 1.6V	-	-	20		
Output leak (P00-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P76) (P80-P82) (P93-P96) (PA1-PA4) (PB2-PB5)	IOOH	VOH = V_{DD} (High impedance mode)		-	-	+1	μA	
	IOOL	VOL = V_{SS} (High impedance mode)		-1*5	-	-		

*1: Sink-out current from V_{DD} to the output pin, which can guarantee the device operation.
*2: Sink-in current from the output pin to V_{SS}, which can guarantee the device operation.
*3: Do not beyond total current.
*4: The total current is on the condition of Duty ≤ 50% (same applies to IOH1).
When the duty > 50% the total current is calculated by following formula.
Total current = IOL3 x 50/n (When the duty is n%)
<For an example> When IOL3 = 100mA and n = 80%,
Total current = IOL3 x 50/80 = 62.5mA
Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.
Do not apply current larger than Absolute Maximum Ratings.
*5: The current flowing out the LSI through the pin is described in the negative number.
The applicable maximum current is the absolute value.
For example, -1mA means the maximum current 1mA flows out the LSI through the pin.
*6: VOH1, VOL1, and VOL2 are satisfied with this spec.

Input / Output pin 3

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input current1 (RESET_N)	IIH1	VIH1 = V_{DD}	-	-	1	µA	4
	IIL1	VIL1 = V_{SS}	-1*1	-	-		
Input current2 (P00/TEST0)	IIL2	VIL2 = V_{SS} (pull-up mode) *2	-1500*1	-300*1	-20*1		
	V/IIL2	VIL2 = V_{SS} (pull-up mode) *2	3.7	10	80	kΩ	
	IIH2Z	VIH1 = V_{DD} (High impedance mode)	-	-	1	µA	
	IIL2Z	VIL1 = V_{SS} (High impedance mode)	-1*1	-	-		
Input current3 (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P82) (P93-P96) (PA1-PA4) (PB2-PB5)	IIL3	VIL1 = V_{SS} (pull-up mode) *2	-250*1	-30*1	-2*1		
	V/IIL3	VIL1 = V_{SS} (pull-up mode) *2	22	100	800	kΩ	
	IIH3Z	VIH1 = V_{DD} (High impedance mode)	-	-	1	µA	
	IIL3Z	VIL1 = V_{SS} (High impedance mode)	-1*1	-	-		
Input current4 (PI00-PI01)	IIH4	VIH1 = V_{DD}	-	-	1		
	IIL4	VIL1 = V_{SS}	-1*1	-	-		
Input voltage1 (RESET_N) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P82) (P93-P96) (PA1-PA4) (PB2-PB5) (PI00-PI01)	VIH1	-	0.7 x V_{DD}	-	V_{DD}	V	5
	VIL1	-	0	-	0.3 x V_{DD}		
Input voltage2 (P00/TEST0)	VIH2	-	0.7 x V_{DD}	-	V_{DD}		
	VIL2	-	0	-	0.25 x V_{DD}		
Pin capacitance (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33) (P40-P47) (P50-P57) (P60-P67) (P70-P77) (P80-P82) (P93-P96) (PA1-PA4) (PB2-PB5) (PI00-PI01)	CPIN	f = 10kHz Ta = +25°C	-	-	10	pF	-

*1:The current flowing out the LSI through the pin is described in the negative number. The applicable maximum current is the absolute value. For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

*2:Measurement conditions: Typ.: V_{DD} = 3.0V, Max.: V_{DD} = 1.6V, Min.: V_{DD} = 5.5V

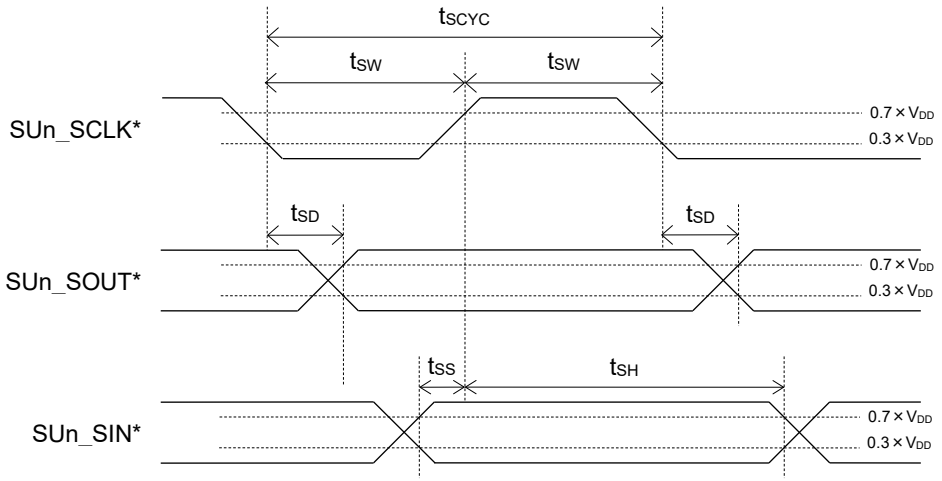
Synchronous Serial Port

Slave mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle	t_{SCYC}	-	1 *2	-	-	µs
SCK input pulse width	t_{SW}	-	0.5 *3	-	-	
SOUT output delay time	t_{SD}	V_{DD} = 2.4 to 5.5V	-	-	100+ HSCLK*1×3	ns
		V_{DD} = 1.8 to 5.5V	-	-	200+ HSCLK*1×3	
SIN input setup time	t_{SS}	-	HSCLK*1 x1	-	-	
SIN input hold time	t_{SH}	-	80+ HSCLK*1×3	-	-	

*1: Cycle of high speed clock
*2: Need input cycles of HSCLK x8 or longer
*3: Need input cycles of HSCLK x4 or longer



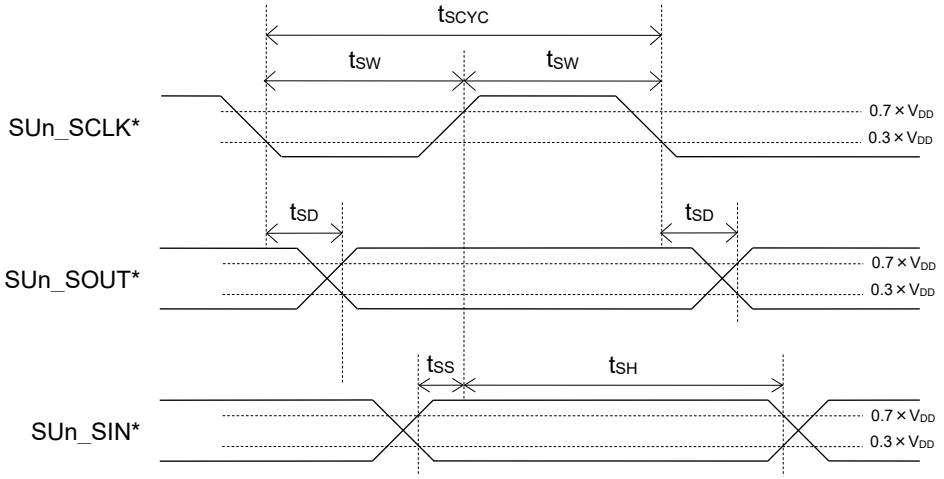
*: 2nd to 8th function of port, n=0~3

Master mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK output cycle	t_{SCYC}	-	-	SCLK*1	-	ns
SCK output pulse width	t_{SW}	-	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	
SOUT output delay time	t_{SD}	V_{DD} = 2.4 to 5.5V	-	-	100	
		V_{DD} = 1.8 to 5.5V	-	-	160	
SIN input setup time	t_{SS}	V_{DD} = 2.4 to 5.5V	120	-	-	
		V_{DD} = 1.8 to 5.5V	180	-	-	
SIN input hold time	t_{SH}	V_{DD} = 2.4 to 5.5V	80	-	-	
		V_{DD} = 1.8 to 5.5V	100	-	-	

*1: Clock cycle selected by bit12~8(SnCK4~0) of the serial port n mode register (SIOnMOD)
V_{DD} ≥ 2.4V: min. 250ns, V_{DD} ≥ 1.8V: min500ns



*: 2nd to 8th function of port, n=0~3

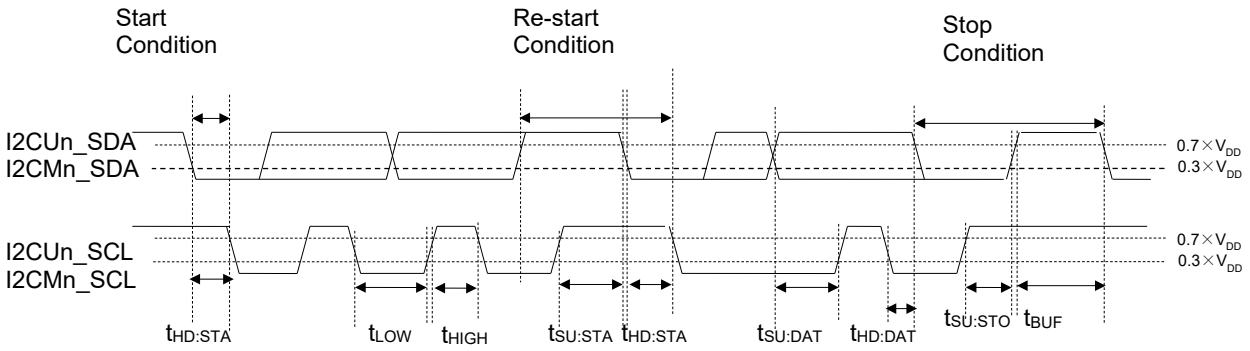
I²C Bus Interface

Standard Mode 100kbps

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	0	-	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	-	4.0	-	-	μs
SCL "L" level time	t_{LOW}	-	4.7	-	-	
SCL "H" level time	t_{HIGH}	-	4.0	-	-	
SCL setup time (restart condition)	$t_{SU:STA}$	-	4.7	-	-	
SDA hold time	$t_{HD:DAT}$	-	0	-	-	
SDA setup time	$t_{SU:DAT}$	-	0.25	-	-	
SDA setup time (stop condition)	$t_{SU:STO}$	-	4.0	-	-	
Bus-free time	t_{BUF}	-	4.7	-	-	

When using the I²C as the master, configure the I²C master n mode register (I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



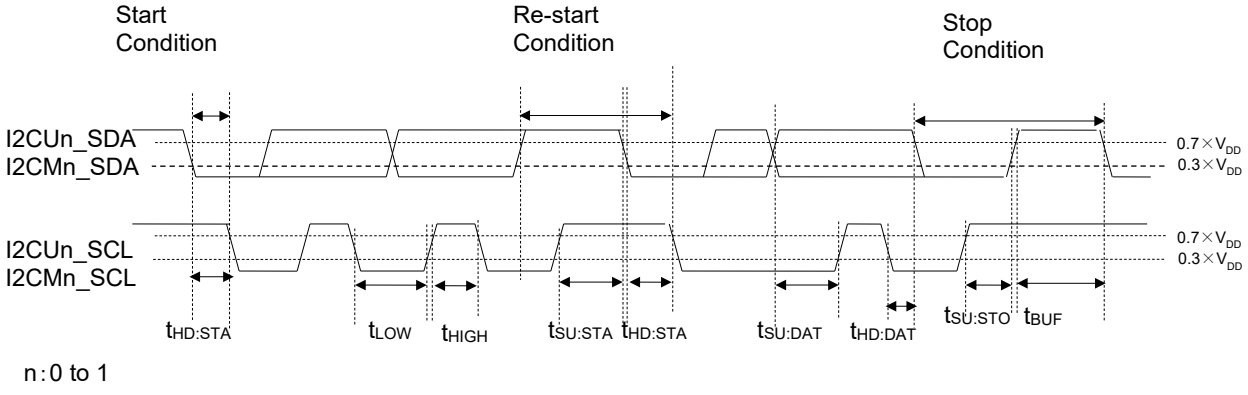
n : 0 to 1

Fast Mode 400kbps

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	0	-	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	-	0.6	-	-	µs
SCL "L" level time	t_{LOW}	-	1.3	-	-	
SCL "H" level time	t_{HIGH}	-	0.6	-	-	
SCL setup time (restart condition)	$t_{SU:STA}$	-	0.6	-	-	
SDA hold time	$t_{HD:DAT}$	-	0	-	-	
SDA setup time	$t_{SU:DAT}$	-	0.1	-	-	
SDA setup time (stop condition)	$t_{SU:STO}$	-	0.6	-	-	
Bus-free time	t_{BUF}	-	1.3	-	-	

When using the I²C as the master, configure the I²C master n mode register (I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



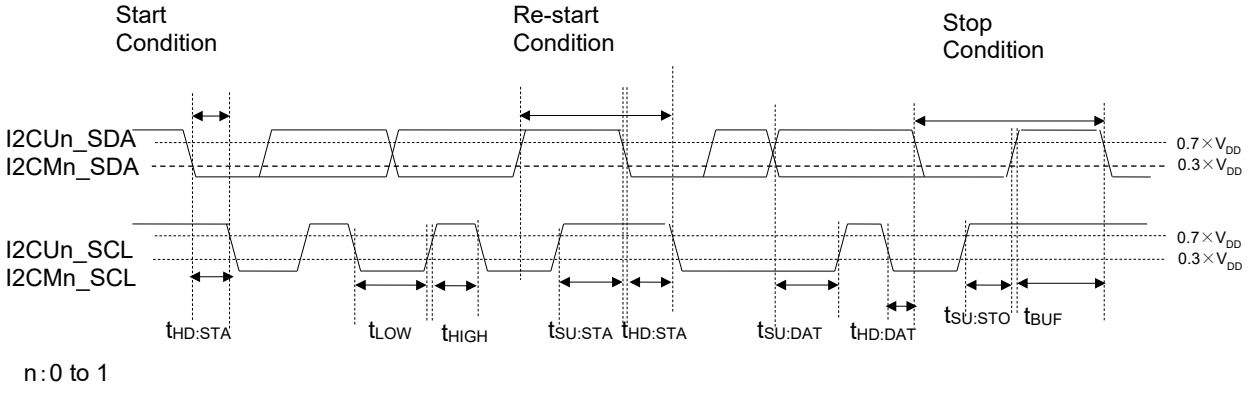
n : 0 to 1

1Mbps Mode

(V_{DD} = 2.7 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	0	-	1000	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	-	0.26	-	-	µs
SCL "L" level time	t_{LOW}	-	0.5	-	-	
SCL "H" level time	t_{HIGH}	-	0.26	-	-	
SCL setup time (restart condition)	$t_{SU:STA}$	-	0.26	-	-	
SDA hold time	$t_{HD:DAT}$	-	0	-	-	
SDA setup time	$t_{SU:DAT}$	-	0.1	-	-	
SDA setup time (stop condition)	$t_{SU:STO}$	-	0.26	-	-	
Bus-free time	t_{BUF}	-	0.5	-	-	

When using the I²C as the master, configure the I²C master n mode register (I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



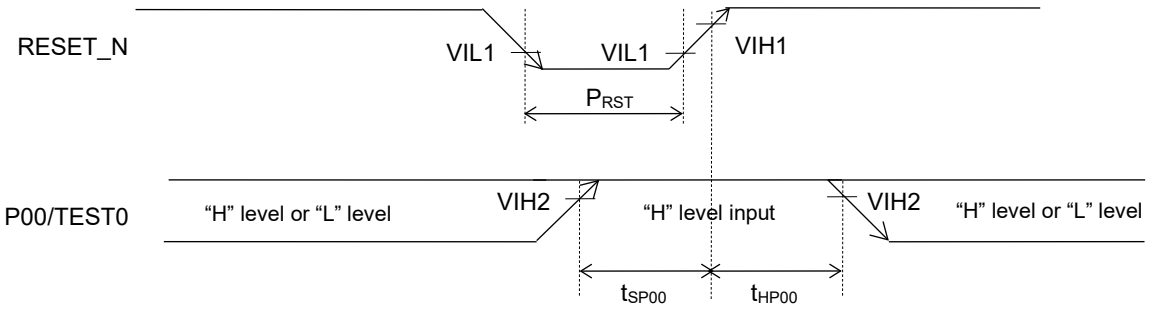
n : 0 to 1

Reset

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Reset pulse width*2	P_{RST}	-	2	-	-	ms	1
P00 "H" level setup time*1	t_{SP00}	-	1	-	-		
P00 "H" level hold time*1	t_{HP00}	-	1	-	-		

*1: The specification is for except the ISP mode. See Chapter 25.4 "In-System Programing Function" in the User's Manual for the timing in ISP mode.
*2: It means the time after the voltage of V_{DD} reached to 1.6V or higher in the case of power on.



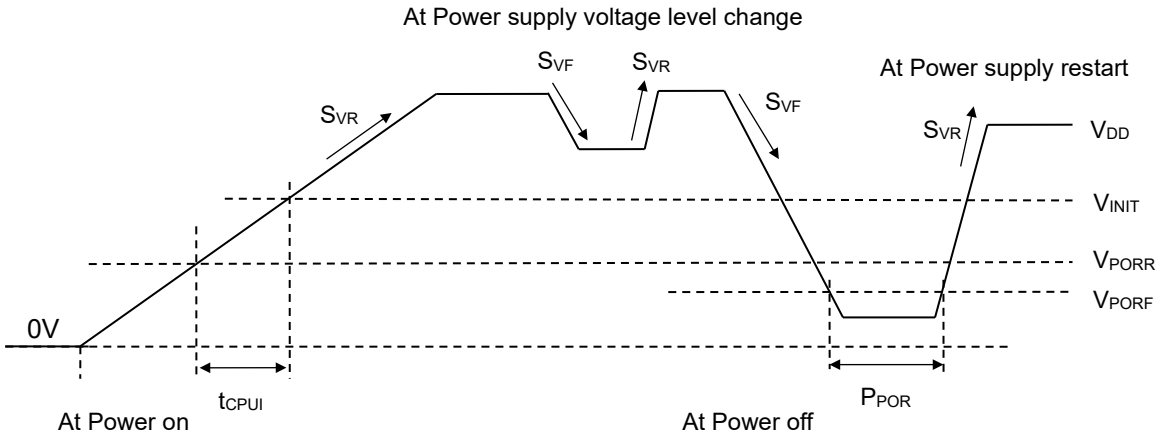
[Note]

- **Do not drive a pulse into the RESET_N pin that has the pulse width shorter than the Reset pulse width (P_{RST}), otherwise unexpected operation may possibly happen.**

Slope of Power supply and Power on Reset

(V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Power on rising slope	S_{VR}	-	-	-	60	V/ms	1
Power on falling slope	S_{VF}	-	-	-	2		
Power on reset detection voltage	V_{PORR}	Power up (rising)	1.47	1.57	1.80	V	
	V_{PORF}	Power down (falling)	1.33	1.49	1.58		
Power on reset minimum pulse width	P_{POR}	-	200	-	-	µs	
Power on voltage	V_{INIT}	At power on	1.8	-	-	V	
CPU operation start time (from the release of reset to the CPU starts to run)	t_{CPUI}	-	11	16	-	ms	



[Note]

- **If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD}, it may cause the MCU malfunction.**
  Apply prevent measurement such as bypass capacitors or external reset input, and so on.
- **Start the high-speed clock when the V_{DD} is within the operating voltage.**

VLS

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition VLS0LV *1		Min.	Typ.	Max.	Unit	Measuring circuit
VLS threshold voltage *2	V_{VLSR}	00H	Rising	3.86	4.06	4.26	V	1
	V_{VLSF}		Falling	3.84	4.00	4.16		
	V_{VLSR}	01H	Rising	3.57	3.76	3.95		
	V_{VLSF}		Falling	3.55	3.70	3.85		
	V_{VLSR}	02H	Rising	2.94	3.11	3.28		
	V_{VLSF}		Falling	2.92	3.05	3.18		
	V_{VLSR}	03H	Rising	2.85	3.01	3.17		
	V_{VLSF}		Falling	2.83	2.95	3.07		
	V_{VLSR}	04H	Rising	2.75	2.91	3.07		
	V_{VLSF}		Falling	2.73	2.85	2.97		
	V_{VLSR}	05H	Rising	2.66	2.81	2.96		
	V_{VLSF}		Falling	2.64	2.75	2.86		
	V_{VLSR}	06H	Rising	2.56	2.71	2.86		
	V_{VLSF}		Falling	2.54	2.65	2.76		
	V_{VLSR}	07H	Rising	2.46	2.61	2.76		
	V_{VLSF}		Falling	2.44	2.55	2.66		
	V_{VLSR}	08H	Rising	2.37	2.51	2.65		
	V_{VLSF}		Falling	2.35	2.45	2.55		
	V_{VLSR}	09H	Rising	1.98	2.11	2.24		
	V_{VLSF}		Falling	1.96	2.05	2.14		
	V_{VLSR}	0AH	Rising	1.89	2.01	2.13		
	V_{VLSF}		Falling	1.87	1.95	2.03		
	V_{VLSR}	0BH	Rising	1.79	1.91	2.03		
	V_{VLSF}		Falling	1.77	1.85	1.93		
VLS Current	I_{VLS}	-		-	50	-	nA	

*1 Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).
*2 The Data VSL0LV = 0CH~0FH is not available to use, if the data is specified it will the same spec as that 0BH is specified.

Analog Comparator

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Comparator same phase input voltage range	V_{CMR}	-	0.1	-	V_{DD} -1.5	V	1
Comparator0 input offset	V_{CMOF}	Ta = +25°C、V_{DD} = 5.0V	-	5	-	mV	
Comparator Reference Voltage	V_{CMREF}	-	0.75	0.8	0.85	V	

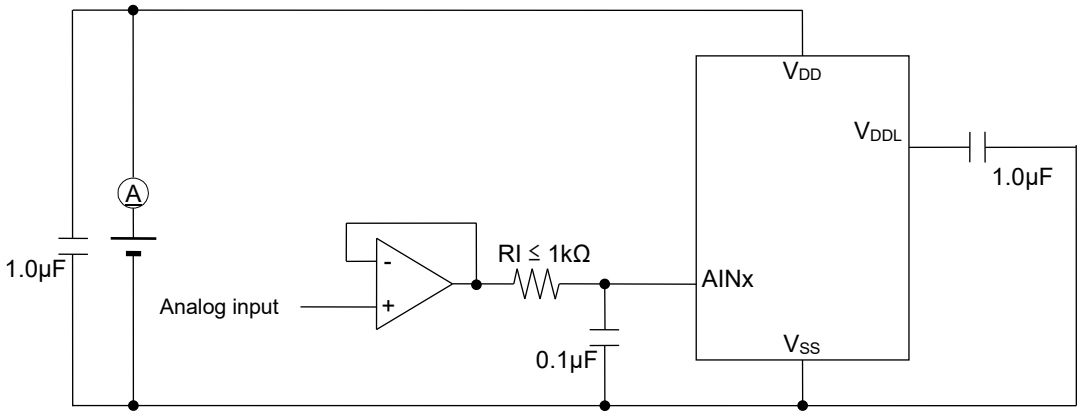
Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n_{AD}	-	-	-	10	bit
Overall error	-	4.5V ≤ V_{REFP} *1 ≤ 5.5V	-3.5	1.2	3.5	LSB
Integral non-linearity error	INL_{AD}	2.7V ≤ V_{REFP} *1 ≤ 5.5V	-4	-	4	
		2.2V ≤ V_{REFP} *1 < 2.7V	-6	-	6	
		1.8V ≤ V_{REFP} *1 < 2.2V	-10	-	10	
		V_{REFP} = Internal reference voltage	-15	-	15	
Differential non-linearity error	DNL_{AD}	2.7V ≤ V_{REFP} *1 ≤ 5.5V	-3	-	3	
		2.2V ≤ V_{REFP} *1 < 2.7V	-5	-	5	
		1.8V ≤ V_{REFP} *1 < 2.2V	-9	-	9	
		V_{REFP} = Internal reference voltage	-14	-	14	
Zero-scale error	ZSE	RI ≤ 1kΩ	-6	-	6	
Full-scale error	FSE	RI ≤ 1kΩ	-6	-	6	
A/D reference voltage	V_{REF}	-	1.8	-	V_{DD}	V
Internal reference voltage	V_{REFI}	-	1.5	1.55	1.6	
Conversion time	t_{CONV}	4.5V ≤ V_{DD} ≤ 5.5V	2.25	-	427	µs
		2.2V ≤ V_{DD} ≤ 5.5V	4.5	-	427	
		1.8V ≤ V_{DD} ≤ 5.5V	18	-	427	

*1 : V_{DD} or P23/V_{REF} is selected for the reference voltage of Successive Approximation Type A/D Converter.

The current flows during the ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1µF capacitor on the ADC input pin is recommended to reduce the noise.



D/A Converter

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n_{DA}	-	-	-	8	bit
Conversion cycle	tc	-	10	-	-	μs
Integral non-linearity error	INL_{DA}	RL = 4MΩ	-2	-	2	LSB
Differential non-linearity error	DNL_{DA}	RL = 4MΩ	-1	-	1	
Output impedance	Ro	DACEN bit of D/A converter enable register =1	3	6	9	kΩ

Reference Voltage Output

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REFO}	-	-	1.55	-	V
Output impedance	R_{VREFO}	-	-	-	500	kΩ

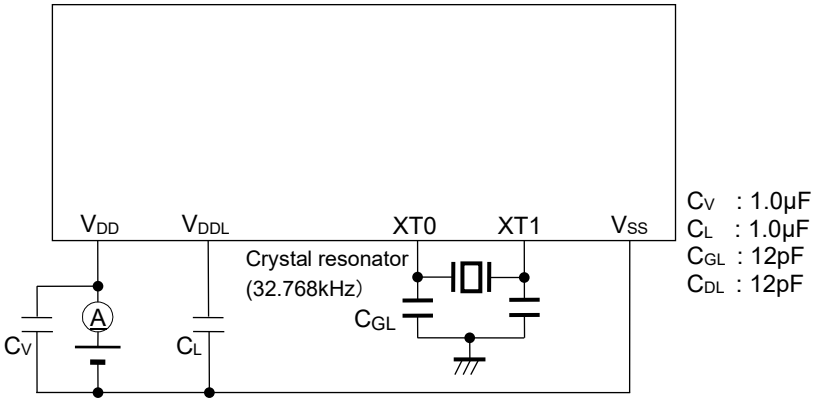
Flash Memory

(V_{SS}= 0V)

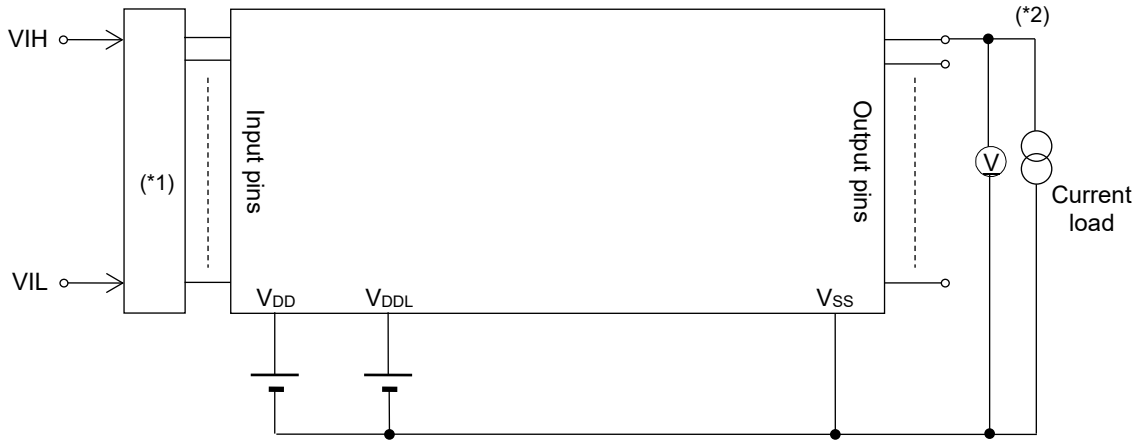
Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		+1.8 to +5.5	V
Maximum rewrite count	CEPD	Data Flash		10000	times
	CEPP	Program Flash		100	
Erase unit	-	Block erase	Program Flash	16K	B
			Data Flash	all area	
	-	Sector erase	Program Flash	1K	B
			Data Flash	128	
Erase time (Max.)	-	Block erase / Sector erase		50	ms
Write unit	-	Program Flash		4	B
		Data Flash		1	
Write time (Max.)	-	Program Flash		80	μs
	-	Data Flash		40	
Data retention period	YDR	-		15	years

Measuring circuit

Measuring circuit 1

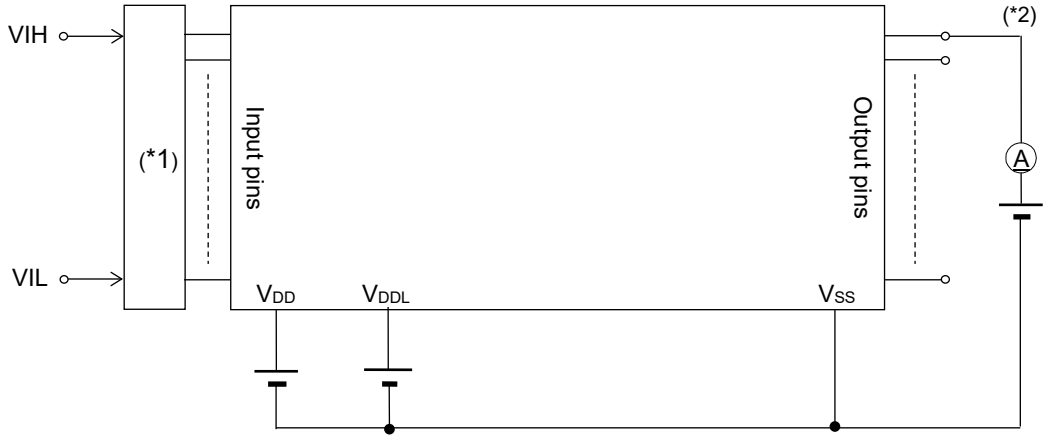


Measuring circuit 2



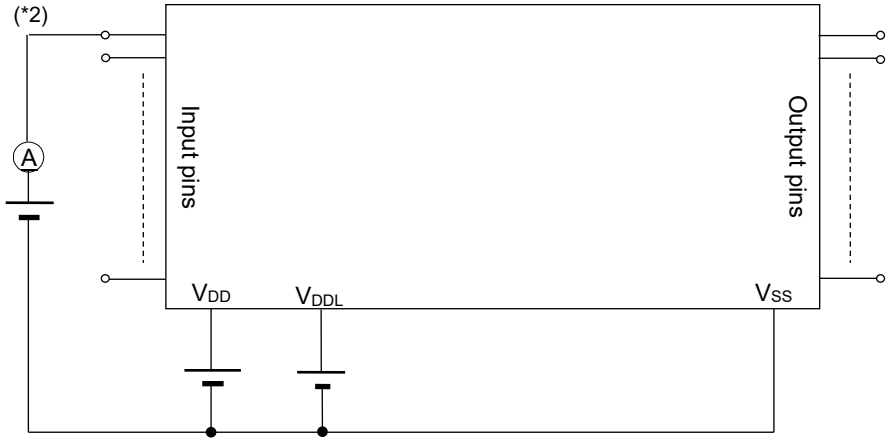
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 3



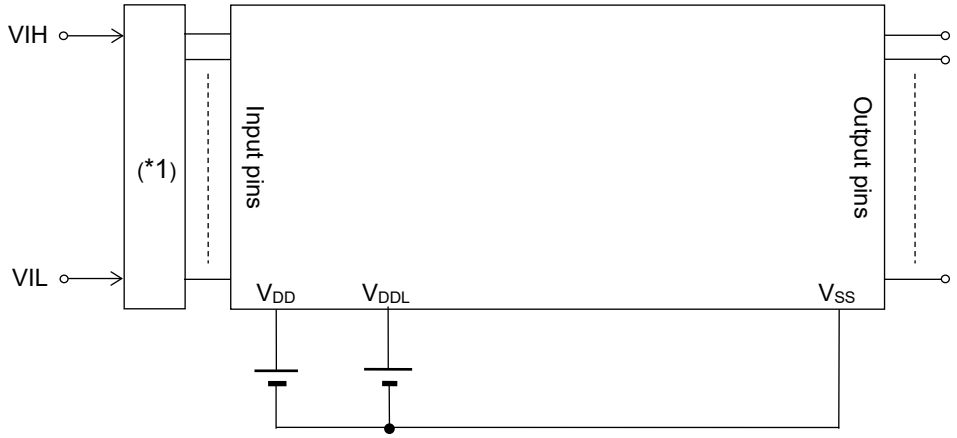
(*1) Input logic circuit to determine the specified measuring conditions
(*2) Measured connecting specified pins

Measuring circuit 4



(*2) Measured connecting specified pins

Measuring circuit 5

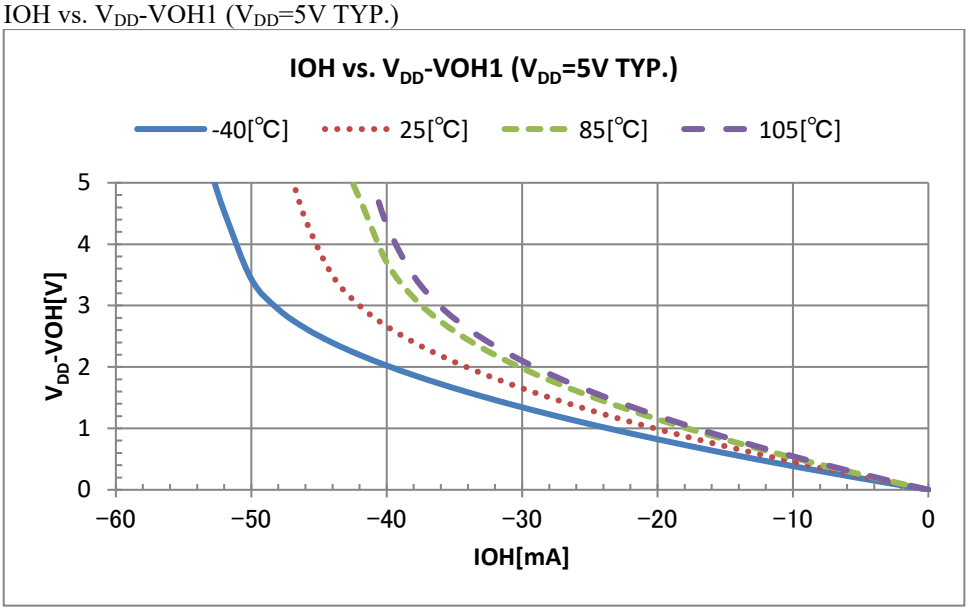


(*1) Input logic circuit to determine the specified measuring conditions

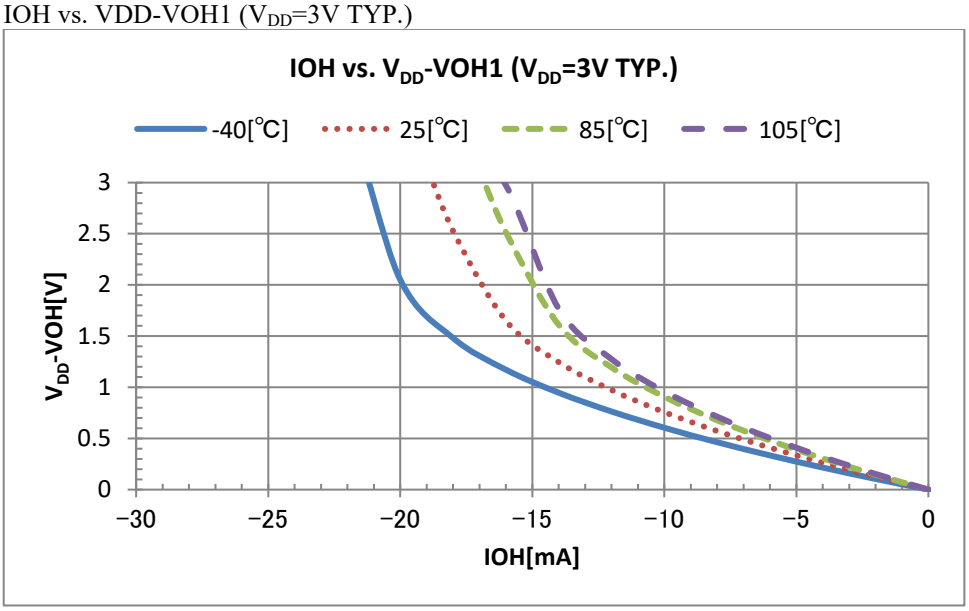
Characteristics graphs

These Graphs on the following pages are references for designing an application.

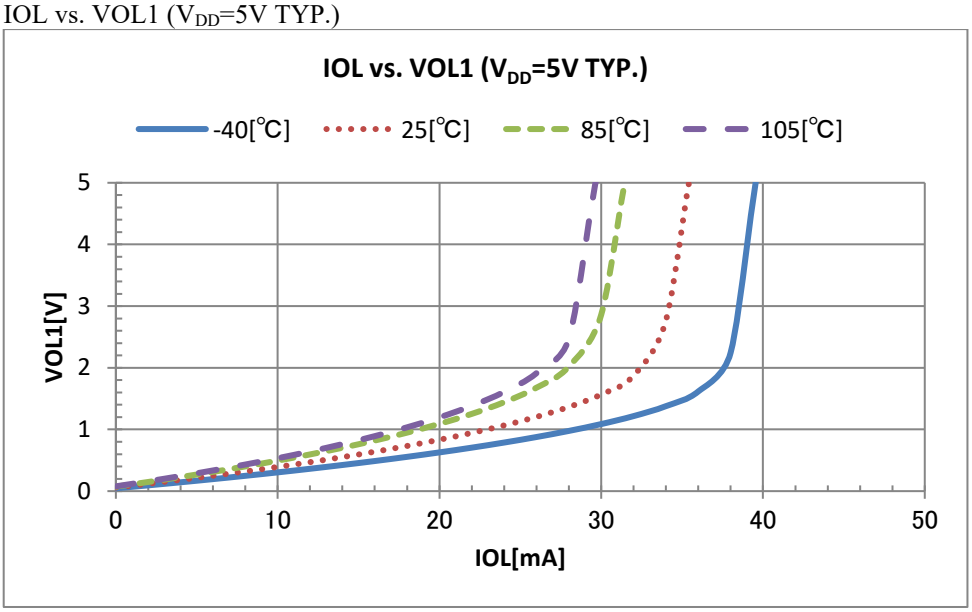
IOH vs. V_{DD}-VOH1 (V_{DD}=5V TYP.)



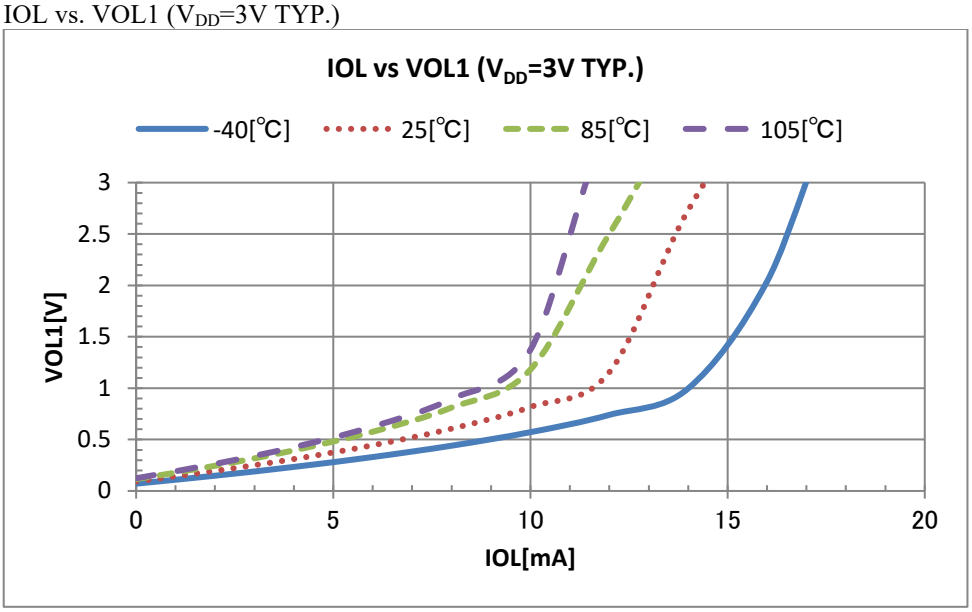
IOH vs. VDD-VOH1 (V_{DD}=3V TYP.)



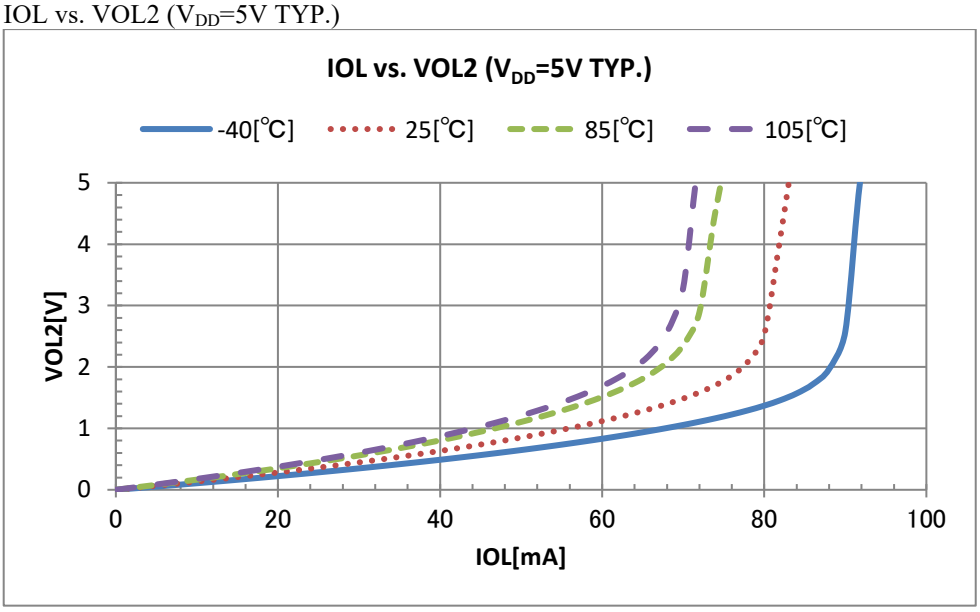
IOL vs. VOL1 (V_{DD}=5V TYP.)



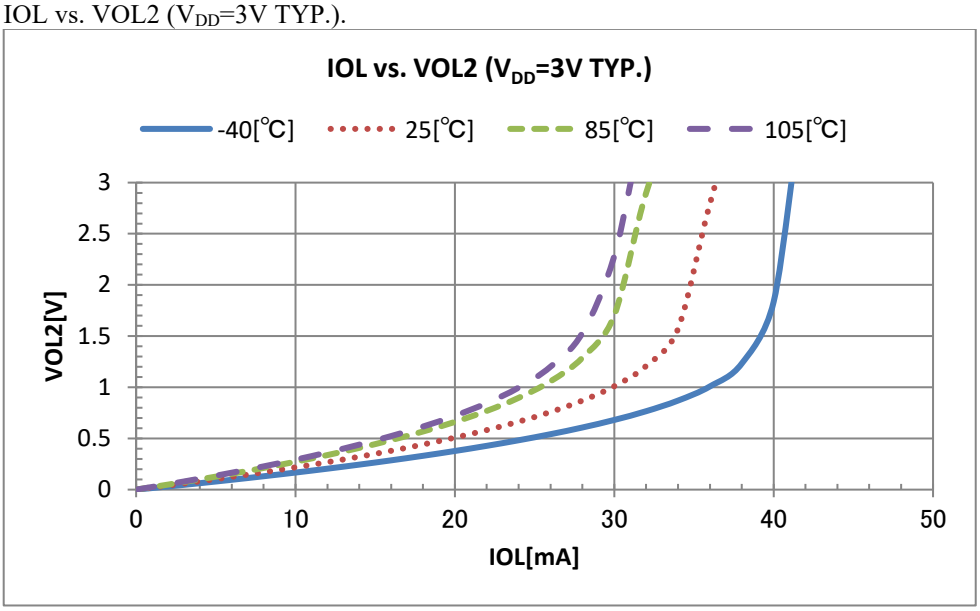
IOL vs. VOL1 (V_{DD}=3V TYP.)



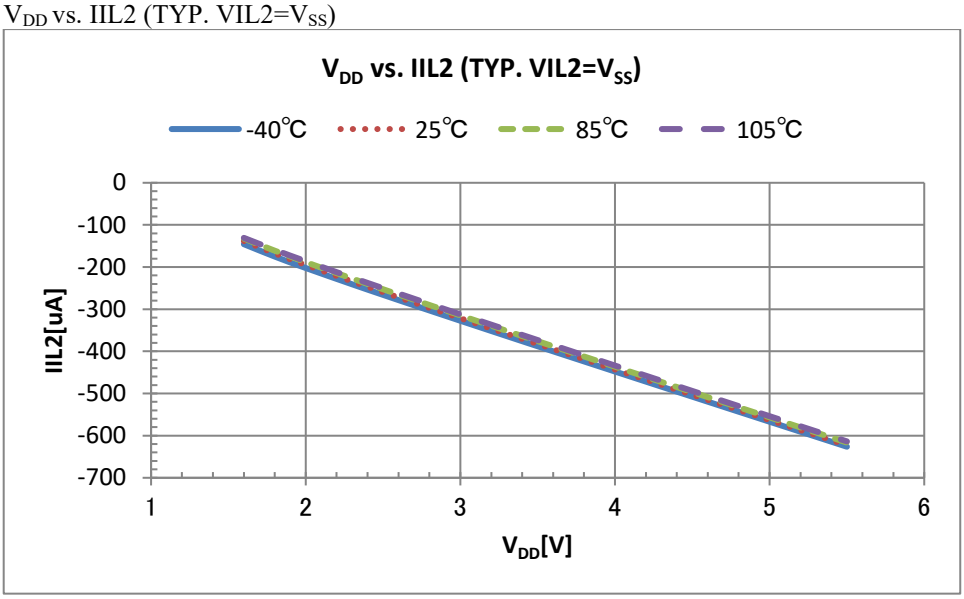
IOL vs. VOL2 (V_{DD}=5V TYP.)



IOL vs. VOL2 (V_{DD}=3V TYP.).

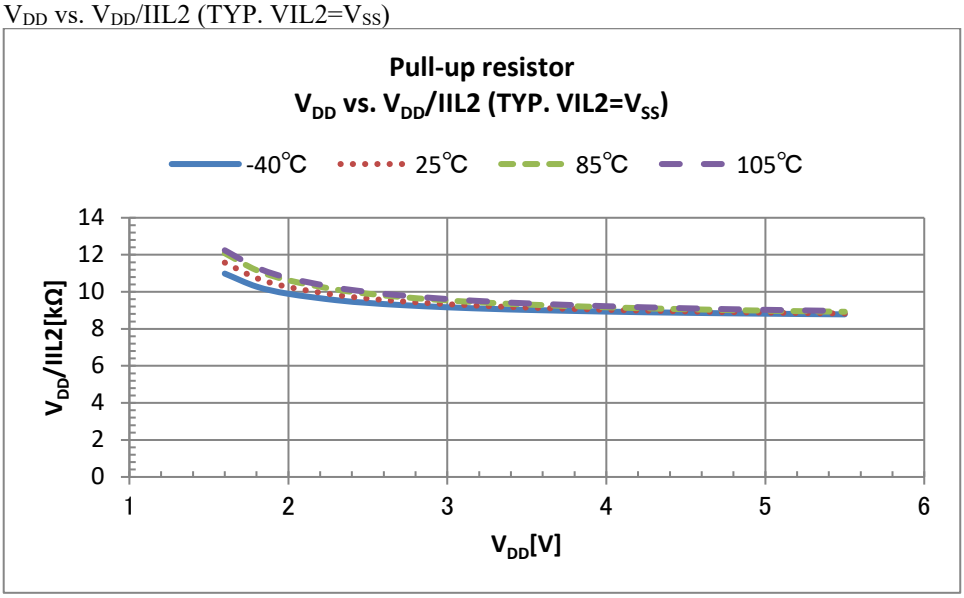


V_{DD} vs. IIL2 (TYP. VIL2=V_{SS})

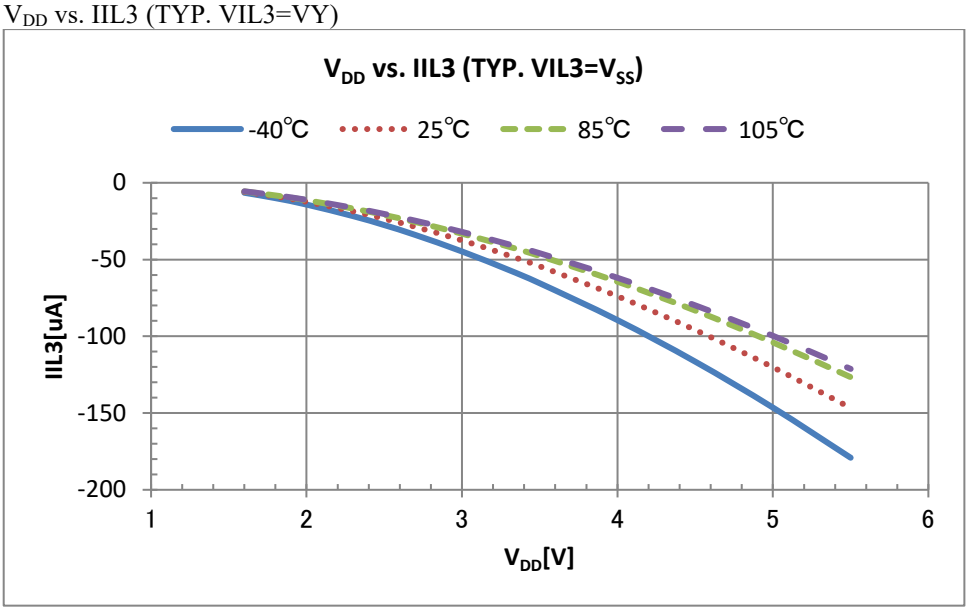


Pull-up resistor

V_{DD} vs. V_{DD}/IIL2 (TYP. VIL2=V_{SS})

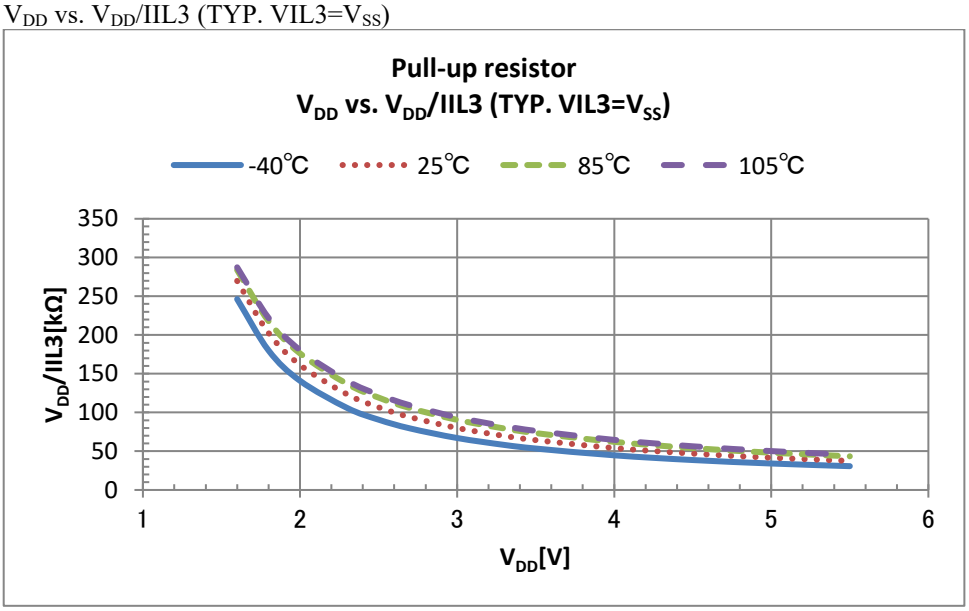


V_{DD} vs. IIL3 (TYP. VIL3=VY)

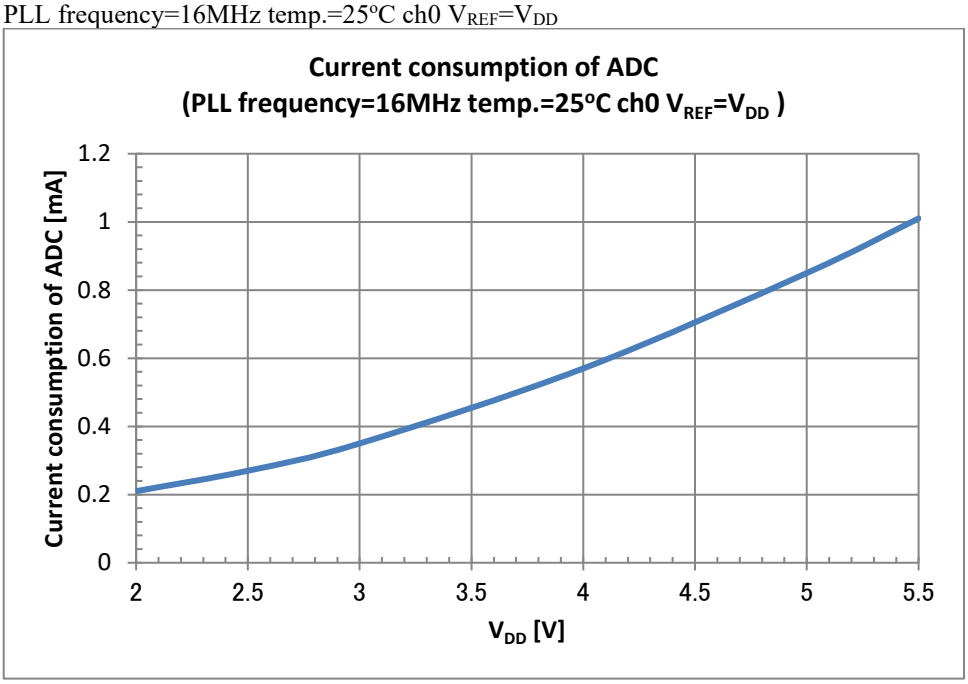


Pull-up resistor

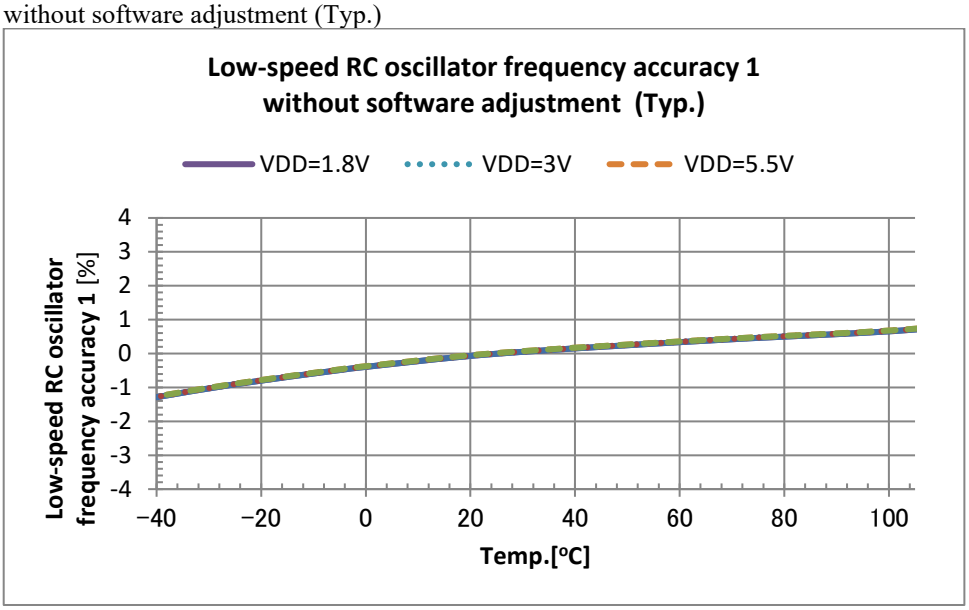
V_{DD} vs. V_{DD}/IIL3 (TYP. VIL3=V_{SS})



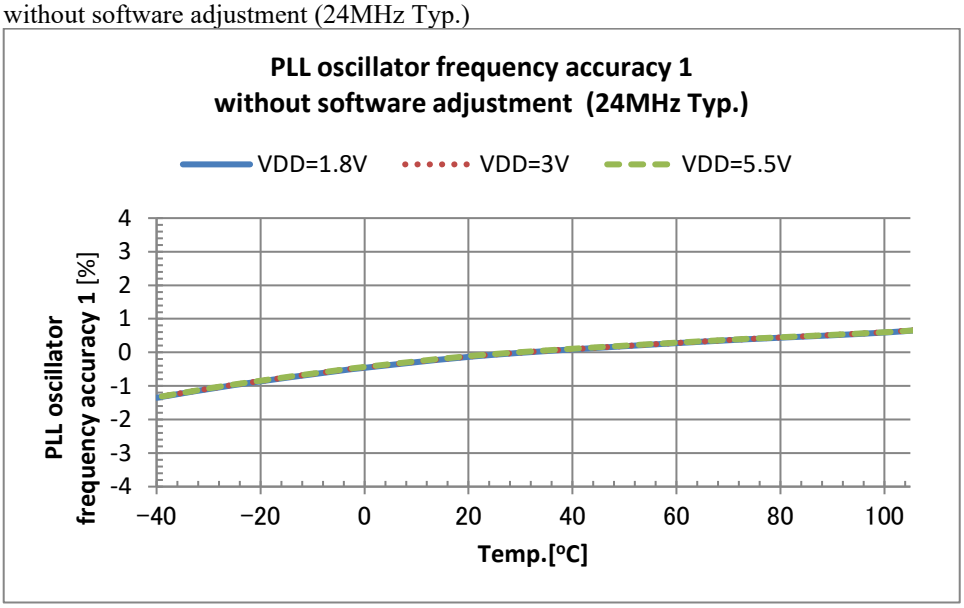
Current consumption of ADC vs. operating voltage
PLL frequency=16MHz temp.=25ºC ch0 $V_{REF}=V_{DD}$



TEMP vs. Low-speed RC oscillator frequency accuracy 1
without software adjustment (Typ.)

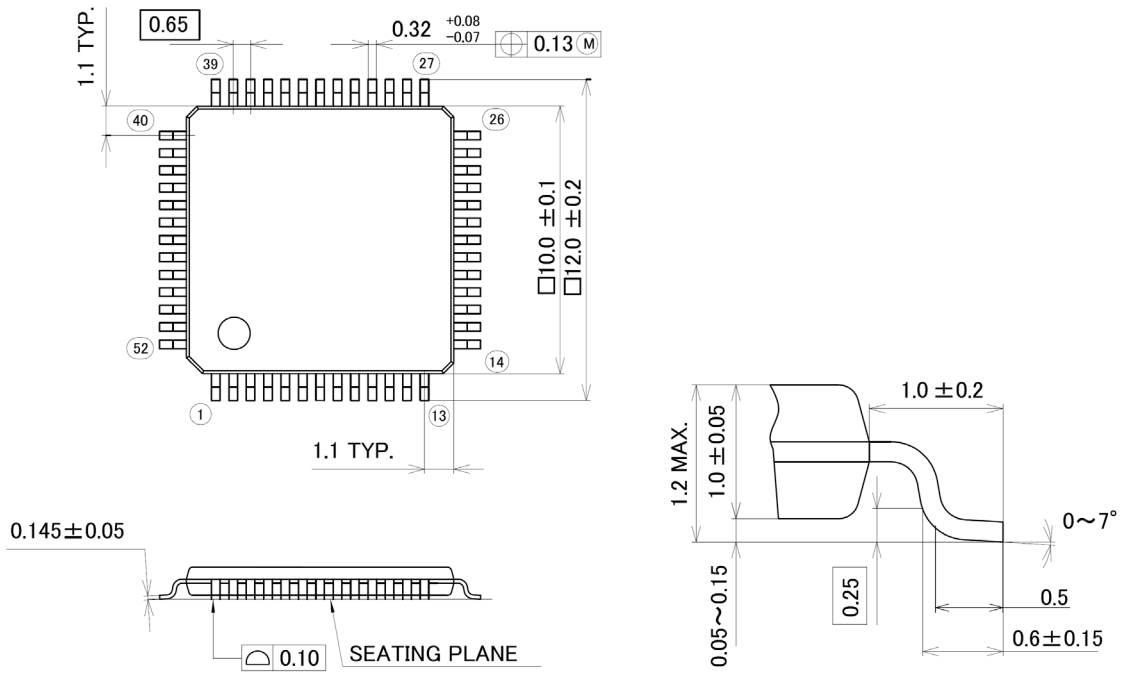


TEMP vs. PLL oscillator frequency accuracy 1
without software adjustment (24MHz Typ.)



PACKAGE DIMENSIONS

52pin TQFP Package



注記
1.リード幅にはダムバーカット残りを含まない。
2.パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
又モールドの上下のズレは含まない。
3.SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION,DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

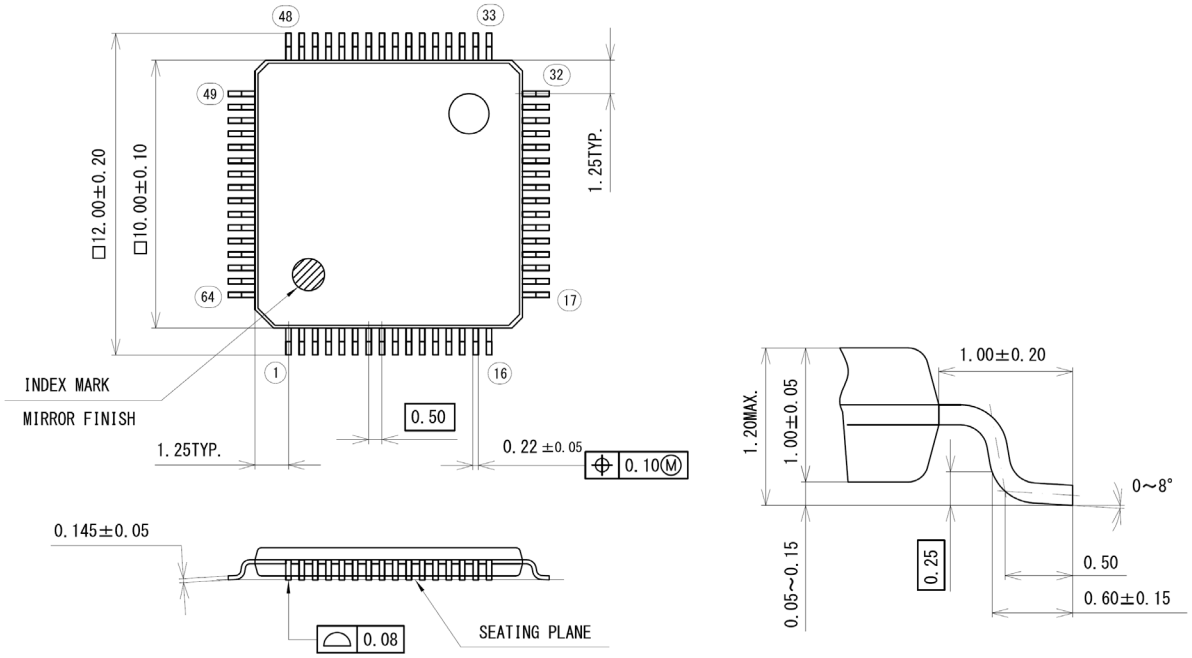
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP52-1010-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69380
LEAD FINISH	Sn	REVISION	2
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	Dec/21/2016
PACKAGE MASS (g)	0.28TYP.	REVISED	Dec/22/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin TQFP Package



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

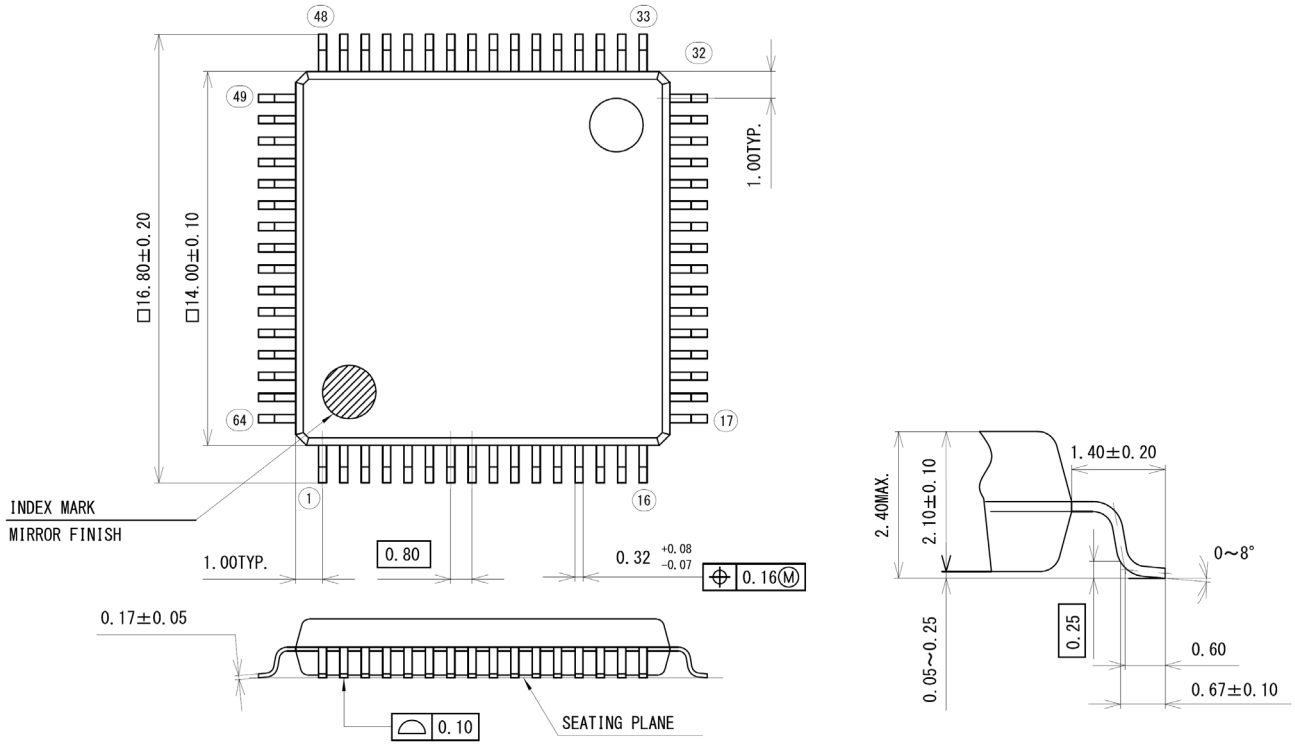
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP64-1010-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69144
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.26TYP.	REVISED	Oct/26/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin QFP Package



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

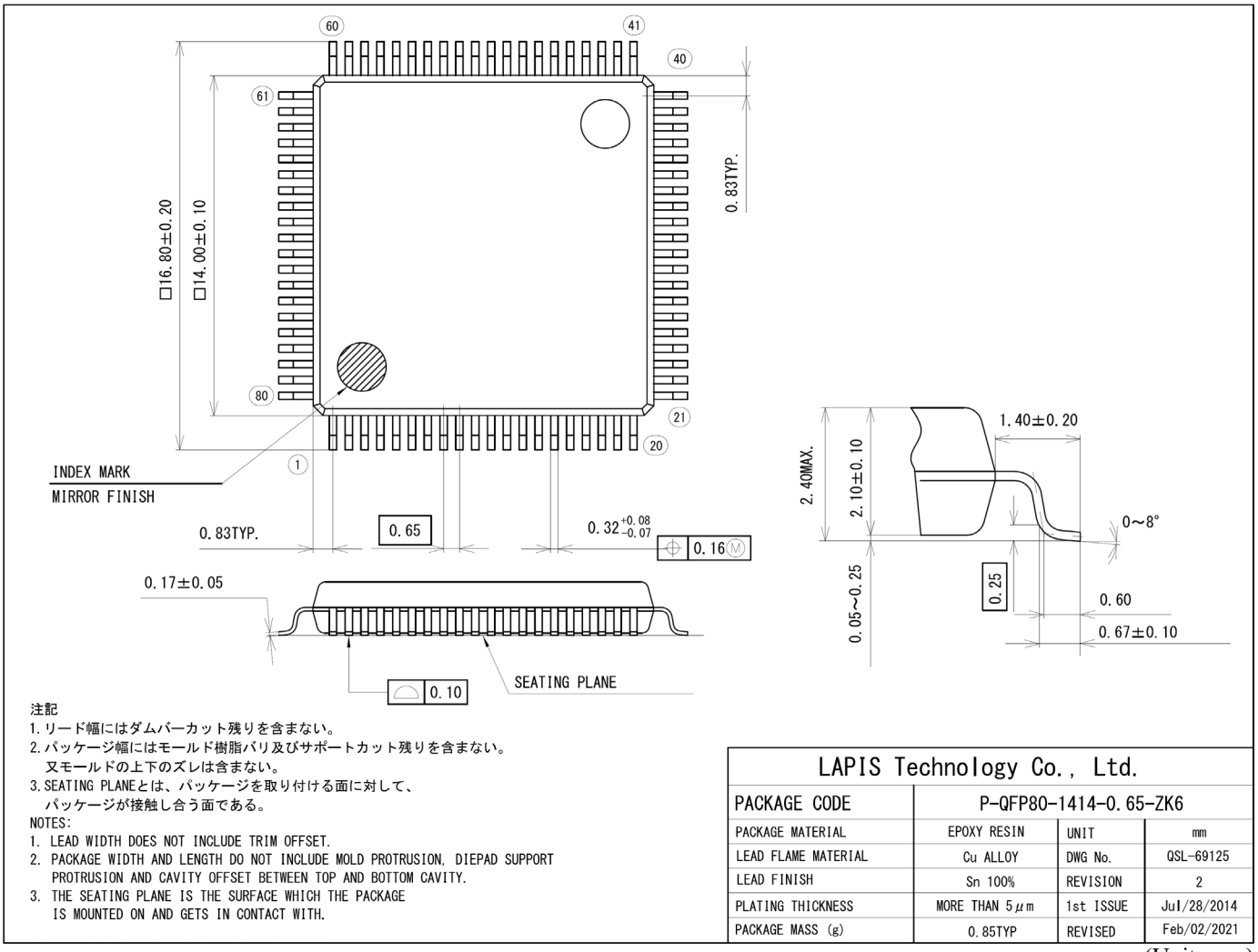
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-QFP64-1414-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69124
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.87TYP.	REVISED	Dec/14/2020

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

80pin QFP Package



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-QFP80-1414-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69125
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.85TYP	REVISED	Feb/02/2021

(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL62Q1500C-01	Nov 15, 2019	-	-	1st Revision.
FEDL62Q1500C-02	Jul 28, 2020	4, 8	4, 8	Changed comment for UART.
		21	21	Changed note for Termination of unused pins.
		22	22	Added parameter “Operating temperature (Chip-Junction)” in Recommended Operating Conditions
		23	-	Removed the section “Operation Confirmed Crystal Unit(32.768kHz)”. This section is mentioned in Applications Note; “Operation-confirmed oscillator for ML62Q1000 series”.
		-	23	Added thermal characteristics section
		37	37	Changed note for Slope of Power supply and Power on Reset.
		*	*	Corrected typo
FEDL62Q1500C-03	May 19, 2022	*	*	Corrected Typo
		-	56	Added Notes for product usage
FEDL62Q1500C-04	Aug 21, 2023	21	21	Added comment in Table 5
		51-54	51-54	Revised Package dimension
FEDL62Q1500C-04	Mar 26, 2024	1	1	Added application information
		7	7	Changed the format of the shipping package information
		8	8	Updated “how to read the part number”
		57	57	Revised the Note

Notes for product usage

Notes on this page are applicable to the all microcontroller products.
For individual notes on each LAPIS Technology microcontroller product, refer to [Note] in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS
   Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON
   At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
   On LAPIS Technology microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
   Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY
   If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCTS
   Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
   When replacing from other product to LAPIS Technology microcontroller products, please evaluate enough the apparatus/system which implemented LAPIS Technology microcontroller products.

5. USE ENVIRONMENT
   When using this product in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

Notes

1) When using LAPIS Technology Products, refer to the latest product information and ensure that usage conditions (absolute maximum ratings*1, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures.
*1: Absolute maximum ratings: a limit value that must not be exceeded even momentarily.

2) The Products specified in this document are not designed to be radiation tolerant.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

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