



Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAMIS Technology Co., Ltd.

Therefore, all references to "LAMIS Technology Co., Ltd.", "LAMIS Technology"
and/or "LAMIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML62Q1300 Group

GENERAL DESCRIPTION

ML62Q1300 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory (Flash memory), data memory (RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC generator, DMA controller, Clock generator, Timer, General Purpose Ports, UART, Synchronous serial port, I²C bus interface unit (Master, Slave), Buzzer, Voltage Level Supervisor (VLS), Successive approximation type A/D converter, D/A converter , Analog comparator, Safety function (IEC60730/60335 Class B) and so on. The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing. The built-in on-chip debug function enables debugging and programming the software. Also, ISP (In-System Programming) function supports the Flash programming in production line.

- Applications

Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

Note:

This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems. Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

- Product list

The ML62Q1300 Group has six packages (16pin - 32pin) and five kinds of memory sizes (16Kbyte - 64Kbyte).

Table 1 ML62Q1300 Group Product List

Program memory	Data memory (RAM)	Data Flash	16pin SSOP16 WQFN16	20pin TSSOP20	24pin WQFN24	32pin TQFP32 WQFN32
64Kbyte	4Kbyte	2Kbyte	-	-	ML62Q1347	ML62Q1367
48Kbyte			-	-	ML62Q1346	ML62Q1366
32Kbyte			-	-	ML62Q1345	ML62Q1365
32Kbyte	2Kbyte	ML62Q1325	ML62Q1335	-	-	-
24Kbyte		ML62Q1324	ML62Q1334	-	-	-
16Kbyte		ML62Q1323	ML62Q1333	-	-	-

Please see the last 2 pages “Notes for product usage” and “Notes” in this document on use with this ML62Q1300 group.

FEATURES

- CPU
 - 16-bit RISC CPU: nX-U16/100 (A35 core)
 - Instruction system: 16-bit length instructions
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - Built-in On-chip debug function
 - Built-in ISP (In-System Programming) function
 - Minimum instruction execution time
 - Approximately 30.5μs (at 32.768kHz system clock)
 - Approximately 62.5ns/41.6ns (at 16MHz/24MHz system clock)
- Coprocessor for multiplication and division
 - Multiplication : 16bit × 16bit (operation time: 4cycles)
 - Division : 32bit ÷ 16bit (operation time: 8cycles)
 - Division : 32bit ÷ 32bit (operation time: 16cycles)
 - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time: 4cycles)
 - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time: 4cycles)
 - Signed or Unsigned is selectable
- Operating voltage and temperature
 - Operating voltage: V_{DD} = 1.6 to 5.5V (V_{DD} should be 1.8V or over at Power-on)
 - Operating temperature: -40°C to +105°C
- Internal memory
 - Program memory area
 - Rewrite count: 100 cycles
 - Write unit: 32bit (4byte)
 - Erase unit: 16Kbyte/1Kbyte
 - Erase/Write temperature: 0°C to +40°C
 - Data Flash memory area
 - Rewrite count: 10,000cycles
 - Write unit: 8bit (1byte)
 - Erase unit: all area/128byte
 - Erase/Write temperature: -40°C to +85°C
 - Back Ground Operation (CPU can work while erasing and rewriting)
- This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.
SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.
- Data RAM area
 - Rewrite unit: 8bit/16bit (1byte/2byte)
 - Parity check function is available (interrupt / reset are generatable at Parity error)
- Clock
 - Low-speed clock (LSCLK)
Internal low-speed RC oscillation: Approximately 32.768kHz
 - High-speed clock (HSCLK)
PLL oscillation: 2 selectable oscillation frequency (24MHz and 16MHz) by code option
 - Watch Dog Timer (WDT): built-in independent clock for WDT (RC1K: Approximately 1kHz)
- Reset
 - Reset by reset input pin
 - Reset by Power-On Reset
 - Reset by WDT overflow
 - Reset by WDT invalid clear
 - Reset by RAM parity error
 - Reset by unused ROM area access (instruction access)
 - Reset by voltage level supervisor (VLS)
 - Software reset by BRK instruction (reset CPU only)
 - Reset the peripherals individually

- Collective reset to the all control pins and peripheral circuits
- Power management
 - HALT mode: CPU stops executing instruction, peripheral circuits continue working
 - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits continue working with low-speed clock
 - STOP mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop.
 - STOP-D mode: CPU and peripheral circuits stops executing instruction, both high-speed oscillation and low-speed oscillation stop. The internal logic voltage (V_{DDL}) goes down to reduce the current consumption (RAM data is retained).
 - Clock gear: High-speed system clock frequency can be changed (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of HSCLK)
 - Block Control Function: Powers down the unused function blocks (reset the block or stop supplying the clock)
- Interrupt controller
 - External interrupt ports: max. 8
 - Non-maskable interrupt source: 1 (Internal sources: WDT)
 - Maskable interrupt sources: max. 32
 - Four step interrupt levels
- Watchdog timer (WDT)
 - Selectable Operating clock: select RC1K or LSCLK by code option
 - Overflow period: 8selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2s and 8s)
 - Selectable window function (enable or disable): configurable clear enable period (50% or 75% of overflow period)
 - Selectable WDT operation: select Enable or Disable by code option
 - Readable WDT counter: WDT counter monitor function
- DMA (Direct Memory Access) controller
 - Channel: 2channel
 - Transfer unit: 8bit/16bit
 - Transfer count: 1 to 1024
 - Transfer cycle: 2 cycle transfer
 - Transfer address: Fixed addressing mode, inclement addressing mode, and decrement addressing mode
 - Transfer target: Special Function Register (SFR)/RAM → SFR/RAM (Transfer from/to Flash is not supported)
 - Transfer request: External pins, Serial communication unit, Successive approximation type A/D converter, 16bit timer, and Functional timer
- Low-speed Time base counter
 - Generate 8 frequency (128Hz to1Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
 - Selectable 3 interrupts from eight frequency internal pulse signals
 - 1Hz or 2Hz output from general purpose port
- Functional timer
 - Channel: 4 channels
 - Built-in timer, capture, and PWM function by 16bit counter
 - Built-in Repeat mode, One shot mode is available
 - Two types of PWM output with the same period and different duties, and complementary PWM output with the dead time
 - Monitor input signal duty and the period by capture function
 - Generate periodical interrupts, duty interrupts, and interrupts coincided with set value
 - Counter Start, Stop, Counter clear triggered by an external inputs or Timer
 - Generate Emergency stop and emergency stop interrupt triggered by an external input
 - Same start/stop among different channels of the functional timer
 - Selectable counter clock (external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channel
- 16-bit General timers
 - Channel: Max. 6channel
 - 8 bits timer mode and 16-bit timer mode

- Same start/stop among different channels of 16bit (8bit) timer
 - Timer output (toggled by overflow)
 - Selectable counter clock (external clock or divided by 1 to 128 of LSCLK or HSCLK) for each channel
- Serial communication unit
 - Synchronous Serial Port (SSIO) mode or UART mode is selectable
 - Channel: 2channel
- < Synchronous Serial Port >
- Selectable from Master and Slave
 - Selectable from LSB first or MSB first
 - Selectable 8bit length or 16bit length
- < UART mode>
- Full-duplex communication mode and half-duplex communication mode
 - 5 to 8bit length, parity or no parity, odd parity or even parity, 1stop bit or 2stop bits
 - Selectable from Positive logic or Negative logic
 - Selectable from LSB first or MSB first
 - Configurable wide range communication speed
 - 32.768kHz operation clock: 1bps to 4,800bps
 - 24MHz operation clock: 600bps to 3Mbps
 - 16MHz operation clock: 300bps to 2Mbps
 - Built-in baud rate generator
- I²C bus unit (Master / Slave)
 - Selectable from Master mode or Slave mode
 - Channel: 1channel
- < Master function >
- Standard mode (100kbps), fast mode (400kbps) and 1Mbps mode(1Mbps)
 - Handshake (Clock synchronization)
 - 7bit address format (10bit address format is supported)
- < Slave function >
- Standard mode (100kbps), fast mode (400kbps) and 1Mbps mode(1Mbps)
 - Clock stretch function
 - 7bit address format
- I²C bus Master
 - Channel: 1channel
 - Standard mode (100kbps), fast mode (400kbps) and 1Mbps mode(1Mbit/s)
 - Handshake (Clock synchronization)
 - 7bit address format (10bit address format is supported)
- General-purpose ports (GPIO)
 - I/O port: Max. 28 (Including one pin for on-chip debug and pins for other shared functions)
 - External interrupt port: 8
 - LED driver port: Max. 27
 - Carrier frequency output function (used for IR communication)
- Successive approximation type A/D converter (SA-ADC)
 - Channel: Max.8channels
 - Resolution: 10bit
 - Conversion time: Min. 2.25μs /channel (When the conversion clock speed is 8MHz)
 - Reference voltages are selectable
 - (V_{DD} pin / Internal reference voltage (V_{REFI} = Approximately 1.55V) / External reference voltage (V_{REF} pin))
 - Selected channel repeat conversion
 - Dedicated result register for each channel
 - Interrupt determining by upper limit or lower limit threshold of conversion result

- Voltage level supervisor (VLS)
 - Accuracy: $\pm 4\%$
 - Threshold voltage: 12 selectable (from 1.85V to 4.00V)
 - Functional Voltage level detection reset (VLS reset)
 - Functional Voltage level detection interrupt (VLS0 interrupt)
- Analog comparator
 - Channel: 1channel
 - Selectable interrupt from the comparator output (rising edge or falling edge)
 - Selectable from sampling or without sampling
 - Comparable with external 2 inputs
 - Comparable with external input and internal reference voltage (0.8V)
- D/A converter
 - Channel: Max 1channel
 - Resolution: 8bit
 - Output impedance: 6k ohm (Typ.)
 - R-2R ladder type
- Buzzer
 - 4 buzzer mode (Continuous sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
 - 8 frequencies (4.096kHz to 293Hz)
 - 15 step duty (1/16 to 15/16)
 - Selectable from positive logic buzzer output or negative logic buzzer output
- CRC (Cyclic Redundancy Check) generator
 - Generation equation: $X^{16}+X^{12}+X^5+1$
 - Selectable from LSB first or MSB first
 - Built-in Automatic program memory CRC calculation mode in HALT mode
- Safety Function (IEC60730/60335 Class B)
 - RAM/SFR guard
 - Automatic program memory CRC calculation
 - RAM parity error detection
 - ROM unused area access reset (instruction access)
 - Clock mutual monitoring
 - WDT counter monitoring
 - SA-ADC test
 - UART test
 - Synchronous serial I/O test
 - I²C bus test
 - GPIO test

- Shipping package

Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Packing form and Product name	
			Tray	Tape & Reel
16 pin plastic SSOP	5.0 × 4.4 (5.0 × 6.4)	0.65	ML62Q1323-xxxMBZ0ARL ML62Q1324-xxxMBZ0ARL ML62Q1325-xxxMBZ0ARL	ML62Q1323-xxxMBZ0ATL ML62Q1324-xxxMBZ0ATL ML62Q1325-xxxMBZ0ATL
16 pin plastic WQFN	4.0 × 4.0 (-)	0.50	ML62Q1323-xxxGDZWAX ML62Q1324-xxxGDZWAX ML62Q1325-xxxGDZWAX	ML62Q1323-xxxGDZWBX ML62Q1324-xxxGDZWBX ML62Q1325-xxxGDZWBX
20 pin plastic TSSOP	6.5 × 4.4 (6.5× 6.4)	0.65	ML62Q1333-xxxTDZWARL ML62Q1334-xxxTDZWARL ML62Q1335-xxxTDZWARL	ML62Q1333-xxxTDZWATL ML62Q1334-xxxTDZWATL ML62Q1335-xxxTDZWATL
24 pin plastic WQFN	4.0 × 4.0 (-)	0.50	ML62Q1345-xxxGDZWAX ML62Q1346-xxxGDZWAX ML62Q1347-xxxGDZWAX	ML62Q1345-xxxGDZWBX ML62Q1346-xxxGDZWBX ML62Q1347-xxxGDZWBX
32 pin plastic TQFP	7.0 × 7.0 (9.0 × 9.0)	0.80	ML62Q1365-xxxTBZWAX ML62Q1366-xxxTBZWAX ML62Q1367-xxxTBZWAX	ML62Q1365-xxxTBZWBX ML62Q1366-xxxTBZWBX ML62Q1367-xxxTBZWBX
32 pin plastic WQFN	5.0 × 5.0 (-)	0.5	ML62Q1365-xxxGDZWAX ML62Q1366-xxxGDZWAX ML62Q1367-xxxGDZWAX	ML62Q1365-xxxGDZWBX ML62Q1366-xxxGDZWBX ML62Q1367-xxxGDZWBX

ML62Q1300 Group how to read the part number

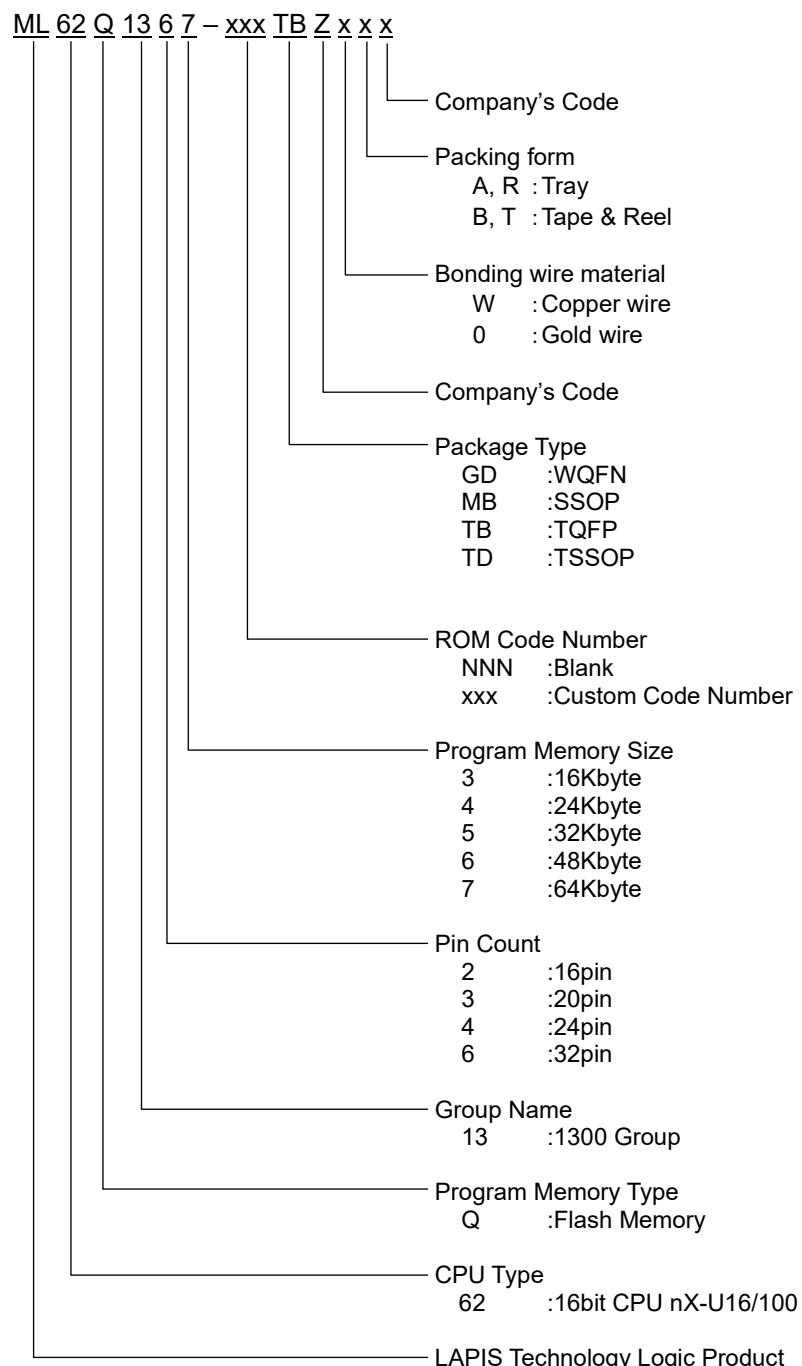


Figure 1 ML62Q1300 Group Part Number

ML62Q1300 Group Main Function List

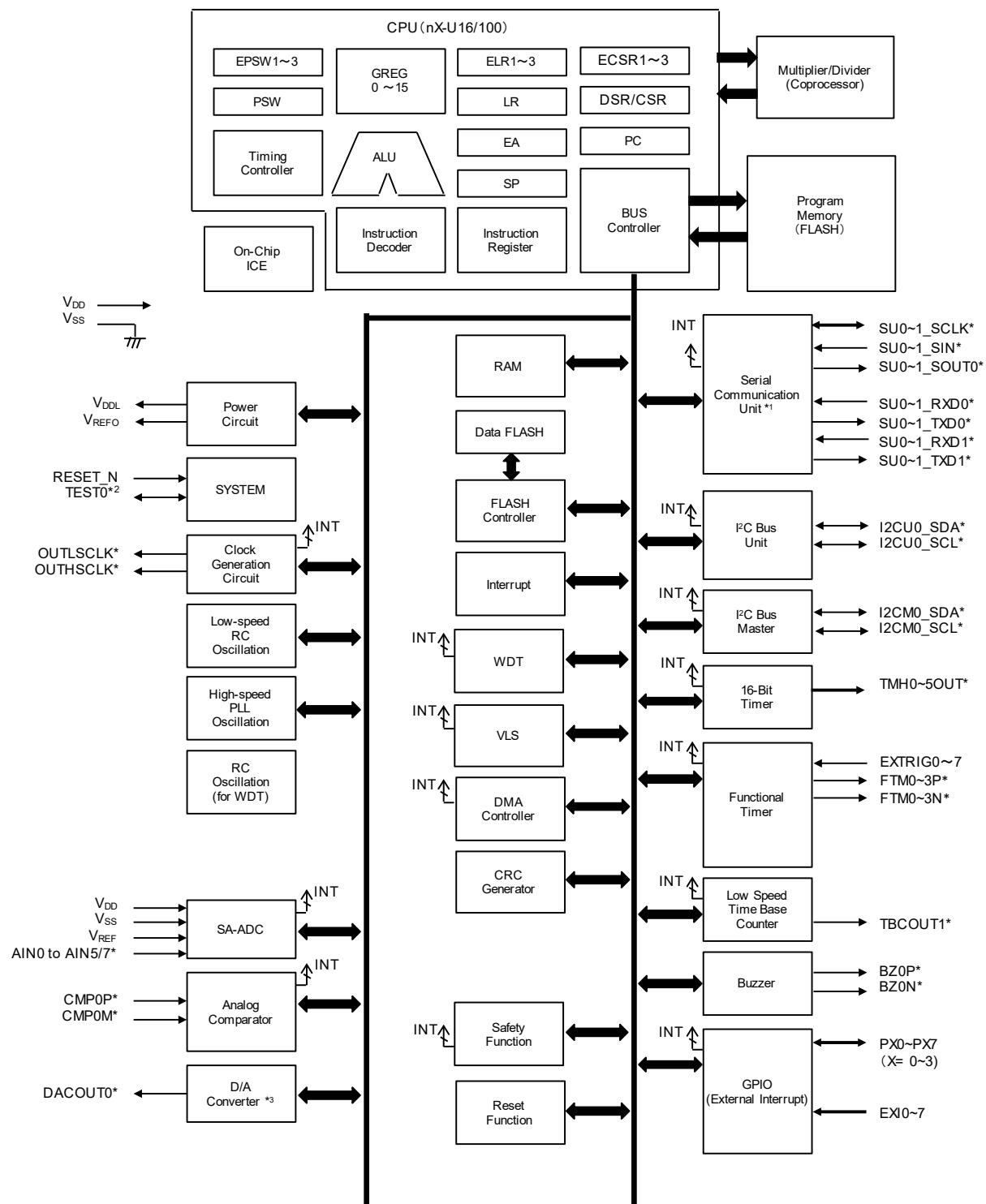
Table 2 ML62Q1300 Group Main Function List

Part number	Pin		Interrupt	Timer	Serial		Analog	
	8bit D/A converter [channel]	0			Analog comparator [input pin]	2	Analog comparator [channel]	1
ML62Q1323								
ML62Q1324								
ML62Q1325								
ML62Q1333								
ML62Q1334								
ML62Q1335								
ML62Q1345								
ML62Q1346								
ML62Q1347								
ML62Q1365								
ML62Q1366								
ML62Q1367								
	Total pin-counts	16	20	24	32	3	1	
	Reset Input pin							
	Power pin counts							

*¹: One 16-bit timer is configurable as two 8-bit timers.

*²: Synchronous Communication unit includes UART and Synchronous Serial Port. UART mode and Synchronous Serial Port can not be used at the same time in the same channel.

BLOCK DIAGRAM



* : Indicates the shared function of general ports.

*1: Shared UART and Synchronous Serial Port.

*2: Not available as the input port when connecting to the on-chip debug emulator.

*3: ML62Q133x and ML62Q132x does not have the peripheral circuits.

Figure 2 ML62Q1300 Group Block Diagram

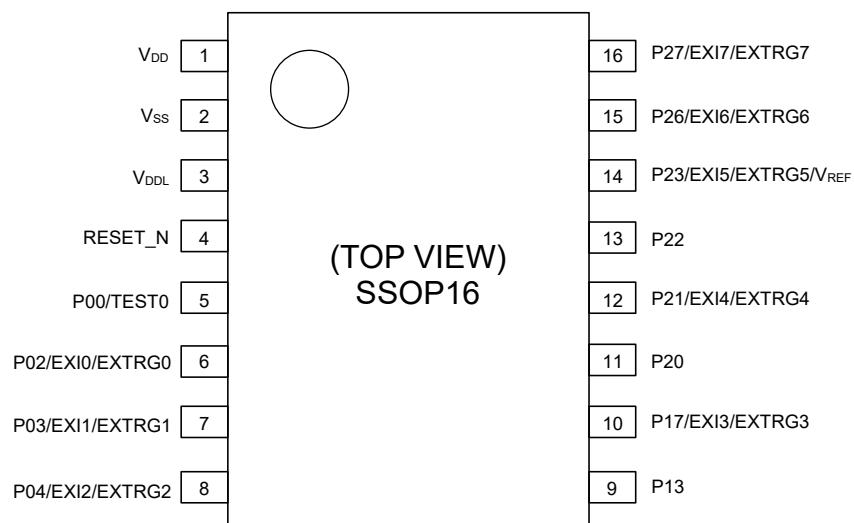
PIN CONFIGURATION**Pin Layout of ML62Q1323/1324/1325 16pin SSOP Package**

Figure 3 Pin Layout of 16pin SSOP Package

Pin Layout of ML62Q1323/1324/1325 16pin WQFN Package

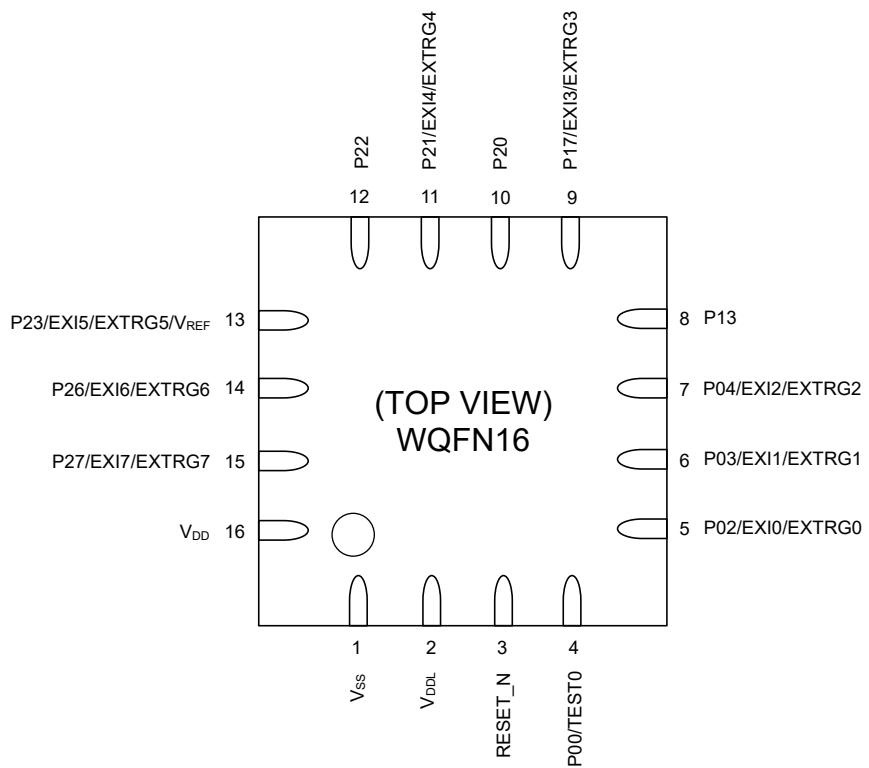


Figure 4 Pin Layout of 16pin WQFN Package

Pin Layout of ML62Q1333/1334/1335 20pin TSSOP Package

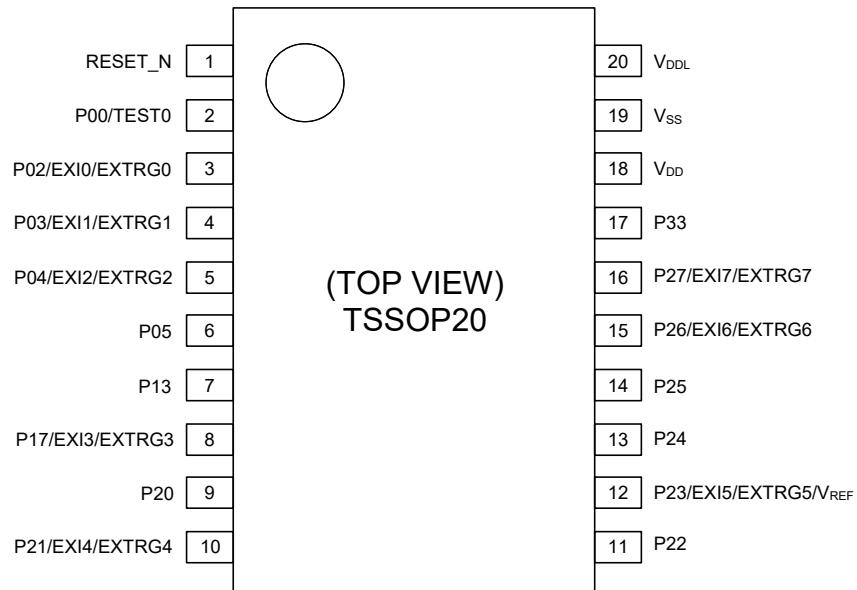


Figure 5 Pin Layout of 20pin TSSOP Package

Pin Layout of ML62Q1345/1346/1347 24pin WQFN Package

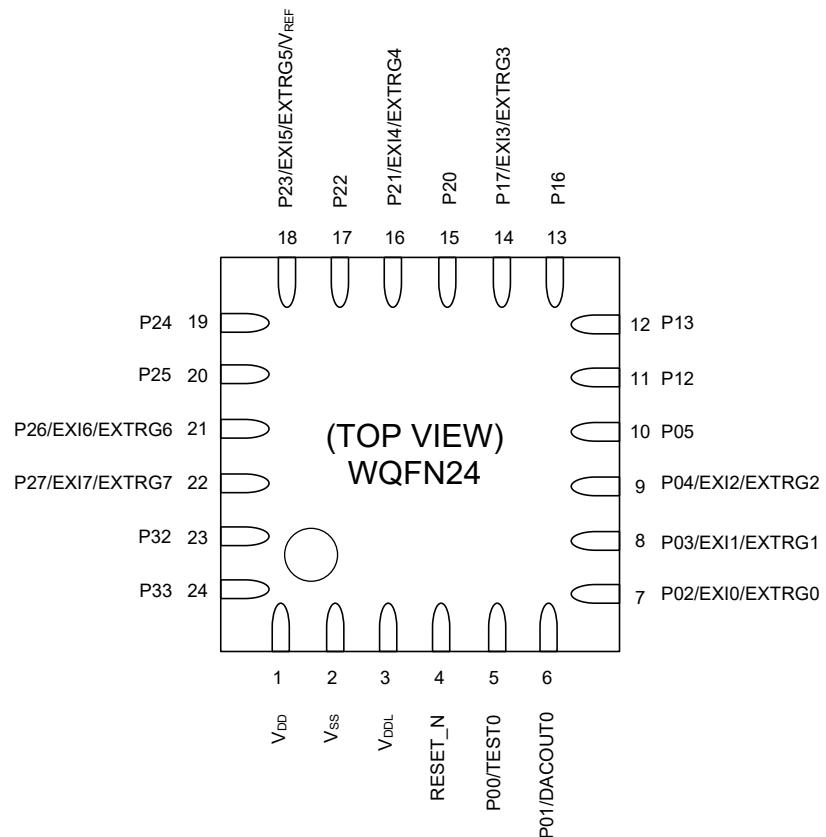


Figure 6 Pin Layout of 24pin WQFN Package

Pin Layout of ML62Q1365/1366/1367 32pin TQFP Package

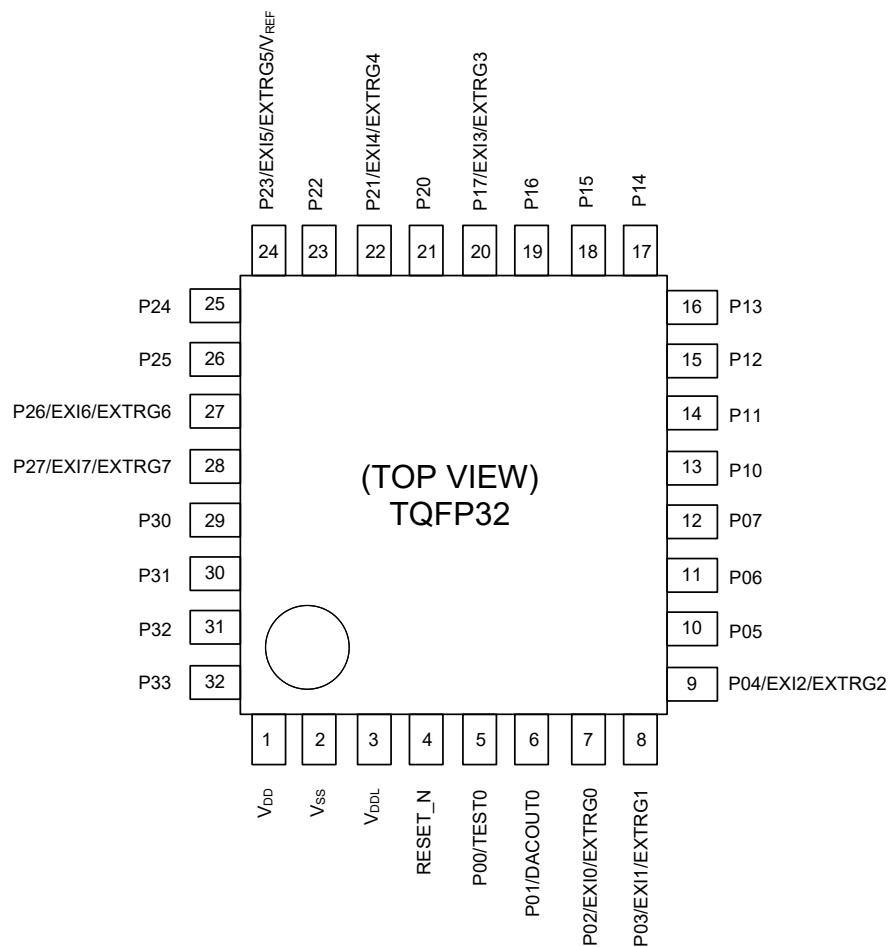


Figure 7 Pin Layout of 32pin TQFP Package

Pin Layout of ML62Q1365/1366/1367 32pin WQFN Package

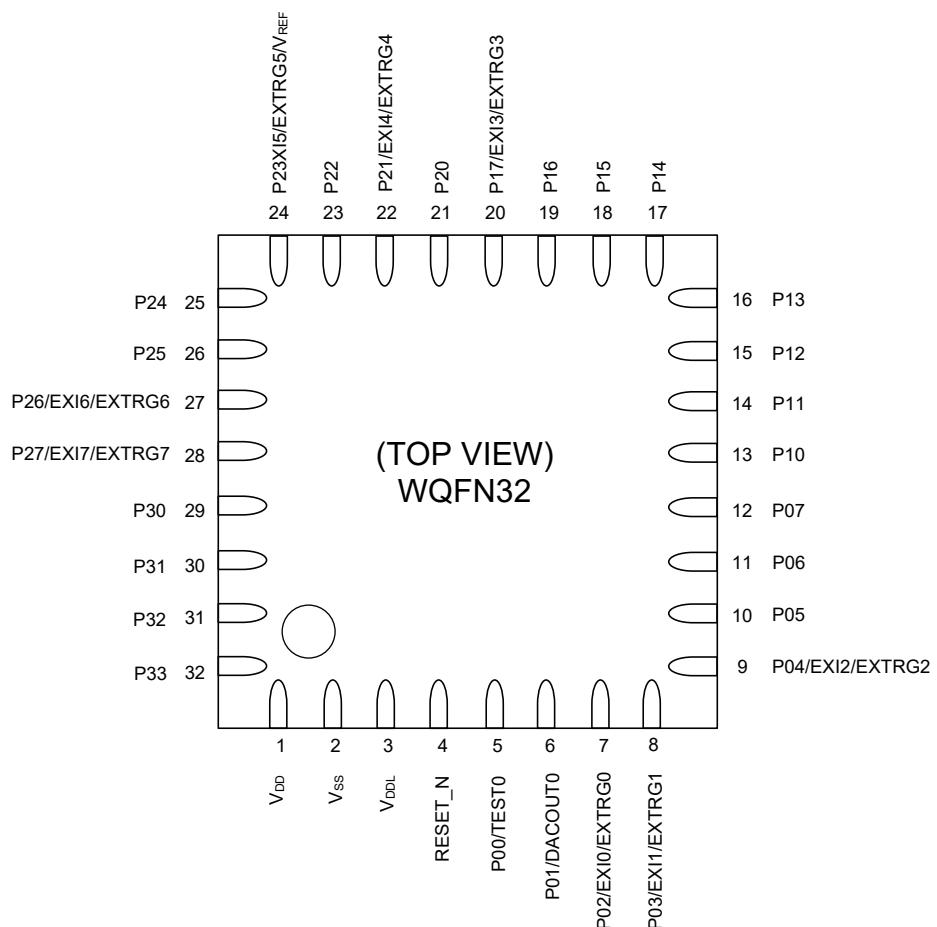


Figure 8 Pin Layout of 32pin WQFN Package

PIN LIST

Table 3 Pin List

Pin No.					Pin name (Primary function)	Primary function Others	2 nd function Communications	3 rd function Communications	4 th function Communications	5 th function Timers	6 th function Others	7 th function Others	8 th function ADC
16Pin No.(SSOP)	16Pin No.(W/QFN)	20Pin No.(TSSOP)	24Pin No.(W/QFN)	32Pin No.(TQFP) (MQFN)									
1	16	18	1	1	V _{DD}	-	-	-	-	-	-	-	-
2	1	19	2	2	V _{SS}	-	-	-	-	-	-	-	-
3	2	20	3	3	V _{DDL}	-	-	-	-	-	-	-	-
4	3	1	4	4	RESET_N	-	-	-	-	-	-	-	-
5	4	2	5	5	P00	TEST0	-	-	-	-	-	-	-
-	-	-	6	6	P01	DACOUT0	-	-	-	-	-	-	-
6	5	3	7	7	P02	EXI0 EXTRG0	SU0_RXD0 SU0_SIN	-	-	FTM0P	OUTLSCLK	CMP0M	-
7	6	4	8	8	P03	EXI1 EXTRG1	SU0_TXD0 SU0_SOUT	SU0_TXD1	I2CU0_SDA	FTM0N	OUTHCLK	CMP0P	-
8	7	5	9	9	P04	EXI2 EXTRG2	SU0_SCLK	-	I2CU0_SCL	TMH0OUT	-	-	-
-	-	6	10	10	P05	-	-	-	-	-	-	-	-
-	-	-	-	11	P06	-	-	-	I2CM0_SDA	-	-	-	-
-	-	-	-	12	P07	-	SU0_RXD1	SU0_RXD0	I2CM0_SCL	-	-	-	-
-	-	-	-	13	P10	-	SU0_TXD1	-	-	-	-	-	-
-	-	-	-	14	P11	-	SU0_SCLK	-	-	-	-	-	-
-	-	-	11	15	P12	-	SU0_RXD0 SU0_SIN	-	-	TMH4OUT	-	-	-
9	8	7	12	16	P13	-	SU0_TXD0 SU0_SOUT	SU0_TXD1	-	TMH1OUT	-	TMH3OUT	-
-	-	-	-	17	P14	-	-	-	-	-	-	-	-
-	-	-	-	18	P15	-	-	-	I2CU0_SDA	-	-	-	-
-	-	-	13	19	P16	-	SU1_SCLK	-	I2CU0_SCL	TMH5OUT	-	-	-
10	9	8	14	20	P17	EXI3 EXTRG3	SU0_RXD1	SU0_RXD0	-	FTM1P	-	BZ0P	AIN0
11	10	9	15	21	P20		SU0_TXD1	-	-	FTM1N	TBCOUT1	BZ0N	AIN1
12	11	10	16	22	P21	EXI4 EXTRG4	SU1_RXD0 SU1_SIN	-	-	FTM2P	OUTLSCLK	-	AIN2
13	12	11	17	23	P22	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	I2CM0_SDA	FTM2N	OUTHCLK	-	AIN3
14	13	12	18	24	P23	EXI5 EXTRG5 V _{REF}	SU1_SCLK	-	I2CM0_SCL	TMH2OUT	-	-	V _{REFO}
-	-	13	19	25	P24	-	SU1_RXD0 SU1_SIN	-	-	-	-	-	AIN4
-	-	14	20	26	P25	-	SU1_TXD0 SU1_SOUT	SU1_TXD1	-	-	-	-	AIN5
15	14	15	21	27	P26	EXI6 EXTRG6	SU1_RXD1	SU1_RXD0	I2CU0_SDA	FTM3P	-	BZ0P	AIN6
16	15	16	22	28	P27	EXI7 EXTRG7	SU1_TXD1	-	I2CU0_SCL	FTM3N	TBCOUT1	BZ0N	AIN7
-	-	-	-	29	P30	-	-	-	-	-	-	-	-
-	-	-	-	30	P31	-	-	-	-	-	-	-	-
-	-	-	23	31	P32	-	SU1_RXD1	SU1_RXD0	-	-	-	-	-
-	-	17	24	32	P33	-	SU1_TXD1	-	-	TMH3OUT	-	-	-

PIN DESCRIPTION

Table 4 Pin Description (1/4)

Function	Signal name	Pin name	I/O	Description	Logic
Power	-	V _{SS}	-	Negative power supply pin (-)	-
	-	V _{DD}	-	Positive power supply pin (+). Connect a capacitor C _V between this pin and V _{SS} .	-
	-	V _{DDL}	-	Power supply pin for internal logic (internal regulator's output). Connect a capacitor C _L (1μF) between this pin and V _{SS} .	-
Test	TEST0	P00	I/O	Input for testing, is used as on-chip debug interface and ISP function. P00 is initialized as pull-up input mode by the system reset.	-
System	V _{REFO}	P23	-	Reference voltage output	-
	RESET_N	RESET_N	I	Reset input. Applying "L" level shifts the MCU in system reset mode. Applying "H" level shifts the CPU in program running mode. Used for on-chip debug interface and ISP function. No pull-up resistor is installed.	Negative
	OUTLSCLK	P02 P21	O	Low-speed clock output.	-
	OUTHSCLK	P03 P22	O	High-speed clock output.	-
	P00	P00	I/O	General purpose I/O port - High impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output Not available to use as I/O pin when using for on-chip debug interface or ISP function.	Positive
General port (GPIO)	P01 – P07	P01 – P07	I/O	General purpose I/O - High impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output	Positive
	P10 – P17	P10 – P17			
	P20 – P27	P20 – P27			
	P30 – P33	P30 – P33			

Table 4 Pin Description (2/4)

Function	Signal name	Pin name	I/O	Description	Logic
UART	SU0_TXD0	P03	O	Serial communication unit0 UART0 data output	Positive
		P13			
	SU0_RXD0	P02	I	Serial communication unit0 Full-duplex data input	Positive
		P07			
		P12		Serial communication unit0 UART0 data input	
		P17			
	SU0_TXD1	P03	O	Serial communication unit0 Full-duplex data output	Positive
		P10			
		P13		Serial communication unit0 UART1 data output	
		P20			
	SU0_RXD1	P07	I	Serial communication unit0 UART1 data input	Positive
		P17			
	SU1_TXD0	P22	O	Serial communication unit1 UART0 data output	Positive
		P25			
	SU1_RXD0	P21	I	Serial communication unit1 Full-duplex data input	Positive
		P24			
		P26		Serial communication unit1 UART0 data input	
		P32			
	SU1_TXD1	P22	O	Serial communication unit1 Full-duplex data output	Positive
		P25			
		P27		Serial communication unit1 UART1 data output	
		P33			
	SU1_RXD1	P26	I	Serial communication unit1 UART1 data input	Positive
		P32			
Synchronous Serial Port	SU0_SIN	P02	I	Serial communication unit0 Synchronous serial data input	Positive
		P12			
	SU0_SCLK	P04	I/O	Serial communication unit0 Synchronous serial clock I/O	Positive
		P11			
	SU0_SOUT	P03	O	Serial communication unit0 Synchronous serial data output	Positive
		P13			
	SU1_SIN	P21	I	Serial communication unit1 Synchronous serial data input	Positive
		P24			
I ² C Bus	I2CU0_SDA	P16	I/O	Serial communication unit1 Synchronous serial clock I/O	Positive
		P23			
		P22		Serial communication unit1 Synchronous serial data output	
	I2CM0_SDA	P25	O		Positive
		P03	I/O	I ² C Unit0 (Master and Slave) Data I/O N-channel open drain Connect a pull-up resistor externally	
		P15			
	I2CM0_SCL	P26			
		P04	I/O	I ² C Unit0 (Master and Slave) Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive
		P16			
	I2CM0_SDA	P27			
		P06	I/O	I ² C Master0 Data I/O pin N-channel open drain output Connect a pull-up resistor externally	Positive
		P22			
	I2CM0_SCL	P07	I/O	I ² C Master0 Clock I/O N-channel open drain output Connect a pull-up resistor externally	Positive
		P23			

Table 4 Pin Description (3/4)

Function	Signal name	Pin name	I/O	Description	Logic
Functional Timer (FTM)	FTM0P	P02	O	Functional Timer0 P output	Positive
	FTM0N	P03	O	Functional Timer0 N output	Negative
	FTM1P	P17	O	Functional Timer1 P output	Positive
	FTM1N	P20	O	Functional Timer1 N output	Negative
	FTM2P	P21	O	Functional Timer2 P output	Positive
	FTM2N	P22	O	Functional Timer2 N output	Negative
	FTM3P	P26	O	Functional Timer3 P output	Positive
	FTM3N	P27	O	Functional Timer3 N output	Negative
	EXTRG0	P02	I	Functional Timer event trigger input	—
	EXTRG1	P03	I	Functional Timer event trigger input	—
	EXTRG2	P04	I	Functional Timer event trigger input	—
	EXTRG3	P17	I	Functional Timer event trigger input	—
	EXTRG4	P21	I	Functional Timer event trigger input	—
	EXTRG5	P23	I	Functional Timer event trigger input	—
	EXTRG6	P26	I	Functional Timer event trigger input	—
	EXTRG7	P27	I	Functional Timer event trigger input	—
16bit General Timer	TMH0OUT	P04	O	16bit General Timer 0 output	Positive
	TMH1OUT	P13	O	16bit General Timer 1 output	Positive
	TMH2OUT	P23	O	16bit General Timer 2 output	Positive
	TMH3OUT	P13	O	16bit General Timer 3 output	Positive
		P33			
	TMH4OUT	P12	O	16bit General Timer 4 output	Positive
	TMH5OUT	P16	O	16bit General Timer 5 output	Positive
	EXTRG0	P02	I	16bit General Timer trigger input	—
	EXTRG1	P03	I	16bit General Timer trigger input	—
Low-Speed Time Base Counter (LTBC)	TBCOUT1	P20	O	Low-speed Time Base Counter output	Positive
		P27			
Buzzer	BZ0P	P17	O	Buzzer output (positive phase)	Positive
		P26			
	BZ0N	P20	O	Buzzer output (negative phase)	Negative
		P27			

Table 4 Pin Description (4/4)

Function	Signal name	Pin name	I/O	Description	Logic
External Interrupt	EXI0	P02	I	External interrupt 0 input	—
	EXI1	P03	I	External interrupt 1 input	—
	EXI2	P04	I	External interrupt 2 input	—
	EXI3	P17	I	External interrupt 3 input	—
	EXI4	P21	I	External interrupt 4 input	—
	EXI5	P23	I	External interrupt 5 input	—
	EXI6	P26	I	External interrupt 6 input	—
	EXI7	P27	I	External interrupt 7 input	—
Successive approximation type A/D converter	V _{REF}	P23	-	SA-ADC external reference voltage input	—
	AIN0	P17	I	SA-ADC channel 0 input	—
	AIN1	P20	I	SA-ADC channel 1 input	—
	AIN2	P21	I	SA-ADC channel 2 input	—
	AIN3	P22	I	SA-ADC channel 3 input	—
	AIN4	P24	I	SA-ADC channel 4 input	—
	AIN5	P25	I	SA-ADC channel 5 input	—
	AIN6	P26	I	SA-ADC channel 6 input	—
Analog comparator	CMP0P	P03	I	Comparator input 0 (noninverting input)	—
	CMP0M	P02	I	Comparator input 0 (inverting input)	—
D/A converter	DACOUT0	P01	O	D/A converter0 output	—

TERMINATION OF UNUSED PINS

Table 5 Termination of unused pins

Pin	pin termination
RESET_N	Connect to V _{DD}
P00/TEST0	Connect to V _{DD} with initial state (pulled-up input mode)
P01 to P07	
P10 to P17	
P20 to P27	
P30 to P33	Open the pins with the initial condition of High impedance (input/output invalid) mode.

Note:

- Terminate unused input pins according to the table 5 in order to avoid unexpected through-current in the pins.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage 1	V _{DD}	Ta = +25°C		-0.3 to +6.5	V
Power supply voltage 2	V _{DDL}	Ta = +25°C		-0.3 to +2.0	
Input voltage	V _{IN}	Ta = +25°C		-0.3 to V _{DD} +0.3* ¹	
Output voltage	V _{OUT}	Ta = +25°C		-0.3 to V _{DD} +0.3* ¹	
"H" level output current	I _{OUTH}	Ta = +25°C	1pin Total	-40* ² -150* ²	mA
"L" level output current	I _{OUTL}	Ta = +25°C	1pin Total	+40 +150	
Power dissipation	PD	Ta = +25°C		1	
Storage temperature	T _{STG}	-		-55 to +150	°C

¹ 6.5V or lower² The current flowing out the LSI through the pin is described in the negative number.

The applicable maximum current is the absolute value.

For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

[Note]

Stresses above the absolute maximum ratings listed in the above table may cause permanent damage to the device.

These are stress ratings only and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambient)	T _a	-	-40 to +105	°C
Operating temperature (Chip-Junction)	T _j	-	-40 to +115	
Operating voltage	V _{DD}	-	1.6 to 5.5	V
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.6 to 5.5V	30k to 4M	Hz
		V _{DD} = 1.8 to 5.5V	30k to 25M	
V _{DDL} pin external capacitance	C _L	-	1.0 ±30%	μF

Thermal characteristics

The maximum chip-junction temperature, $T_{j\max}$, may be calculated using the following equation.

$$T_{j\max} = T_{a\max} + P_{D\max} \times \theta_{ja}$$

$T_{a\max}$: maximum ambient temperature

$P_{D\max}$: LSI maximum power dissipation

θ_{ja} : Package junction to ambient thermal resistance

Design a Mounting board by considering heat radiation such as power dissipation and ambient temperature to satisfy the recommended conditions.

The following table shows the each package's thermal resistance for thermal design reference estimated by simulation based on the PCB (printed circuit board) conditions define as a below.

Parameter	Symbol	Package type	Value		Unit
			L1	L2	
Thermal resistance	θ_{ja}	SSOP16	90.5	84.3	°C/W
		WQFN16	80.8	74.7	
		TSSOP20	79.6	74.0	
		WQFN24	59.0	51.0	
		WQFN32	50.6	43.5	
		TQFP32	67.6	61.8	

PCB conditions:

PCB name	L1	L2	Unit
PCB size (L / W / T)	114.3 / 76.2 / 1.6	114.3 / 76.2 / 1.6	mm
Number of layers	1	2	layer
Wiring density	60% (top layer)	60% (top and bottom layer)	-
Wind condition	No wind (0m/s)		

WQFN package's thermal resistance is simulated on the condition that the exposed pad is soldered on the PCB.

Current Consumption 1

Product: ML62Q1323, ML62Q1324, ML62Q1325, ML62Q1333, ML62Q1334, ML62Q1335

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ. * ³	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85°C	-	0.60	17	μA
			Ta = -40 to +105°C	-		36	
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85°C	-	0.75	20	1
			Ta = -40 to +105°C	-		42	
Supply current 2	IDD2	Low-speed RC32K Oscillating. CPU is in HALT state* ¹ . PLL oscillation is stopped.	Ta = -40 to +85°C	-	3.6	27	mA
			Ta = -40 to +105°C	-		44	
Supply current 3	IDD3	CPU: Running with 32kHz RC oscillation clock* ¹ * ² PLL oscillation is stopped.	Ta = -40 to +105°C	-	17	66	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock* ¹ * ² PLL 16MHz is oscillating. V _{DD} = 1.8 to 5.5V	Ta = -40 to +105°C	-	3.1	3.8	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock* ¹ * ² PLL 24MHz is oscillating. V _{DD} = 1.8 to 5.5V	Ta = -40 to +105°C	-	4.4	5.3	

*¹: LTBC and WDT is operating, Significant bits of BCKCON0-3 and BRECON0-3 registers are all "1"*²: CPU running in wait mode*³: On the condition of V_{DD} = 3.0V, Ta = +25°C

Current Consumption 2

Product: ML62Q1345, ML62Q1346, ML62Q1347, ML62Q1365, ML62Q1366, ML62Q1367

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ. * ³	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	-	0.80	18	μA
			Ta = -40 to +105 °C	-		40	
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	-	0.95	21	1
			Ta = -40 to +105 °C	-		45	
Supply current 2	IDD2	Low-speed RC32K Oscillating. CPU is in HALT state* ¹ . PLL oscillation is stopped.	Ta = -40 to +85 °C	-	4.3	33	mA
			Ta = -40 to +105 °C	-		50	
Supply current 3	IDD3	CPU: Running with 32kHz RC oscillation clock* ^{1*²} PLL oscillation is stopped.	Ta = -40 to +105 °C	-	20	70	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock* ^{1*²} PLL 16MHz is oscillating. V _{DD} = 1.8 to 5.5V	Ta = -40 to +105 °C	-	4.3	4.8	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock* ^{1*²} PLL 24MHz is oscillating. V _{DD} = 1.8 to 5.5V	Ta = -40 to +105 °C	-	6.4	7.0	

*¹: LTBC and WDT is operating, Significant bits of BCKCON0-3 and BRECON0-3 registers are all "1"*²: CPU running in wait mode*³ On the condition of V_{DD} = 3.0V, Ta = +25°C

On-chip Oscillator

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed RC oscillator frequency accuracy 1 Without software adjustment	f _{RCL1}	Ta = +25°C V _{DD} = 1.8 to 5.5V	Typ. -1.0%	32.768	Typ. +1.0%	kHz	1
		Ta = -40 to +85°C V _{DD} = 1.8 to 5.5V	Typ. -2.5%	32.768	Typ. +2.5%		
		Ta = -40 to +105°C V _{DD} = 1.8 to 5.5V	Typ. -3.0%	32.768	Typ. +3.0%		
		V _{DD} = 1.6 to 1.8V	Typ. -3.5%	32.768	Typ. -3.5%		
Low-speed RC oscillator frequency accuracy 2 With software adjustment	f _{RCL2}	Ta = -40 to +85°C V _{DD} = 1.8 to 5.5V	Typ. -1.0%	32.768	Typ. +1.0%	MHz	1
		Ta = -40 to +105°C V _{DD} = 1.8 to 5.5V	Typ. -1.5%	32.768	Typ. +1.5%		
PLL oscillation frequency accuracy 1 Without software adjustment	f _{PLL1}	Ta = -40 to +85°C V _{DD} = 1.8 to 5.5V	Typ. -2.5%	16/24	Typ. +2.5%	MHz	1
		Ta = -40 to +105°C V _{DD} = 1.8 to 5.5V	Typ. -3.0%	16/24	Typ. +3.0%		
		V _{DD} = 1.6 to 1.8V	Typ. -3.5%	16/24	Typ. +3.5%		
PLL oscillation frequency accuracy 2 With software adjustment	f _{PLL2}	Ta = -40 to +85°C V _{DD} = 1.8 to 5.5V	Typ. -1.0%	16/24	Typ. +1.0%	MHz	1
		Ta = -40 to +105°C V _{DD} = 1.8 to 5.5V	Typ. -1.5%	16/24	Typ. +1.5%		
PLL oscillation start time	T _{PLL}	V _{DD} = 1.6 to 5.5V	-	-	2	ms	
1kHz Low-speed RC oscillator (for WDT) frequency accuracy	f _{RCL1K}	Ta = -40 to +105°C V _{DD} = 1.6 to 5.5V	0.5	1	2.5	kHz	

Input / Output pin 1

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit	
Output voltage1 "H"/"L" level (P00-P07) (P10-P17) (P20-P27) (P30-P33)	VOH1	IOH1 = -10mA V _{DD} ≥ 4.5V	V _{DD} -1.5	-	-	V	2	
		IOH1 = -1mA V _{DD} ≥ 1.6V	V _{DD} -0.5	-	-			
	VOL1	IOL1 = +10mA V _{DD} ≥ 4.5V	-	-	1.5			
		IOL1 = +1mA V _{DD} ≥ 1.6V	-	-	0.5			
Output voltage2 "L" level (P01-P07) (P10-P17) (P20-P27) (P30-P33)	VOL2	When N-ch open drain output mode is selected	IOLO2 = +15mA V _{DD} ≥ 4.5V	-	-	0.7	V	2
			IOLO2 = +8mA V _{DD} ≥ 3.0V	-	-	0.5		
			IOLO2 = +3mA V _{DD} ≥ 2.0V	-	-	0.4		
			IOLO2 = +2mA V _{DD} ≥ 1.6V	-	-	0.4		

Input / Output pin 2

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
"H" level output current1 *6	IOH1	1pin	V _{DD} ≥ 4.5V	-10*3*5	-	-	mA
			V _{DD} ≥ 1.6V	-1*3*5	-	-	
"H" level output current *1*4	IOH3	Total of 'P00-P07 and P10-P13 or Total of 'P14-P17, P20-P27 and P30-P33 (Duty ≤ 50%)	V _{DD} ≥ 4.5V	-50*5	-	-	3
			V _{DD} ≥ 1.6V	-20*5	-	-	
		All pin total (Duty ≤ 50%)	V _{DD} ≥ 4.5V	-100*5	-	-	
			V _{DD} ≥ 1.6V	-40*5	-	-	
"L" level output current1 *6	IOL1	1pin (CMOS output mode)	V _{DD} ≥ 4.5V	-	-	10*3	mA
			V _{DD} ≥ 1.6V	-	-	1*3	
"L" level output current2 *6	IOL2	1pin (N-ch open drain output mode)	V _{DD} ≥ 4.5V	-	-	15*3	
			V _{DD} ≥ 3.0V	-	-	8*3	
			V _{DD} ≥ 2.0V	-	-	3*3	
			V _{DD} ≥ 1.6V	-	-	2*3	
"L" level output total current *2*4	IOL3	Total of P00-P07 and P10-P13 or Total of P14-P17, P20-P27 and P30-P33 (N-ch open drain output mode, duty ≤ 50%)	V _{DD} ≥ 4.5V	-	-	60	μA
			V _{DD} ≥ 3.0V	-	-	40	
			V _{DD} ≥ 2.0V	-	-	15	
			V _{DD} ≥ 1.6V	-	-	10	
		All pin total (N-ch open drain output mode, duty ≤ 50%)	V _{DD} ≥ 4.5V	-	-	120	
			V _{DD} ≥ 1.6V	-	-	20	
Output leak (P00-P07) (P10-P17) (P20-P27) (P30-P33)	IOOH	VOH = V _{DD} (High impedance mode)	-	-	+1	μA	
	IOOL	VOL = V _{SS} (High impedance mode)	-1*5	-	-		

*1: Sink-out current from V_{DD} to the output pin, which can guarantee the device operation.*2: Sink-in current from the output pin to V_{SS}, which can guarantee the device operation.

*3: Do not exceed total current.

*4: The total current is on the condition of Duty ≤ 50% (same applies to IOH1).

When the duty > 50% the total current is calculated by following formula.

Total current = IOL3 × 50/n (When the duty is n%)

<For an example> When IOL3 = 100mA and n = 80%,

Total current = IOL3 × 50/80 = 62.5mA

Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.

Do not apply current larger than Absolute Maximum Ratings.

*5: The current flowing out the LSI through the pin is described in the negative number.

The applicable maximum current is the absolute value.

For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

*6: These values are satisfied with VOH1, VOL1 and VOL2.

Input / Output pin 3

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit	
Input current1 (RESET_N)	I _{IIH1}	V _{IH1} = V _{DD}	-	-	1	μA	4	
	I _{IIL1}	V _{IL1} = V _{SS}	-1*1	-	-			
Input current2 (P00/TEST0)	I _{IIL2}	V _{IL2} = V _{SS} (pull-up mode) ^{*2}	-1500*1	-300*1	-20*1	kΩ	5	
	V/I _{IIL2}	V _{IL2} = V _{SS} (pull-up mode) ^{*2}	3.7	10	80			
	I _{IIH2Z}	V _{IH2} = V _{DD} (High impedance mode)	-	-	1	μA		
	I _{IIL2Z}	V _{IL2} = V _{SS} (High impedance mode)	-1*1	-	-			
Input current3 (P01-P07) (P10-P17) (P20-P27) (P30-P33)	I _{IIL3}	V _{IL1} = V _{SS} (pull-up mode) ^{*2}	-250*1	-30*1	-2*1	kΩ	5	
	V/I _{IIL3}	V _{IL1} = V _{SS} (pull-up mode) ^{*2}	22	100	800			
	I _{IIH3Z}	V _{IH1} = V _{DD} (High impedance mode)	-	-	1	μA		
	I _{IIL3Z}	V _{IL1} = V _{SS} (High impedance mode)	-1*1	-	-			
Input voltage1 (RESET_N) (P01-P07) (P10-P17) (P20-P27) (P30-P33)	V _{IH1}	-	0.7 x V _{DD}	-	V _{DD}	V	5	
	V _{IL1}	-	0	-	0.3 x V _{DD}			
Input voltage2 (P00/TEST0)	V _{IH2}	-	0.7 x V _{DD}	-	V _{DD}			
	V _{IL2}	-	0	-	0.25 x V _{DD}			
Pin capacitance (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33)	C _{PIN}	f = 10kHz Ta = +25°C	-	-	10	pF	-	

^{*1} The current flowing out the LSI through the pin is described in the negative number.

The applicable maximum current is the absolute value.

For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

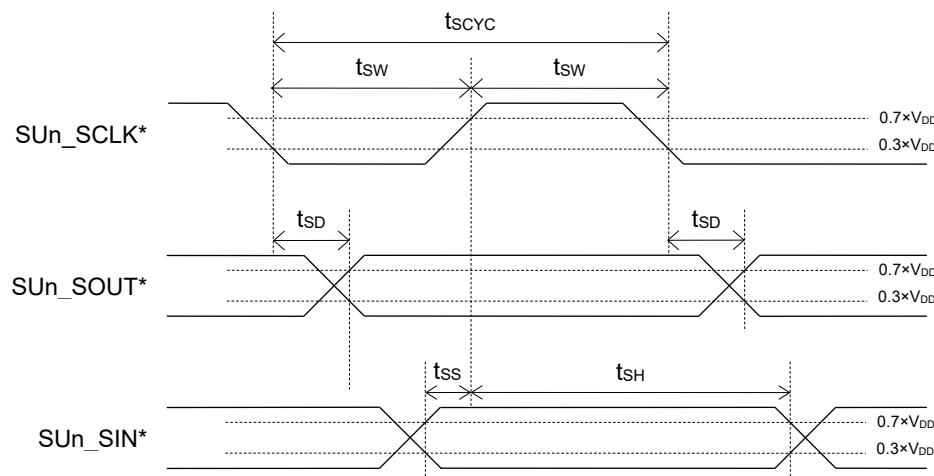
^{*2} Measurement conditions: Typ.: V_{DD} = 3.0V, Max.: V_{DD} = 1.6V, Min.: V_{DD} = 5.5V

Synchronous Serial Port

Slave mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

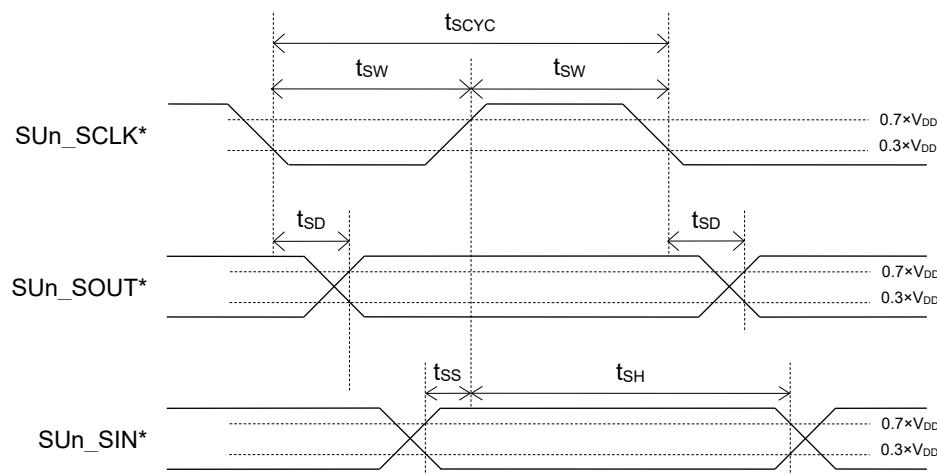
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle	t _{SCYC}	-	1 * ²	-	-	
SCK input pulse width	t _{sw}	-	0.5 * ³	-	-	μs
SOUT output delay time	t _{SD}	V _{DD} = 2.4 to 5.5V	-	-	100+	HSCLK* ¹ ×3
		V _{DD} = 1.8 to 5.5V	-	-	200+	
SIN input setup time	t _{ss}	-	HSCLK* ¹ ×1	-	-	ns
SIN input hold time	t _{SH}	-	80+ HSCLK* ¹ ×3	-	-	

¹: Cycle of high speed clock²: Need input cycles of HSCLK x8 or longer³: Need input cycles of HSCLK x4 or longer* 2nd to 8th function of port, n = 0 to 1

Master mode

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK output cycle	t _{SCYC}	-	-	SCLK* ¹	-	
SCK output pulse width	t _{sw}	-	SCLK* ¹ ×0.4	SCLK* ¹ ×0.5	SCLK* ¹ ×0.6	
SOUT output delay time	t _{SD}	V _{DD} = 2.4 to 5.5V	-	-	100	ns
		V _{DD} = 1.8 to 5.5V	-	-	160	
SIN input setup time	t _{ss}	V _{DD} = 2.4 to 5.5V	120	-	-	
		V _{DD} = 1.8 to 5.5V	180	-	-	
SIN input hold time	t _{SH}	V _{DD} = 2.4 to 5.5V	80	-	-	
		V _{DD} = 1.8 to 5.5V	100	-	-	

¹: Clock cycle selected by bit12 to 8 (SnCK4 to 0) of the serial port n mode register (SIOOnMOD)V_{DD} ≥ 2.4V: min. 250ns, V_{DD} ≥ 1.8V: min. 500ns* 2nd to 8th function of port, n = 0 to 1

I²C Bus Interface

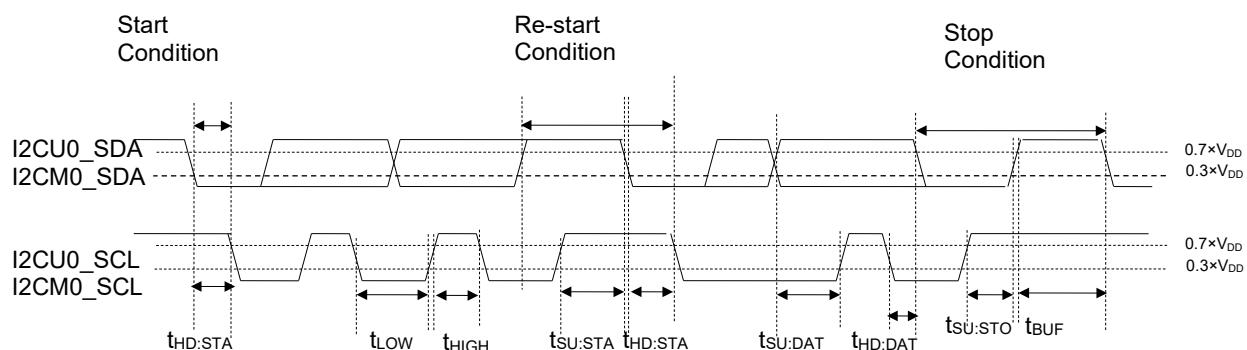
Standard Mode (100k bit/s)

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f _{SCL}	-	0	-	100	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	-	4.0	-	-	
SCL "L" level time	t _{LOW}	-	4.7	-	-	
SCL "H" level time	t _{HIGH}	-	4.0	-	-	
SCL setup time (restart condition)	t _{SU:STA}	-	4.7	-	-	
SDA hold time	t _{HD:DAT}	-	0	-	-	
SDA setup time	t _{SU:DAT}	-	0.25	-	-	
SDA setup time (stop condition)	t _{SU:STO}	-	4.0	-	-	
Bus-free time	t _{BUF}	-	4.7	-	-	

μs

When using the I²C as the master, configure the I²C master n mode register (I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



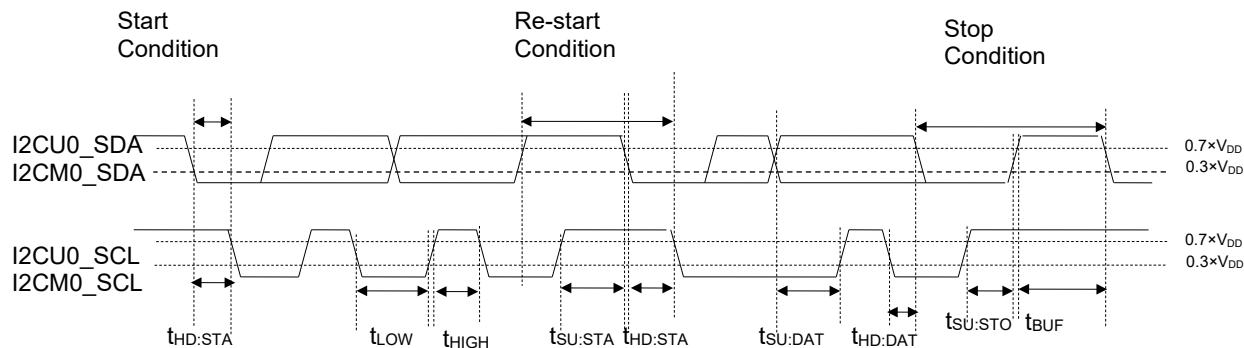
Fast Mode (400k bit/s)

 $(V_{DD} = 1.8 \text{ to } 5.5V, V_{SS} = 0V, Ta = -40 \text{ to } +105^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	-	0	-	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	-	0.6	-	-	
SCL "L" level time	t_{LOW}	-	1.3	-	-	
SCL "H" level time	t_{HIGH}	-	0.6	-	-	
SCL setup time (restart condition)	$t_{SU:STA}$	-	0.6	-	-	
SDA hold time	$t_{HD:DAT}$	-	0	-	-	
SDA setup time	$t_{SU:DAT}$	-	0.1	-	-	
SDA setup time (stop condition)	$t_{SU:STO}$	-	0.6	-	-	
Bus-free time	t_{BUF}	-	1.3	-	-	

μs

When using the I²C as the master, configure the I²C master n mode register (I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

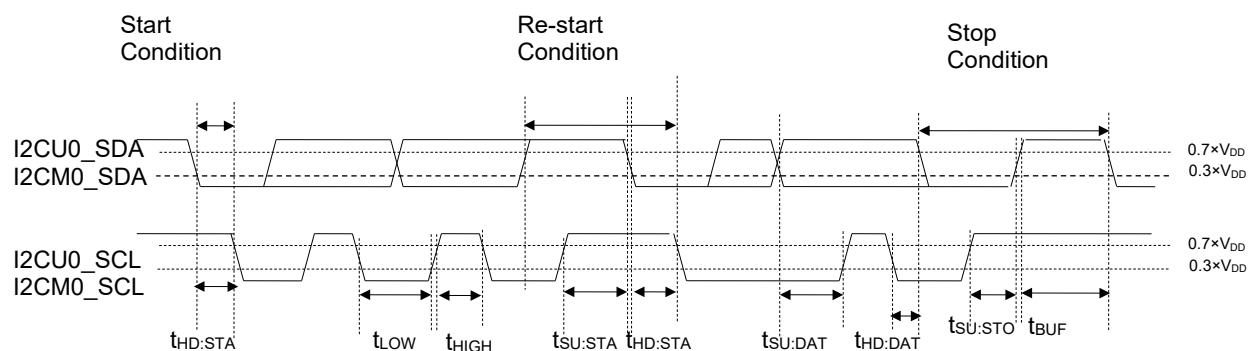


1Mbps Mode (1M bit/s)

(V_{DD} = 2.7 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f _{SCL}	-	0	-	1000	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	-	0.26	-	-	μs
SCL "L" level time	t _{LOW}	-	0.5	-	-	
SCL "H" level time	t _{HIGH}	-	0.26	-	-	
SCL setup time (restart condition)	t _{SU:STA}	-	0.26	-	-	
SDA hold time	t _{HD:DAT}	-	0	-	-	
SDA setup time	t _{SU:DAT}	-	0.1	-	-	
SDA setup time (stop condition)	t _{SU:STO}	-	0.26	-	-	
Bus-free time	t _{BUF}	-	0.5	-	-	

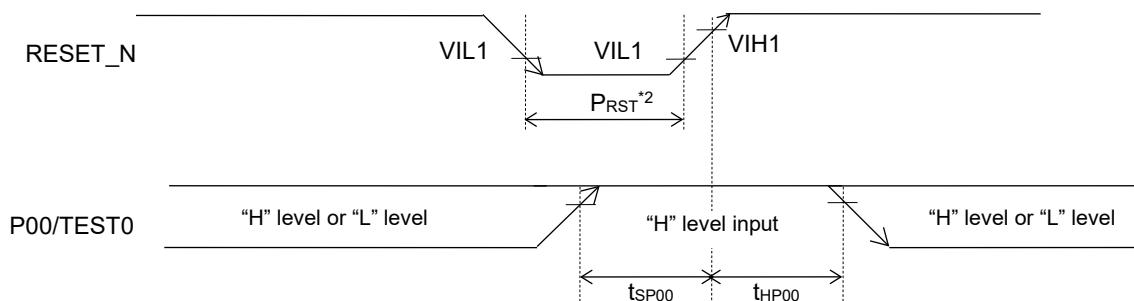
When using the I²C as the master, configure the I²C master n mode register (I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



Reset

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Reset pulse width ^{*2}	P _{RST}	-	2	-	-	ms	1
P00 "H" level setup time ^{*1}	t _{SP00}	-	1	-	-	ms	
P00 "H" level hold time ^{*1}	t _{HP00}	-	1	-	-	ms	

^{*1}: except ISP mode. Refer to the User's manual "25.4 In-System Programming Function" for the timing in ISP mode.^{*2}: V_{DD}=1.6V or over at power on

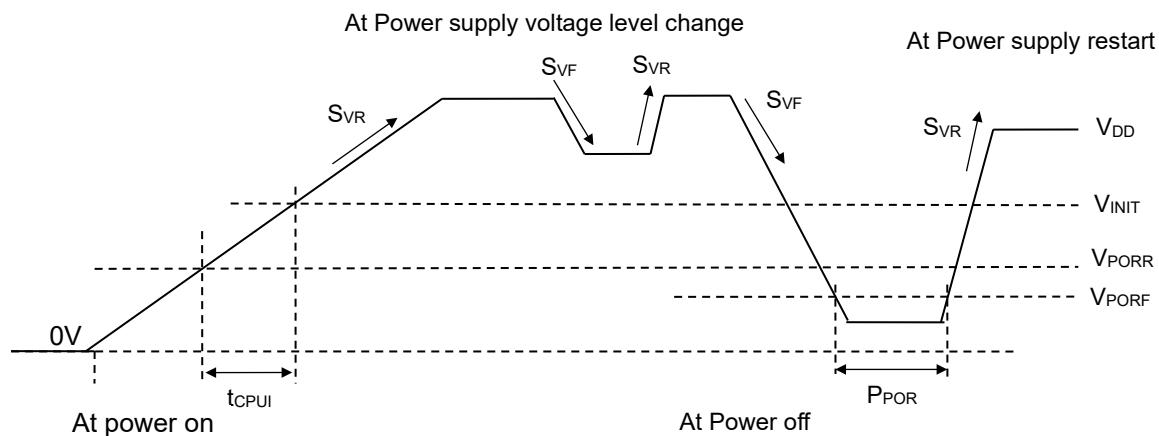
Note:

- RESET_N input shorter pulse than the Reset pulse width (P_{RST}) valid time should be avoided.
The shorter pulse input may cause unexpected behavior.

Slope of Power supply and Power On Reset

(V_{SS} = 0V, -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Power on rising slope	S _{VR}	-	-	-	60	V/ms	1
Power on falling slope	S _{VF}	-	-	-	2	V	
Power on reset detection voltage	V _{PORR}	At Power up (rising)	1.47	1.57	1.80	V	
	V _{PORF}	At Power down (falling)	1.33	1.49	1.58	V	
Power on reset minimum pulse width	P _{POR}	-	200	-	-	μs	
Power on voltage	V _{INIT}	At power on	1.8	-	-	V	
CPU operation start time (from the release of reset to the CPU starts to run)	t _{CPU1}	-	11	16	-	ms	-



Note:

- If a pulse shorter than the Power on reset minimum pulse width is asserted to V_{DD}, it may cause the MCU malfunction.
- Apply prevent measurement such as bypass capacitors or external reset input, and so on.
- Start the high-speed clock when the V_{DD} is within the operating voltage.

VLS

(V_{DD} = 1.6 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
		VLS0LV *1						
VLS threshold voltage *2	V _{VLSR}	00H	Rising	3.86	4.06	4.26	V	1
	V _{VLSF}		Falling	3.84	4.00	4.16		
	V _{VLSR}	01H	Rising	3.57	3.76	3.95		
	V _{VLSF}		Falling	3.55	3.70	3.85		
	V _{VLSR}	02H	Rising	2.94	3.11	3.28		
	V _{VLSF}		Falling	2.92	3.05	3.18		
	V _{VLSR}	03H	Rising	2.85	3.01	3.17		
	V _{VLSF}		Falling	2.83	2.95	3.07		
	V _{VLSR}	04H	Rising	2.75	2.91	3.07		
	V _{VLSF}		Falling	2.73	2.85	2.97		
	V _{VLSR}	05H	Rising	2.66	2.81	2.96		
	V _{VLSF}		Falling	2.64	2.75	2.86		
	V _{VLSR}	06H	Rising	2.56	2.71	2.86		
	V _{VLSF}		Falling	2.54	2.65	2.76		
	V _{VLSR}	07H	Rising	2.46	2.61	2.76		
	V _{VLSF}		Falling	2.44	2.55	2.66		
	V _{VLSR}	08H	Rising	2.37	2.51	2.65		
	V _{VLSF}		Falling	2.35	2.45	2.55		
	V _{VLSR}	09H	Rising	1.98	2.11	2.24		
	V _{VLSF}		Falling	1.96	2.05	2.14		
	V _{VLSR}	0AH	Rising	1.89	2.01	2.13		
	V _{VLSF}		Falling	1.87	1.95	2.03		
	V _{VLSR}	0BH	Rising	1.79	1.91	2.03		
	V _{VLSF}		Falling	1.77	1.85	1.93		
VLS Current	I _{VLS}	-	-	-	50	-	nA	

*1: Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).

*2: The Data VLS0LV = 0CH~0FH is not available to use, if the data is specified it will be the same spec as that 0BH is specified.

Analog Comparator

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Comparator same phase input voltage range	V _{CMR}	Ta = +25°C, V _{DD} = 5.0V	0.1	-	V _{DD} -1.5	V	1
Comparator0 input offset	V _{CMOF}		-	5	-	mV	
Comparator Reference Voltage	V _{CMREF}	-	0.75	0.8	0.85	V	

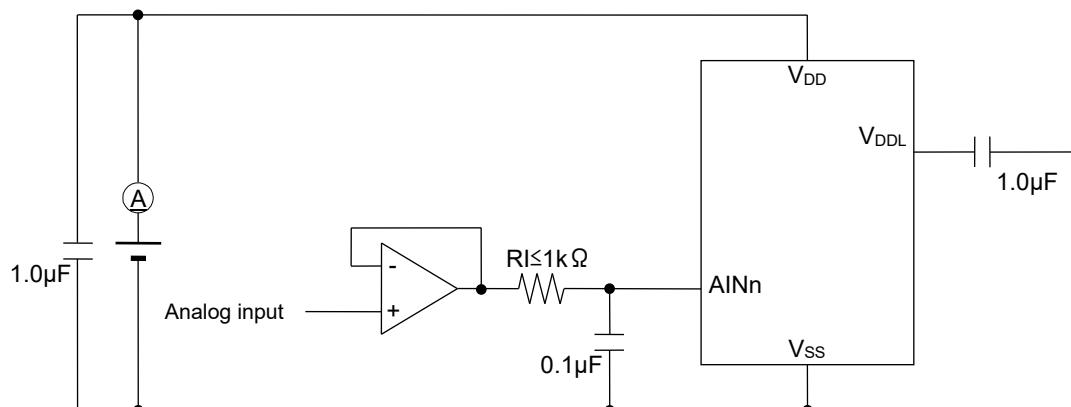
Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n _{AD}	-	-	-	10	bit
Overall error	-	4.5V ≤ Reference voltage* ¹ ≤ 5.5V	-3.5	1.2	3.5	
Integral non-linearity error	INL _{AD}	2.7V ≤ Reference voltage* ¹ ≤ 5.5V	-4	-	4	LSB
		2.2V ≤ Reference voltage* ¹ < 2.7V	-6	-	6	
		1.8V ≤ Reference voltage* ¹ < 2.2V	-10	-	10	
		Reference voltage =Internal reference voltage	-15	-	15	
Differential non-linearity error	DNL _{AD}	2.7V ≤ Reference voltage* ¹ ≤ 5.5V	-3	-	3	
		2.2V ≤ Reference voltage* ¹ < 2.7V	-5	-	5	
		1.8V ≤ Reference voltage* ¹ < 2.2V	-9	-	9	
		Reference voltage =Internal reference voltage	-14	-	14	
Zero-scale error	ZSE	R _I ≤ 1kΩ	-6	-	6	
Full-scale error	FSE	R _I ≤ 1kΩ	-6	-	6	
A/D reference voltage	V _{REF}	-	1.8	-	V _{DD}	V
Internal reference voltage	V _{REFI}	-	1.5	1.55	1.6	
Conversion time	t _{CONV}	4.5V ≤ V _{DD} ≤ 5.5V	2.25	-	427	
		2.2V ≤ V _{DD} ≤ 5.5V	4.5	-	427	μs
		1.8V ≤ V _{DD} ≤ 5.5V	18	-	427	

*¹: V_{DD} or P23/V_{REF} is selected for the reference voltage of Successive Approximation Type A/D Converter.

The current flows during the ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1μF capacitor on the ADC input pin is recommended to reduce the noise.



D/A Converter

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, T_a = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n_{DA}	-	-	-	8	bit
Conversion cycle	t_c	-	10	-	-	μs
Integral non-linearity error	INL_{DA}	$RL = 4M\Omega$	-2	-	2	
Differential non-linearity error	DNL_{DA}	$RL = 4M\Omega$	-1	-	1	LSB
Output impedance	R_o	-	3	6	9	$k\Omega$

Reference Voltage Output

(V_{DD} = 1.8 to 5.5V, V_{SS} = 0V, T_a = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REFO}	-	-	1.55	-	V
Output impedance	R_{VREFO}	-	-	-	500	$k\Omega$

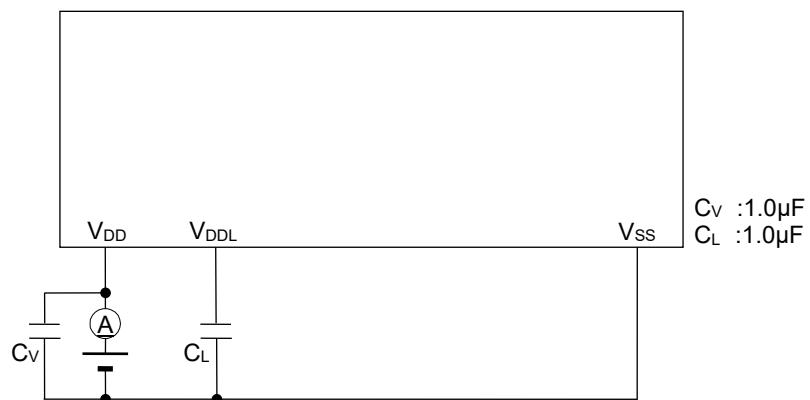
Flash Memory

($V_{SS} = 0V$)

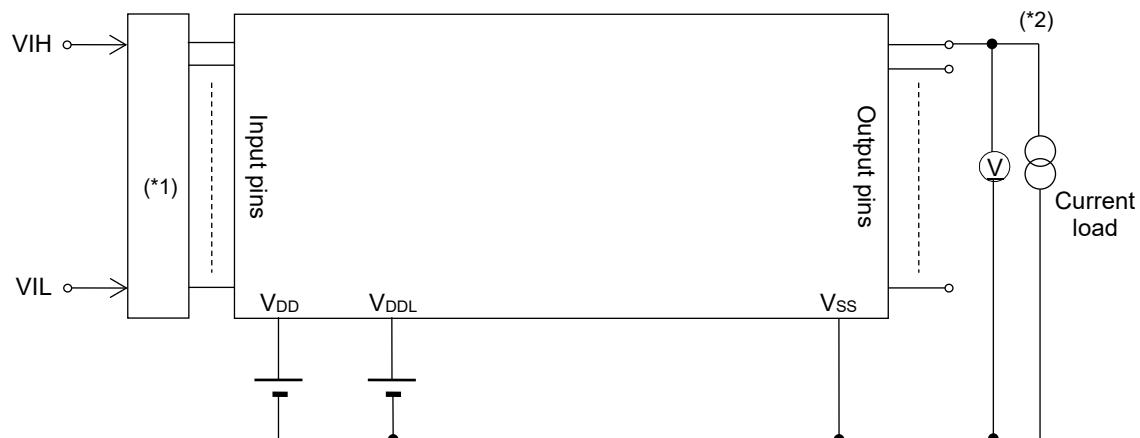
Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase	-40 to +85	°C
		Flash ROM, At write/erase	0 to +40	
Operating voltage	V_{DD}	At write/erase	+1.8 to +5.5	V
Maximum rewrite count	CEPD	Data Flash (4Kbyte)	10000	times
	CEPP	Program Flash	100	
Erase unit	-	Block erase	Program Flash	B
			Data Flash	
	-	Sector erase	Program Flash	B
			Data Flash	
Erase time (Max.)	-	Block erase / Sector erase	50	ms
Write unit	-	Program Flash	4	B
		Data Flash	1	
Write time (Max.)	-	Program Flash	80	μs
		Data Flash	40	
Data retention period	YDR	-	15	years

Measuring circuit

Measuring circuit 1

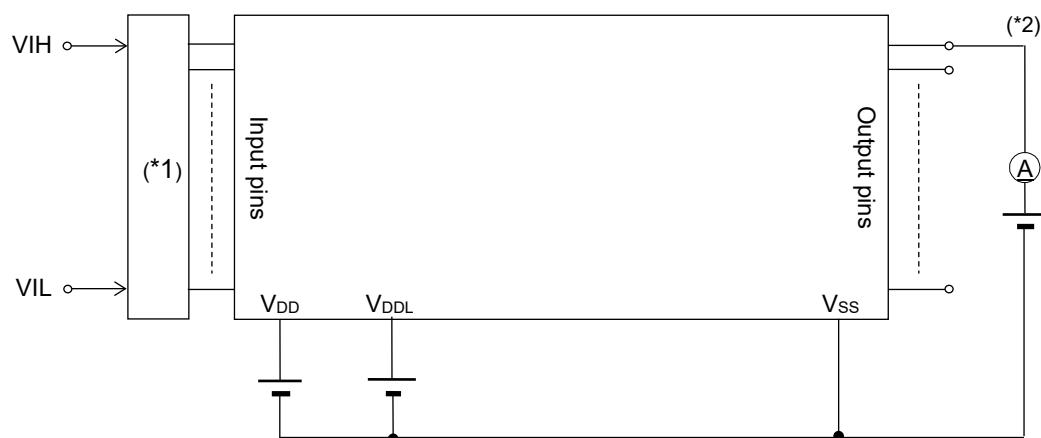


Measuring circuit 2



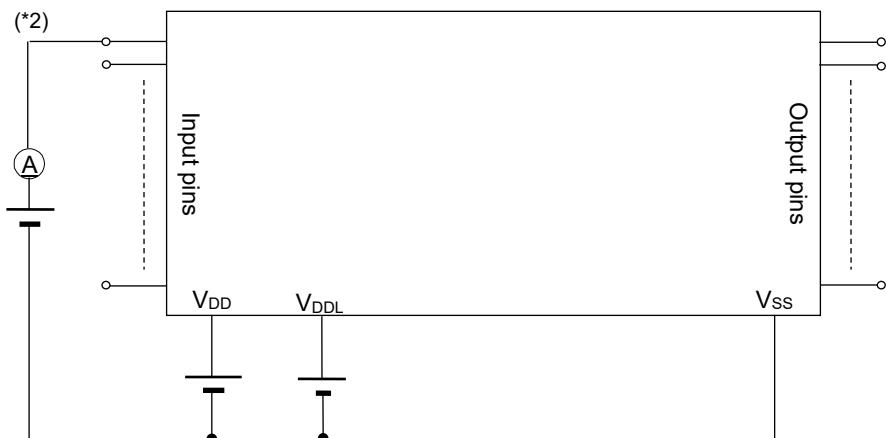
(*1) Input logic circuit to determine the specified measuring conditions
 (*2) Measured connecting specified pins

Measuring circuit 3



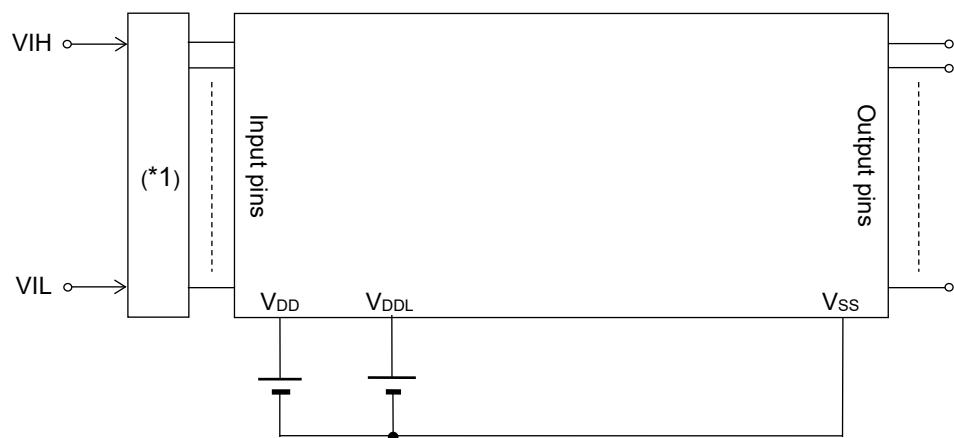
(*1) Input logic circuit to determine the specified measuring conditions
 (*2) Measured connecting specified pins

Measuring circuit 4



(*2) Measured connecting specified pins

Measuring circuit 5

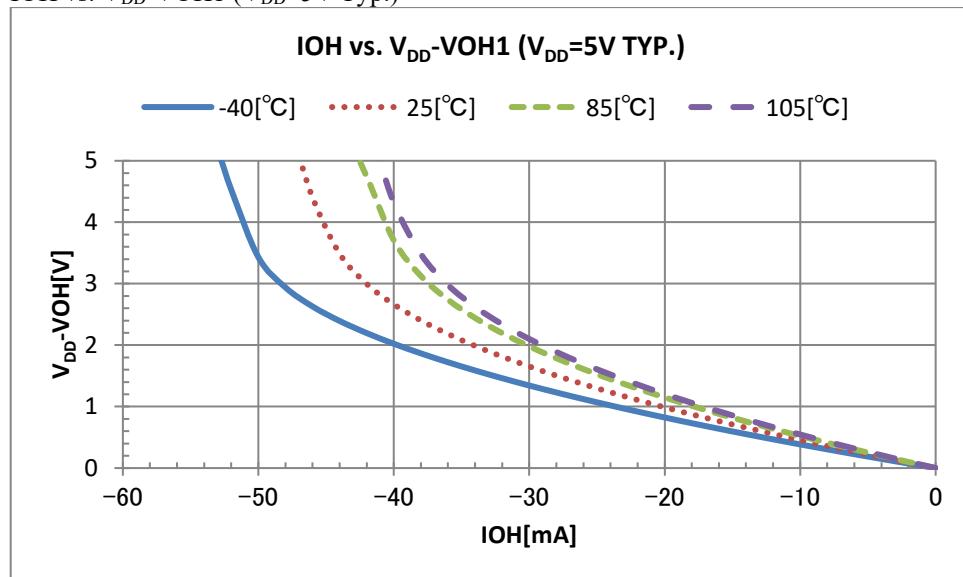


(*1) Input logic circuit to determine the specified measuring conditions

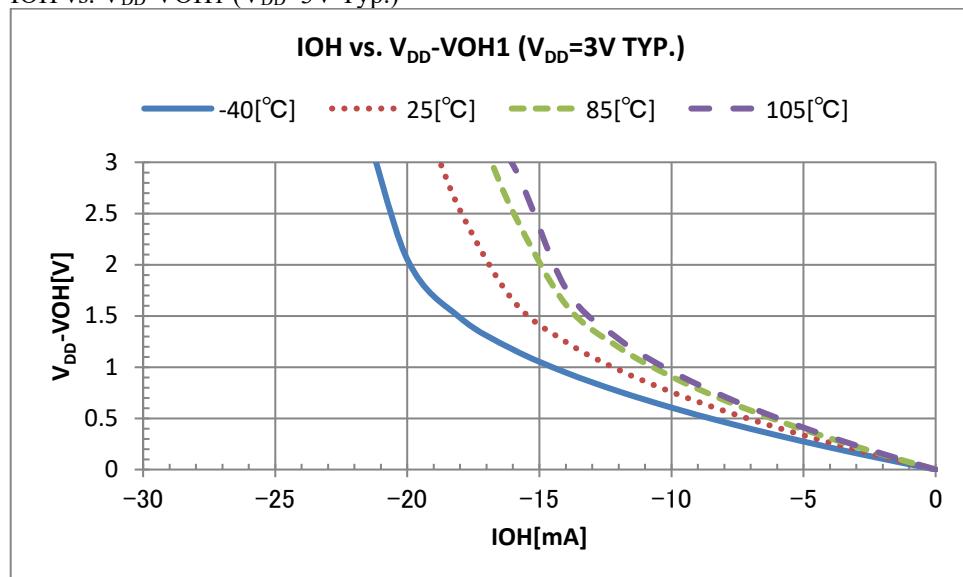
Characteristics graphs

These Graphs on the following pages are references for designing an application.

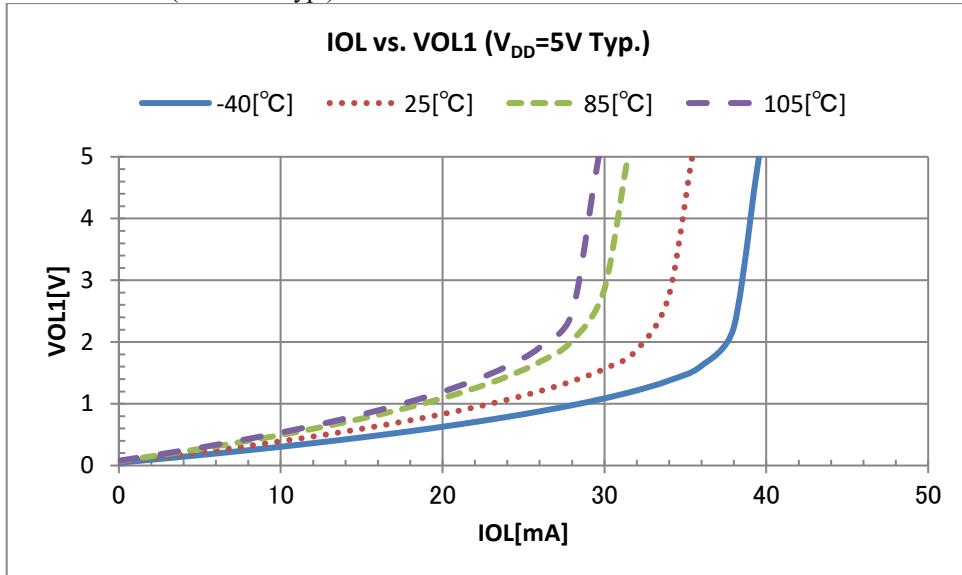
IOH vs. V_{DD}-VOH1 (V_{DD}=5V Typ.)



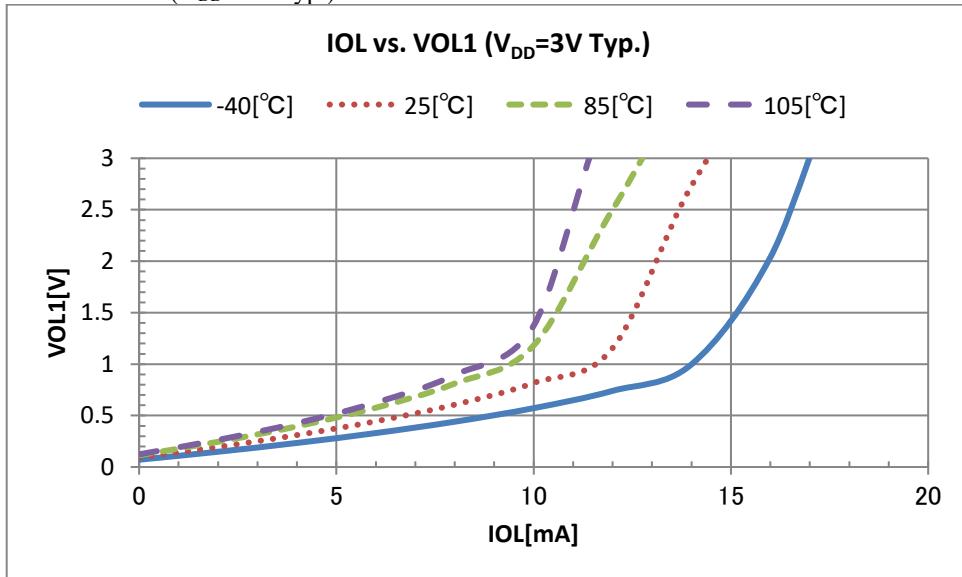
IOH vs. V_{DD}-VOH1 (V_{DD}=3V Typ.)



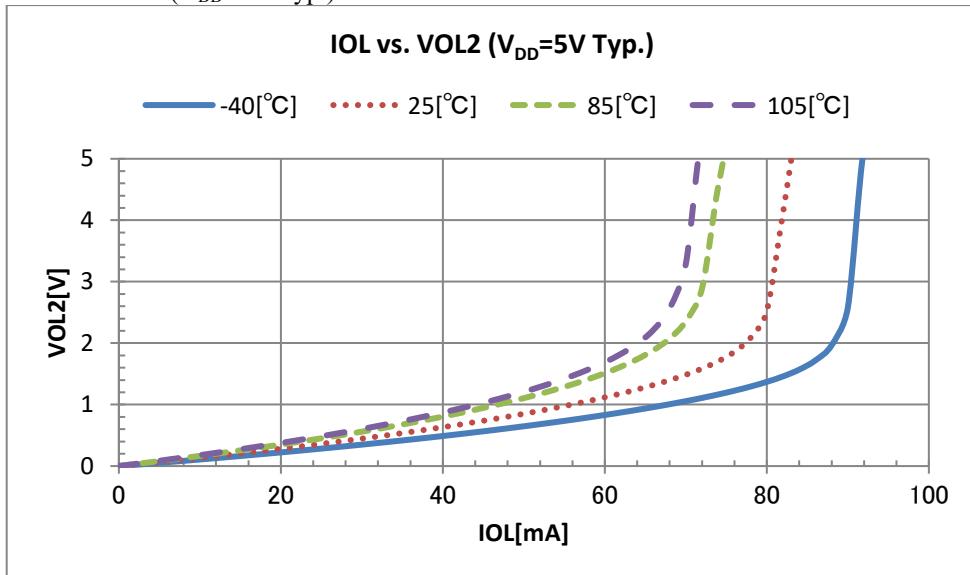
IOL vs. VOL1 ($V_{DD}=5V$ Typ.)



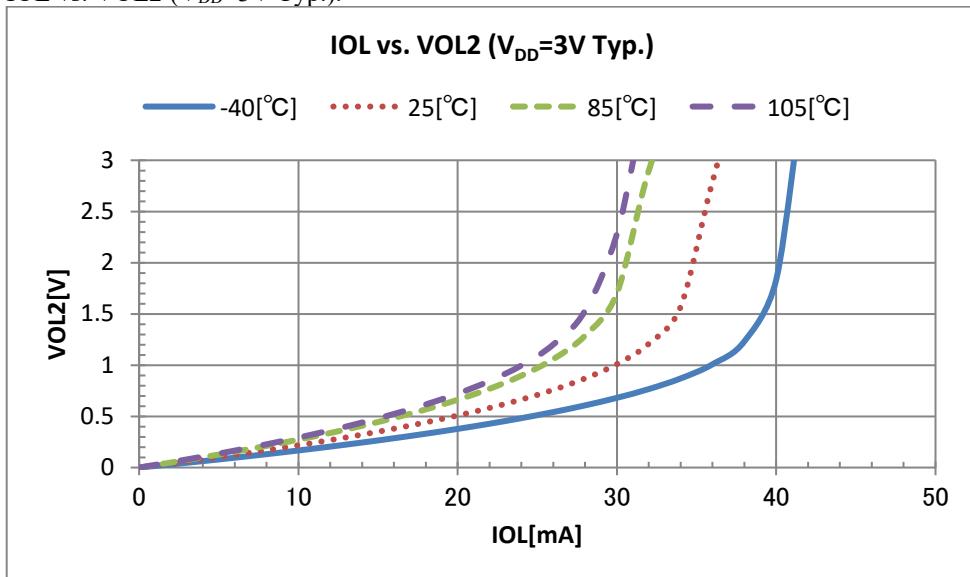
IOL vs. VOL1 ($V_{DD}=3V$ Typ.)



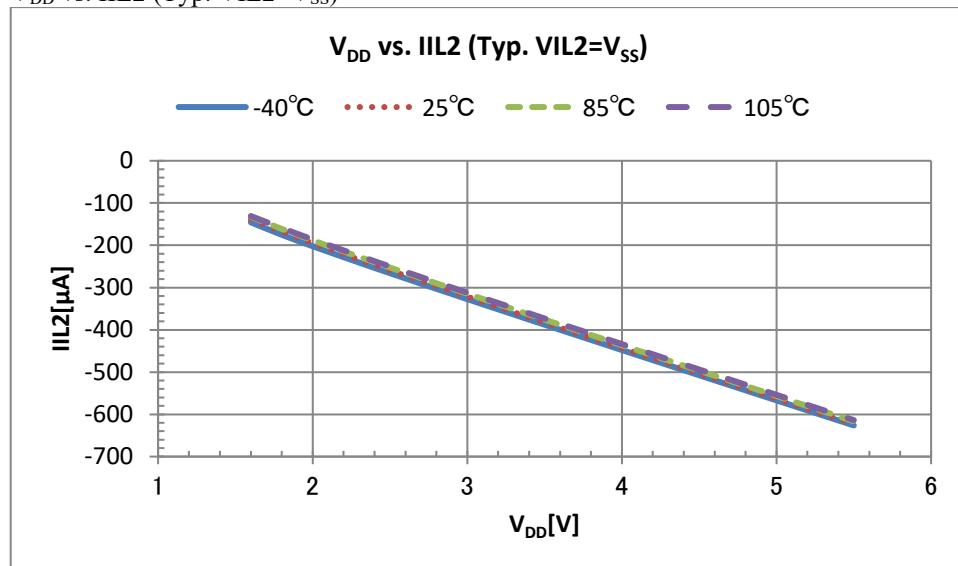
IOL vs. VOL2 ($V_{DD}=5V$ Typ.)



IOL vs. VOL2 ($V_{DD}=3V$ Typ.).

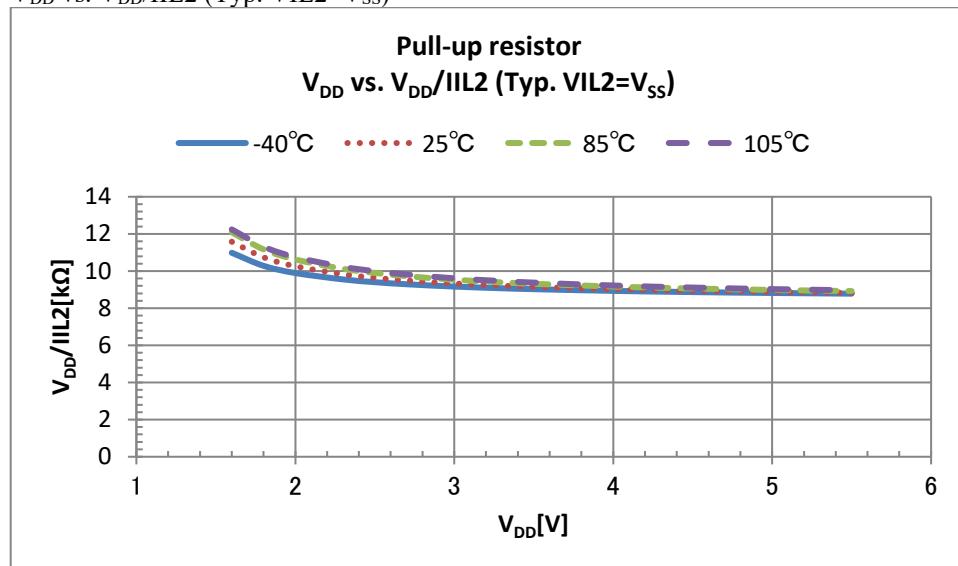


V_{DD} vs. IIL2 (Typ. $V_{IL2}=V_{SS}$)

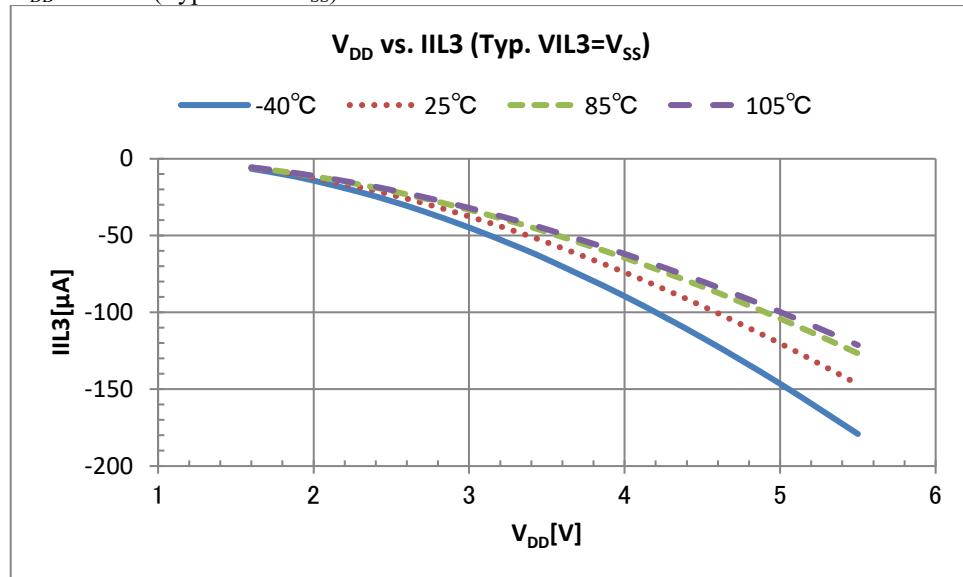


Pull-up resistor

V_{DD} vs. $V_{DD}/IIL2$ (Typ. $V_{IL2}=V_{SS}$)

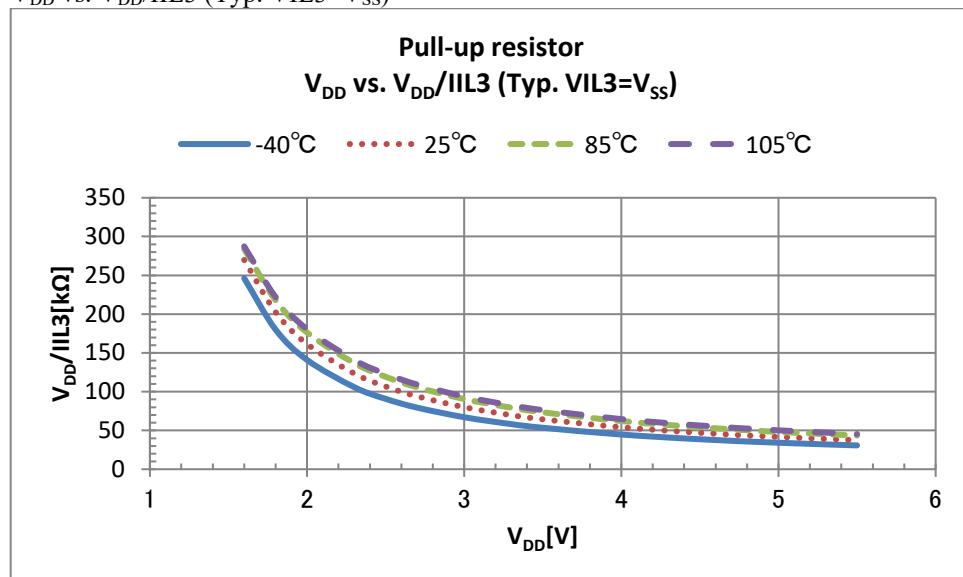


V_{DD} vs. IIL3 (Typ. $V_{IL3}=V_{SS}$)



Pull-up resistor

V_{DD} vs. $V_{DD}/IIL3$ (Typ. $V_{IL3}=V_{SS}$)



Product: ML62Q1323, ML62Q1324, ML62Q1325, ML62Q1333, ML62Q1334, ML62Q1335

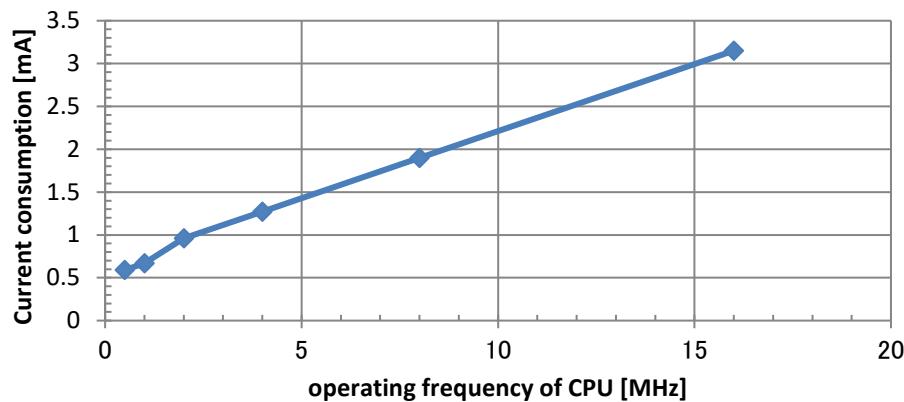
Current consumption vs. operating frequency of CPU

 $V_{DD}=3V$, temp.= 25°C PLL 16MHz Wait mode (Typ.)

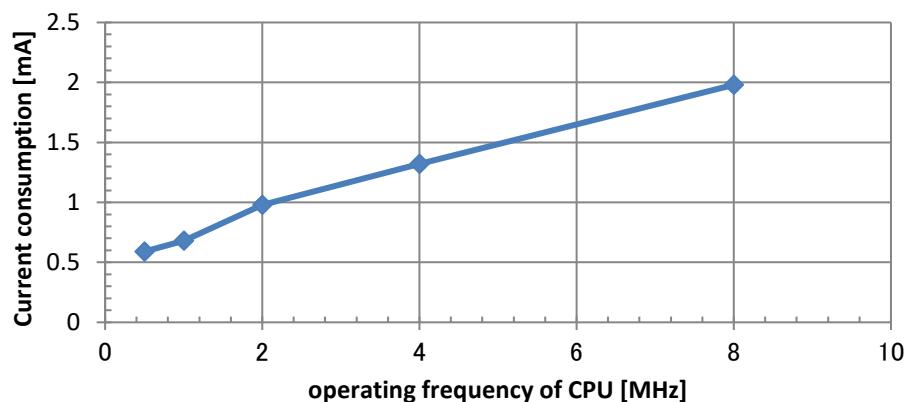
Stop the clock supply to peripherals.

Current consumption vs. operating frequency of CPU $V_{DD}=3V$, temp.= 25°C PLL 16MHz Wait mode (Typ.)

Stop the clock supply to peripherals.

 $V_{DD}=3V$, temp.= 25°C PLL 16MHz no Wait mode (Typ.)**Current consumption vs. operating frequency of CPU** $V_{DD}=3V$, temp.= 25°C PLL 16MHz no Wait mode (Typ.)

Stop the clock supply to peripherals.



Product: ML62Q1323, ML62Q1324, ML62Q1325, ML62Q1333, ML62Q1334, ML62Q1335

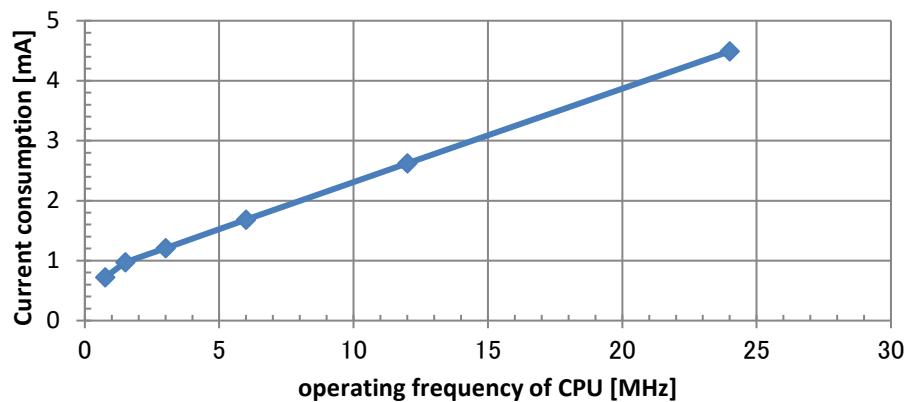
Current consumption vs operating frequency of CPU

 $V_{DD}=3V$, temp.= 25°C PLL 24MHz Wait mode (Typ.)

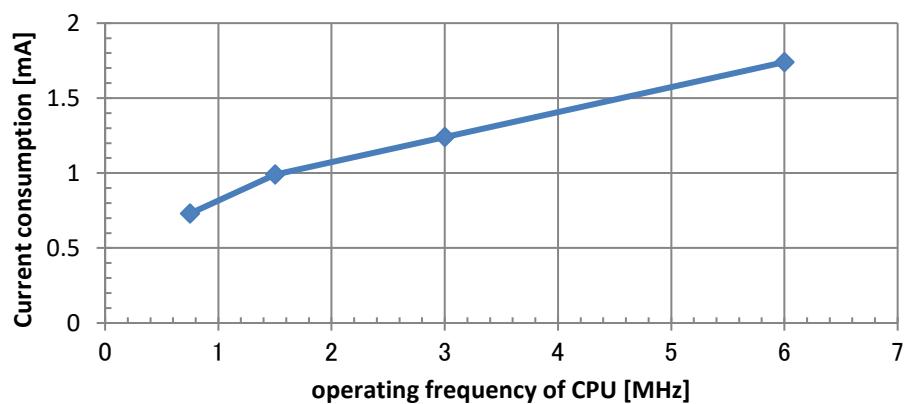
Stop the clock supply to peripherals.

Current consumption vs. operating frequency of CPU $V_{DD}=3V$, temp.= 25°C PLL 24MHz Wait mode (Typ.)

Stop the clock supply to peripherals.

 $V_{DD}=3V$, temp.= 25°C PLL 24MHz no Wait mode (Typ.)**Current consumption vs. operating frequency of CPU** $V_{DD}=3V$, temp.= 25°C PLL 24MHz no Wait mode (Typ.)

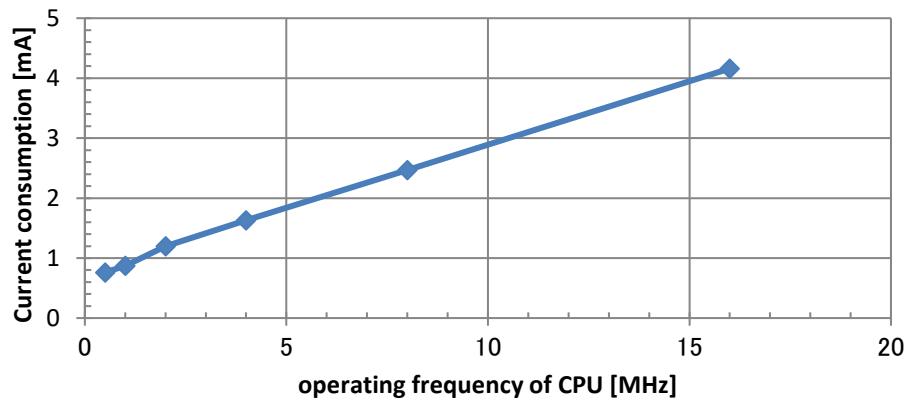
Stop the clock supply to peripherals.



Product: ML62Q1345, ML62Q1346, ML62Q1347, ML62Q1365, ML62Q1366, ML62Q1367

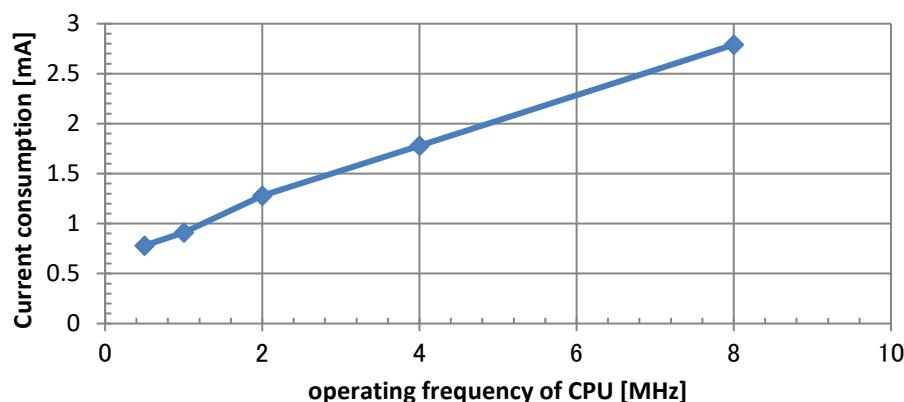
Current consumption vs. operating frequency of CPU
 $V_{DD}=3V$, temp.= 25°C PLL 16MHz Wait mode (Typ.)
Stop the clock supply to peripherals.

Current consumption vs. operating frequency of CPU
 $V_{DD}=3V$, temp.= 25°C PLL 16MHz Wait mode (Typ.)
Stop the clock supply to peripherals.



$V_{DD}=3V$, temp.= 25°C PLL 16MHz no Wait mode (Typ.)

Current consumption vs. operating frequency of CPU
 $V_{DD}=3V$, temp.= 25°C PLL 16MHz no Wait mode (Typ.)
Stop the clock supply to peripherals.

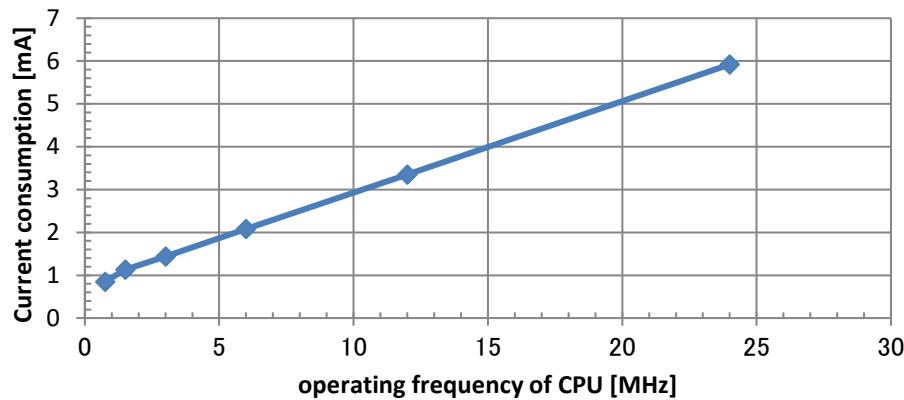
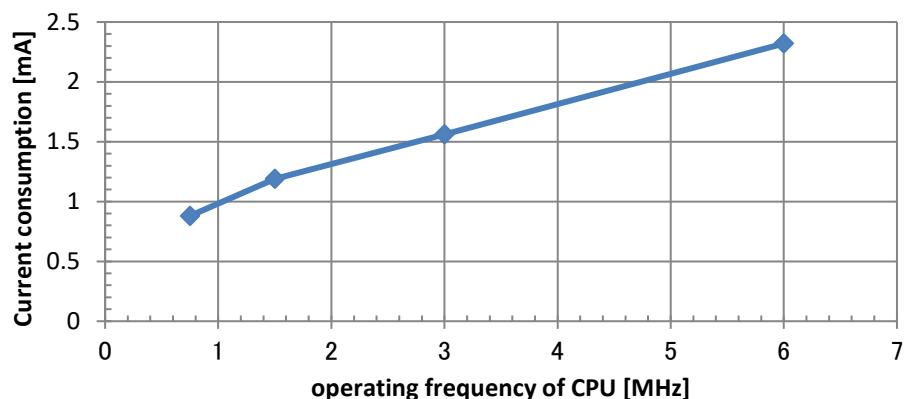


Product: ML62Q1345, ML62Q1346, ML62Q1347, ML62Q1365, ML62Q1366, ML62Q1367

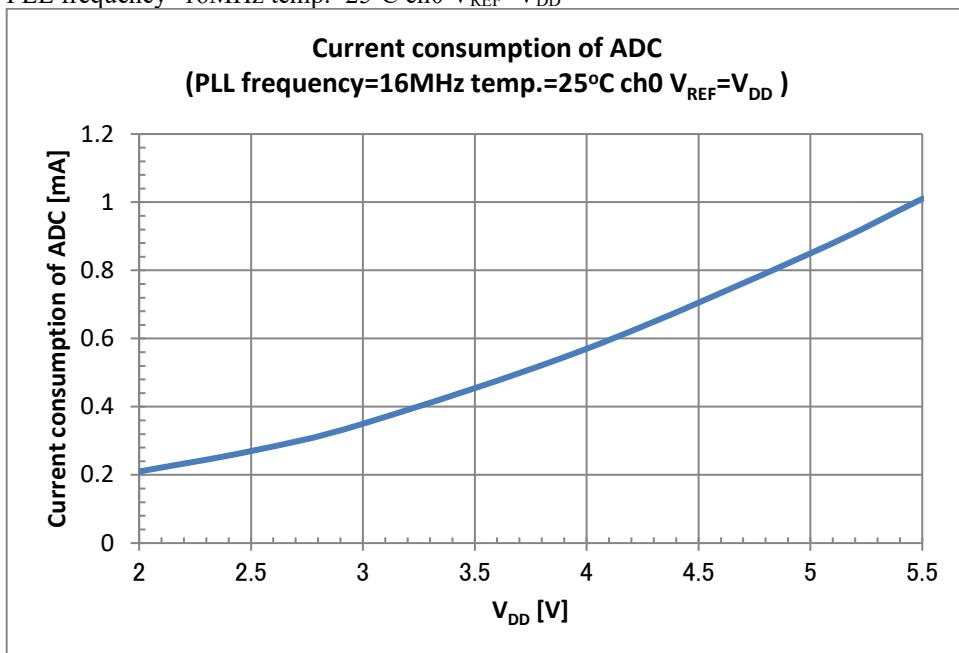
Current consumption vs operating frequency of CPU

V_{DD}=3V, temp.=25°C PLL 24MHz Wait mode (Typ.)

Stop the clock supply to peripherals.

Current consumption vs. operating frequency of CPU**V_{DD}=3V, temp.=25°C PLL 24MHz Wait mode (Typ.)****Stop the clock supply to peripherals.**V_{DD}=3V, temp=25 °C PLL 24MHz no Wait mode (Typ.)**Current consumption vs. operating frequency of CPU****V_{DD}=3V, temp.=25°C PLL 24MHz no Wait mode (Typ.)****Stop the clock supply to peripherals.**

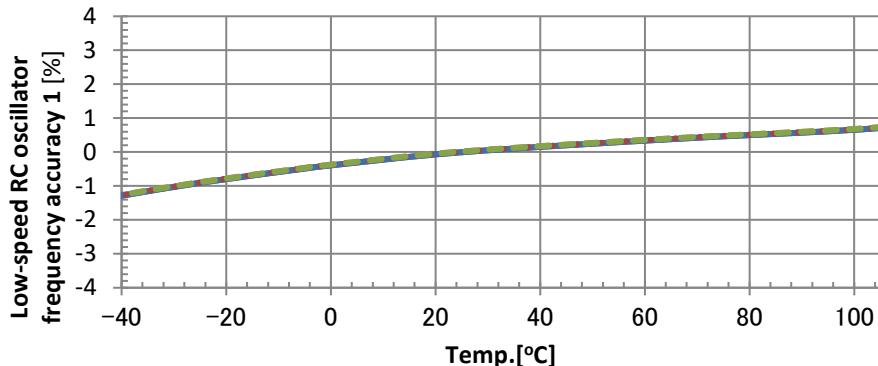
Current consumption of ADC vs. operating voltage
PLL frequency=16MHz temp.=25°C ch0 V_{REF}=V_{DD}



Temp. vs. Low-speed RC oscillator frequency accuracy 1
without software adjustment (Typ.)

**Low-speed RC oscillator frequency accuracy 1
without software adjustment (Typ.)**

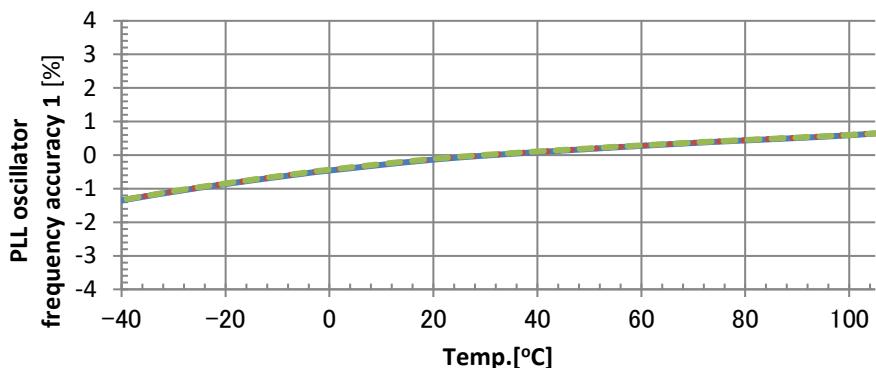
— VDD=1.8V ····· VDD=3V - - - VDD=5.5V



Temp. vs. PLL oscillator frequency accuracy 1
without software adjustment (24MHz Typ.)

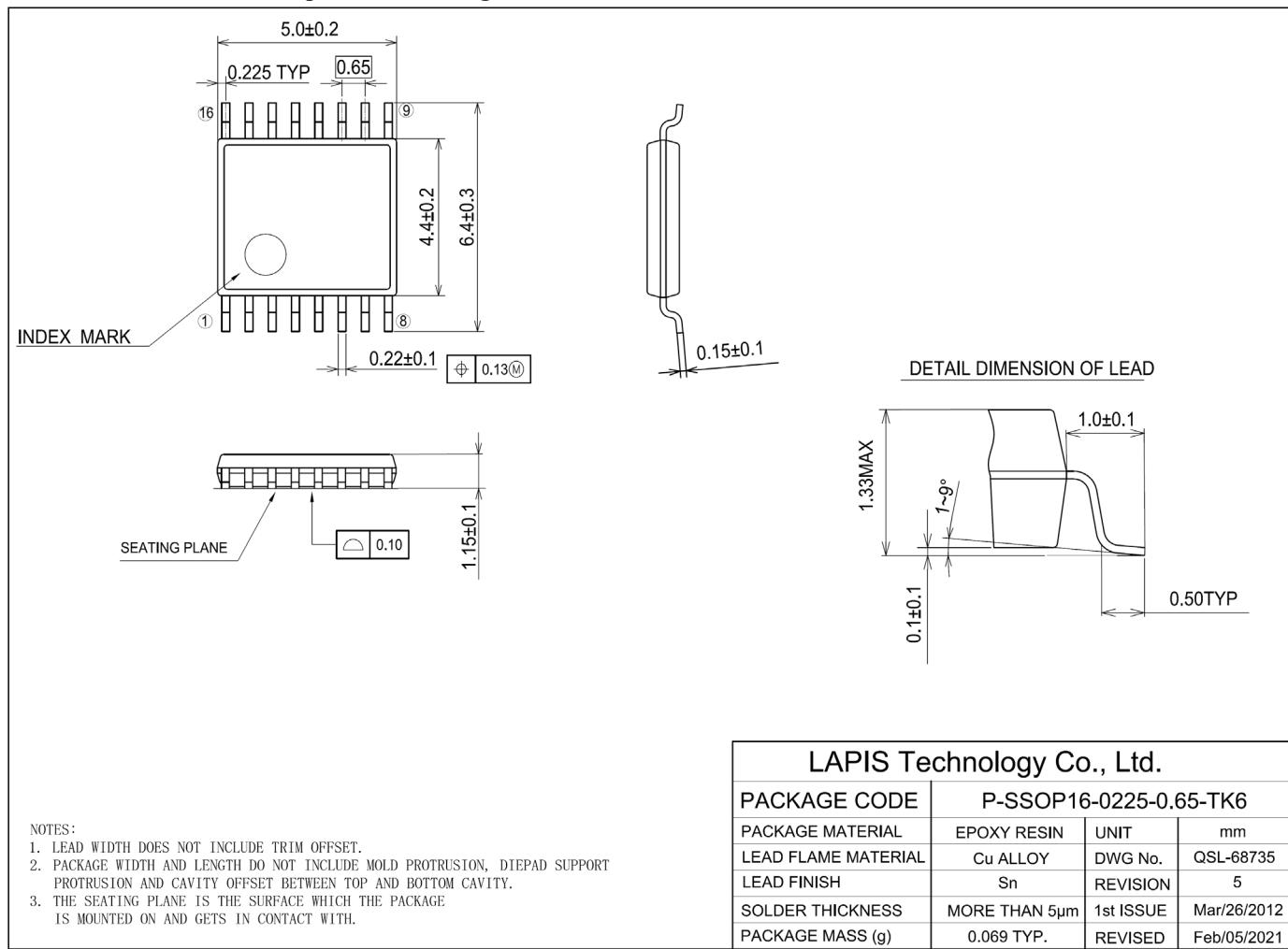
**PLL oscillator frequency accuracy 1
without software adjustment (24MHz Typ.)**

— VDD=1.8V ····· VDD=3V - - - VDD=5.5V



PACKAGE DIMENSIONS

ML62Q1323/1324/1325 16pin SSOP Package

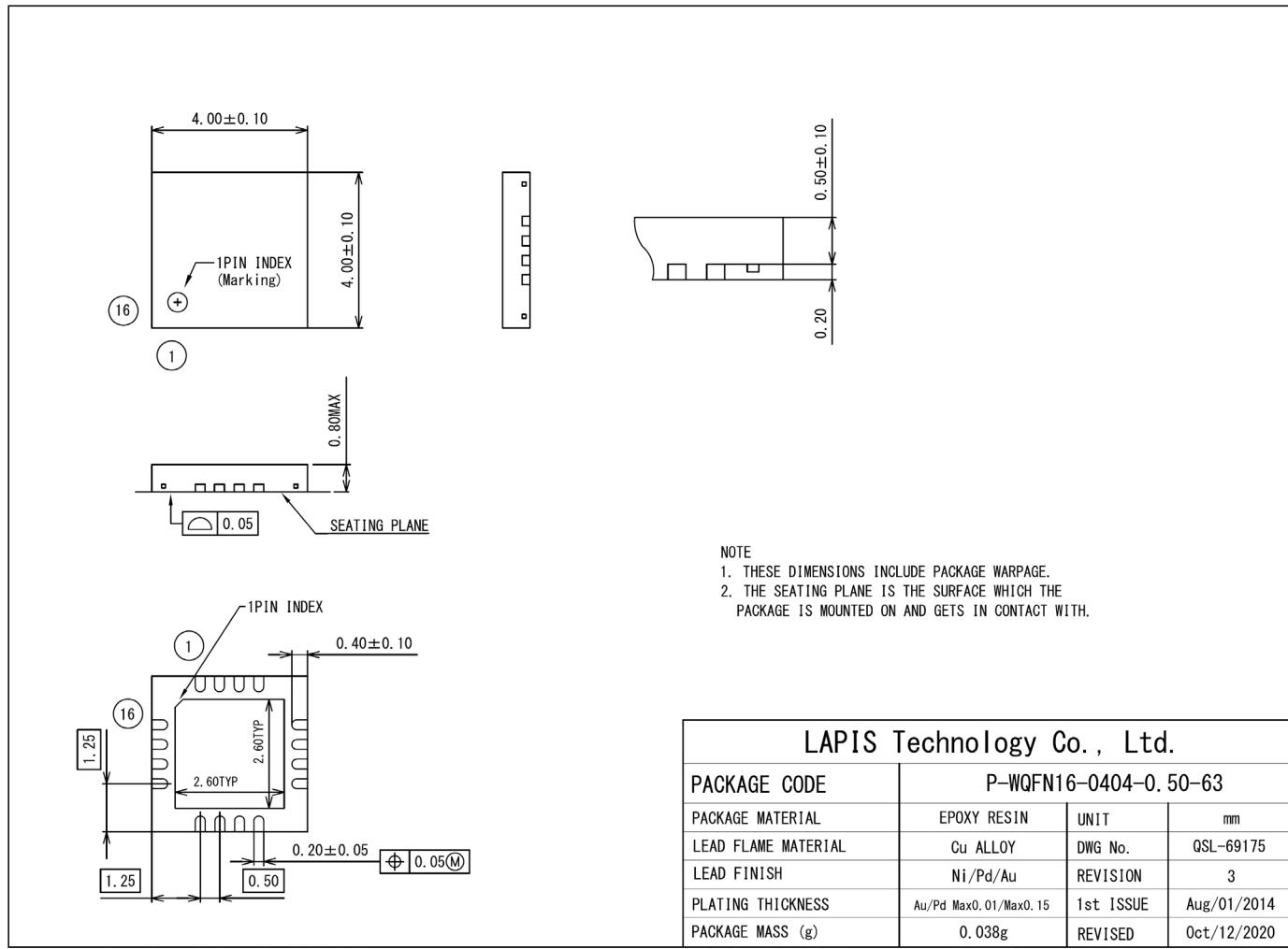


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1323/1324/1325 16pin WQFN Package



(Unit: mm)

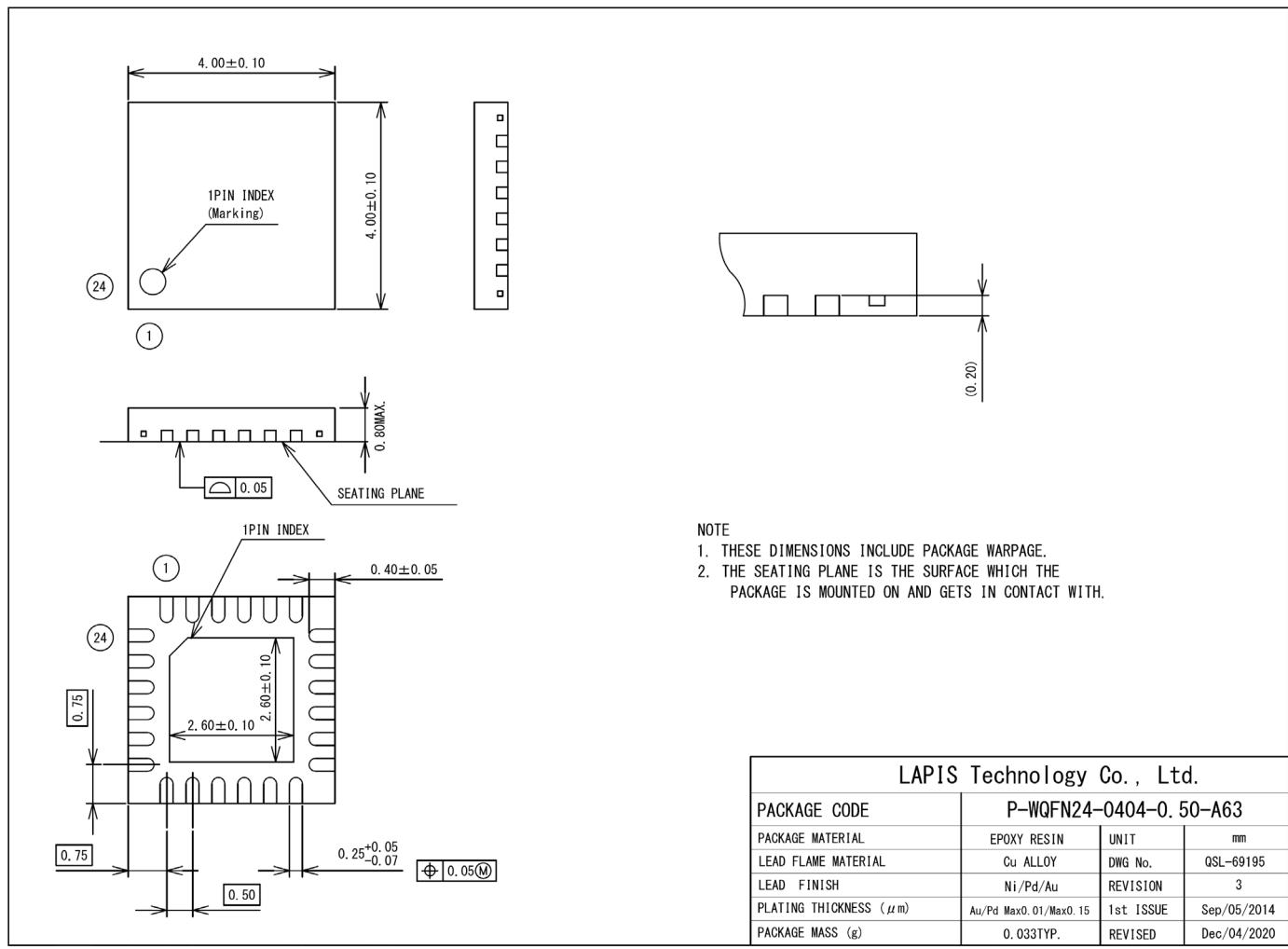
Notes for Mounting the Surface Mount Type Package

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Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

ML62Q1345/1346/1347 24pin WQFN Package



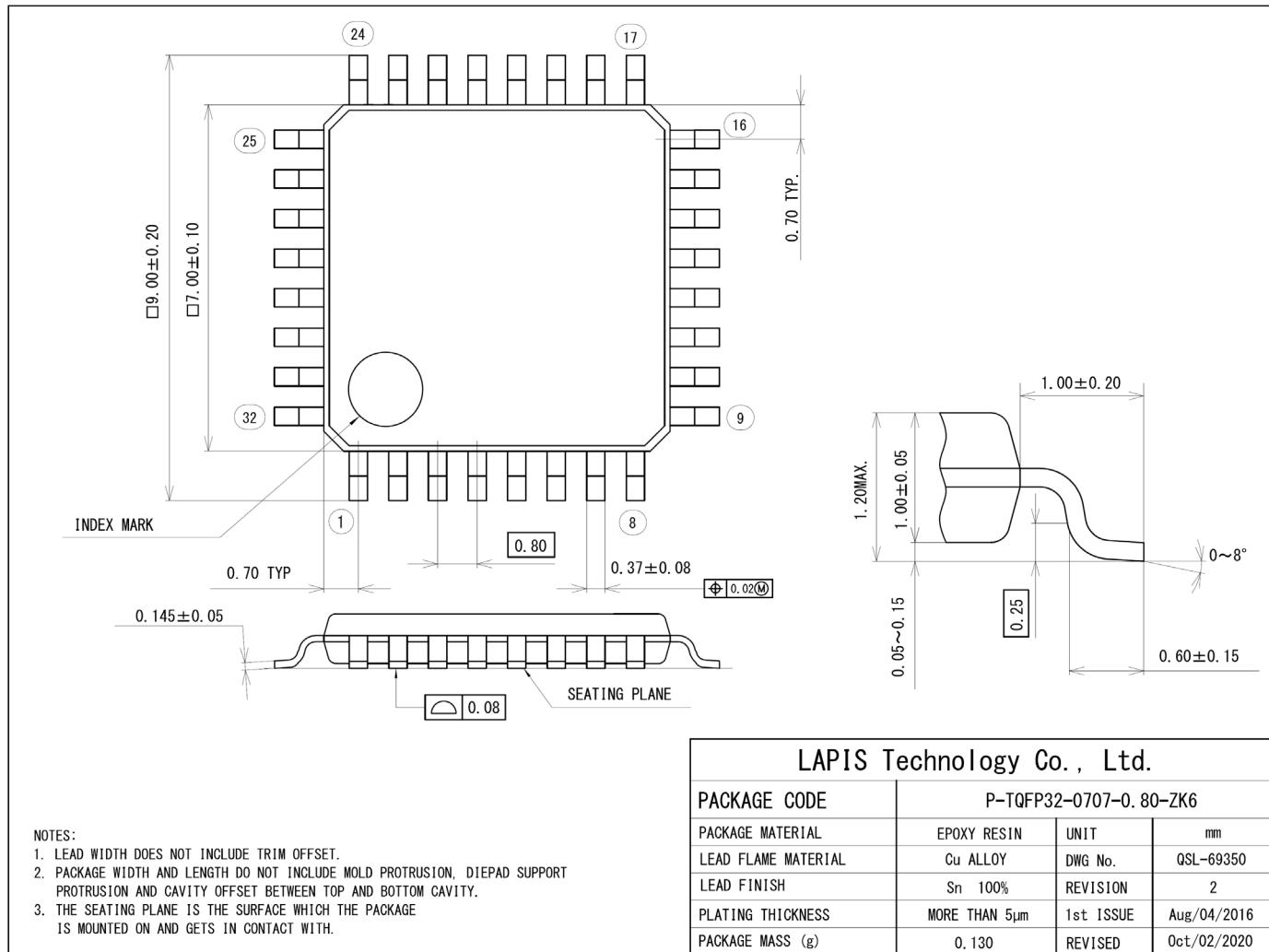
Notes for Mounting the Surface Mount Type Package

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Note for the package with exposed die pad

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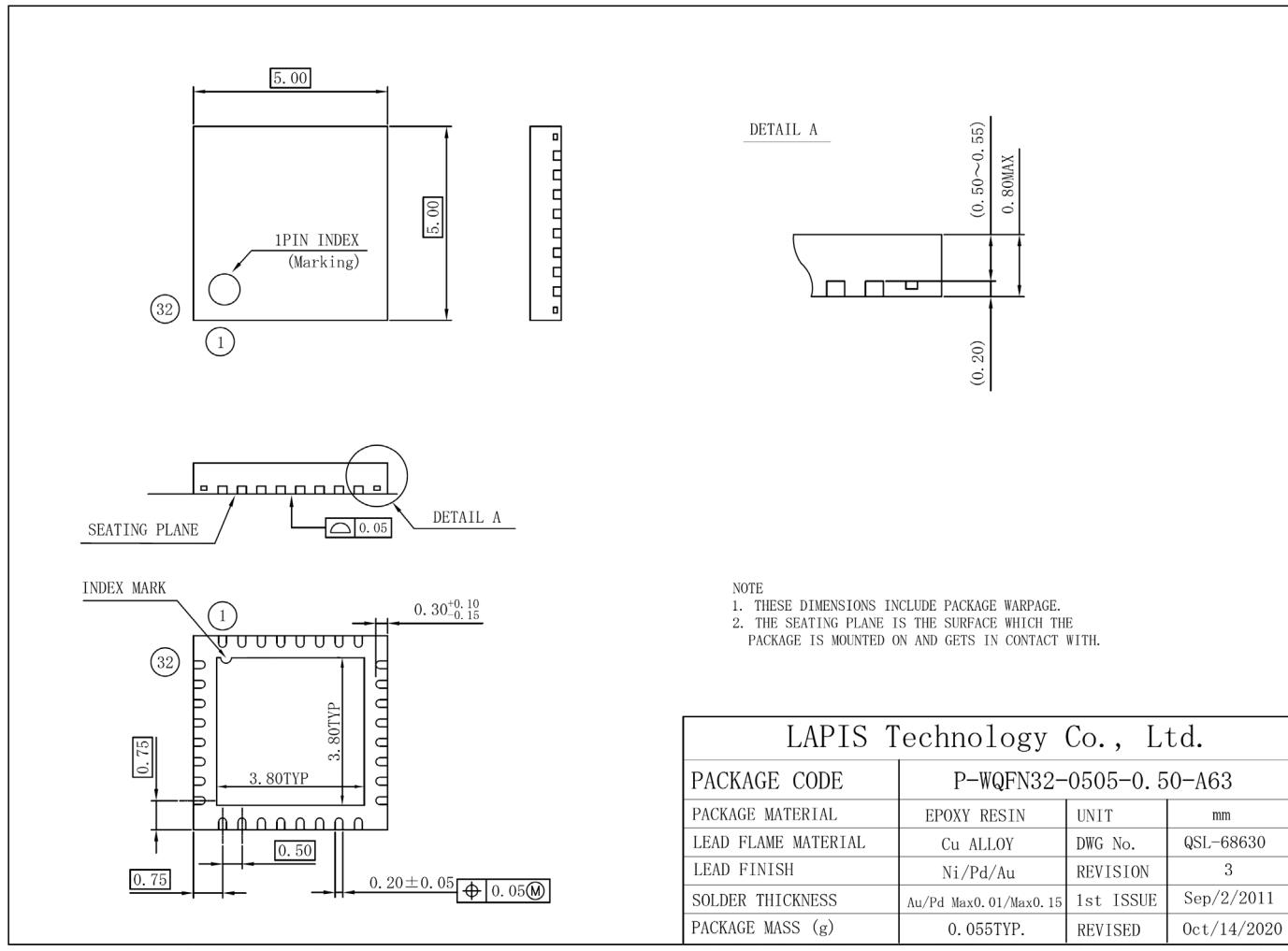
ML62Q1365/1366/1367 32pin TQFP Package



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1365/1366/1367 32pin WQFN Package



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL62Q1300-01	Nov 15, 2018	-	-	1 st Revision.
FEDL62Q1300-02	Sep 27, 2019	1	1	Changed the products status (Table 1 ML62Q1300 Group Product List)
		-	23	Added Current Consumption 1
		26	27	Added comment “*6” to the IOHL.
		46	49	Updated 24MHz Characteristics graph
		-	46,47	Added ML62Q1323/ML62Q1324/ML62Q1325/ML62Q1333/ML62Q1334/ML62Q1335 Current consumption VS operating frequency of CPU
		*	*	Correction of errors
FEDL62Q1300-03	Mar 25, 2020	21	21	Changed termination of unused pins
		22	22	Added parameter “Operating temperature(Chip-Junction)” in Recommended Operating Conditions
		—	23	Added thermal characteristics section
		34	35	Added comments and notes to the reset characteristics
		34	36	Revised overall of “Power On Reset” section as “Slope of Power supply and Power On Reset” section. The major revisions are Added definitions of Power on rising/falling slope, Power on voltage, CPU operation start time, and added Note.
		*	*	Corrected typo
FEDL62Q1300-04	Nov 15, 2020	4,8,9	4,8,9	Changed comment for UART.
		22	22	Corrected the operating temperature (Chip-Junction).
FEDL62Q1300-05	May 19, 2022	-	-	Changed company name
		—	1,6,12,16 ,23,57	Add SSOP20
		1	1	Added Notes in general description section.
		—	62	Added Notes for product usage
		—	—	Corrected Typo
FEDL62Q1300-06	Jun 14, 2023	1,6,12,16 ,23, 56	1,6,12,16 ,23 ,56	Deleted SSOP20 information
		54-60	54-60	Revised the package outline
FEDL62Q1300-07	Mar 26, 2024	1	1	Added application information
		6	6	Changed the format of the shipping package information Corrected WQFN part number
		7	7	Updated “how to read the part number”
		61	61	Revised the Note

Notes for product usage

Notes on this page are applicable to the all microcontroller products.

For individual notes on each LAPISTechnology microcontroller product, refer to [Note] in the chapters of each user's manual.

The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS

Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON

At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.

On LAPISTechnology microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.

Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY

If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCTS

Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.

When replacing from other product to LAPISTechnology microcontroller products, please evaluate enough the apparatus/system which implemented LAPISTechnology microcontroller products.

5. USE ENVIRONMENT

When using this product in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

Notes

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