Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL610Q339-01
Issue Date: Apr. 18, 2022

ML610Q327/38/39

8-bit Microcontroller with Voice Output Function

GENERAL DESCRIPTION

Equipped with a 8-bit CPU nX-U8/100, the ML610Q327/338/339 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as timer, PWM, UART, I^2C bus interface, synchronous serial port, successive approximation type 10-bit A/D converter and voice output function. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture. The ML610Q327/338/339 is also equipped with a flash memory* that has achieved low voltage and low power consumption (at read) equivalent to mask ROM, so it is best suited to battery-driven applications such as alarm and portable devices. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

*: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.
SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.

This product consists of seven varieties of LSI whose package and flash memory size are different each other.
LSI list of this product which has 48pin to 64pin and 192Kbyte[*1] to 256Kbyte[*1] in the lineup is shown below.

LSI List of This Product

Flash memory (Program area), Estimated audio playback time	The number of pins, Package, Product name		
	48pin TQFP48	52pin TQFP52	64pin TQFP64
256Kbyte[*1], 95s[*2]	—	ML610Q338	ML610Q339
192Kbyte[*1], 69s[*2]	ML610Q327	—	—

[*1]: Including unusable 1Kbyte test data area
[*2]: In case 16Kbyte is used for control program, 6.4kHz sampling frequency and HQ-ADPCM are selected

Please see last 2 pages; “Notes for product usage” and “Notes” in this document on use with this production.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    Approx 30.5 µs (@32.768kHz system clock)
    Approx 0.244 µs (@4.096 MHz system clock)@V_{DD}=2.0 to 5.5V
    Approx 0.122 µs (@8.192 MHz system clock)@V_{DD}=2.2 to 5.5V

•Internal memory
- Flash-memory (Program area)

Product	Program area	Rewrite cycle
ML610Q327	192Kbyte (96K×16bits)*3	100 times
ML610Q338/ML610Q339	256Kbyte (128K×16bits)*3	

*3: Including unusable 1Kbyte test data area

- Data Flash memory: 2Kbyte (1K×16 bits) Rewrite cycle: 10,000 times
  Built into Back Ground Operation (BGO) function (CPU continues program processing while the data flash erase/write)
- Internal RAM : 4Kbyte (4K × 8 bits)

•Interrupt controller
- 1 non-maskable interrupt source
  Internal source: 1(Watchdog timer)
- 29 maskable interrupt sources
  Internal source: 21(Data flash erase/write completion, SSIO0, SSIO1, UART0, UART1, I^2C bus master/slave interface, Timer 0, Timer 1, Timer 2, Timer 3, PWM0, PWM1, PWM2, A/D converter, Voice sound reproduction, Speaker pin short detection, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
  External source: 8(P80, P81, P82, P83, P84, P85, P86, P87)

•Time base counter
- Low-speed time base counter × 1 channel
- High-speed time base counter × 1 channel

•Watchdog timer
- Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
- Free running
- Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s at 32.768kHz)

•Timers
- 8 bits × 4ch (16-bit configuration available)

•PWM
- Resolution 16 bits × 3ch

•Voice output function
- Voice synthesis method: HQ-ADPCM / 4-bit ADPCM2 / non-linear 8-bit PCM / straight 8-bit PCM / straight 16-bit PCM
- Sampling frequency: 6.4kHz, 8kHz, 10.7kHz, 12.8kHz, 16kHz, 21.3 kHz, 25.6 kHz, 32 kHz

Ky's Technology

HQ-ADPCM is audio compression technology featuring high-quality sound. It was developed by “Ky’s”.
“Ky’s” is a registered trademark of Kyushu Institute of Technology, one of the national universities in Japan.

- Successive approximation type A/D converter
  - 10-bit A/D converter
  - Input: 8ch
  - Conversion time: 24.4 μs per channel at 4.096MHz V_{DD}≥2.2V
  - Conversion time: 12.2 μs per channel at 8.192MHz V_{DD}≥2.5V
  - Continuous conversion / Single conversion selectable

- Synchronous serial port (SSIO)
  - 2ch
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - Half-duplex × 2ch (A full-duplex is also possible by using 2 channels)
  - TXD/RXD
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function: standard mode (100 kbps) and Fast mode (400 kbps)
  - Slave function: standard mode (100 kbps) and Fast mode (400 kbps)

- General-purpose ports
  - Output-only port × 6ch (Including secondary functions)
  - Input/output port (Including secondary functions)

Product	Input/output ports (Including secondary functions)
ML610Q327	26ch
ML610Q338	30ch
ML610Q339	42ch

- Speaker amplifier(D-class) output power
  - 1.0W(at 5.0V)/0.45W(at 3.0V)
  - Disconnection detection circuit
  - Speaker pin short detection circuit

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - PLL oscillation stop detection reset
  - Low level detection (LLD) reset

- Clock
  - Low-speed clock
    Built-in RC oscillation (32.768 kHz)
  - High-speed clock
    Built-in PLL oscillation (Approx. 1.024MHz / 2.048MHz / 4.096MHz / 8.192MHz)

- Power management
  - STOP mode: Stop of oscillation (Operations of CPU and peripheral circuits are stopped.)
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/2, 1/4, 1/8, or 1/16 of the oscillation clock)
  - Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

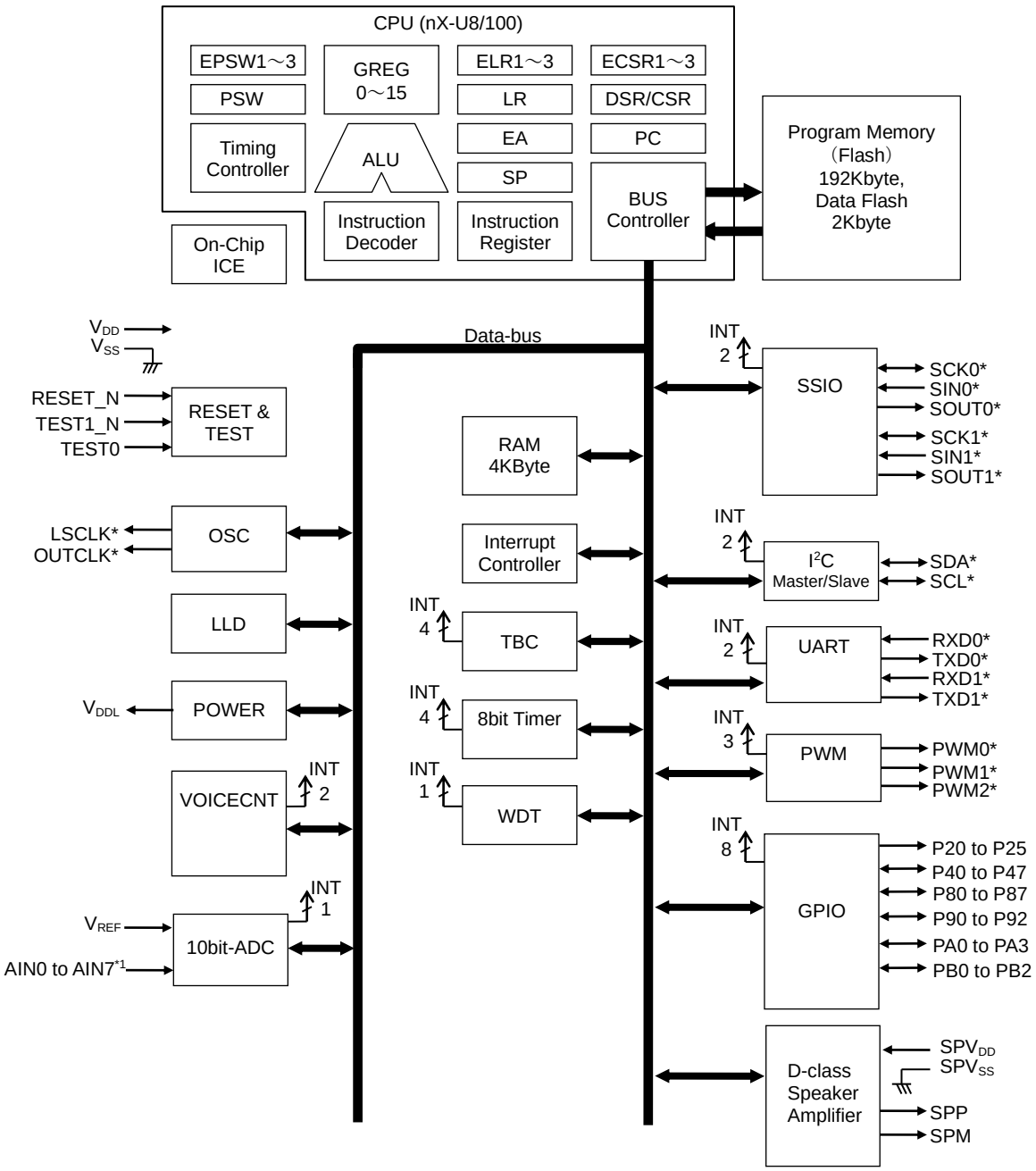
- Shipment

Product	Shipment
ML610Q327	48pin TQFP (P-TQFP48-0707-0.50-ZK6)
ML610Q338	52pin TQFP (P-TQFP52-1010-0.65-ZK6)
ML610Q339	64pin TQFP (P-TQFP64-1010-0.50-ZK6)

- Guaranteed operating range
  - Operating temperature: –40°C to 85°C
  - Operating voltage: V_{DD} = 2.0V to 5.5V, SPV_{DD} = 2.0V to 5.5V

BLOCK DIAGRAM

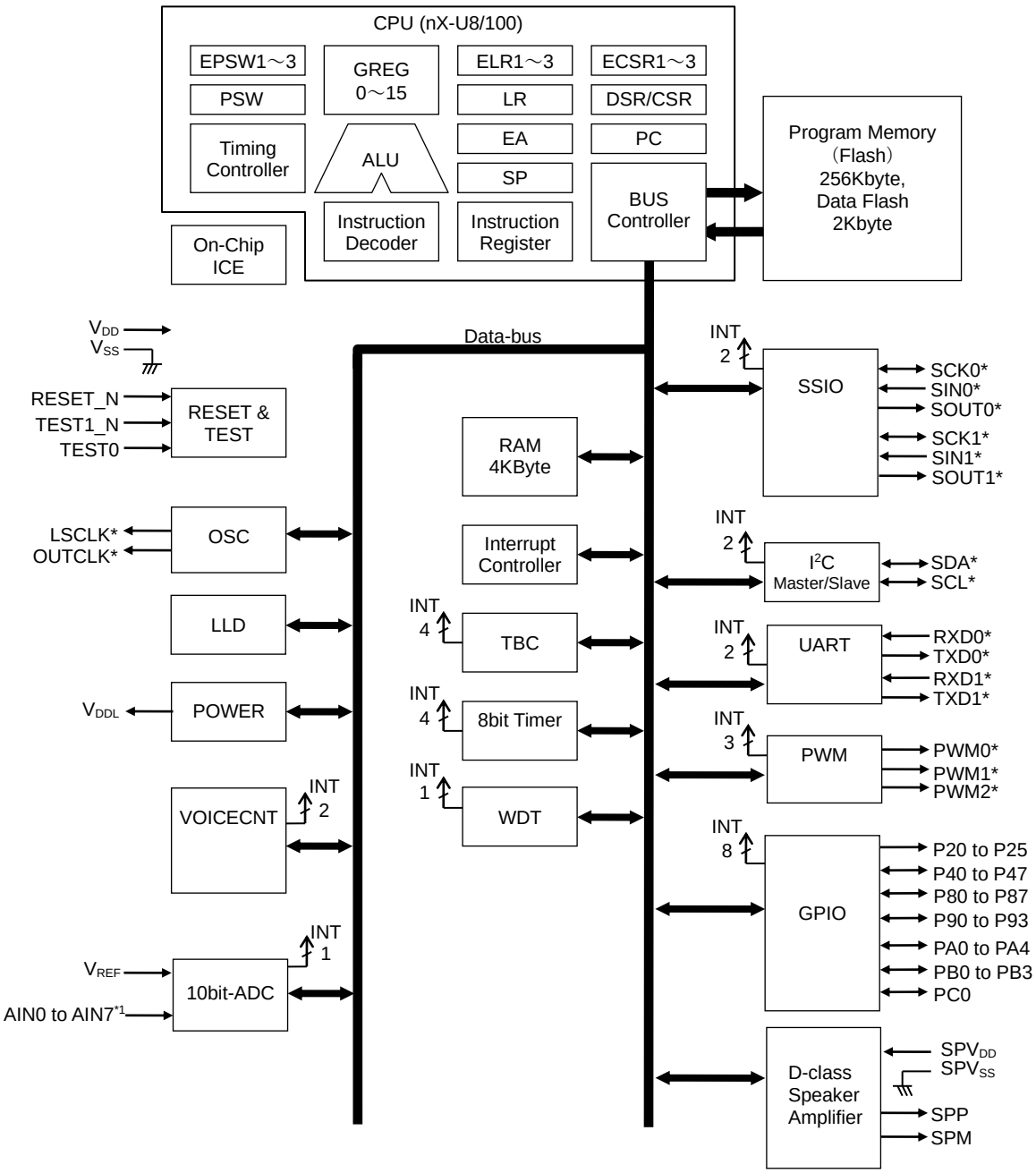
Block Diagram of ML610Q327



* : Secondary or tertiary function
*1: Select I/O port or A/D converter input terminal

Block Diagram of ML610Q327

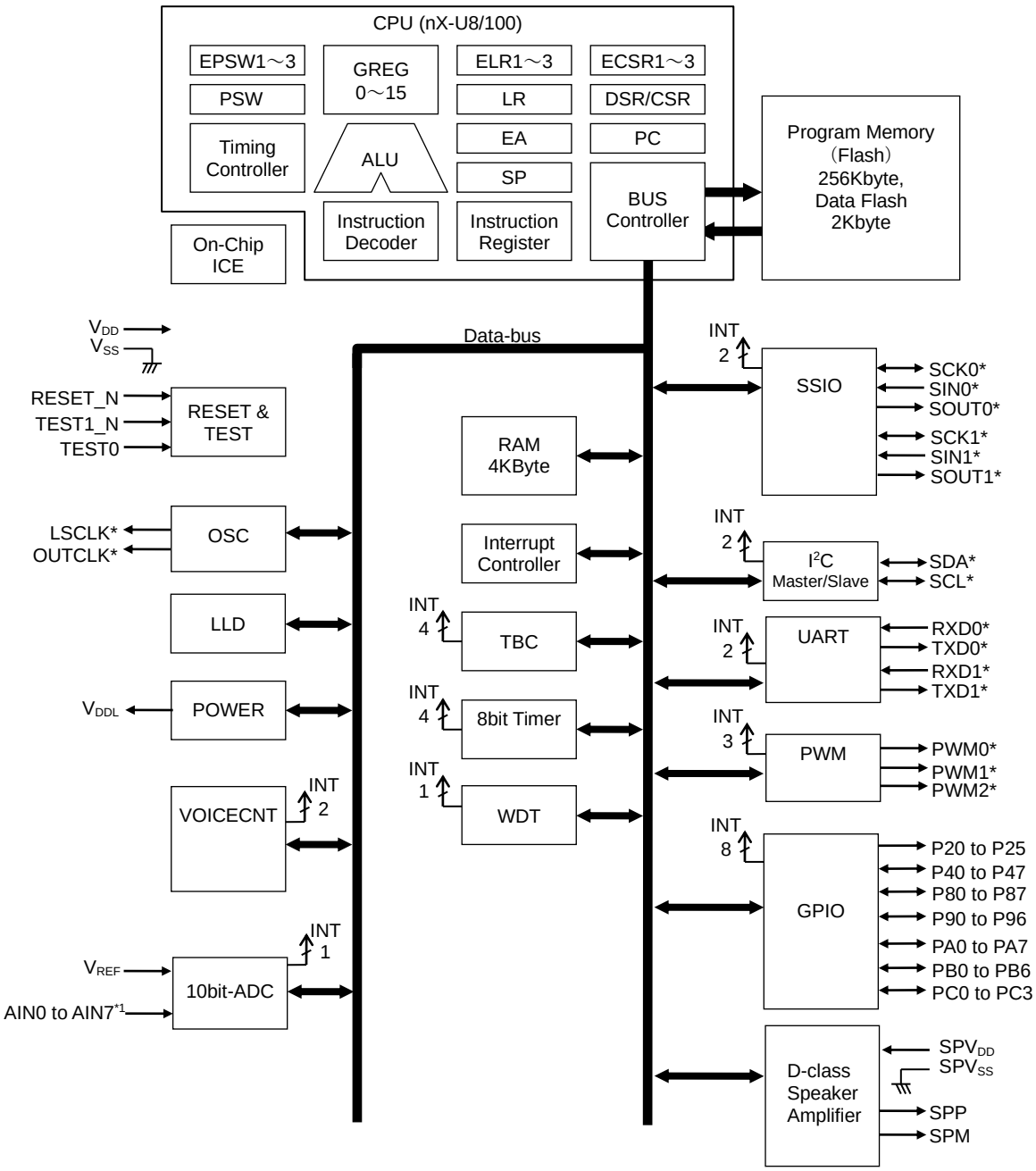
Block Diagram of ML610Q338



* : Secondary or tertiary function
*1: Select I/O port or A/D converter input terminal

Block Diagram of ML610Q338

Block Diagram of ML610Q339

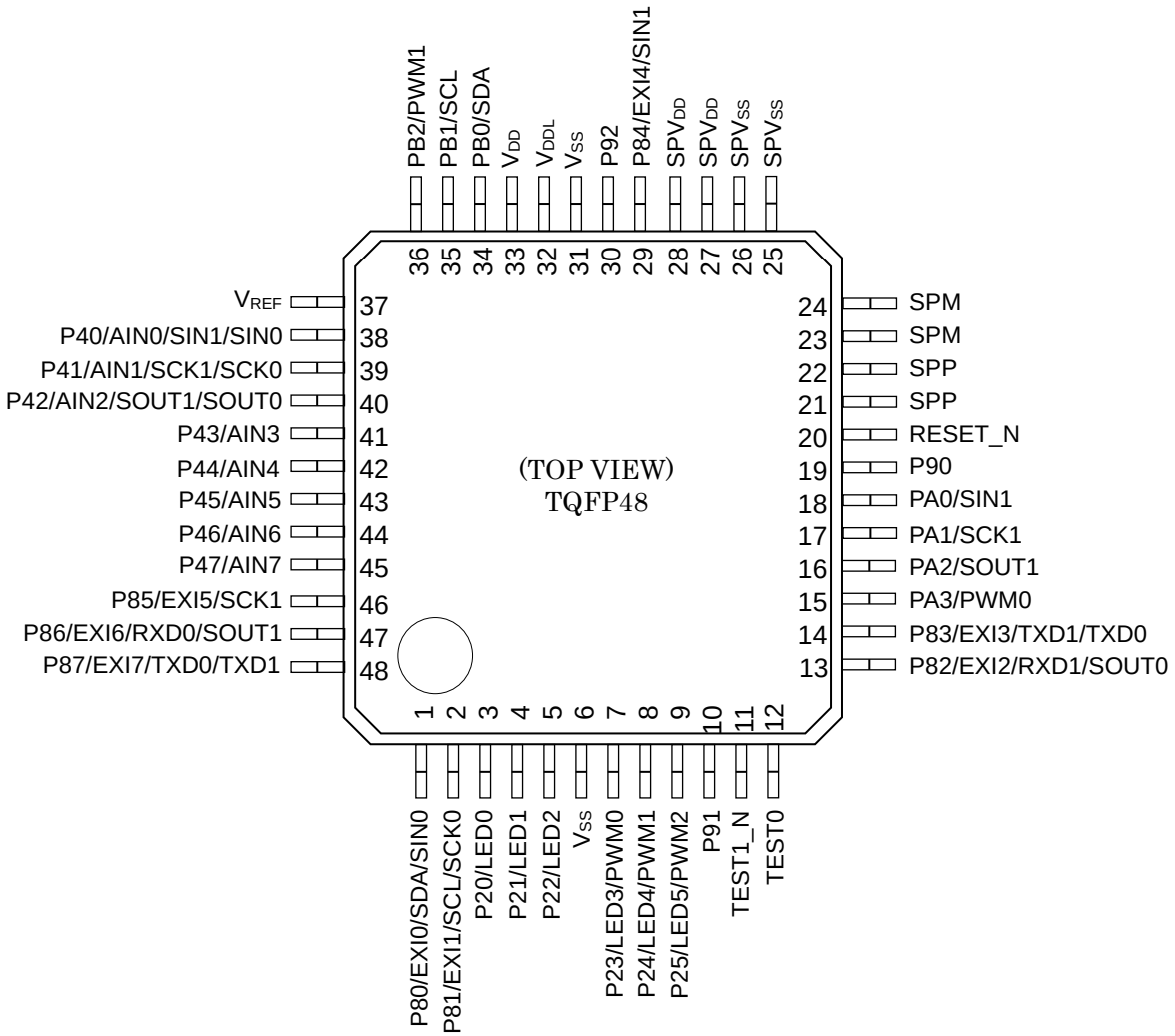


*: Secondary or tertiary function
*1: Select I/O port or A/D converter input terminal

Block Diagram of ML610Q339

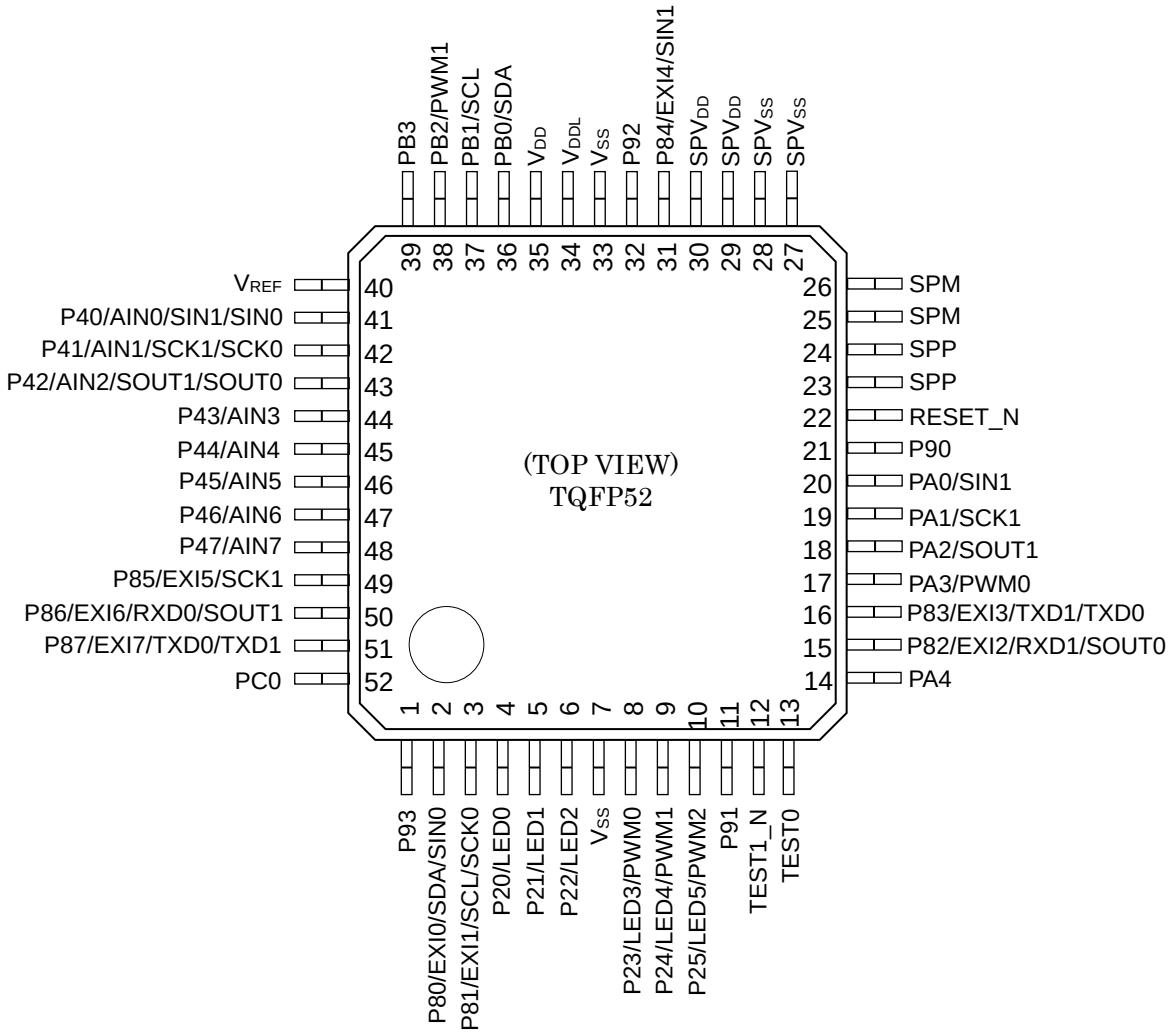
PIN CONFIGURATION

Pin Layout of ML610Q327 48pin TQFP Package



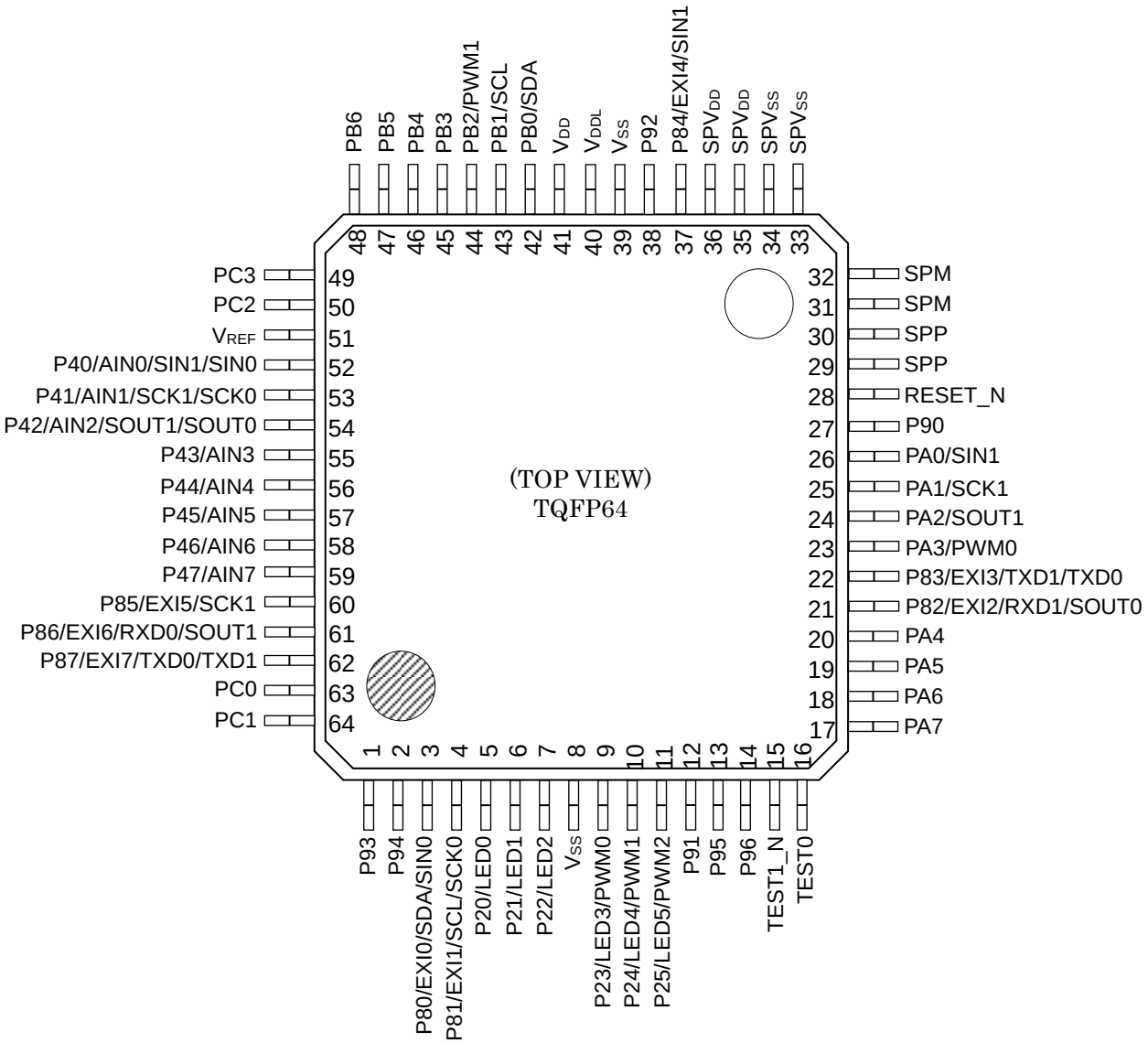
Pin Layout of ML610Q327 48pin TQFP Package

Pin Layout of ML610Q338 52pin TQFP Package



Pin Layout of ML610Q338 52pin TQFP Package

Pin Layout of ML610Q339 64pin TQFP Package



Pin Layout of ML610Q339 64pin TQFP Package

LIST OF PINS

In the I/O column, "—" denotes a power pin, "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	Desc-ription	Pin name	I/O	Desc-ription	Pin name	I/O	Desc-ription
21, 22	23, 24	29, 30	SPP	O	Positive output pin of the built-in speaker amplifier	—	—	—	—	—	—	—	—	—
23, 24	25, 26	31, 32	SPM	O	Negative output pin of the built-in speaker	—	—	—	—	—	—	—	—	—
25, 26	27, 28	33, 34	SPVss	—	Negative power supply pin for built-in speaker amplifier	—	—	—	—	—	—	—	—	—
27, 28	29, 30	35, 36	SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—	—	—	—	—	—	—	—
6, 31	7, 33	8, 39	V_{SS}	—	Negative power supply pin	—	—	—	—	—	—	—	—	—
32	34	40	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—	—	—	—
33	35	41	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—	—	—	—
37	40	51	V_{REF}	—	Reference power supply pin for successive-approximation type ADC	—	—	—	—	—	—	—	—	—
20	22	28	RESET_N	I	Reset input pin	—	—	—	—	—	—	—	—	—
12	13	16	TEST0	I/O	Input/output pin for testing	—	—	—	—	—	—	—	—	—
11	12	15	TEST1_N	I	Input pin for testing	—	—	—	—	—	—	—	—	—
3	4	5	P20/LED0	O	Output port / LED port	LSCLK	O	Low-speed clock output	—	—	—	—	—	—
4	5	6	P21/LED1	O	Output port / LED port	OUTCLK	O	high-speed clock output	—	—	—	—	—	—
5	6	7	P22/LED2	O	Output port / LED port	—	—	—	—	—	—	—	—	—
7	8	9	P23/LED3	O	Output port / LED port	PWM0	O	PWM0 output	—	—	—	—	—	—
8	9	10	P24/LED4	O	Output port / LED port	PWM1	O	PWM1 output	—	—	—	—	—	—
9	10	11	P25/LED5	O	Output port / LED port	PWM2	O	PWM2 output	—	—	—	—	—	—
38	41	52	P40/AIN0	I/O	Input port/Output port /Successive-approximation type ADC input0	SIN1	I	SSIO1 data input	SIN0	I	SSIO0 data input	—	—	—
39	42	53	P41/AIN1	I/O	Input port/Output port /Successive-approximation type ADC input1	SCK1	I/O	SSIO1 clock input/output	SCK0	I/O	SSIO0 clock input/output	—	—	—
40	43	54	P42/AIN2	I/O	Input port/Output port /Successive-approximation type ADC input2	SOUT1	O	SSIO1 data output	SOUT0	O	SSIO0 data output	—	—	—
41	44	55	P43/AIN3	I/O	Input port/Output port /Successive-approximation type ADC input3	—	—	—	—	—	—	—	—	—
42	45	56	P44/AIN4	I/O	Input port/Output port /Successive-approximation type ADC input4	—	—	—	—	—	—	—	—	—
43	46	57	P45/AIN5	I/O	Input port/Output port /Successive-approximation type ADC input5	—	—	—	—	—	—	—	—	—
44	47	58	P46/AIN6	I/O	Input port/Output port /Successive-approximation type ADC input6	—	—	—	—	—	—	—	—	—

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	Desc-ription	Pin name	I/O	Desc-ription	Pin name	I/O	Desc-ription
45	48	59	P47/AIN7	I/O	Input port/Output port /Successive-approximation type ADC input7	—	—	—	—	—	—	—	—	—
1	2	3	P80/EXI0	I/O	Input port/Output port / External interrupt	SDA	I/O	I^2C data input/ output	SIN0	I	SSIO0 data input	—	—	—
2	3	4	P81/EXI1	I/O	Input port/Output port / External interrupt	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 clock input/output	—	—	—
13	15	21	P82/EXI2	I/O	Input port/Output port / External interrupt	RXD1	I	UART1 data input	SOUT0	O	SSIO0 data output	—	—	—
14	16	22	P83/EXI3	I/O	Input port/Output port / External interrupt	TXD1	O	UART1 data output	TXD0	O	UART0 data output	—	—	—
29	31	37	P84/EXI4	I/O	Input port/Output port / External interrupt	—	—	—	SIN1	I	SSIO1 data input	—	—	—
46	49	60	P85/EXI5	I/O	Input port/Output port / External interrupt	—	—	—	SCK1	I/O	SSIO1 clock input/output	—	—	—
47	50	61	P86/EXI6	I/O	Input port/Output port / External interrupt	RXD0	I	UART0 data input	SOUT1	O	SSIO1 data output	—	—	—
48	51	62	P87/EXI7	I/O	Input port/Output port / External interrupt	TXD0	O	UART0 data output	TXD1	O	UART1 data output	—	—	—
19	21	27	P90	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
10	11	12	P91	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
30	32	38	P92	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	1	1	P93	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	2	P94	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	13	P95	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	14	P96	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
18	20	26	PA0	I/O	Input port/Output port	SIN1	I	SSIO1 data input	—	—	—	—	—	—
17	19	25	PA1	I/O	Input port/Output port	SCK1	I/O	SSIO1 clock input/output	—	—	—	—	—	—
16	18	24	PA2	I/O	Input port/Output port	SOUT1	O	SSIO1 data output	—	—	—	—	—	—
15	17	23	PA3	I/O	Input port/Output port	PWM0	O	PWM0 output	—	—	—	—	—	—
—	14	20	PA4	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	19	PA5	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	18	PA6	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	17	PA7	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
34	36	42	PB0	I/O	Input port/Output port	SDA	I/O	I^2C data input/ output	—	—	—	—	—	—
35	37	43	PB1	I/O	Input port/Output port	SCL	I/O	I^2C clock input/output	—	—	—	—	—	—
36	38	44	PB2	I/O	Input port/Output port	PWM1	O	PWM1 output	—	—	—	—	—	—
—	39	45	PB3	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	46	PB4	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	47	PB5	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	48	PB6	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	52	63	PC0	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	64	PC1	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	50	PC2	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—
—	—	49	PC3	I/O	Input port/Output port	—	—	—	—	—	—	—	—	—

Note: The function which is not chosen is lost when either a secondary function or a tertiary function is chosen. However, when using it as an input, read-out of an input data is possible at a port n data register (PnD).

PIN DESCRIPTION

In the I/O column, "—" denotes a power pin, "I" an input pin, "O" an output pin, and "I/O" an input/output pin.

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated) Connect the capacitor C_L(1uF)(Refer to Measuring circuit 1) to V_{SS}	—	—
SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—
SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—
V_{REF}	—	Reference power supply pin for successive-approximation type ADC	—	—
Test				
TEST0	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
TEST1_N	I	Input pin for testing. Has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a "H" level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—
General-purpose Output port				
P20 to P25	O	General-purpose output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
General-purpose Input/output port				
P40 to P47	I/O	General-purpose input/output ports. Provided with a secondary function or a tertiary function. Cannot be used as ports if their secondary function or tertiary function is used.	Primary	Positive
P80 to P87	I/O	General-purpose input/output ports. Provided with a secondary function or a tertiary function. Cannot be used as ports if their secondary function or tertiary function is used.	Primary	Positive
P90 to P96[*1]	I/O	General-purpose input/output ports.	Primary	Positive
PA0 to PA7[*1]	I/O	General-purpose input/output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
PB0 to PB6[*1]	I/O	General-purpose input/output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
PC0 to PC3[*1]	I/O	General-purpose input/output ports.	Primary	Positive

[*1]: ML610Q327/ML610Q338/ML610Q339 have a different pin configuration for each package. See "LIST OF PINS" for more details.

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P80 pin and PB0 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	I/O	I^2C clock input/output pin. This pin is used as the secondary function of the P81 pin and PB1 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin and P80 pin.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 pin and P81 pin.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 pin and P82 pin.	Tertiary	Positive
SIN1	I	Synchronous serial data input pin. Allocated to the tertiary function of the P84 pin and the secondary function of the P40 pin and PA0 pin.	Secondary/ Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P85 pin and the secondary function of the P41 pin and PA1 pin.	Secondary/ Tertiary	—
SOUT1	O	Synchronous serial data output pin. Allocated to the tertiary function of the P86 pin and the secondary function of the P42 pin and PA2 pin.	Secondary/ Tertiary	Positive
UART				
TXD0	O	UART0 data output pin. Allocated to the secondary function of the P87 pin and the tertiary function of the P83 pin.	Secondary	Positive
RXD0	I	UART0 data input pin. Allocated to the secondary function of the P86 pin.	Secondary	Positive
TXD1	O	UART1 data output pin. Allocated to the secondary function of the P83 pin and the tertiary function of the P87 pin.	Secondary	Positive
RXD1	I	UART1 data input pin. Allocated to the secondary function of the P82 pin.	Secondary	Positive
PWM				
PWM0	O	PWM0 output pin. Allocated to the secondary function of the P23 pin and PA3 pin.	Secondary	Positive
PWM1	O	PWM1 output pin. Allocated to the secondary function of the P24 pin and PB2 pin.	Secondary	Positive
PWM2	O	PWM2 output pin. Allocated to the secondary function of the P25 pin.	Secondary	Positive
External interrupt				
EXI0 to 7	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P80 to P87 pins.	Primary	Positive/ Negative
LED drive				
LED0 to 5	O	Pins for LED driving. Allocated to the primary function of the P20 to P25 pins.	Primary	Positive/ Negative
Voice output function				
SPP	O	Positive output pin of the internal speaker amplifier.	—	—
SPM	O	Negative output pin of the internal speaker amplifier.	—	—
Successive-approximation type A/D converter				
AIN0 to 7	I	Analog inputs to Ch0 to Ch7 of the successive-approximation type A/D converter. Allocated to the primary function of the P40 to P47 pins.	Primary	—

TERMINATION OF UNUSED PINS

How to Terminate Unused Pins

Pin	Recommended pin termination
RESET_N	Open
TEST0	Open
TEST1_N	Open or connect to V_{DD} *2
V_{REF}	Connect to V_{DD}
P40 to P47 (AIN0 to AIN7)	Open
SPV_{DD}	Connect to V_{DD}
SPV_{SS}	Connect to V_{SS}
SPP	Open
SPM	Open
P20 to P25	Open
P80 to P87	Open
P90 to P96*1	Open
PA0 to PA7*1	Open
PB0 to PB6*1	Open
PC0 to PC3*1	Open

*1: ML610Q327/ML610Q338/ML610Q339 have a different pin configuration for each package. See "LIST OF PINS" for more details.

*2: TEST1_N pin has the built-in pull-up resistor (Typ.10kΩ). It is recommended to connect to V_{DD} or be pulled up by around 1kΩ resistor in a severe enviroment such as noise.

Notes:

- The unused input ports or unused input/output ports should not be configured as high-impedance inputs and left open. If the corresponding pins are configured as high-impedance inputs and left open, because the input buffer of both Nch and Pch MOS transistor turn on, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.
- When the power is turned on, the state of the general-purpose port is undefined. Therefore, there is a possibility of outputting high-level or low-level.If the undefined state at the power-on is a problem, take measures with the peripheral components on the user board.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	−0.3 to +6.5	V
Power supply voltage 2	SPV_{DD}	Ta=25°C	−0.3 to +6.5	V
Power supply voltage 3	V_{DDL}	Ta=25°C	−0.3 to +2.0	V
Reference supply voltage	V_{REF}	Ta=25°C	−0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	Ta=25°C	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	−0.3 to V_{DD}+0.3	V
Output current 1 (P40 to P47, P80 to P87, P90 to P96[*1], PA0 to PA7[*1], PB0 to PB6[*1], PC0 to PC3[*1])	I_{OUT1}	Ta=25°C	−12 to +11	mA
Output current 2 (P20 to P25)	I_{OUT2}	Ta=25°C When setting Nch open drain mode.	−12 to +20	mA
Power dissipation	PD	Ta=25°C	1.0	W
Storage temperature	T_{STG}	—	−55 to +150	°C

[*1]: ML610Q327/ML610Q338/ML610Q339 have a different pin configuration for each package. See “LIST OF PINS” for more details.

Recommended Operating Conditions

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	−40 to +85	°C
Operating voltage	V_{DD}	—	2.0 to 5.5	V
	SPV_{DD}	—	2.0 to 5.5	
Reference supply voltage	V_{REF}	$V_{DD} \geq V_{REF}$	2.2 to V_{DD}	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 2.0 to 5.5V	27k to 4.2M	Hz
		V_{DD} = 2.2 to 5.5V	4.2M to 8.4M	
Capacitor externally connected to V_{DD} pin	C_V	—	More than 1.0±30%	µF
Capacitor externally connected to V_{DDL} pin	C_L	—	1.0±30%	µF

Operating Conditions of Flash Memory

(V_{SS}= SPV_{SS}=0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	At write/erase (Data flash area)		-40 to +70	°C
		At write/erase (Program code area)		0 to +40	
Operating voltage	V_{DD}	At write/erase		2.2 to 5.5	V
Maximum rewrite count*1	C_{EPD}	Data flash area(512Byte x 4)		10,000	cycles
	C_{EPP}	Program code area		100	
Erase unit	—	Chip erase		All program and data area	—
	—	Block erase	Program area	16	KB
			Data area	2	
	—	Sector erase		512	B
Erase time(Maximum)	—	Chip/Block/Sector erase		50	ms
Program unit	—	—		1word(2Bytes)	—
Program time(Maximum)	—	1word(2Bytes)	Program area	40	µs
			Data area	60	
Data retention period	Y_{DR}	—		15	years

*1 : It means one erase and one program. Even when erasing is interrupted, it counts as one time.

DC Characteristics (Supply Current)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measuring circuit
				Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped	Ta≤+50°C	—	0.7	4.0	µA	1
			Ta≤+85°C	—	0.7	9.0		
Supply current 2	IDD2	CPU: In HALT state (LTBC,WDT: Operating) High-speed oscillation: Stopped	Ta≤+50°C	—	2.0	5.0		
			Ta≤+85°C	—	2.0	10		
Supply current 3	IDD3	CPU: Running at 32.768 kHz*1 High-speed oscillation: Stopped		—	15	30		
Supply current 4	IDD4	CPU: Running at 4.096MHz RC oscillating mode	V_{DD}=SPV_{DD}= 3.0V	—	1.0	2.5	mA	
			V_{DD}=SPV_{DD}= 5.0V	—	1.0	2.5		
		CPU: Running at 8.192MHz RC oscillating mode	V_{DD}=SPV_{DD}= 3.0V	—	2.0	3.5		
			V_{DD}=SPV_{DD}= 5.0V	—	2.0	3.5		
Supply current 5	IDD5	CPU: Running at 4.096MHz RC oscillating mode During voice playback of 1kHz,2.98db,SIN-wave (no output load)	V_{DD}=SPV_{DD}= 3.0V	—	2.0	5.0		
			V_{DD}=SPV_{DD}= 5.0V	—	4.0	8.0		
		CPU: Running at 8.192MHz RC oscillating mode During voice playback of 1kHz,2.98db,SIN-wave (no output load)	V_{DD}=SPV_{DD}= 3.0V	—	3.0	6.0		
			V_{DD}=SPV_{DD}= 5.0V	—	5.0	9.0		

*1: Case when the CPU operating rate is 100% (no HALT state).

DC Characteristics (VOHL, IOHL, IIHL)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P25) (P40 to P47) (P80 to P87) (P90 to P96[*1]) (PA0 to PA7[*1]) (PB0 to PB6[*1]) (PC0 to PC3[*1])	VOH1	IOH1=−0.5mA (When one port is selected as output mode)		V_{DD} −0.5	—	—	V	2
	VOL1	IOL1=+0.5mA (When one port is selected as output mode)		—	—	0.5		
Output voltage 2 (P20 to P25)	VOL2	(When one port is selected as Nch open drain mode)	IOL2=+5mA V_{DD}≥2.2V	—	—	0.5		
			IOL2=+8mA V_{DD}≥2.3V	—	—	0.5		
Output voltage 3 (P80 to P81) (PB0 to PB1)	VOL3	IOL3=+3mA (I^2C bus input/output mode, When one port is selected as output)		—	—	0.4		
Output leakage (P20 to P25) (P40 to P47) (P80 to P87) (P90 to P96[*1]) (PA0 to PA7[*1]) (PB0 to PB6[*1]) (PC0 to PC3[*1])	IOOH	VOH=V_{DD} (in high-impedance state)		—	—	1.0	μA	3
	IOOL	VOL=V_{SS} (in high-impedance state)		−1.0	—	—		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1=V_{DD}		0	—	1.0	μA	4
	IIL1	VIL1=V_{SS}		−1500	−300	−20		
Input current 2 (P40 to P47) (P80 to P87) (P90 to P96[*1]) (PA0 to PA7[*1]) (PB0 to PB6[*1]) (PC0 to PC3[*1])	IIH2	VIH2=V_{DD} (when pulled-down)		2	30	250		
	IIL2	VIL2=V_{SS} (when pulled-up)		−250	−30	−2		
	IIH2Z	VIH2=V_{DD} (in high-impedance state)		—	—	1.0		
	IIL2Z	VIL2=V_{SS} (in high-impedance state)		−1.0	—	—		
Input current 3 (TEST0)	IIH3	VIH3=V_{DD}		20	300	1500		
	IIL3	VIL3=V_{SS}		−1.0	—	—		

[*1]: ML610Q327/ML610Q338/ML610Q339 have a different pin configuration for each package. See “LIST OF PINS” for more details.

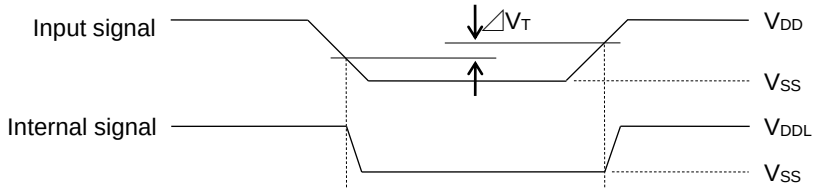
DC Characteristics (VIHL)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (TEST1_N) (P40 to P47) (P80 to P87) (P90 to P96*1) (PA0 to PA7*1) (PB0 to PB6*1) (PC0 to PC3*1)	VIH1	—	0.7×V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3×V_{DD}		
Hysteresis width (RESET_N) (TEST0) (TEST1_N) (P40 to P47) (P80 to P87) (P90 to P96*1) (PA0 to PA7*1) (PB0 to PB6*1) (PC0 to PC3*1)	⊿V_T	—	0.05×V_{DD}	—	0.4×V_{DD}		
Input pin capacitance (P40 to P47) (P80 to P87) (P90 to P96*1) (PA0 to PA7*1) (PB0 to PB6*1) (PC0 to PC3*1)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	10	pF	—

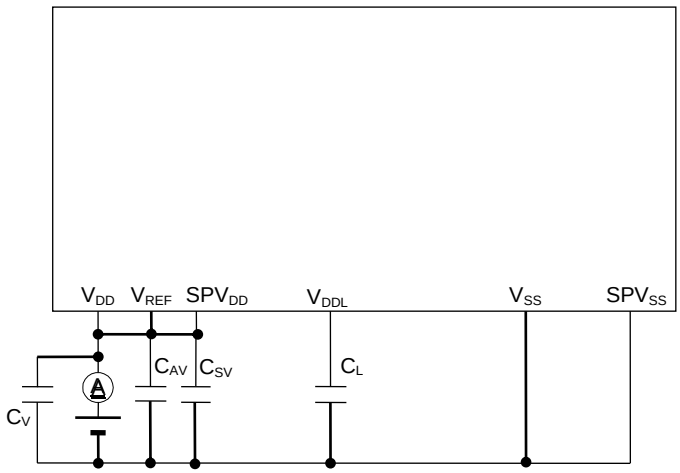
*1: ML610Q327/ML610Q338/ML610Q339 have a different pin configuration for each package. See “LIST OF PINS” for more details.

Hysteresis Width



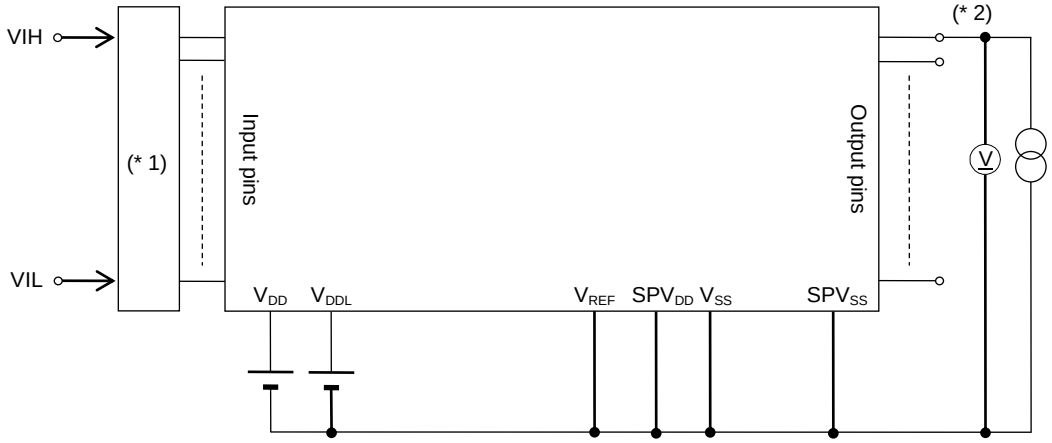
Measuring circuit

・Measuring circuit 1



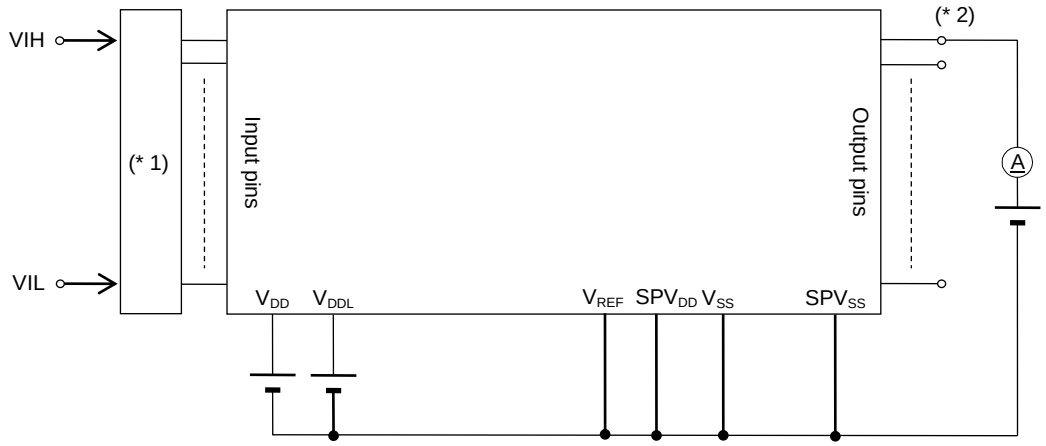
C_V : 1.0μF
C_{SV} : 1.0μF
C_{AV} : 1.0μF
C_L : 1.0μF

・Measuring circuit 2



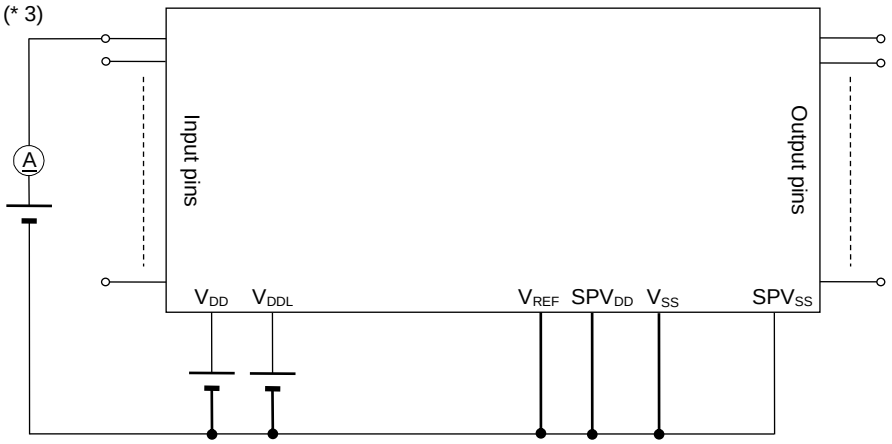
(* 1) Input logic circuit to determine the specified measuring conditions.
(* 2) Measured at the specified output pins.

・Measuring circuit 3



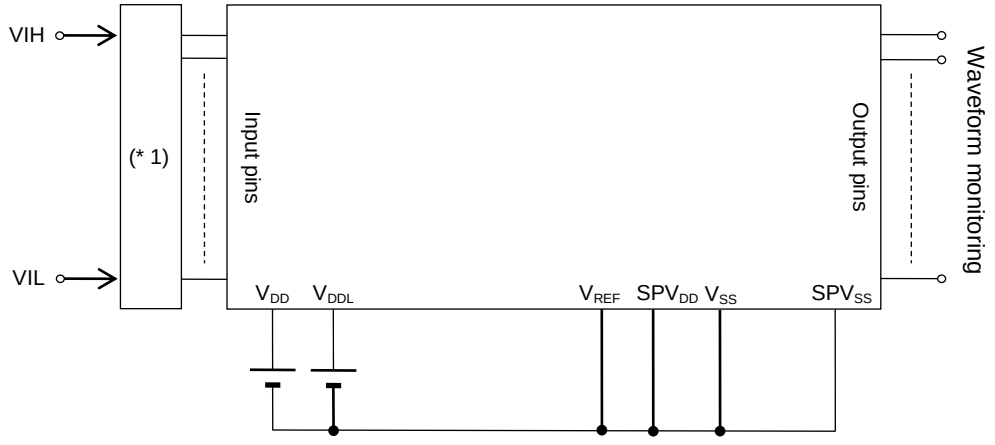
(* 1) Input logic circuit to determine the specified measuring conditions.
(* 2) Measured at the specified output pins.

・Measuring circuit 4



(* 3) Measured at the specified output pins.

・Measuring circuit 5



(* 1) Input logic circuit to determine the specified measuring conditions.

AC Characteristics (Oscillation Circuit)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring Circuit
			Min.	Typ.	Max.		
Built-in RC oscillation frequency	f_{LCR}	Ta = −10 to +50°C	Typ -1.5%	32.768	Typ +1.5%	kHz	1
		Ta = −40 to +85°C	Typ -3.0%		Typ +3.0%		
PLL oscillation frequency	f_{HPLL}	Ta = −10 to +50°C	Typ -1.5%	4.096 or 8.192	Typ +1.5%	MHz	
		Ta = −40 to +85°C	Typ -3.0%		Typ +3.0%		

Electrical Characteristics of Speaker amp

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

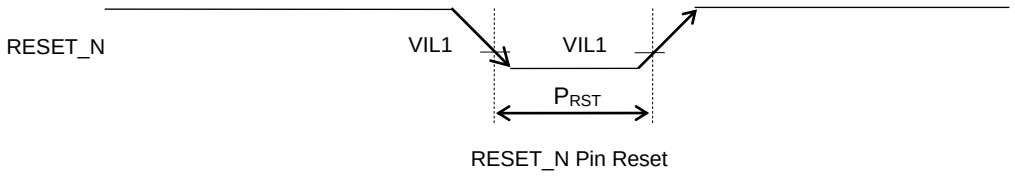
Parameter	Symbol	Condition	Rating			Unit	
			Min.	Typ.	Max.		
SPM, SPP output load resistance	R_{LSP}	—	6.4	8	—	Ω	
Speaker amp output power	P_{SPO1}	SPV_{DD}=3.0V, f=1kHz R_{SPO}=8Ω, THD≥10%	—	0.45	—	W	
	P_{SPO2}	SPV_{DD}=5.0V, f=1kHz R_{SPO}=8Ω, THD≥10%	—	1.0	—		

AC Characteristics (Power on, Reset Sequence)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Time until it starts SPV_{DD} after starting V_{DD}	t_{VDD}	—	0	—	—	ns	1
Reset *1 pulse width	P_{RST}	—	100	—	—	µs	
Reset *1 noise elimination pulse width	P_{NRST}	—	—	—	0.4		
Power-on rising slope	S_{POR}	—	0.1	—	—	V/ms	

*1 : reset from RESET_N pin



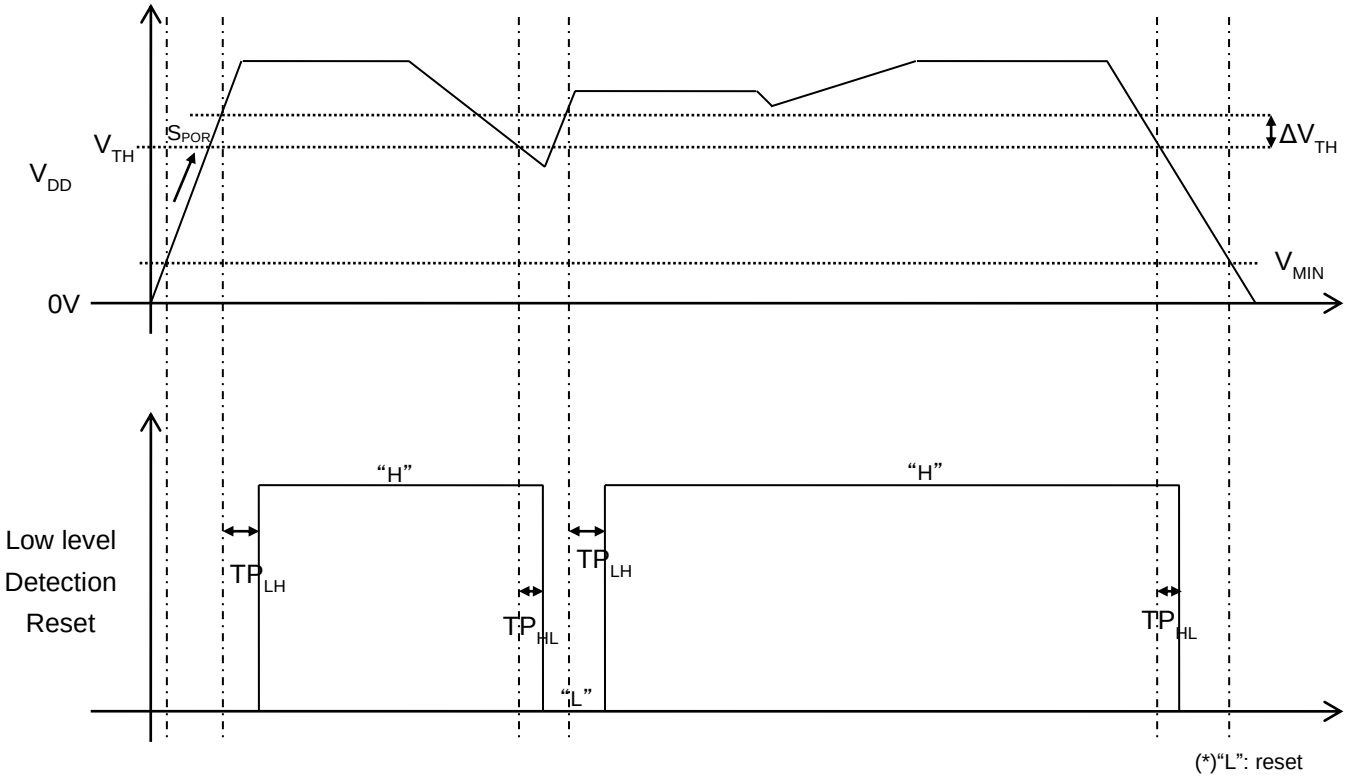
RESET_N Pin Reset

Power-on rising slope

Electrical Characteristics of Low Level Detection Reset

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

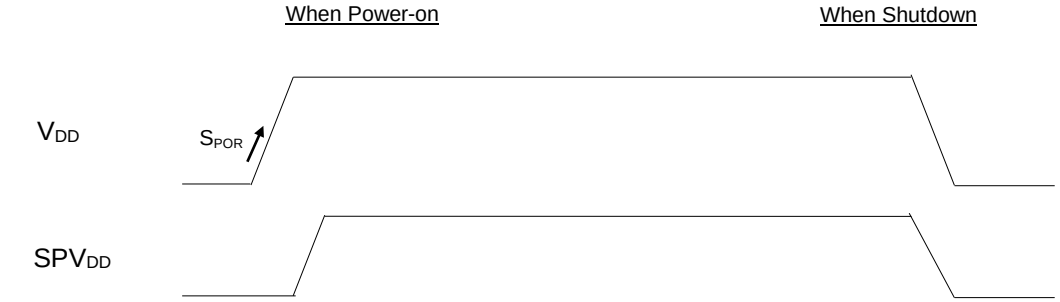
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Detection voltage	V_{TH}	LLD2-0=7H	Typ. -5%	1.9	Typ. +5%	V	1
		LLD2-0=2H or LLD2-0=6H	Typ. -5%	2.1	Typ. +5%		
		LLD2-0=1H or LLD2-0=5H	Typ. -5%	2.3	Typ. +5%		
		LLD2-0=0H or LLD2-0=4H	Typ. -5%	2.5	Typ. +5%		
		LLD2-0=3H	Typ. -7%	2.7	Typ. +7%		
Hysteresis width	ΔV_{TH}	—	0.05	0.1	0.15	V	
Output delay when power rising	TP_{LH}	—	—	10	200	µs	
Output delay when power falling	TP_{HL}	—	—	10	200	µs	
Low level detection reset operating voltage	V_{MIN}	—	1.0	—	—	V	



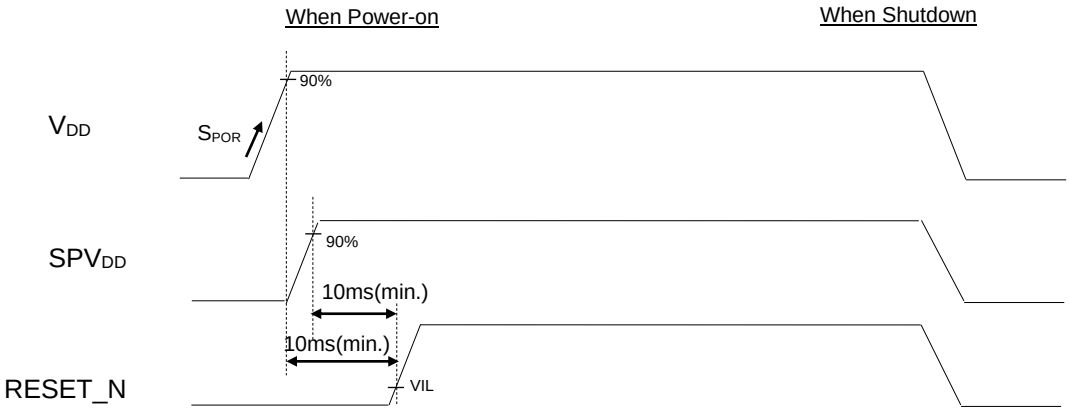
Note:
When the detection voltage of Low Level Detection Reset (V_{TH}) is set to 1.9V(LLD2-0=7H), Low Level Detection Reset is not asserted in the voltage lange from lower minimum recommended operating volatge (V_{DD}=2.0V) to upper detection voltage (V_{TH}=1.9V). During power shutdown sequence, if this voltage lange is kept, depending on the LSI operationg condition, the internal regulated power supply circuit (VRL) can not keep the operationg votage, and the program may NOT operate properly. Therefore, please take measures, such as, setting Low Level Detection Reset (V_{TH}) to except 1.9V (LLD2-0 =7H), and reset generation from RESET_N pin for fail-safe

Power-on/Shutdown Sequence

・When the power-on rising slope is 0.1V/ms(Min.) or more



・When the power-on rising slope is less than 0.1V/ms(Min.)



Recommended power-on/shutdown sequence
There are no ristrictions of order, slope time, time lag in turnning on/off V_{DD} and SPV_{DD}.

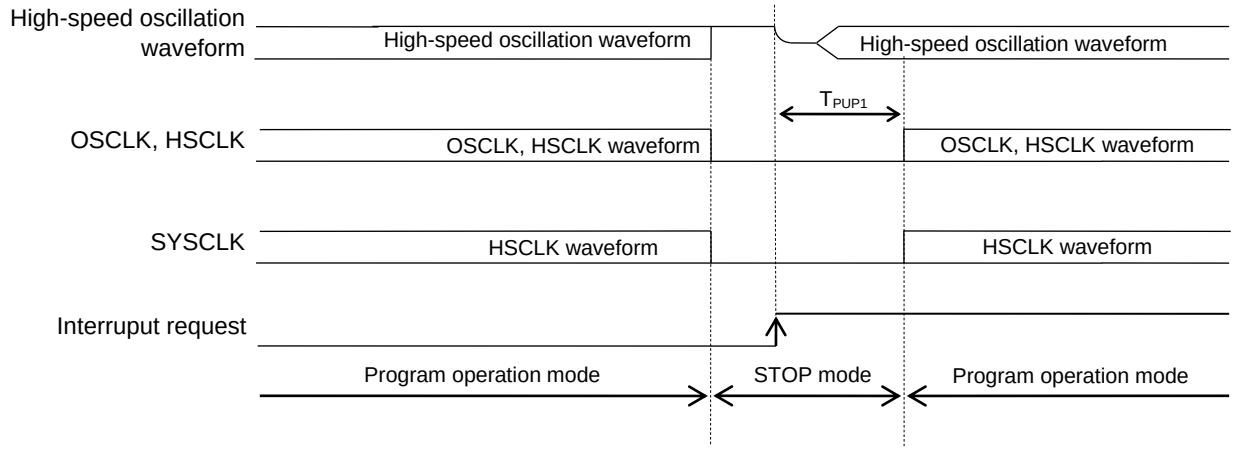
Notes:

- When the power is turned on, the state of the general-purpose port is undefined. Therefore, there is a possibility of outputting high-level or low-level.If the undefined state at the power-on is a problem, take measures with the peripheral components on the user board.
- When power-on reset is generated because of instantaneous power failure etc., or, when the glitch which is narrower than output delay when power falling (TP_{HL}) is generated on V_{DD} power, or, When V_{DD} power is decreased below low level detection reset operating voltage (V_{MIN}) before output delay when power falling (TP_{HL}) is passed, the LSI may NOT get reset, and the program may NOT operate properly. Therefore, please take measures, such as, power voltage drop prevention by bypass capacitors, and reset generation from RESET_N pin for fail-safe.

AC Characteristics (Oscillation stable time after STOP release)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

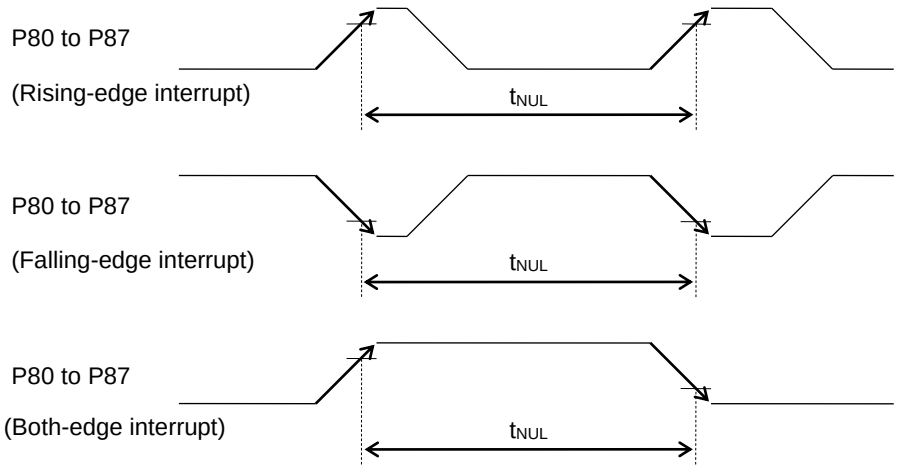
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation stable time after STOP release	T_{PUP1}	—	—	—	2	ms



AC Characteristics (External Interrupt)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=–40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE=1) CPU: NOP operation	2.5×sysclk	—	3.5×sysclk	µs

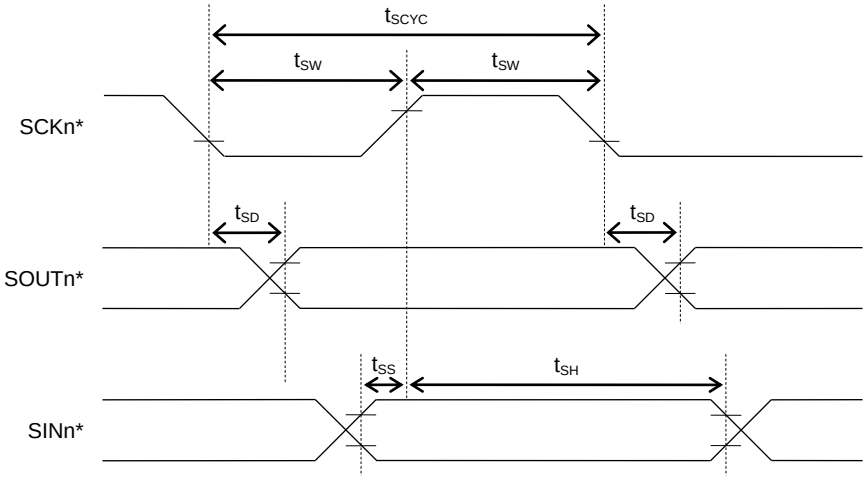


AC Characteristics (Synchronous Serial Port)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	µs
		When high-speed oscillation is active	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	VDD≥2.4V	—	4	—	MHz
		VDD≥2.0V	—	2	—	
SCK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	µs
		When high-speed oscillation is active	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK*1 ×0.4	SCK*1 ×0.5	SCK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected with SnCK3–0 of the serial port n mode register (SIOnMOD1) (n=0,1)



*: Indicates the secondary/tertiary function of the port. n=0, 1

AC Characteristics (I^2C Bus Interface: Standard Mode 100kbps)

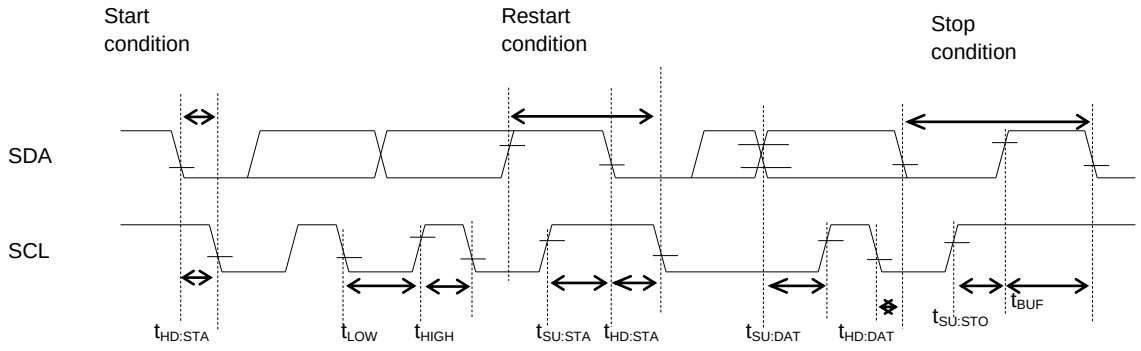
(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL ”L” level time	t_{LOW}	—	4.7	—	—	µs
SCL ”H” level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC Characteristics (I^2C Bus Interface: Fast Mode 400kbps)

(V_{DD}= 2.0 to 5.5V, SPV_{DD}=2.0 to 5.5V, V_{SS}= SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL ”L” level time	t_{LOW}	—	1.3	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs

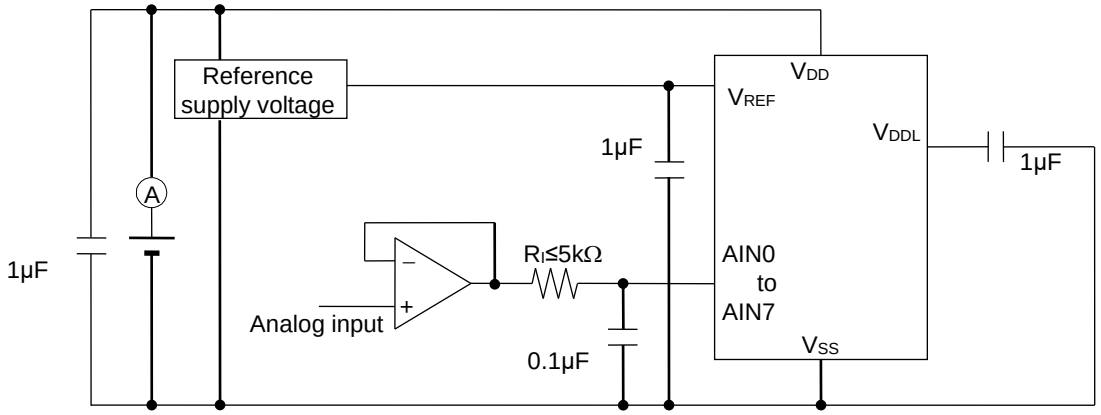


Electrical Characteristics of Successive Approximation Type A/D Converter

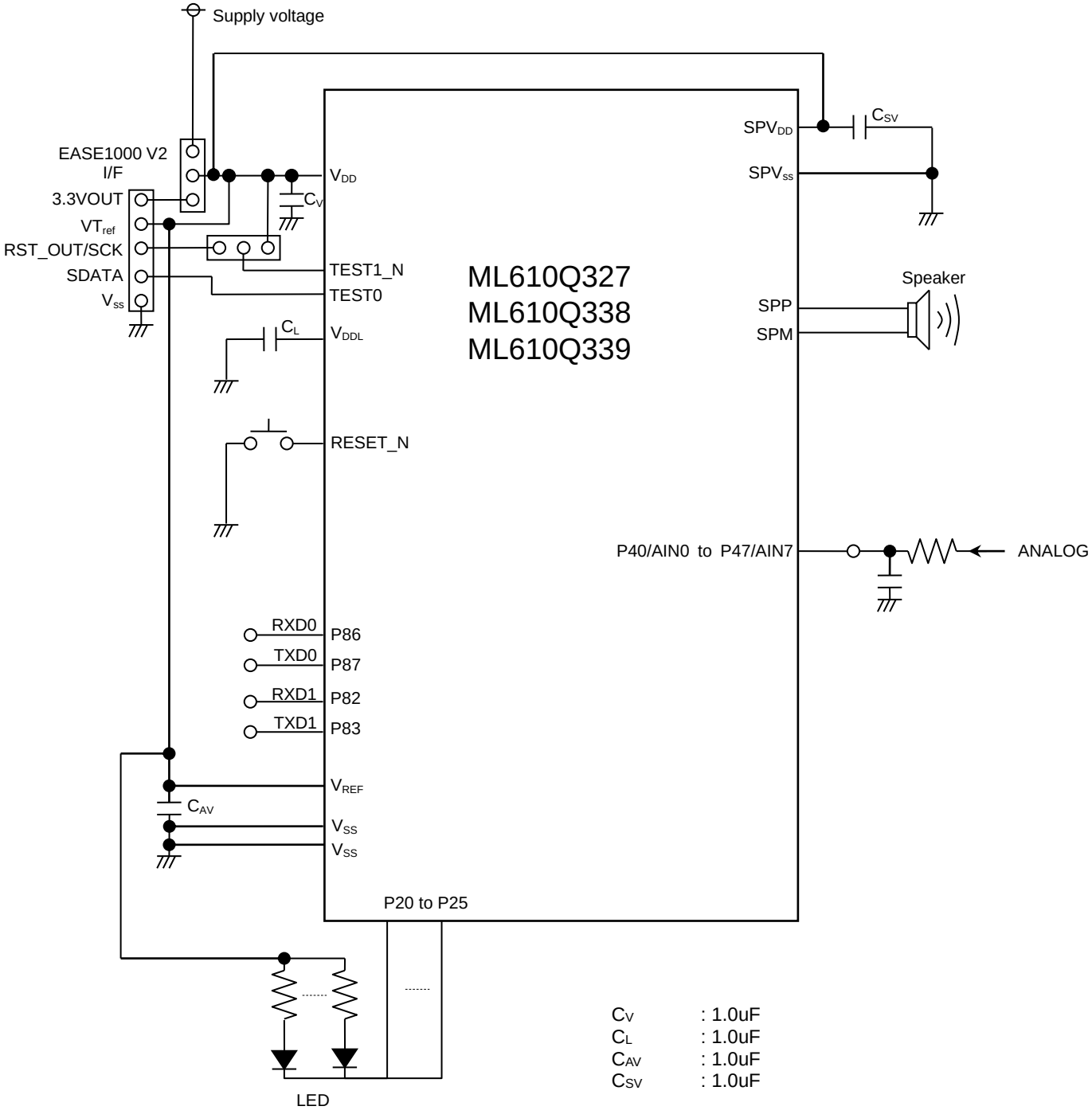
(V_{DD}=SPV_{DD}=2.2 to 5.5V, V_{REF}=2.2 to 5.5V, V_{SS}=SPV_{SS}=0V, Ta=−40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	10	bit
Integral non-linearity error	IDL	2.7V≤V_{REF}≤5.5V	−4	—	+4	LSB
		2.2V≤V_{REF}<2.7V	−5	—	+5	
Differential non-linearity error	DNL	2.7V≤V_{REF}≤5.5V	−3	—	+3	
		2.2V≤V_{REF}<2.7V	−4	—	+4	
Zero-scale error	V_{OFF}	R_I≤5kΩ	−4	—	+4	
Full-scale error	FSE	R_I≤5kΩ	−4	—	+4	
Prefilter resistance	R_I	—	—	—	5k	Ω
Reference supply voltage	V_{REF}	—	2.2	—	V_{DD}	V
Conversion time	t_{CONV}	HSCLK=4M to 8.4MHz	—	102	—	ϕ/CH

ϕ: Period of high-speed clock (HSCLK)

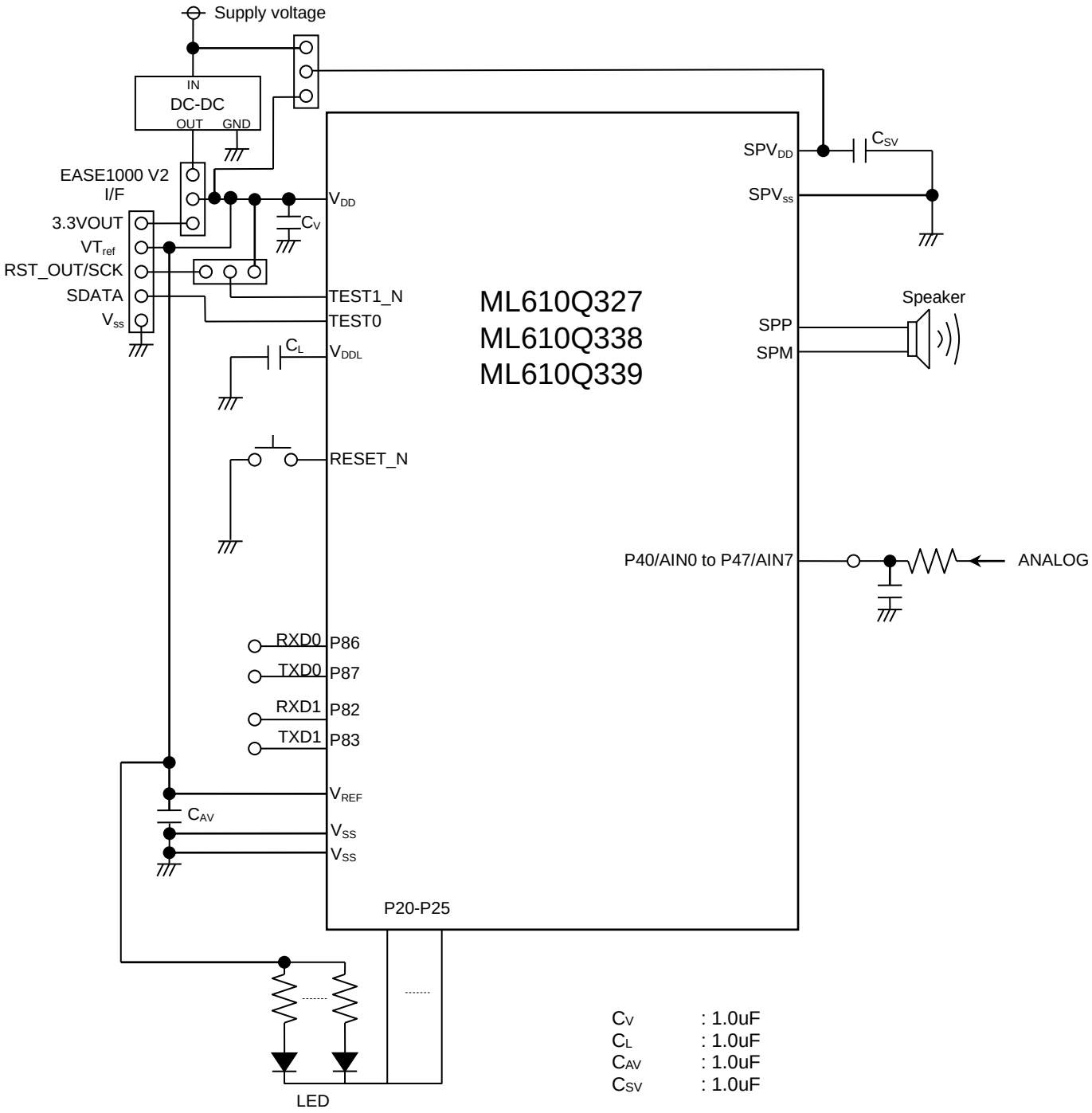


Example of Application Circuit



V_{DD} and SPV_{DD} are supplied from same power supply

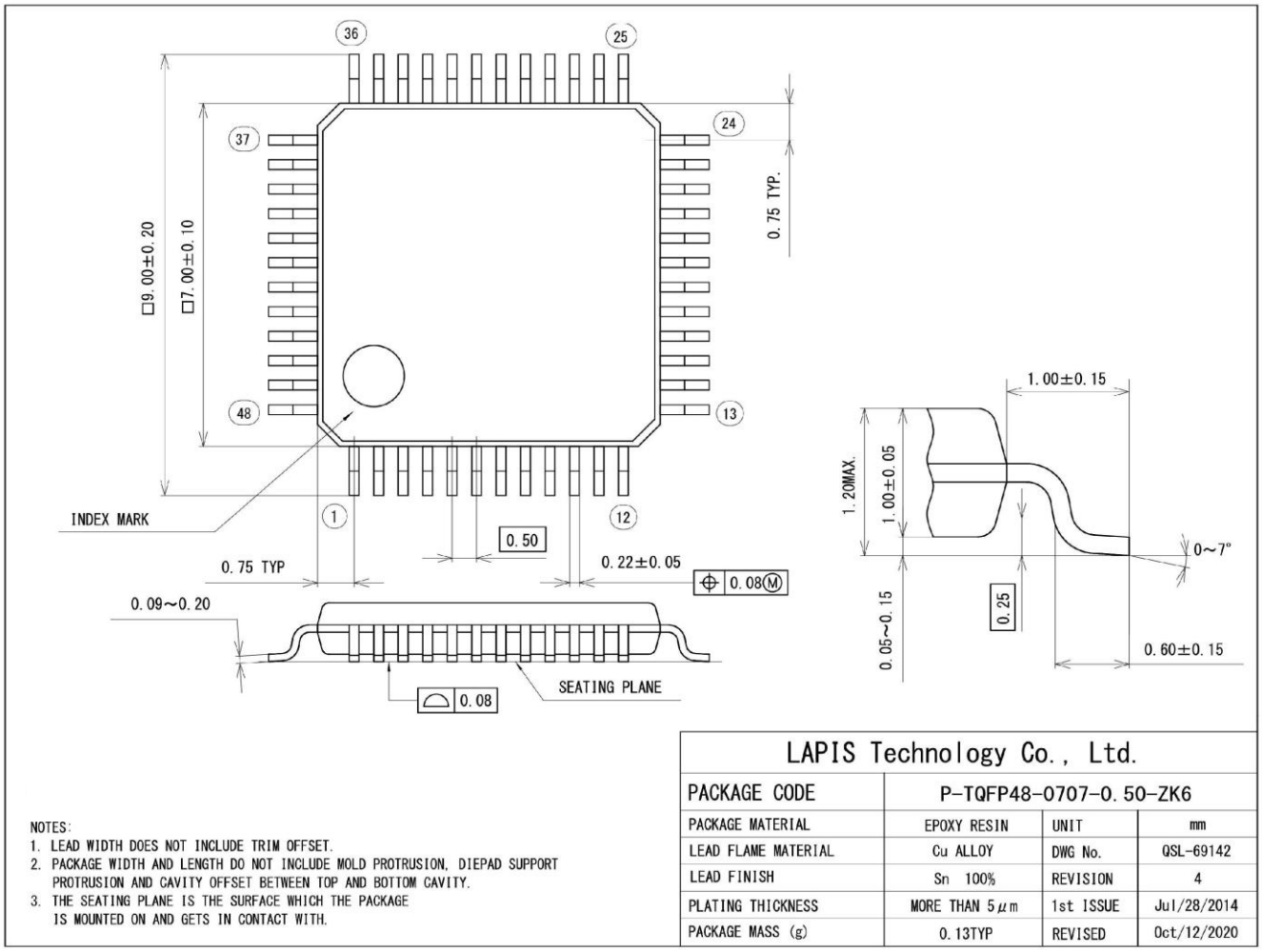
Note:
Design the PCB layout having the shortest wiring distance between V_{DDL} pin and V_{DDL} pin's external capacitor (C_L), and between V_{DDL} pin's external capacitor (C_L) and V_{SS} for noise reduction purpose.



V_{DD} is supplied through DC-DC converter from SPV_{DD}

Note:
Design the PCB layout having the shortest wiring distance between V_{DDL} pin and V_{DDL} pin's external capacitor (C_L), and between V_{DDL} pin's external capacitor (C_L) and V_{SS} for noise reduction purpose.

PACKAGE DIMENSIONS (48pin TQFP)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

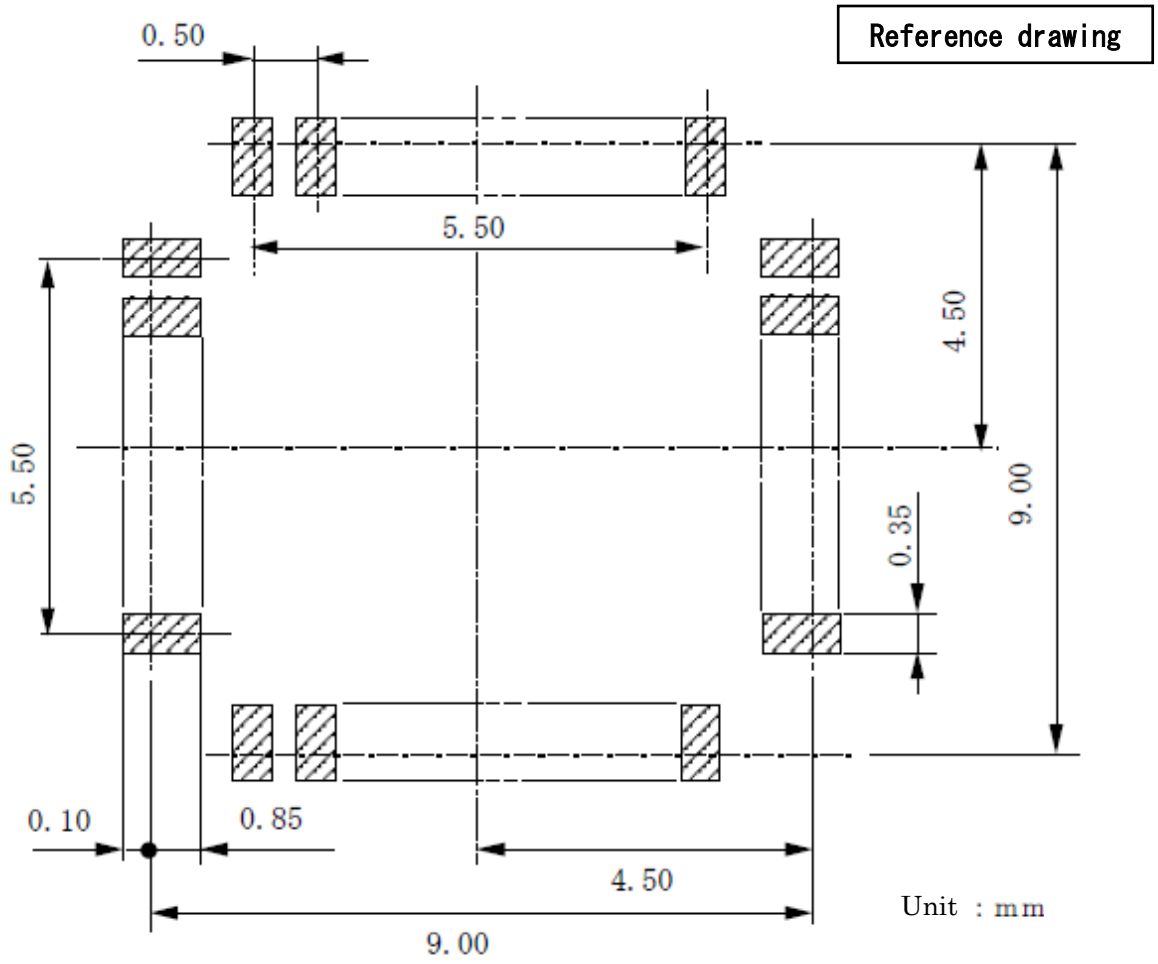
The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	W/L/t=76.2 / 114.3 / 1.6(mm)
PCB Layer	JEDEC 4layers
Air cooling conditions	Calm(0m/sec)
Heat resistance(θJa)	53.5 [°C/W]
Power consumption of Chip PMax	0.300[W]

TjMax of this LSI is 110 °C. TjMax is expressed with the following formulas.

TjMax = TaMax + θJa × PMax

Figure of soldering department terminal existence range (48pin TQFP)

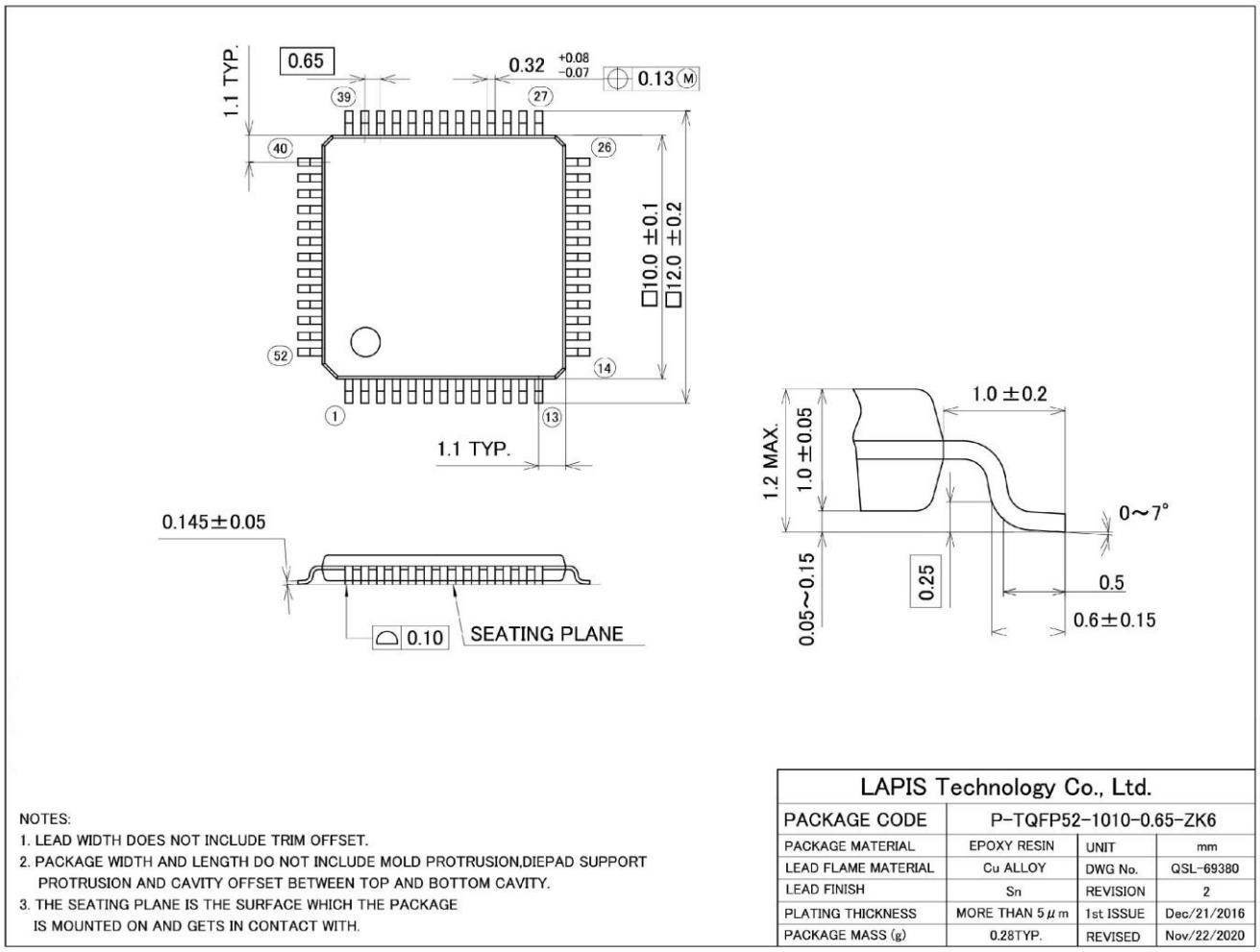


Attention of the layout of a mounting board

Please take into consideration enough that there are not ease of a mounting, the reliability of contact, leading about of a wiring, and a solder bridge generate in the case of layout of the foot pattern of a mounting board.

The optimal layout of a foot pattern changes by the board quality of material, the solder paste category to be used, thickness, the soldering methodology, etc. Therefore, since the span where the terminator of this package may exist is shown as a "soldering part terminator extent drawing", please give as reference data of a foot pattern design.

PACKAGE DIMENSIONS (52pin TQFP)



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION,DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP52-1010-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69380
LEAD FINISH	Sn	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Dec/21/2016
PACKAGE MASS (g)	0.28TYP.	REVISED	Nov/22/2020

Notes for Mounting the Surface Mount Type Package

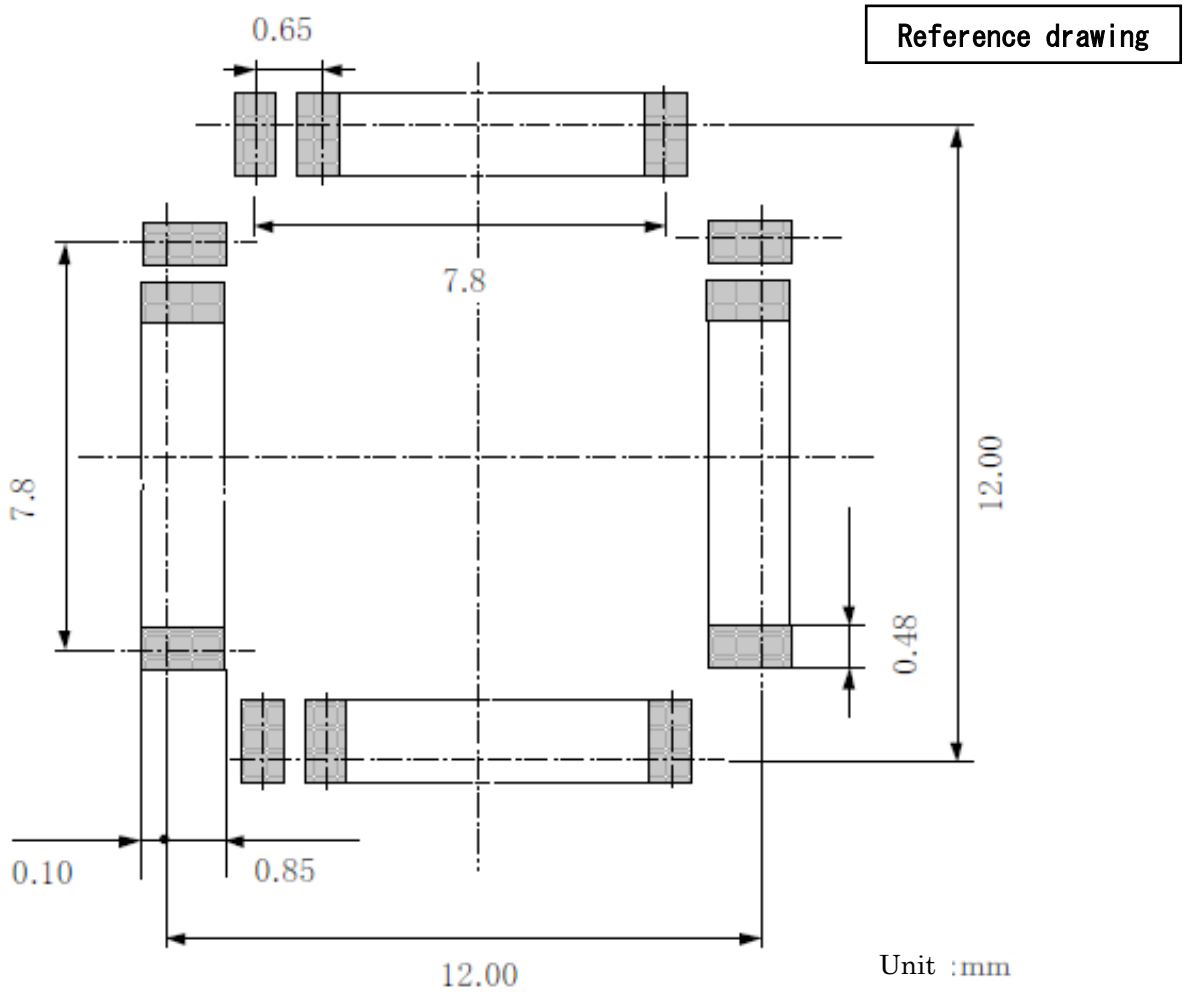
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	W/L/t=76.2 / 114.3 / 1.6（mm）
PCB Layer	JEDEC 4layers
Air cooling conditions	Calm（0m/sec）
Heat resistance（θJa）	49.9 [°C/W]
Power consumption of Chip PMax	0.300[W]

TjMax of this LSI is 110 °C. TjMax is expressed with the following formulas.
TjMax = TaMax + θJa × PMax

Figure of soldering department terminal existence range (52pin TQFP)



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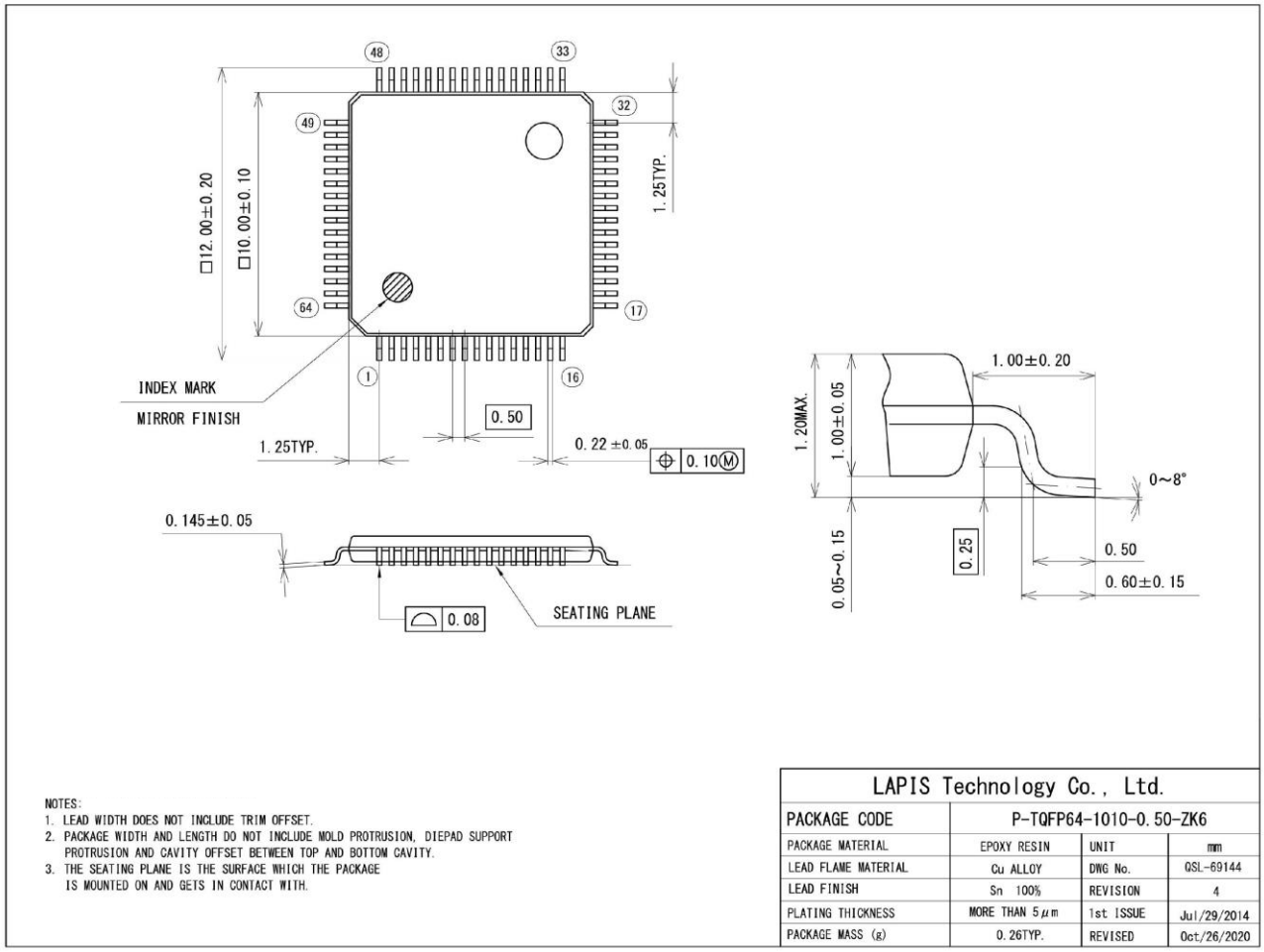
The optimal layout of a foot pattern changes by the board quality of material, the solder paste category to be used, thickness, the soldering methodology, etc. Therefore, since the span where the terminator of this package may exist is shown as a "soldering part terminator extent drawing", please give as reference data of a foot pattern design.

PACKAGE DIMENSIONS (64pin TQFP)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

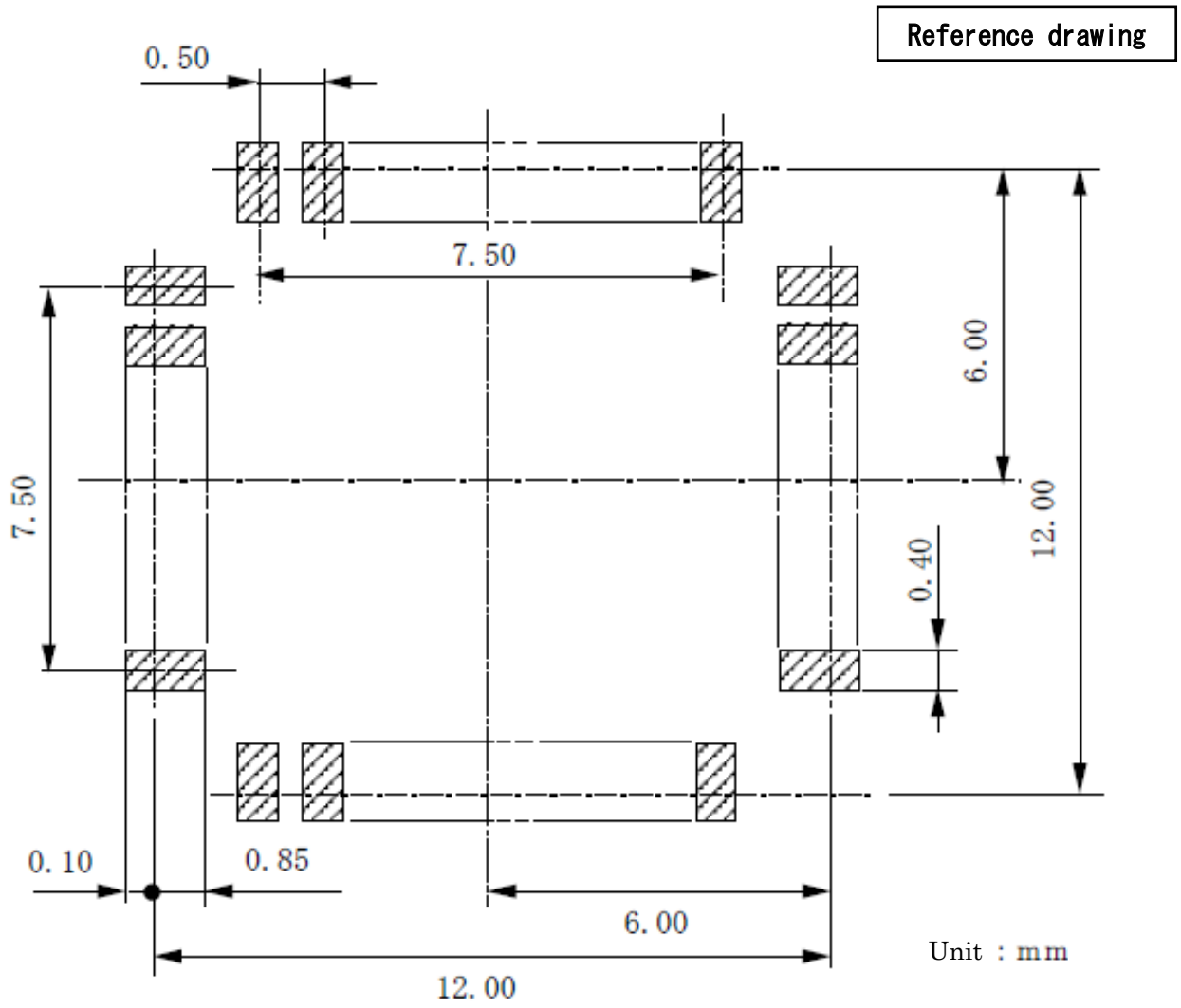
The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

PCB	W/L/t=76.2 / 114.3 / 1.6（mm）
PCB Layer	JEDEC 4layers
Air cooling conditions	Calm（0m/sec）
Heat resistance（θJa）	39.6 [°C/W]
Power consumption of Chip PMax	0.300[W]

TjMax of this LSI is 110 °C. TjMax is expressed with the following formulas.

TjMax = TaMax + θJa × PMax

Figure of soldering department terminal existence range (64pin TQFP)



Attention of the layout of a mounting board

Please take into consideration enough that there are not ease of a mounting, the reliability of contact, leading about of a wiring, and a solder bridge generate in the case of layout of the foot pattern of a mounting board.

The optimal layout of a foot pattern changes by the board quality of material, the solder paste category to be used, thickness, the soldering methodology, etc. Therefore, since the span where the terminator of this package may exist is shown as a "soldering part terminator extent drawing", please give as reference data of a foot pattern design.

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q339-01	Apr. 18, 2022	—	—	Final edition 1

Notes for product usage

Notes on this page are applicable to the all LAPIS Technology microcontroller products.
For individual notes on each LAPIS Technology microcontroller product, refer to [Note] in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS

Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON

At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
On LAPIS Technology microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY

If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCT

Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
When replacing from other product to LAPIS Technology microcontroller products, please evaluate enough the apparatus/system which implemented LAPIS Technology microcontroller products.

5. USE ENVIRONMENT

When using LAPIS Technology microcontroller products in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

Notes

1) The information contained herein is subject to change without notice.

2) When using LAPIS Technology Products, refer to the latest product information (data sheets, user's manuals, application notes, etc.), and ensure that usage conditions (absolute maximum ratings, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. You are responsible for evaluating the safety of the final products or systems manufactured by you.

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