Dear customer

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Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML5810A

High-Side Switch Driver IC for Battery Pack

■General Description

ML5810A is charge/discharge high-side switch Nch power MOSFET gate driver for battery pack. ML5810A assert external input reference voltage(CFS, DFS)+12V(typ) as the voltage for drive by charge pump. And also, built-in PchMOSFET gate driver for low current precharge in battery over-discharge state.

■Features

- •High-side switch Nch power MOSFET gate driver for battery pack protection
- •Built-in Pch MOSFET gate driver for low current precharge/predischarge
- •80V breakdown voltage applicable to 48V battery system
- •Built-in charge pump
- •Gate driver for charge/discharge ”H” output voltage : Reference voltage(CFS, DFS)+10V (min)
- •Gate driver for precharge/predischarge ”L” output voltage : Reference voltage (PCFS)-9V (min)
- Current consumption : 210uA(typ), 480uA(max)
- Power supply voltage range : +6.5V to +64V
  (Absolute Maximum Rating: 80V)
- Operating temperature range : -40℃ to +105℃
- Package : 20pin TSSOP

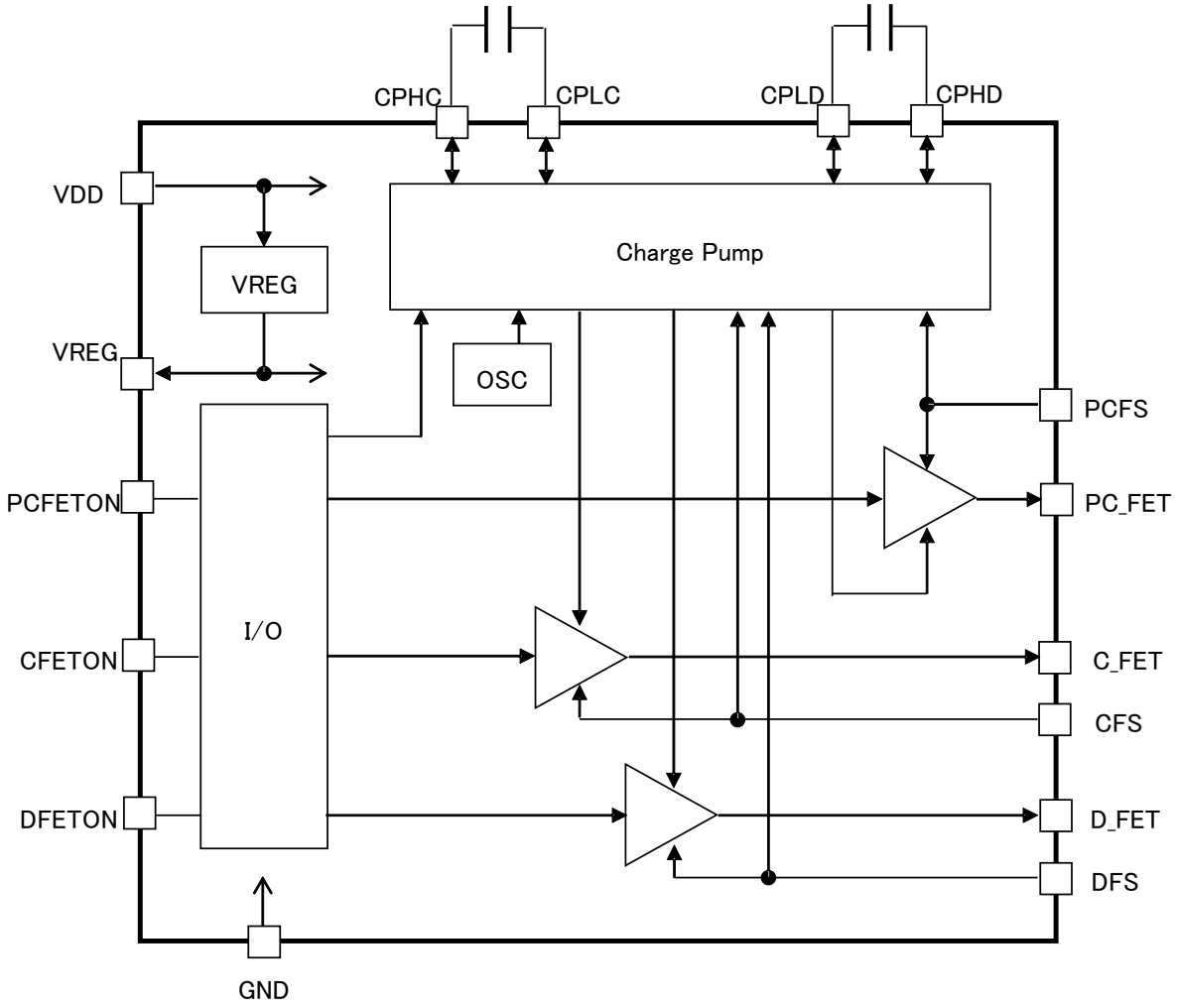
■Application

- ・E-Bike
- ・Uninterruptible Power Supplies (UPS)
- ・Energy Storage Systems (ESS)
- ・12V to 48V Battery pack for industrial

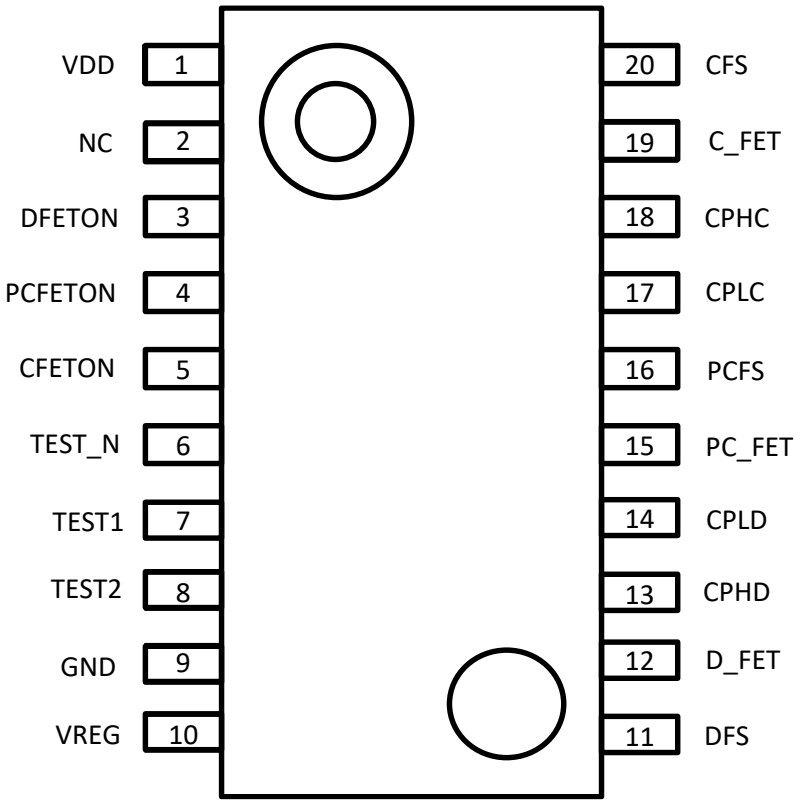
■Part number

ML5810ATD.

■Block Diagram



■Pin Configuration(Top View)



■Pin Description

Pin No.	Pin	I/O	Description
1	VDD	—	Power supply. Connect an external CR filter for noise rejection.
2	NC	—	—
3	DFETON	I	D_FET enable input.(pulldown resistance:1MΩ)
4	PCFETON	I	PC_FET enable input.(pulldown resistance:1MΩ)
5	CFETON	I	C_FET enable input.(pulldown resistance:1MΩ)
6	TEST_N	I	TEST_N input. Should be fixed to VDD.
7	TEST1	I	TEST1 input.(pulldown resistance:1MΩ) Should be fixed to GND.
8	TEST2	I	TEST2 input.(pulldown resistance:1MΩ) Should be fixed to GND.
9	GND	—	Ground.
10	VREG	O	Built-in 3.3V regurator output. Connect a 4.7μF capacitor between this pin and GND.
11	DFS	I	Reference voltage input for the D_FET drive charge pump. Connect to the source pin of the discharge FET.
12	D_FET	O	Discharge Nch-FET gate drive. Connect to the gate pin of the external Nch-FET. In the ON state, the DFS level +12V (typ) is asserted.In the OFF state DFS level is asserted.
13	CPHD	O	Charge pump capacitor input for D_FET drive. Connect a capacitor which approximately 8-times of the discharge FET gate capacitance, between the CPHD and CPLD pins.
14	CPLD	O	
15	PC_FET	O	Precharge/predischarge Pch-FET gate drive. Connected to the gate pin of the external Pch-FET. In the ON state, the PCFS level -12V (typ) is asserted, while the PCFS level is asserted in the OFF state.
16	PCFS	I	Reference voltage input for the PC_FET drive charge pump. Connected to the source pin of the precharge/predischarge FET.
17	CPLC	O	Charge pump capacitor input for C_FET drive. Connect a capacitor with approximately twice the gate capacitance of the charge FET between the CPHC and CPLC pins.
18	CPHC	O	
19	C_FET	O	Charge Nch-FET gate drive. Connected to the gate pin of the external Nch-FET. In the ON state, the CFS level +12V (typ) is asserted, while the CFS level is asserted in the OFF state.
20	CFS	I	Reference voltage input for the C_FET drive charge pump. Connected to the source pin of the charge FET.

■Absolute Maximum Ratings

GND=0V, Ta=25°C

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Applied to VDD pin	-0.3 to +86.5	V
Input voltage	V_{IN1}	Applied to CFS,DFS, and PCFS pins	-0.3 to +86.5	V
	V_{IN2}	Applied to CFETON, DFETON,PCFETON,TEST1, and TEST2,TEST_N pins	-0.3 to VDD+0.3	V
Output voltage	V_{OUT1}	Applied to D_FET pin V_{DFS}=DFS pin voltage	V_{DFS}-0.5 to +86.5	V
	V_{OUT2}	Applied to C_FET pin V_{CFS}=CFS pin voltage	V_{CFS}-0.5 to +86.5	V
	V_{OUT3}	Applied to PC_FET pin	-0.5 to +71.5	V
Short circuit output current	I_{OS1}	VDD=50V Applied to VREG pin	5	mA
	I_{OS2}	VDD=50V Applied to C_FET and D_FET pins	20	mA
	I_{OS3}	VDD=50V Applied to PC_FET pin	2	mA
Power dissipation	P_D	Ta=25℃	2.3	W
Package thermal resistance	θ ja	JEDEC double-side board mounted	33.7	℃/W
Storage temperature	T_{STG}	—	-55 to +150	°C

■Recommended Operating Conditions

（GND= 0 V）

Parameter	Symbol	Condition	Range	Unit
Power supply voltage	V_{DD}	Applied to VDD pin	6.5～64	V
Operating temperature	Ta	No VREG output load	－40～＋105	°C

■Electrical Characteristics

V_{DD}=6.5～64V,GND=0V,Ta=-40 to +105°C, no VREG output load

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital ”H” input voltage(*1)	V_{IH}	—	2.15	—	VDD+0.3	V
Digital ”L” input voltage(*1)	V_{IL}	—	0	—	0.35	V
Digital ”H” input current(*1)	I_{IH}	V_{IH} = VDD	—	—	130	μA
Digital ”L” input current(*1)	I_{IL}	V_{IL} = GND	-2	—	—	μA
C_FET / D_FET output voltage(C_FET-CFS, D_FET-DFS)	V_{OH11}	I_{OH}=-1.5μA (V_{DD}*0.95)≧10V	10	12	15	V
	V_{OH12}	I_{OH}=-1.5μA (V_{DD}*0.93)＜10V	V_{DD}*0.93	—	V_{DD}	V
PC_FET output voltage (PCFS-PC_FET)	V_{OL21}	I_{OL}=+1.5μA (V_{DD}*0.8)≧9V	9	12	15	V
	V_{OL22}	I_{OL}=+1.5μA (V_{DD}*0.8)＜9V	V_{DD}*0.8	—	V_{DD}	V
C_FET / D_FET rise time	Tfetr1	Ccp=80nF, Rg=1kΩ, Rfs=100Ω, FET gate capacitance=10nF From FET-on to 80% of output voltage V_{OH11}, V_{OH12}	—	150	350	us
C_FET / D_FET fall time	Tfetf1	Ccp=80nF, Rg=1kΩ, Rfs=100Ω, FET gate capacitance=10nF From FET-off to 20% of output voltage V_{OH11}, V_{OH12}	—	40	70	us
PC_FET fall time	Tfetf2	Ccp=80nF, Rg=1kΩ, Rfs=1kΩ, FET gate capacitance=1nF From FET-on to 80% of output voltage V_{OL21}, V_{OL22}	—	110	400	us
PC_FET rise time	Tfetr2	Ccp=80nF, Rg=1kΩ, Rfs=1kΩ, FET gate capacitance=1nF From FET-off to 20% of output voltage V_{OL21}, V_{OL22}	—	20	70	us
Current consumption in operation (charge and discharge ） (*2)	IDD1	CFETON=1 & DFETON=1 & PCFETON=0 VDD=CFS=DFS=PCFS	—	210	480	uA
Current consumption in operation (precharge or predischarge ）(*2)	IDD2	CFETON=0 & DFETON=0 & PCFETON=1 VDD=CFS=DFS=PCFS	—	135	380	uA

VREG output voltage	V_{REG1}	V_{DD}=6.5V～64V Output load current＜1mA	3.0	3.3	3.6	V
C_FET / D_FET charge pump frequency	F_{CPCD}	—	6.25	7.8125	9.4	kHz
PC_FET charge pump frequency	F_{CPPC}	—	0.78	0.9766	1.2	kHz

*1：Applied to CFETON,DFETON,PCFETON,TEST1,TEST2 and TEST_N pins

*2：Current consumption are sum of VDD,CFS,DFS, and PCFS currents

■Functional Description

Operating state of ML5810A in each input status of 3 control input(PCFETON, DFETON, CFETON) is indicated in the following table.
“Charge pump ON, FET stand-by” is in which a charge pump powers up and each FET gate voltage output enable. The wait time is required at transition from power-up, and please refer to the “■ Timing diagram” mentioned later for details.
”FET ON state” is the state in which each FET gate voltage is asserted by a relevant pin actually. Please refer to “■ electrical characteristic” about rise and fall time of gate voltage.

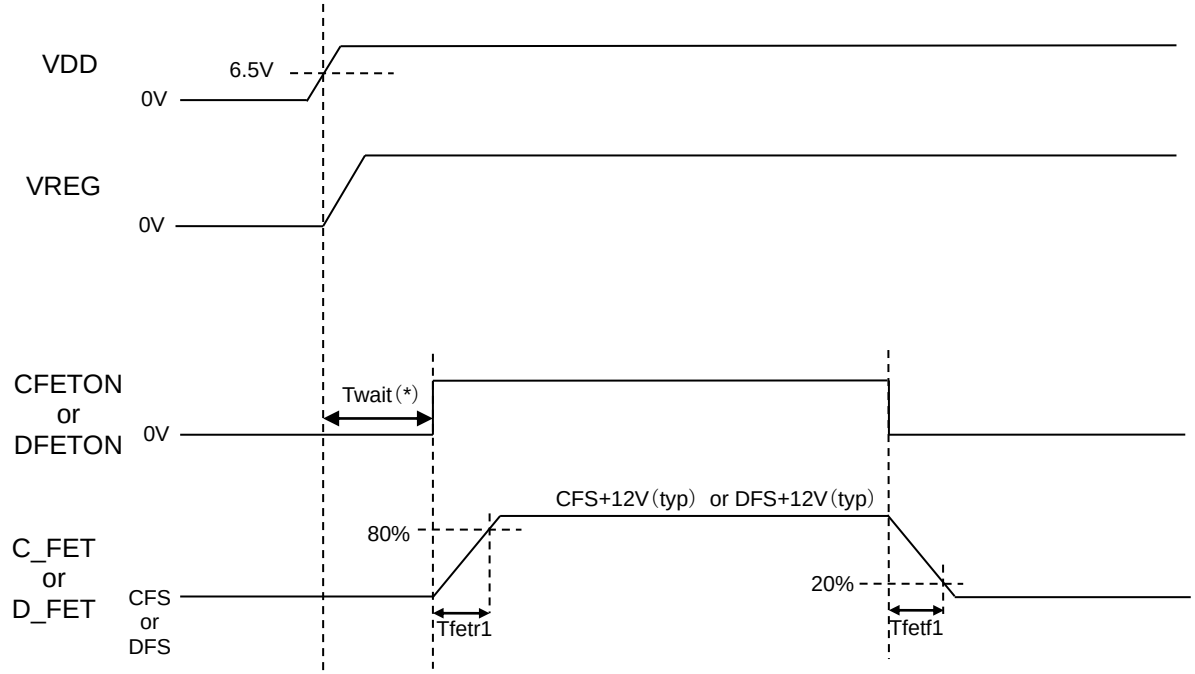
Input			ML5810A Operating status
PCFETON	DFETON	CFETON	
0	0	0	Charge pump ON, FET stand-by
More than one is ”1”			FET ON

C_FET and D_FET can be turn on at the same time, but PC_FET is exclusively other FETs and can’t be turn on at the same time. A truth table of FET ON/OFF is following. As it's shown on the table, CFETON, DFETON is priority more than PCFETON .

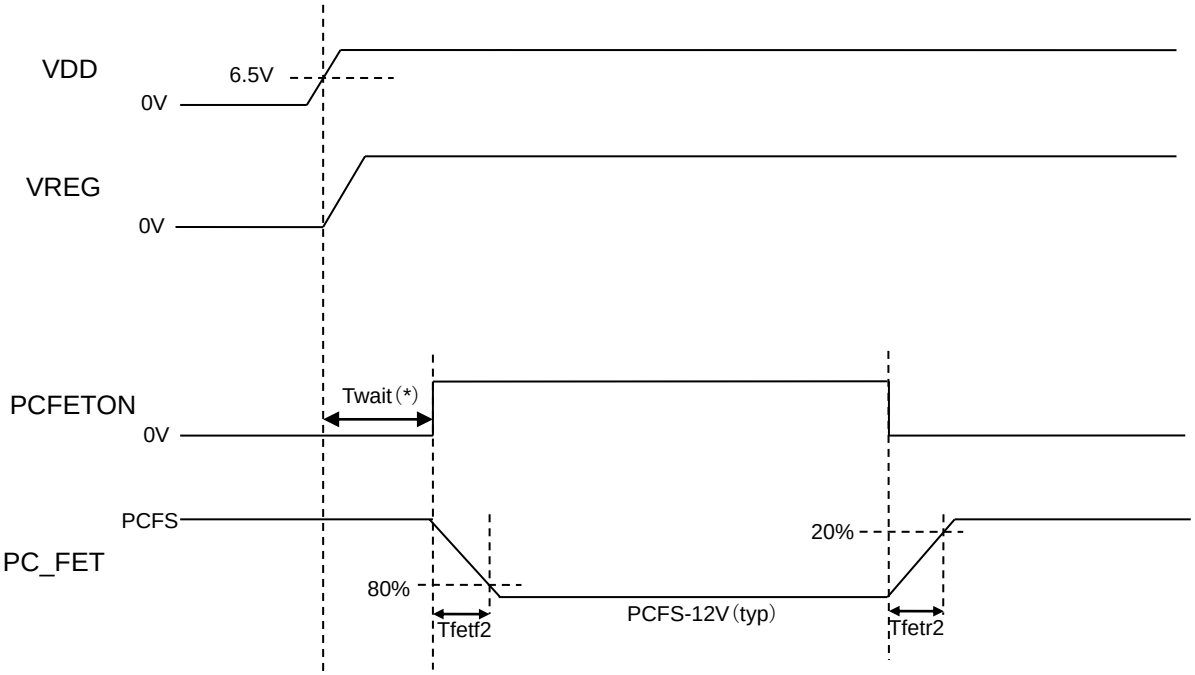
Input			Output		
PCFETON	DFETON	CFETON	PC_FET	D_FET	C_FET
0	0	0	OFF	OFF	OFF
0 or 1	0	1	OFF	OFF	**ON**
0 or 1	1	0	OFF	**ON**	OFF
0 or 1	1	1	OFF	**ON**	**ON**
1	0	0	**ON**	OFF	OFF

■Timing diagram

C_FET / D_FET timing

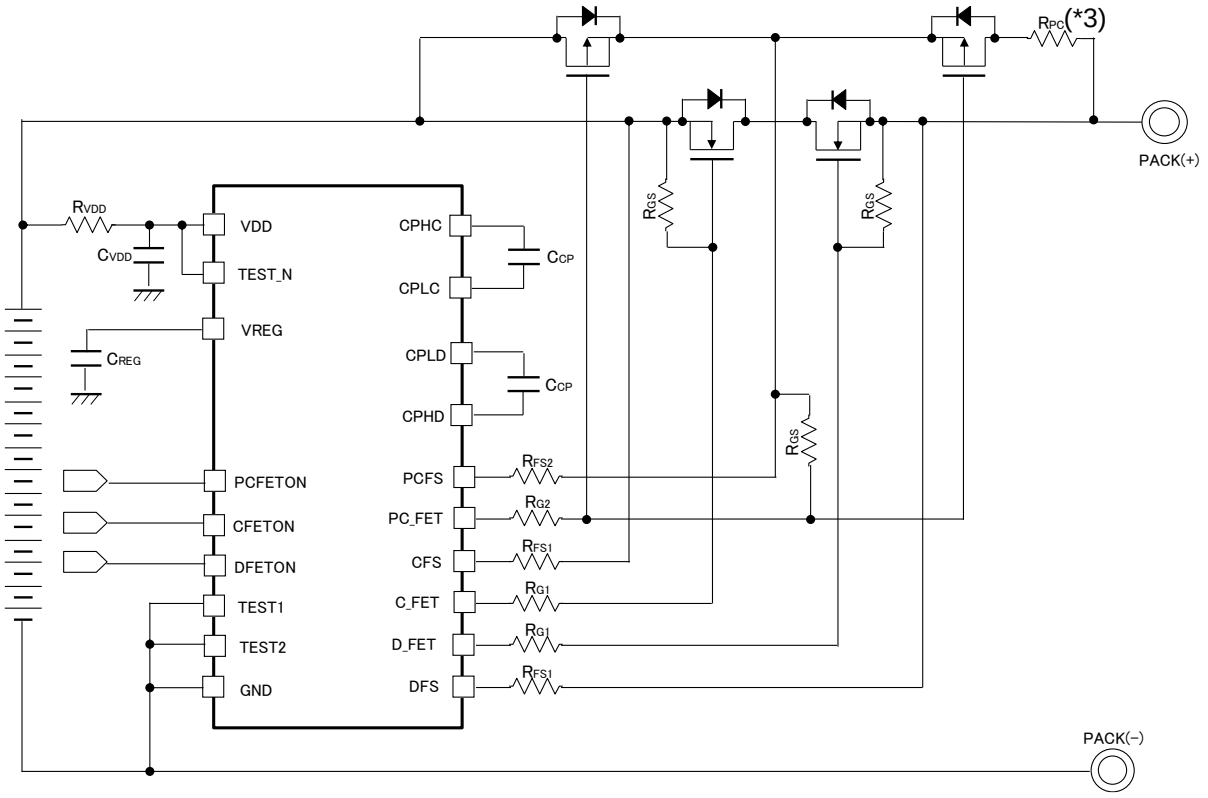


PC_FET timing



(*) Twait must be more than 50ms, when CFETON, DFETON, and PCFETON are set to H from L (0v).

■Application Circuit Example



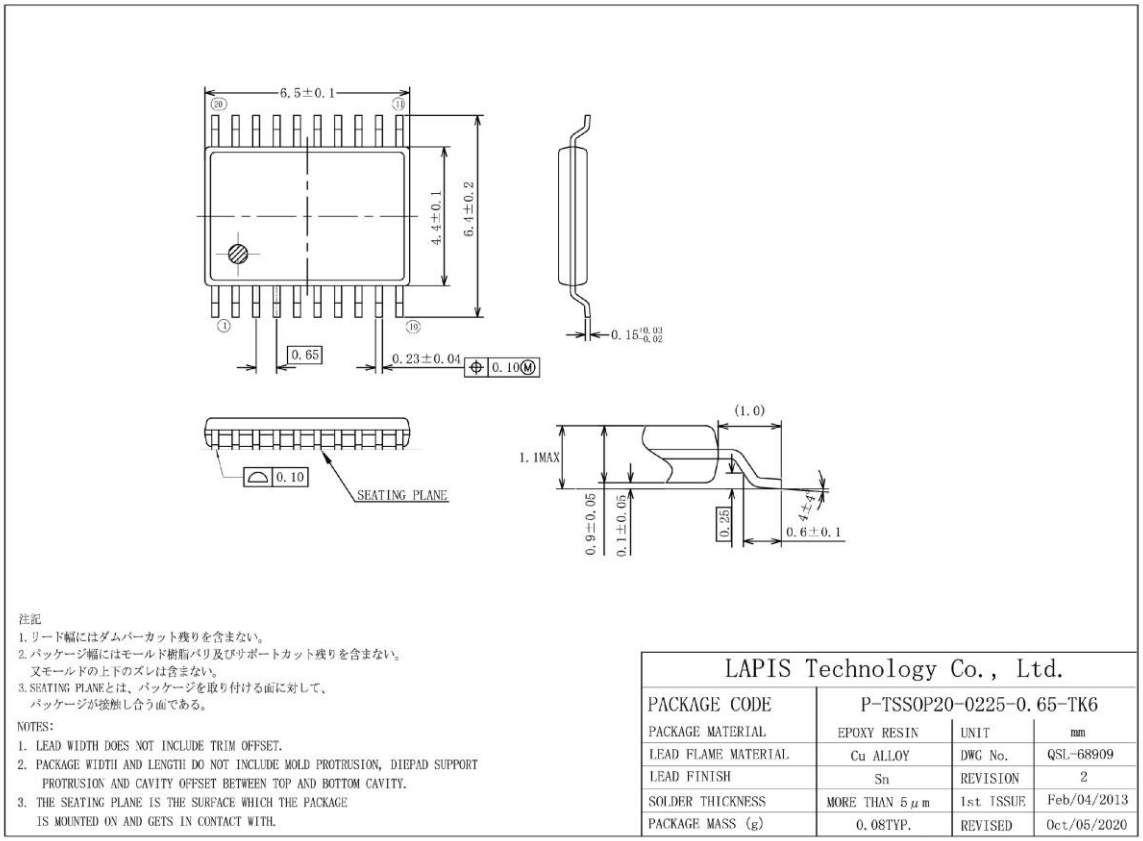
Recommended Values for External Components

Component	Recommended value
R_{VDD} (*1)	510Ω to 1.5kΩ
C_{VDD}	2.2μF to 10μF
C_{REG}	4.7μF
R_{G1}	1kΩ
R_{FS1}	100Ω
R_{G2}	1kΩ
R_{FS2}	1kΩ
R_{GS}	10MΩ
C_{CP}	82nF (*2)

(*1) Recommended R_{VDD}=1.5kΩ for C_{VDD}=2.2μF.
(*2) Set 80nF to 100nF, when gate capacitance of external Nch-FET is 10nF.
Set about 8-times of gate capacitance of external Nch-FET to C_{CP}.
(*3) Set R_{PC} according to current of Pch-FET.

Notice: Example of application circuit and the recommended values to parts list shall not guarantee performance under all conditions. Full and detailed tests are suggested on your actual application.

■ Package Dimensions



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TSSOP20-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68909
LEAD FINISH	Sn	REVISION	2
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.08TYP.	REVISED	Oct/05/2020

Causion regarding surface mount type packages

Surface mount type packages are susceptible to applied heat in solder reflow or moisture absorption during storage. Please contact your local ROHM sales representative for the recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

■ Revision History

Document No.	Issue date	Page		Descriptions
		Previous	New	
Version-02	2019.07.18	—	—	English version first edition issued
Version-03	2019.07.19	3	3	Error in writing corrected
Version-03	2019.07.25	5,10	5,10	Error in writing corrected
Version-04	2020.06.05	3	3	Error in Pin Configuration corrected (pin 2,8,15,16)
Version-04	2020.06.05	10	10	■Application Circuit Example Added TEST1, TEST2, TEST_N pin.
Version-05	2020.10.30	—	—	Changed Company name and “notes” page.
Version-06	2023.06.09	11	11	Changed "Package Dimensions".
Version-07	Jan. 9, 2024	1	1	Add Application Part number
		13	13	Add Notes

Notes

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