Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

FEDL5239-07

January 9, 2024

ML5239

Analog Front-End IC for 16-Serial-Cell Lithium-Ion Secondary Battery Protection

■ General Description

ML5239 is a power voltage monitoring IC for 5 to 16-cell lithium-ion secondary battery pack. It can be connected in multi-stage series to monitor the voltage of more than 17-cell lithium-ion battery.
It also has a pin for driving an external cell balance FET, enabling to control the balance for each battery cell.

■ Features

- 5 to 16 cell voltage measurement function
  Built-in 12-bit successive approximation type ADC
  Cell voltage measurement precision: ±10mV at 25°C, cell voltage 3.6V
- Cell voltage measurement time:1ms (typ)/cell
- Open/short detection function of cell voltage measurement pin
- Multi-stage series IC-IC communication function
  MCU interface: SPI serial interface
  CRC communication error detection
- SPI communication speed = 500kHz (max) at four-stage configuration
  Multi-stage connection ICs: 16 (max)
- Cell balance FET driving pin
- Temperature sensor input: 4 channels
- Current consumption
  Cell voltage measurement state: 1.2mA (typ), 2.4mA (max)
  Power-down state: 0.1µA (typ), 1µA (max)
- Power supply voltages: 10 to 72V
- Operational temperature: -40 to 85°C
- Package: 64-pin plastic TQFP

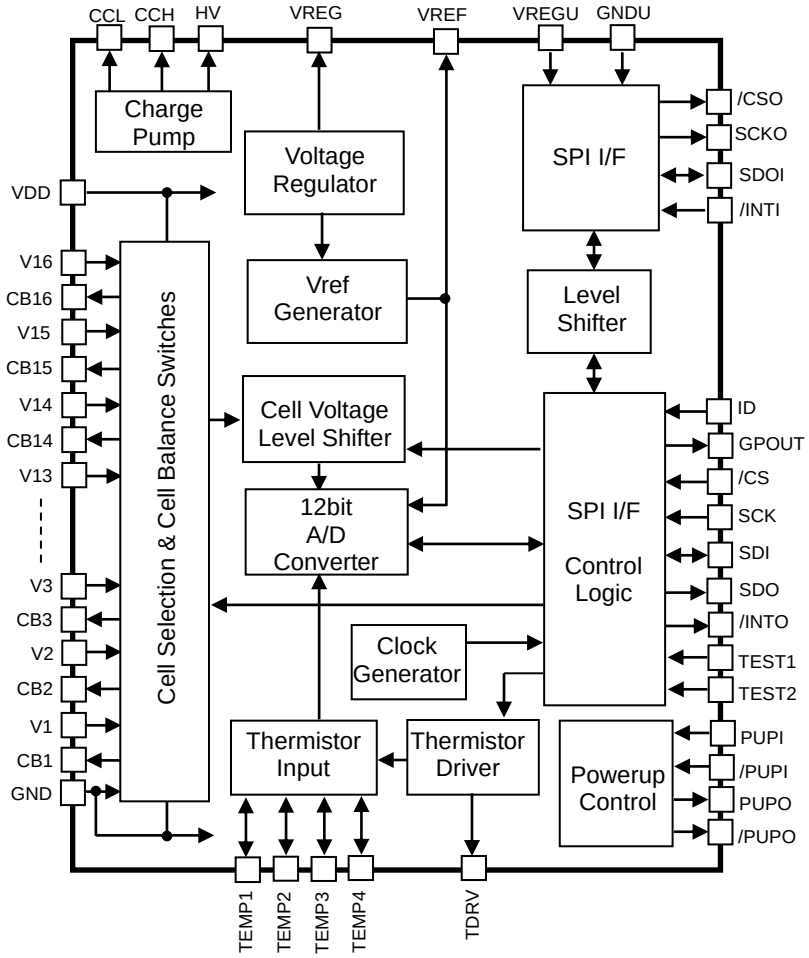
■ Application

・Power tools and Garden tools
・E-Bike and Electric assisted bicycle
・Uninterruptible Power Supplies (UPS)
・Energy Storage Systems (ESS)

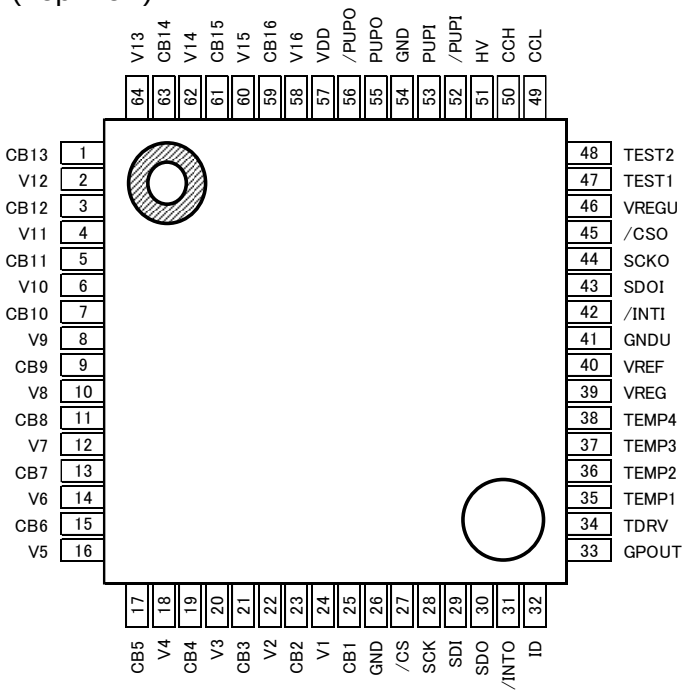
■ Part number

ML5239TB

■ Block Diagram



■ Pin Configuration (Top View)



■ Pin Description

Pin No.	Pin name	I/O	Description
1	CB13	O	Battery cell 13 cell balance control output pin.
2	V12	I	Battery cell 13 low voltage input and Battery cell 12 high voltage input pins. If the number of connected battery cells is in the range of 5 to 11, input the same potential as the highest V pin (V5 to V11) of the battery connected to the IC.
3	CB12	O	Battery cell 12 cell balance control output pin.
4	V11	I	Battery cell 12 low voltage input and Battery cell 11 high voltage input pins. If the number of connected battery cells is in the range of 5 to 10, input the same potential as the highest V pin (V5 to V10) of the battery connected to the IC.
5	CB11	O	Battery cell 11 cell balance control output pin.
6	V10	I	Battery cell 11 low voltage input and Battery cell 10 high voltage input pins. If the number of connected battery cells is in the range of 5 to 9, input the same potential as the highest V pin (V5 to V9) of the battery connected to the IC.
7	CB10	O	Battery cell 10 cell balance control output pin.
8	V9	I	Battery cell 10 low voltage input and Battery cell 9 high voltage input pins. If the number of connected battery cells is in the range of 5 to 8, input the same potential as the highest V pin (V5 to V8) of the battery connected to the IC.
9	CB9	O	Battery cell 9 cell balance control output pin.
10	V8	I	Battery cell 9 low voltage input and Battery cell 8 high voltage input pins. If the number of connected battery cells is in the range of 5 to 7, input the same potential as the highest V pin (V5 to V7) of the battery connected to the IC.
11	CB8	O	Battery cell 8 cell balance control output pin.
12	V7	I	Battery cell 8 low voltage input and Battery cell 7 high voltage input pins. If the number of connected battery cells is in the range of 5 to 6, input the same potential as the highest V pin (V5 to V6) of the battery connected to the IC.
13	CB7	O	Battery cell 7 cell balance control output pin.
14	V6	I	Battery cell 7 low voltage input and Battery cell 6 high voltage input pin. If the number of connected battery cells is in the range of 5, input the same potential as the highest V pin (V5) of the battery connected to the IC.
15	CB6	O	Battery cell 6 cell balance control output pin.
16	V5	I	Battery cell 6 low voltage input and Battery cell 5 high voltage input pins.
17	CB5	O	Battery cell 5 cell balance control output pin.
18	V4	I	Battery cell 5 low voltage input and Battery cell 4 high voltage input pins.
19	CB4	O	Battery cell 4 cell balance control output pin.
20	V3	I	Battery cell 4 low voltage input and Battery cell 3 high voltage input pins.
21	CB3	O	Battery cell 3 cell balance control output pin.
22	V2	I	Battery cell 3 low voltage input and Battery cell 2 high voltage input pins.
23	CB2	O	Battery cell 2 cell balance control output pin.
24	V1	I	Battery cell 2 low voltage input and Battery cell 1 high voltage input pins.
25	CB1	O	Battery cell 1 cell balance control output pin.
26	GND	—	These are ground pins.

Pin No.	Pin name	I/O	Description
27	/CS	I	SPI interface chip select pin. The SPI interface is active if the input is "L" level. Be sure to input "H" level when completing one data write/read operation.
28	SCK	I	SPI interface clock input pin. Capture the SDI input into the LSI at the rising edge of the SCK clock. Output the data from the SDO pin or SDI pin at the falling edge of the SCK.
29	SDI	IO	SPI interface data input pin. It is data I/O pin for upper IC in multi-stage connection.
30	SDO	O	SPI interface data output pin. If /CS input is in "H" level, output of this pin is Hi-Z state.
31	/INTO	O	Interrupt signal output to an external MCU. This pin is an NMOS open drain output pin and outputs "L" level if interrupted.
32	ID	I	ID identification pin at multi-stage connection. Set it to the GND level without multi-stage connection or for the lowest IC connected with the external MCU. Set it to the VREG level of the IC at multi-stage connection for ICs other than the lowest one.
33	GPOUT	O	General output pin. This pin has an NMOS open drain output.
34	TDRV	O	Ground pin for thermistor. Set this to 0V output during temperature measurement or to be the Hi-Z state otherwise. This pin has an NMOS open drain output.
35	TEMP1	IO	Temperature measurement thermistor connection pin. Connect an NTC thermistor between this pin and the TDRV pin and a resistor between this pin and the VREG pin. This can be switched to general output by the register setting.
36	TEMP2	IO	
37	TEMP3	IO	
38	TEMP4	IO	
39	VREG	O	Built-in 5.3V regulator output pin. Connect a 1μF capacitor between this pin and GND. Power supply for IC internal circuit.
40	VREF	O	Reference voltage output pin for the built-in ADC. Connect a 1μF capacitor between this pin and GND.
41	GNDU	—	GND pin for the communication circuit with a higher IC at multi-stage connection. Connect to the GND pin of the higher IC via a resistor. Connect to the VDD pin without a higher IC.
42	/INTI	I	Interrupt signal input pin from a higher IC at multi-stage connection. Connect to the /INTO pin of the higher IC via a resistor. It has a built-in 100kΩ pull-up resistor between this pin and the VREGU pin. Set this to the open state without a higher IC.
43	SDOI	IO	Data I/O pin of the SPI interface with a higher IC at multi-stage connection. Connect to the SDI pin of the higher IC via a resistor. Set this to the open state without a higher IC.
44	SCKO	O	Serial clock output pin of the SPI interface with a higher IC at multi-stage connection. Connect to the SCK pin of the higher IC via a resistor. Set this to the open state without a higher IC.
45	/CSO	O	Chip select output pin of the SPI interface with a higher IC at multi-stage connection. Connect to the /CS pin of the higher IC via a resistor. Set this to the open state without a higher IC.
46	VREGU	—	Power supply pin for the communication circuit with a higher IC at multi-stage connection. Connect to the VREG pin of the higher IC via a resistor. Connect to the VDD pin without a higher IC.
47	TEST1	I	LSI test input pin. Fix to GND level.

Pin No.	Pin name	I/O	Description
48	TEST2	I	It has a built-in 1MΩ (typ) pull-down resistor in the LSI.
49	CCL	O	Connection pin of capacitor for the internal voltage multiplier circuit. Connect a capacitor of 0.22μF between this pin and the CCH pin of this IC.
50	CCH	O	Connection pin of capacitor for the internal voltage multiplier circuit. Connect a capacitor of 0.22μF between this pin and the CCL pin of this IC.
51	HV	O	Pin for smoothing multiplied voltage. Connect a capacitor of 0.22μF between this pin and the VDD pin of this IC.
52	/PUPI	I	Power-up trigger signal input pin (reverse phase). The "L" pulse input moves the state from power-down to power-up. Set it to the GND level without multi-stage connection or for the lowest IC connected with the external MCU.
53	PUPI	I	Power-up trigger signal input pin (normal phase). The "H" pulse input moves the state from power-down to power-up.
54	GND	—	These are ground pins.
55	PUPO	O	Power-up trigger signal output pin (normal phase). Connect to the PUPI pin of a higher IC via a resistor at multi-phase connection. Set this to the open state without a higher IC.
56	/PUPO	O	Power-up trigger signal output pin (reverse phase). Connect to the /PUPI pin of a higher IC via a resistor at multi-phase connection. Set this to the open state without a higher IC.
57	VDD	—	Power supply input pin. Connect an external CR filter for noise rejection.
58	V16	I	Battery cell 16 high voltage input pin. If the number of connected battery cells is in the range of 5 to 15, input the same potential as the highest V pin (V5 to V15) of the battery connected to the IC.
59	CB16	O	Battery cell 16 cell balance control output pin.
60	V15	I	Battery cell 16 low voltage input and Battery cell 15 high voltage input pins. If the number of connected battery cells is in the range of 5 to 14, input the same potential as the highest V pin (V5 to V14) of the battery connected to the IC.
61	CB15	O	Battery cell 15 cell balance control output pin.
62	V14	I	Battery cell 15 low voltage input and Battery cell 14 high voltage input pins. If the number of connected battery cells is in the range of 5 to 13, input the same potential as the highest V pin (V5 to V13) of the battery connected to the IC.
63	CB14	O	Battery cell 14 cell balance control output pin.
64	V13	I	Battery cell 14 low voltage input and Battery cell 13 high voltage input pins. If the number of connected battery cells is in the range of 5 to 12, input the same potential as the highest V pin (V5 to V12) of the battery connected to the IC.

■ Absolute Maximum Ratings

(GND= 0V, Ta = 25°C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Potential difference between VDD, VREGU, GNDU, and HV	-0.3 to +86.5	V
	V_{REG}	Potential difference between	-0.3 to +6.5	V
	V_{REGU}	Potential difference between	-0.3 to +6.5	V
Input voltage	V_{IN1}	Applied to V1 to V16, TEST1, and TEST2 pins	-0.3 to V_{DD}+0.3	V
	V_{IN2}	Applied to /CS, SCK, SDI, TEMP1 to TEMP4, and ID pins	-0.3 to V_{REG}+0.3	V
	V_{IN3}	Potential difference between SDOI and /INTI pins and GNDU pin	-0.3 to V_{REGU}+0.3	V
	V_{IN4}	Applied to PUPI and /PUPI pins	-0.5 to V_{DD}+0.3	V
Short-circuit output current	I_{OS}	VDD=50V, Applied to VREG, VREF, SDI, SDO, /INTO, GPOUT, PUPO, /PUPO, SDOI, /CSO, SCKO, TDRV, and TEMP1 to TEMP4 pins	20	mA
Power dissipation	P_D	Ta=25°C	3.6	W
Storage	T_{STG}	—	-50 to +150	°C

■ Recommended Operating Conditions

(GND= 0V)

Item	Symbol	Condition	Range	Unit
Supply voltage	V_{DD}	Applied to VDD pin	10 to 72	V
	V_{REGU}	Potential difference between VREGU and GNDU pins (if there is upper IC)	5.1 to 5.5	V
Operational temperature	Ta	No VREG output load	-40 to +85	°C

■ Electrical Characteristics

● DC Characteristics

V_{DD} = 10 to 72V, VREGU-GNDU = 5.1 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital "H" input voltage (Note 1)	V_{IH}	—	0.8×V_{REG}	—	V_{REG}	V
Digital "L" input voltage (Note 1)	V_{IL}	—	0	—	0.2×V_{REG}	V
Digital "H" input voltage (Note 2)	V_{IHU}	GNDU pin reference	0.8×V_{REGU}	—	V_{REGU}	V
Digital "L" input voltage (Note 2)	V_{ILU}	GNDU pin reference	0	—	0.2×V_{REGU}	V
PUPI and /PUPI pins "H" input voltage	V_{IHP}	—	3.6	—	VDD	V
PUPI and /PUPI pins "L" input voltage	V_{ILP}	—	0	—	0.7	V
Digital "H" input current (Note 1)	I_{IH}	V_{IH} = V_{REG}	—	—	2	µA
Digital "L" input current (Note 1)	I_{IL}	V_{IL} = GND	–2	—	—	µA
Digital "H" input current (Note 2)	I_{IHU}	V_{IH} = V_{REGU}	—	—	2	µA
SDOI pin "L" input current	I_{ILU}	V_{IL} = GNDU	–2	—	—	µA
/INTI pin "L" input current	I_{ILU}	V_{REGU}=5.3V, V_{IL} = GNDU	–106	-53	-26	µA
PUPI and /PUPI pins "H" input current	I_{IHP}	V_{IH} = 5V	—	—	2	µA
PUPI and /PUPI pins "L" input current	I_{ILP}	V_{IL} = GND	–2	—	—	µA
Digital "H" output voltage (Note 3)	V_{OH}	I_{OH}=-100µA	V_{REG}-0.2	—	V_{REG}	V
Digital "L" output voltage (Note 4)	V_{OL}	I_{OL}=1mA	0	—	0.2	V
Digital "H" output voltage (Note 5)	V_{OHU}	I_{OH}=-100µA GNDU pin reference	V_{REGU}-0.2	—	V_{REGU}	V
Digital "L" output voltage (Note 5)	V_{OLU}	I_{OL}=1mA GNDU pin reference	0	—	0.4	V
PUPO and /PUPO pins "H" output voltage	V_{OHP}	I_{OH}=-50µA VDD pin reference	V_{HV}-0.2	—	V_{HV}	V
PUPO and /PUPO pins "L" output voltage	V_{OLP}	I_{OL}=50µA VDD pin reference	0	—	0.4	V
Digital output leakage current (*6)	I_{OLK}	V_{OH}=V_{REG}, V_{OL}=0V	–2	—	2	µA
VREG output voltage	V_{REG}	10V < V_{DD} pin voltage < 72V Output load current < 1.5mA	5.1	5.3	5.5	V
VREF output voltage	V_{REF1}	Output load current < 0.1µA	4.68	4.7	4.72	V
HV pin output voltage range	V_{HV}	VDD pin reference	3.3	—	5.5	V
CB pin output resistor	R_{CB}	—	50	100	220	kΩ
CB pin output voltage	V_{CB}	Applied to CBn pin n=1 to 16	Vn-1	—	Vn	V
VREG dropping detection voltage	V_{RGD}	—	4.0	4.3	4.6	V
VREG return detection voltage	V_{RGR}	—	4.3	4.7	5.1	V

Note 1: Applied to /CS, SCK, SDI, and ID pins.
Note 2: Applied to SDOI and /INTI pins.
Note 3: Applied to SDO, SDI, and TEMP1 to TEMP4 pins.
Note 4: Applied to SDO, /INTO, GPOUT, SDI, and TEMP1 to TEMP4 pins.
Note 5: Applied to /CSO, SCKO, and SDOI pins.
Note 6: Applied to SDO, /INTO, and GPOUT pins.

- Supply Current Characteristics

V_{DD} = 10 to 72V, GND = 0V, Ta = -40 to +85°C, no VREG and VREF output load.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell voltage measuring state supply current (Note 1)	I_{DD1}	Scan measurement VREGU=GNDU=VDD	—	1.2	2.4	mA
Power-down supply current (Note 1)	I_{DDS}	VREGU=GNDU=VDD	—	0.1	1.0	µA
VREGU power supply current	I_{REGU}	At multi-stage connection VREGU-GNDU=5.3V	—	250	500	µA

(Note 1) This is defined by total current flowing into the VDD and VREGU pins without multi-stage connection.

- Cell Voltage Measurement Characteristics

V_{DD} = 10 to 72V, GND = 0V, Ta = -40 to +85°C, no VREG output load.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Cell monitoring pin input current	I_{INVC}	Cell voltage being measured	-1	—	1	µA
Cell monitoring pin input leakage current	I_{ILVC}	Cell voltage not being measured	-1	—	1	µA
Cell voltage measurement error	V_{CERT}	Each cell voltage = 3.6V Ta= 25°C	-10	—	10	mV
	V_{CER}	Each cell voltage = 1 to 4.3V Ta=-10 to 60°C	-25	—	25	mV
Measurement resolution	V_{LSB}	—	—	5000/4095	—	mV
Cell voltage measurement time	t_{SCAN}	16-cell scan measurement	7.0	8.3	10.0	ms
	t_{SEL}	Select measurement	0.8	1	1.2	ms

- Temperature Sensor Input Measurement Characteristics

V_{DD} = 10 to 72V, GND = 0V, Ta = -40 to +85°C, no VREG output load.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
TEMP1 - TEMP4 pins input current	I_{TEMP}	TEMP input = 0.4 to 4.5V	-2	—	2	µA
TDRV pin "L" output voltage	V_{OLT}	TDRV bit = "0" I_{OL}=1mA	0	—	0.1	V
TDRV pin output leakage current	I_{TDRV}	TDRV bit = "1" TDRV pin voltage=0 to 3V	-2	—	2	µA
TEMP pin input voltage measurement error	V_{TER}	TEMP input = 0.4 to 4.5V Ta=-10 to 60°C	-20	—	20	mV
Measurement resolution	V_{LSB}	—	—	4700/4095	—	mV
Temperature measurement time	t_{SCAN}	4 temperature scan measurement	1.9	2.3	2.7	ms
	t_{SEL}	Select measurement	0.8	1	1.2	ms

- AC Characteristics

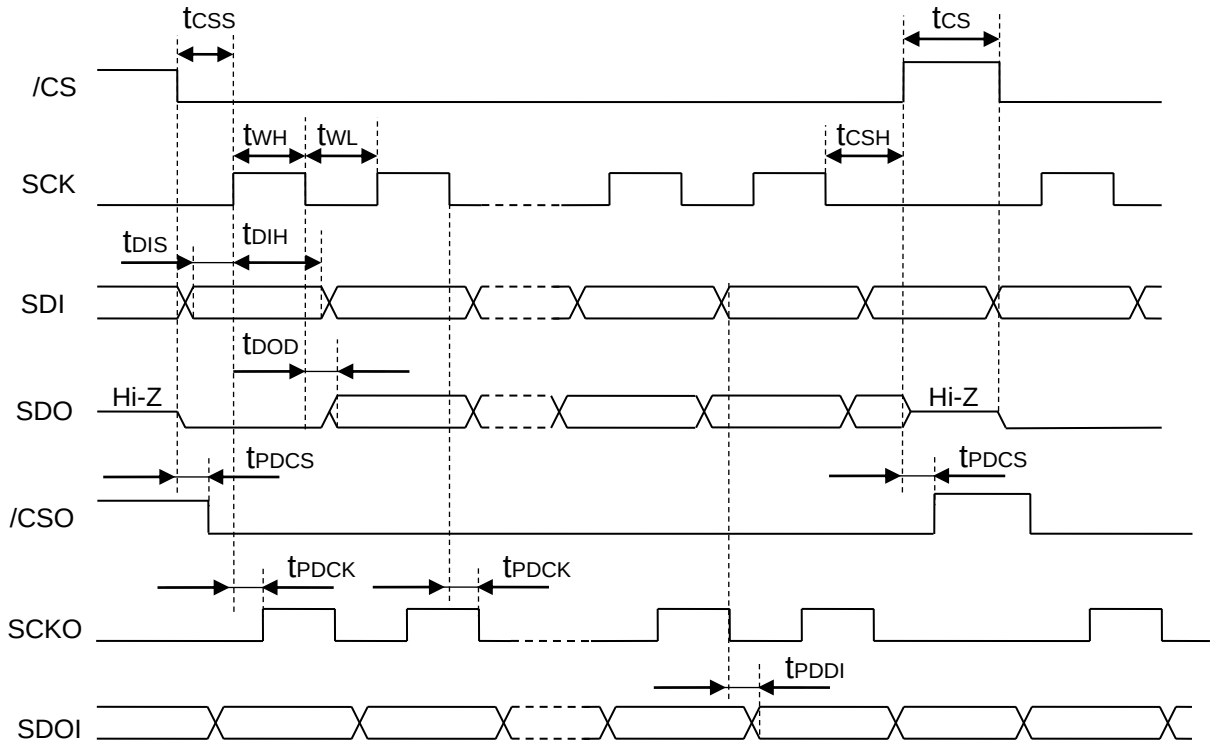
V_{DD} = 10 to 72V, VREGU-GNDU = 5.1 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SPI communication speed	fck	operating at 4 or less-stage configuration(Note1)	100	—	500	kHz
SPI communication speed (ID Automatic Setting)	fckid	operating at 2 to 16 stage configuration(Note1)	500	—	650	kHz
/CS-SCK setup time	t_{CSS}	operating at 4 or less-stage configuration(Note1)	1000	—	—	ns
SCK-/CS hold time	t_{CSH}		1000	—	—	ns
SCK "H" pulse width	t_{WH}		950	—	—	ns
SCK "L" pulse width	t_{WL}		950	—	—	ns
SCK-SDI setup time	t_{DIS}		200	—	—	ns
SCK-SDI hold time	t_{DIH}		200	—	—	ns
SCK-SDO output delay time	t_{DOD}		—	—	700	ns
/CS "H" pulse width	t_{CS}		2	—	—	µs
/CS-/CSO output delay time	t_{PDCS}		—	—	100	ns
SCK-SCKO output delay time	t_{PDCK}		—	—	100	ns
SDI-SDOI output delay time	t_{PDDI}		—	—	115	ns
/CSO and SCKO output delay time difference	$\lvert t_{PDCS}-t_{PDCK}\rvert$		0	—	15	ns
SCKO and SDOI output delay time difference	$\lvert t_{PDDI}-t_{PDCK}\rvert$		10	—	35	ns
SDOI-SDO output delay time	t_{PDDO}		—	—	115	ns

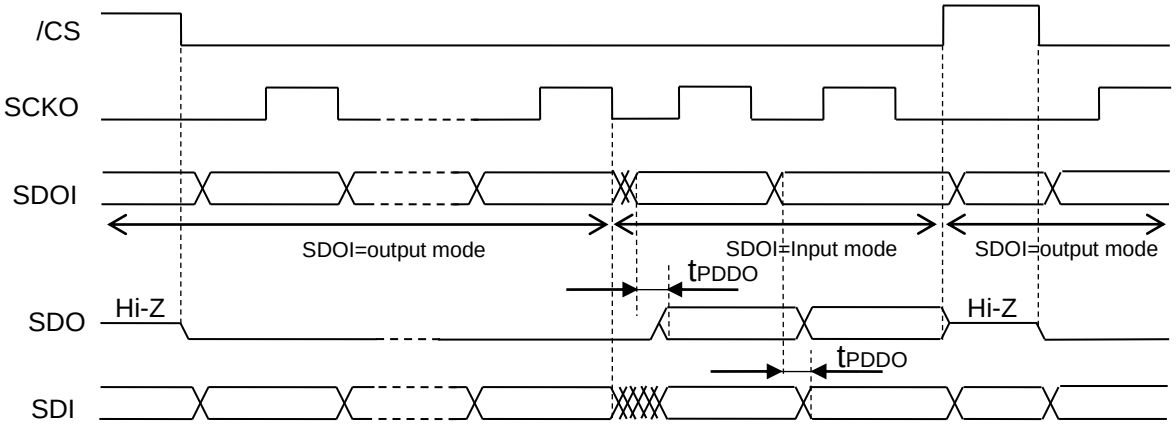
Note1: This product is recommended to communicate on the same board for multi-stage series connection. IC-IC transmission delay time is assumed to be less than 10ns.

R_{SPI}=100Ω to 330Ω, R_{VREGU}=100Ω to 330Ω, R_{GNDU}=100Ω to 330Ω, C_{REGU}=10nF to 1.0uF

Timing diagram at data write



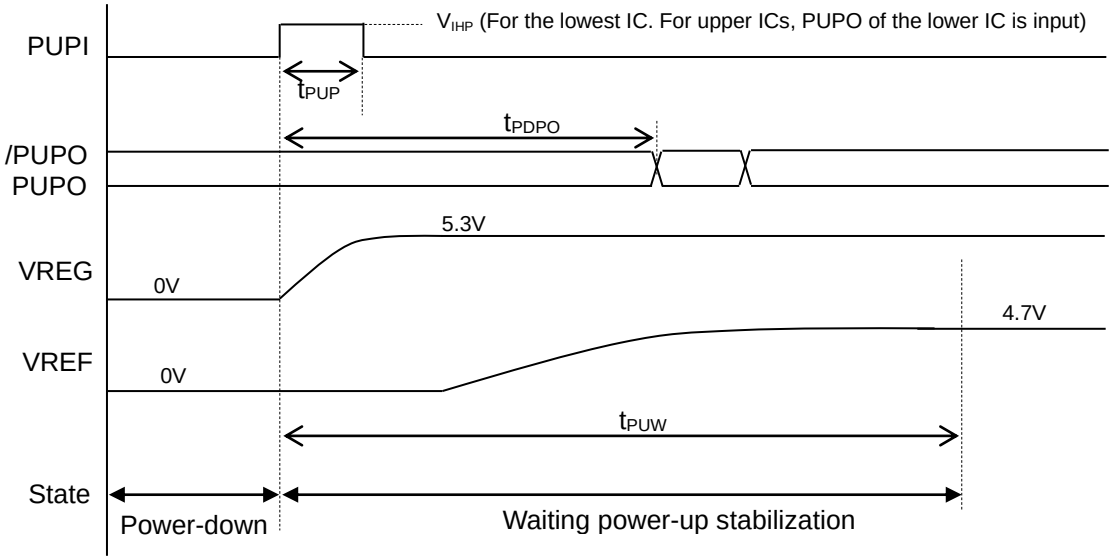
Timing diagram at multi-stage connection



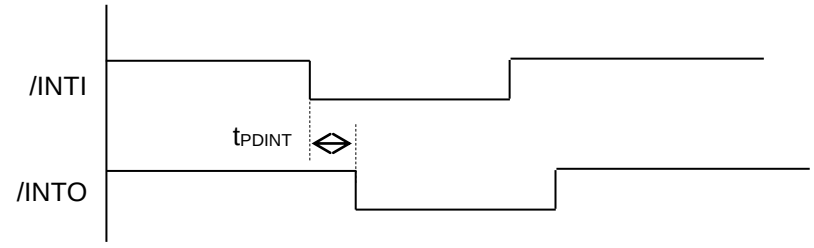
V_{DD} = 10 to 72V, VREGU-GNDU = 5.1 to 5.5V, GND = 0V, Ta = -40 to +85°C, no VREG output load.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
PUPI "H" pulse width	t_{PUP}	—	6.0	—	—	µs
PUPI-PUPO output delay time	t_{PDPO}	—	—	5	10	ms
Power-up waiting time	t_{PUW}	—	20	—	—	ms
/INTI- /INTO output delay time	t_{PDINT}	—	—	—	1	µs

Power-up operation timing diagram



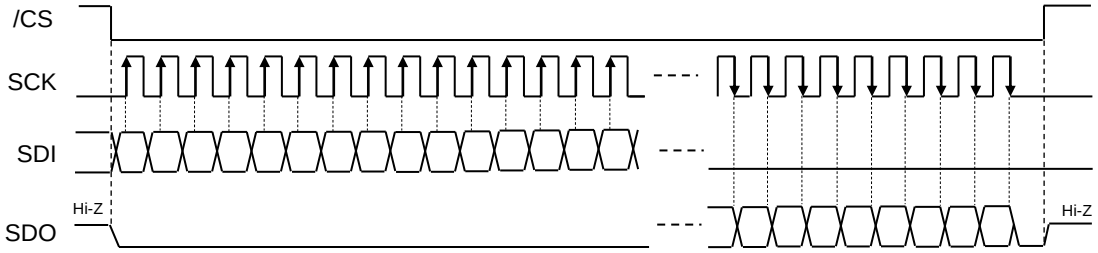
Interrupt output timing diagram



■ Functional Description

● MCU Interface

The ML5239 is equipped with the SPI interface.
The SPI interface is enabled by setting the /CS pin to the "L" level. It imports the SDI pin data into the LSI in synchronization with the SCK pin clock rise. It outputs the read data to the SDO pin in synchronization with the SCK pin clock fall. The SPI interface is disabled by setting the /CS pin to the "H" level to return to the initial state. Always set the /CS pin to the "H" level every time one data write/read operation completes.



The communication format consists of the control register address, access mode/ID data, write data/read data, and CRC code, all in 8 bits (1 byte) with MSB first.
Data write operation is performed in one byte.
One data read operation can read data from successive addresses.

Communication format at data write

Register address	Access mode	Write data (8 bit)	CRC code (8 bit)

Communication format at data read

Register address	Access mode	Number of data bytes	Read data 1 (8 bit)	Read data 2 (8 bit)	-----	CRC code (8 bit)

Access mode/ID data

The following table shows the configuration.

	7	6	5	4	3	2	1	0
Bit name	RD/WR	WR_ALL	—	—	ID3	ID2	ID1	ID0

The ID address of an IC in multi-stage connection is specified by ID0 to ID3 bits. Each ID at 16-stages connection is shown in the following table.

ID3	ID2	ID1	ID0	Multi-stage connection order
0	0	0	0	Lowest IC
0	0	0	1	2nd lowest IC
0	0	1	0	3rd lowest IC
:				:
1	1	0	1	14th lowest IC
1	1	1	0	15th lowest IC
1	1	1	1	16th lowest IC

A data write operation can be performed for all the ICs in multi-stage connection using WR_ALL bit. At read operation, the WR_ALL bit is ignored, and data is read from the specified IC.

WR_ALL	Accessed IC
0	IC specified using the ID0 to ID3 bits
1	All ICs in multi-stage connection

The access mode of read/write is selected using the RD/WR bit.

RD/WR	Access mode
0	Write
1	Read

Number of data bytes

The following table shows the configuration.

	7	6	5	4	3	2	1	0
Bit name	—	—	—	DB4	DB3	DB2	DB1	DB0

The number of bytes of read data is specified using the DB0 to DB4 bits. "Number of read data bytes - 1" should be set. If only one byte is read, "0" should be specified. Up to 32 bytes can be read successively.

CRC calculation

This IC is equipped with the 8-bit CRC calculation circuit to detect any communication error, and it appends a CRC (Cycle Redundancy Code) generated using a polynomial X^8+X^2+X+1 to each communication data. It is calculated from all of the address to write/read data, and the result is generated in MSB first. (It includes the empty bits 4 and 5 of the access mode/ID data and 5 to 7 of the number of data bytes.) When the /CS pin is set to "H" level, the CRC calculation is initialized, and the initial value is set to FF [h].
The data write operation is performed on the specified register only when the CRC computation result matches the received CRC code. Otherwise, the data write operation is not performed. When a CRC error is detected, the CRC error flag is set, allowing the interrupt signal to the external MCU to be output to the /INTO pin. For details, refer to the INT_EN and INT_REQ registers of the control register.
The CRC computation is also performed for each transmit/receive data during data read operation to output the result at the end of the read data. The external MCU can detect any communication error by comparing the CRC computation result and the received CRC code.

- Control Register

The control register map is shown below.
* Note: The initial value of the INT_REQ register is value after software reset.

Address	Register name	R/W	Initial value	Description
00H	NOOP	R/W	55H	Register for user
01H	RSTREQ	W	00H	Software reset request register
02H	INT_EN	R/W	80H	Interrupt enable register
03H	INT_REQ	R/W	00H *	Interrupt request register
04H	PDACP	W	00H	Power-down code acceptor
05H	POWER	R/W	00H	Power-down control register
06H	MEAS_VCELL	R/W	00H	Cell voltage measurement control register
07H	MEAS_TEMP	R/W	00H	Temperature sensor measurement control register
08H	MEAS_VREG	R/W	00H	VREG voltage measurement control register
09H	MEAS_VOPSH	R/W	00H	Open/short detection measurement control register
0AH	STATUS	R	00H	Status register
0BH	STAT_VML	R	00H	Cell voltage measurement status (lower eight cells)
0CH	STAT_VMH	R	00H	Cell voltage measurement status (higher eight cells)
0DH	STAT_TM	R	00H	Temperature sensor measurement status
0EH	CBALL	R/W	00H	Cell balancing control register (lower eight cells)
0FH	CBALH	R/W	00H	Cell balancing control register (higher eight cells)
10H	IDSEL	R	00H	ID storing register
11H	IDACP	W	00H	ID automatic setting code acceptor
12H	IDREG	R/W	00H	ID automatic setting register
13H	WDTACP	W	00H	WDT setting acceptor
14H	SETWDT	R/W	00H	WDT setting register
15H	SELOUT	R/W	00H	Pin switch register
16H	SETOUT	R/W	09H	Pin output setting register
17H to 1FH	RSVD	R	00H	Reserved register
20H	VCELL1L	R	00H	Cell 1 measurement result register (lower byte)
21H	VCELL1H	R	00H	Cell 1 measurement result register (higher byte)
22H	VCELL2L	R	00H	Cell 2 measurement result register (lower byte)
23H	VCELL2H	R	00H	Cell 2 measurement result register (higher byte)
24H	VCELL3L	R	00H	Cell 3 measurement result register (lower byte)
25H	VCELL3H	R	00H	Cell 3 measurement result register (higher byte)
26H	VCELL4L	R	00H	Cell 4 measurement result register (lower byte)
27H	VCELL4H	R	00H	Cell 4 measurement result register (higher byte)
28H	VCELL5L	R	00H	Cell 5 measurement result register (lower byte)

29H	VCELL5H	R	00H	Cell 5 measurement result register (higher byte)
Address	Register name	R/W	Initial value	Description
2AH	VCELL6L	R	00H	Cell 6 measurement result register (lower byte)
2BH	VCELL6H	R	00H	Cell 6 measurement result register (higher byte)
2CH	VCELL7L	R	00H	Cell 7 measurement result register (lower byte)
2DH	VCELL7H	R	00H	Cell 7 measurement result register (higher byte)
2EH	VCELL8L	R	00H	Cell 8 measurement result register (lower byte)
2FH	VCELL8H	R	00H	Cell 8 measurement result register (higher byte)
30H	VCELL9L	R	00H	Cell 9 measurement result register (lower byte)
31H	VCELL9H	R	00H	Cell 9 measurement result register (higher byte)
32H	VCELL10L	R	00H	Cell 10 measurement result register (lower byte)
33H	VCELL10H	R	00H	Cell 10 measurement result register (higher byte)
34H	VCELL11L	R	00H	Cell 11 measurement result register (lower byte)
35H	VCELL11H	R	00H	Cell 11 measurement result register (higher byte)
36H	VCELL12L	R	00H	Cell 12 measurement result register (lower byte)
37H	VCELL12H	R	00H	Cell 12 measurement result register (higher byte)
38H	VCELL13L	R	00H	Cell 13 measurement result register (lower byte)
39H	VCELL13H	R	00H	Cell 13 measurement result register (higher byte)
3AH	VCELL14L	R	00H	Cell 14 measurement result register (lower byte)
3BH	VCELL14H	R	00H	Cell 14 measurement result register (higher byte)
3CH	VCELL15L	R	00H	Cell 15 measurement result register (lower byte)
3DH	VCELL15H	R	00H	Cell 15 measurement result register (higher byte)
3EH	VCELL16L	R	00H	Cell 16 measurement result register (lower byte)
3FH	VCELL16H	R	00H	Cell 16 measurement result register (higher byte)
40H	TEMP1L	R	00H	TEMP1 measurement result register (lower byte)
41H	TEMP1H	R	00H	TEMP1 measurement result register (higher byte)
42H	TEMP2L	R	00H	TEMP2 measurement result register (lower byte)
43H	TEMP2H	R	00H	TEMP2 measurement result register (higher byte)
44H	TEMP3L	R	00H	TEMP3 measurement result register (lower byte)

45H	TEMP3H	R	00H	TEMP3 measurement result register (higher byte)
Address	Register name	R/W	Initial value	Description
46H	TEMP4L	R	00H	TEMP4 measurement result register (lower byte)
47H	TEMP4H	R	00H	TEMP4 measurement result register (higher byte)
48H	VREGL	R	00H	VREG voltage measurement result register (lower byte)
49H	VREGH	R	00H	VREG voltage measurement result register (higher byte)
Others	TEST	R/W	00H	For test (Do not use. Operation is not guaranteed if it is used.)

1. NOOP Register (Adrs = 00H)

	7	6	5	4	3	2	1	0
Bit name	NO7	NO6	NO5	NO4	NO3	NO2	NO1	NO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	1	0	1	0	1	0	1

No function is assigned to the NOOP register. Read/write access to this register does not change the LSI state. The written data can be read as it is.

2. RSTREQ Register (Adrs = 01H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	—	—	RST
R/W	R	R	R	R	R	R	R	W
Initial value	0	0	0	0	0	0	0	0

The RSTREQ register requests a software reset.
Setting the RST bit to "1" generates a reset by software request.
All the registers other than IDREG are initialized by the software reset execution.
This is a write-only register. If you read it, 00H is read.

RST	Software reset
0	Reset is not performed (initial value)
1	Reset is performed

3. INT_EN Register (Adrs = 02H)

Bit	7	6	5	4	3	2	1	0
name	EWDOV	EVRGR	EVRGD	ECRC	EID	EMVR	EMT	EMVC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	0	0

The INT_EN register sets whether or not to enable the interrupt signal output to the /INTO pin.

The EMVC bit sets whether or not to enable an interrupt on completion of cell voltage measurement.

EMVC	Cell voltage measurement completion interrupt
0	Disabled (initial value)
1	Enabled

The EMT bit sets whether or not to enable an interrupt on completion of temperature sensor measurement.

EMT	Temperature sensor measurement completion interrupt
0	Disabled (initial value)
1	Enabled

The EMVR bit sets whether or not to enable an interrupt on completion of VREG voltage measurement.

EMVR	VREG voltage measurement completion interrupt
0	Disabled (initial value)
1	Enabled

The EID bit sets whether or not to enable an interrupt on completion of ID automatic setting.

EID	ID automatic setting completion interrupt
0	Disabled (initial value)
1	Enabled

The ECRC bit sets whether or not to enable an interrupt when a CRC error is detected.

ECRC	CRC error interrupt
0	Disabled (initial value)
1	Enabled

The EVRGD bit sets whether or not to enable an interrupt when a VREG output voltage dropping is detected.

EVRGD	VREG dropping detection interrupt
0	Disabled (initial value)
1	Enabled

The EVRGR bit sets whether or not to enable an interrupt when a VREG output voltage return is detected.

EVRGR	VREG return detection interrupt
0	Disabled (initial value)
1	Enabled

The EWDOV bit sets whether or not to enable an interrupt when WDT overflows.

EWDOV	WDT overflow interrupt
0	Prohibited
1	Enabled (initial value)

4. INT_REQ Register (Adrs = 03H)

	7	6	5	4	3	2	1	0
Bit name	QWDOV	QVRGR	QVRGD	QCRC	QID	QMVR	QMT	QMVC
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0 *	0 *	0	0	0	0	0

The INT_REQ register contains interrupt request flags. Each request flag is set to "1" when an interrupt is generated, regardless of the setting of INT_EN register. Only when an interrupt enabled by the INT_EN register is generated, the "L" level is output to the /INTO pin.
An interrupt can be cleared by writing data "0". Writing data "1" is ignored. If you want to clear only one interrupt, write "1" to the other bits. When all enabled interrupt request flags are cleared to "0", the output to /INTO pin is set to the "Hi-Z" level.
* Note: The initial values of the QVRGR bit and the QVRGD bit are values after software reset. Please initialize before use.

The QMVC bit indicates whether a cell voltage measurement completion interrupt has been generated.

QMVC	Cell voltage measurement completion interrupt
0	Without interrupt (initial value)
1	An interrupt is generated

The QMT bit indicates whether a temperature sensor measurement completion interrupt has been generated.

QMT	Temperature sensor measurement completion interrupt
0	Without interrupt (initial value)
1	An interrupt is generated

The QMVR bit indicates whether a VREG voltage measurement completion interrupt has been generated.

QMVR	VREG voltage measurement completion interrupt
0	Without interrupt (initial value)
1	An interrupt is generated

The QID bit indicates whether an ID automatic setting completion interrupt has been generated.

QID	ID automatic setting completion interrupt
0	Without interrupt (initial value)
1	An interrupt is generated

The QCRC bit indicates whether an interrupt has been generated when a CRC error is detected.

QCRC	CRC error interrupt
0	Without interrupt (initial value)
1	An interrupt is generated

The QVRGD bit indicates whether an interrupt has been generated when a VREG output voltage dropping is detected.
If a dropping is detected during the VREG output voltage return state, an interrupt occurs, and it is cleared during the VREG output voltage dropping detection state, then an interrupt does not occur even in the dropping detection state.

QVRGD	VREG dropping detection interrupt
0	Without interrupt (initial value *)
1	An interrupt is generated

The QVRGR bit indicates whether an interrupt has been generated when a VREG output voltage return is detected.
If a return from VREG output voltage dropping detection state is detected, an interrupt occurs.

QVRGR	VREG return detection interrupt
0	Without interrupt (initial value *)
1	An interrupt is generated

The QWDOV bit indicates whether an interrupt occurs when WDT overflows.

QWDOV	WDT overflow interrupt
0	Without interrupt (initial value)
1	An interrupt is generated

5. PDACP Register (Adrs = 04H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	—	—	—
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

The PDACP register enables writing to PDWN of the POWER register to avoid entering the power-down mode accidentally. Writing 0x55 and 0xAA successively to this register enables setting PDWN of POWER register to "1".

6. POWER Register (Adrs = 05H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	PDWN	—	—	—	—
R/W	R	R	R	W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The POWER register controls the power-down.

The PDWN bit is used to enable the power-down state.

PDWN	Power-down
0	Normal state (initial value)
1	Power-down

7. MEAS_VCELL Register (Adrs = 06H)

	7	6	5	4	3	2	1	0
Bit name	MVC	—	—	SCV	C3	C2	C1	C0
R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The MEAS_VCELL register controls the cell voltage measurement.

Use the SCV bit and the C0 to C3 bits to select the measurement mode and the battery cell(s) to be measured.

SCV	C3	C2	C1	C0	Cell voltage measurement
0	0	0	0	0	Only cell 1 is measured
0	0	0	0	1	Only cell 2 is measured
0	0	0	1	0	Only cell 3 is measured
0	0	0	1	1	Only cell 4 is measured
0	0	1	0	0	Only cell 5 is measured
0	0	1	0	1	Only cell 6 is measured
0	0	1	1	0	Only cell 7 is measured
0	0	1	1	1	Only cell 8 is measured
0	1	0	0	0	Only cell 9 is measured
0	1	0	0	1	Only cell 10 is measured
0	1	0	1	0	Only cell 11 is measured
0	1	0	1	1	Only cell 12 is measured
0	1	1	0	0	Only cell 13 is measured
0	1	1	0	1	Only cell 14 is measured
0	1	1	1	0	Only cell 15 is measured
0	1	1	1	1	Only cell 16 is measured
1	0	0	0	0	Only cell 1 is measured
1	0	0	0	1	Cell 1 to cell 2 are measured in the scan mode
1	0	0	1	0	Cell 1 to cell 3 are measured in the scan mode
1	0	0	1	1	Cell 1 to cell 4 are measured in the scan mode
1	0	1	0	0	Cell 1 to cell 5 are measured in the scan mode
1	0	1	0	1	Cell 1 to cell 6 are measured in the scan mode
1	0	1	1	0	Cell 1 to cell 7 are measured in the scan mode
1	0	1	1	1	Cell 1 to cell 8 are measured in the scan mode
1	1	0	0	0	Cell 1 to cell 9 are measured in the scan mode
1	1	0	0	1	Cell 1 to cell 10 are measured in the scan mode
1	1	0	1	0	Cell 1 to cell 11 are measured in the scan mode
1	1	0	1	1	Cell 1 to cell 12 are measured in the scan mode
1	1	1	0	0	Cell 1 to cell 13 are measured in the scan mode
1	1	1	0	1	Cell 1 to cell 14 are measured in the scan mode
1	1	1	1	0	Cell 1 to cell 15 are measured in the scan mode
1	1	1	1	1	Cell 1 to cell 16 are measured in the scan mode

The MVC bit is used to control the start/stop of cell voltage measurement and to verify the cell voltage measurement completion status. The cell voltage measurement results are stored in the VCELLnL and VCELLnH registers (20H to 3FH).

Write		Read	
MVC	Cell voltage measurement	MVC	Cell voltage measurement
0	Stop (initial value)	0	Completed/stopped (initial value)
1	Start	1	Measuring

It is possible to stop the cell voltage measurement by writing "0" to the MVC bit while measuring the cell voltage. In that case, the measurement stops after the cell voltage measurement in progress is completed. The read value of MVC bit remains "1" until the measurement stops, and it is reset to "0" after the measurement stops.
Any change in the settings of the SCV bit and C3 to C0 bits is ignored during the measurement (while the read value of MVC bit is "1").
Also, setting the MVC bit to "1" is ignored while measuring temperature sensor, VREG voltage, and open/short detection.

8. MEAS_TEMP Register (Adrs = 07H)

	7	6	5	4	3	2	1	0
Bit name	MT	—	—	SCT	—	—	T1	T0
R/W	R/W	R	R	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The MEAS_TEMP register controls the measurement of the temperature sensors (TEMP1 to TEMP4 pins input voltage).

The SCT, T0, and T1 bits select the temperature sensor measurement mode.

SCT	T1	T0	Temperature sensor measurement mode
0	0	0	TEMP1 pin input voltage measurement only (initial value)
0	0	1	TEMP2 pin input voltage measurement only
0	1	0	TEMP3 pin input voltage measurement only
0	1	1	TEMP4 pin input voltage measurement only
1	0	0	TEMP1 pin input voltage measurement only
1	0	1	TEMP1 to TEMP2 pins input voltage scan measurement
1	1	0	TEMP1 to TEMP3 pins input voltage scan measurement
1	1	1	TEMP1 to TEMP4 pins input voltage scan measurement

The MT bit is used to control the start/stop of temperature sensor measurement and to verify the temperature sensor measurement completion status. The temperature sensor measurement results are stored in the TEMPnL and TEMPnH registers (40H to 47H).

Write		Read	
MT	TEMP pin voltage measurement	MT	TEMP pin voltage measurement
0	Stop (initial value)	0	Completed/stopped (initial value)
1	Start	1	Measuring

It is possible to stop the temperature sensor measurement by writing "0" to the MT bit while measuring the temperature sensor. In that case, the measurement stops after the temperature sensor measurement in progress is completed. The read value of MT bit remains "1" until the measurement stops, and it is reset to "0" after the measurement stops.
Any change in the settings of the SCT, T0, T1 bits is ignored during the measurement (while the read value of the MT bit is "1").
Also, setting the MT bit to "1" is ignored while measuring cell voltage, VREG voltage, and open/short detection.

9. MEAS_VREG Register (Adrs = 08H)

	7	6	5	4	3	2	1	0
Bit name	MVR	—	—	—	—	—	—	—
R/W	R/W	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The MEAS_VREG register controls the VREG voltage measurement.
The voltage actually measured by this register is VREG×1/2 instead of VREG itself.

The MVR bit is used to control the start/stop of VREG voltage measurement and to verify the VREG voltage measurement completion status. The VREG voltage measurement result is stored in the VREGL and VREGH registers (48H to 49H).

Write		Read	
MVR	VREG voltage measurement	MVR	VREG voltage measurement
0	Disabled (initial value)	0	Completed/stopped (initial value)
1	Start	1	Measuring

Writing "0" to the MVR bit cannot stop the VREG voltage measurement while measuring the VREG voltage.
Also, setting the MVR bit to "1" is ignored while measuring cell voltage, temperature sensor, and open/short detection.

10. MEAS_VOPSH Register (Adrs = 09H)

	7	6	5	4	3	2	1	0
Bit name	MOS	—	—	—	—	—	—	—
R/W	R/W	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The MEAS_VOPSH register controls measuring the open/short detection of the cell voltage measurement pin.

The MOS bit is used to control the open/short detection measurement start/stop of cell voltage measurement pin and to verify the cell voltage measurement completion status. The cell voltage measurement results are stored in the VCELLnL and VCELLnH registers (20H to 3FH).

Write		Read	
MOS	Open/short detection measurement	MOS	Open/short detection measurement
0	Stop (initial value)	0	Completed/stopped (initial value)
1	Start	1	Measuring

It is possible to stop the detection measurement by writing "0" to the MOS bit while measuring open/short detection of cell voltage measurement pin. In that case, the measurement stops after the cell voltage measurement in progress is completed. The read value of MOS bit remains "1" until the measurement stops, and it is reset to "0" after the measurement stops.
Setting the MOS bit to "1" is ignored during the cell voltage measurement, temperature sensor measurement, and VREG voltage measurement.

11. STATUS Register (Adrs = 0AH)

	7	6	5	4	3	2	1	0
Bit name	—	VRGD	CBALH	CBALL	MOS	MVR	MT	MVC
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The STATUS register indicates various status information. Writing to this register is ignored.
The MVC bit indicates the cell voltage measurement state. This is the same as the MVC bit of the MEAS_VCELL register.

MVC	Cell voltage measuring state
0	Measuring completed (initial value)
1	Measuring

The MT bit indicates the temperature sensor measurement state. This is the same as the MT bit of the MEAS_TEMP register.

MT	Temperature sensor measurement
0	Measuring completed (initial value)
1	Measuring

The MVR bit indicates the VREG voltage measurement state. This is the same as the MVR bit of the MEAS_VREG register.

MVR	VREG measurement
0	Measuring completed (initial value)
1	Measuring

The MOS bit indicates the open/short detection measurement state of the cell voltage measurement pin. This is the same as the MOS bit of the MEAS_VOPSH register.

MOS	Open/short detection measurement state
0	Measuring completed (initial value)
1	Measuring

The CBALL bit indicates the CB pin output status of the lower eight cells.

CBALL	CB1 to CB8 pin status
0	All outputs at Vn-1 pin (initial value)
1	Any outputs at Vn pin

The CBALH bit indicates the CB pin output status of the higher eight cells.

CBALH	CB9 to CB16 pin status
0	All outputs at Vn-1 pin (initial value)
1	Any outputs at Vn pin

The VRGD bit indicates the VREG output voltage dropping detection state.

VRGD	VREG output voltage dropping detection state
0	Not detecting dropping (initial value)
1	Detecting dropping

12. STAT_VML Register (Adrs = 0BH)

	7	6	5	4	3	2	1	0
Bit name	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The STAT_VML register indicates the cell voltage measurement state and the open/short detection measurement state of the lower eight cells.
If the cell voltage measurement is started with the MVC bit of the MEAS_VCELL register set to "1", the VC1 to VC8 bits are reset to "0", and the bits corresponding to measured cells are reset to "1". The progress of the cell voltage measurement can be checked by reading this register.
If open/short detection measurement of cell voltage measurement pin is started with the MOS bit of the MEAS_VOPSH register set to "1", the VC1 to VC8 bits are reset to "0", and the bits corresponding to measured cells are reset to "1". The progress of the open/short detection measurement can be checked by reading this register.
The VC1 to VC8 bits indicate the cell voltage measurement completion state.

VCn	Cell voltage measuring state
0	During measurement or not to be measured (initial value)
1	Measurement completed

13. STAT_VMH Register (Adrs = 0CH)

	7	6	5	4	3	2	1	0
Bit name	VC16	VC15	VC14	VC13	VC12	VC11	VC10	VC9
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The STAT_VMH register indicates the cell voltage measurement state and the open/short detection measurement state of the higher eight cells.
If the cell voltage measurement is started with the MVC bit of the MEAS_VCELL register set to "1", the VC9 to VC16 bits are reset to "0", and the bits corresponding to measured cells are reset to "1".
The progress of the cell voltage measurement can be checked by reading this register.
If open/short detection measurement of cell voltage measurement pin is started with the MOS bit of the MEAS_VOPSH register set to "1", the VC9 to VC16 bits are reset to "0", and the bits corresponding to measured cells are reset to "1". The progress of the open/short detection measurement can be checked by reading this register.
The VC9 to VC16 bits indicate the cell voltage measurement completion state.

VCn	Cell voltage measuring state
0	During measurement or not to be measured (initial value)
1	Measurement completed

14. STAT_TM Register (Adrs = 0DH)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	TM4	TM3	TM2	TM1
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The STAT_TM register indicates the temperature sensor measurement state.
If the temperature sensor measurement is started with the MT bit of the MEAS_TEMP register set to "1", the TM1 to TM4 bits are reset to "0", and the bits corresponding to measured pins are reset to "1".
The progress of the temperature sensor measurement can be checked by reading this register.
The TM1 to TM4 bits indicate the temperature sensor measurement completion state.

TMn	Temperature sensor measurement
0	During measurement or not to be measured (initial value)
1	Measurement completed

15. CBALL Register (Adrs = 0EH)

	7	6	5	4	3	2	1	0
Bit name	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The CBALL register sets the CBn pin output of the lower eight cells.
Use the SW1 to SW8 bits to set each CBn pin output. Multiple bits can be set to "1".

SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	CB1 to CB8 pin status
0	0	0	0	0	0	0	0	CBn = Vn-1 (initial value)
0	0	0	0	0	0	0	1	CB1 pin = V1 pin Other CBn pin = Vn-1
0	0	0	0	0	0	1	0	CB2 pin = V2 pin Other CBn pin = Vn-1
0	0	0	0	0	1	0	0	CB3 pin = V3 pin Other CBn pin = Vn-1
0	0	0	0	1	0	0	0	CB4 pin = V4 pin Other CBn pin = Vn-1
0	0	0	1	0	0	0	0	CB5 pin = V5 pin Other CBn pin = Vn-1
0	0	1	0	0	0	0	0	CB6 pin = V6 pin Other CBn pin = Vn-1
0	1	0	0	0	0	0	0	CB7 pin = V7 pin Other CBn pin = Vn-1
1	0	0	0	0	0	0	0	CB8 pin = V8 pin Other CBn pin = Vn-1

16. CBALH Register (Adrs = 0FH)

	7	6	5	4	3	2	1	0
Bit name	SW16	SW15	SW14	SW13	SW12	SW11	SW10	SW9
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The CBALH register sets the CBn pin output of the higher eight cells.
Use the SW9 to SW16 bits to set each CBn pin output. Multiple bits can be set to "1".

SW16	SW15	SW14	SW13	SW12	SW11	SW10	SW9	CB9 to CB16 pin status
0	0	0	0	0	0	0	0	CBn = Vn-1 (initial value)
0	0	0	0	0	0	0	1	CB9 pin = V9 pin Other CBn pin = Vn-1
0	0	0	0	0	0	1	0	CB10 pin = V10 pin Other CBn pin = Vn-1
0	0	0	0	0	1	0	0	CB11 pin = V11 pin Other CBn pin = Vn-1
0	0	0	0	1	0	0	0	CB12 pin = V12 pin Other CBn pin = Vn-1
0	0	0	1	0	0	0	0	CB13 pin = V13 pin Other CBn pin = Vn-1
0	0	1	0	0	0	0	0	CB14 pin = V14 pin Other CBn pin = Vn-1
0	1	0	0	0	0	0	0	CB15 pin = V15 pin Other CBn pin = Vn-1
1	0	0	0	0	0	0	0	CB16 pin = V16 pin Other CBn pin = Vn-1

17. IDSEL Register (Adrs = 10H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	—	—	ID
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	pin status

The IDSEL register stores the state (input level) of the ID pin.

18. IDACP Register (Adrs = 11H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	—	—	—
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

The IDACP register allows writing to IDREG in order to prevent IDREG from being accidentally written. Writing 0x5A to this register enables the writing operation to IDREG.

19. IDREG Register (Adrs = 12H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	ID3	ID2	ID1	ID0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The IDREG register stores the ID assignment of each IC in multi-stage connection.
The IDs which are automatically set are as follows. For instructions on configuring automatic setting, refer to "ID Automatic Setting Function".

ID3	ID2	ID1	ID0	Multi-stage connection order
0	0	0	0	Lowest IC
0	0	0	1	2nd lowest IC
0	0	1	0	3rd lowest IC
:				:
1	1	0	1	14th lowest IC
1	1	1	0	15th lowest IC
1	1	1	1	16th lowest IC

20. WDTACP Register (Adrs = 13H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	—	—	—
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

The WDTACP register allows writing to SETWDT in order to prevent SETWDT from being accidentally written. Writing 0xA5 to this register enables the writing operation to SETWDT.

21. SETWDT Register (Adrs = 14H)

	7	6	5	4	3	2	1	0
Bit name	ENWD	—	—	—	—	—	WDT1	WDT0
R/W	R/W	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The SETWDT register sets the watchdog timer run/stop and the overflow period.

The WDT0 and WDT1 bits set the overflow period.

WDT1	WDT0	Overflow period (Typ)
0	0	1 second (initial value)
0	1	2 seconds
1	0	4 seconds
1	1	8 seconds

The ENWD bit controls the run/stop of the watchdog timer.

ENWD	WDT operation state
0	Run (initial value)
1	Stop

22. SELOUT Register (Adrs = 15H)

	7	6	5	4	3	2	1	0
Bit name	STO4	STO3	STO2	STO1	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The SELOUT register switches the thermistor connection pin for temperature measurement to the general-purpose output.

The STO1 to STO4 bits set the TEMPn pin status.

STOn	TEMPn pin status
0	Input for temperature sensor measurement (initial value)
1	General-purpose output

23. SETOUT Register (Adrs = 16H)

	7	6	5	4	3	2	1	0
Bit name	TO4	TO3	TO2	TO1	GPO	—	—	TDRV
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
Initial value	0	0	0	0	1	0	0	1

The SETOUT register sets the output level of the output pin.

The TDRV bit sets the TDRV pin output status.

TDRV	TDRV pin output status
0	L output
1	HiZ (initial value)

The GPO bit sets the GPOUT pin output status.

GPO	GPOUT pin output status
0	L output
1	HiZ (initial value)

The TO1 to TO4 bits set the TEMPn pin output status.

TOn	TEMPn pin output status
0	L output (initial value)
1	HOutput

24. RSVD Register (Adrs = 17H to 1FH)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	—	—	—	—
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The RSVD register is a reserved register.
The data write is disabled, and the read data is 00H.

25. VCELLnL Register (Adrs = even addresses from 20H to 3FH)

	7	6	5	4	3	2	1	0
Bit name	VAD7	VAD6	VAD5	VAD4	VAD3	VAD2	VAD1	VAD0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The VCELLnL register (n = 1 to 16) stores the lower byte data of the A/D conversion result and open/short detection measurement result of the cell voltages.

26. VCELLnH Register (Adrs = odd addresses from 20H to 3FH)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	VAD11	VAD10	VAD9	VAD8
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The VCELLnH register (n = 1 to 16) stores the high-order 4-bit data of the A/D conversion result and open/short detection measurement result of the cell voltages.

27. TEMPnL Register (Adrs = even addresses from 40H to 47H)

	7	6	5	4	3	2	1	0
Bit name	TAD7	TAD6	TAD5	TAD4	TAD3	TAD2	TAD1	TAD0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The TEMPnL register (n = 1 to 4) stores the lower byte data of the A/D conversion result of the TEMP1 to TEMP4 pins.

28. TEMPnH Register (Adrs = odd addresses from 40H to 47H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	TAD11	TAD10	TAD9	TAD8
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The TEMPnH register (n = 1 to 4) stores the high-order 4-bit data of the A/D conversion result of the TEMP1 to TEMP4 pins.

29. VREGL Register (Adrs = 48H)

	7	6	5	4	3	2	1	0
Bit name	RAD7	RAD6	RAD5	RAD4	RAD3	RAD2	RAD1	RAD0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

The VREGL register stores the lower byte data of the A/D conversion result of VREG×1/2 voltage.

30. VREGH Register (Adrs = 49H)

	7	6	5	4	3	2	1	0
Bit name	—	—	—	—	RAD11	RAD10	RAD9	RAD8
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

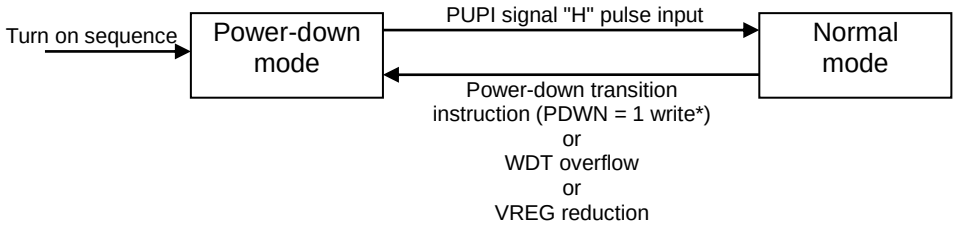
The VREGH register stores the high-order 4-bit data of the A/D conversion result of VREG×1/2 voltage.

- Operation Mode

This IC has the following operation modes.

Normal operation mode	All the functions operate.
Power-down mode	All the circuits other than power-up are stopped to reduce the current consumption.

The transition conditions to each mode are shown in the following figure.



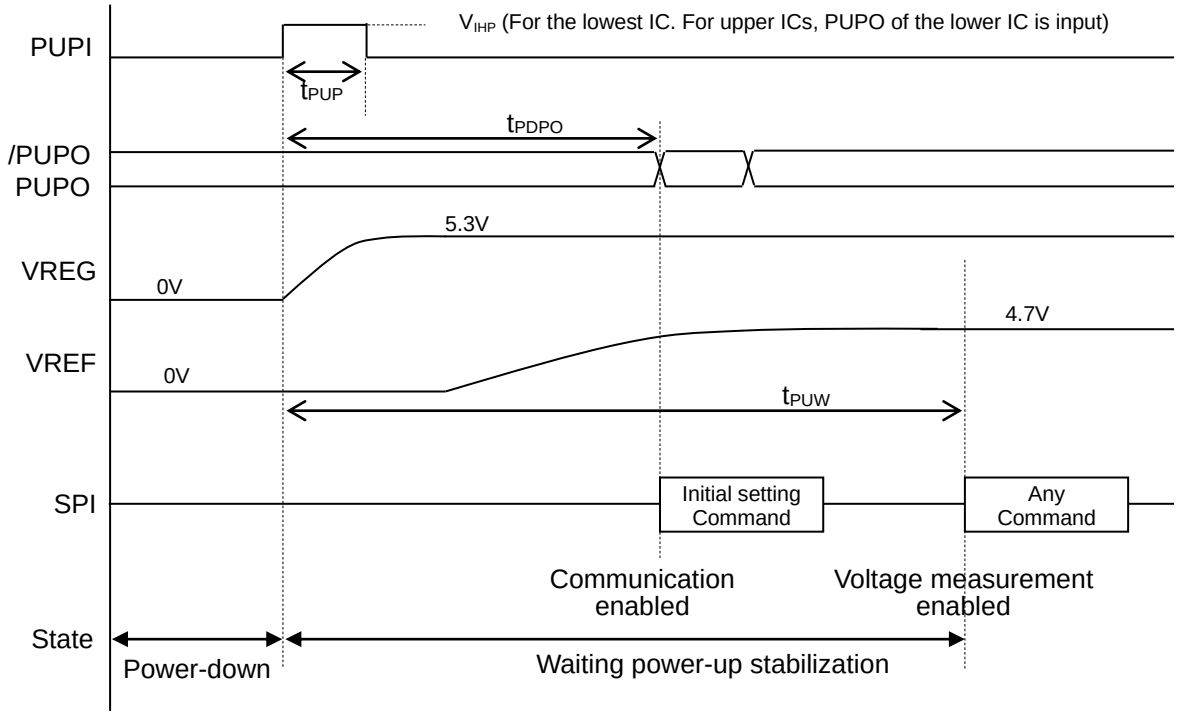
* To write 1 to PDWN, PDACP is required to enable writing in advance.

Transition from power-down mode to normal mode needs time for internal circuits to stabilize after inputting "H" pulse to PUPI pin. The waiting time before preparing for SPI communication is as follows:

SPI instruction	Waiting time
Other than voltage measurement (various settings, etc.)	t_{PDPO}×number of multi-stage stages
Voltage measurement (cell, temperature sensor, VREG)	t_{PUW}+t_{PDPO}×(number of multi-stage stages - 1)

If the voltage measurement is performed during power-up stabilization (t_{PUW} interval), the measurement error cannot be guaranteed.
For multi-stage connection, ID assignment to each IC is needed after transition to the normal mode.

Power-up operation (starting SPI communication) timing diagram



ID Automatic Setting Function

ML5239 has a function to assign each IC with ID automatically at multi-stage connection.
After internal circuit stabilization wait time at power-on, the ID automatic setting register IDREG of all ICs in multi-stage connection has an initial value 0x00. Write 0x5A to the ID automatic setting code acceptor IDACP with ID = WR_ALL using SPI communication to enable writing to the ID automatic setting register IDREG.
Then, write "number of multi-stage stages -1" to the ID automatic setting register IDREG with ID = WR_ALL to automatically set IDs in turns from the 2nd lowest IC, as shown in the following table.

ID3	ID2	ID1	ID0	Multi-stage connection order
0	0	0	0	Lowest IC
0	0	0	1	2nd lowest IC
0	0	1	0	3rd lowest IC
:				:
1	1	0	1	14th lowest IC
1	1	1	0	15th lowest IC
1	1	1	1	16th lowest IC

The ID automatic setting takes about 170μs per stage of multi-stage connection after writing any value to IDREG. Do not execute any SPI communication from MCU during ID automatic setting. For automatic ID setting, each higher ML5239 ID are set by the lowest ML5239, sequentially. And the MCU clock is not used but the SCKO from the lowest ML5239 is used.
The interrupt signal can be output to the external MCU on the /INTO pin on completion of the ID automatic setting. To output the interrupt signal, specify ID=”0” and the EID bit of the INT_EN register needs to be used to enable ID automatic setting completion interrupt before ID automatic setting. For details, refer to the INT_EN and INT_REQ registers of the control register.

Watchdog Timer Function

ML5239 has a watchdog timer function which detects failure when an SPI communication is not performed for certain period of time.
To clear the counter of WDT (for IC to recognize the SPI communication operation), 16CLK of SCK clock should be input with /CS="L" state.

Power-on/Power-off Sequence

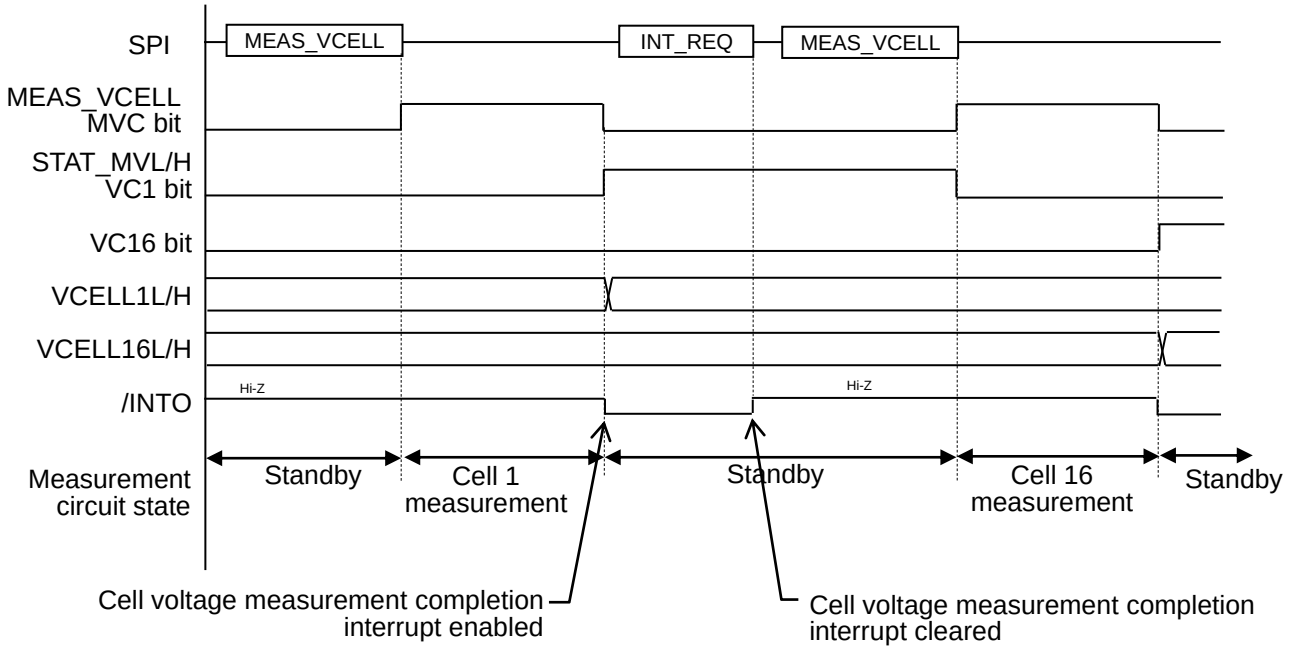
Battery cells can be connected in any order, but we recommend that you connect the GND and VDD pins first, then connect from lower cells.
Note that the initial state is the power-down mode after power-on. Write "H" pulse to the PUPI pin to power up. For details, please refer to "Operation Mode".

- Cell Voltage Measurement

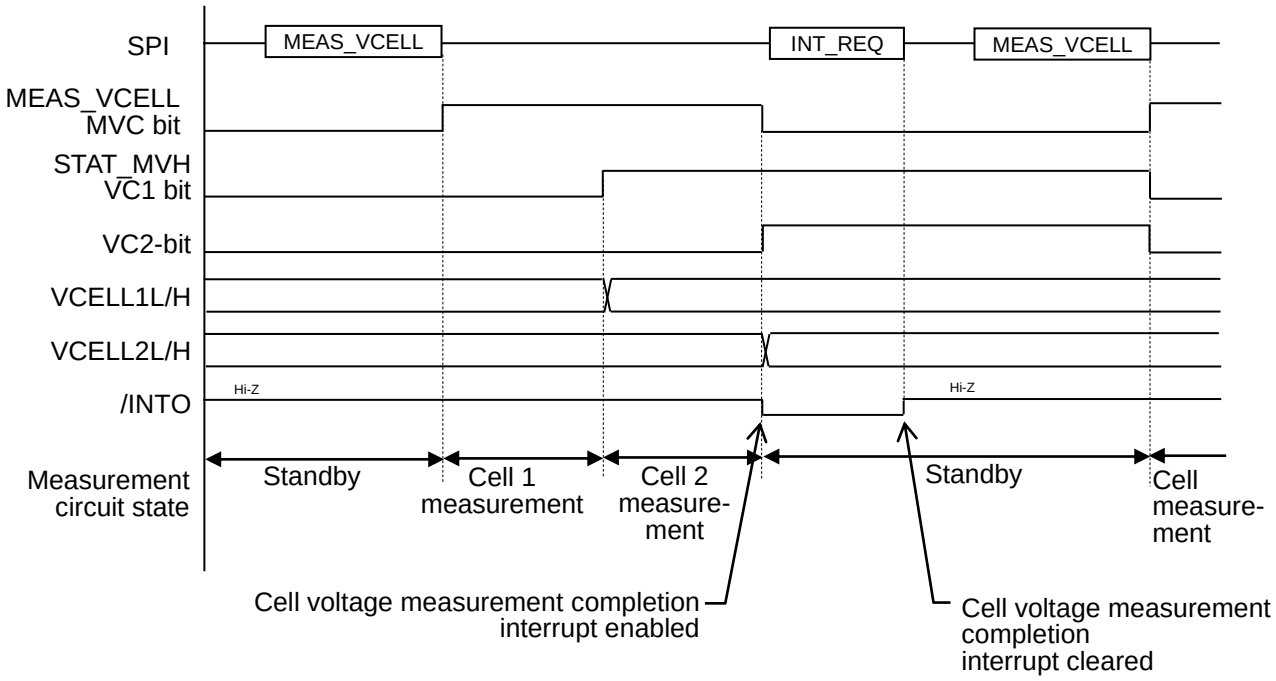
There are two modes of the cell voltage measurement method. The select measurement measures the voltage of one selected cell, and the scan measurement continuously measures the voltages of selected multiple cells.
The MEAS_VCELL register is used to select the cell voltage measurement mode and set the measurement. For details, see the MEAS_VCELL register section.

The following timing diagrams show the cell voltage measurement operation for both measurement modes.

Select measurement mode operation timing diagram (measuring the lowest cell 1 and the cell 16)



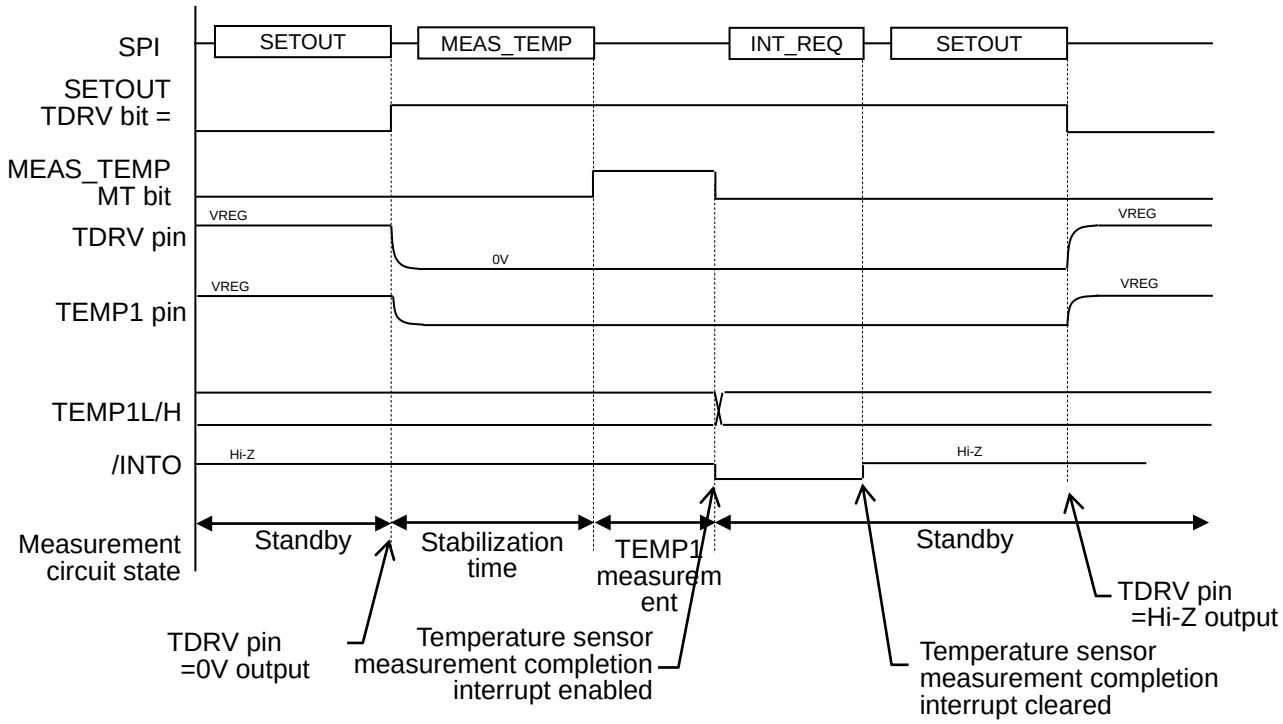
Scan measurement mode operation timing diagram (cells 1 and 2 measured)



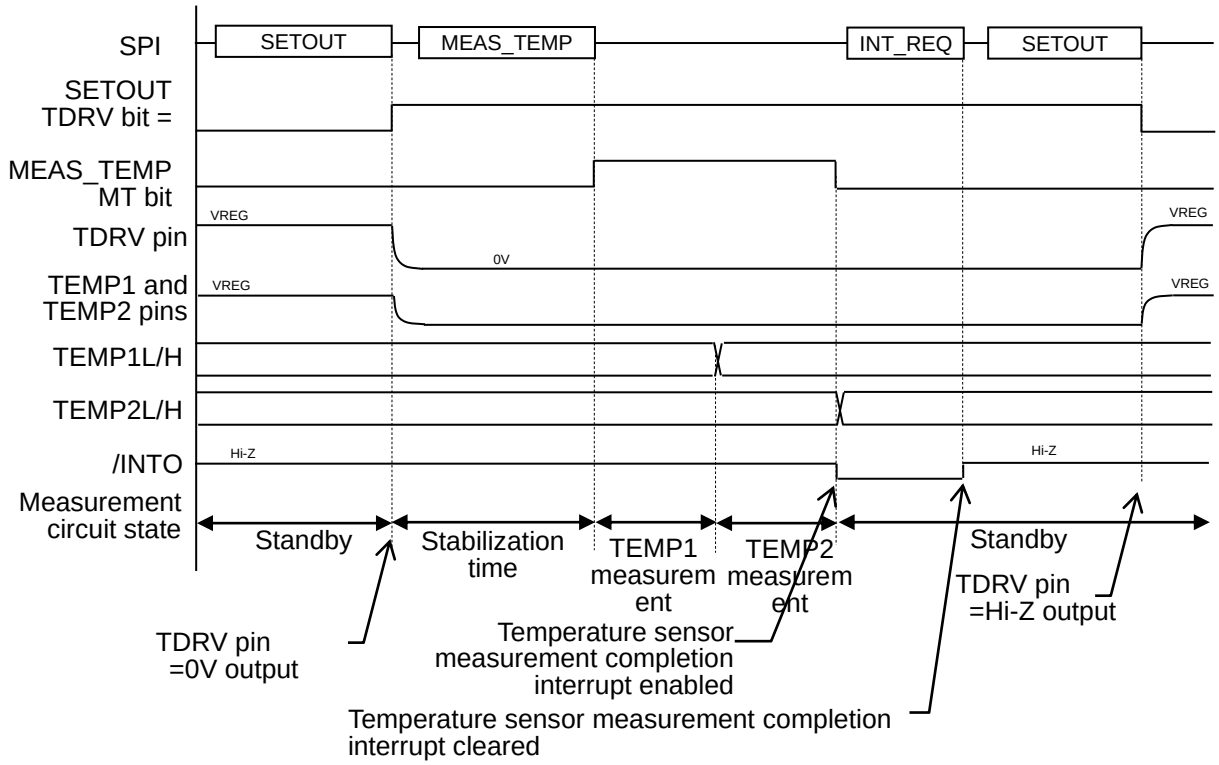
- Temperature Sensor Input Voltage Measurement

There are two modes of the temperature sensor input voltage measurement method. The select measurement mode measures the voltage of one selected temperature sensor input, and the scan measurement mode continuously measures the voltages of multiple temperature sensor inputs.
The MEAS_TEMP register is used to select the temperature sensor measurement mode and set the measurement.
For temperature sensor measurement, output 0V to the TDRV pin, and wait until the TEMP1 to TEMP4 pin input voltages stabilize before starting the measurement. For details, refer to the SETOUT and MEAS_TEMP registers. After the temperature sensor measurement completes, we recommend that you set the TDRV pin to the Hi-Z state for reduced current consumption and minimized VREG output voltage drop.
The following timing diagrams show the temperature sensor input voltage measurement operation for both measurement modes.

Select measurement mode operation timing diagram (TEMP1 pin input measured)



Scan measurement mode operation timing diagram (TEMP1 and TEMP2 measured)

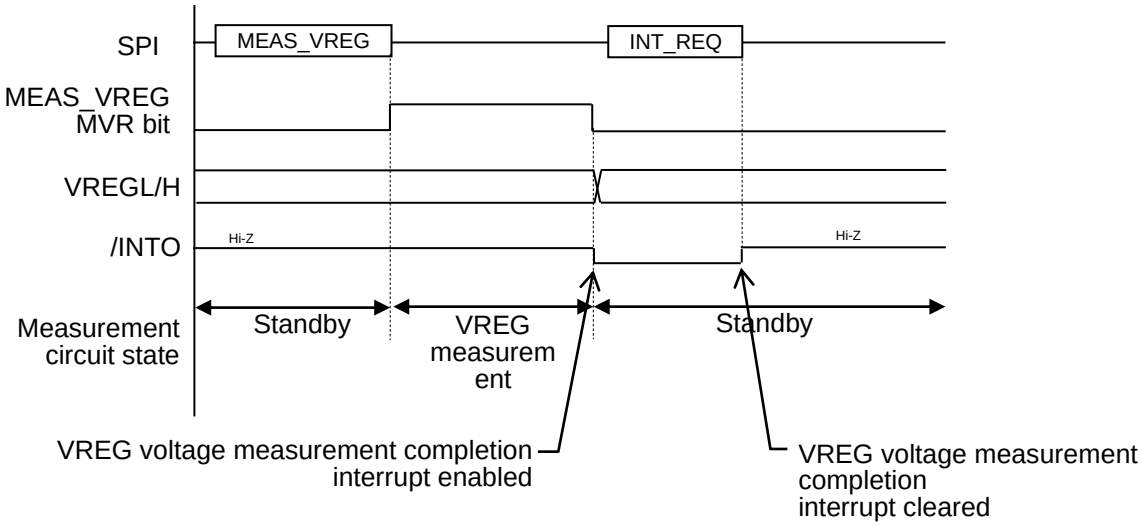


- VREG Voltage Measurement

The VREG voltage measurement is performed using the MEAS_VREG register. For details, see the MEAS_VREG register section.

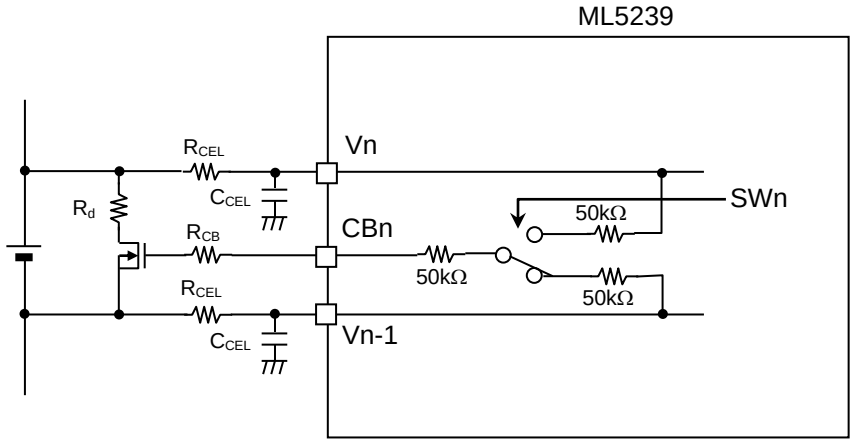
The following timing diagram shows the VREG voltage measurement operation.

VREG voltage measurement operation timing diagram



- Cell Balancing

Use an external Nch-FET to configure the cell balancing circuit shown in the following figure.
For cell balancing, a 100kΩ (typ) resistor is connected between the CBn and Vn pins by setting the SWn bit of the CBALL and CBALH registers to "1". If the SWn bit is "0", 100kΩ (typ) resistor is connected between CBn pin and Vn-1 pin.



- Interrupt Signal Output

This function outputs interrupt signals from the /INTO pin to notify the external MCU of measurement completion and error occurrence.
The INT_EN register is used to enable various interrupts, and the INT_REQ register is read/written to check and clear generated interrupts.
The following table shows interrupt sources, generation conditions, and states after generation.

Interrupt source	Interrupt generation condition	State after interrupt
Cell voltage measurement completion	The MVC bit of the MEAS_VCELL register is set to "1", then the cell voltage measurement is completed.	The measurement result is stored in the VCELLnL/H register.
Temperature sensor input Measurement completed	The MT bit of the MEAS_TEMP register is set to "1", then the temperature sensor measurement is completed.	The measurement result is stored in the TEMPnL/H register.
VREG voltage measurement completed	The MVR bit of the MEAS_VREG register is set to "1", then the VREG voltage measurement is completed.	The measurement result is stored in the VREGL/H register.
CRC error	The received CRC code does not match the calculation result.	The received SPI communication data is disabled.
ID automatic setting completed	ID automatic setting is completed.	All ICs enter the Standby (instruction acceptable) state.
VREG output voltage dropping detection	It is detected that the VREG pin output voltage is equal to or less than 4.3V (typ).	Various measurement results are not valid.
VREG output voltage return detection	It is detected that the VREG pin output voltage is equal to or more than 4.85V (typ). An interrupt does not occur during VREG output rising at power-up.	Various measurements can be performed successfully.
WDT	An overflow occurs.	IC powers down.

* When VREG is less than the recommended operation range, an interrupt occurs. In addition, when it drops nearly to a level where internal IC circuits cannot operate normally, it enters the power-down.

- Cell Connection Method

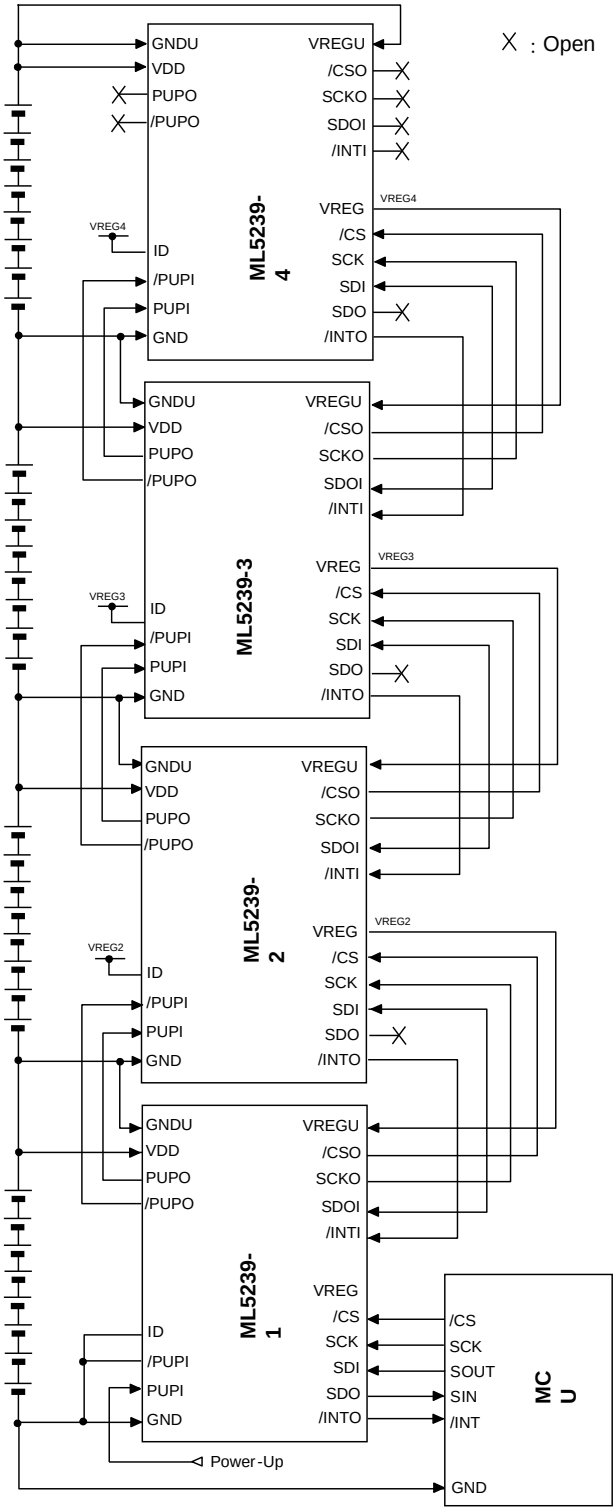
We recommend the following connections when the number of connected cells is 15 or less.

Connected cells	V16 pin	V15 pin	V14 pin	V13 pin	V12 pin	V11 pin	V10 pin	V9 pin	V8 pin	V7 pin	V6 pin	V1 to V5 pins
15	V_{TOP}	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell
14	V_{TOP}	V_{TOP}	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell
13	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell
12	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell	Cell	Cell	Cell	Cell	Cell	Cell
11	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell	Cell	Cell	Cell	Cell	Cell
10	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell	Cell	Cell	Cell	Cell
9	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell	Cell	Cell	Cell
8	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell	Cell	Cell
7	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell	Cell
6	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell	Cell
5	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	V_{TOP}	Cell

* V_{TOP}: Same potential as highest connected battery V pin of the IC

- Multi-stage Connection Method

ML5239 allows up to 16 ICs to be used in multi-stage connection.
In multi-stage connection, ICs should be connected as shown in the following figure. Refer to an application circuit example for more connection details.
Set the ID pin of the lowest IC to "L" level. Set the ID pin of all the higher ICs to "H" level.
For the SDOI pin and SDI pin of the higher ICs, the I/O mode automatically switches according to read/write operation.
Use an actual application to check the SPI communication speed, which is limited by IC-IC wiring parasitic capacitance, etc.



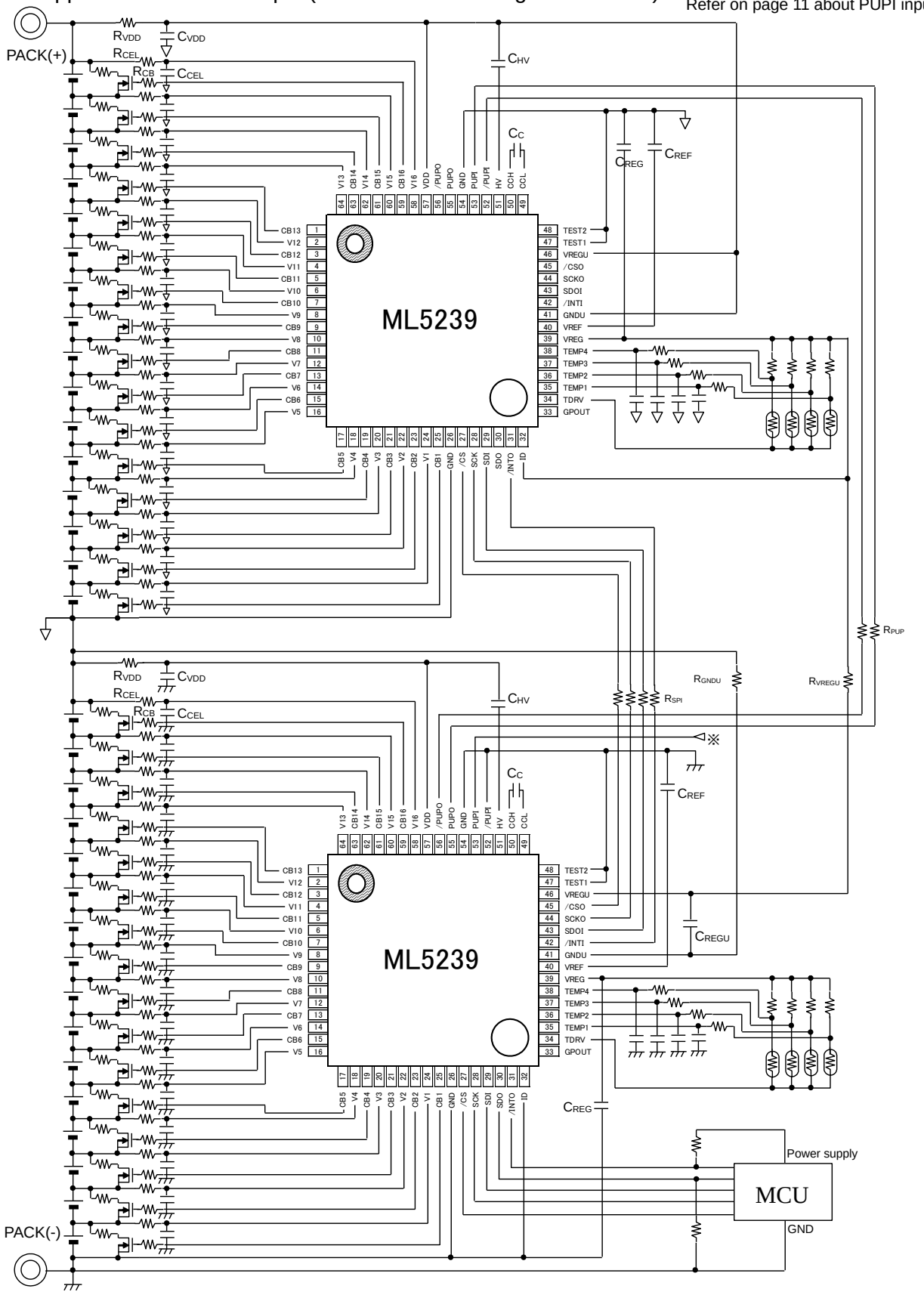
- Unused Pins Treatment

The following table shows how to handle unused pins.

Unused pins	Recommended treatment
V6 to V16	Same potential as highest connected battery V pin of the IC
CB1 to CB16	Open
TDRV	Left open or connected to the GND pin
TEMP1 to TEMP4	Connected to the GND pin
/INTO	Left open or connected to the GND pin
PUPO	Open
/PUPO	Open
/INTI	Open
SDOI	Open
SCKO	Open
/CSO	Open

■ Application circuit example (16 cells with two-stage connection)

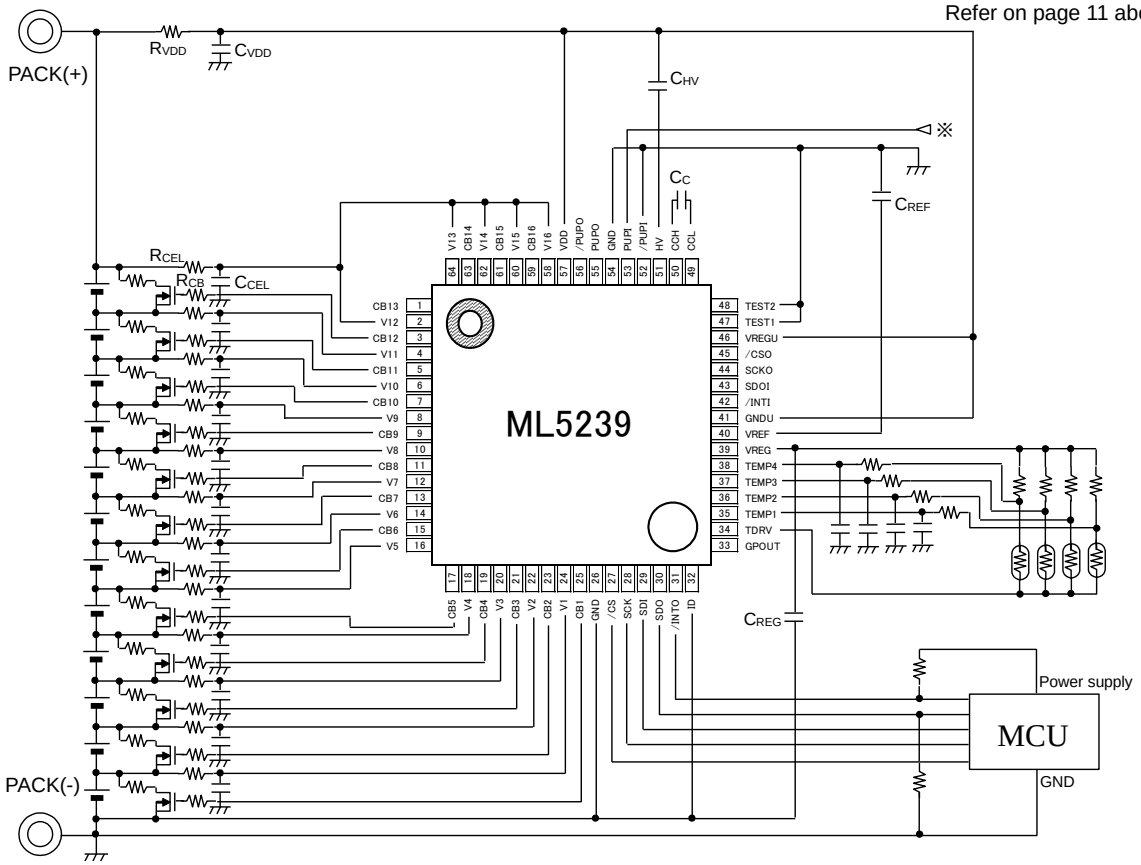
Unconnected pins are open.
Refer on page 11 about PUPI input.



(Note) GND wiring Recommendation, the lowest Cell 1 measurement measures the voltage between the V1 and GND pins of ML5239.As the current flowing to GND increases, the measurement error increases.
It is recommended to separate from other GND with large current such as MCU and use independent wiring.

■ Application circuit example (12 cells without multi-stage connection)

Unconnected pins are open.
Refer on page 11 about PUPI input.



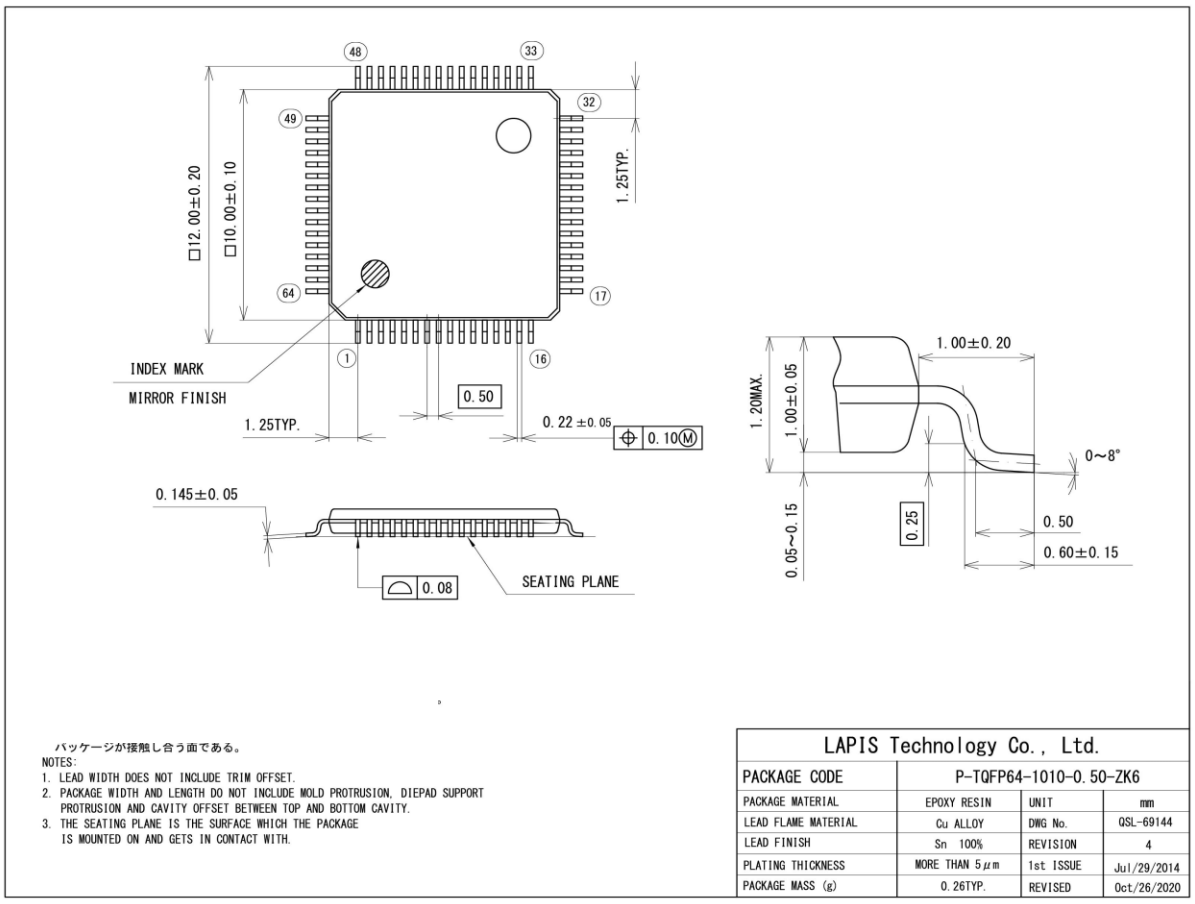
(Note) GND wiring Recommendation, the lowest Cell 1 measurement measures the voltage between the V1 and GND pins of ML5239.As the current flowing to GND increases, the measurement error increases.
It is recommended to separate from other GND with large current such as MCU and use independent wiring.

● Recommended Values for Externally Connected Components

Component	Recommended value			
	Withstanding pressure[V]	Min	Typ	Max
R_{VDD}	—	100Ω	—	330Ω
C_{VDD}	100	1.0μF	—	—
R_{CEL}	—	100Ω	—	1kΩ
C_{CEL}	100	0.1μF	—	—
R_{CB}	—	1kΩ	—	—
C_C	10	—	0.22μF	—
C_{HV}	10	—	0.22μF	—
C_{REF}	10	—	1.0μF	—
C_{REG}	10	—	1.0μF	—
C_{REGU}	10	10nF	0.1μF	1.0μF
R_{VREGU}	—	100Ω	—	330Ω
R_{GNDU}	—	100Ω	—	330Ω
R_{SPI}	—	100Ω	—	330Ω
R_{PUP}	—	500Ω	—	1kΩ

(Note) Required tolerance are $\Delta R \pm 1\%$, $\Delta C \pm 20\%$.
These circuit examples and recommended values of external parts do not guarantee the operation under all operation conditions. The product should be evaluated using the actual application to select an optimal circuit configuration and part constants.

■ Package Dimensions



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP64-1010-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69144
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.26TYP.	REVISED	Oct/26/2020

Remarks for surface mount type package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM sales representative for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■ Revision History

Document No.	Issue date	Pages		Revision description
		Before	After	
FEDL5239-01	March 12, 2015	-	-	Initial release
FEDL5239-02	March 29, 2019	9	9	Change AC Characteristics
		35	35	Add automatic ID setting description.
		44	44	Change Recommended values for externally connected components.
FEDL5239-03	August 8, 2019	6	6	Change Absolute maximum ratings of PUPI, /PUPI input voltage
FEDL5239-04	March 23, 2020	7	7	Change Electrical Characteristics of VHV L-limit 3.8V to 3.3V
FEDL5239-05	Dec. 1, 2020	-	-	Changed Company name
		47	47	Changed “Notes”
FEDL5239-06	Dec. 7, 2022	6	6	Add condition of Vregu
		43,44	43,44	Change Application circuit example, and Add GND wiring Recommendation
FEDL5239-07	Jan. 9, 2024	1	1	Add Application Part number, Delete notes
		47	47	Add Notes

Notes

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