Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML5233

4- to 10-Series Cell Li-ion Rechargeable Battery Protection IC

■ General Description

The ML5233 is a protection IC for the 4- to 10-cell Li-ion rechargeable battery pack. It detects individual cell overvoltage/undervoltage and the pack overcurrent/over-temperature, and then automatically turns on or turns off the external charge/discharge NMOS-FETs accordingly. Also the ML5233 can be cascaded to handle battery packs with more than 10 cells.

■ Features

- 4 to 10 cell high-precision overvoltage and undervoltage detection function
  Voltage monitoring function for individual cells
  Overvoltage detection threshold 4.25 V, Detection accuracy: ±15 mV (max)
  Undervoltage detection threshold 2.7 V, Detection accuracy: ±50 mV (max)

- Overcurrent detection function
  Discharge overcurrent detection threshold 150 mV, Detection accuracy: ±10 mV (max)
  Charge overcurrent detection threshold -40 mV, Detection accuracy: ±15 mV (max)

- Short circuit detection function
  Short circuit detection threshold 300 mV, Detection accuracy: ±15 mV (max)
  Detection delays adjustable using an external capacitor

- Temperature detection function : With external NTC (10 kΩ, B=3435) and 4.7 kΩ resistor
  Discharge inhibition temperature: 75 °C or higher
  Charge inhibition temperature : 55 °C or higher

- External charge/discharge FET control: NMOS-FET gate driver built-in
  External shut down command is accepted on the /CFOFF and /DFOFF pins
  In a cascade configuration external circuits can be minimized with the power-up control pin VRSO

- Cell number selectable from predefined 4 values using the CS0 and CS1 pins
  Product code 001 supports 7, 8, 9 or 10-cell connectivity
  Cell numbers and other parameters can be redefined and supplied as an individual product code

- Low current consumption
  Normal operation state : 25 µA (typ.), 60 µA (max)
  Power-down state : 0.1 µA (typ.), 1 µA (max)

- Supply voltage : +5 V to +60 V

- Operating temperature : -40°C to +85°C

- Package : 32-pin LQFP

■ Application

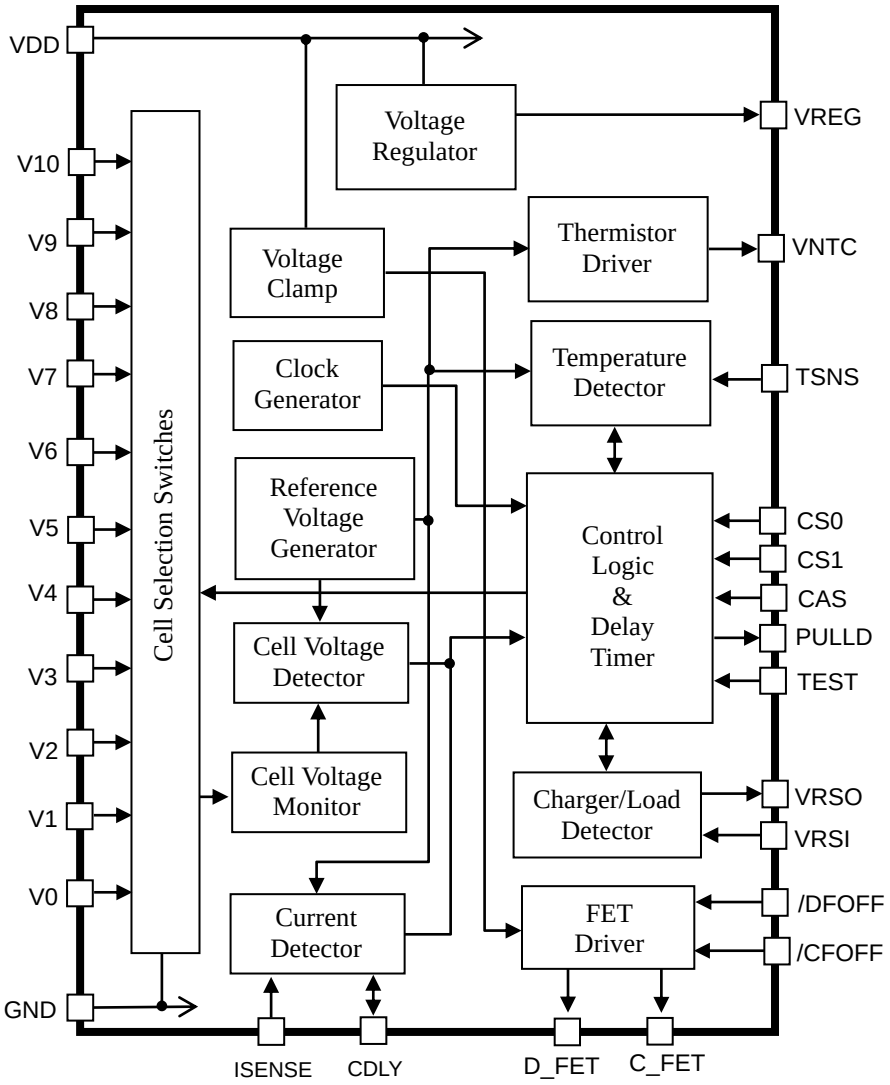
・Power tools and Garden tools
・Cordless Cleaner
・E-Bike and Electric assisted bicycle
・Uninterruptible Power Supplies (UPS)
・Energy Storage Systems (ESS)

■ Part number

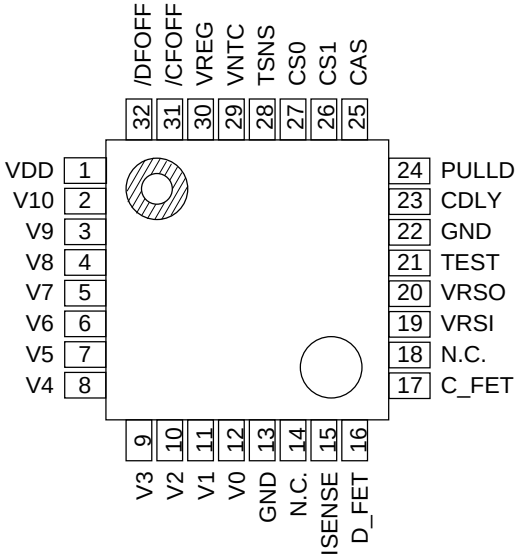
ML5233-001TC

ROHM SEMICONDUCTOR

■ Block Diagram



■ Pin Configuration (top view)



■ Pin Description

Pin No.	Pin	I/O	Description
1	VDD	—	Power supply input pin. Connect an external CR filter for noise rejection.
2	V10	I	Battery cell 10 high voltage input pin.
3	V9	I	Battery cell 10 low voltage input and Battery cell 9 high voltage input pin.
4	V8	I	Battery cell 9 low voltage input and Battery cell 8 high voltage input pin.
5	V7	I	Battery cell 8 low voltage input and Battery cell 7 high voltage input pin.
6	V6	I	Battery cell 7 low voltage input and Battery cell 6 high voltage input pin.
7	V5	I	Battery cell 6 low voltage input and Battery cell 5 high voltage input pin. Should be connected to GND for the 4 cell series connected battery pack application.
8	V4	I	Battery cell 5 low voltage input and Battery cell 4 high voltage input pin. Should be connected to GND for the 4 to 5 cell series connected battery pack application.
9	V3	I	Battery cell 4 low voltage input and Battery cell 3 high voltage input pin. Should be connected to GND for the 4 to 6 cell series connected battery pack application.
10	V2	I	Battery cell 3 low voltage input and Battery cell 2 high voltage input pin. Should be connected to GND for the 4 to 7 cell series connected battery pack application.
11	V1	I	Battery cell 2 low voltage input and Battery cell 1 high voltage input pin. Should be connected to GND for the 4 to 8 cell series connected battery pack application.
12	V0	I	Battery cell 1 low voltage input pin. Should be connected to GND for the 4 to 9 cell series connected battery pack application.
13, 22	GND	—	Ground pins.
15	ISENSE	I	Current sense resistor input pin. Connect a resistor of the resistance value corresponding to the detecting current between this pin and the GND pin. Should be tied to GND if not used.
16	D_FET	O	Discharge FET control signal output pin. Should be tied to the gate pin of the external NMOS FET.
17	C_FET	O	Charge FET control signal output pin. Should be tied to the gate pin of the external NMOS FET.
19	VRSI	IO	Negative terminal of the load/charger input pin. Load or charger presence is decided by this input level.
20	VRSO	O	Power-up signal output pin in cascade connection. Should be tied to the next upper VRSI pin.
21	TEST	I	LSI test input pin. Should be fixed to GND.
23	CDLY	IO	Short current detection delay time setting pin. Should be tied to GND through a capacitor.
24	PULLD	O	External pull-down control signal output for load removal detection. Should be tied to the gate of the external pull-down control NMOS-FET when cascaded.
25	CAS	I	Cascade mode selection input. Should be fixed to the VREG level when cascaded.
26	CS1	I	Pins to specify battery cell number. Either the VREG or the GND level should be applied.
27	CS0	I	
28	TSNS	I	Input pin for high temperature charge/discharge inhibition detection. Connect a thermistor between this pin and GND. Should be tied to the VNTC pin if not used.
29	VNTC	O	Thermistor power supply. Should be connected to TSNS through a 4.7 kΩ resistor. Should be pulled down with a 100 kΩ resistor if not used.
30	VREG	O	Built-in 4.3 V regulator output pin. Should be tied to GND through a 1 μF capacitor. Do not use this pin as power supply for an external circuit.
31	/CFOFF	I	OFF control command input pin for the charge FET. The "L" level input forces Hi-Z on the C_FET output. Should be tied to the next upper C_FET pin through an external resistor when cascaded.
32	/DFOFF	I	OFF control command input pin for the discharge FET. The "L" level input forces "L" on the D_FET output. Should be tied to the next upper D_FET pin through an external resistor when cascaded.
14, 18	N.C.	—	No connect. Leave them electrically unconnected.

■ Absolute Maximum Ratings

GND=0V, Ta=25°C

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Applied to VDD pin	-0.3 to +86.5	V
Input voltage	V_{IN1}	Applied to V0 to V10 pins	-0.3 to V_{DD}+0.3	V
	V_{IN2}	Applied to VRSI pin	V_{DD}-86.5 to V_{DD}+0.3	V
	V_{IN3}	Applied to /CFOFF and /DFOFF pins	-0.3 to +86.5	V
	V_{IN4}	Applied to CS0, CS1, CAS, TSNS, CDLY, and ISENSE pins	-0.3 to V_{REG}+0.3	V
	V_{IN5}	Applied to TEST pin	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT1}	Applied to D_FET and VRSO pins	-0.3 to V_{DD}+0.3	V
	V_{OUT2}	Applied to C_FET pin	V_{DD}-86.5 to V_{DD}+0.3	V
	V_{OUT3}	Applied to VREG pin	-0.3 to +6.5	V
	V_{OUT4}	Applied to VNTC and PULLD pins	-0.3 to V_{REG}+0.3	V
Power dissipation	P_D	—	1.0	W
Short-circuit output current	I_{OS}	Applied to VREG, VNTC, PULLD, C_FET, D_FET, and VRSO pins	10	mA
Storage temperature	T_{STG}	—	-55 to +150	°C

■ Recommended Operating Conditions

(GND= 0 V)

Item	Symbol	Condition	Range	Unit
Supply voltage	V_{DD}	Applied to VDD pin	5 to 60	V
Operational temperature	T_{OP}	—	-40 to +85	°C

■ Electrical Characteristics

● DC Characteristics

V_{DD}=5 V to 60 V, GND=0 V, Ta=-40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital "H" input voltage (Note 1)	V_{IH1}	—	0.8×V_{REG}	—	V_{REG}	V
Digital "L" input voltage (Note 1)	V_{IL1}	—	0	—	0.2×V_{REG}	V
Digital "H" input current (Note 1)	I_{IH1}	V_{IH} = V_{REG}	—	—	2	µA
Digital "L" input current (Note 1)	I_{IL1}	V_{IL} = GND	–2	—	—	µA
Cell monitoring pin Input current (Note 2)	I_{INVC}	Average current in normal operation mode	–0.1	0.1	3	µA
Cell monitoring pin Input leakage current (Note 2)	I_{ILVC}	Power-down mode	—	—	2	µA
FET "H" output voltage (Note 3)	V_{OH1}	I_{OH}=-10 µA V_{DD} =18 V to 60 V	10	14	18	V
FET "L" output voltage (Note 4)	V_{OL1}	I_{OL} = 100 µA	—	—	0.2	V
C_FET output leakage current	I_{LCF}	V_{CFET}= 0 V to V_{DD}	–5	—	5	µA
/CFOFF and /DFOFF pins "H" input voltage	V_{IH2}	—	V_{DD}-0.1	—	V_{DD}+18	V
/CFOFF and /DFOFF pins "L" input voltage	V_{IL2}	—	0	—	V_{DD}-1.5	V
/CFOFF and /DFOFF pins "H" input current	I_{IH2}	V_{IH2}=V_{DD}	—	—	2	µA
/CFOFF and /DFOFF pins "L" input current	I_{IL2}	V_{IL2}=0 V	–2	—	—	µA
PULLD pin "H" output voltage	V_{OH2}	I_{OH} = -100 µA	V_{REG}-0.4	—	V_{REG}	V
PULLD pin "L" output voltage	V_{OL2}	I_{OL} = 100 µA	—	—	0.1	V
CDLY pin "L" output voltage	V_{OL3}	I_{OL} = 100 µA	—	—	0.4	V
CDLY pin pull-up resistor	R_{PUC}	At short current detection	44	63	82	kΩ
VREG pin output voltage	V_{REG}	With load current 1 mA or less	3.8	4.3	4.8	V
VNTC pin output voltage	V_{NTC}	With 14.7 kΩ resistor connection	2.2	2.4	2.6	V
VNTC pin output leakage current	I_{LNTC}	V_{NTC}=0 V to 3.5 V	–2	—	2	µA
TSNS pin input leakage current	I_{ILTS}	V_{TSNS}=0 V to 3.5 V	–2	—	2	µA
ISENSE pin input leakage current	I_{ILIS}	V_{ISENSE}=0 V to 3.5 V	–2	—	2	µA
TEST pin pull-down resistance	R_{PDT}	—	50	100	200	kΩ

Note 1: Applied to CS0, CS1, and CAS pins.
Note 2: Applied to V0 to V10 pins.
Note 3: Applied to C_FET and D_FET pins.
Note 4: Applied to D_FET pin.
Note 5: Applied to C_FET pin.

● Supply Current Characteristics

V_{DD}= 5 to 60 V, GND=0 V, Ta=-40 to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in normal operation	I_{DD}	No output load	—	25	60	µA
Current consumption in power-down mode	I_{DDS}	No output load	—	0.1	1.0	µA

- Detection/Release Threshold Characteristics (Ta = 25 °C)

V_{DD}=36 V, GND=0 V, Ta=+25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.235	4.25	4.265	V
Overvoltage release threshold	V_{OVR}	—	3.95	4.00	4.05	V
Undervoltage detection threshold	V_{UV}	—	2.65	2.70	2.75	V
Undervoltage release threshold	V_{UVR}	—	2.95	3.00	3.05	V
Discharge overcurrent detection threshold	V_{OCU}	—	140	150	160	mV
Charge overcurrent detection threshold	V_{OCO}	—	-55	-40	-25	mV
Short circuit detection threshold	V_{SHRT}	—	285	300	315	mV
High temperature charge inhibition detection threshold	V_{CHD}	—	0.99	1.02	1.05	V
High temperature charge inhibition release threshold	V_{CHR}	—	1.16	1.21	1.26	V
High temperature discharge inhibition detection threshold	V_{DHD}	—	670	700	730	mV
High temperature discharge inhibition release threshold	V_{DHR}	—	800	850	900	mV

- Detection/Release Threshold Characteristics (Ta = 0 to 60 °C)

V_{DD}=36 V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection threshold	V_{OV}	—	4.225	4.25	4.275	V
Overvoltage release threshold	V_{OVR}	—	3.93	4.00	4.07	V
Undervoltage detection threshold	V_{UV}	—	2.6	2.7	2.8	V
Undervoltage release threshold	V_{UVR}	—	2.9	3.0	3.1	V
Discharge overcurrent detection threshold	V_{OCU}	—	135	150	165	mV
Charge overcurrent detection threshold	V_{OCO}	—	-65	-40	-15	mV
Short circuit detection threshold	V_{SHRT}	—	270	300	330	mV
High temperature charge inhibition detection threshold	V_{CHD}	—	0.97	1.02	1.07	V
High temperature charge inhibition release threshold	V_{CHR}	—	1.14	1.21	1.28	V
High temperature discharge inhibition detection threshold	V_{DHD}	—	650	700	750	mV
High temperature discharge inhibition release threshold	V_{DHR}	—	780	850	920	mV
VREG drop detection threshold	V_{UREG}	—	3.0	3.4	3.8	V
VREG drop release threshold	V_{RREG}	—	3.4	3.8	4.2	V

- Charger Detection / Removal and Load Removal Threshold Characteristics (Ta=25 °C)

V_{DD}=36 V, GND=0 V, Ta=+25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Charger detection VRSI threshold	V_{PC}	Wake-up from power-down mode	V_{DD}X0.4	V_{DD}X0.5	V_{DD}X0.6	V
Charger removal VRSI threshold	V_{PLU1}	In charge overcurrent state CAS pin = "L"	0.1	0.2	0.3	V
	V_{PLU2}	In charge overcurrent state CAS pin = "H"	0.3	0.4	0.5	V
	V_{PLD}	Power-down mode	V_{DD}X0.7	V_{DD}X0.75	V_{DD}X0.8	V
Load removal VRSI threshold	V_{RL}	In discharge overcurrent state	2.2	2.4	2.6	V

- Charger Detection / Removal and Load Removal Threshold Characteristics (Ta=0 to 60 °C)

V_{DD}=36 V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Charger detection VRSI threshold	V_{PC}	Wake-up from power-down mode	V_{DD}X0.35	V_{DD}X0.5	V_{DD}X0.65	V
Charger removal VRSI threshold	V_{PLU1}	In charge overcurrent state CAS pin = "L"	0	0.2	0.4	V
	V_{PLU2}	In charge overcurrent state CAS pin = "H"	0.2	0.4	0.6	V
	V_{PLD}	Power-down mode	V_{DD}X0.65	V_{DD}X0.75	V_{DD}X0.85	V
Load removal VRSI threshold	V_{RL}	In discharge overcurrent state	2.0	2.4	2.8	V
VRSI pin pull-up resistance	R_{PU}	In charge overcurrent state, power-down mode	200	500	1000	kΩ
VRSI pin pull-down resistance	R_{PD}	In discharge overcurrent state CAS pin = "L"	0.5	2	4	MΩ
VRSI pin input current	I_{LPS1}	Without pull-up/-down resistor CAS pin = "L"	-2	—	2	µA
	I_{LPS2}	Without pull-up/-down resistor CAS pin = "H"	-3	-0.2	2	µA
VRSO pin output current	I_{OL}	CAS pin = "H" VRSI pin = "L" V_{OL} = 5 V	0.5	1	2	µA
VRSO pin output leakage current	I_{OLK}	VRSI pin = "H" V_{RSO} = 36 V	0	—	2	µA
VRSO pin pull-down resistance	R_{PDR}	CAS pin = "H" at wake-up	200	500	1000	kΩ

- Detection Delay and Monitor Cycle Characteristics (Ta = 25 °C)

V_{DD}=36 V, GND=0 V, Ta=+25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection delay (Note)	t_{OV}	—	2.6	3.0	4.0	sec
Undervoltage detection delay (Note)	t_{UV}	—	0.85	1.00	1.65	sec
Charge overcurrent detection delay	t_{OCO}	—	70	100	130	ms
Discharge overcurrent detection delay	t_{OCU}	—	70	100	130	ms
Short circuit detection delay	t_{SC}	C_{DLY}=10 nF	0.7	1.0	1.3	ms
Cell voltage monitor cycle	t_{DET}	—	320	400	480	ms
Temperature monitor cycle	t_{PT}	—	320	400	480	ms
Temperature measurement time	t_{TM}	—	2.3	3	3.7	ms
Load removal delay	t_{ORL}	—	70	100	130	ms
Charger removal delay	t_{OCHG}	—	70	100	130	ms
Internal source oscillation clock cycle	t_{OSC}	—	85	100	115	µs
Overvoltage detection delay for test mode (Note)	t_{OVT}	TSNS pin = V_{REG}	70	100	610	ms
Undervoltage detection delay for test mode (Note)	t_{UVT}	TSNS pin = V_{REG}	70	100	610	ms
Cell voltage monitor cycle for test mode	t_{DETT}	TSNS pin = V_{REG}	70	100	130	ms
Temperature monitor cycle for test mode	t_{PTT}	TSNS pin = V_{REG}	70	100	130	ms
TSNS pin input voltage for test mode	V_{TST}	—	V_{REG}-0.3	—	V_{REG}	V

(Note) Time lag due to cell voltage monitor cycle should be added on top of these values.

- Detection Delay and Monitor Cycle Characteristics (Ta = 0 to 60 °C)

V_{DD}=36 V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Overvoltage detection delay (Note)	t_{OV}	—	2.4	3.0	4.2	sec
Undervoltage detection delay (Note)	t_{UV}	—	0.80	1.00	1.75	sec
Charge overcurrent detection delay	t_{OCO}	—	50	100	150	ms
Discharge overcurrent detection delay	t_{OCU}	—	50	100	150	ms
Short circuit detection delay	t_{SC}	C_{DLY}=10 nF	0.6	1.0	1.4	ms
Cell voltage monitor cycle	t_{DET}	—	300	400	500	ms
Temperature monitor cycle	t_{PT}	—	300	400	500	ms
Temperature measurement time	t_{TM}	—	2	3	4	ms
Load removal delay	t_{ORL}	—	50	100	150	ms
Charger removal delay	t_{OCHG}	—	50	100	150	ms
Internal source oscillation clock cycle	t_{OSC}	—	80	100	120	µs

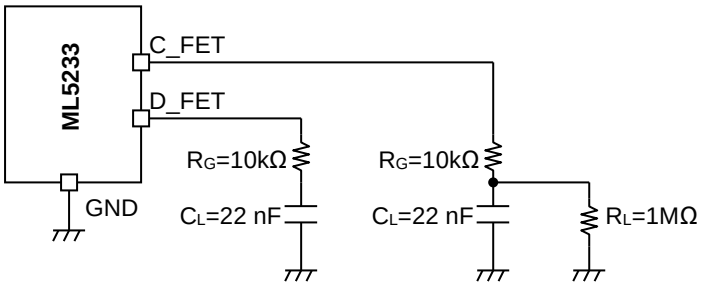
(Note) Time lag due to cell voltage monitor cycle should be added on top of these values.

- Transient Characteristics

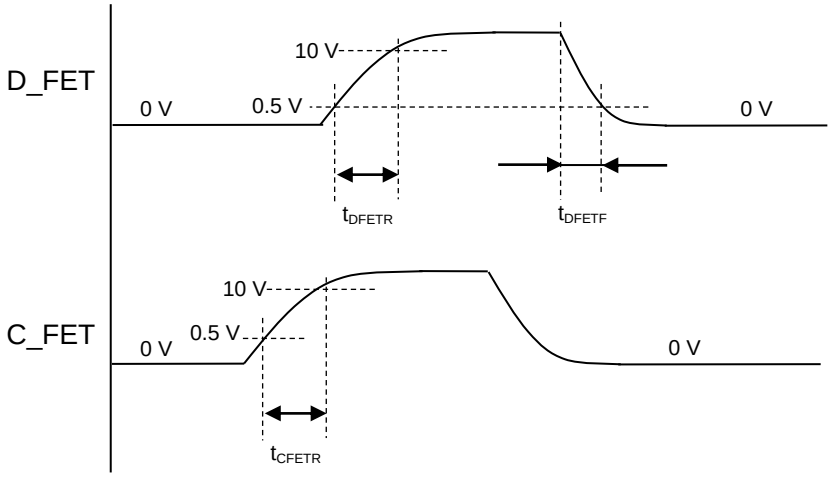
V_{DD}=36 V, GND=0 V, Ta=0 to 60°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
D_FET pin output rise time	t_{DFETR}	C_L=22 nF, R_G=10 kΩ	—	95	400	µs
C_FET pin output rise time	t_{CFETR}	C_L=22 nF, R_G=1 0kΩ R_L=1 MΩ	—	95	400	µs
D_FET pin output fall time	t_{FETF}	C_L=22 nF, R_G=10 kΩ	—	1	150	µs

◆Measurement circuit



◆Timing Diagrams

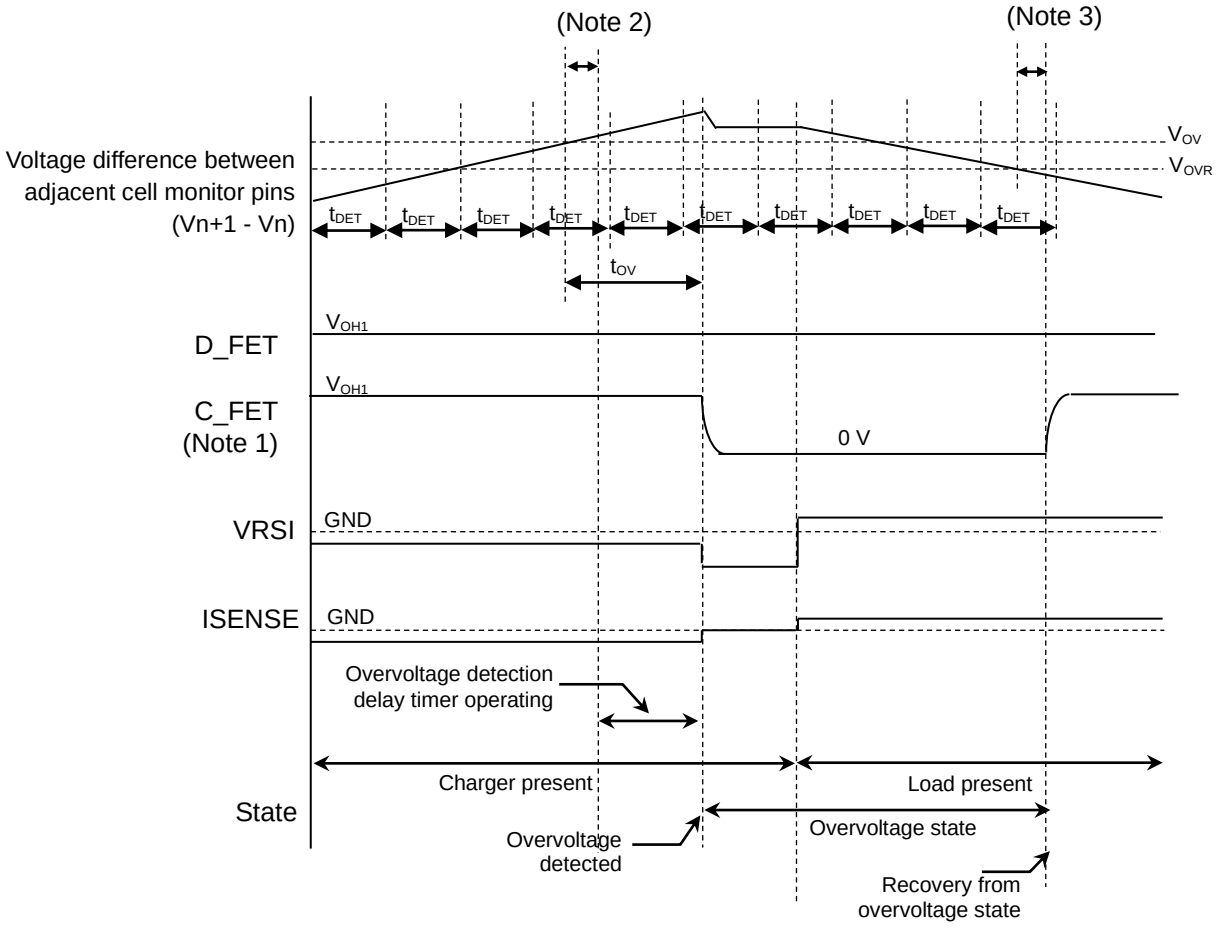


(Note) C_FET output fall depends on the time constant of the external loads R_L and C_L

■ Timing Diagrams

This section shows the timing diagrams of application circuit example 1 (without cascade connection).

● Overvoltage Detection and Recovery

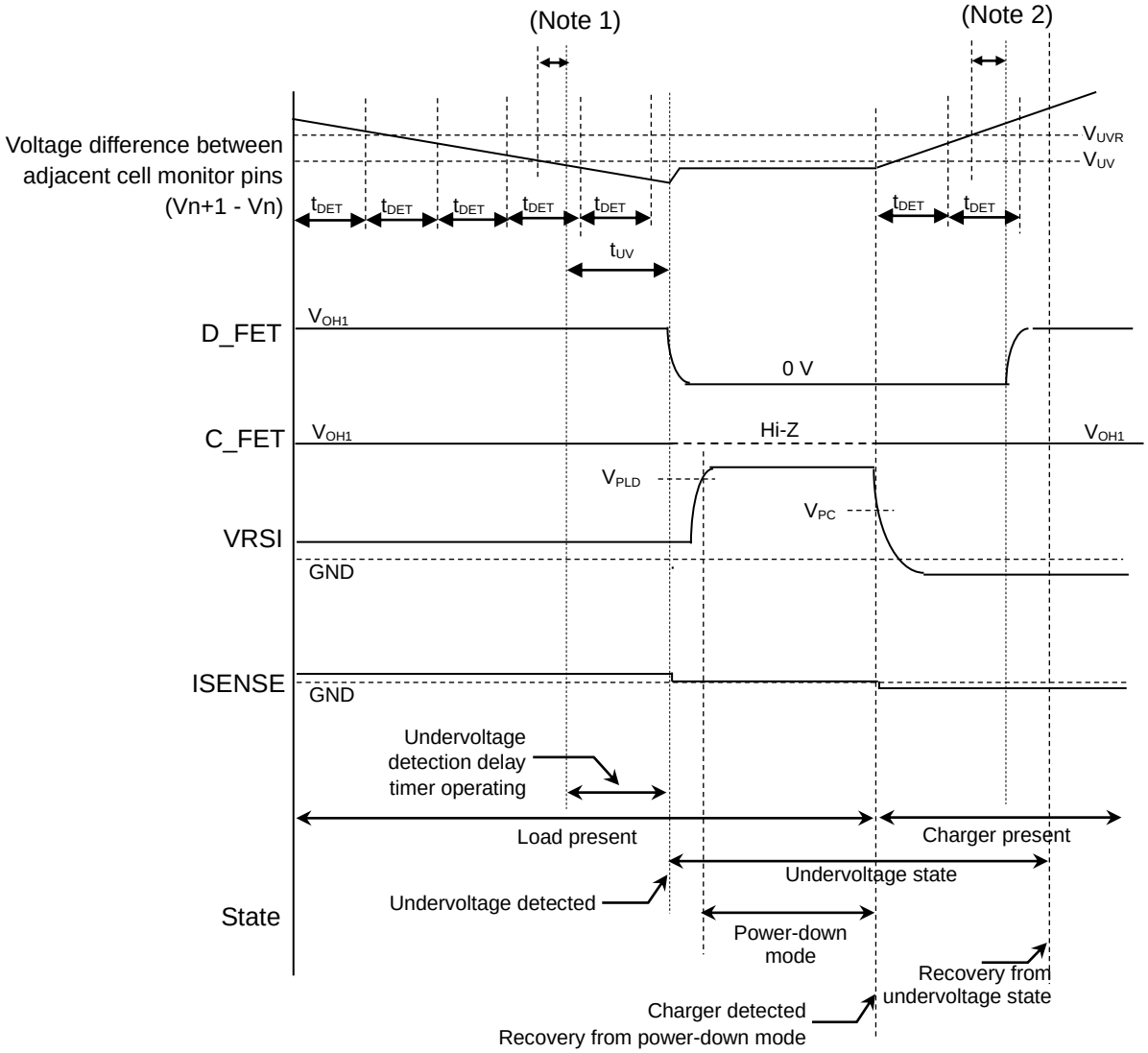


(Note 1) C_FET pin is pulled down with a resistor.

(Note 2) Even if the voltage difference between Vn+1 and Vn reaches or exceeds the overvoltage detection threshold V_{OV}, there may be a time lag before starting the overvoltage detection delay timer because cell voltages are monitored every 400 ms (typ.).

(Note 3) Even if the voltage difference between Vn+1 and Vn reaches or exceeds the overvoltage release threshold V_{OVR}, there may be a time lag before recovering from the overvoltage state because cell voltages are monitored every 400 ms (typ.).

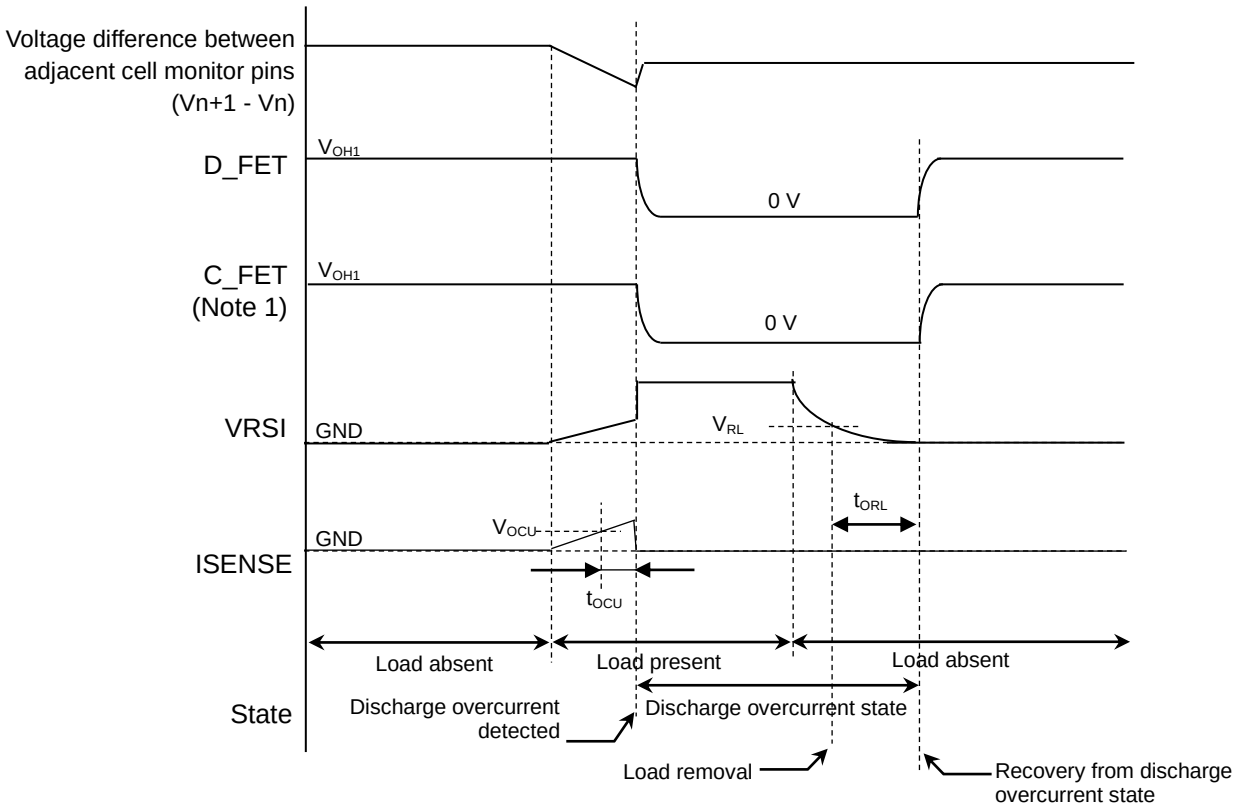
- Overvoltage Detection, Transition to Power-down Mode and Recovery



(Note 1) Even if the voltage difference between Vn+1 and Vn reaches or exceeds the undervoltage detection threshold V_{UV}, there may be a time lag before starting the undervoltage detection delay timer because cell voltages are monitored every 400 ms (typ.).

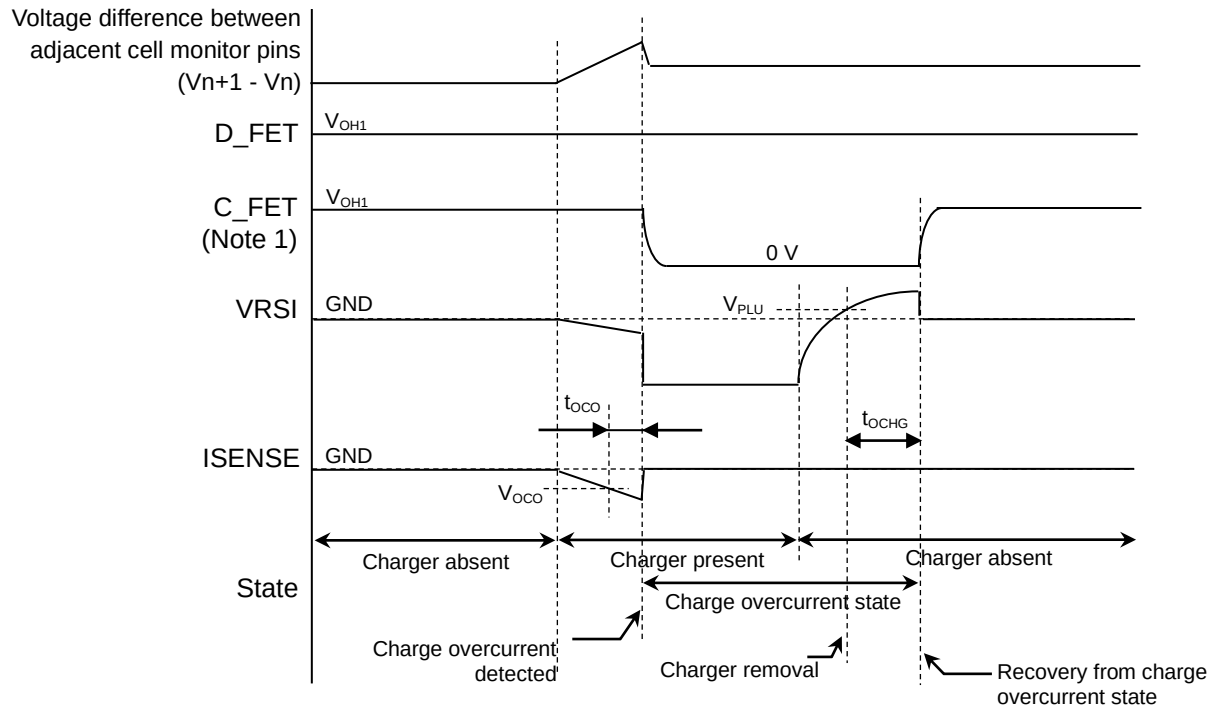
(Note 2) Even if the voltage difference between Vn+1 and Vn reaches or exceeds the undervoltage release threshold V_{UVR}, there may be a time lag before recovering from the undervoltage state because cell voltages are monitored every 400 ms (typ.).

- Discharge Overcurrent Detection and Recovery



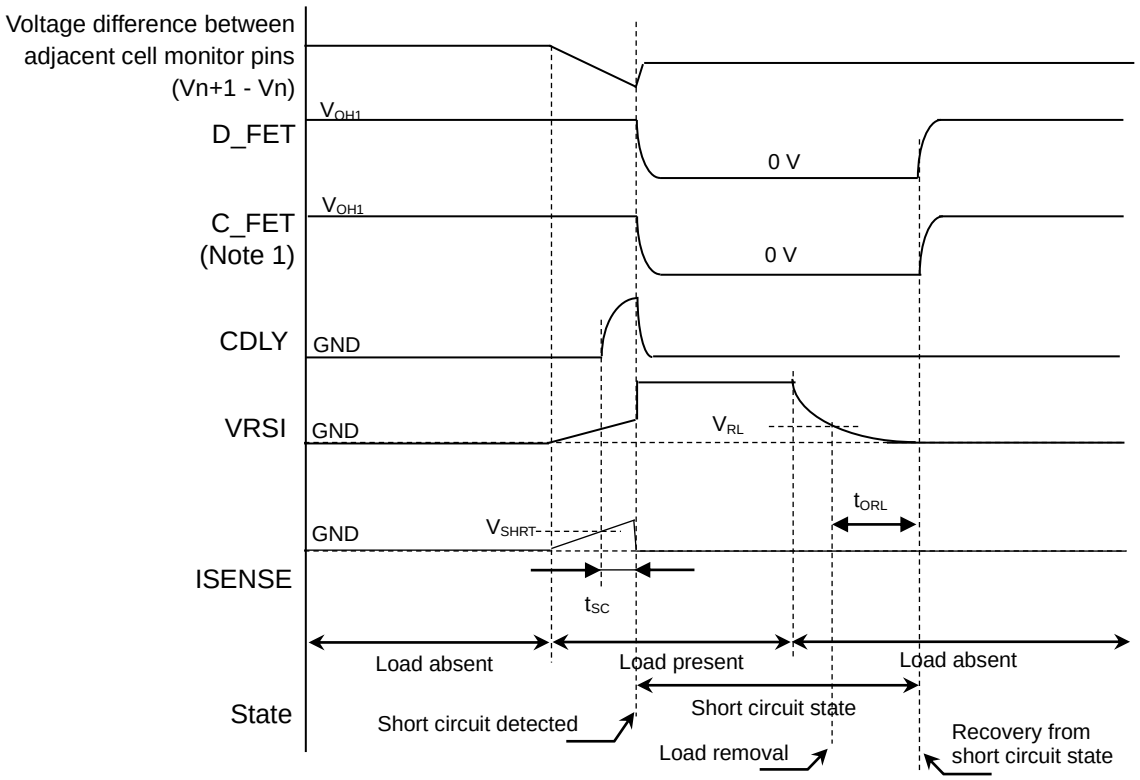
(Note 1) C_FET pin is pulled down with a resistor.

- Charge Overcurrent Detection and Recovery



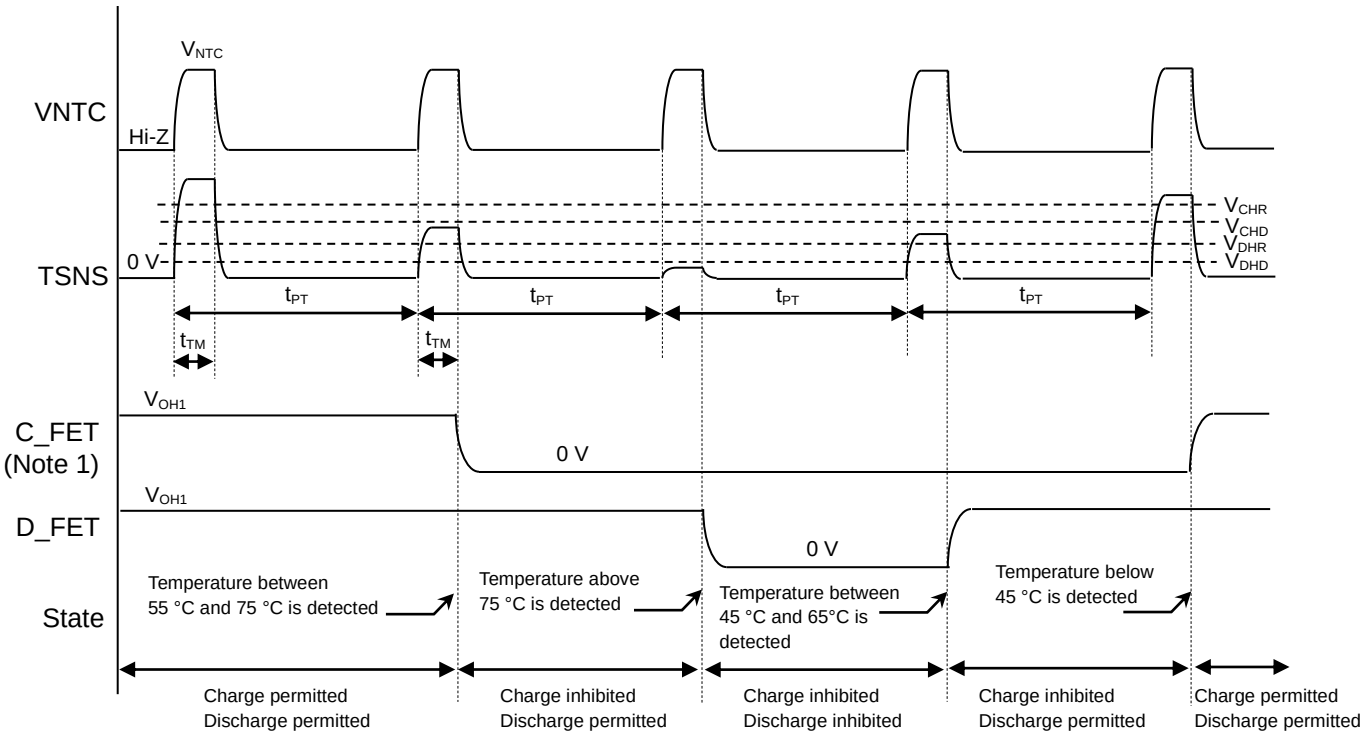
(Note 1) C_FET pin is pulled down with a resistor.

- Short Circuit Detection and Recovery



(Note 1) C_FET pin is pulled down with a resistor.

- High Temperature Detection and Recovery



(Note 1) C_FET pin is pulled down with a resistor.
(Note 2) NTC(10kΩ,B=3435) and 4.7kΩ resistor is connected.

■ Functional Description

● States of ML5233

The ML5233 has the following eight states which depend on individual cell voltages and the input levels of the ISENSE and TSNS pins.

1. Initial state
2. Normal operation state
3. Overvoltage state
4. Undervoltage state (including power-down mode)
5. Discharge overcurrent state
6. Charge overcurrent state
7. Short circuit state
8. High temperature state

Each state is described below, without cascade connection (CAS pin fixed to GND).

1. Initial State

The initial state refers to the period while the battery cells are being connected to the ML5233 and connection of all the battery cells specified by the CS0 and CS1 pins is completed, before transitioning to the normal state. In the initial state, when the VREG pin voltage reaches or exceeds the VREG drop detection threshold, the D_FET pin output is set to the "L" level and the C_FET pin output to the "H" level, where discharge is inhibited and charge is permitted.

When the VREG pin level reaches or exceeds the VREG drop release threshold, individual cell voltage monitoring takes place. If all the battery cells specified by the CS0 and CS1 pins reach or exceed the undervoltage release threshold V_{UVR}, the system transitions to the normal state. Overvoltage and overcurrent detection is also performed in parallel.

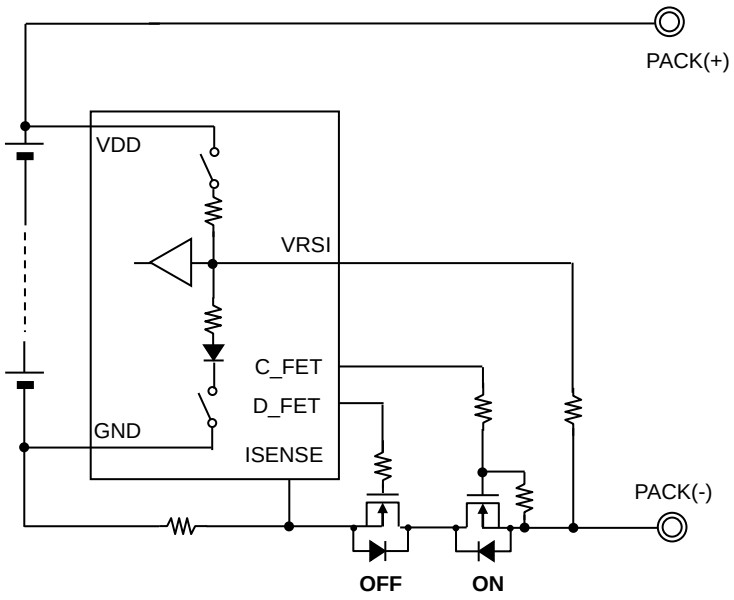


Figure 1 Initial State

2. Normal Operation State

The normal state refers to the period where all the battery cell voltages do not reach or exceed the overvoltage/undervoltage detection threshold, the ISENSE pin voltage is below the overcurrent detection threshold, and the TSNS pin voltage is above the high temperature detection threshold. In the normal state, both the D_FET and C_FET pin outputs are set to the "H" level, where both charge and discharge is permitted.

Individual cell voltages are monitored every 0.4 second for performing overvoltage/undervoltage detection, while the pack temperature is also monitored using an external thermistor every 0.4 second. The ISENSE pin voltage is always monitored to detect overcurrent in parallel.

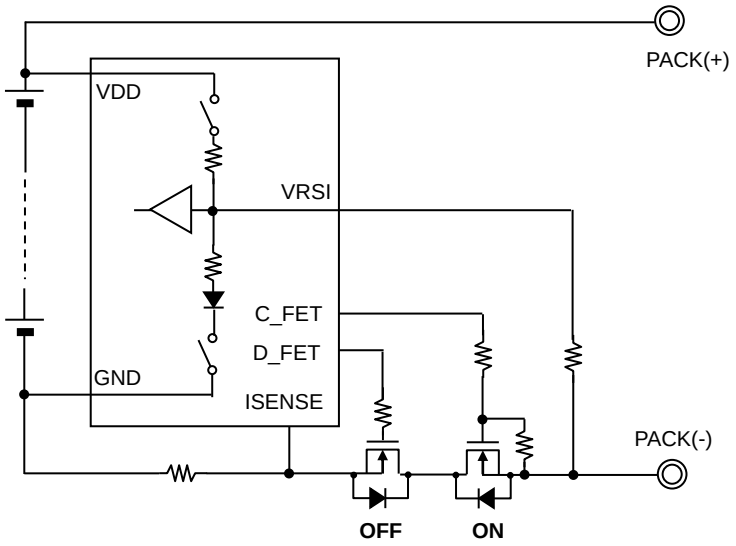


Figure 2 Normal Operation State

3. Overvoltage State

When any one or more battery cell voltages reach or exceed the overvoltage detection threshold V_{OV} for longer than the overvoltage detection delay time $t_{OV,}$ the system enters the overvoltage state. In the overvoltage state, the C_FET pin output is set to "Hi-Z" to inhibit charge, while the D_FET pin output maintains the value in the previous state.

Battery cell voltages decrease gradually by self-discharge or a connected light load. When all of them reach or exceed the overvoltage detection release threshold V_{OVR}, the system recovers from the overvoltage state.

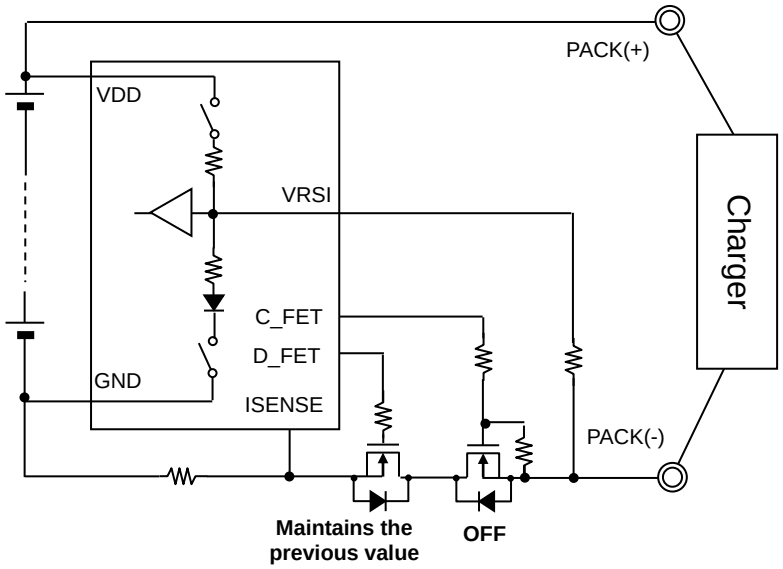


Figure 3 Overvoltage State

4. Undervoltage State

When any one or more battery cell voltages reach or exceed the undervoltage detection threshold V_{UV} for longer than the undervoltage detection delay time t_{UV}, the system enters the undervoltage state. In the undervoltage state, the D_FET pin output is set to the "L" level to inhibit discharge, while the C_FET pin output maintains the value in the previous state.

In the undervoltage state, a 500 kΩ pull-up resistor is connected between the VRSI pin and VDD. When the VRSI pin voltage increases and reaches the charger removal VRSI threshold V_{PLD} after turning off the external discharge FET, the system enters power-down mode to reduce current consumption. The VRSI pin voltage decreases when a charger is present. If it reaches or exceeds the charger detection voltage V_{PC}, the system wakes up all the circuits to resume monitoring individual battery cell voltages.

If the system was in the overvoltage, undervoltage, high temperature or any overcurrent state before entering power-down mode, these error flags are cleared during power-down. After wake-up, if these errors are detected again for longer than the specified detection delay time, the system reenters the corresponding error state.

Battery cell voltages increase gradually while charging, and if all cell voltages reach or exceed the undervoltage detection release threshold V_{UVR}, the system recovers from the undervoltage state and the pull-up resistor between VRSI pin and VDD is disconnected.

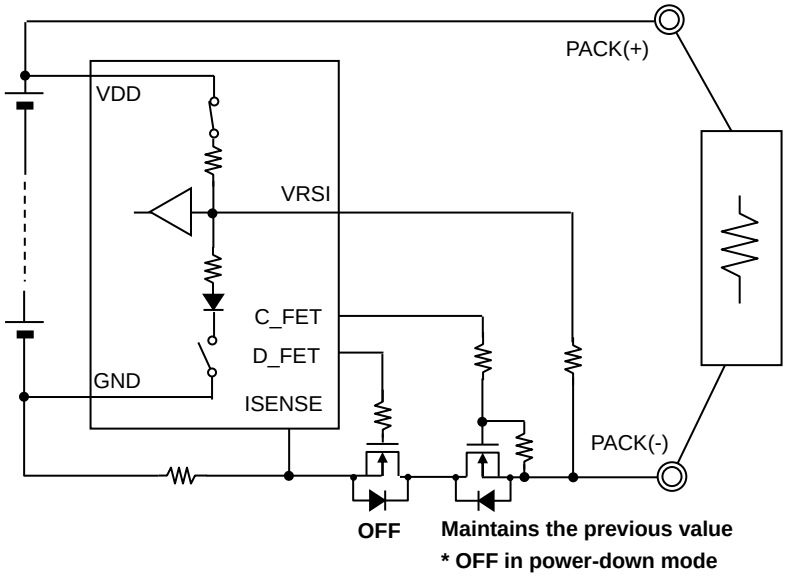


Figure 4 Undervoltage State (Power-down mode)

5. Discharge Overcurrent State

When the load is connected and ISENSE pin voltage reaches or exceeds the discharge overcurrent detection threshold V_{OCU} for longer than the discharge overcurrent detection delay time t_{OCU}, the system enters the discharge overcurrent state, regardless of the individual battery cell voltages. In the discharge overcurrent state, the D_FET pin output is set to the "L" level to inhibit discharge, while the C_FET pin output is set to "Hi-Z" to monitor load removal.

In the discharge overcurrent state, the VRSI pin is pulled-down with a 2 MΩ resistor and a backflow prevention diode. If the load is released, the VRSI pin level approaches the GND level. The system recovers from the discharge overcurrent state when the VRSI pin level reaches or exceeds the load disconnection detection threshold V_{RL} for longer than the load disconnection detection delay time t_{ORL} .

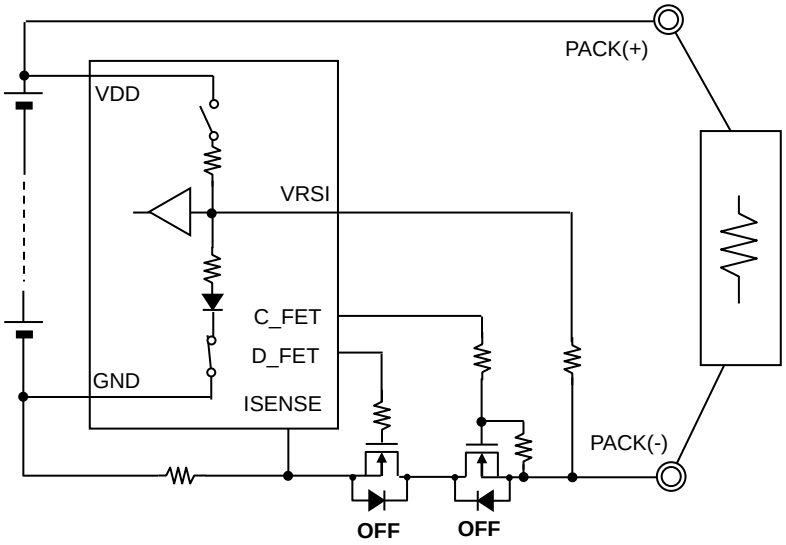


Figure 5 Discharge Overcurrent State

6. Charge Overcurrent State

When the charger is connected and ISENSE pin voltage reaches or exceeds the charge overcurrent detection threshold V_{OCO} for longer than the charge overcurrent detection delay time t_{OCO}, the system enters the charge overcurrent state, regardless of the individual battery cell voltages. In the charge overcurrent state the C_FET pin output is set to "Hi-Z" to inhibit charge, while the D_FET pin output maintains the value in the previous state.

In the charge overcurrent state, a 500 kΩ pull-up resistor is connected between the VRSI pin and VDD pin to detect charger removal. If the charger is removed, the VRSI pin level increases. The system recovers from the charge overcurrent state when the VRSI pin voltage reaches or exceeds the charger removal detection threshold V_{PLU} for longer than the charger removal delay time t_{OCHG}.

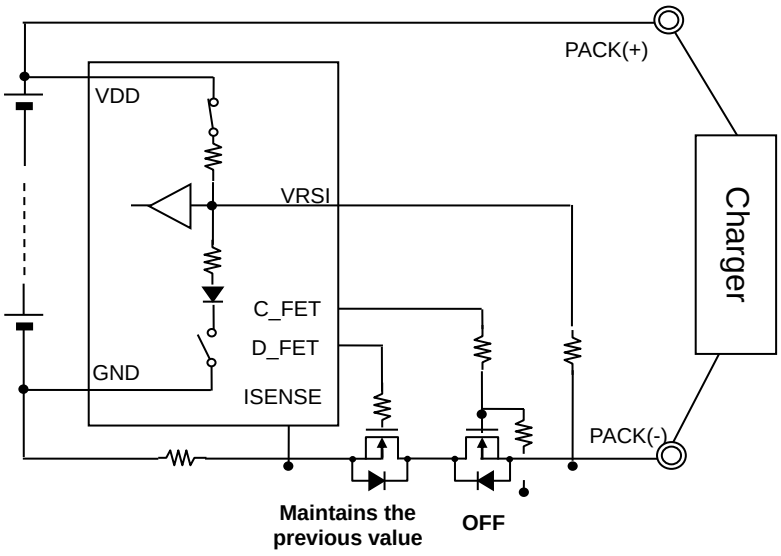


Figure 6 Charge Overcurrent State

7. Short Circuit State

When the pack is overloaded and the ISENSE pin voltage reaches or exceeds the short circuit detection threshold V_{SHRT}, the capacitor connected to the CDLY pin is started to charge, regardless of the battery cell voltages. When the CDLY pin voltage is increased to a specific level, the system enters the short circuit state. In the short circuit state, the D_FET pin output is set to "L" level to inhibit discharge, while the C_FET pin output is set to "Hi-Z" to detect load removal. Also, a 2 MΩ pull-down resistor is connected between the VRSI pin and the GND pin through a backflow prevention diode.

If the load is removed, the VRSI pin level approaches the GND level. The system recovers from the short circuit state when the VRSI pin level reaches or exceeds the load removal detection threshold V_{RL} for longer than the load removal detection delay time t_{ORL}.

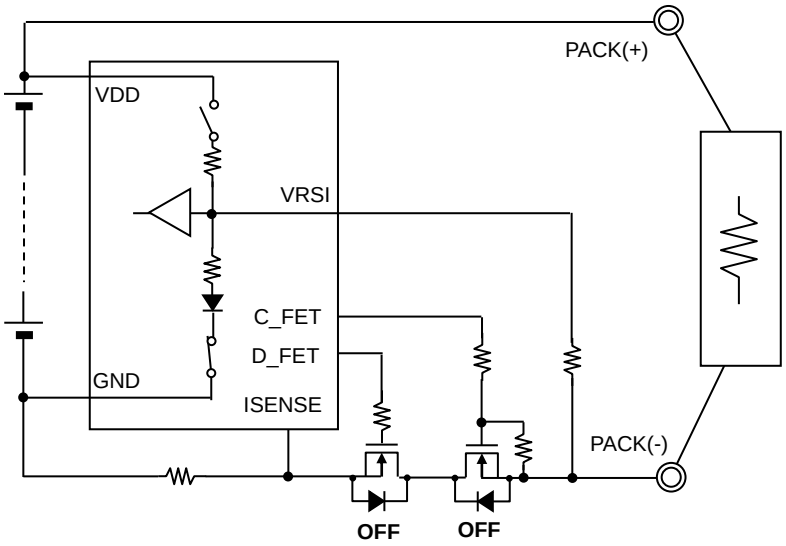


Figure 7 Short Circuit State

8. High Temperature State

Pack temperature is monitored using an external thermistor every 0.4 seconds when the ML5233 is not in power-down mode, regardless of battery cell voltages. When the TSNS pin voltage reaches or exceeds the high temperature charge inhibition detection threshold V_{CHD}, the C_FET pin output is set to the "Hi-Z" state to inhibit charge.

As temperature increases further, if the TSNS pin voltage reaches or exceeds the high temperature discharge inhibition detection threshold V_{DHD}, the D_FET pin output is set to the "L" level to inhibit discharge. Temperature monitoring is continued every 0.4 second in the high temperature state, too, and if the TSNS pin voltage reaches or exceeds the high temperature release threshold, the system recovers from the high temperature state.

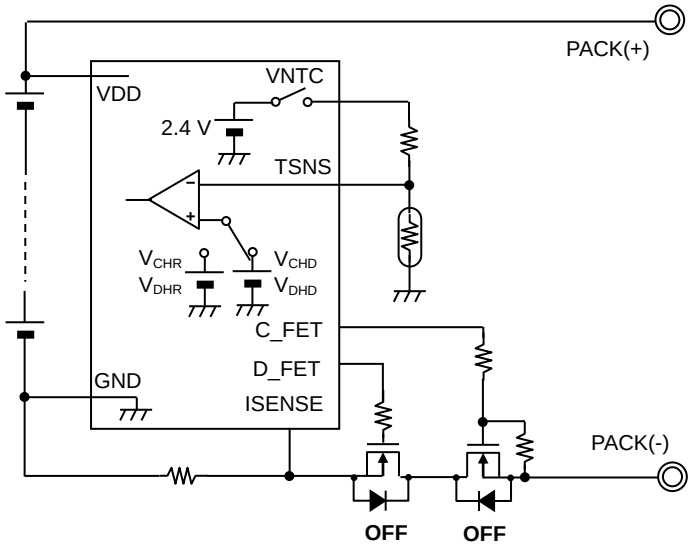


Figure 8 High Temperature State

- Selecting the Number of Battery Cells

Cell count is selectable from predefined 4 values using the CS0 and CS1 pins.
Product code 001 supports 7, 8, 9 or 10 cells, and its configuration is given in the table below.

CS1	CS0	Battery cell number	Unused Vn pins
GND	GND	10 cell	None
GND	VREG	9 cell	V0
VREG	GND	8 cell	V0, V1
VREG	VREG	7 cell	V0, V1, V2

All unused Vn pins should be tied to GND.

- Power-on/Power-off Sequence

Battery cells can be connected in any order, but it is recommend that the GND and VDD pins are connected first, and then connection continues from lower to higher voltage cells. There are no restrictions on the power supply voltage rise time at power-on, and power-off sequence or power supply voltage fall time at power-off.

After power-on, the system usually transitions to the normal state. However, it may transition to the undervoltage state due to chattering at power-on or other reasons. If it has transitioned to the undervoltage state and moved to power-down mode, apply the charger connection detection threshold V_{PC} or lower level to the VRSI pin to power it up again.

- Handling VDD Pin and V0 to V10 Pins

Since the VDD pin is the power supply input, put a noise elimination RC filter in front of the VDD input for stabilization. If the drive current on the external charge/discharge control FETs is large, the resistor value of this noise filter should be adjusted so that the voltage drop across the resistor is smaller than 1 V.

The V0 to V10 pins are the monitor pins for individual cell voltages. Put a noise elimination RC filter in front of each battery cell to prevent false detection. On a system with less than 10 battery cells, unused Vn pins should be tied to GND.

- Handling VREG Pin

The VREG pin is the power source of the built-in regulator which supplies power to the internal modules. Connect a 1 µF or larger capacitor between this pin and GND for stabilization. Do not use it as a power supply for external circuits since the supply current of the built-in regulator is limited.

- Setting Short Circuit Detection Delay

The short circuit detection delay (t_{SC}) depends on the charge time of the capacitor (C_{DLY}) connected to the CDLY pin, which is described by the following equation.

Short circuit detection delay t_{SC} [ms] = C_{DLY} [nF] × 0.1

A 1 nF or larger capacitor is recommended for C_{DLY}. For a smaller capacitance, 20 µs (typ.) should be added as a delay for the short current detection comparator. Note that the external CR filter on the ISENSE pin also comprises the total delay.

- External Control of Charge/Discharge Control FET

The C_FET and D_FET pin output values can be directly controlled by the /CFOFF and /DFOFF pin inputs, regardless of the detected state on the ML5233.
When the /CFOFF pin input is set to "L", the C_FET pin output is fixed to “Hi-Z”.
When the /DFOFF pin input is set to "L", the D_FET pin output is fixed to GND.
When the /CFOFF and /DFOFF pin inputs are set to "H", the C_FET and D_FET pin outputs depend on the detected state on the ML5233.

- Output Pin Values in Each Detection State

The output pin values in each detection state are shown in the table below.

State	D_FET	C_FET	VRSI	VREG
Initial state	GND	14 V	Hi-Z	4.3 V
Normal operation state	14 V	14 V	Hi-Z	4.3 V
Overvoltage state	No change	Hi-Z	No change	4.3 V
Undervoltage state	GND	No change	Pull-up	4.3 V
Power-down mode	GND	Hi-Z	Pull-up	0 V
Discharge overcurrent state	GND	Hi-Z	Pull-down	4.3 V
Charge overcurrent state	No change	Hi-Z	Pull-up	4.3 V
Short circuit state	GND	Hi-Z	Pull-down	4.3 V
High temperature charge inhibition state	No change	Hi-Z	No change	4.3 V
High temperature discharge inhibition state	GND	Hi-Z	No change	4.3 V

(Note) "No change" means that the previous pin value is maintained in a new state.

- Unused Pin Treatment

The following table shows how to handle unused pins.

Unused pins	Recommended treatment
V0 to V5	Pull down
ISENSE	Pull down
CDLY	Open
/CFOFF,/DFOFF	Pull up
VRSO	Open
TSNS	Tied to the VNTC pin
VNTC	Pull down with a 100 kΩ resistor
PULLD	Open

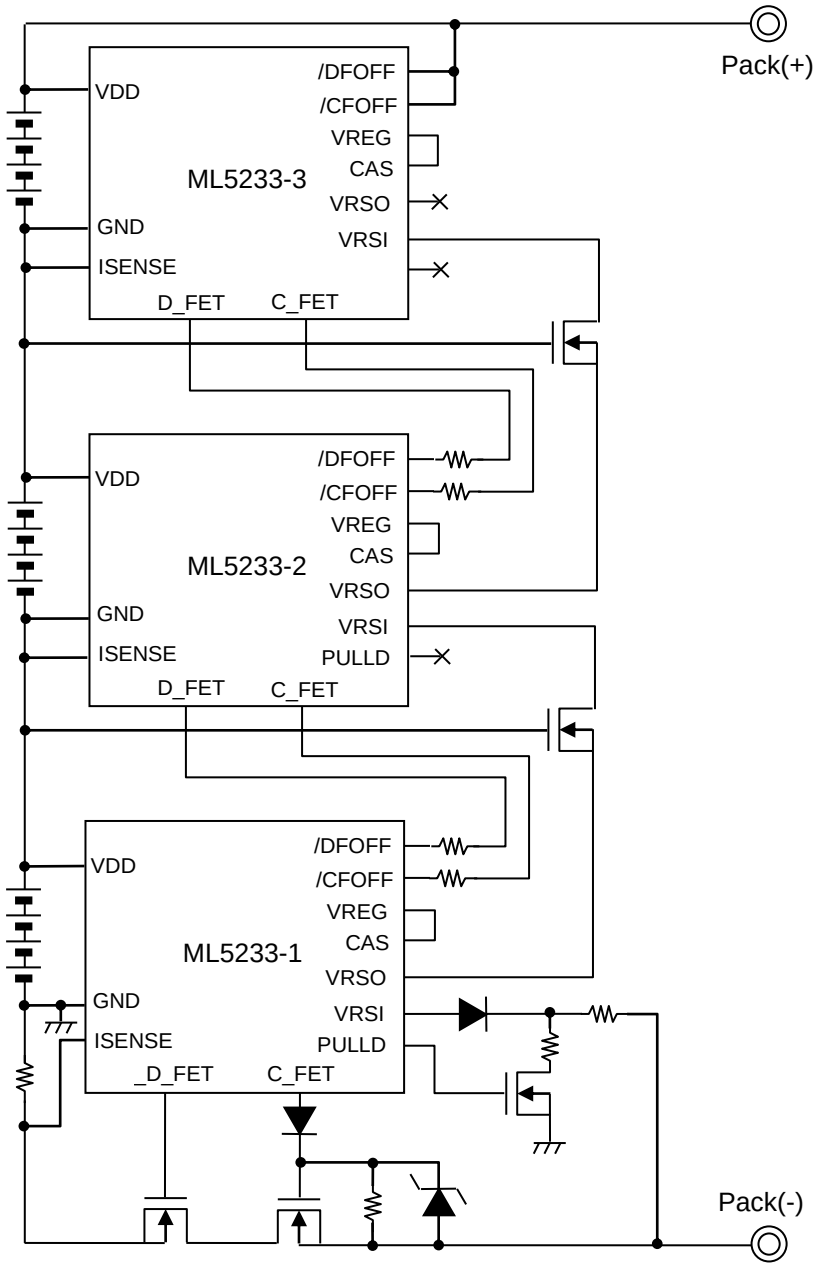
- Reducing Monitor Cycles and Detection Delays

The cell monitor cycle and overvoltage/undervoltage detection delays are reduced to 100 ms (typ.) by applying the VREG level to the TSNS pin. The temperature monitor cycle is also reduced to 100 ms (typ.), but high temperature detection does not work because the TSNS pin is fixed to the VREG level.

- Cascade Connection

Cascade wiring for three ML5233 devices is shown below.

1. Fix the CAS pin to the VREG level.
2. Connect the higher C_FET pin and the lower /CFOFF pin through a resistor.
3. Connect the higher D_FET pin and the lower /DFOFF pin through a resistor.
4. Connect the highest /CFOFF and /DFOFF pins to VDD pin.
5. Connect the lower VRSO pin and the higher VRSI pin through an NMOS-FET.
6. Connect the lowest VRSI pin to Pack(-) through a diode and a resistor.
7. Leave the top VRSO pin electrically open.
8. Connect the lowest PULLD pin to the NMOS-FET gate, whose drain terminal should be tied to Pack(-) through a resistor.



It is recommended that a greater number of cells should be assigned to the lowest IC to drive the charge/discharge control FETs on the GND correctly. For example, when 7 cells and 10 cells are cascaded, the 10 cells should be assigned to the lower IC and the 7 cells to the higher one.

- Redefinition of Battery Cell Number

4 cell numbers can be redefined so that one of them is selectable with CS0 and CS1 in the range shown in the following table.

CS1	CS0	Range of cell numbers						
GND	GND	4	5	6	7	8	9	10
GND	VREG	4	5	6	7	8	9	10
VREG	GND	4	5	6	7	8	9	10
VREG	VREG	4	5	6	7	8	9	10

- Redefinition of Detection/Release Threshold Range and Step

The detection/release thresholds can be redefined as shown in the following table.
Since some combinations are unavailable, contact us for details.

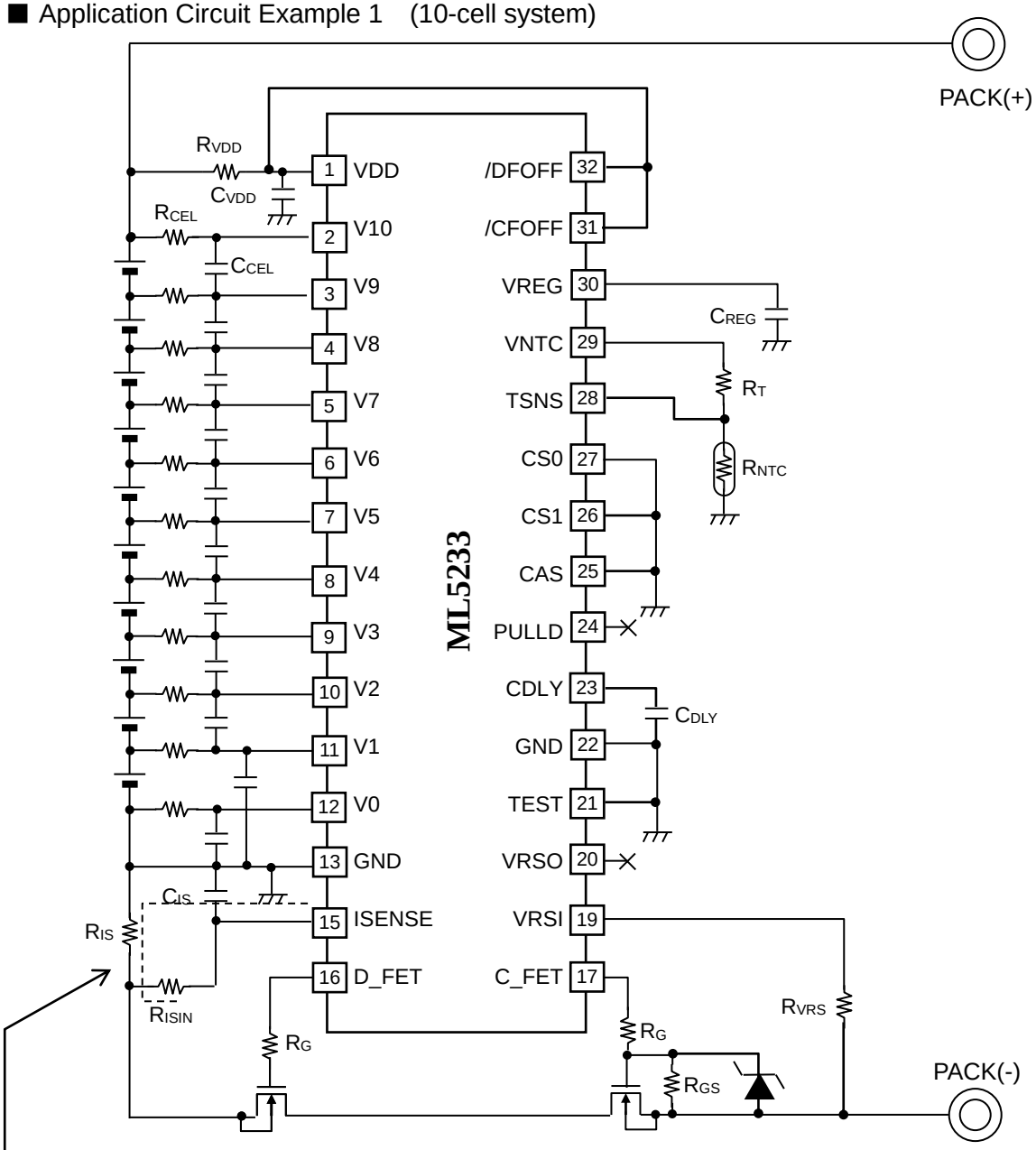
Detecting voltage	Threshold range	Threshold step
Overvoltage detection threshold	3.65 V to 4.35 V	25 mV
Overvoltage release threshold	3.5 V to 4.25 V	25 mV
Undervoltage detection threshold	1.6 V to 3 V	100 mV
Undervoltage release threshold	2.3 V to 4.3 V	100 mV
Discharge overcurrent detection threshold	50 mV to 200 mV	10 mV
Charge overcurrent detection threshold	-60 mV to -20 mV	10 mV
Short circuit detection threshold	100 mV to 500 mV	10 mV
High temperature detection threshold	0.6 V to 1.2 V	10 mV
High temperature release threshold	0.7 V to 1.3 V	10 mV

- Redefinition of Detection Delay Time

The detection delay times can be redefined as shown in the following table.

Detection delay time	Settable time					Unit
Overvoltage detection delay time	1	2	3	4	5	sec
Undervoltage detection delay time	1	2	3	4	5	sec
Discharge overcurrent detection delay time	25	50	100	200	400	ms
Charge overcurrent detection delay time	25	50	100	200	400	ms

■ Application Circuit Example 1 (10-cell system)



The wire length indicated by a dotted line should be minimized, because the voltage drop due to wire resistance may affect the current detection accuracy.

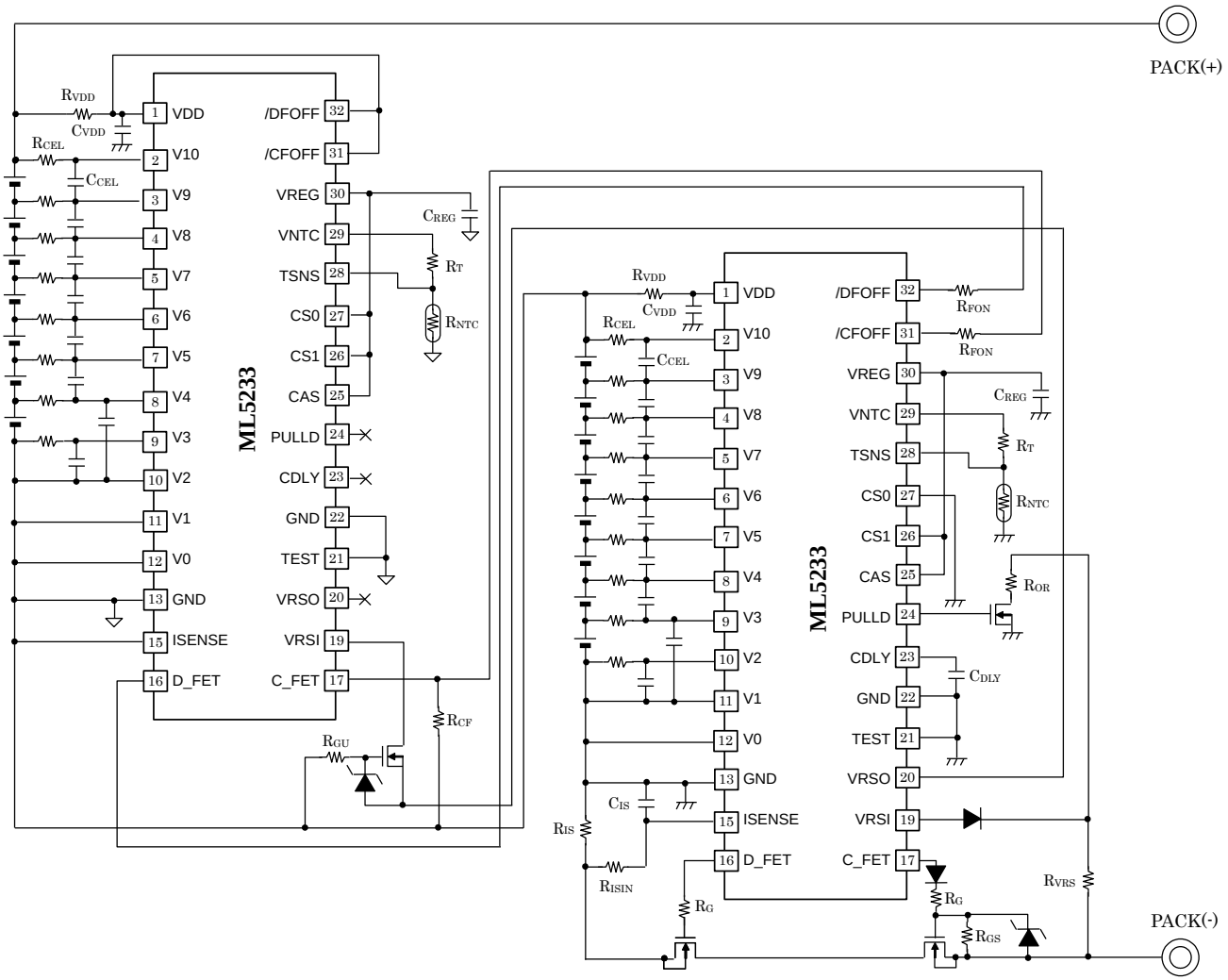
■ Recommended Values for External Components

Component	Recommended value
R_{VDD}	510 Ω
C_{VDD}	10 µF or more
R_{CEL}	1 kΩ to 10 kΩ
C_{CEL}	0.1 µF or more
C_{REG}	1µF
C_{IS}	10 nF
C_{DLY}	1 nF to 10 nF

Component	Recommended value
R_{GS}	1 MΩ
R_G	10 kΩ to 47 kΩ
R_{VRS}	1 kΩ
R_{IS}	1 mΩ to 5 mΩ
R_{ISIN}	1 kΩ
R_T	4.7 kΩ
R_{NTC}	10 kΩ, B3435

(Note) This circuit example and the recommended values of external components are not always warranted. Evaluation on customer's application is required and select circuit and parts depend on customer's application.

■ Application Circuit Example 2 (15-cell system, 8 cells and 7 cells)



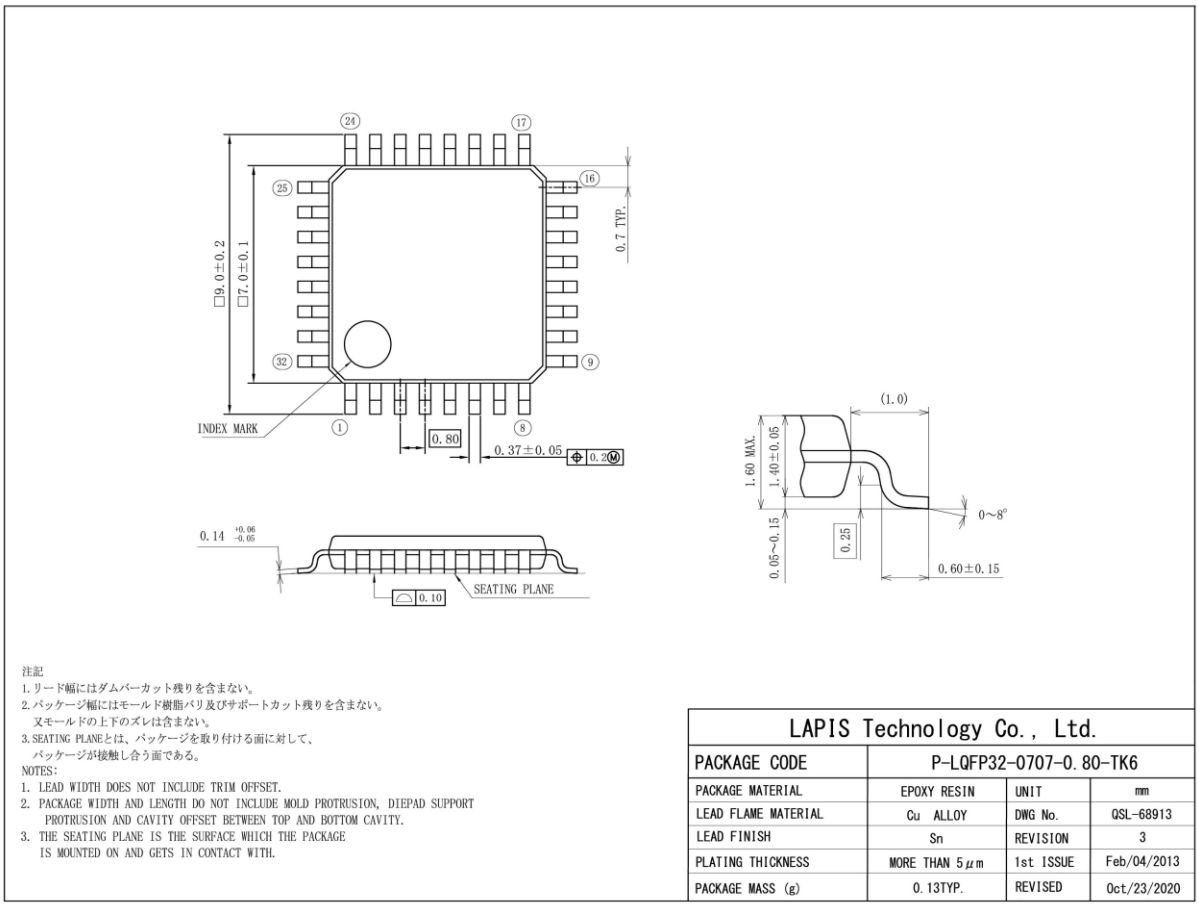
■ Recommended Values for External Components

Component	Recommended value
R_{VDD}	510 Ω
C_{VDD}	10 µF or more
R_{CEL}	1 kΩ to 10 kΩ
C_{CEL}	0.1 µF or more
C_{REG}	1 µF
C_{IS}	10 nF
C_{DLY}	1 nF to 10 nF
R_{GS}	1 MΩ

Component	Recommended value
R_G	10 kΩ to 47 kΩ
R_{VRS}	1 kΩ
R_{IS}	1 mΩ to 5 mΩ
R_{ISIN}	1 kΩ
R_T	4.7 kΩ
R_{NTC}	10 kΩ, B3435
R_{GU} ,R_{FON}	5.1 MΩ
R_{OR}	1 MΩ
R_{CF}	1.2 MΩ

(Note) This circuit example and the recommended values of external components are not always warranted. Evaluation on customer's application is required and select circuit and parts depend on customer's application.

■ Package Dimensions



注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
　又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
　パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-LQFP32-0707-0.80-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68913
LEAD FINISH	Sn	REVISION	3
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Feb/04/2013
PACKAGE MASS (g)	0.13TYP.	REVISED	Oct/23/2020

Caution regarding surface mount type packages

Surface mount type packages are susceptible to heat applied in solder reflow and moisture absorbed during storage. Please contact your local ROHM sales representative for recommended mounting conditions (reflow sequence, temperature and cycles) and storage environment.

■ Revision History

Document No.	Issue date	Page		Revision description
		Before revision	After revision	
FEDL5233-01	14 Sep, 2015	-	-	Initial release, based on FJDL5233-01.
FEDL5333-02	25 Dec, 2015	28	28	Cascade connection, pin name is corrected.
FEDL5333-03	25 Mar, 2016	6	6	High temperature charge inhibition detection threshold (Ta=25℃) is 0.97(min)->0.99(min)
		17	17	High Temperature Detection and Recovery, note2 is added.
		30,31	30,31	Application Circuit examples; capacitor connection of lowest cell is modified. Note is added
		31	31	Application Circuit example 2; the value of R_{GU} is modified.
FEDL5333-04	1 Dec, 2020	-	-	Changed Company name
		34	34	Changed “Notes”
FEDL5333-05	Jan. 9, 2024	1	1	Add Application Part number, Delete notes
		34	34	Add Notes

Notes

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