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ROHM Co., Ltd.
April 1, 2024

RB-S22Q573MB30

User's Manual

Issue Date: October 14, 2021

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1. Overview

This instruction manual is for the RB-S22Q573MB30 which is the reference board for ML22Q573/ML2257X/ML22Q563/ML2256X/ML22Q553 (hereinafter referred to as "Speech Synthesis LSIs").

This board can be combined with Sound Device Control Board 3 (hereinafter referred to as "SDCB3") to do the following:

- Voice playback by ML22Q573/ML2257X/ML22Q563/ML2256X/ML22Q553.
- Writing sound code data into ML22Q573/ML22Q563/ML22Q553.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22Q573MB30.

- Turn off the power when attaching the RB-S22Q573MB30 to the SDCB3.
- Turn off the power when loading Speech Synthesis LSIs into the RB-S22Q573MB30. Pin 1 is the position of the board silk ▲ at the bottom left with respect to the socket opening. The Figure 1 shows the setting directions of Speech Synthesis LSIs.
- Use the RB-S22Q573MB30 with a power supply voltage of 5.0V.
- Connect JACK1 jack and JACK2 jack to the mono speaker.
- RB-S22Q573MB30 is a device used only by experts in R&D facilities for research and development purposes. RB-S22Q573MB30 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Technology does not provide any RB-S22Q573MB30 support. Replace only in case of initial failure.

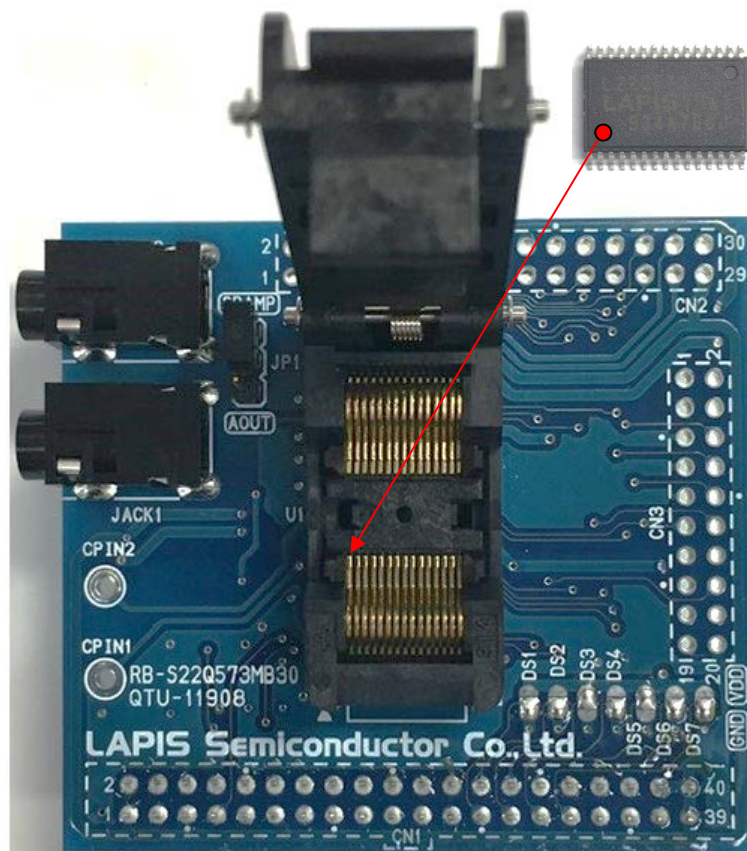


Figure 1 Outline Diagram

3. Specification

3.1. JP1 jumper pin

JP1 jumper pin is jumper pin that switch the connection of SPP pin of Speech Synthesis LSIs.

OUT	Contents
AOUT	SPP pin is connected to JACK1 jack.
SPAMP	SPP pin is connected to JACK2 jack.

3.2. JACK1 jack

JACK1 jack is a jack where the signal from SPP pins of Speech Synthesis LSIs is output via the speaker amplifier.
Set the JP1 jumper pin to AOUT when using JACK1 jack.
Connect a monaural speaker.

3.3. JACK2 jack

JACK2 jack is a jack where the signal from SPP,SPM pins of Speech Synthesis LSIs is output.
Set the JP1 jumper pin to SPAMP when using JACK2 jack.
Connect a monaural speaker.

3.4. CPIN1, CPIN2 through hall

CPIN1, CPIN2 through hole is used to input signals from an external source to the AIN pin of Speech Synthesis LSIs.
Input the speaker amplifier input signal to CPIN1, CPIN2 through hole.

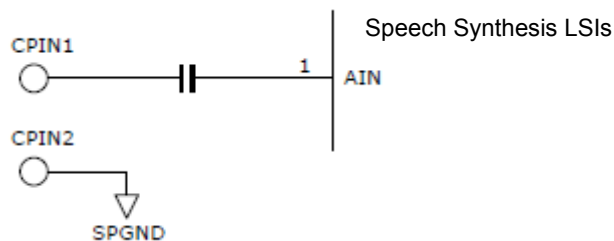


Figure 2 CPIN1, CPIN2 through hall

3.5. CN1 connector

CN1 connector is used to connect to SDCB3.

3.6. CN2 connector

CN2 connector is used to connect to the pins of Speech Synthesis LSIs.

CN2 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit
1	1	AIN	O	I
2	2	SG	O	O
3	3	VDDR	O	O
4	4,18	DVDD *	O	I
5	5,15	DGND	O	I
6	6	VDDL	O	O
7	7	DIPH	O	I
8	8	STATUS	O	O
9	9	ERR	O	O
10	10	CSB	O	I
11	11	SCK	O	I
12	12	SI	O	I
13	13	SO	O	O
14	14	CBUSYB	O	O
15	5,15	DGND	O	I
16	16	XTB	O	O
17	17	XT	O	O
18	4,18	DVDD *	O	I
19	-	-	-	-
20	20	RESETB	O	I
21	21	TESTI0 (MODE)	O	I
22	22	TESTI1 (nTRST)	O	I
23	23	TESTI2 (TMS)	O	I
24	24	TESTI3 (TDI)	O	I
25	25	TESTI4 (TCK)	O	I
26	26	TESTO (TDO)	O	O
27	27	SPM	O	O
28	28	SPP	O	O
29	29	SPGND	O	I
30	30	SPVDD *	O	I

*1 Do not supply DVDD,SPVDD from CN2 when connecting SDCB3.

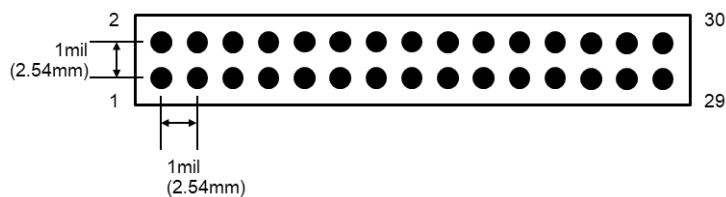


Figure 3 CN2 connectors hole pattern

3.7. CN3 connector

CN3 connector is used to connect to the serial audio interface pin of Speech Synthesis LSIs.

CN3 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit
1	-	-	-	-
2	4,18	DVDD	O	I
3	-	-	-	-
4	4,18	DVDD	O	I
5	5,15	DGND	O	I
6	25	TESTI4 (TCK)	O	I
7	5,15	DGND	O	I
8	24	TESTI3 (TDI)	O	I
9	5,15	DGND	O	I
10	26	TESTO (TDO)	O	O
11	23	TESTI2 (TMS)	O	I
12	22	TESTI1 (nTRST)	O	I
13	-	-	-	-
14	-	-	-	-
15	-	-	-	-
16	21	TESTI0 (MODE)	O	I
17	-	-	-	-
18	-	-	-	-
19	-	-	-	-
20	5,15	DGND	O	I

*1 Do not supply DVDD from CN3 when connecting SDCB3.

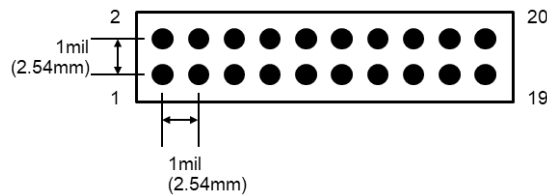


Figure 4 CN3 connectors hole pattern

4. Appendix

4.1. PCB layout

Figure 5 shows the RB-S22Q573MB30 PCB layout.

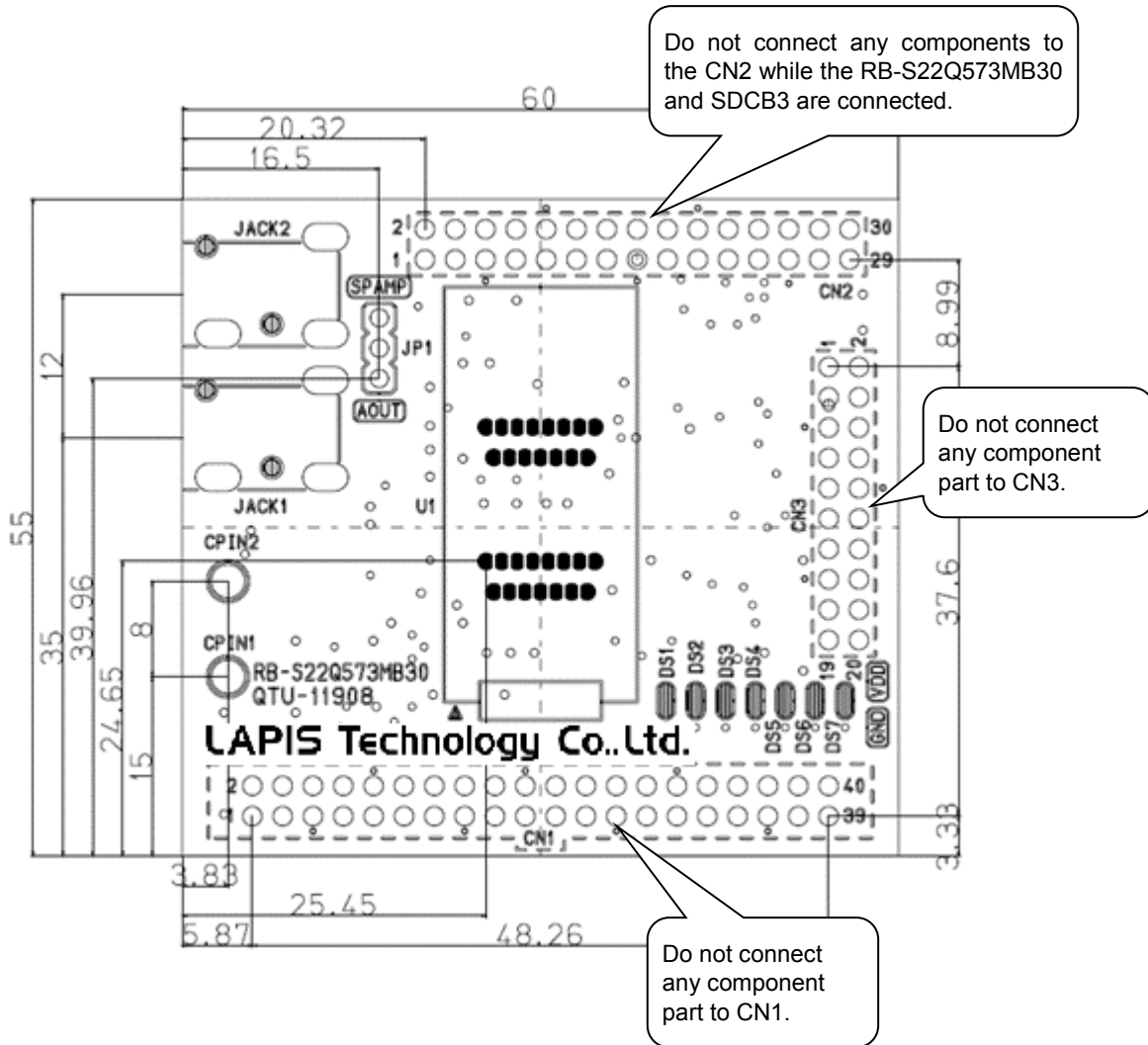
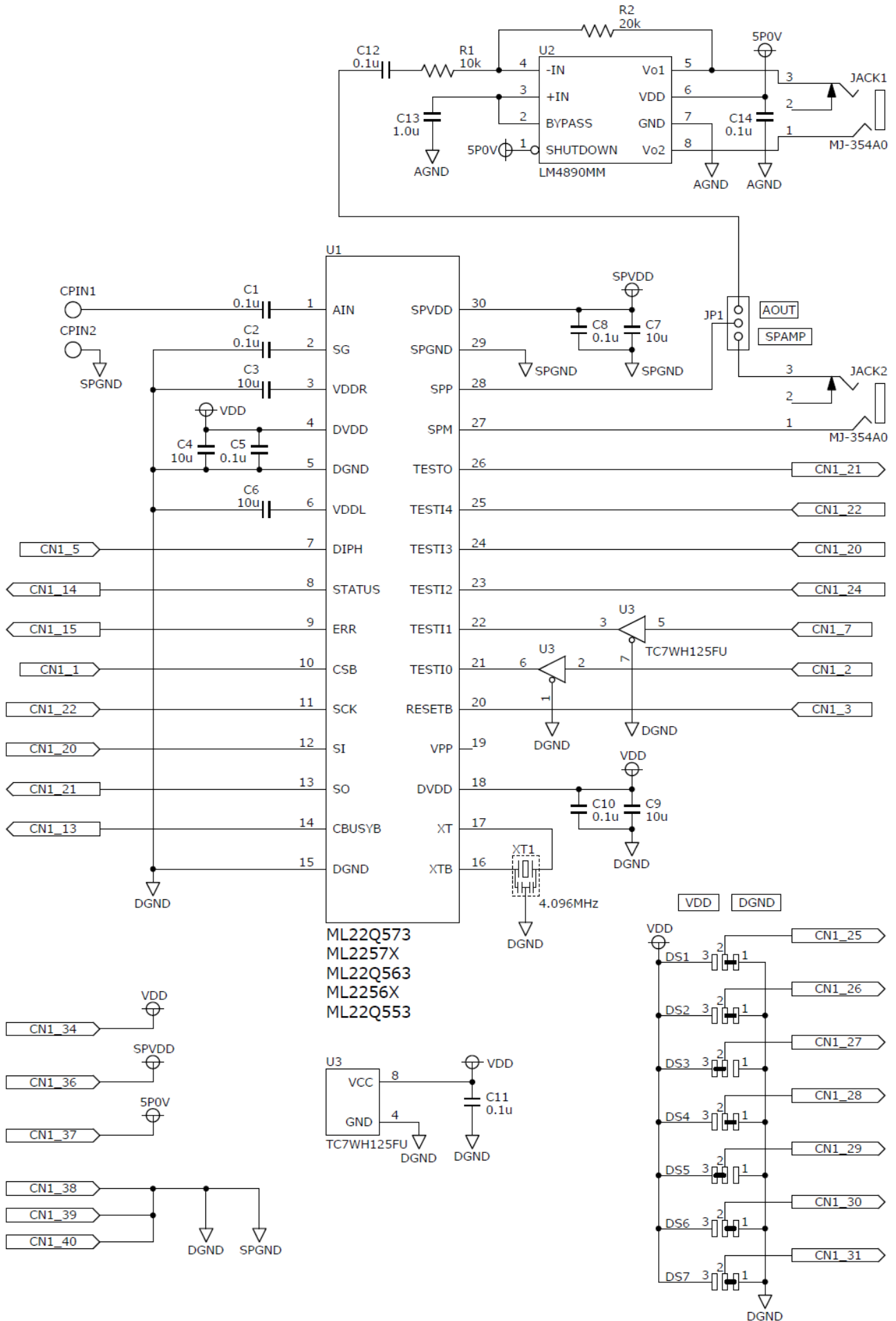


Figure 5 PCB layout

4.2. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11908	RB-S22Q573MB30	PCB	1	LAPIS Technology Co., Ltd.
2	CGA3E2X7R1E104K080AA	C1, C2, C5, C8, C10, C11, C12, C14	Ceramic Capacitor 0.1 μ F/25V X7R	8	TDK Corporation
3	CGA3E1X7R1C105K080AC	C13	Ceramic Capacitor 1.0 μ F/16V X7R	1	TDK Corporation
4	EMK212ABJ106KD-T	C3, C4, C6, C7, C9	Ceramic Capacitor 10 μ F/16V X5R	5	TAIYO YUDEN CO., LTD.
5	HIF3FB-40DA-2.54DSA(71)	CN1	HIF3FB-40DA-2.54DSA(71)	1	Hirose Electric Co., Ltd.
6	-	DS1, DS2, DS3, DS4, DS5, DS6, DS7	Select pad	7	-
7	MJ-354A0	JACK1, JACK2	2-Conductor Miniature Jack	2	MARUSHIN ELECTRIC MFG. CO., LTD.
8	A2-3PA-2.54DSA	JP1	3pin Pin Header	1	Hirose Electric Co., Ltd.
9	MCR03EZPJ103	R1	Resistor 10k Ω \pm 5%	1	Rohm Co., Ltd.
10	MCR03EZPJ203	R2	Resistor 20k Ω \pm 5%	1	Rohm Co., Ltd.
11	IC51-0302-914	U1	SSOP30 Socket	1	YAMAICHI ELECTRONICS Co., Ltd.
12	LM4890MM/NOPB	U2	Audio Power Amplifier	1	Texas Instruments Incorporated
13	TC7WH125FU	U3	Bus Buffer with 3-State Output	1	Toshiba Corporation
14	CSTCR4M09G55B-R0	XT1	Ceramic Resonators 4.096MHz 39pF	1	Murata Manufacturing Co., Ltd.
15	HIF3GA-2.54SP	-	Short Pin	1	Hirose Electric Co., Ltd.
16	-	CN2	Unmounted	1	-
17	-	CN3	Unmounted	1	-
18	-	CPIN1, CPIN2	Unmounted	2	-



5. Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22Q573RB-01	March 19, 2020	-	-	First edition.
FEBL22Q573RB-02	July 30 2021	Notes	Notes	Change the description. Company name change.
		1	1	2. Operational notes Added to connect a monaural speaker to the JACK1 jack and JACK2 jack.
		-	2	3.1. JP1 jumper pin Changed chapter name.
		-	2	3.2. JACK1 jack Changed chapter number. Added SDCB Controller settings when using JACK1 jack. Added to connect a monaural speaker to the JACK1 jack.
		-	2	3.3. JACK2 jack Changed chapter number. Added SDCB Controller settings when using SP jack. Added to connect a monaural speaker to the JACK2 jack.
		-	2	3.5. CPIN1, CPIN2 through hall Changed chapter number. Changed chapter name. Added connection diagram.
		-	3	3.5. CN1 connector Changed chapter number.
		-	3	3.6. CN2 connector Changed chapter number. Added input/output directions when SDCB3 is connected and single unit is used.
		-	4	3.7. CN3 connector Changed chapter number. Added input/output directions when SDCB3 is connected and single unit is used.
		-	4	3.10. Ceramic resonator Deleted chapter.
-	5	4. Appendix Added chapter.		
-	5	4.1. PCB layout Changed chapter number. Changed Figure 5.		
-	6	4.2. BOM list, Schematic Changed chapter number. Company name change.		
-	7	4.2. BOM list, Schematic Changed chapter number. Company name change.		

FEBL22Q573RB-03	October 14 2021	7	7	4.2. BOM list, Schematic Fixed an error in the connection destination of 24pin of U1. Fixed an error in the connection destination of 25pin of U1. Fixed an error in the connection destination of 26pin of U1.
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