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ROHM Co., Ltd.
April 1, 2024

ROHM GROUP
LAPIS TECHNOLOGY

FEBL22Q53xRB-04

RB-S22Q53xTB48
User's Manual

Issue Date: February 5, 2021

ROHM SEMICONDUCTOR

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Table of Contents

1. Overview

This instruction manual is for the RB-S22Q53xTB48 which is the reference board for ML22Q532/ML22Q533/ML22Q535 (hereinafter referred to as "Speech Synthesis LSIs").

This board can be combined with Sound Device Control Board 3 (hereinafter referred to as "SDCB3") to do the following:

- Voice playback by ML22Q532/ML22Q533/ML22Q535.
- Writing sound code data into ML22Q532/ML22Q533/ML22Q535.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22Q53xTB48.

- Turn off the power when attaching the RB-S22Q53xTB48 to the SDCB3.
- Turn off the power when loading Speech Synthesis LSIs into the RB-S22Q53xTB48. Pin 1 is the position of the board silk ▲ at the bottom left with respect to the socket opening. The Figure 1 shows the setting directions of Speech Synthesis LSIs.
- The ML22Q532/ML22Q533/ML22Q535 supply voltages are 2.7 to 3.6V / 3.3 to 5.5V. Use the RB-S22Q53xTB48 with a power supply voltage of 3.0V.
- Connect LOUT jack and SP jack to the mono speaker.
- This board cannot use the playback sound error detection function targeting FB1,FB2 pin inputs of Speech Synthesis LSIs. (Refer to 3.9. Connection of FB1,FB2 pin)

- RB-S22Q53xTB48 is a device used only by experts in R&D facilities for research and development purposes. RB-S22Q53xTB48 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Technology does not provide any RB-S22Q53xTB48 support. Replace only in case of initial failure.

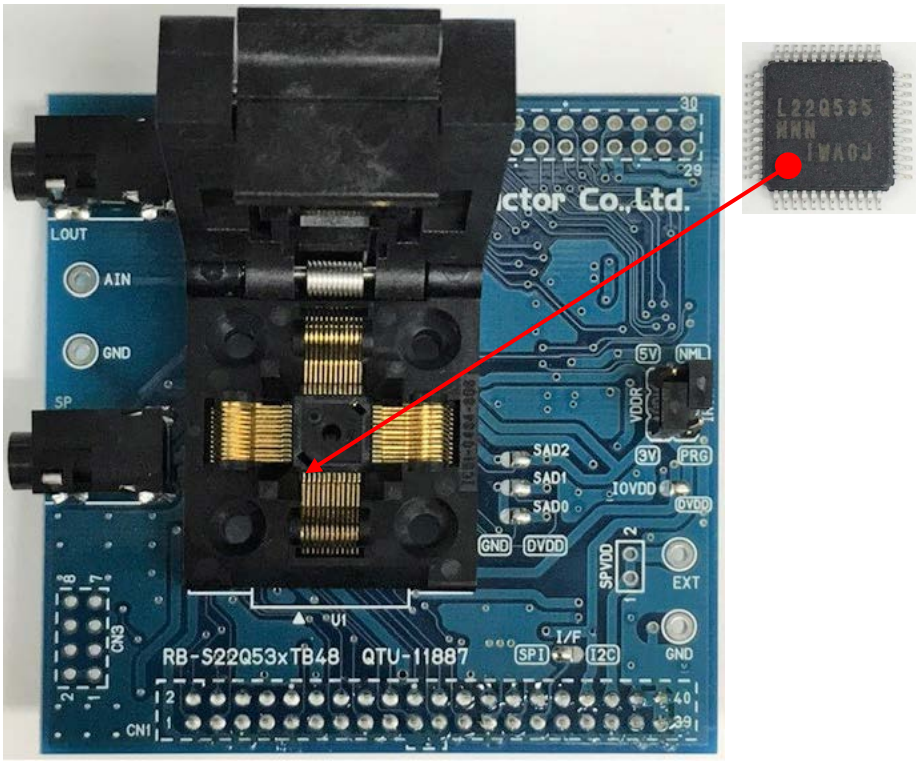


Figure 1 Outline Diagram

3. Specification

3.1. VDDR jumper pin

VDDR jumper pin is jumper pin that switch the connection of VDDR pin of Speech Synthesis LSIs.

VDDR	Contents
3V	VDDR pin is connected to DVDD.
5V	VDDR pin is open.

Set to 3V when connecting to a SDCB3 for use.

3.2. IRON jumper pin

IRON jumper pin is jumper pin that switch the connection of IRON pin of Speech Synthesis LSIs.

IRON	Contents
NML	IRON pin is connected to CN1,CN2.
PRG	IRON pin is connected to IOVDD.

Set to NML when connecting to SDCB3 for use. IRON pin is controlled from SDCB3.
When this board is used by itself, setting PRG enables the flash memory interface of Speech Synthesis LSIs.

3.3. LOUT jack

LOUT jack is a jack where the signal from LOUT pins of Speech Synthesis LSIs is output via the speaker amplifier.
Set Mode of Play setting of SDCB Controller to Line AMP(LOUT). (Refer to Speech LSI Utility User's Manual.)
Connect a monaural speaker.

3.4. SP jack

SP jack is a jack where the signal from SPP,SPM pins of Speech Synthesis LSIs is output.
Set Mode of Play setting of SDCB Controller to Speaker AMP. (Refer to Speech LSI Utility User's Manual.)
Connect a monaural speaker.

3.5. AIN through hall

AIN through hole is used to input signals from an external source to the AIN pin of Speech Synthesis LSIs.
Input the speaker amplifier input signal to AIN through hole.

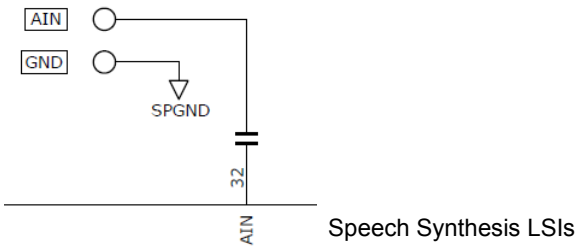


Figure 2 AIN through hall

3.6. SPVDD jumper terminal, EXT through hall

SPVDD jumper terminal is used to switch the destination of SPVDD pins of Speech Synthesis LSIs.
When supplying from SDCB3, connect 1-2pin of SPVDD jumper terminal.
To supply from an external source, cut the pattern between 1 and 2 pins of SPVDD jumper terminal and input SPVDD from the EXT throughhole.

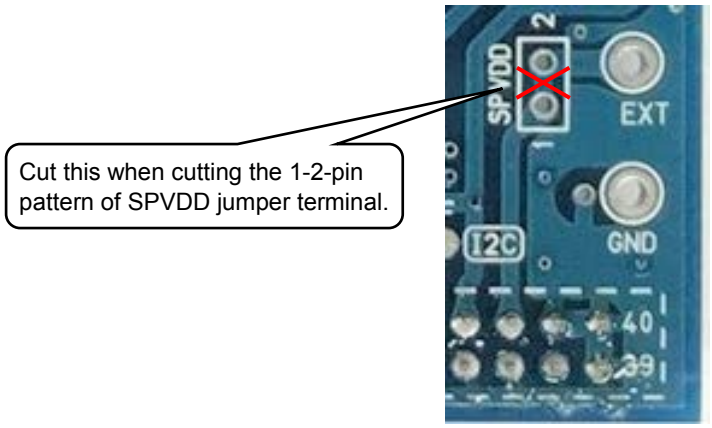


Figure 3 SPVDD jumper terminal

3.7. SAD2-0 lands

SAD2-0 lands are used to change SAD2-0 setting of Speech Synthesis LSIs.
This board is shipped to DVDD (I2C slave address is 111_101).
When connecting this board to SDCB3 and using it, set DVDD to the factory default settings.
To set any I2C slave address, change the connection of SAD2-0 lands.

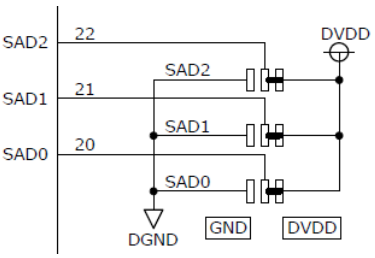


Figure 4 SAD2-0 lands

3.8. XT1 land, J1 land

XT1 land is used to mount the Ceramic resonator.
When using a ceramic resonator for the clock of Speech Synthesis LSIs, mount the components.
When no component is mounted, Speech Synthesis LSIs operates with built-in RC oscillation.

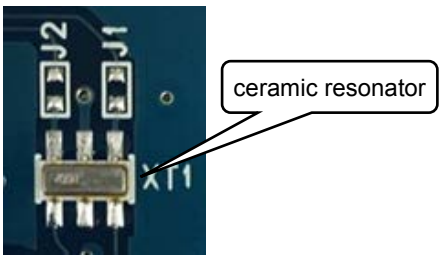


Figure 5 Ceramic resonator

A typical example of a ceramic resonator that matches XT1 land foot pattern is shown below.

Vendor	Frequency[Hz]	Parts Number
Murata Manufacturing Co., Ltd.	4M	CSTCR4M00G55B-R0
Murata Manufacturing Co., Ltd.	4.096M	CSTCR4M09G55B-R0

J1 land is land connecting the XT pin of speech synthesis LSIs to the 28pin (XT) of CN2.
To use an external clock for Speech Synthesis LSIs clock, connect the pins of the J1 land and input them from the 28pin (XT) of CN2.

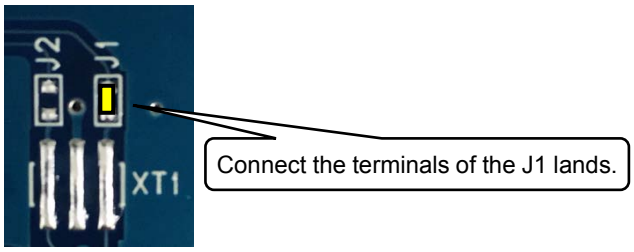


Figure 6 J1 land

3.9. Connection of FB1,FB2 pin

This board cannot use the playback sound error detection function targeting FB1,FB2 pin inputs of Speech Synthesis LSIs. However, LSI internal playback sound error detection function can be used.

CAUTION: This board is incorrect.
When using the playback sound error detection function targeting FB1,FB2 pin, connect the signal output from the SPP pin to FB1 pin and the signal output from the SPM pin to FB2 pin on the customer's board.

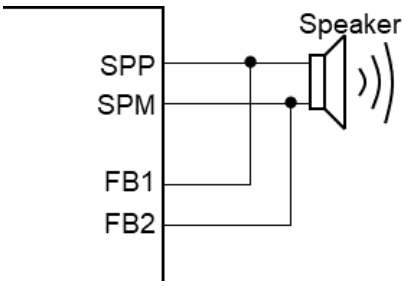


Figure 7 Connection example of FB1, FB2 pins and the SPP, SPM pins

3.10. CN1 connector

CN1 connector is used to connect to SDCB3.

3.11. CN2 connector

CN2 connector is used to connect to the pins of Speech Synthesis LSIs.

CN2 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit
1	26	DVDD *1	O	I
2	26	DVDD *1	O	I
3	43	RESETB	O	I
4	44	TEST0	O	I
5	45	STATUS1	O	O
6	46	STATUS2	O	O
7	47	CBUSYB	O	O
8	-	-	-	-
9	2	SCL	O	I
10	3	SDA	O	I/O
11	8	CSB	O	I
12	9	SCK	O	I
13	10	SI	O	I
14	11	SO	O	O
15	1, 25	DGND	-	-
16	1, 25	DGND	-	-
17	13	IRCSB	O	I
18	14	IRSCK	O	I
19	15	IRSO	O	O
20	16	IRSI	O	I
21	17	IRON	O	I
22	-	-	-	-
23	18	IOVDD *1	O	O
24	19	VDDR	O	O
25	1, 25	DGND	-	-
26	1, 25	DGND	-	-
27	23	XTB *2	O	O
28	24	XT *2	O	I
29	1, 25	DGND	-	-
30	1, 25	DGND	-	-

*1 Do not supply DVDD,IOVDD from CN2 when connecting SDCB3.
*2 When the J1 and J2 lands are connected, the XT and XTB pins of Speech Synthesis LSIs are input and output.

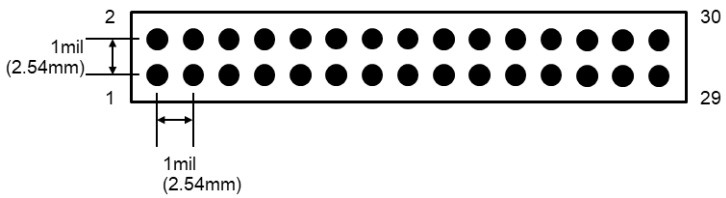


Figure 8 CN2 connectors hole pattern

3.12. CN3 connector

CN3 connector is used to connect to the serial audio interface pin of Speech Synthesis LSIs.

CN3 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit
1	26	DVDD *	O	I
2	26	DVDD *	O	I
3	4	LRCLK	I	I
4	5	BCLK	I	I
5	6	SAI_IN	I	I
6	7	SAI_OUT	O	O
7	1, 25	DGND	-	-
8	1, 25	DGND	-	-

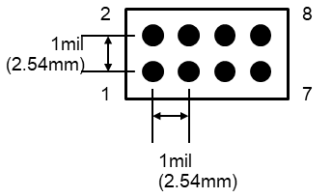


Figure 9 CN3 connectors hole pattern

4. Appendix

4.1. PCB layout

Figure 10 shows the RB-S22Q53xTB48 PCB layout.

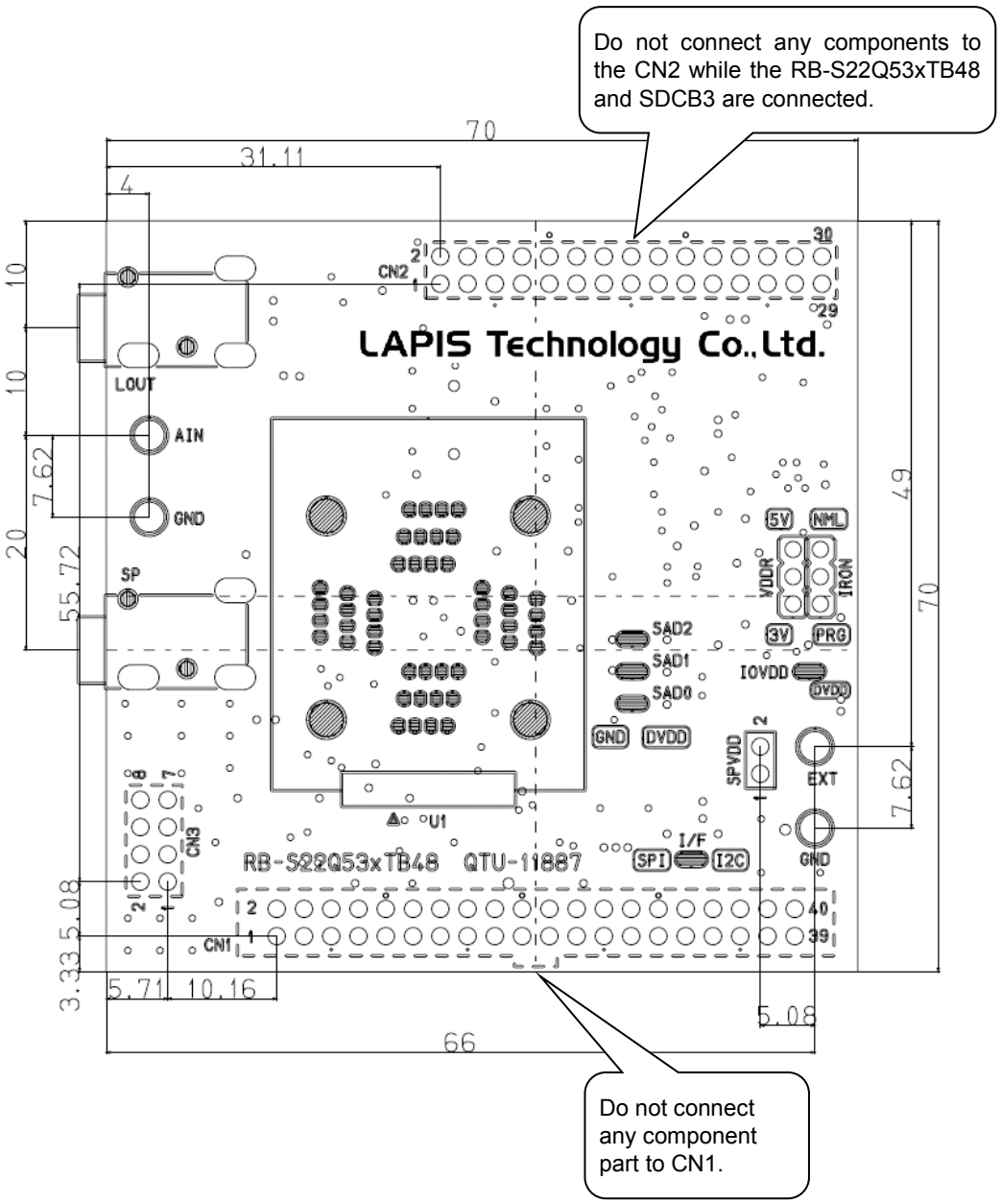
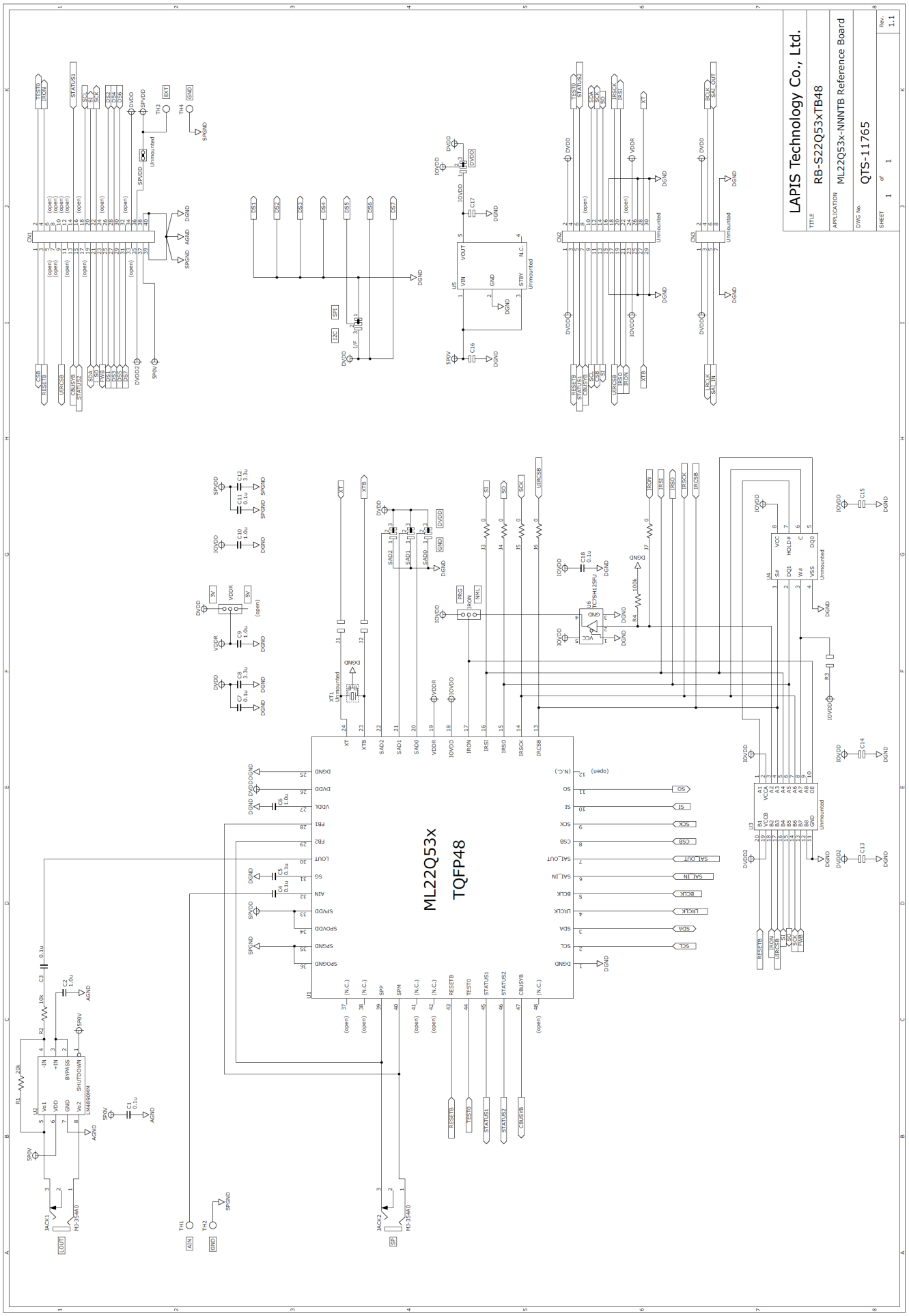


Figure 10 PCB layout

4.2. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11887	RB-S22Q53xTB48	PCB	1	LAPIS Technology Co., Ltd.
2	CGA3E2X7R1E104K080AA	C1,C3,C4,C5, C7,C11	Ceramic Capacitor 0.1μF/25V X7R	6	TDK Corporation
3	CGA3E1X7R1C105K080AC	C2,C6,C9,C10, C18	Ceramic Capacitor 1.0μF/16V X7R	5	TDK Corporation
4	C1608X5R1C335K080AC	C8,C12	Ceramic Capacitor 3.3μF/16V X5R	2	TDK Corporation
5	HIF3FB-40DA-2.54DSA(71)	CN1	40pin Receptacle	1	Hirose Electric Co., Ltd.
6	A2-3PA-2.54DSA	IRON,VDDR	3pin Pin Header	2	Hirose Electric Co., Ltd.
7	-	I/F,IOVDD	Select pad	2	-
8	MCR03EZPJ000	J3,J4,J5,J6,J7	Resistor 0Ω	5	Rohm Co., Ltd.
9	MJ-354A0	JACK1,JACK2	2-Conductor Miniature Jack	2	MARUSHIN ELECTRIC MFG. CO., LTD.
10	MCR03EZPJ203	R1	Resistor 20kΩ ±5%	1	Rohm Co., Ltd.
11	MCR03EZPJ103	R2	Resistor 10kΩ ±5%	1	Rohm Co., Ltd.
12	MCR03EZPJ104	R4	Resistor 100kΩ ±5%	1	Rohm Co., Ltd.
13	-	SAD0,SAD1,SAD2	Select pad	3	-
14	IC51-806.A106725-001	U1	TQFP P0.50 48P Socket	1	YAMAICHI ELECTRONICS Co., Ltd.
15	LM4890MM/NOPB	U2	Audio Power Amplifier	1	Texas Instruments Incorporated
16	TC7SH125FU	U6	Bus Buffer with 3-State Output	1	Toshiba Corporation
17	HIF3GA-2.54SP	-	Short Pin	2	Hirose Electric Co., Ltd.
18	-	C13,C14,C15,C16, C17	Unmounted	5	-
19	-	CN2	Unmounted	1	-
20	-	CN3	Unmounted	1	-
21	-	J1,J2	Unmounted	2	-
22	-	SPVDD	Unmounted	1	-
23	-	R3	Unmounted	1	-
24	-	TH1,TH2,TH3,TH4	Unmounted	4	-
25	-	U3	Unmounted	1	-
26	-	U4	Unmounted	1	-
27	-	U5	Unmounted	1	-
28	-	XT1	Unmounted	1	-


LAPIS Technology Co., Ltd.
TITLE RB-S22Q53xTB48
APPLICATION ML22Q53x-NNNTB Reference Board
DWG No. QTS-11765
SHEET 1 of 1
Rev. 1.1
ML22Q53x
TQFP48

5. Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22Q53xRB-01	October 31, 2019	–	–	First edition.
FEBL22Q53xRB-03	March 26, 2020	3	3	3.3. BOM list, Schematic
FEBL22Q53xRB-04	February 5 2021	Notes	Notes	Change the description.
				Company name change.
		1	1	2. Operational notes Added to connect a monaural speaker to the LOUT jack and SP jack.
				2. Operational notes Added that playback sound error detection function for FB1,FB2 pins cannot be used.
		-	2	3.1. VDDR jumper pin Added chapter.
				3.2. IRON jumper pin Added chapter.
				3.3. LOUT jack Changed chapter number. Added SDCB Controller settings when using LOUT jack. Added to connect a monaural speaker to the LOUT jack.
				3.4. SP jack Changed chapter number. Added SDCB Controller settings when using SP jack. Added to connect a monaural speaker to the LOUT jack.
				3.5. AIN through hall Changed chapter number. Changed chapter name. Added connection diagram.
		-	3	3.6, SPVDD jumper terminal, EXT through hall Added chapter.
				3.7, SAD2-0 lands Added chapter.
				3.8. XT1 land, J1 land Changed chapter number. Changed chapter name. Added operation in RC oscillation.
		-	4	3.9. Connection of FB1,FB2 pin Added chapter.
				3.10. CN1 connector Changed chapter number.
		-	5	3.11. CN2 connector Changed chapter number. Added input/output directions when SDCB3 is connected and single unit is used.

		-	6	3.12. CN3 connector Changed chapter number. Added input/output directions when SDCB3 is connected and single unit is used.
		-	7	4. Appendix Added chapter.
				4.1. PCB layout Changed chapter number. Changed Figure 10.
		-	8	4.2. BOM list, Schematic Changed chapter number. Company name change.
		-	9	4.2. BOM list, Schematic Changed chapter number. Company name change.