



Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

RB-S22Q374TD20 V2

User's Manual

Issue Date: February 24, 2021

Notes

- 1) The information contained herein is subject to change without notice.
- 2) When using LAPIS Technology Products, refer to the latest product information (data sheets, user's manuals, application notes, etc.), and ensure that usage conditions (absolute maximum ratings, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. You are responsible for evaluating the safety of the final products or systems manufactured by you.
- 3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.
- 4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples, etc.). Therefore LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.
- 5) The Products are intended for use in general electronic equipment (AV/OA devices, communication, consumer systems, gaming/entertainment sets, etc.) as well as the applications indicated in this document. For use of our Products in applications requiring a high degree of reliability (as exemplified below), please be sure to contact a LAPIS Technology representative and must obtain written agreement: transportation equipment (cars, ships, trains, etc.), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us. Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc.
- 6) The Products specified in this document are not designed to be radiation tolerant.
- 7) LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Technology does not warrant that such information is error-free and LAPIS Technology shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.
- 8) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.
- 9) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act..
- 10) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.
- 11) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) "LAPIS Technology" as used in this document means LAPIS Technology Co., Ltd.

Copyright 2021 LAPIS Technology Co., Ltd.

LAPIS Technology Co., Ltd.

2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
<https://www.lapis-tech.com/en/>

Table of Contents

1. Overview.....	1
2. Operational notes.....	1
3. Specification	2
3.1. SPVDD jumper pin, EXT through hall	2
3.2. Jack	2
3.3. J1 jumper terminal	2
3.4. R6,R7 land	2
3.5. CN1 connector	3
3.6. CN2 connector	3
4. Appendix.....	4
4.1. PCB layout.....	4
4.2. BOM list, Schematic	5
5. Revision History.....	7

1. Overview

This instruction manual is for the RB-S22Q374TD20 V2 which is the reference board for ML22Q374 (hereinafter referred to as "Speech Synthesis LSIs").

This board can be combined with Sound Device Control Board 3 (hereinafter referred to as "SDCB3") to do the following:

- Voice playback by ML22Q374.
- Writing sound code data into ML22Q374.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22Q374TD20 V2.

- Turn off the power when attaching the RB-S22Q374TD20 V2 to the SDCB3.
- Turn off the power when loading Speech Synthesis LSIs into the RB-S22Q374TD20 V2. Pin 1 is the position of the board silk ▲ at the bottom left with respect to the socket opening. The Figure 1 shows the setting directions of Speech Synthesis LSIs.
- The ML22Q374 supply voltages 2.0 to 5.5V. Use the RB-S22Q374TD20 V2 with a power supply voltage of 3.0 to 5.5V. When connecting to SDCB3, the power supply voltage of RB-S22Q374TD20 V2 is 3.0V.
- Connect jack to the mono speaker.
- RB-S22Q374TD20 V2 is supported in Speech LSI Tools versions R3.6.0 and later.
- RB-S22Q374TD20 V2 is a device used only by experts in R&D facilities for research and development purposes. RB-S22Q374TD20 V2 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Technology does not provide any RB-S22Q374TD20 V2 support. Replace only in case of initial failure.

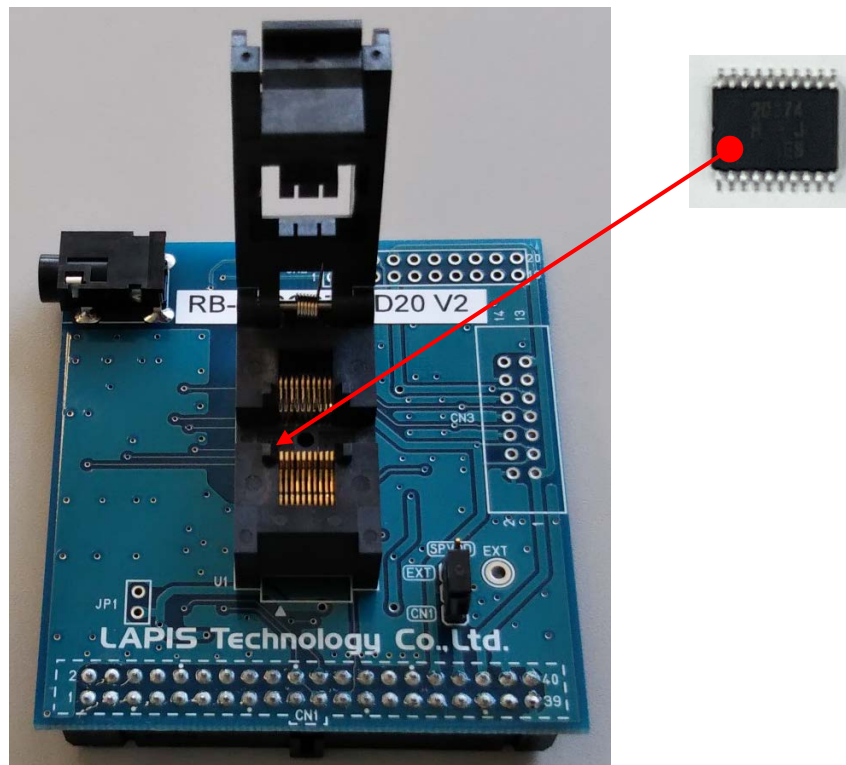


Figure 1 Outline Diagram

3. Specification

3.1. SPVDD jumper pin, EXT through hall

SPVDD jumper pin is jumper pin that switch the connection of SPVDD pin of Speech Synthesis LSIs.

SPVDD	Contents
CN1	SPVDD pin is connected to 34pin of CN1.
EXT	SPVDD pin is connected to the EXT through hall.

When supplying from SDCB3, set SPVDD jumper pin to CN1.

To supply from an external source, set SPVDD jumper pin to EXT and input SPVDD from the EXT through hole.

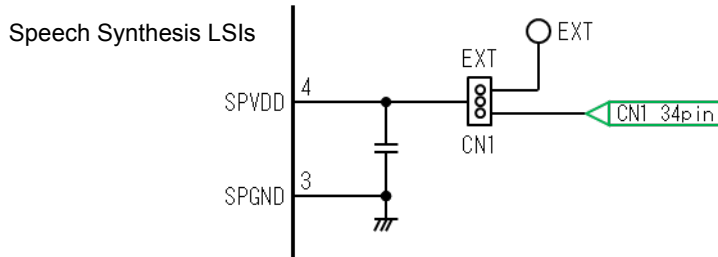


Figure 2 SPVDD jumper pin, EXT through hall

3.2. Jack

Jack is a jack where the signal from SPP,SPM pins of Speech Synthesis LSIs is output. Connect a monaural speaker.

3.3. JP1 jumper terminal

JP1 jumper terminal is a jumper terminal that enables or disables the signal input from CN1 (SDCB3) to the input pin (RESET_N, TEST) of Speech Synthesis LSIs.

JP1 jumper terminal	Contents
Through hall	
Not connect	Enables: Signals are input from CN1 to the input pins of Speech Synthesis LSIs.
Connect	Disables: No signals are input from CN1 to the input pins of Speech Synthesis LSIs.

When connecting to a SDCB3 for use, not connect the through holes of the JP1 jumper terminal.

When using this board alone, connect the through holes of the JP1 jumper terminal.

When this board is shipped, there is no connection between the through holes of the JP1 jumper terminal.

3.4. R6,R7 land

R6 is a pull up resistor mounting land for BUSYB pin of Speech synthesizer LSIs.

R7 is a pull down resistor mounting land for BUSYB pin of Speech synthesizer LSIs.

R6,R7 are not mounted at the time of shipment from this board.

BUSYB pin of Speech Synthesis LSIs select the pin status from COMS output, Nch open drain output, Pch open drain output, and Hi-Z output according to Code Option setting. (Refer to Speech LSI Utility User's Manual.)

When using BUSYB pin with Nch open drain output, mount resistor (10kΩ or less, size:1608) to R6 on the back of the board.

When using BUSYB pin with Pch open drain output, mount resistor (1kΩ or less, size:1608) to R7 on the back of the board.

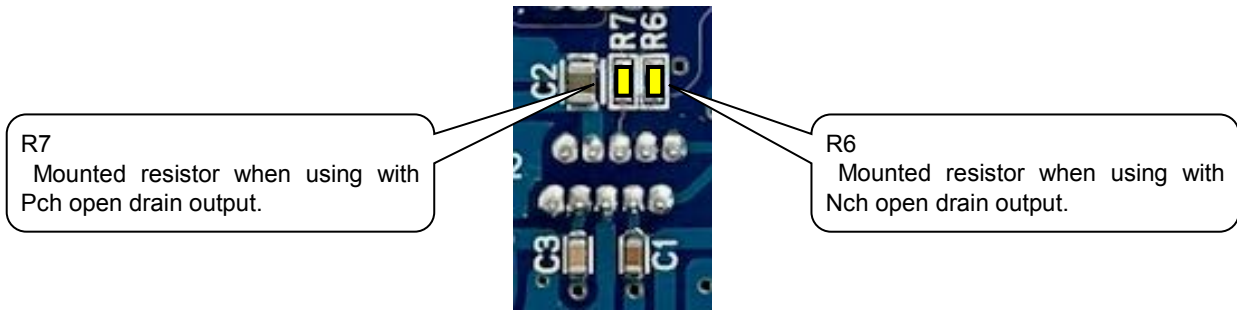


Figure 3 R6,R7 land

3.5. CN1 connector

CN1 connector is used to connect to SDCB3.

3.6. CN2 connector

CN2 connector is used to connect to the pins of Speech Synthesis LSIs.

CN2 Pin No	LSI		I/O	
	Pin No	Pin Name	SDCB3 connection	Single unit ^{*2}
1	1	SPP	O	O
2	2	SPM	O	O
3	3	SPGND	-	-
4	4	SPVDD *1	O	I
5	5	BUSYB	O	O
6	6	DGND	-	-
7	7	VDDL	O	O
8	8	DVDD *1	O	I
9	9	-	-	-
10	10	-	-	-
11	11	-	-	-
12	12	-	-	-
13	13	CSB	O	I
14	14	SI	O	I
15	15	SCK	O	I
16	16	-	-	-
17	17	-	-	-
18	18	VPP	O	I
19	19	TEST	O	I
20	20	RESET_N	O	I

*1 Do not supply DVDD,SPVDD from CN2 when connecting SDCB3.

*2 When using a single unit, connect the terminals of JP1 jumper terminal. (Refer to 3.3 JP1 jumper terminal.)

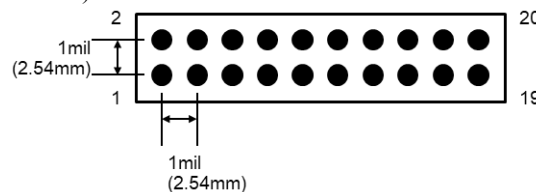


Figure 4 CN2 connectors hole pattern

4. Appendix

4.1. PCB layout

Figure 5 shows the RB-S22Q374TD20 V2 PCB layout.

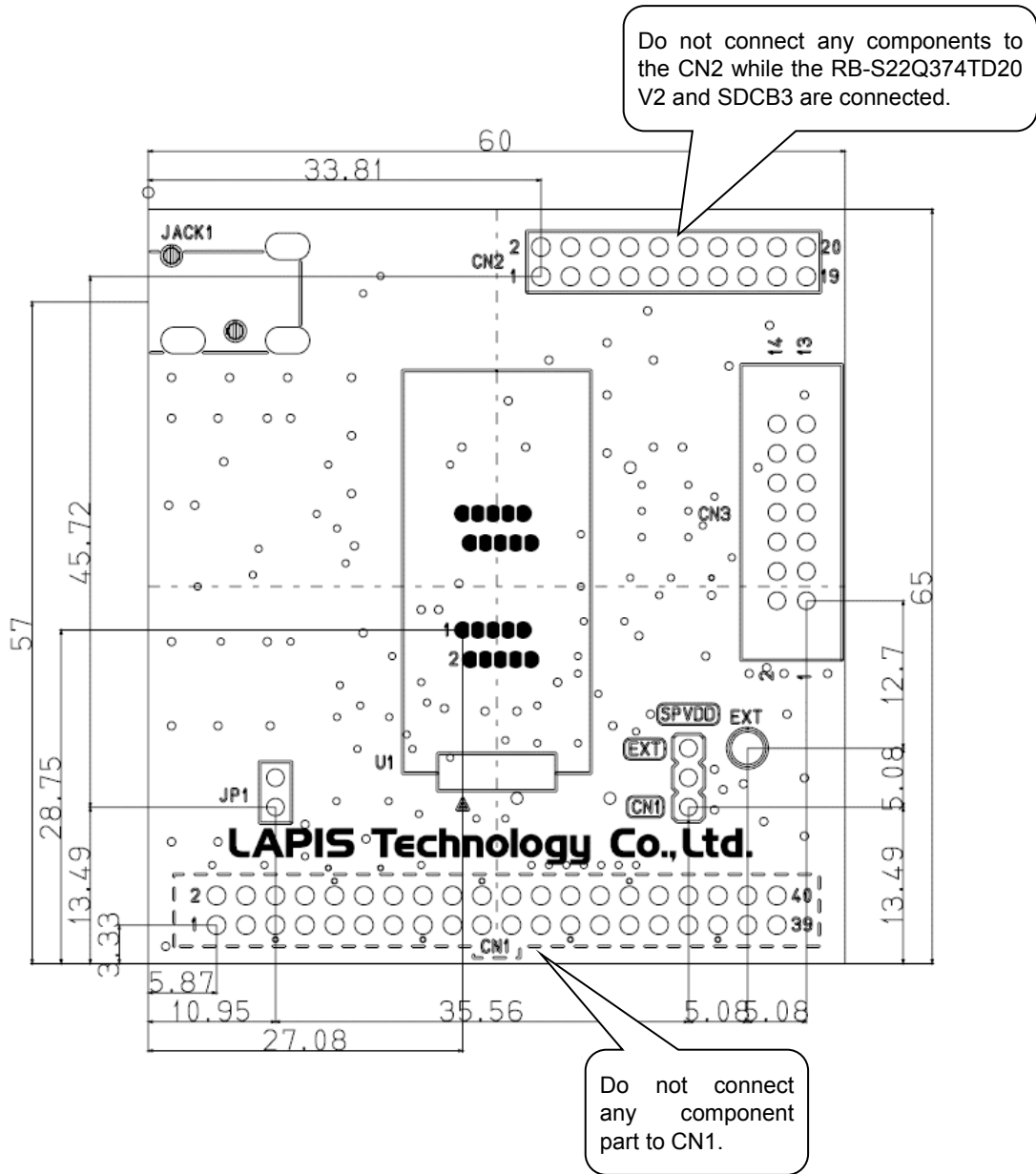


Figure 5 PCB layout

4.2. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11923	RB-S22Q374TD20 V2	PCB	1	LAPIS Technology Co., Ltd.
2	CGA3E1X7R1C105K080AC	C1	Ceramic Capacitor 1.0 μ F/16V X7R	1	TDK Corporation
3	EMK212ABJ106KD-T	C2	Ceramic Capacitor 10 μ F/16V X5R	1	TAIYO YUDEN Co., Ltd.
4	CGA3E2X7R1E104K080AA	C3,C4,C5,C8	Ceramic Capacitor 0.1 μ F/25V X7R	4	TDK Corporation
5	CGA3E1X7R1C474K080AC	C6,C7	Ceramic Capacitor 0.47 μ F/16V X7R	2	TDK Corporation
6	HIF3FB-40DA-2.54DSA(71)	CN1	40pin Receptacle	1	Hirose Electric Co., Ltd.
7	-	CN2	Unmounted	1	-
8	-	CN3	Unmounted	1	-
9	-	EXT	Unmounted	1	-
10	MCR01MZPJ000	J1,J2, J5,J8,J9,J12, J13,J16,J18	Resistor 0 Ω	9	ROHM Co., Ltd.
11	-	J3,J4, J6,J7,J10,J11, J14,J15,J17	Unmounted	9	-
12	MJ-354A0	JACK1	2-Conductor Miniature Jack	1	MARUSHIN ELECTRIC MFG. Co., Ltd.
13	-	JP1	Unmounted	1	-
14	RZF020P01TL	Q1	Pch MOSFET	1	ROHM Co., Ltd.
15	RE1C001UNTCL	Q2	Nch MOSFET	1	ROHM Co., Ltd.
16	MCR03EZPJ103	R1,R2,R4	Resistor 10k Ω \pm 5%	3	ROHM Co., Ltd.
17	MCR03EZPJ104	R3,R5	Resistor 100k Ω \pm 5%	2	ROHM Co., Ltd.
18	-	R6,R7	Unmounted	2	-
19	A2-3PA-2.54DSA(71)	SPVDD	3pin Pin Header	1	Hirose Electric Co., Ltd.
20	IC51-0202-779	U1	TSSOP20 Socket	1	YAMAICHI ELECTRONICS Co., Ltd.
21	TC7W53FU	U2,U3	2-Channel Multiplexer/Demultiplexer	2	Toshiba Corporation
22	BU27TD3WG-TR	U4	LDO Regulators	1	ROHM Co., Ltd.
23	TC7SH04FU	U5	Inverter	1	Toshiba Corporation
24	HIF3GA-2.54SP	-	Short Pin	1	Hirose Electric Co., Ltd.

5. Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22Q374RBV2-01	February 24, 2021	–	–	First edition.