Dear customer

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Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020



ML2276X/ML2286X Reference Board User's Manual

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1. Overview

This is the instruction manual for ML2276X /ML2286X Reference Board

ML2276X Reference Board supports following functions in combination with Sound Device Control Board.

- 1. Voice Playback by ML2276X
- 2. Writing voice data into ML2276X.

Please notice that the LSI written by this reference board can be used only as a prototype.

It is not guaranteed as a mass-produced quality.

ML2286X Reference Board supports following functions in combination with Sound Device Control Board.

- 1. Voice Playback by ML2286X
- 2. Writing voice data into ML2286X.

Please notice that the LSI written by this reference board can be used only as a prototype.

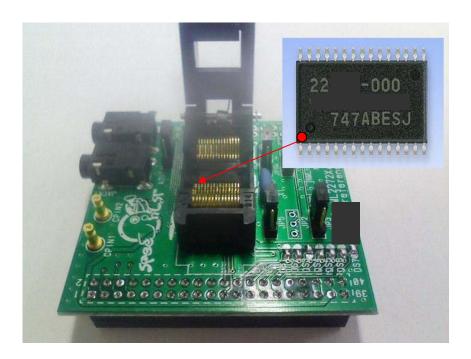
It is not guaranteed as a mass-produced quality.

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2. Operating Suggestions

It is the operating suggestions for ML2276X/ML2286X Reference Board.

- 1. Please do not supply a power to sound device control board, when the reference board is being mounted on it.
- 2. Please do not supply a power to sound device control board, when the LSIs are being mounted in the socket on the reference board. Then please confirm the aspect of the LSIs. The pin no.1 of LSIs must be placed at left near side of the socket.
- LAPIS SEMICONDUCTOR will not provide any support for this board, but the board can be exchanged with a
 new product only when it has an initial failure.



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3.1 **Circuit Diagram** VDD(5V) GND LM4890 CPIN2 Q O CPIN1 JACK1 ShutDown VOUT2 C1:0.1uF **BYPASS** GND VDD +N $\text{C3:0.1uF} \quad \text{R1:10k}\,\Omega$ VOUT1 R2 : 20k Ω C10:1uF ML2276X/ML2286X JACK2 AIN CN1_2 TESTI0 SPP CN1_3 PGM At : 7.75V RESETB SPGND C4:0.1uF CN1_4 Read Verify: 7.75V TESTO SPVDD Read Check : GND SAD0 DGND C5:0.1u CN1_6 SEL0 SG PGM At :4.4V CN1_7 TESTI1(VPP) SEL1 Read Verify: 4.4V DGND VDDR C6:0.1u CN1_1 Read Check : 3V SAD1 DVDD SCL VDDL 2.5V (300 JP8 CN1_20 20 SDA NC 2.75V CN1_19 :10uF SAD2 DGND CN1_21 18 CBUSYB NC VDD(3V) CN1_13 DGND DVDD C8:0.1u 16 XTB Crystal: 4.096MHz CN1_22 CN1_18 JP6 JP5 CN1_26 CN1_34 C10:33pF C11:33pF CN1_27 C2:10uF CN1_28 CN1_29 CN1_32 CN1_30 CN1_33 VDD(3Vor4V) CN1_31 CN1_35 Device Select CN1_36 CN1_37 CN1_38 CN1_39 CN1_40

Figure 1, ML2276X/ML2286X reference board circuit diagram

3.2 Rough PCB layout

ML2276X/ML2286X reference board rough layout is described.

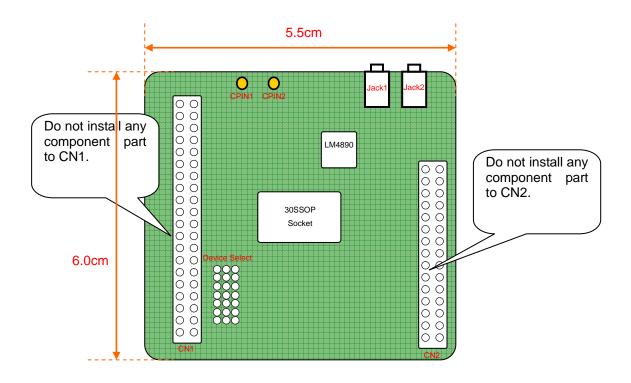
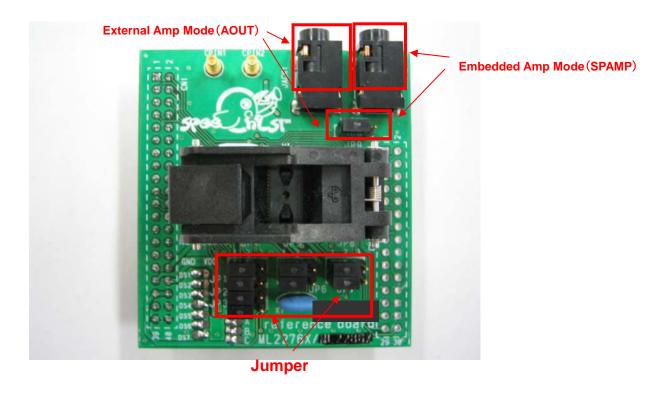
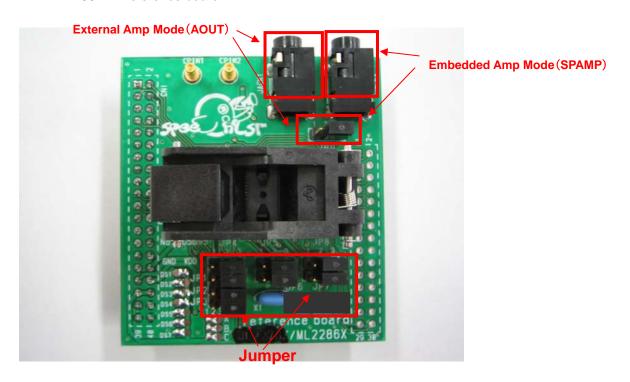


Figure 2, ML2276X/ML2286X reference board rough layout

ML2276X Reference board



ML2286X Reference board



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3.3 CN1 connector pin connections

CN1 Pin No		Connect LSI	LSI Pin No	LSI Pin Name
1	I/O	JP1	1	_
2	I/O	ML2276X/ML2286X	2	TESTI0
3	I/O	ML2276X/ML2286X	3	RESETB
4	I/O	ML2276X/ML2286X	4	TESTO
5	I/O	_		_
6	I/O	ML2276X/ML2286X	6	SEL0
7	I/O	ML2276X/ML2286X	7	SEL1
8	I/O		<u></u> _	
9	I/O	_		
10	I/O	_		
11	I/O	_		
12	I/O	_		_
13	1/0	— ML2276X/ML2286X	13	CBUSYB
14	1/0	IVILZZI OX/IVILZZOOX	10	CDOSTB
15	1/0	_		_
16	1/0	_		_
	1/0	_	_	_
17				_
18	I/O	JP4	3	_
19	I/O	JP2	3	_
20	I/O	JP2	1	_
21	I/O	JP3	1	_
22	I/O	JP4	1	_
23	I/O	_	_	_
24	I/O	_	_	_
25	Device Select	ML2276X:GND,ML2286X:VDD	_	_
26	Device Select	ML2276X:GND,ML2286X:GND	<u> </u>	_
27	Device Select	ML2276X:GND,ML2286X:GND		_
28	Device Select	ML2276X:VDD,ML2286X:VDD		_
29	Device Select	ML2276X:GND,ML2286X:GND	_	_
30	Device Select	ML2276X:GND,ML2286X:GND	_	_
31	Device Select	ML2276X:VDD,ML2286X:VDD	_	_
32	VPP	ML2276X/ML2286X	24	TESTI1(VPP)
33	VDD()	JP8	1	_
34	VDD(3V)	JP7	1	_
35	VDD(Variable)	ML2276X/ML2286X	17,22	DVDD
		SAD SEL_a(Connect)	1	_
		SAD SEL_b(Connect)	1	_
		SAD SEL_c(Connect)	1	_
36	VDD(3V)	ML2276X/ML2286X 27		SPVDD
37	VDD(5V)			ShutDown VDD
38			8,14,19,26	DGND
		SAD SEL_a(Open)		
		SAD SEL_b(Open) 3 SAD SEL_c(Open) 3		_
		SAD SEL_c(Open)		_
39	GND	ML2276X/ML2286X 28 SPGN		
40	GND	LM4890 7 GNI		

3.4 CN2 connector specificationCN2 is connecting to all ML2276X/ML2286X terminals. It has two rows 30 pins.

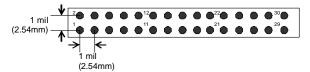


Figure 3, CN2 connectors hole pattern

3.5 CN2 connector pin connections

CN2 Pin No	LSI Pin No	LSI Pin Name
1	1	AIN
2	2	TESTI0
3	3	RESETB
4	4	TESTO
5	5	SAD0
6	6	SEL0
7	7	SEL1
8	8	DGND
9	9	SAD1
10	10	SCL
11	11	SDA
12	12	SAD2
13	13	CBUSYB
14	14	DGND
15	15	XT
16	16	XTB
17	17	DVDD
18	18	NC
19	19	DGND
20	20	NC
21	21	VDDL
22	22	DVDD
23	23	VDDR
24	24	TESTI1(VPP)
25	25	SG
26	26	DGND
27	27	SPVDD
28	28	SPGND
29	29	SPP
30	30	SPM

3.6 Jumper specifications

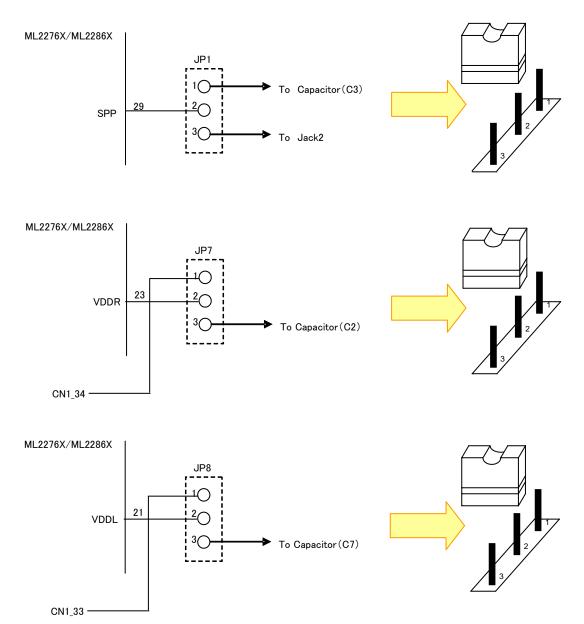
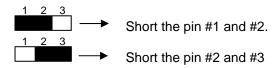


Figure 4, JP1/JP7/JP8 pattern

3.7 ML2276X/ML2286X Jumper Pin Setting



① AMP

Jumper Pin No.	SPAMP	AOUT
JP9	1 2 3	1 2 3

② Playback / Write

Lumnar Din Na	Playbad	Muito / Vouity	
Jumper Pin No.	3.3V	5.0V	Write / Verify
JP1	1 2	3	1 2 3
JP2	1 2	3	1 2 3
JP3	1 2	3	1 2 3
JP4	1 2	3	1 2 3
JP5	1 2	3	1 2 3
JP6	1 2	3	1 2 3
JP7	1 2 3	1 2 3	1 2 3
JP8	1 2	3	1 2 3

Revision History

	Date	Page		
Revision NO.		Previous Edition	Current Edition	Description
1	2008.10.20	_	_	Preliminary edition 1
		5	5	Add the Figure1
		6	6	Change the Figure Number : Figure5 -> Figure2
	2009.08.06	8	8	CN1 Pin No 2, 32:
				Change the LSI Pin Name
				CN1 Pin No 25-31 :
2				Change the text (Board Select -> Device Select) Fixed condition is specified
				CN1 Pin No 35, 38 :
				Fixed condition is specified (SAD SEL_a/b/c)
			9	Add the Figure3
		9		CH2 Pin No 2, 5, 9, 10, 11, 12, 24
				Change the LSI Pin Name
3	2011.02.02	3	3	Add to operating suggestions

ML2276X/ML2286X Reference Board User's Manual

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