Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ROHM GROUP
LAPIS TECHNOLOGY

FEBL22620RB-04

RB-S22620TB32
User's Manual

Issue Date: February 5, 2021

ROHM SEMICONDUCTOR

Notes

1) The information contained herein is subject to change without notice.

2) When using LAPIS Technology Products, refer to the latest product information (data sheets, user's manuals, application notes, etc.), and ensure that usage conditions (absolute maximum ratings, recommended operating conditions, etc.) are within the ranges specified. LAPIS Technology disclaims any and all liability for any malfunctions, failure or accident arising out of or in connection with the use of LAPIS Technology Products outside of such usage conditions specified ranges, or without observing precautions. Even if it is used within such usage conditions specified ranges, semiconductors can break down and malfunction due to various factors. Therefore, in order to prevent personal injury, fire or the other damage from break down or malfunction of LAPIS Technology Products, please take safety at your own risk measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. You are responsible for evaluating the safety of the final products or systems manufactured by you.

3) Descriptions of circuits, software and other related information in this document are provided only to illustrate the standard operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. And the peripheral conditions must be taken into account when designing circuits for mass production. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, and other related information.

4) No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Technology or any third party with respect to LAPIS Technology Products or the information contained in this document (including but not limited to, the Product data, drawings, charts, programs, algorithms, and application examples、etc.). Therefore LAPIS Technology shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

5) The Products are intended for use in general electronic equipment (AV/OA devices, communication, consumer systems, gaming/entertainment sets, etc.) as well as the applications indicated in this document. For use of our Products in applications requiring a high degree of reliability (as exemplified below), please be sure to contact a LAPIS Technology representative and must obtain written agreement: transportation equipment (cars, ships, trains, etc.), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems, etc. LAPIS Technology disclaims any and all liability for any losses and damages incurred by you or third parties arising by using the Product for purposes not intended by us. Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters, etc.

6) The Products specified in this document are not designed to be radiation tolerant.

7) LAPIS Technology has used reasonable care to ensure the accuracy of the information contained in this document. However, LAPIS Technology does not warrant that such information is error-free and LAPIS Technology shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

8) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. LAPIS Technology shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

9) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act..

10) Please contact a ROHM sales office if you have any questions regarding the information contained in this document or LAPIS Technology's Products.

11) This document, in part or in whole, may not be reprinted or reproduced without prior consent of LAPIS Technology.

(Note) "LAPIS Technology" as used in this document means LAPIS Technology Co., Ltd.

LAPIS Technology Co.,Ltd.

2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/

Table of Contents

1. Overview

This instruction manual is for the RB-S22620TB32 which is reference board for the ML22620 (hereinafter referred to as "Speech Synthesis LSIs").

This board can be combined with Sound Device Control Board 3 (hereinafter referred to as "SDCB3") to do the following:

- Voice playback by ML22620.
- Writing sound code data into serial FLASH memory.

By connecting a flash writer to the RB-S22620TB32, sound code data can be written to the serial flash memory.

2. Operational notes

The following describes the precautions to follow when handling the RB-S22620TB32.

- Turn off the power when attaching the RB-S22620TB32 to the SDCB3.
- Turn off the power when loading Speech Synthesis LSIs into the RB-S22620TB32. Pin 1 is the position of the board silk ▲ at the bottom left with respect to the socket opening. The Figure 1 shows the setting directions of Speech Synthesis LSIs.
- The ML22620 supply voltages are 2.7 to 3.6V / 3.3 to 5.5V. Use the RB-S22620TB32 with a power supply voltage of 3.0V.
- Connect LOUT jack and SP jack to the mono speaker.

- RB-S22620TB32 is a device used only by experts in R&D facilities for research and development purposes. RB-S22620TB32 is not intended to be used in mass-produced products or parts thereof.
- The information in this document is subject to change without notice due to product improvement and technological improvement. Prior to use, please ensure that the information is up to date.
- LAPIS Technology does not provide any RB-S22620TB32 support. Replace only in case of initial failure.

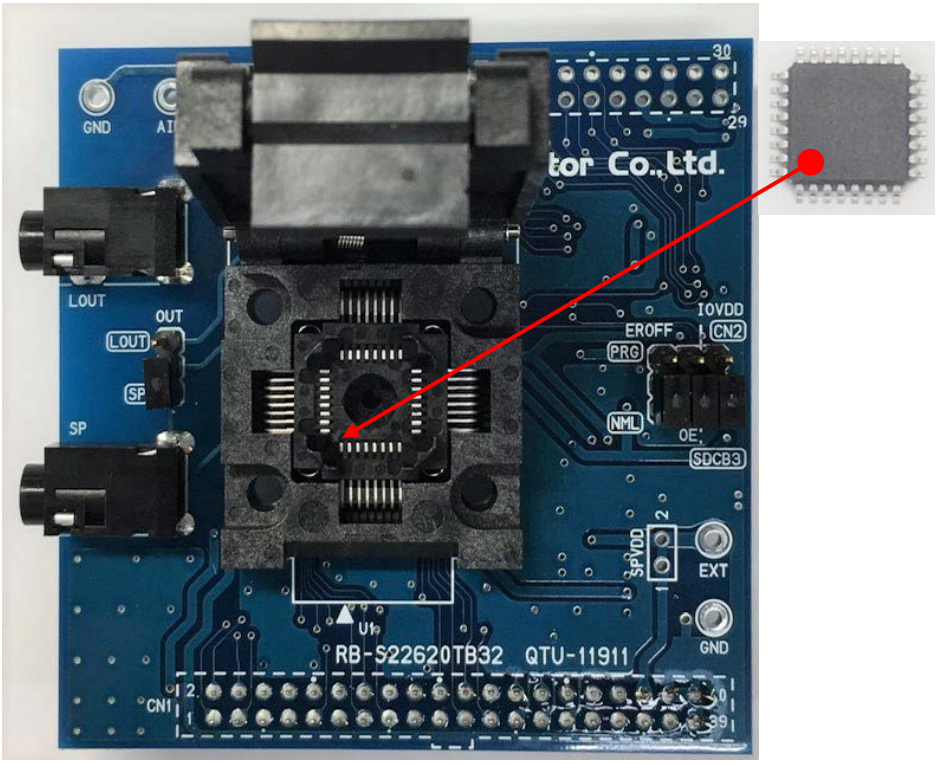


Figure 1 Outline Diagram

3. Specification

3.1. EROFF jumper pin

EROFF jumper pin is jumper pin that switch the connection of EROFF pin of Speech Synthesis LSIs.

EROFF	Contents
NML	EROFF pin is connected to CN1,CN2.
PRG	EROFF pin is connected to IOVDD.

Set to NML when connecting to SDCB3 for use. EROFF pin is controlled from SDCB3.
When this board is used by itself, setting PRG enables the serial flash memory interface of Speech Synthesis LSIs.

3.2. OE jumper pin

OE jumper pin is a jumper pin that enables or disables the signal input/output of CN1 pins to the serial flash memory pins.

OE	Contents
NML	Enable: The pins of the serial flash memory are input/output from the pins of CN1.
PRG	Disable: The pins of the serial flash memory do not input/output from the pins of CN1.

Set to NML when connecting to SDCB3 for use.
When this board is used by itself, the serial flash memory interface signal of Speech Synthesis LSIs and CN2 signal are input/output to the serial flash memory when OE jumper pin is set to PRG.

3.3. IOVDD jumper pin

IOVDD jumper pin is jumper pin that switch the connection of IOVDD pin of Speech Synthesis LSIs.

IOVDD	Contents
SDCB3	IOVDD pin is connected to the output (3.0V) of the LDO mounted on this board.
CN2	IOVDD pin is connected to 23pin of CN2.

Set to SDCB3 when connecting to SDCB3 for use.
When this board is used by itself, power can be supplied to IOVDD terminal of the speech synthesis LSI from 23pin of CN2 when IOVDD jumper pin is set to CN2.

3.4. OUT jumper pin

OUT jumper pin is jumper pin that switch the connection of SPP pin of Speech Synthesis LSIs.

OUT	Contents
LOUT	SPP pin is connected to LOUT jack.
SP	SPP pin is connected to SP jack.

3.5. LOUT jack

LOUT jack is a jack where the signal from LOUT pins of Speech Synthesis LSIs is output via the speaker amplifier.
Set Mode of Play setting of SDCB Controller to Line AMP(SPP). (Refer to Speech LSI Utility User's Manual.)
Connect a monaural speaker.

3.6. SP jack

SP jack is a jack where the signal from SPP,SPM pins of Speech Synthesis LSIs is output.
Set Mode of Play setting of SDCB Controller to Speaker AMP. (Refer to Speech LSI Utility User's Manual.)
Connect a monaural speaker.

3.7. AIN through hall

AIN through hole is used to input signals from an external source to the AIN pin of Speech Synthesis LSIs.
Input the speaker amplifier input signal to AIN through hole.

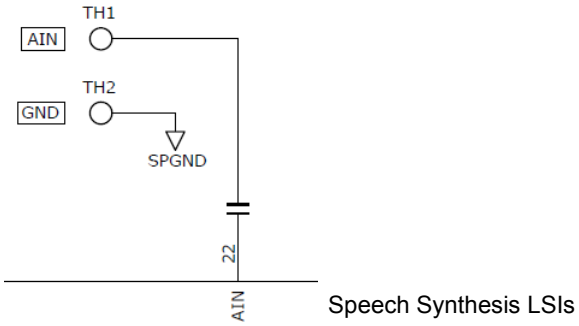


Figure 2 AIN through hall

3.8. SPVDD jumper terminal, EXT through hall

SPVDD jumper terminal is used to switch the destination of SPVDD pins of Speech Synthesis LSIs.
When supplying from SDCB3, connect 1-2pin of SPVDD jumper terminal.
To supply from an external source, cut the pattern between 1 and 2 pins of SPVDD jumper terminal and input SPVDD from the EXT throughhole.

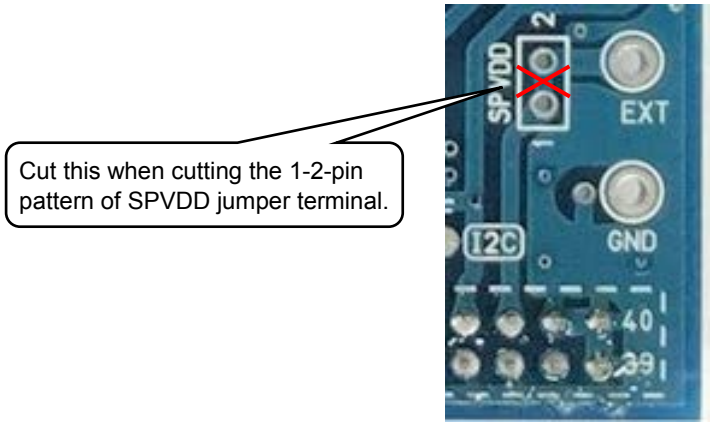


Figure 3 SPVDD jumper terminal

3.9. XT1 land, J1 land

XT1 land is used to mount the Ceramic resonator.
When using a ceramic resonator for the clock of Speech Synthesis LSIs, mount the components.
When no component is mounted, Speech Synthesis LSIs operates with built-in RC oscillation.

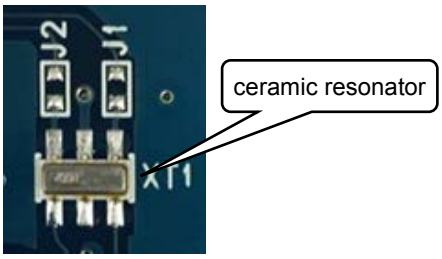


Figure 4 Ceramic resonator

A typical example of a ceramic resonator that matches XT1 land foot pattern is shown below.

Vendor	Frequency[Hz]	Parts Number
Murata Manufacturing Co., Ltd.	4M	CSTCR4M00G55B-R0
Murata Manufacturing Co., Ltd.	4.096M	CSTCR4M09G55B-R0

J1 land is land connecting the XT pin of speech synthesis LSIs to the 28pin (XT) of CN2.
To use an external clock for Speech Synthesis LSIs clock, connect the pins of the J1 land and input them from the 28pin (XT) of CN2.

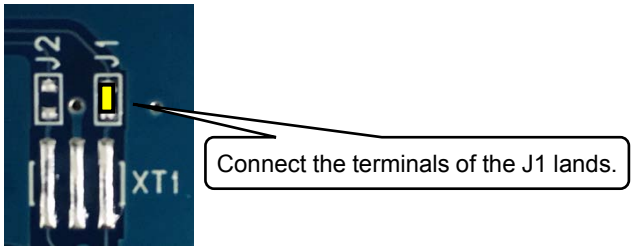


Figure 5 J1 land

3.10. CN1 connector

CN1 connector is used to connect to SDCB3.

3.11. CN2 connector

CN2 connector is used to connect to the pins of Speech Synthesis LSIs.

CN2 Pin No	LSI		I/O		
	Pin No	Pin Name	SDCB3 connection	Single unit serial flash memory interface: Enable	Single unit serial flash memory interface: Disable
1	19	DVDD *1	O	I	I
2	19	DVDD *1	O	I	I
3	28	RESETB	O	I	I
4	29	TEST0	O	I	I
5	30	STATUS1	O	O	O
6	31	STATUS2	O	O	O
7	32	CBUSYB	O	O	O
8	-	-	-	-	-
9	-	-	O	I	I
10	-	-	O	I/O	I/O
11	4	CSB	O	I	I
12	5	SCK	O	I	I
13	6	SI	O	I	I
14	7	SO	O	O	O
15	1, 18	DGND	-	-	-
16	1, 18	DGND	-	-	-
17	9	ERCSB	O	O	I
18	10	ERSCK	O	O	I
19	11	ERSI	O	O	O
20	12	ERSO	O	O	I
21	13	EROFF	O	O	I
22	-	-	-	-	-
23	14	IOVDD *1,3	O	I	I
24	-	-	-	-	-
25	1, 18	DGND	-	-	-
26	1, 18	DGND	-	-	-
27	16	XTB *2	O	O	O
28	17	XT *2	O	I	I
29	1, 18	DGND	-	-	-
30	1, 18	DGND	-	-	-

*1 Do not supply DVDD,IOVDD from CN2 when connecting SDCB3.
*2 When the J1 and J2 lands are connected, the XT and XTB pins of Speech Synthesis LSIs are input and output.
*3 Supply IOVDD externally when IOVDD jumper pin is set to CN2.

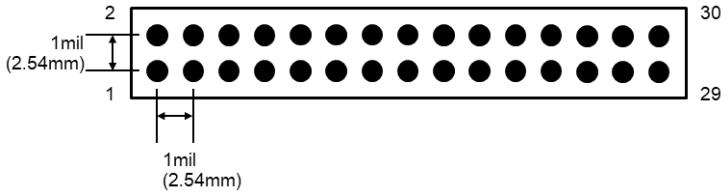


Figure 6 CN2 connectors hole pattern

4. Appendix

4.1. PCB layout

Figure 7 shows the RB-S22620TB32 PCB layout.

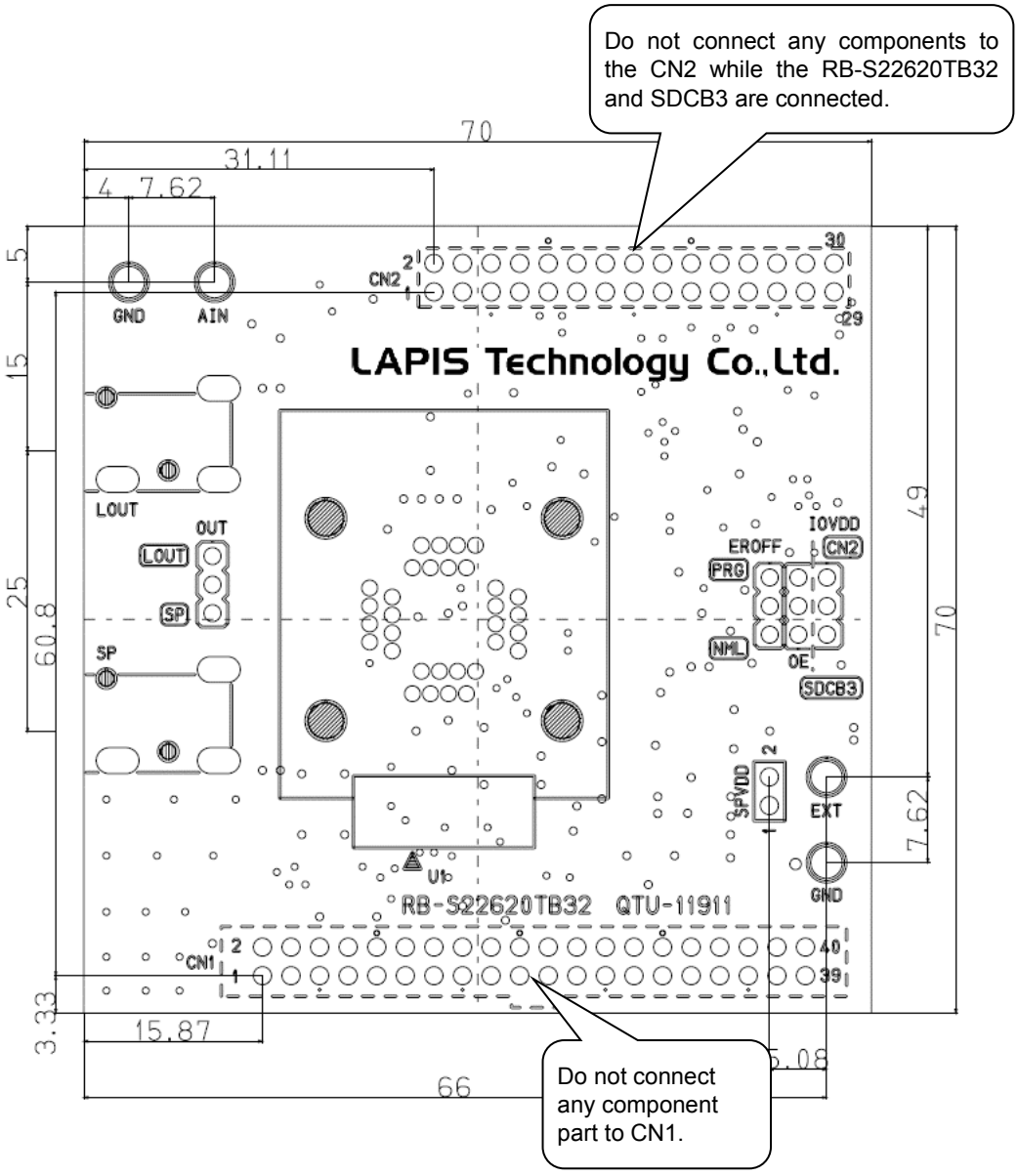
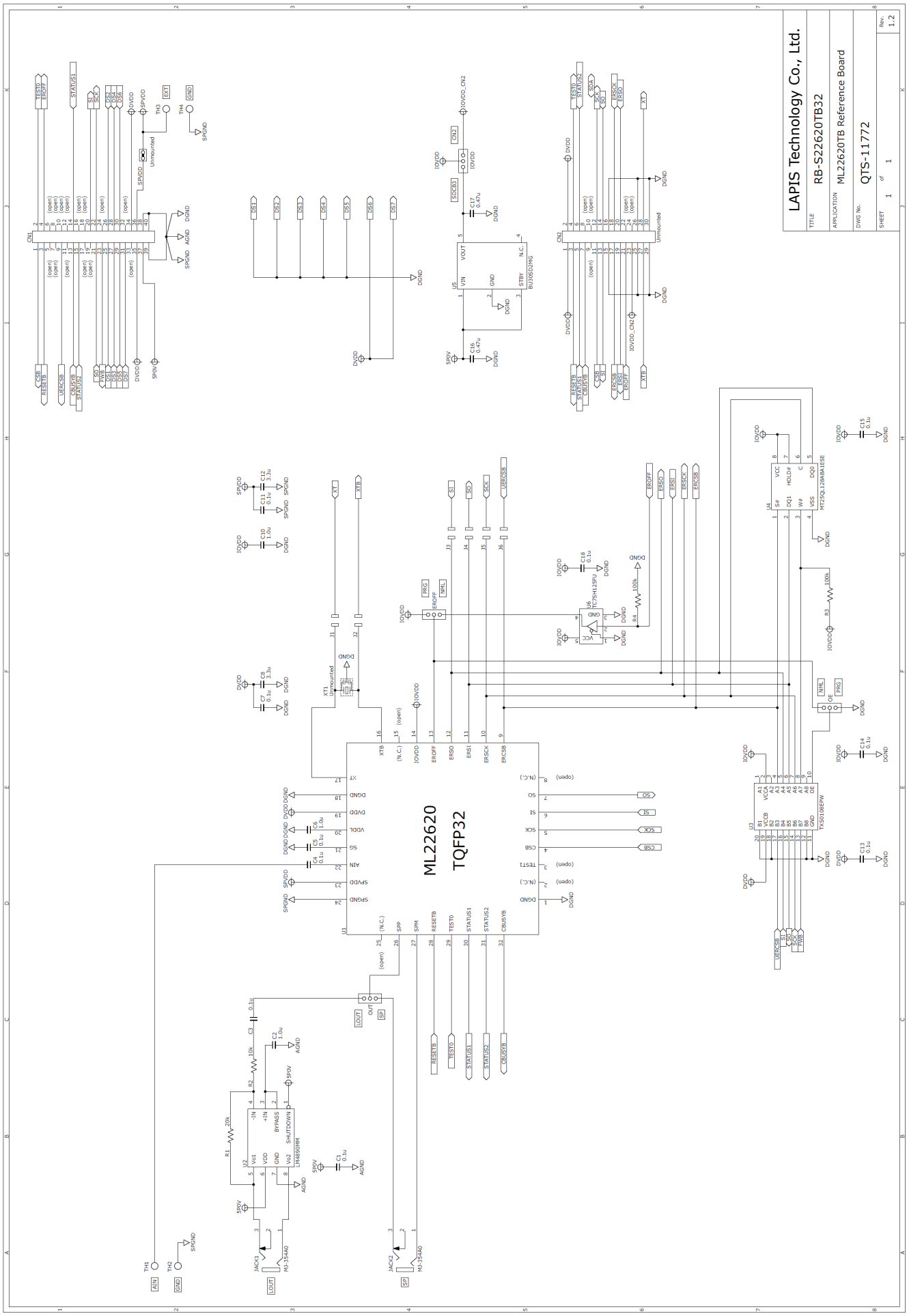


Figure 7 PCB layout

4.2. BOM list, Schematic

	Parts Number	Symbol	Contents	Qty.	Vendor
1	QTU-11911	RB-S22620TB32	PCB	1	LAPIS Technology Co., Ltd.
2	CGA3E2X7R1E104K080AA	C1,C3,C4,C5, C7,C11,C13,C14, C15,C18	Ceramic Capacitor 0.1μF/25V X7R	10	TDK Corporation
3	CGA3E1X7R1C474M080AC	C16,C17	Ceramic Capacitor 0.47μF/16V X7R	2	TDK Corporation
4	CGA3E1X7R1C105K080AC	C2,C6,C10	Ceramic Capacitor 1.0μF/16V X7R	3	TDK Corporation
5	C1608X5R1C335K080AC	C8,C12	Ceramic Capacitor 3.3μF/16V X5R	2	TDK Corporation
6	HIF3FB-40DA-2.54DSA(71)	CN1	40pin Receptacle	1	Hirose Electric Co., Ltd.
7	A2-3PA-2.54DSA	EROFF,OUT,IOVDD,OE	3pin Pin Header	4	Hirose Electric Co., Ltd.
8	MJ-354A0	JACK1,JACK2	2-Conductor Miniature Jack	2	MARUSHIN ELECTRIC MFG. CO., LTD.
9	MCR03EZPJ203	R1	Resistor 20kΩ ±5%	1	Rohm Co., Ltd.
10	MCR03EZPJ103	R2	Resistor 10kΩ ±5%	1	Rohm Co., Ltd.
11	MCR03EZPJ104	R3,R4	Resistor 100kΩ ±5%	2	Rohm Co., Ltd.
12	FPQ-32-0.8-007S-00	U1	QFP P0.80 32P Socket	1	Enplas Corporation
13	LM4890MM/NOPB	U2	Audio Power Amplifier	1	Texas Instruments Incorporated
14	TXS0108EPWR	U3	Voltage level translation	1	Texas Instruments Incorporated
15	MT25QL128ABA1ESE	U4	128Mb Serial NOR Flash Memory	1	Micron Technology, Inc.
16	BU30SD2MG-MTR	U5	LDO Regulator	1	Rohm Co., Ltd.
17	TC7SH125FU	U6	Bus Buffer with 3-State Output	1	Toshiba Corporation
18	HIF3GA-2.54SP	-	Short Pin	4	Hirose Electric Co., Ltd.
19	M20-7831542	CN2	Unmounted	1	Harwin Plc
20	-	J1,J2,J3,J4,J5,J6	Unmounted	6	-
21	A2-2PA-2.54DSA	SPVDD	Unmounted	1	Hirose Electric Co., Ltd.
22	-	TH1,TH2,TH3,TH4	Unmounted	4	-
23	CSTCR4M00G55B-R0	XT1	Unmounted	1	Murata Manufacturing Co., Ltd.


LAPIS Technology Co., Ltd.
TITLE RB-S22620TB32
APPLICATION ML22620TB Reference Board
DWG No. QTS-11772
SHEET 1 of 1
Rev. 1.2
ML22620
TQFP32

5. Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEBL22620RB-01	October 31, 2019	–	–	First edition.
FEBL22620RB-03	March 26, 2020	1	1	Figure 1 Outline Diagram
		2	2	Figure 2 PCB layout
		3	3	3.3. BOM list, Schematic
FEBL22620RB-04	February 5 2021	Notes	Notes	Change the description.
				Company name change.
		1	1	2. Operational notes Added to connect a monaural speaker to the LOUT jack and SP jack.
		-	2	3.1. EROFF jumper pin Added chapter.
				3.2. OE jumper pin Added chapter.
				3.3. IOVDD jumper pin Added chapter.
				3.4. OUT jumper pin Added chapter.
				3.5. LOUT jack Changed chapter number. Added SDCB Controller settings when using LOUT jack. Added to connect a monaural speaker to the LOUT jack.
		-	3	3.6. SP jack Changed chapter number. Added SDCB Controller settings when using SP jack. Added to connect a monaural speaker to the LOUT jack.
				3.7. AIN through hall Changed chapter number. Changed chapter name. Added connection diagram.
				3.8, SPVDD jumper terminal, EXT through hall Added chapter.
		-	4	3.9. XT1 land, J1 land Changed chapter number. Changed chapter name. Added operation in RC oscillation.
				3.10. CN1 connector Changed chapter number.
		-	5	3.11. CN2 connector Changed chapter number. Added input/output directions when SDCB3 is connected and single unit is used.

		-	6	4. Appendix Added chapter.
				4.1. PCB layout Changed chapter number. Changed Figure 7.
		-	7	4.2. BOM list, Schematic Changed chapter number. Company name change.
		-	8	4.2. BOM list, Schematic Changed chapter number. Company name change.