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ROHM Co., Ltd.
April 1, 2024

ROHM GROUP
LAPIS TECHNOLOGY

FEUL62Q2700-02

ML62Q2700 Group
User's Manual

Issue Date: Mar. 26, 2024

ROHM SEMICONDUCTOR

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LTSZ08023・01・002

Notes for product usage

Notes on this page are applicable to the all LAPIS Technology microcontroller products.
For individual notes on each LAPIS Technology microcontroller product, refer to [Note] in the chapters of each user's manual.
The individual notes of each user's manual take priority over those contents in this page if they are different.

1. HANDLING OF UNUSED INPUT PINS

Fix the unused input pins to the power pin or GND to prevent to cause the device performing wrong operation or increasing the current consumption due to noise, etc. If the handlings for the unused pins are described in the chapters, follow the instruction.

2. STATE AT POWER ON

At the power on, the data in the internal registers and output of the ports are undefined until the power supply voltage reaches to the recommended operating condition and "L" level is input to the reset pin.
On LAPIS Technology microcontroller products that have the power on reset function, the data in the internal registers and output of the ports are undefined until the power on reset is generated.
Be careful to design the application system does not work incorrectly due to the undefined data of internal registers and output of the ports.

3. ACCESS TO UNUSED MEMORY

If reading from unused address area or writing to unused address area of the memory, the operations are not guaranteed.

4. CHARACTERISTICS DIFFERENCE BETWEEN THE PRODUCT

Electrical characteristics, noise tolerance, noise radiation amount, and the other characteristics are different from each microcontroller product.
When replacing from other product to LAPIS Technology microcontroller products, please evaluate enough the apparatus/system which implemented LAPIS Technology microcontroller products.

5. USE ENVIRONMENT

When using LAPIS Technology microcontroller products in a high humidity environment and an environment where dew condensation, take moisture-proof measures.

Preface

This manual describes the operation of the hardware of the 16-bit microcontroller ML62Q2700 Group.

See the relevant manuals listed in supplementary volume; “MCU Relevant Documents list” as necessary.

Notation

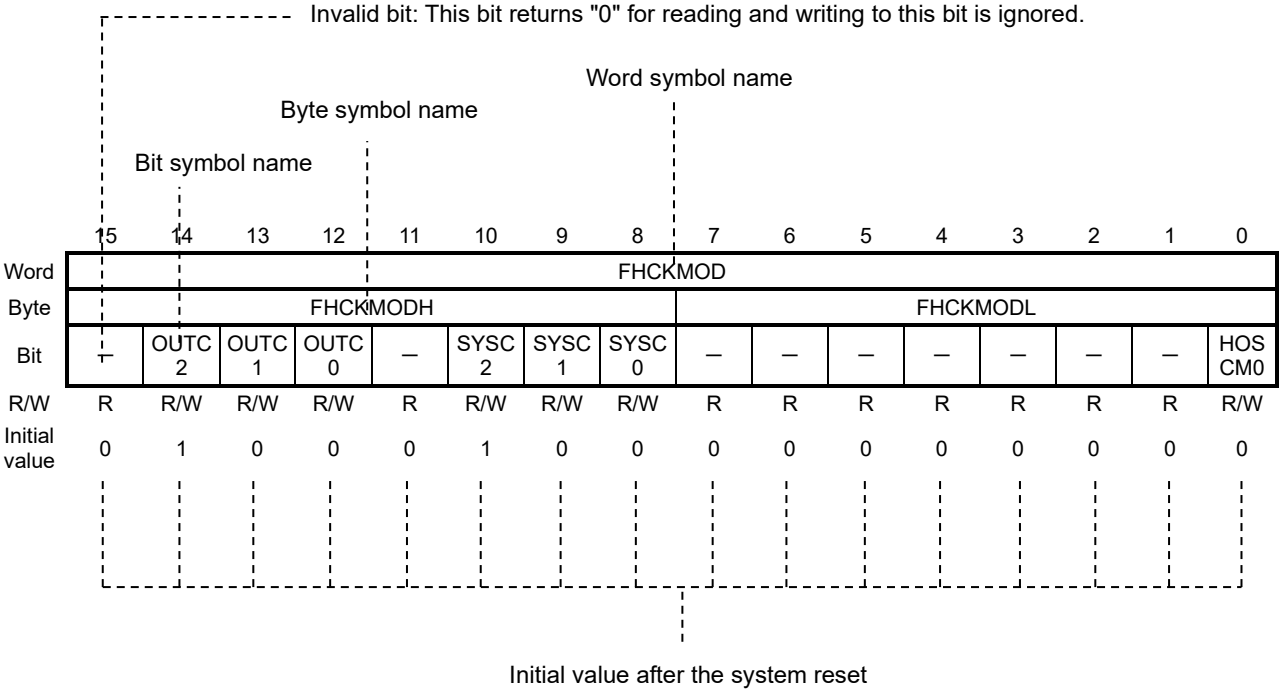
Classification	Notation	Description
Numeric value	XXh, XXH, 0xXX	Indicates a hexadecimal number.
Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	2^{10} = 1024
	kilo-, k	10^3 = 1000
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
Terminology	"H" level	Indicates high level voltage V_{IH} and V_{OH} as specified by the electrical characteristics in the data-sheet.
	"L" level	Indicates low level voltage V_{IL} and V_{OL} as specified by the electrical characteristics in the data-sheet.
	SFR	Special function register. It is control register for system or peripherals.

- Register description

"R/W" indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.

MSB: The highest bit of 16-bit register
LSB: The lowest bit of 16-bit register

Registers that have a word symbol allow the word-access. If writing or reading the registers not using the word symbol, specify the even number addresses.



Chapter 1 Overview

- **Please see the "Notes" and the "Notes for product usage" in this document.**

1. Overview

ML62Q2700 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory(Flash memory), data memory(RAM), data Flash (Erase unit:128byte, Write unit:1byte) and rich peripheral functions such as the multiplier/divider, CRC generator, Clock generator, Timer, General Purpose Ports, UART, Synchronous serial port, I^2C bus interface unit(Master, Slave), Voltage Level Supervisor(VLS), Successive approximation type 12bit A/D converter, Audio playback function, LCD driver, Safety function (IEC60730/60335 Class B) and so on.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.
The built-in on-chip debug function enables debugging and programming the software. Also, ISP (In-System Programming) function supports the Flash programming in production line.

- Applications
  Consumer and Industrial equipment (e.g., Household appliances, Housing equipment, Office equipment, Measurement instrumentation, etc)

【NOTE】
This product cannot be applicable for automotive use, automatic train control systems, and railway safety systems. Please contact ROHM sales office in advance if contemplating the integration of this product into applications that requires high reliability, such as transportation equipment for ships and railways, communication equipment for trunk lines, traffic signal equipment, power transmission systems, core systems for financial terminals and various safety control devices.

- Product List
  The ML62Q2700 Group has products as show in the Table 1-1 with multiple package and memory size combinations.

Table 1-1 Product List

Program memory	Data memory (RAM)	Data Flash	48pin TQFP48 WQFN48	52pin TQFP52	64pin QFP64 TQFP64	80pin QFP80	100pin QFP100 TQFP100
256Kbyte	16Kbyte	4Kbyte	-	-	ML62Q2727	ML62Q2737	ML62Q2747
192Kbyte			-	-	ML62Q2726	ML62Q2736	ML62Q2746
160Kbyte			-	-	ML62Q2725	ML62Q2735	ML62Q2745
96Kbyte	8Kbyte		ML62Q2703	ML62Q2713	ML62Q2723	-	-
64Kbyte			ML62Q2702	ML62Q2712	ML62Q2722	-	-

1.1 Features

- CPU
  - 16-bit RISC CPU : nX-U16/100 (A35 core)
  - Instruction system : 16-bit length instructions
  - Instruction set : Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Built-in On-chip debug function (connect to the Lapis Technology on-chip debug emulator)
  - Minimum instruction execution time: 1 count of system clock
    Approximately 30.5µs/62.5ns/41.6ns (at 32.768 kHz/16 MHz/24MHz system clock)

- Coprocessor for multiplication and division
  - Signed or Unsigned is selectable

Parameter	Expression	Operation time [cycle]
Multiplication	16bit × 16bit	4
Division	32bit ÷ 16bit	8
	32bit ÷ 32bit	16
Multiply-accumulate (non-saturating, non-saturating)	16bit × 16bit + 32bit	4

- Operating voltage and temperature
  - Operating voltage: V_{DD} = 1.8 to 5.5 V
  - Operating temperature: -40 °C to +105 °C

- Flash memory

Parameter	Program memory area	Data Flash memory area
Erase/Write count	100 cycles	10,000 cycles
Write unit	32bit(4byte)	8bit(1byte)
Erase unit	16Kbyte/1Kbyte	all area/128byte
Erase/Write temperature	0 °C to +40 °C	-40 °C to +85 °C

  - Background Operation (CPU can work while erasing and rewriting to the Data Flash memory area.)
  - The built-in on-chip debug function and ISP (In-System Programming) function enable Flash programming
    This product uses Super Flash® technology licensed from Silicon Storage Technology, Inc.
    Super Flash® is a registered trademark of Silicon Storage Technology, Inc.

- Data RAM area
  - Rewrite unit: 8bit/16bit (1byte/2byte)
  - Parity check function is available (interrupt or reset is generatable at Parity error)

- Clock generation circuit
  - Low-speed clock (LSCLK)
    Internal low-speed RC oscillation (RC32K) : Approx. 32.768 kHz
    External low-speed clock input (EXT32K) : Approx. 32.768 kHz
    External low-speed crystal oscillation (XT32K) : Approx. 32.768 kHz,
    Selectable 4 mode (Tough, Normal, Low power mode, and Ultra low power mode)
  - High-speed clock (HSCLK)
    PLL oscillation: selectable 3 oscillation frequency (24MHz ,16MHz and 1MHz) by code option
  - Built-in dedicated clock generator (RC1K: Approx. 1.024kHz) for Watch Dog Timer (WDT)
  - High-speed time base clock (HTBCLK)
    Generates a clock with a period of 2 to 8 times that of HSCLK as a peripheral clock.

- Reset
  - System resets by reset input pin, Power-On Reset, voltage level supervisor (VLS), WDT overflow, WDT invalid clear, RAM parity error, and PC error (unused ROM area access (instruction access))
  - Software reset by BRK instruction (reset CPU only)
  - Reset the peripherals individually/collectively by software

- Power management
  - Optimal power management with various standby modes
    - STOP/STOP-D mode (All clocks are stopped), HALT-D mode (clocks for System and part of the peripheral block are stopped), HALT/HALT-H mode (clocks for System are stopped)
    - HALT-D mode is suitable for long term standby, HALT-H mode is suitable for short term Intermittent operation standby
  - Individual clock input control to the peripheral blocks by software
  - High-speed clock frequency (HSCLK) is configurable (1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of PLL clock, Max. 7steps)
  - Clock gear: High-speed system clock frequency is changeable dynamically
  - (1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of HSCLK, Max 6steps)

- Interrupt controller
  - Non-maskable interrupt source : 1 (Internal sources: WDT)
  - Maskable interrupt sources : Max. 50 (included the external interrupt 9 sources)
  - Four step interrupt levels
  - External interrupt ports (EXI) : 8 (selectable from Max.32 pins) with sampling filter and edge (rise, fall, both) selection.
  - Expanded external interrupt ports : Max. 4 with sampling filter and edge(rise, fall, both)selection

- General-purpose ports (GPIO)
  - I/O port : Max. 92 (Including pins for shared functions)
  - Input port : 3 (Including one pin for shared on-chip debug and two pins for shared low speed crystal oscillation)
  - Carrier frequency output function (for IR communication)

- Watchdog timer (WDT): 1 channel
  - Overflow period: 8selectable (7.8, 15.6, 31.3, 62.5, 125, 500, 2000, 8000ms)
  - Selectable window function (enable or disable):
    configurable clear enable period (50% or 75% of overflow period) with invalid clear
    When disable, Interrupts the first overflow and resets the second overflow
    When enable, reset occurs for the first overflow
  - Selectable WDT operation : select Enable or Disable by code option
  - Selectable operation during HALT/HALT-H mode and HALT-D mode (Continue counting/Stop counting)
  - WDT counter operation monitoring function (Readable WDT counter)

- Low-speed Time base counter (LTBC): 2 channels
  - Generate 8 frequency (128, 64, 32, 16, 8, 4, 2, 1Hz) internal pulse signals by dividing the Low-speed clock (LSCLK)
  - 4 interrupts are generatable from 8 different frequencies internal pulse signals
  - One of internal pulse signals selected to interrupt can be output from general purpose port (TBCO)

- Functional timer : Max. 8 channels
  - Various modes (Continuous, One shot, capture, PWM with the same period and different duties, and complementary PWM output with the dead time)
  - Event trigger (external pin, 16bit timer, functional timer, LTBC, RC1K)
  - Selectable counter clock from various sources (divided by 1 to 8 of LSCLK, HSCLK, HTBCLK, and external clock)

- 16-bit General timers : Max. 8 channels
  - Timer output (toggled by overflow)
  - Selectable counter clock from various sources (divided by 1 to 8 of LSCLK, HSCLK, HTBCLK, LTBC, RC1K, and external clock)
  - Timer X is shared with waiting for the stability of low-speed crystal oscillation

- Synchronous Serial Port: Max. 7 channels (with FIFO: 1 channel, without FIFO: Max. 6 channels)
  - FIFO: 4steps for each transmitting and receiving
  - Selectable from Master and Slave
  - Selectable from LSB first or MSB first
  - Selectable 8-bit length or 16-bit length

- UART (Full-duplex communication mode): Max. 6 channels
  - Selectable from 5 to 8bit length, parity or no parity, odd parity or even parity, 1 stop bit or 2 stop bits, Positive logic or Negative logic, LSB first or MSB first
  - Sampling filter for receiving data and start bit
  - Built-in baud rate generator
    - 1bps to 4,800bps (Clock frequency is 32.768kHz)
    - 300bps to 2Mbps (Clock frequency is 16MHz)
    - 600bps to 3Mbps (Clock frequency is 24MHz)

- I^2C bus: 3 channels
  - Select from Master mode or Slave mode: 1 channel. Master mode only: 2 channels
  - Standard mode (100kbps), fast mode (400kbps) and 1Mbps mode(1Mbps)
  - 7bit address format
  - Master mode : Handshake (Clock synchronization), 10bit slave address format is supported
  - Slave mode : Clock stretch function

- Successive approximation type 12bit A/D converter (SA-ADC): input 14 channels
  - Conversion time: Min. 1.375μs / ch (When the VDD is higher than 2.7V and the conversion clock is 16MHz)
  - Reference voltages are selectable from VDD pin input voltage or External reference voltage (VREF pin)
  - dedicated result register for each channel
  - Continuous conversion, Trigger start, Interrupt determining by upper limit or lower limit threshold of conversion result

- Voltage Level Supervisor (VLS): 1 channel
  - Threshold voltage: selectable from 15 level (from 1.85V to 4.00V)
  - Functional Voltage level detection reset (VLS reset) or Functional Voltage level detection interrupt (VLS0 interrupt) is generatable
  - Equipped with single mode / with sampling filter / low consumption operation

- Audio playback function: 1channel
  - Audio synthesis method: 4bit ADPCM2, 8bit-non-linear PCM, 8bit Straight PCM, 16bit Straight PCM
  - Sampling frequency: 7.81kHz, 15.63kHz, 31.25kHz, 10.42kHz, 20.83kHz, 6.25kHz, 12.50kHz, 25.00kHz.

- LCD driver
  - Max. 480 dots (60seg x 8 com) [*1]

    ML62Q2702/ML62Q2703:
    24seg×8com (com Max.), 29seg×3com (seg Max.)
    ML62Q2712/ML62Q2713:
    27seg×8com (com Max.), 32seg×3com (seg Max.)
    ML62Q2722/ML62Q2723/ML62Q2725/ML62Q2726/ML62Q2727:
    35seg×8com (com Max.), 40seg×3com (seg Max.)
    ML62Q2735/ML62Q2736/ML62Q2737:
    45seg×8com (com Max.), 50seg×3com (seg Max.)
    ML62Q2745/ML62Q2746/ML62Q2747:
    60seg×8com (com Max.), 65seg×3com (seg Max.)

    [*1] : Five pins are shared for common or segment, selectable by setting a SFR
  - 1/3 bias (built-in bias generation circuit)
  - Frame frequency selection (Approx. 32Hz, 38Hz, 64Hz, 75Hz, 128Hz, and 150Hz)
  - Four bias generation modes (Internal voltage boost, External capacitive voltage divide, Internal capacitive voltage divide, and External supply voltages)
  - Contrast adjustment (16 steps) is available in the Internal voltage boost mode.

- CRC (Cyclic Redundancy Check) generator
  - Generation equation: $X^{16}+X^{12}+X^5+1$
  - Selectable from LSB first or MSB first
  - Built-in automatic program memory CRC calculation mode in HALT mode

- Safety Function
  - Automatic switching to the internal low-speed RC oscillation in case the low-speed crystal oscillation stopped
  - RAM/SFR guard
  - Automatic program memory CRC calculation
  - RAM parity error detection
  - ROM unused area access reset (instruction access)
  - Clock mutual monitoring, WDT counter monitoring
  - SA-ADC test
  - Communication loop back test (UART, Synchronous serial port, I^2C bus(master))
  - GPIO test

- Shipping package

Package	Body size (including lead) [mm × mm]	Pin pitch [mm]	Product name	
			Tray	Tape & Reel
48 pin plastic TQFP	7.0 × 7.0 (9.0 × 9.0)	0.50	ML62Q2702-xxxTBZWAY ML62Q2703-xxxTBZWAY	ML62Q2702-xxxTBZWBY ML62Q2703-xxxTBZWBY
48 pin plastic WQFN	7.0 × 7.0 (-)	0.50	ML62Q2702-xxxGDZW5AY ML62Q2703-xxxGDZW5AY	ML62Q2702-xxxGDZW5BY ML62Q2703-xxxGDZW5BY
52 pin plastic TQFP	10.0 × 10.0 (12.0 × 12.0)	0.65	ML62Q2712-xxxTBZWAY ML62Q2713-xxxTBZWAY	ML62Q2712-xxxTBZWBY ML62Q2713-xxxTBZWBY
64 pin plastic TQFP	10.0 × 10.0 (12.0 × 12.0)	0.50	ML62Q2722-xxxTBZWAY ML62Q2723-xxxTBZWAY ML62Q2725-xxxTBZWAY ML62Q2726-xxxTBZWAY ML62Q2727-xxxTBZWAY	ML62Q2722-xxxTBZWBY ML62Q2723-xxxTBZWBY ML62Q2725-xxxTBZWBY ML62Q2726-xxxTBZWBY ML62Q2727-xxxTBZWBY
64 pin plastic QFP	14.0 × 14.0 (16.0 × 16.0)	0.80	ML62Q2722-xxxGAZWAY ML62Q2723-xxxGAZWAY ML62Q2725-xxxGAZWAY ML62Q2726-xxxGAZWAY ML62Q2727-xxxGAZWAY	-
80 pin plastic QFP	14.0 × 14.0 (16.0 × 16.0)	0.65	ML62Q2735-xxxGAZWAY ML62Q2736-xxxGAZWAY ML62Q2737-xxxGAZWAY	-
100 pin plastic TQFP	14.0 × 14.0 (16.0 × 16.0)	0.50	ML62Q2745-xxxTBZWAY ML62Q2746-xxxTBZWAY ML62Q2747-xxxTBZWAY	-
100 pin plastic QFP	14.0 × 20.0 (19.0 × 25.0)	0.65	ML62Q2745-xxxGAZWAY ML62Q2746-xxxGAZWAY ML62Q2747-xxxGAZWAY	-

xxx: ROM code number, (NNN: ROM code is blank)

1.1.1 How To Read The Part Number

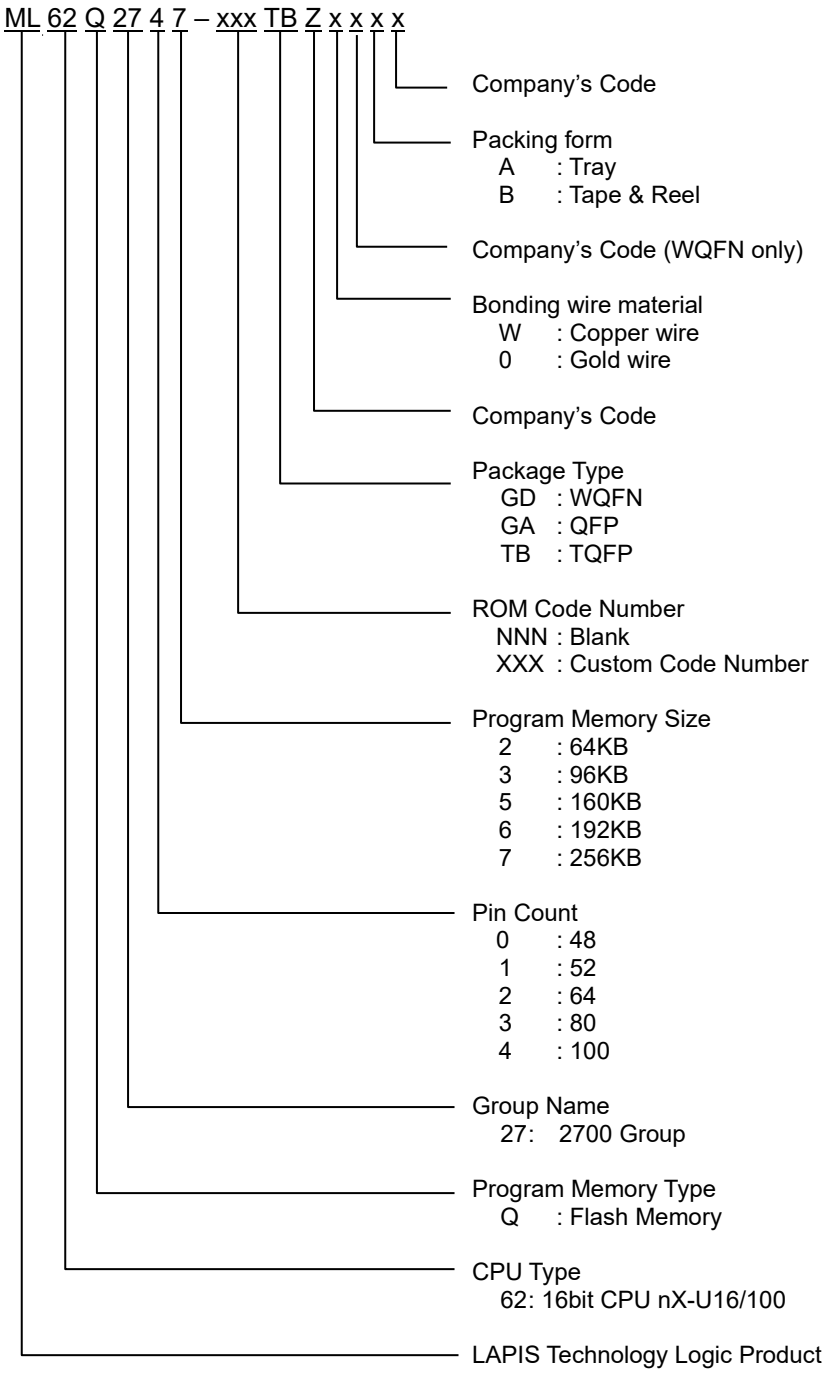


Figure 1-1 Part Number

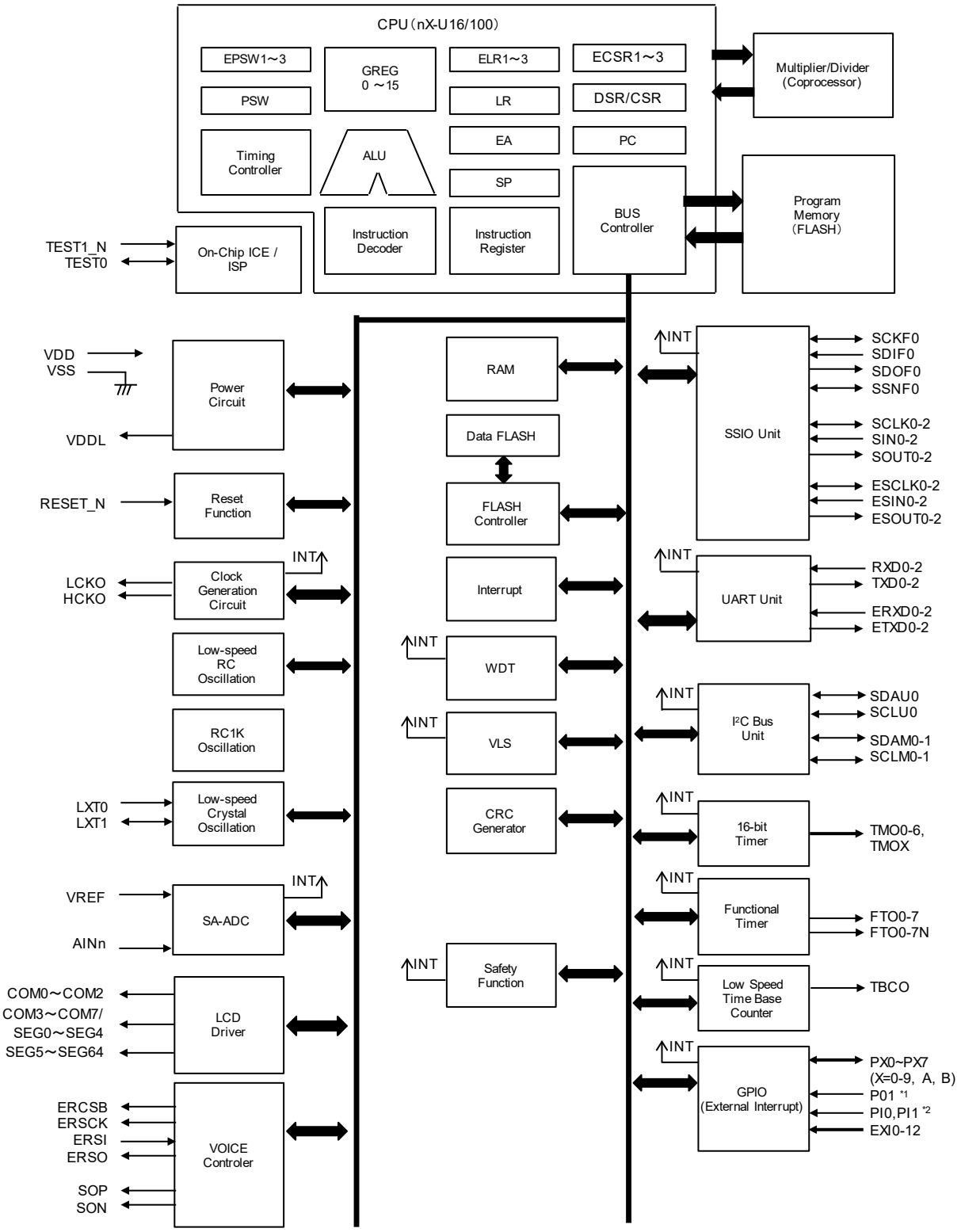
1.1.2 Main Function List

Table 1-2 Main Function List

Part number	Pin										Interrupt			Timer					Communication					Analog		Other
	Total pin count	Power pin	Reset Input pin	Debug Input port	General purpose Input pin *1	General purpose I/O pin (LED drive is supported)	LCD common/segment shared pin *2*3	LCD common pin *3	LCD segment pin *3	LCD bias pin	External interrupt pin	External interrupt source	Non maskable interrupt source	Internal maskable interrupt source	16bit Timer [ch]	16bit Functional Timer [ch]	16bit Functional Timer [Port]	Watchdog Timer [ch]	Time base counter [ch]	Synchronous serial (without FIFO) [ch]	Synchronous serial (with FIFO) [ch]	Full-duplex UART [ch]	I²C bus interface (Master only) [ch]	I²C bus unit (Master/Slave) [ch]	12bit Successive type A/D converter [ch]	Voltage Level Supervisor [ch]	Audio playback function
ML62Q2702	48	3	1	1	3	35	5	3	24	5	20	9	1	32	6	6	12	1	2	2	1	2	2	1	12	1	1
ML62Q2703																											
ML62Q2712	52					39			27		23																
ML62Q2713																											
ML62Q2722	64					51			35		32			41	8	8	16			6	1	6	2		16		
ML62Q2723																											
ML62Q2725																											
ML62Q2726																											
ML62Q2727																											
ML62Q2735	80	4				65			45		36																
ML62Q2736																											
ML62Q2737																											
ML62Q2745	100					85			60																		
ML62Q2746																											
ML62Q2747																											

*1: Shared with pins for crystal oscillation and debug input.
*2: The LCD common/segment shared pins are shared for common or segment, selectable by setting a SFR
*3: All LCD drive pins are shared with general purpose I/O ports.

1.2 Block Diagram



*1 : Not available as the input port when connecting to the on-chip debug emulator.
*2 : Not available as the input port when connecting to the crystal resonator.

Figure 1-2 Block Diagram of ML62Q2700 group

1.3 Pin

1.3.1 Pin Layout

1.3.1.1 ML62Q2745/ML62Q2746/ML62Q2747 : 100 pin TQFP

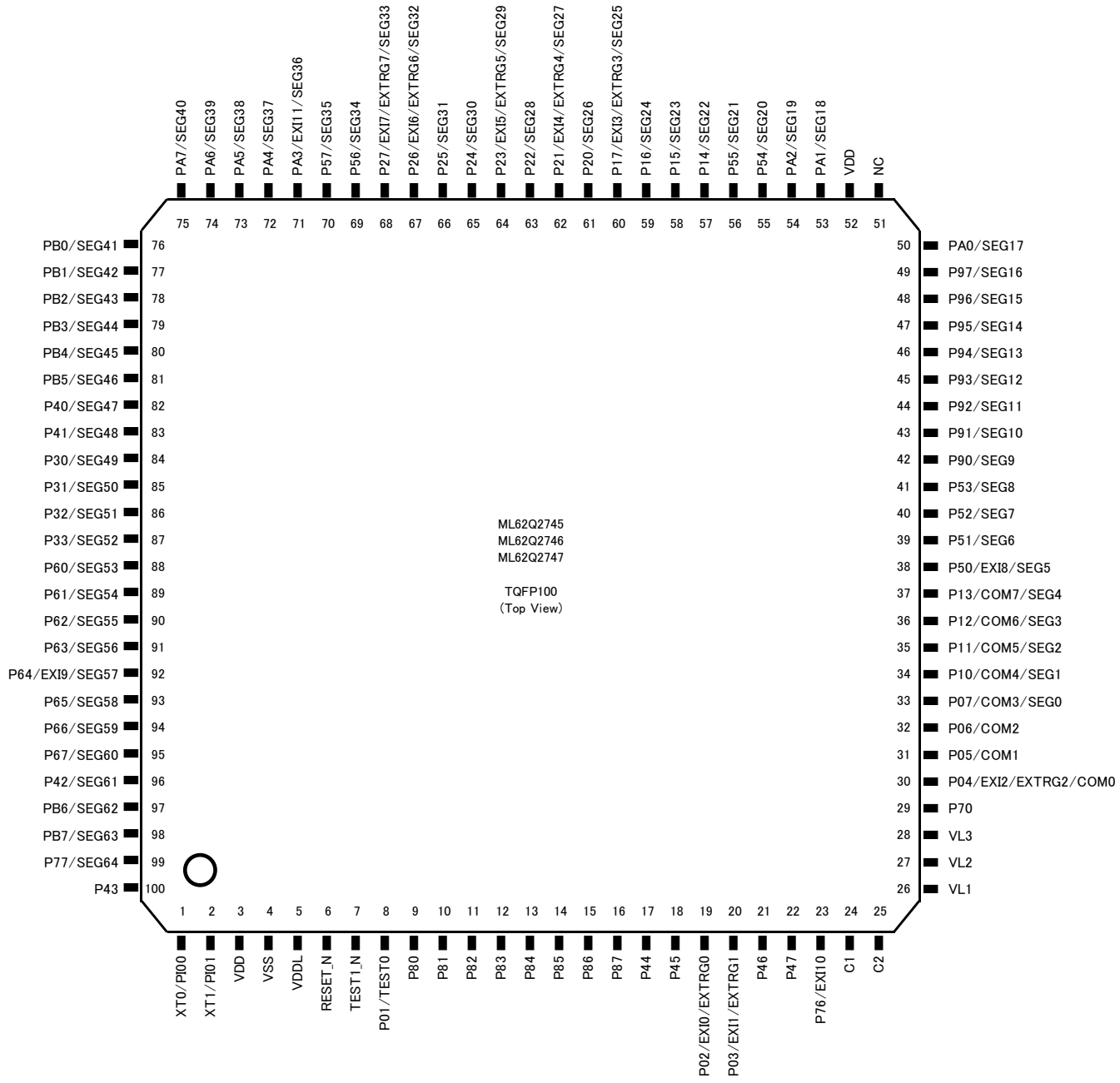


Figure 1-3-1 100 pin TQFP

1.3.1.2 ML62Q2745/ML62Q2746/ML62Q2747 : 100 pin QFP

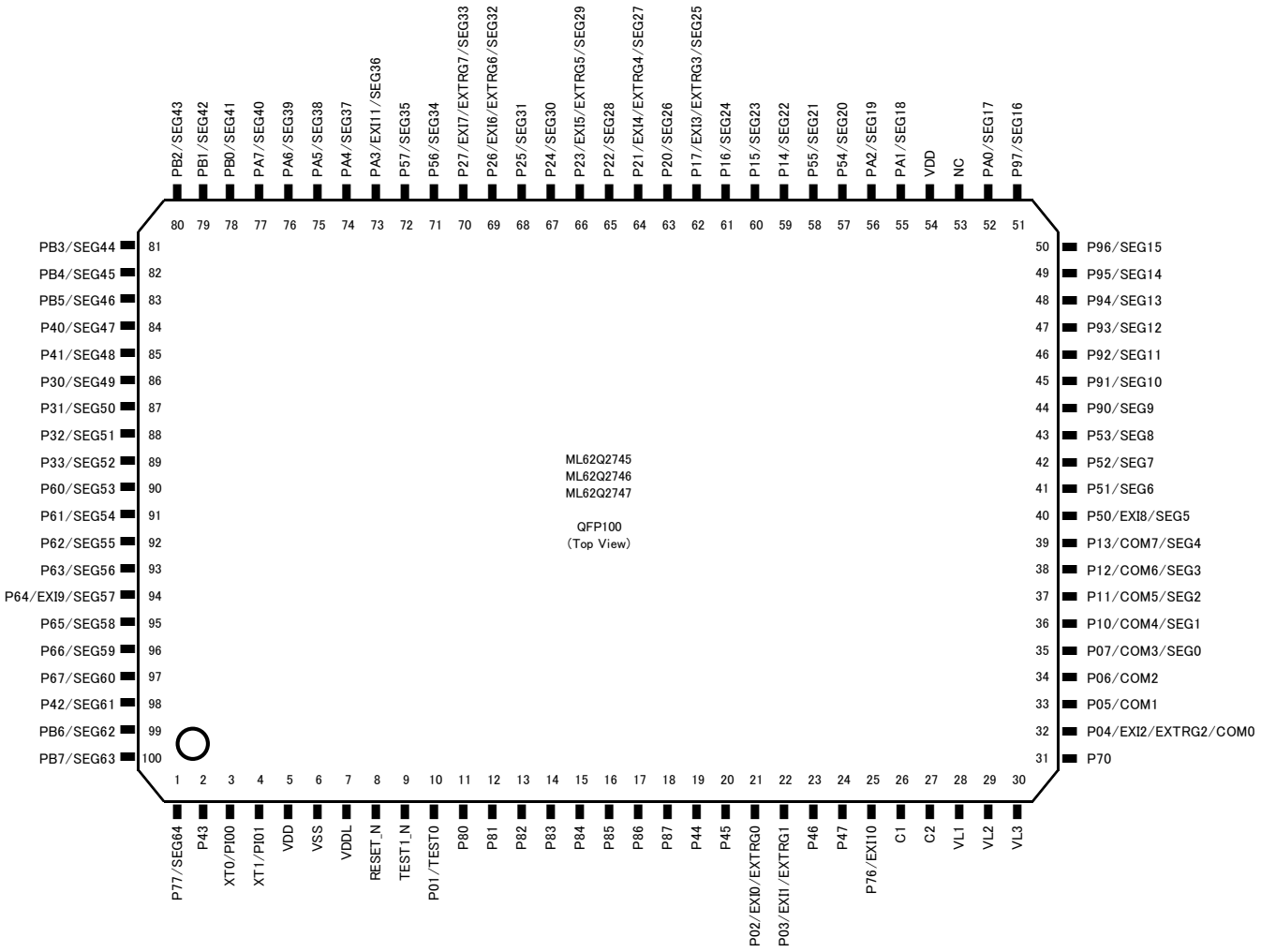


Figure 1-3-2 100 pin QFP

1.3.1.3 ML62Q2735/ML62Q2736/ ML62Q2737 : 80 pin QFP

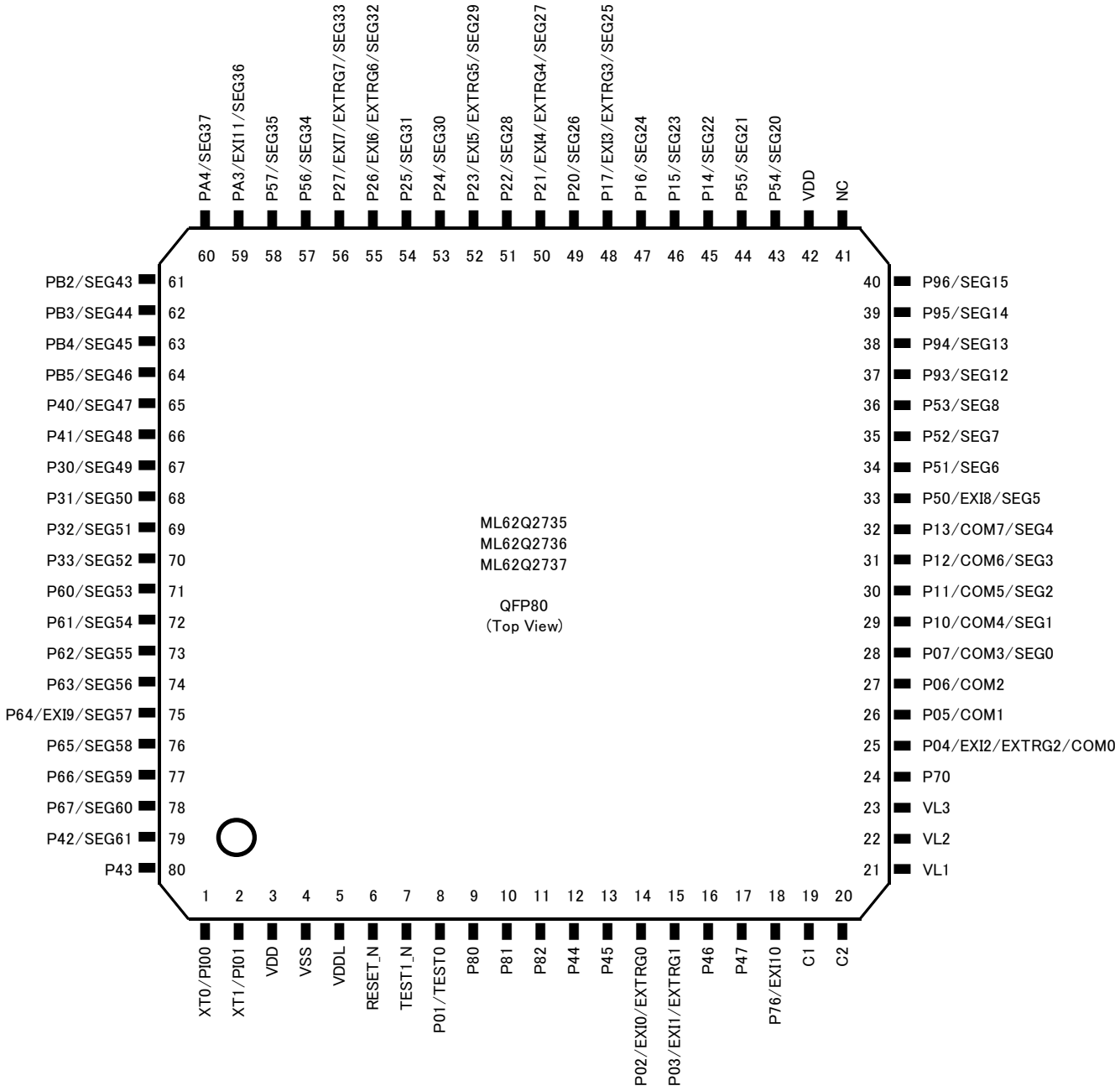


Figure 1-3-3 80 pin QFP

1.3.1.4 ML62Q2722/ML62Q2723/ML62Q2725/ ML62Q2726/ML62Q2727 : 64 pin TQFP/QFP

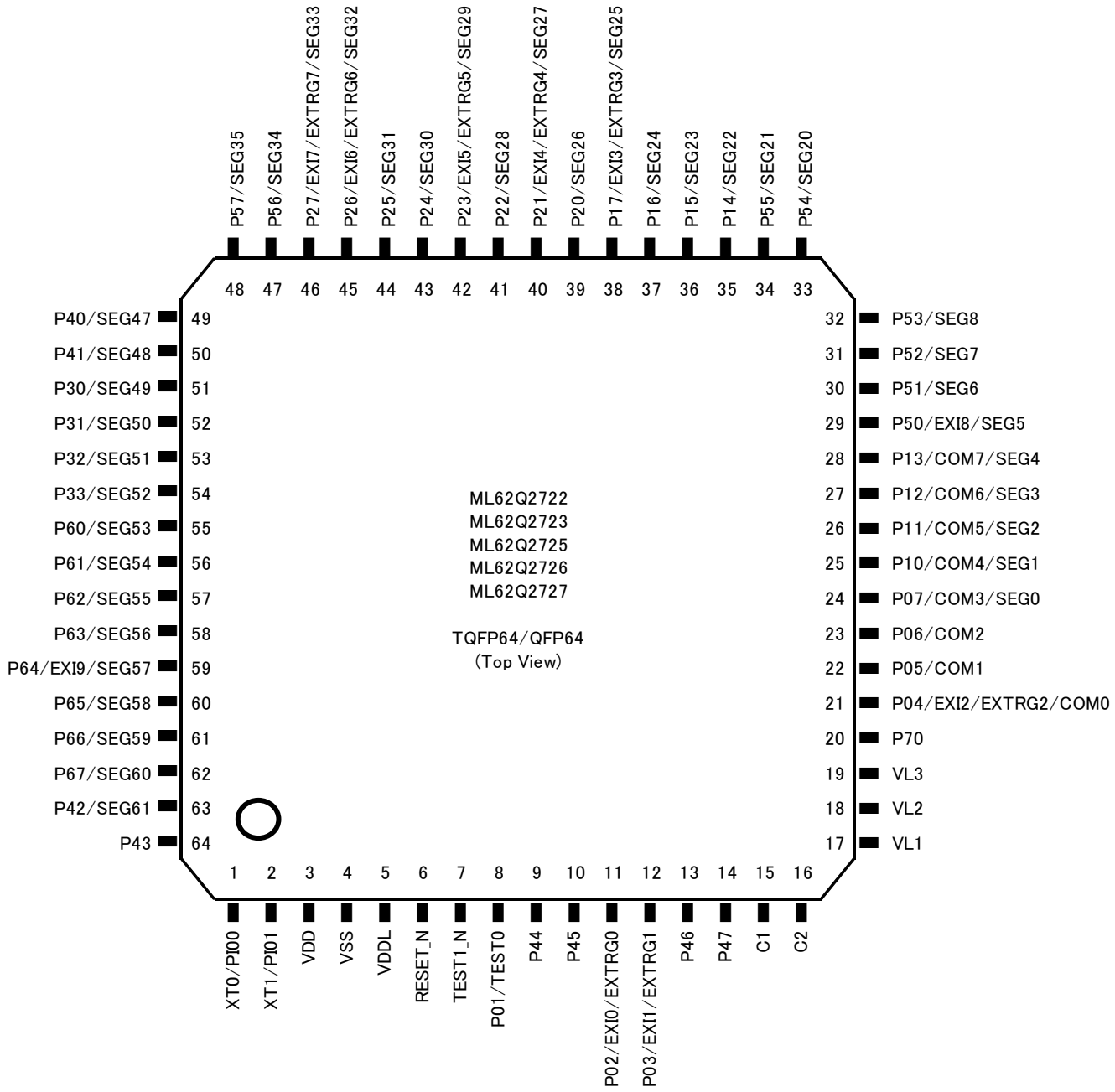


Figure 1-3-4 64 pin TQFP/QFP

1.3.1.5 ML62Q2712/ML62Q2713 : 52 pin TQFP

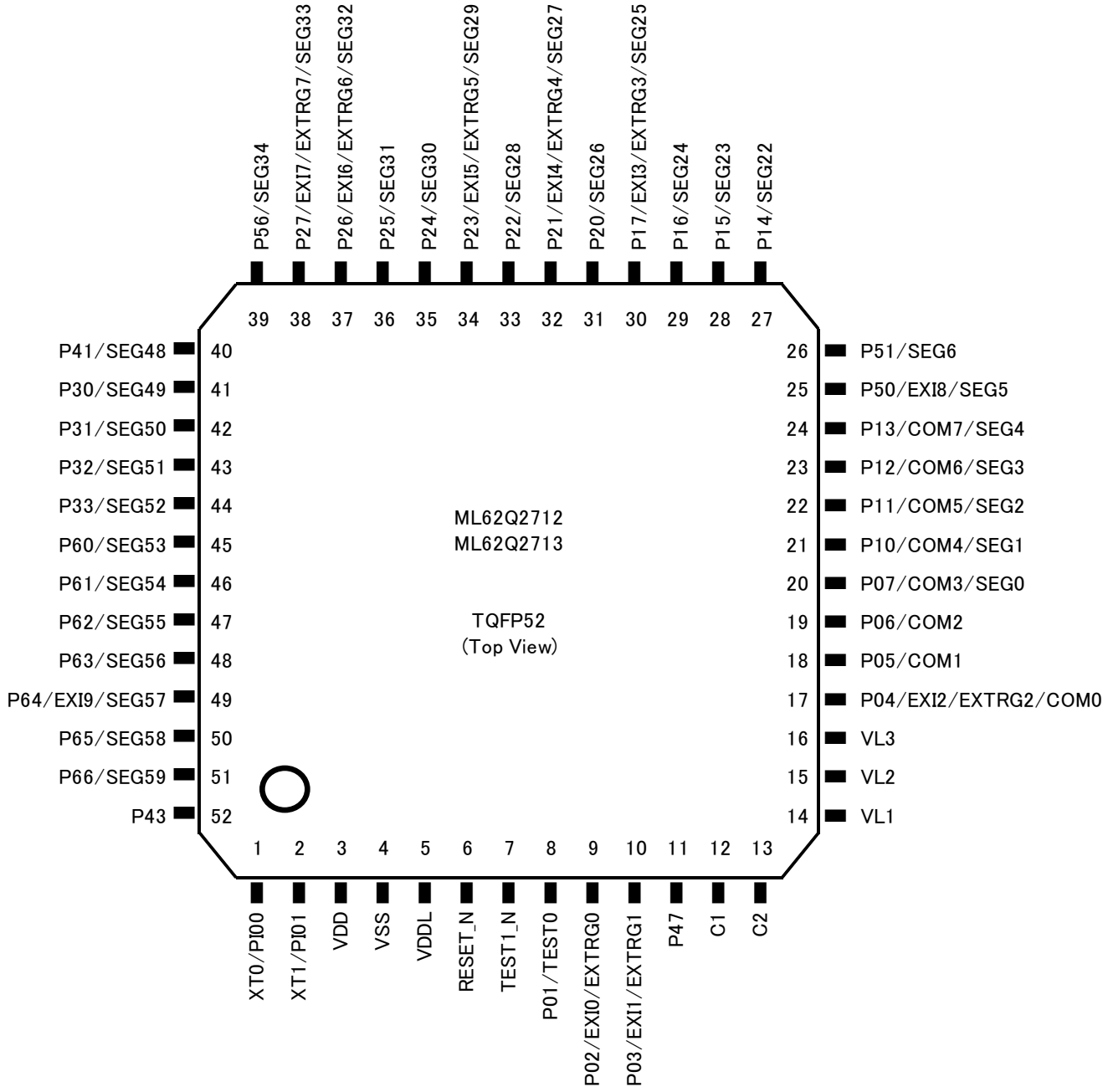


Figure 1-3-5 52 pin TQFP

1.3.1.6 ML62Q2702/ML62Q2703 : 48 pin WQFN

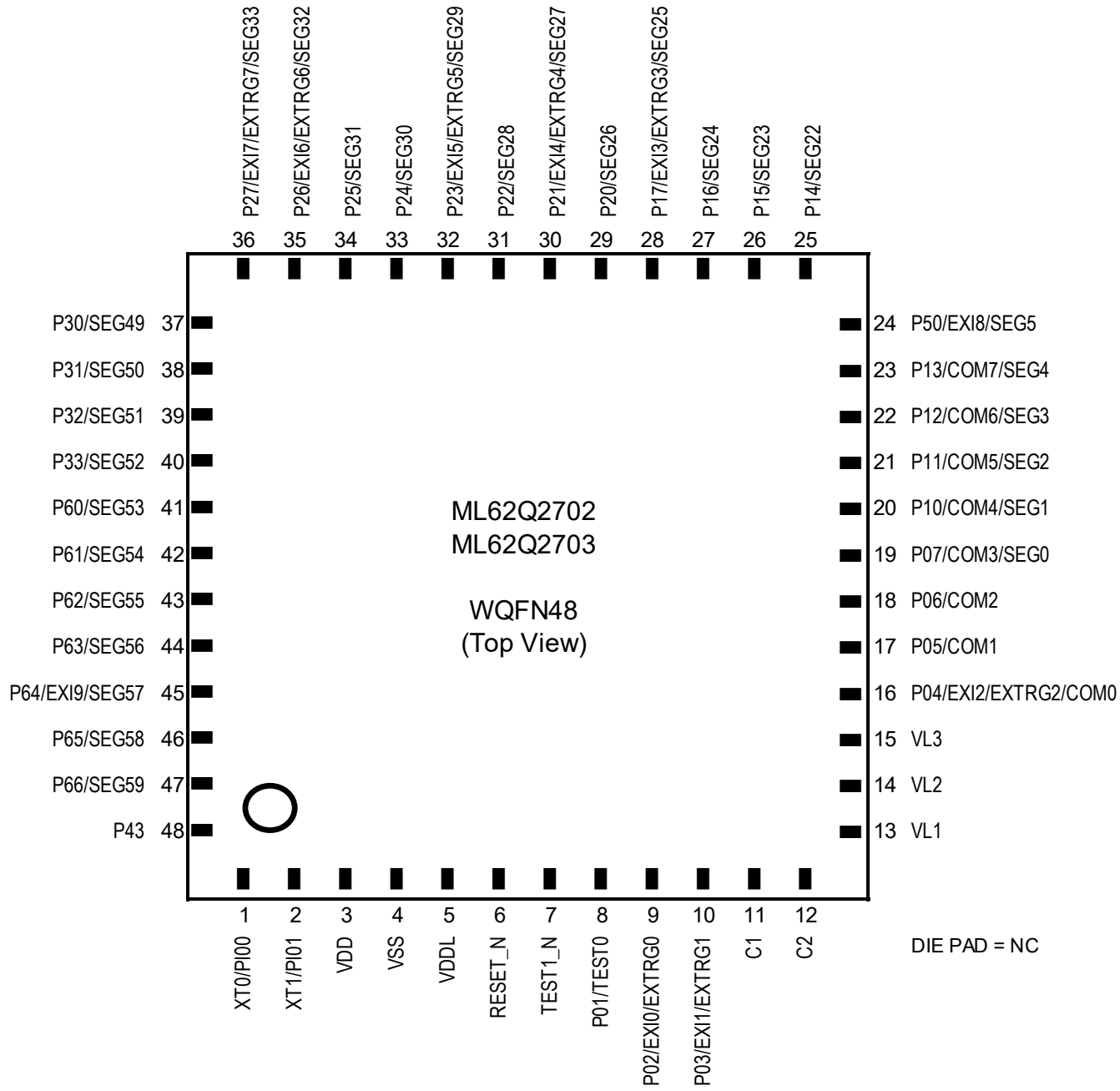


Figure 1-3-6 48 pin WQFN

1.3.1.7 ML62Q2702/ML62Q2703 : 48 pin TQFP

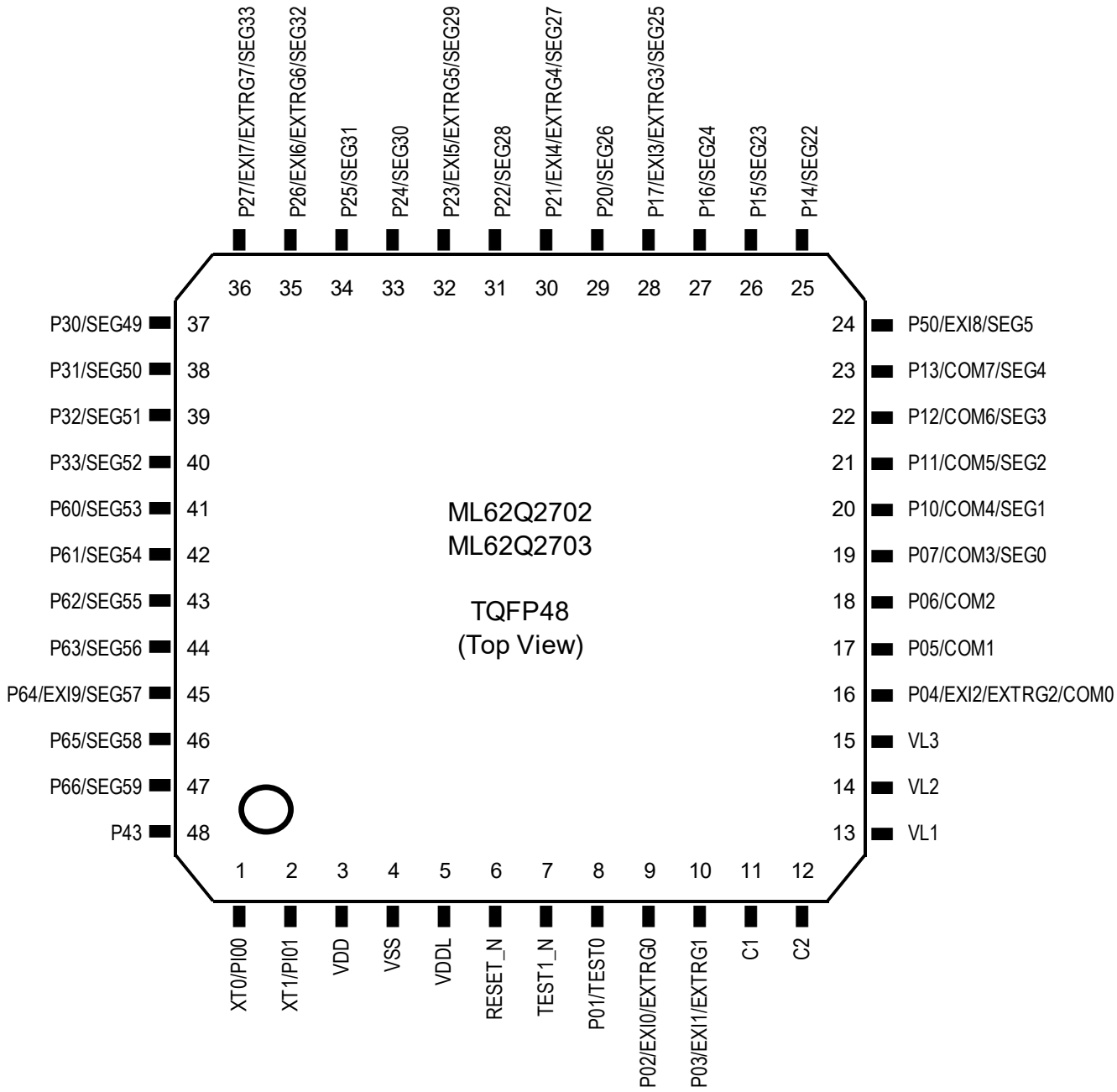


Figure 1-3-7 48 pin TQFP

1.3.2 Pin List

Table 1-3 shows the pin list of ML62Q2700 group.

Table 1-3 ML62Q2700 Group Pin List (1/3)

Pin No.						LSI Pin name	Career frequency output	1st func.	2nd func.	3rd func.	4th func.	5th func.	6th func.	7th func.
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100			EXI/ LCD/ ADC	SSIO	UART	I^2C	FTM	Timer	CLKOUT/ LTBC
3	3	3	3	3	5	VDD	-	-	-	-	-	-	-	-
-	-	-	42	52	54	VDD	-	-	-	-	-	-	-	-
4	4	4	4	4	6	VSS	-	-	-	-	-	-	-	-
-	-	-	41	51	53	NC	-	-	-	-	-	-	-	-
5	5	5	5	5	7	VDDL	-	-	-	-	-	-	-	-
1	1	1	1	1	3	XT0	-	PI00	-	-	-	-	-	-
2	2	2	2	2	4	XT1	-	PI01	-	-	-	-	-	-
6	6	6	6	6	8	RESET_N	-	-	-	-	-	-	-	-
7	7	7	7	7	9	TEST1_N	-	-	-	-	-	-	-	-
8	8	8	8	8	10	P01/TEST0	-	-	-	-	-	-	-	-
9	9	11	14	19	21	P02	-	EXI0	SIN0	RXD0	SCLU0	FTO0	-	LCKO
10	10	12	15	20	22	P03	●	EXI1 AIN11	SOUT0	TXD0	SDAU0	FTO0N	-	HCKO*1
16	17	21	25	30	32	P04	-	EXI2 COM0	SCLK0	-	SCLU0	-	TMO0	-
17	18	22	26	31	33	P05	-	COM1	SIN2*3	-	-	-	-	-
18	19	23	27	32	34	P06	-	COM2	SOUT2*3	-	SDAM0	-	-	-
19	20	24	28	33	35	P07	-	COM3 SEG0	SCLK2*3	RXD0	SCLM0	-	-	-
20	21	25	29	34	36	P10	-	COM4 SEG1	-	TXD0	-	-	-	-
21	22	26	30	35	37	P11	●	EXI1 COM5 SEG2	SCLK0	-	-	-	-	-
22	23	27	31	36	38	P12	-	EXI6 COM6 SEG3	SIN0	RXD0	-	-	TMO4	-
23	24	28	32	37	39	P13	●	EXI7 COM7 SEG4	SOUT0	TXD0	-	-	TMO1	TMO3
25	27	35	45	57	59	P14	-	EXI2 SEG22	SDIF0	-	-	-	-	ERSI*2
26	28	36	46	58	60	P15	-	SEG23	SSNF0	-	SDAU0	-	-	ERCSB*2
27	29	37	47	59	61	P16	-	SEG24	SCLK1	SDOF0*2	SCLU0	-	TMO5*3	ERSO*2
28	30	38	48	60	62	P17	-	EXI3 SEG25 AIN0	-	RXD0	-	FTO1	-	-
29	31	39	49	61	63	P20	●	SEG26 AIN1	-	TXD0	-	FTO1N	-	TBCO
30	32	40	50	62	64	P21	-	EXI4 SEG27 AIN2	SIN1	RXD1	-	FTO2	-	LCKO
31	33	41	51	63	65	P22	●	AIN3 SEG28	SOUT1	TXD1	SDAM0	FTO2N	-	HCKO*1
32	34	42	52	64	66	P23	-	EXI5 SEG29 VREF	SCLK1	-	SCLM0	-	TMO2	-
33	35	43	53	65	67	P24	-	SEG30 AIN4	SIN1	RXD1	-	-	-	-
34	36	44	54	66	68	P25	●	SEG31 AIN5	SOUT1	TXD1	-	-	-	-
35	37	45	55	67	69	P26	-	EXI6 SEG32 AIN6	-	RXD1	SDAU0	FTO3	-	-

*1: Assign each function; HCKO to only one LSI pin.
*2: No assignment to ML62Q2747/ML62Q2746/ML62Q2745/ML62Q2737/ML62Q2736/ML62Q2735/ M62Q2727/ML62Q2726/ML62Q2725.
*3: No assignment to ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.

Table 1-3 ML62Q2700 Group Pin List (2/3)

Pin No.						LSI Pin name	Career frequency output	1st func.	2nd func.	3rd func.	4th func.	5th func.	6th func.	7th func.
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100			EXI/ LCD/ ADC	SSIO	UART	I^2C	FTM	Timer/ SOUND	CLKOUT/ LTBC/ SFMIF
36	38	46	56	68	70	P27	●	EXI7 SEG33 AIN7	36	38	46	56	68	70
37	41	51	67	84	86	P30	-	SEG49	ESIN1*3	-	-	-	-	-
38	42	52	68	85	87	P31	-	EXI1 SEG50	ESOUT1*3	-	-	-	-	TBCO
39	43	53	69	86	88	P32	-	SEG51	ESCLK1*3	RXD1	-	-	-	-
40	44	54	70	87	89	P33	●	EXI2 SEG52	-	TXD1	-	-	TMO3	-
-	-	49	65	82	84	P40	-	SEG47	-	ETXD2*3	-	-	-	-
-	40	50	66	83	85	P41	-	EXI0 SEG48	-	ERXD2*3	-	-	-	-
-	-	63	79	96	98	P42	-	SEG61	-	ETXD0*3	-	-	-	-
48	52	64	80	100	2	P43	-	EXI7 AIN10	-	-	-	-	-	TBCO
-	-	9	12	17	19	P44	-	EXI2	-	ERXD1*3	-	FTO3N	-	-
-	-	10	13	18	20	P45	-	EXI3	-	ETXD1*3	-	-	-	-
-	-	13	16	21	23	P46	-	EXI4	-	-	SDAU0	FTO1N	-	-
-	11	14	17	22	24	P47	-	EXI5	SCLK0	-	SCLU0	FTO1	-	-
24	25	29	33	38	40	P50	-	EXI8 SEG5	SCKF0	-	-	-	-	ERSCK
-	26	30	34	39	41	P51	-	EXI3 SEG6	SDOF0	-	-	-	-	ERSO
-	-	31	35	40	42	P52	-	EXI4 SEG7	SDIF0	ERXD1*3	-	-	-	ERSI
-	-	32	36	41	43	P53	-	EXI5 SEG8	SSNF0	ETXD1*3	-	-	-	ERCSB
-	-	33	43	55	57	P54	-	EXI0 SEG20	SCKF0	RXD2*3	-	FTO7*3	TMOX	-
-	-	34	44	56	58	P55	-	EXI1 SEG21	SDOF0	TXD2*3	-	FTO7N*3	-	-
-	39	47	57	69	71	P56	-	SEG34 AIN12*4	SIN2*3	RXD2*3	-	-	-	-
-	-	48	58	70	72	P57	-	SEG35 AIN13*4	SOUT2*3	TXD2*3	-	-	-	-
41	45	55	71	88	90	P60	-	SEG53	ESIN2*3	-	SCLM1	-	-	-
42	46	56	72	89	91	P61	-	EXI3 SEG54	ESOUT2*3	-	SDAM1	-	SOP	-
43	47	57	73	90	92	P62	-	SEG55	ESCK2*3	-	-	FTO4N	SON	-
44	48	58	74	91	93	P63	-	EXI4 SEG56	-	-	-	FTO4	-	-
45	49	59	75	92	94	P64	-	EXI9 SEG57	ESIN0*3	ERXD0*3	-	FTO5	-	-
46	50	60	76	93	95	P65	-	EXI5 SEG58 AIN8	ESOUT0*3	ETXD0*3	-	FTO5N	-	-
47	51	61	77	94	96	P66	-	SEG59 AIN9	ESCLK0*3	-	-	FTO6*3	-	-
-	-	62	78	95	97	P67	-	EXI6 SEG60	-	ERXD0*3	-	FTO6N*3	-	-
-	-	20	24	29	31	P70	-	EXI0	-	-	-	-	TMO6*3	-
15	16	19	23	28	30	VL3	-	-	-	-	-	-	-	-
14	15	18	22	27	29	VL2	-	-	-	-	-	-	-	-
13	14	17	21	26	28	VL1	-	-	-	-	-	-	-	-
12	13	16	20	25	27	C2	-	-	-	-	-	-	-	-
11	12	15	19	24	26	C1	-	-	-	-	-	-	-	-
-	-	-	18	23	25	P76	-	EXI10	-	-	-	-	-	-
-	-	-	-	99	1	P77	-	SEG64	-	-	-	-	-	-

*3: No assignment to ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.
*4: No assignment to ML62Q2727/ML62Q2726/ML62Q2725/ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.

Table 1-3 ML62Q2700 Group Pin List (3/3)

Pin No.						LSI Pin name	Career frequency output	1st func.	2nd func.	3rd func.	4th func.	5th func.	6th func.	7th func.
48Pin	52Pin	64Pin	80Pin	TQFP100	QFP100			EXI/ LCD/ ADC	SSIO	UART	I^2C	FTM	Timer	CLKOUT/ LTBC
-	-	-	9	9	11	P80	-	EXI6	ESIN1*3	ERXD1*3	-	-	-	-
-	-	-	10	10	12	P81	-	EXI7	ESOUT1*3	ETXD1*3	-	-	-	-
-	-	-	11	11	13	P82	-	-	ESCLK1*3	-	-	-	-	-
-	-	-	-	12	14	P83	-	-	-	ERXD2*3	-	-	-	-
-	-	-	-	13	15	P84	-	-	-	ETXD2*3	-	-	-	-
-	-	-	-	14	16	P85	-	-	-	-	-	-	-	-
-	-	-	-	15	17	P86	-	-	-	-	-	FTO7*3	-	-
-	-	-	-	16	18	P87	-	-	-	-	-	FTO7N*3	-	-
-	-	-	-	42	44	P90	-	SEG9	-	-	-	-	-	-
-	-	-	-	43	45	P91	-	SEG10	-	-	-	-	-	-
-	-	-	-	44	46	P92	-	SEG11	-	-	-	-	-	-
-	-	-	37	45	47	P93	-	SEG12	ESIN1*3	ERXD1*3	-	FTO6*3	-	-
-	-	-	38	46	48	P94	-	SEG13	ESOUT1*3	ETXD1*3	-	FTO6N*3	-	-
-	-	-	39	47	49	P95	-	SEG14	ESCLK1*3	-	-	-	-	-
-	-	-	40	48	50	P96	-	SEG15	-	-	-	-	-	-
-	-	-	-	49	51	P97	-	SEG16	-	-	-	-	-	-
-	-	-	-	50	52	PA0	-	SEG17	-	-	-	-	-	-
-	-	-	-	53	55	PA1	-	SEG18	-	-	-	-	-	-
-	-	-	-	54	56	PA2	-	SEG19	-	-	-	-	-	-
-	-	-	59	71	73	PA3	-	EXI11 SEG36 AIN14	SCLK2*3	-	-	FTO7*3	-	-
-	-	-	60	72	74	PA4	-	SEG37 AIN15	-	-	-	FTO7N*3	-	-
-	-	-	-	73	75	PA5	-	SEG38	-	-	-	-	-	-
-	-	-	-	74	76	PA6	-	SEG39	-	-	-	-	-	-
-	-	-	-	75	77	PA7	-	SEG40	-	-	-	-	-	-
-	-	-	-	76	78	PB0	-	SEG41	-	-	-	-	-	-
-	-	-	-	77	79	PB1	-	SEG42	-	-	-	-	-	-
-	-	-	61	78	80	PB2	-	SEG43	ESIN2*3	ERXD2*3	-	-	-	-
-	-	-	62	79	81	PB3	-	SEG44	ESOUT2*3	ETXD2*3	-	-	-	-
-	-	-	63	80	82	PB4	-	SEG45	ESCLK2*3	-	-	-	-	-
-	-	-	64	81	83	PB5	-	SEG46	-	ERXD2*3	-	-	-	-
-	-	-	-	97	99	PB6	-	SEG62	-	-	-	-	-	-
-	-	-	-	98	100	PB7	-	SEG63	-	-	-	-	-	-

*3: No assignment to ML62Q2723/ML62Q2713/ML62Q2703/ML62Q2722/ML62Q2712/ML62Q2702.

1.3.3 Pin Description

Table 1-4 shows the pin list categorized by the function.
"-" : Power pin, "I": Input pin, "O" Output pin and "I/O" : input/output pin

Table 1-4 Pin Description (1/5)

Function	Functional pin name	LSI pin name	I/O	Description
Power	-	VSS	-	Negative power supply pin (-) Define this terminal potential as V_{SS}.
	-	VDD	-	Positive power supply pin (+). Connect a capacitor C_V (more than 1µF) between this pin and VSS. Define this terminal potential as V_{DD}.
	-	VDDL	-	Power supply for internal logic (internal regulator's output). Connect a capacitor C_L (1µF) between this pin and VSS.
Debug ISP	TEST0	P01/ TEST0	I/O	Input/output for testing This pin which is shared with P01 is used as on-chip debug interface and ISP function. and is initialized as pull-up input mode by the system reset.
	TEST1_N	TEST1_N	I	Input for testing This pin is used as on-chip debug interface, ISP function, and is initialized as pull-up input mode by the system reset.
Reset	RESET_N	RESET_N	I	Reset input. Appling this pin "L" level shifts MCU to system reset mode. Appling this pin "H" level shifts MCU to program running mode. No pull-up resistor is built-in.
Not used	NC	NC	-	Open
General input port (GPI)	PI00, PI01	XT0, XT1	I	General purpose input. - High-impedance (initial value) - Input without Pull-up
	P01	P01/ TEST0	I	General purpose input. - Input with Pull-up (initial value) - Input without Pull-up Not available as general inputs when using the on-chip debug interface or ISP function.
General port (GPIO)	P02～P07	P02～P07	I/O	General purpose input/output - High-impedance (initial value) - Input with Pull-up - Input without Pull-up - CMOS output - N channel (N-ch) open drain output
	P10～P17	P10～P17		
	P20～P27	P20～P27		
	P30～P33	P30～P33		
	P40～P47	P40～P47		
	P50～P57	P50～P57		
	P60～P67	P60～P67		
	P70, P76～P77	P70, P76～P77		
	P80～P87	P80～P87		
	P90～P97	P90～P97		
	PA0～PA7	PA0～PA7		
	PB0～PB7	PB0～PB7		
Clock Input	XT0	XT0	I	Connect a Low speed(32.768kHz) crystal resonator and connect capacitors between the pin and VSS. When inputting a square wave clock, input from XT1 pin
	XT1	XT1	I/O	
Clock Output (7^{th} func.)	HCKO	P03 P22	O	High-speed clock output.
	LCKO	P02 P21	O	Low-speed clock output.
	TBCO	P20 P27 P31 P43	O	Low-speed time base counter output.
Career frequency output	-	P03 P11 P13 P20 P22 P25 P27 P33	O	Career frequency output

Table 1-4 Pin Description (2/5)

Function	Functional pin name	LSI pin name	I/O	Description
External Interrupt (1st func.)	EXI0	P02 P41 P54 P70	I	External Maskable Interrupt 0 Input
	EXI1	P03 P11 P31 P55	I	External Maskable Interrupt 1 Input
	EXI2	P04 P33 P14 P44	I	External Maskable Interrupt 2 Input
	EXI3	P17 P61 P51 P45	I	External Maskable Interrupt 3 Input
	EXI4	P21 P63 P52 P46	I	External Maskable Interrupt 4 Input
	EXI5	P23 P65 P53 P47	I	External Maskable Interrupt 5 Input
	EXI6	P26 P67 P12 P80	I	External Maskable Interrupt 6 Input
	EXI7	P27 P43 P13 P81	I	External Maskable Interrupt 7 Input
	EXI8	P50	I	External Maskable Interrupt 8 Input
	EXI9	P64	I	External Maskable Interrupt 9 Input
	EXI10	P76	I	External Maskable Interrupt 10 Input
	EXI11	PA3	I	External Maskable Interrupt 11 Input
16bit General Timer (6th func.)	TMO0	P04	O	16bit General Timer 0 output
	TMO1	P13	O	16bit General Timer 1 output
	TMO2	P23	O	16bit General Timer 2 output
	TMO3	P13 P33	O	16bit General Timer 3 output
	TMO4	P12	O	16bit General Timer 4 output
	TMO5	P16	O	16bit General Timer 5 output
	TMO6	P70	O	16bit General Timer 6 output
	TMOX	P54	O	16bit General Timer X output
Functional Timer (5th func.)	FTO0	P02	O	Functional Timer0 P output
	FTO0N	P03	O	Functional Timer0 N output
	FTO1	P17 P47	O	Functional Timer1 P output
	FTO1N	P20 P46	O	Functional Timer1 N output
	FTO2	P21	O	Functional Timer2 P output
	FTO2N	P22	O	Functional Timer2 N output
	FTO3	P26	O	Functional Timer3 P output
	FTO3N	P27 P44	O	Functional Timer3 N output
	FTO4	P63	O	Functional Timer4 P output
	FTO4N	P62	O	Functional Timer4 N output
	FTO5	P64	O	Functional Timer5 P output
	FTO5N	P65	O	Functional Timer5 N output
	FTO6	P66 P93	O	Functional Timer6 P output
	FTO6N	P67 P94	O	Functional Timer6 N output
	FTO7	P54 P86 PA3	O	Functional Timer7 P output
	FTO7N	P55 P87 PA4	O	Functional Timer7 N output
I2C Bus (4th func.)	SCLU0	P02	I/O	I2C Unit0 Clock input/output
		P04		
		P16		
		P27		
		P47		
	SDAU0	P03	I/O	I2C Unit0 Data input/output
		P15		
		P26		
		P46		
	SCLM0	P07	I/O	I2C Master0 Clock input/output
		P23		
	SDAM0	P06	I/O	I2C Master0 Clock input/output
		P22		
	SCLM1	P60	I/O	I2C Master1 Clock input/output
	SDAM1	P61	I/O	I2C Master1 Data input/output

Table 1-4 Pin Description (3/5)

Function	Functional pin name	LSI pin name	I/O	Description
UART (3rd func.)	RXD0	P02 P07 P12 P17	I	UART0 received data input
	TXD0	P03 P10 P13 P20	O	UART0 transmission data output
	RXD1	P21 P24 P26 P32	I	UART1 received data input
	TXD1	P22 P25 P27 P33	O	UART1 transmission data output
	RXD2	P54 P56	I	UART2 received data input
	TXD2	P55 P57	O	UART2 transmission data output
	ERXD0	P64 P67	I	Expanded UART0 received data input
	ETXD0	P42 P65	O	Expanded UART0 transmission data output
	ERXD1	P44 P52 P80 P93	I	Expanded UART1 received data input
	ETXD1	P45 P53 P81 P94	O	Expanded UART1 transmission data output
	ERXD2	P41 P83 PB2 PB5	I	Expanded UART2 received data input
	ETXD2	P40 P84 PB3	O	Expanded UART2 transmission data output
Synchronous Serial Port (2nd func.)	SCKF0	P50 P54	I/O	Synchronous serial0 (with FIFO) clock input/output
	SDIF0	P14 P52	I	Synchronous serial0 (with FIFO) data input
	SDOF0	P51 P55	O	Synchronous serial0 (with FIFO) data output
	SSNF0	P15 P53	I/O	Synchronous serial0 (with FIFO) slave select input/output
	SCLK0	P04 P11 P47	I/O	Synchronous serial0 clock input/output
	SIN0	P02 P12	I	Synchronous serial0 data input
	SOUT0	P03 P13	O	Synchronous serial0 data output
	SCLK1	P16 P23	I/O	Synchronous serial1 clock input/output
	SIN1	P21 P24	I	Synchronous serial1 data input
	SOUT1	P22 P25	O	Synchronous serial1 data output
	SCLK2	P07 PA3	I/O	Synchronous serial2 clock input/output
	SIN2	P05 P56	I	Synchronous serial2 data input
	SOUT2	P06 P57	O	Synchronous serial2 data output
	ESCLK0	P66	I/O	Expanded Synchronous serial0 clock input/output
	ESIN0	P64	I	Expanded Synchronous serial0 data input
	ESOUT0	P65	O	Expanded Synchronous serial0 data output
	ESCLK1	P32 P82 P95	I/O	Expanded Synchronous serial1 clock input/output
	ESIN1	P30 P80 P93	I	Expanded Synchronous serial1 data input
	ESOUT1	P31 P81 P94	O	Expanded Synchronous serial1 data output
	ESCLK2	P62 PB4	I/O	Expanded Synchronous serial2 clock input/output
	ESIN2	P60 PB2	I	Expanded Synchronous serial2 data input
	ESOUT2	P61 PB3	O	Expanded Synchronous serial2 data output
Audio Playback Function (6th func.)	SOP	P61	O	P-side output of PWM for audio
	SON	P62	O	N-side output of PWM for audio
Serial Memory Interface (7th func.)	ERSCK	P50	I/O	Serial clock output of external serial flash memory for audio
	ERSO	P16*1	O	Serial data output of external serial flash memory for audio
		P51		
	ERSI	P14	I	Serial data input for external serial flash memory for audio
		P52		
	ERCSB	P15	I/O	Chip select input/output of external serial flash memory for audio
		P53		
Successive approximation type A/D converter (SA-ADC) (1st func.)	VREF	P23	I	SA-ADC external reference voltage input Define the potential of reference voltage for SA-ADC as V_{REF}
	AIN0~AIN15	P17 P20 P21 P22 P24 P25 P26 P27 P65 P66 P43 P03 P56 P57 PA3 PA4	I	SA-ADC channel 0 to 15 analog input

Table 1-4 Pin Description (4/5)

Function	Functional pin name	LSI pin name	I/O	Description
LCD Driver	COM0	P04	-	Common output
	COM1	P05	-	Common output
	COM2	P06	-	Common output
	COM3/SEG0	P07	-	Common/Segment output shared
	COM4/SEG1	P10	-	Common/Segment output shared
	COM5/SEG2	P11	-	Common/Segment output shared
	COM6/SEG3	P12	-	Common/Segment output shared
	COM7/SEG4	P13	-	Common/Segment output shared
	SEG5	P50	-	Segment output
	SEG6	P51	-	Segment output
	SEG7	P52	-	Segment output
	SEG8	P53	-	Segment output
	SEG9	P90	-	Segment output
	SEG10	P91	-	Segment output
	SEG11	P92	-	Segment output
	SEG12	P93	-	Segment output
	SEG13	P94	-	Segment output
	SEG14	P95	-	Segment output
	SEG15	P96	-	Segment output
	SEG16	P97	-	Segment output
	SEG17	PA0	-	Segment output
	SEG18	PA1	-	Segment output
	SEG19	PA2	-	Segment output
	SEG20	P54	-	Segment output
	SEG21	P55	-	Segment output
	SEG22	P14	-	Segment output
	SEG23	P15	-	Segment output
	SEG24	P16	-	Segment output
	SEG25	P17	-	Segment output
	SEG26	P20	-	Segment output
	SEG27	P21	-	Segment output
	SEG28	P22	-	Segment output
	SEG29	P23	-	Segment output
	SEG30	P24	-	Segment output
	SEG31	P25	-	Segment output
	SEG32	P26	-	Segment output
	SEG33	P27	-	Segment output
	SEG34	P56	-	Segment output
	SEG35	P57	-	Segment output
	SEG36	PA3	-	Segment output
	SEG37	PA4	-	Segment output
	SEG38	PA5	-	Segment output
	SEG39	PA6	-	Segment output
	SEG40	PA7	-	Segment output
	SEG41	PB0	-	Segment output
	SEG42	PB1	-	Segment output
	SEG43	PB2	-	Segment output

Table 1-4 Pin Description (5/5)

Function	Functional pin name	LSI pin name	I/O	Description
LCD Driver	SEG44	PB3	-	Segment output
	SEG45	PB4	-	Segment output
	SEG46	PB5	-	Segment output
	SEG47	P40	-	Segment output
	SEG48	P41	-	Segment output
	SEG49	P30	-	Segment output
	SEG50	P31	-	Segment output
	SEG51	P32	-	Segment output
	SEG52	P33	-	Segment output
	SEG53	P60	-	Segment output
	SEG54	P61	-	Segment output
	SEG55	P62	-	Segment output
	SEG56	P63	-	Segment output
	SEG57	P64	-	Segment output
	SEG58	P65	-	Segment output
	SEG59	P66	-	Segment output
	SEG60	P67	-	Segment output
	SEG61	P42	-	Segment output
	SEG62	PB6	-	Segment output
	SEG63	PB7	-	Segment output
	SEG64	P77	-	Segment output
	C1, C2	C1, C2	-	LCD bias power source generation capacitor connection Connect a capacitor
	VL1 ~ VL3	VL1 ~ VL3	-	LCD bias power source. Connect the capacitors (C_{L1}, C_{L2}, C_{L3}) between the pin and VSS.

1.3.4 Termination of Unused Pins

Table 1-5 shows the processing of unused pins.

Table 1-5 Termination of unused pins

Pin	pin termination
NC	Open
RESET_N	Connect to VDD
TEST1_N	Connect to VDD
P01/TEST0	Open with the initial condition of pulled-up input mode
XT0, XT1	Open with the initial condition of Hi-impedance mode.
P02 ~ P07 P10 ~ P17 P20 ~ P27 P30 ~ P33 P50 ~ P57 P60 ~ P67 P70, P76, P77 P80 ~ P87 P90 ~ P97 PA0 ~ PA7 PB0 ~ PB7	
C1, C2	Open
VL1, VL2	Open
VL3	Connect to VDD Connect a resistor (1kΩ or more) between VL3 and VDD is recommended.

[Note]

- **Terminate unused input pins according to the table 1-5 in order to avoid unexpected through-current in the pins.**

Chapter 2 CPU and Memory Space

2. CPU and Memory Space

2.1 General Description

ML62Q2700 group has LAPIS Technology's original 16-bit CPU nX-U16/100 (A35 core), the multiplier/divider in the coprocessor, flash memory in the program memory space, and RAM and data flash in the data memory space.
In addition, it has the built-in remap function that remaps a 4 Kbyte area in the program memory space.
Table 2-1 show the memory size of the program memory space and the data memory space as well as the CPU memory model. For details of memory model, see "nX-U16/100 Core Instruction Manual".

Table 2-1 Program Memory Space and Data Memory Space

<table>
<tr><th rowspan="2">Product name</th><th>Program memory space</th><th>Data memory space</th><th rowspan="2">Data flash size</th><th rowspan="2">Memory model</th></tr>
<tr><th>ROM size</th><th>RAM size</th></tr>
<tr><td>ML62Q2747
ML62Q2737
ML62Q2727</td><td>256 Kbyte</td><td rowspan="3">16 Kbyte</td><td rowspan="5">4 Kbyte</td><td rowspan="4">LARGE</td></tr>
<tr><td>ML62Q2746
ML62Q2736
ML62Q2726</td><td>192 Kbyte</td></tr>
<tr><td>ML62Q2745
ML62Q2735
ML62Q2725</td><td>160 Kbyte</td></tr>
<tr><td>ML62Q2723
ML62Q2713
ML62Q2703</td><td>96 Kbyte</td><td rowspan="2">8 Kbyte</td></tr>
<tr><td>ML62Q2722
ML62Q2712
ML62Q2702</td><td>64 Kbyte</td><td>SMALL</td></tr>
</table>

2.2 CPU nX-U16/100

nX-U16/100 has following features. See "nX-U16/100 Core Instruction Manual" for details.

- Various instruction sets
  - Instructions for data transfers, arithmetic, comparison, logic operations, multiplication/division, bit manipulation, bitwise logic operations, branches, conditional branches, call/return stack manipulation, and arithmetic shifts
- Variety of addressing modes
  - Register addressing
  - Register indirect addressing
  - Stack pointer addressing
  - Control register addressing
  - EA register indirect addressing
  - General-purpose register indirect addressing
  - Direct addressing
  - Register indirect bit addressing
  - Direct bit addressing
- Memory space
  - Program memory space
  - Data memory space
- Interrupts
  - Dedicated emulator interrupt
  - Non-maskable interrupt
  - Maskable interrupt
  - Software interrupt

2.2.1 Wait Mode and No-wait Mode

ML62Q2700 group has two CPU operation modes: wait mode and no-wait mode.
The mode can be slected by Code Option. The maximum CPU operating frequency differs between the wait mode and no-wait mode depending on PLL reference frequency selected by the Code Option. Table 2-2 shows maximum operating frequency of high-speed clock, peripheral circuit and CPU. See Chapter 30 "Code Option" for details on how to set the Code Option.

Table 2-2 Maximum Operating Frequency

PLL reference frequency	Maximum operating frequency of peripheral circuit	Maximum operating frequency of CPU	
		Wait mode	No-wait mode
24MHz	24MHz	24MHz	6MHz
16MHz	16MHz	16MHz	8MHz
1MHz	1MHz	1MHz	1MHz

- Wait mode
  In this mode, instruction codes read from the program memory are stored into the built-in buffer. The CPU can work at high speed to read the instructions from the buffer. In contiguous address instruction processing, the instructions can be executed without a wait time for storing them in the buffer. In branch instruction processing, the number of execution cycles increases due to a wait time for storing the instructions in the buffer.
- No-wait mode
  This mode allows the CPU to directly execute instruction codes read from the program memory without involving the buffer. This mode minimizes the number of instruction execution cycles.

See Appendix C "Instruction execution cycle" for the number of instruction execution cycles in wait and no-wait modes.
The CPU operation mode (wait mode or no-wait mode) can be chosen by the Code Option is applied even when the low-speed clock (LSCLK) is used for the system clock.

2.2.2 Notes When Executing SB/RB Instruction

The bit access SB/RB instruction reads in bytes from a register containing the target bits, generates the byte data while rewriting only the values of the target bits, then writes it in bytes.
If an SB/RB instruction is executed to a register where multiple bits are placed, bits not targeted for the SB/RB instruction are rewritten with the values read at that time.
Note that the SB/RB instruction may rewrite the state of bits not targeted for the SB/RB instruction if it is executed to a register where values of some bits change depending on the hardware state.

2.2.3 Notes on the Description of Read-modify-write

When reading values from SFR and changing only some of the values and writing them back (read-modify-write), C compiler may convert it to a bit-access instruction. (Even if the change is two bits, it may be converted to two bit-access instructions.) Therefore, there are cases where you think you are writing at the same time, but you are not, and cases where you think you are doing word-access, but it is converted to bit-access.
If you do not want to be converted to a bit-access instruction, you can avoid it by the following description.

Example of a description that is converted to a bit-access instruction:

```
SFR &= 0xFFFE;

SFR |= 0x0081;
```

Converted to RB SFR.0 ;

Converted to SB SFR.7 ;
SB SFR.0 ;

Example of a description that is not converted to a bit-access instruction:

```
volatile unsigned short vald;
vald = SFR;
SFR = vald & 0xFFFE;

vald = SFR;
SFR = vald | 0x0081 ;
```

The conversion to bit-access instructions can be avoided by assigning the variable once to a volatile-qualified variable.

2.3 Coprocessor

ML62Q2700 group has the built-in multiplier/divider in the coprocessor.
The multiplier/divider is operated using coprocessor data transfer instructions of the CPU. For coprocessor data transfer instructions, see "nX-U16/100 Core Instruction Manual".

2.3.1 Multiplier/Divider

The multiplier/divider has following arithmetic functions:

- Multiplication : 16 bit × 16 bit (operation time 4 cycles)
- Division : 32 bit ÷ 16 bit (operation time 8 cycles)
- Division : 32 bit ÷ 32 bit (operation time 16 cycles)
- Multiply-accumulate (non-saturating) : 16 bit × 16 bit + 32 bit (operation time 4 cycles)
- Multiply-accumulate (saturating) : 16 bit × 16 bit + 32 bit (operation time 4 cycles)
- Signed or unsigned operation setting
- In a saturating multiply-accumulate operation, the result is fixed to 0x7FFF_FFFF for a positive number and 0x8000_0000 for a negative number when it is out of the expressible range.

See user's manual for the multiplication/division library using the multiplier/divider.

2.3.2 List of Coprocessor General-purpose Registers

The coprocessor general-purpose registers are byte type and readable or writable as word type registers (CERn), double word type registers (CXRn), or quad word type registers (CQRn) combining the consecutive registers.

Table 2-3 List of coprocessor general-purpose registers

Address	Coprocessor general-purpose register	Symbol name				R/W	Initial value
		Byte	Word	Double word	Quad word		
-	A register L	CR0	CER0	CXR0	CQR0	R/W	0x00
-	A register H	CR1				R/W	0x00
-	B register L	CR2	CER2			R/W	0x00
-	B register H	CR3				R/W	0x00
-	C register L	CR4	CER4	CXR4		R/W	0x00
-	C register H	CR5				R/W	0x00
-	D register L	CR6	CER6			R/W	0x00
-	D register H	CR7				R/W	0x00
-	Operation mode register	CR8	CER8	CXR8	CQR8	R/W	0x00
-	Operation status register	CR9				R/W	0x00
-	-	CR10	CER10			R/W	0x00
-	-	CR11				R/W	0x00
-	-	CR12	CER12	CXR12		R/W	0x00
-	-	CR13				R/W	0x00
-	-	CR14	CER14			R/W	0x00
-	Coprocessor ID register	CR15				R	0x81

CR0 to CR7 are registers to store the setting of the input values of operations and operation results.
CR8 is a register to set each operation mode (signed, unsigned) and to enable/disable the operation.
CR9 is a register to store the status of each operation result.
CR15 is a register to indicate coprocessor ID.
CR10 to CR14 have no function. Reading them returns "0x00". These registers are not writable.

2.3.2.1 A, B, C, D Registers (CR0 to CR7)

These registers store the input values of operations and operation results.
These are byte type registers and can be accessed as a word type register (CERn), double word type register (CXRn), or quad word type register (CQRn) combining the consecutive registers.
The bit symbols are unavailable to use in the software.

Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CER0															
Byte	CR1								CR0							
Bit	areg15	areg14	areg13	areg12	areg11	areg10	areg9	areg8	areg7	areg6	areg5	areg4	areg3	areg2	areg1	areg0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CER2															
Byte	CR3								CR2							
Bit	breg15	breg14	breg13	breg12	breg11	breg10	breg9	breg8	breg7	breg6	breg5	breg4	breg3	breg2	breg1	breg0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CER4															
Byte	CR5								CR4							
Bit	creg15	creg14	creg13	creg12	creg11	creg10	creg9	creg8	creg7	creg6	creg5	creg4	creg3	creg2	creg1	creg0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CER6															
Byte	CR7								CR6							
Bit	dreg15	dreg14	dreg13	dreg12	dreg11	dreg10	dreg9	dreg8	dreg7	dreg6	dreg5	dreg4	dreg3	dreg2	dreg1	dreg0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2-4 shows assignment of an input and results.
As soon as the data is written in register CR7, operation is started.
In a saturating multiply-accumulate operation, the result is fixed to 0x7FFF_FFFF for a positive number and 0x8000_0000 for a negative number when it is out of the expressible range.
In a signed operation, each of the most significant bits of input and output is a sign.

Table 2-4 assignment of an input and results

Quad word symbol		CQR0							
Double word symbol		CXR4				CXR0			
Word symbol		CER6		CER4		CER2		CER0	
Byte symbol		CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Multiplication 16 bit x 16 bit	Input	Multiplicand [15:0]		Multiplier [15:0]		-			
	Result	-		-		Product [31:0]			
Division 32 bit ÷ 16 bit	Input	Divisor [15:0]		-		Dividend [31:0]			
	Result	-		Remainder [15:0]		Quotient [31:0]			
Division 32 bit ÷ 32 bit	Input	Divisor [31:0]				Dividend [31:0]			
	Result	Remainder [31:0]				Quotient [31:0]			
Multiply-accumulate (non-saturating) 16 bit x 16bit + 32 bit	Input	Multiplicand [15:0]		Multiplier [15:0]		Addend [31:0]			
	Result	-		-		Multiply-accumulate [31:0]			
Multiply-accumulate (saturating) 16 bit x 16bit + 32 bit	Input	Multiplicand [15:0]		Multiplier [15:0]		Addend [31:0]			
	Result	-		-		Multiply-accumulate [31:0]			

"-" indicates that the previous value is retained.

2.3.2.2 Operation Mode Register (CR8), Operation Status Register (CR9)

The operation mode register (CR8) is a coprocessor general-purpose register to set the operation mode and enables/disables the operation.
The operation status register (CR9) is a register to store the status of each operation result.
CR8 and CR9 are byte type registers and they can be accessed as a word type register (CERn), double word type register (CXRn), or quad word type register (CQRn) combining the consecutive registers.
The bit symbols are unavailable to use in the software.

Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CER8															
Byte	CR9								CR8							
Bit	c	z	s	ov	q	-	-	use	clen	-	-	sign	-	clmod2	clmod1	clmod0
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	c	This becomes "1" if the operation result is carried or the divisor is 0 in the division mode. The value is updated in each operation. In addition, a value can be written.
14	z	This becomes "1" if the operation result is "0". The value is updated in each operation. In addition, a value can be written.
13	s	This becomes "1" if the operation result is a negative number. For a multiply-accumulate (saturating/non-saturating) operation, this indicates the state of the most significant bit in the operation result. The value is updated in each operation. In addition, a value can be written.
12	ov	This becomes "1" if the operation result exceeds the range expressible by two's complement. The value is updated every time the operation is executed. In addition, a value can be written.
11	q	This becomes "1" for the saturated result of a saturating multiply-accumulate operation. The value is held in the next operation. To initialize it to "0", it is necessary to write "0".
8	use	A bit to indicate that the operation is in progress. 0: Operation under suspension (initial value) 1: Operating
7	clen	A bit to enable/disable the operation. If the clen bit is cleared to "0" during an operation, the next operation is disabled after completion of the current one. 0: Operation disabled (initial value) 1: Operation enabled
4	sign	A bit to set the sign operation. 0: Unsigned operation (initial value) 1: Signed operation
2 to 0	clmod2 to clmod0	Bits to select the operation mode. 000: Multiplication 16 bit × 16 bit (initial value) 001: Division 32 bit ÷ 16 bit 010: Multiply-accumulate (non-saturating) 16 bit × 16 bit + 32 bit 011: Multiply-accumulate (saturating) 16 bit × 16 bit + 32 bit 100: No operation function 101: Division 32 bit ÷ 32 bit 110: No operation function 111: No operation function

Table 2-5 shows values to be set to CR8 register for execution of each operation mode.
Table 2-6 shows flags changing during each operation.

Table 2-5 Configured CR8

Value set to CR8	Signed	Unsigned
Multiplication 16 bit ×16 bit (initial value)	0x90	0x80
Division 32 bit ÷ 16 bit	0x91	0x81
Division 32 bit ÷ 32 bit	0x95	0x85
Multiply-accumulate (non-saturating) 16 bit × 16 bit + 32 bit	0x92	0x82
Multiply-accumulate (saturating) 16 bit × 16 bit + 32 bit	0x93	0x83

Table 2-6 Flag of CR9

Operation mode	sign	c	z	s	ov	q
Multiplication 16 bit × 16 bit	1 (signed)	-	●	●	-	-
	0 (unsigned)	-	●	-	-	-
Division 32 bit ÷ 16 bit	1 (signed)	●	●	●	●	-
	0 (unsigned)	●	●	-	-	-
Division 32 bit ÷ 32 bit	1 (signed)	●	●	●	●	-
	0 (unsigned)	●	●	-	-	-
Multiply-accumulate (non-saturating) 16 bit ×16 bit + 32 bit	1 (signed)	●	●	●	●	-
	0 (unsigned)	●	●	●	●	-
Multiply-accumulate (saturating) 16 bit × 16 bit + 32 bit	1 (signed)	●	●	●	●	●
	0 (unsigned)	●	●	●	●	●

●: Varies depending on the result. -: Retains the previous value.

2.3.2.3 Coprocessor ID Register (CR15)

This is a read-only register to indicate coprocessor ID.
The value in CR15 register is fixed to "0x81".
It is a byte type register and it can be accessed as a word type register (CERn), double word type register (CXRn), or quad word type register (CQRn) combining the consecutive registers.
The bit symbols are unavailable to use in the software.

Access: R
Access size: 8/16 bit
Initial value: 0x8100

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CER14															
Byte	CR15								CR14							
Bit	copid7	copid6	copid5	copid4	copid3	copid2	copid1	copid0	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

2.3.3 How to Use Multiplier/Divider

For the use of the multiplier/divider, the multiplication/division library is provided. See MULDIVU8LIB manual for details.

2.4 Memory Space

The memory space refers to the address range of the memory that can be specified from the CPU. Figure 2-1 shows the general scheme of the memory space. The memory space of the nX-U16/100 is composed of the program memory space and data memory space. The memory space is managed as one segment consists of 64 Kbyte.
The program memory space can be read with a memory access instruction through the ROM window area or the mirror area. To read the data memory space, a memory access instruction is used.
The ROM window is an area provided to read the program memory space segment 0 through a memory access instruction. In reading the program memory space from this area, it is expected to gain the advantage of data compression and improvement in access speed because it is not required to specify DSR of the data memory space. In addition, the mirror area is provided to read program memory space segments 0 to 7 through a memory access instruction. There is no address limitation when reading the program memory space from this area.

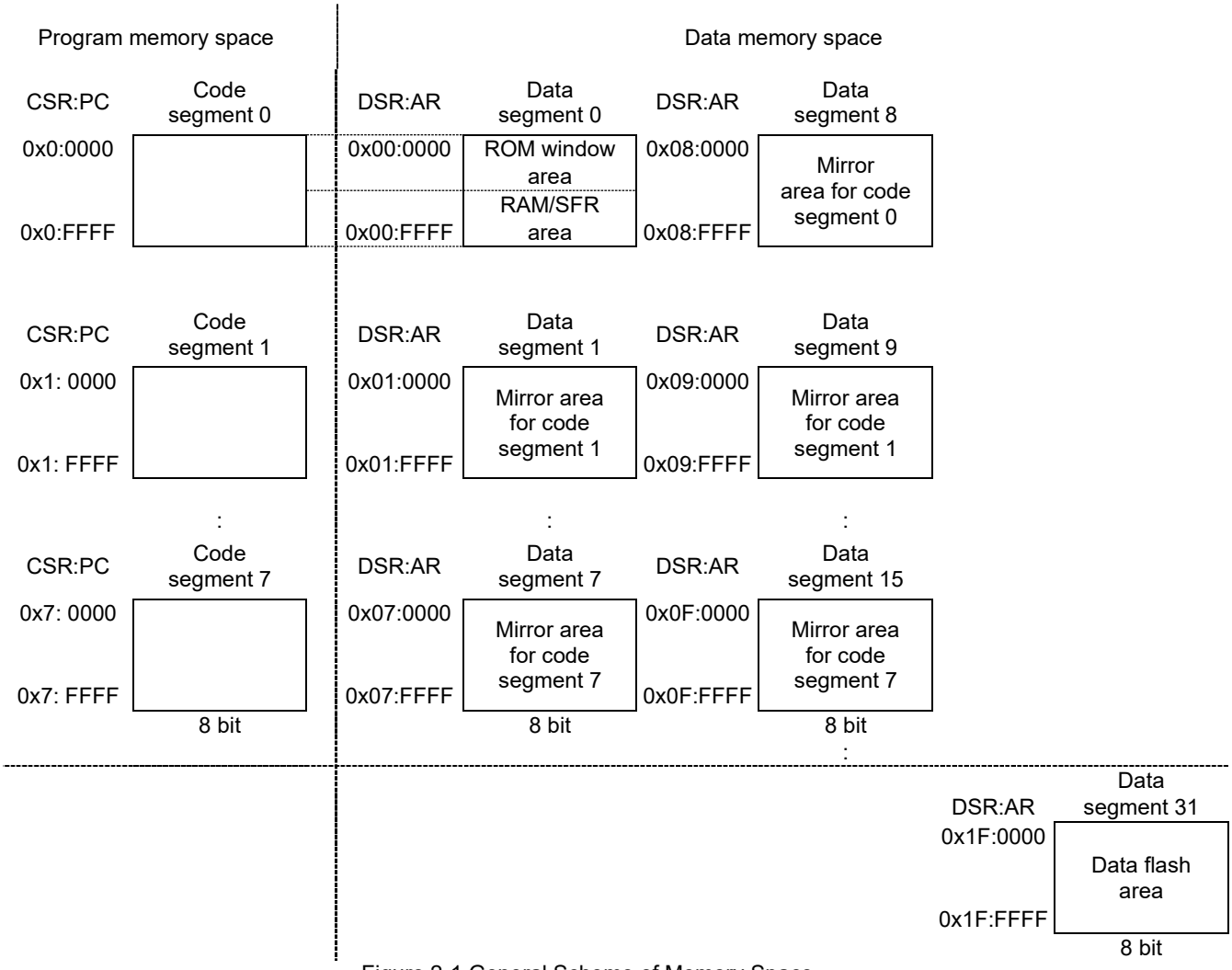


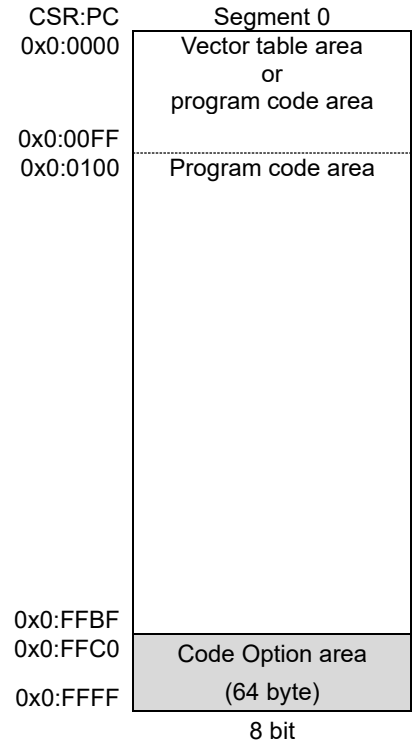
Figure 2-1 General Scheme of Memory Space

2.5 Program Memory Space

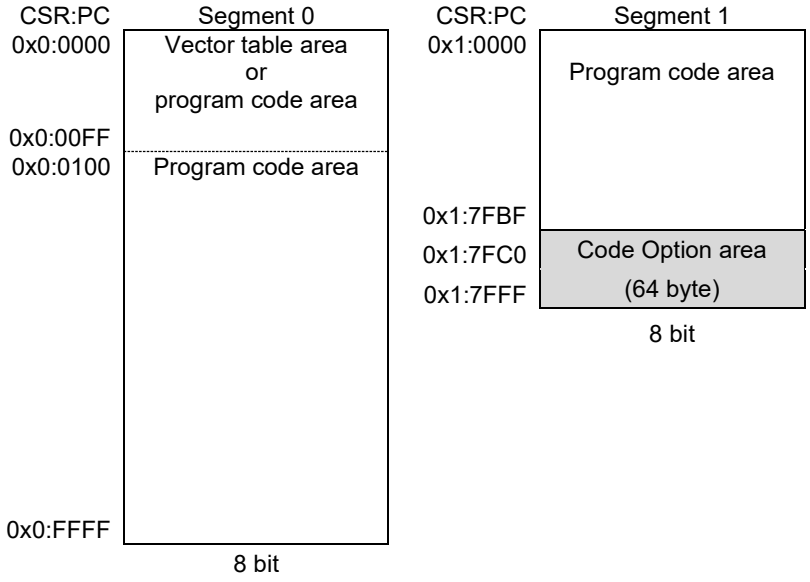
The program memory space is an area to store the program code, vector table, and Code Options.
The program memory space is specified by 20 bits (CSR:PC) consisting of higher 4 bits as code segment register (CSR) and lower 16 bits as program counter (PC).
The vector table area is used as the reset vector, hardware interrupt vector, and software interrupt vector. Unused software interrupt vector area is available as a program code area.
The Code Option area can be used to choose the CPU operation mode, PLL reference frequency, watchdog timer (WDT) operation mode, unused ROM area access reset enabled/disabled, and remapping function enabled/disabled.
The program code, vector table, and Code Option areas can be read from the ROM window area or the mirror area of the data memory space by executing the memory access instruction.
Figures 2-2 show the program memory space configuration of each product of the ML62Q2700 group.

[Note]

- **CSR[3] is unused on the ML62Q2700 group. The data of CSR "0x8 to 0xF" are handled as "0x0 to 0x7".**
- **The Code Option area (64 bytes) is not available for the program code area. For details of Code Option settings, see Chapter 30 "Code Option" and make sure the setting data is correct.**
- **It is recommended to fill unused areas with data "0xFFFF" (BRK instruction) in the program memory space to ensure failsafe using the generation tool of the ROM code data. See its manual for details on how to use. See "nX-U16/100 Core Instruction Manual" for details of the BRK instruction.**
- **Do not read or program unused areas to prevent the CPU works incorrectly.**



ML62Q2702/2712/2722
Size 64 Kbyte
Figure 2-2-1 Configuration of Program Memory Space 1



ML62Q2703/2713/2723
Size 96 Kbyte
Figure 2-2-2 Configuration of Program Memory Space 2

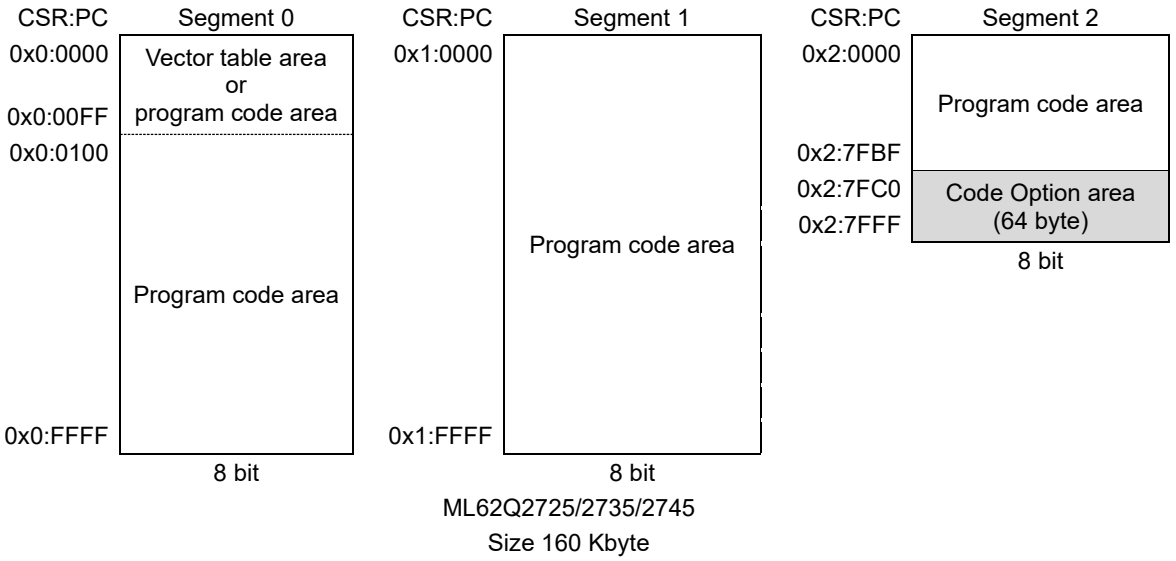


Figure 2-2-3 Configuration of Program Memory Space 3

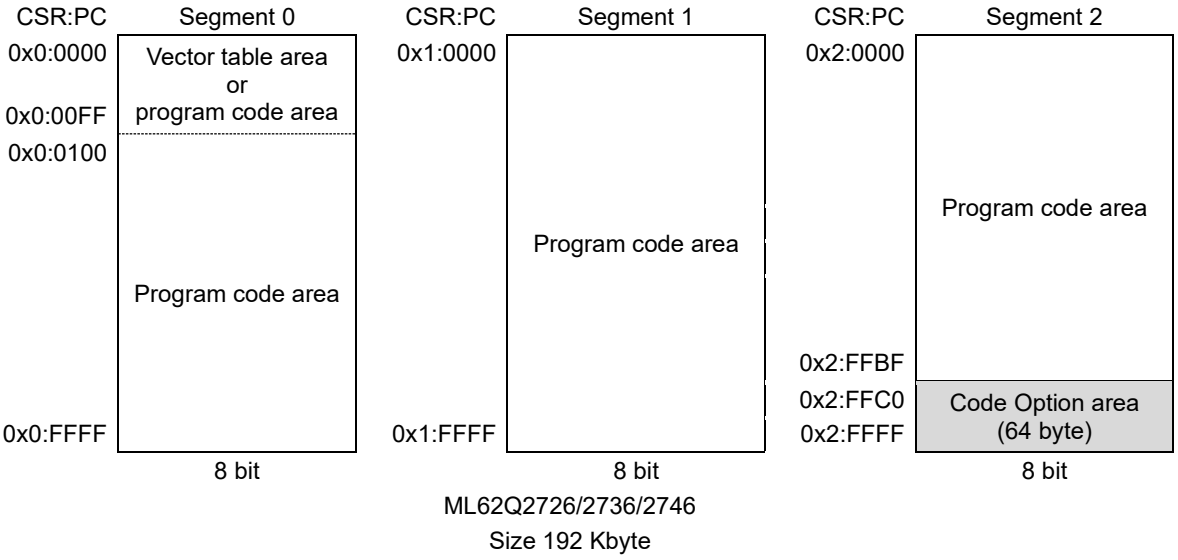


Figure 2-2-4 Configuration of Program Memory Space 4

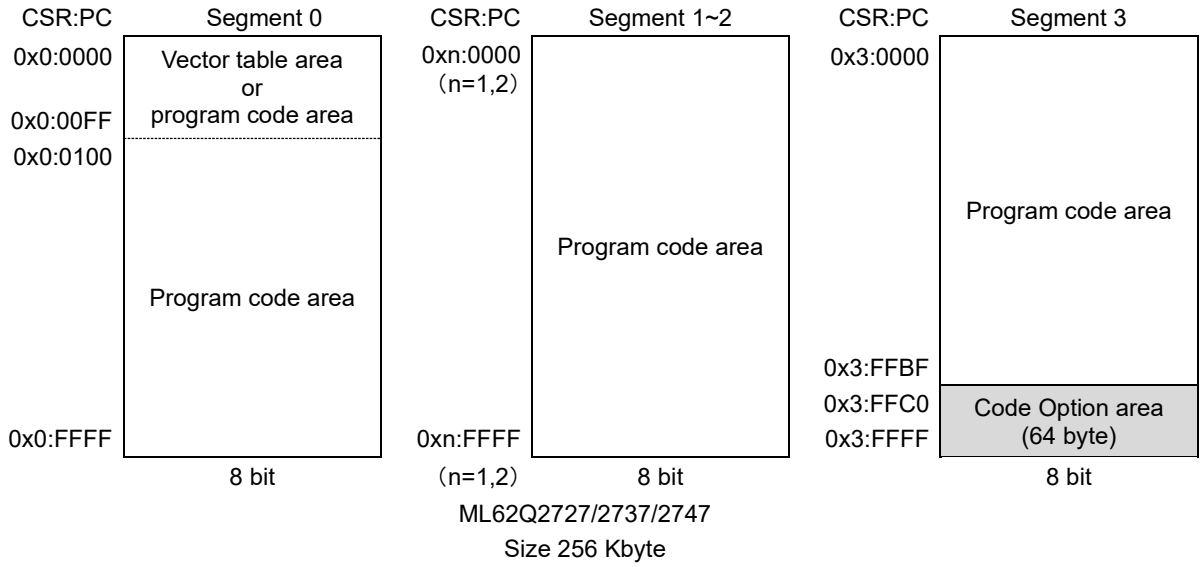


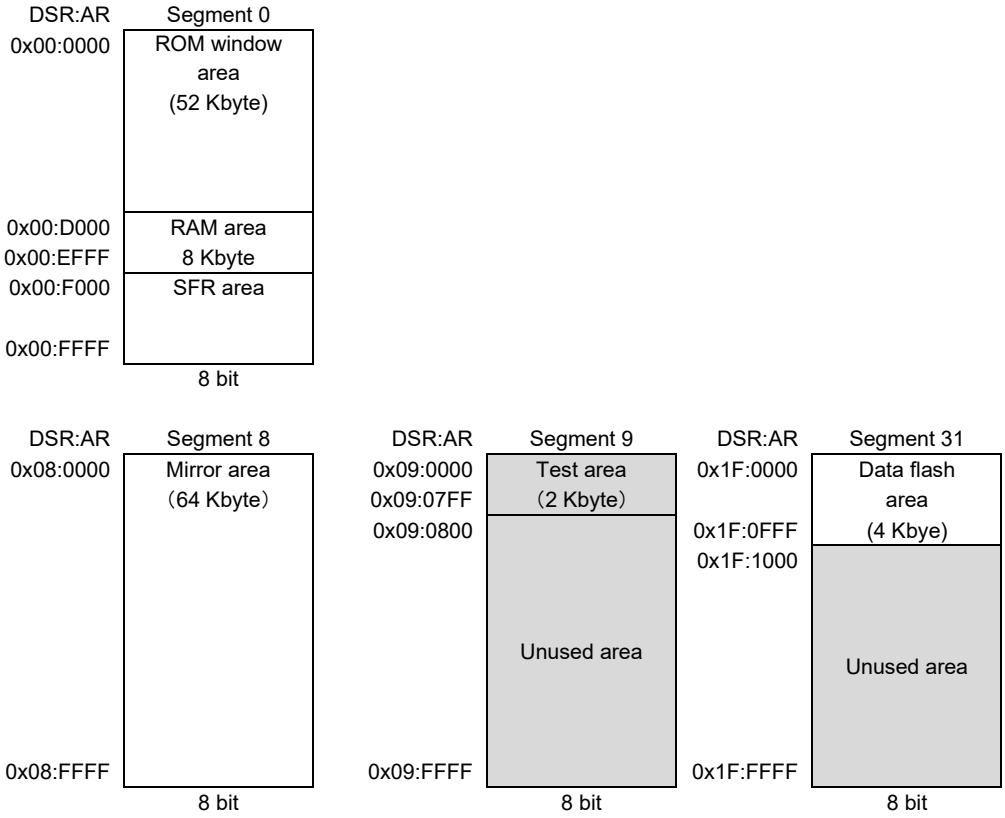
Figure 2-2-5 Configuration of Program Memory Space 5

2.6 Data Memory Space

The data memory space consists of the segment 0 for ROM window area, RAM area, SFR area, segments 1 to 15 for mirror area, test area, and segment 31 for the data flash area.
The data memory stores 8-bit data and is specified by 21 bits consisting of higher 5 bits as the data segment register (DSR) and lower 16 bits as data address (address register: AR) specified by each instruction.
The segment 0 of program memory space and the segment of data memory space are in different space, but the segment 0 of program memory space is readable through the ROM window area of the data memory space.
The segment 1 to 7 are mirror area of segment 1 to 7 in the program memory space. The segment 8 to 15 are mirror area of segment 0 to 7 in the program memory space.
The 2K byte of test area includes device-specific data,
Figures 2-3 show the configuration of the data memory space of ML62Q2700 series products. Other segments not shown in the figures are unused areas.
The read value of the unused area is 0xFF.

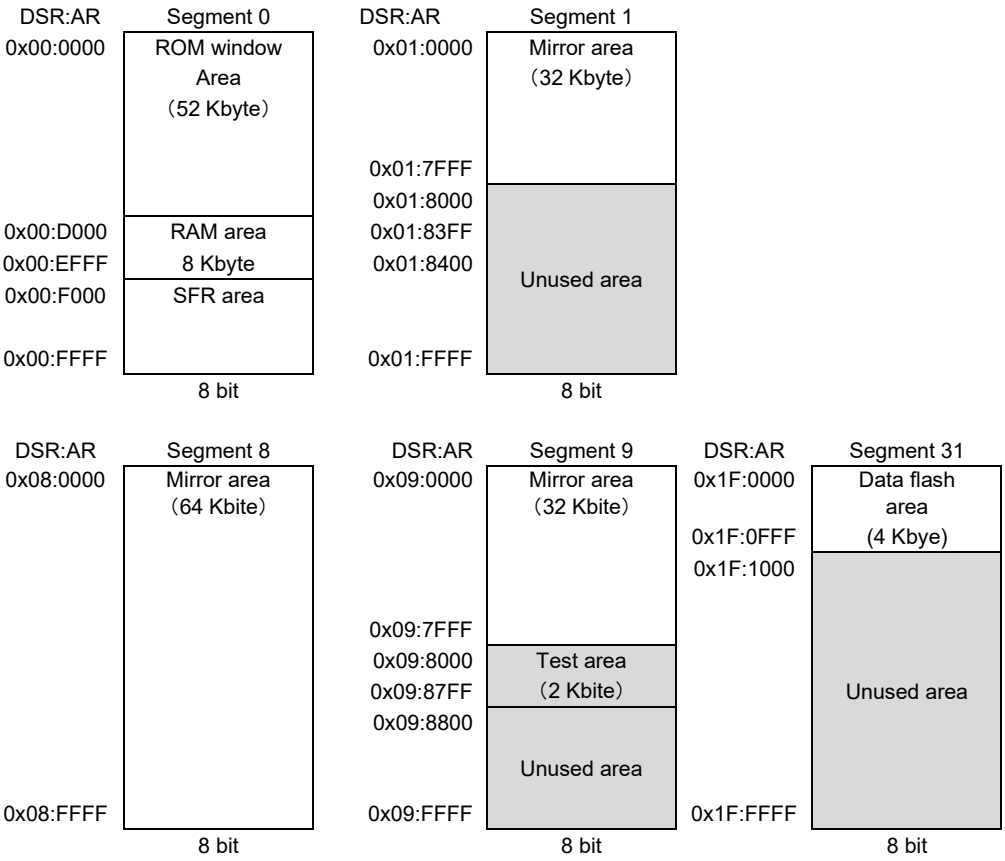
[Note]

- **The contents of the RAM area are undefined at power-on and system reset. Initialize this area by the software.**
- **Do not read/write unused areas to prevent the CPU works incorrectly.**



ML62Q2702 / 2712 / 2722

Figure 2-3-1 Configuration of Data Memory Space 1



ML62Q2703 / 2713 / 2723

Figure 2-3-2 Configuration of Data Memory Space 2

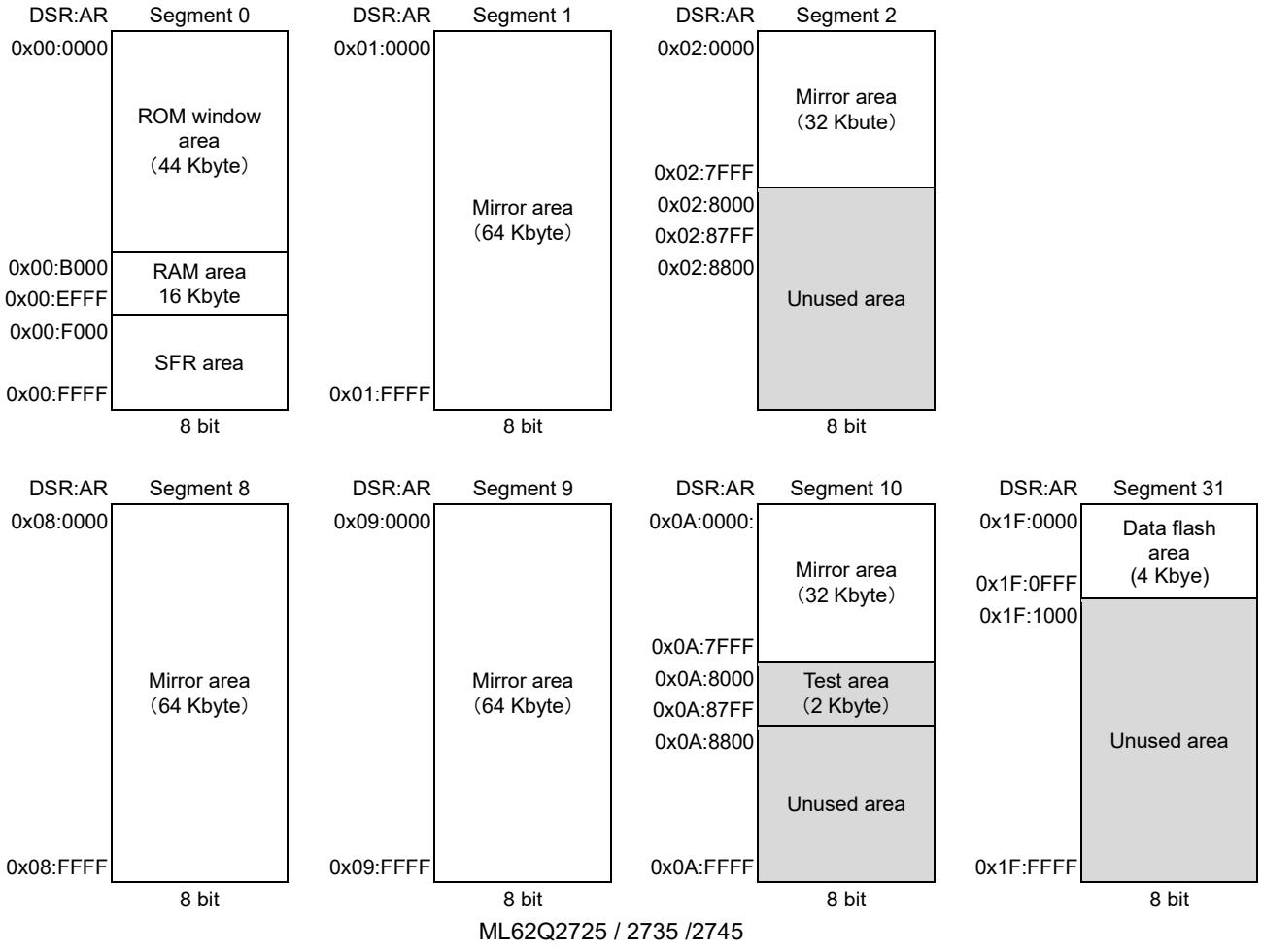


Figure 2-3-3 Configuration of Data Memory Space 3

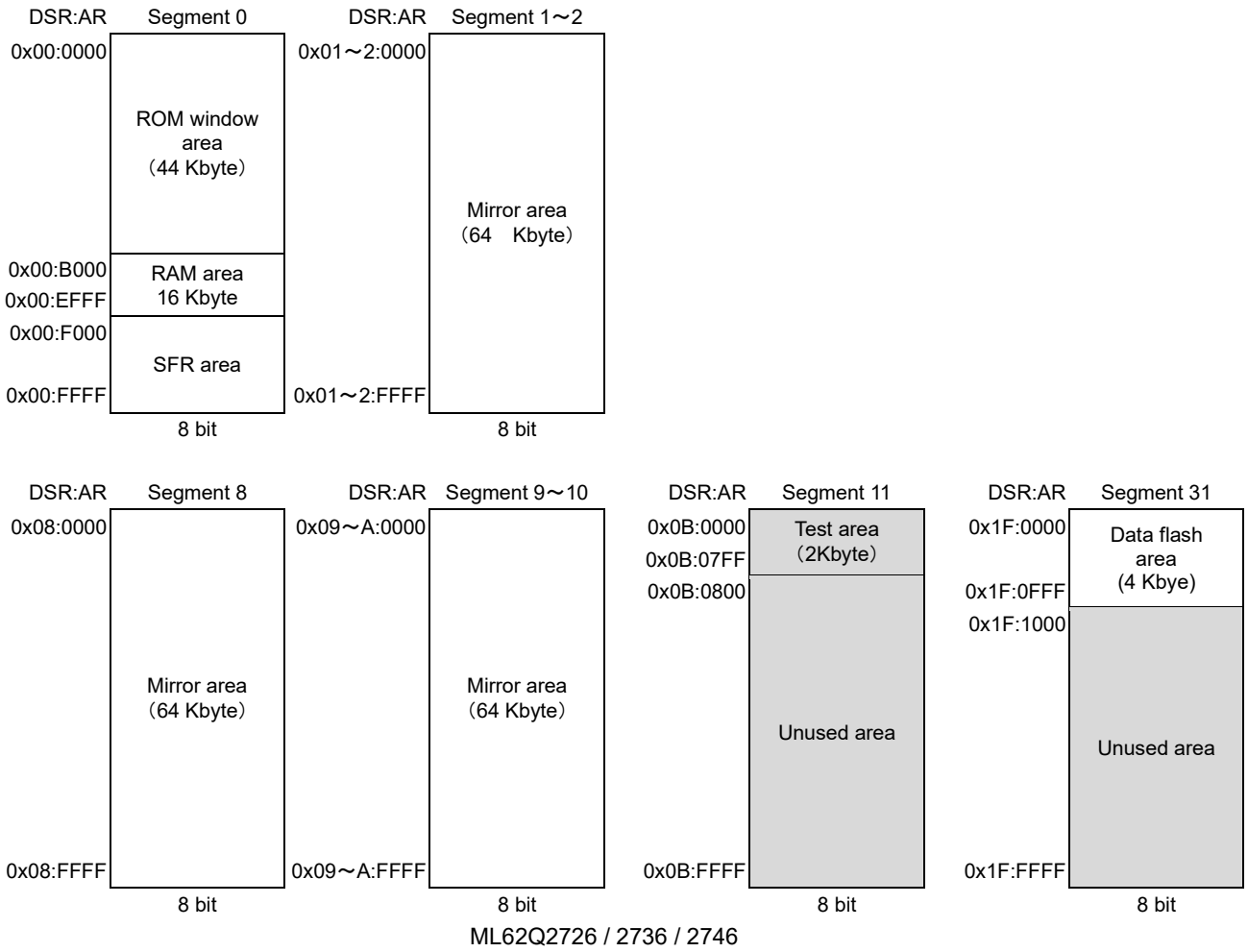


Figure 2-3-4 Configuration of Data Memory Space 4

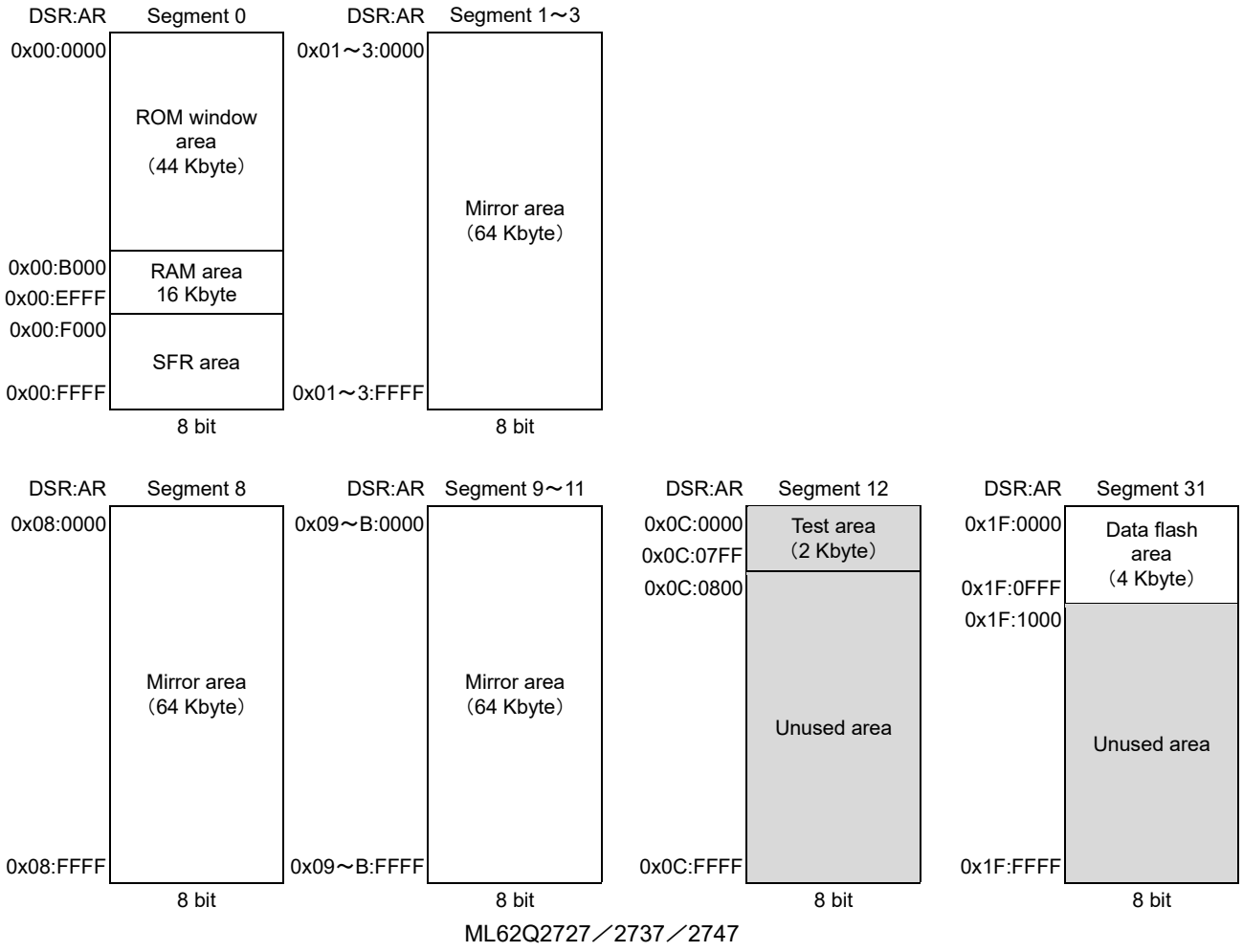


Figure 2-3-5 Configuration of Data Memory Space 5

2.7 Description of Registers

2.7.1 List of Registers

Address	Name	Symbol name		R/W	Size	Initial value
		Byte	Word			
0xF000	Data segment register	DSR	-	R/W	8	0x00
0xF0A0	Flash remap address register	REMAPADD	-	R/W	8	*1
0xF0A4	Reserved	-	-	R/W	8	0x00
0xF0A6	Reserved	-	-	R/W	8	0x00

*1: The initial value depends on Code Option settings. See “30.2.4 Code Options 2 (CODEOP2)” for details of Code Option settings.

2.7.2 Data Segment Register (DSR)

DSR is a SFR to specify a data segment.
See "nX-U16/100 Core Instruction Manual" for details of DSR.

Address: 0xF000(DSR)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								DSR							
Bit	-	-	-	-	-	-	-	-	-	-	-	DSR4	DSR3	DSR2	DSR1	DSR0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 5	-	Reserved bits
4 to 0	DSR4 to DSR0	00000: Data segment 0 (initial value) 00001: Mirror area of code segment 1 00010: Mirror area of code segment 2 00011: Mirror area of code segment 3 00100: Mirror area of code segment 4 00101: Mirror area of code segment 5 00110: Mirror area of code segment 6 00111: Mirror area of code segment 7 01000: Data segment 8 (mirror area of code segment 0) 01001: Data segment 9 (mirror area of code segment 1) 01010: Data segment 10 (mirror area of code segment 2) 01011: Data segment 11 (mirror area of code segment 3) 01100: Data segment 12 (mirror area of code segment 4) 01101: Data segment 13 (mirror area of code segment 5) 01110: Data segment 14 (mirror area of code segment 6) 01111: Data segment 15 (mirror area of code segment 7) :::::::::::: Data segments 16 to 30 (unused areas) 11111: Data segment 31 (data flash area)

2.7.3 Flash Remap Address Register (REMAPADD)

REMAPADD is a SFR to specify the 4 Kbyte area to be remapped.

Address: 0xF0A0 (REMAPADD)
Access: R/W
Access size: 8 bit
Initial value: *1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								REMAPADD							
Bit	-	-	-	-	-	-	-	-	-	RES2	RES1	RES0	REA15	REA14	REA13	REA12
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	*1	*1	*1	*1	*1

For example, when writing "0x1" to RES2-0 and "0xF" to REA15-12, then remapping them, the area of 0xF000-0xFFFF of code segment 1 is remapped with the area of 0x0000-0x0FFF of segment 0.
A CPU reset for break is happened if setting unused area to this register, and a PC error is not happened.

Bit No.	Bit symbol name	Description
7	-	Reserved bit
6 to 4	RES2 to RES0	Bits to set the code segment of the area to remap. The RES2 and RES1 bits are reserved.
3 to 0	REA15 to REA12	Bits to set the higher 4 bits (bit 15 to 12) of the beginning address of the area to be remapped.

*1: The initial value depends on Code Option settings. See “30.2.4 Code Options 2 (CODEOP2)” for details of Code Option settings.

2.7.4 Reserved register 1

This register is reserved. Don't execute writing this.

Address: 0xF0A4
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								rsvd							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rsvd
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	rsvd	Reserved bit

2.7.5 Reserved register 2

This register is reserved. Don't execute writing this.

Address: 0xF0A6
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								rsvd							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	rsvd
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	rsvd	Reserved bit

2.8 Remapping Function

The remapping function replaces the addresses 0x0000 to 0x0FFF (initial boot area) in the program memory space with the specified arbitrary 4 Kbyte area.
Figure 2-4 shows the general scheme of the remapping function.
The program can be started to execute at the area different from the initial boot area using the remapping function, that enables updating(reprograming) the program code area including the initial boot area with the self-programming function.
The remap function and IAP (In-Application Programming) program enable your application to reprogram the firmware.

Two ways are available to start the remap function.

- Software Remap: Start remapping by resetting only the CPU after setting a remap address into the Flash Remap Address Register (REMAPADD).
- Code Option Remap: Start remapping at the system reset, available by setting the Code Option.

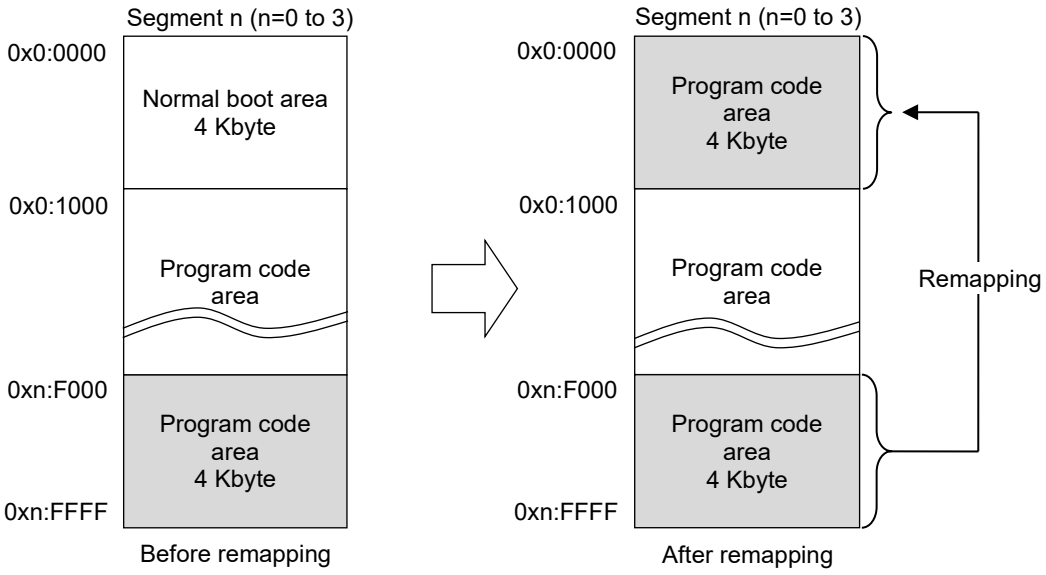


Figure 2-4 Memory Map Before and After Remapping of Program Memory Space

2.8.1 Description of Remapping Function

The remapping function allows the normal boot area of addresses 0x0:0000 to 0x0:0FFF (4 Kbytes) to be replaced (remapped) with the arbitrary 4 Kbyte area set in the REMAPADD register.

To use the remapping function, enable it in advance by writing "0" to the REMAPMD bit of Code Option 0.

When using the remapping function, the vector table area (reset vector, hardware interrupt vector, and software interrupt vector) is also read from the area specified in the REMAPADD register. Prepare the vector table area for areas specified in the REMAPADD register.

After remapping, the remapped areas are read through the data segment 0.
If reading the normal boot area (0x0:0000 to 0x0:0FFF) prior to remapping, read it through the data segment 8 in the data memory space (the mirror area of segment 0).

After remapping, if reprogramming the 4Kbyte area in the normal boot area, set "0x0:0000 to 0x0:0FFF" into the Flash Address Register (FLASHA).

Refer to IAP Sample Program supplied by LAPIS, for how to re-write the user application program on the flash memory using the remapping function.

2.8.2 Software Remap

The remapping function is activated by software setting a value to the REMAPADD register to use the BRK instruction to only reset the CPU.

- Set "0" in advance to the REMAPMD bit of Code Option 0 (see Chapter 30 "Code Option" for details on how to set the Code Option).
- Set the code segment and higher 4 bits of the beginning address of the area to be remapped to the REMAPADD register.
- Set ELEVEL of CPU program status word to "2", then execute the BRK instruction (see "nX-U16/100 Core Instruction Manual" for details of ELEVEL and BRK instruction).
- Only the CPU is initialized and it executes the program from the area specified in the REMAPADD register.

Figure 2-5 below shows an example of the program script of software remapping.

<If the beginning address of the area to be remapped is 0x1:F000>

```
#asm
      mov    r0,    #01fh
      st     r0,    REMAPADD    ; REMAPADD = 0x1F
      mov    psw,   #02h        ; ELEVEL = 2
      nop
      nop
      brk                       ; BRK instruction
#endasm
```

Figure 2-5 Program Script Example of Software Remapping

[Note]
- **If the entire LSI is reset through a system reset, the remapping function is disabled as the REMAPADD register is restored with the initial value.**

2.8.3 Code Option Remap

LSI can always be started from the remapped state by setting CREMAPMD, CRES1~0, and CREA15~CREA12 in code option 2.

- By setting both REMAPMD and CREMAPMD to "0", LSI starts running at the address set in CRES2-0 and CREA15-CREA12.
- After updating the address in the REMAPADD register, the address is not initialized by the CPU reset (BRK instruction) and the remap starts at the updated address. However, the REMAPADD register is initialized by the system reset, LSI starts running at the address specified by the Code Option.

Table 2-7 shows the CPU address at releasing reset of each condition.

Table 2-7 CPU address at releasing reset

Reset	REMAPMD	CREMAPMD	CPU instruction execution start address
CPU reset (BRK instruction)	1	1	0x0000
	1	0	
	0	1	Address set in the REMAPADD register
	0	0	
System reset (Reset other than BRK instruction)	1	1	0x0000
	1	0	
	0	1	
	0	0	Initial data of the REMAPADD register (data set by the Code Options 2)

Chapter 3 Reset Function

3. Reset Function

3.1 General Description

ML62Q2700 group has a function to reset the CPU, peripheral circuits and other hardware due to the causes described in table 3-1.
This chapter describes the system reset mode, reset input pin reset and power-on reset (POR). See reference chapters for other causes of resets. See Table 3-1 for reference for each cause of resets. See Table 3-2 for the availability of resets for each cause.

Table 3-1 Reference for Details of Causes of Resets

Cause	Reference
Reset input pin reset (pin reset)	This chapter
Power-On Reset (POR)	This chapter
Watchdog timer (WDT) overflow reset	Chapter 10 Watchdog Timer
Watchdog timer (WDT) invalid clear reset	Chapter 10 Watchdog Timer
Voltage Level Supervisor reset (VLS0 reset)	Chapter 22 Voltage Level Supervisor
RAM parity error reset	Chapter 29 Safety Function
Unused ROM area access reset	Chapter 29 Safety Function
CPU reset by BRK instruction execution (when ELEVEL is 2 or higher)	"nX-U16/100 Core Instruction Manual"
Individual reset to the peripheral circuits (Block reset)	Chapter 4 Power Management
One-time reset to the all peripheral circuits and port controller (SOFTR reset)	Chapter 4 Power Management

3.1.1 Features

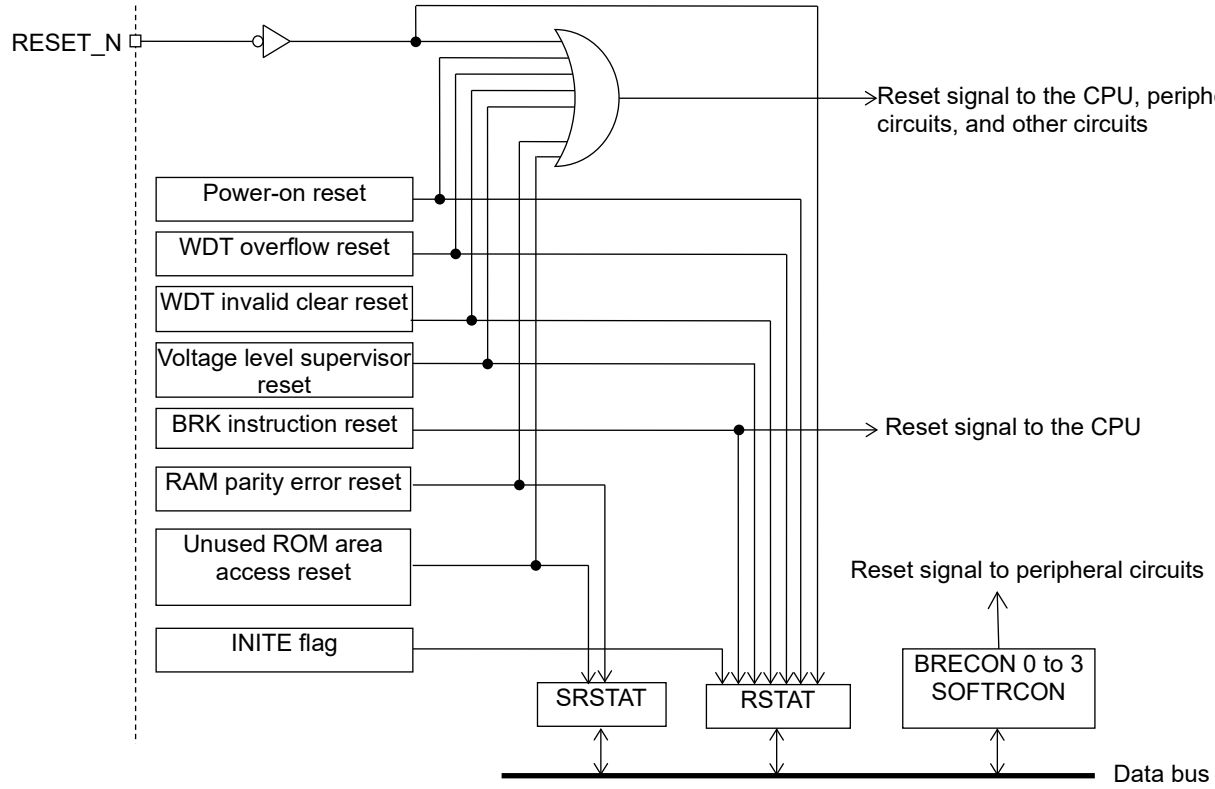
Each reset can uniquely be managed depending on its cause as this function contains following features to identify the cause in an early stage.

- Reset status register (RSTAT) to indicate the cause of the reset.
- Reset status register (SRSTAT) to indicate the cause of the safety function reset.

In addition, ML62Q2700 Series has the INITE flag function to detect abnormal start-up of the LSI.

3.1.2 Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT : Reset status register
SRSTAT : Safety function reset status register
BRECON 0 to 3 : Block reset control register 0 to 3
SOFTRCON : Software reset control register
Other circuits : Power supply circuit, oscillation circuits, start control block, and so on.

Figure 3-1 Configuration of Reset Generation Circuit

3.1.3 List of Pins

Pin name	I/O	Function
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1 List of Registers

Address	Name	Symbol name		R/W	Size	Initial value
		Byte	Word			
0xF058	Reset status register	RSTATL	RSTAT	R/W	8/16	Undefined
0xF059		RSTATH		R/W	8	Undefined
0xF05A	Safety function reset status register	SRSTAT	-	R/W	8	Undefined

3.2.2 Reset Status Register (RSTAT)

RSTAT is a SFR to indicate a factor of occurrence of a reset.
When a reset occurs except power-on reset, only the bit that indicates the cause of the reset being set to "1". Other bits except INITE bit retain their values before occurrence of the reset. When the power-on reset occurs, all bits except POR bit are initialized. After determining the cause of the reset, write "0xFFFF" to RSTAT register to initialize the bits of cause of the reset in preparation for the next identification of the cause of the reset.

Address: 0xF058 (RSTATL/RSTAT), 0xF059 (RSTATH)
Access: R/W
Access size: 8/16 bit
Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	RSTAT															
Byte	RSTATH								RSTATL							
Bit	-	-	-	-	-	-	-	BRKR	INITE	RSTR	-	VLS0R	WDT WR	WDTR	-	POR
R/W	R	R	R	R	R	R	R	R/W	R	R/W	R	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0/1	0	0/1	0	0/1	0/1	0/1	0	0/1

Common description of each bits except bit 7:
It indicates that target reset has occurred. It is initialized to “0” when “1” is written.
0: No target reset occurred. (Initial value)
1: Target reset occurred

Bit No.	Bit symbol name	Description (target reset)
15 to 9	-	Reserved bits
8	BRKR	CPU reset by BRK instruction
7	INITE	A read-only bit to indicate that an abnormality occurred in starting LSI. If this bit is set to "1", restart the LSI by causing a reset to occur with the reset input pin reset, WDT invalid reset, WDT overflow reset or power-on. 0: LSI started-up normally 1: Abnormality occurred in start-up of LSI
6	RSTR	Reset input pin reset
5	-	Reserved bit
4	VLS0R	VLS reset
3	WDTWR	WDT invalid clear reset
2	WDTR	WDT overflow reset
1	-	Reserved bit
0	POR	Power-on reset or command reset of the on-chip debug function.

3.2.3 Safety Function Reset Status Register (SRSTAT)

SRSTAT is a SFR to indicate a factor of occurrence of a safety function reset.
When safety function reset occurs, only the bit that indicates the cause of the reset occurred is set to "1". Other bits retain their values before occurrence of the reset. After identifying the cause of the reset, write "0xFF" to SRSTAT register to initialize it to "0x00" for preparing the next reset.
See Chapter 29 "Safety Function" for details of the safety function.

Address: 0xF05A (SRSTAT)
Access: R/W
Access size: 8 bit
Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SRSTAT							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RPER	FIAR
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1

Common description of each bits:
It indicates that target reset has occurred. It is initialized to “0” when “1” is written.
0: No target reset occurred. (Initial value)
1: Target reset occurred

Bit No.	Bit symbol name	Description (target reset)
7 to 2	-	Reserved bits
1	RPER	RAM parity error reset
0	FIAR	Unused ROM area access reset

3.3 Description of Operation

3.3.1 Operation of Reset Function

Table 3-2 shows the availability of resets for each cause.

Table 3-2 Availability of Resets for Each Cause

Category	Cause	CPU	RAM	Crystal Oscillation Circuit *1	Voltage Level Supervisor	Other Peripheral Circuit	System Circuit *2
System reset	Reset input pin reset (pin reset)	●	-	●	●	●	●
	Power-on reset (POR)	●	-	●	●	●	●
	WDT overflow reset	●	-	●	●	●	●
	WDT invalid clear reset	●	-	●	●	●	●
	Voltage level supervisor reset	●	-	●	-	●	●
	RAM parity error reset	●	-	●	●	●	●
	Unused ROM area access reset	●	-	●	●	●	●
	Command reset in On-chip debug	●	-	-	-	●	●
CPU reset	BRK instruction reset	●	-	-	-	-	-
Peripheral reset	Block reset	-	-	-	-	●	-
	SOFTR reset	-	-	-	-	●	-

●: Reset available -: Reset unavailable
*1: Target SFRs are FLMOD, FBUSTAT register. See Chapter 6 for details.
*2: Power supply circuit, internal oscillation circuit, start control part, code option control part, etc.

[Note]

- **The BRK instruction reset only initializes the CPU if ELEVEL is 2 or higher. Peripheral circuits and other circuits are not initialized. Use the pin reset or the watchdog timer (WDT) reset to reliably initialize the LSI when an abnormality is detected.**
- **Command reset in on-chip debug does not reset to crystal oscillation circuit and VLS parts. Turn off each function by SFR operation with the debugger if necessary. See Chapter 28 for details.**

3.3.2 System Reset Mode

When a reset occurs due to any of the cause of the reset except CPU reset, block reset, or SOFTR reset, the LSI enters system reset mode.
Entering system reset mode takes precedence over all operations and aborts previous processing.
In system reset mode, the following processes are performed.

1. The fundamental hardware for the LSI operation, such as the power supply circuit and oscillation circuit, is initialized. In addition, functions chosen by the code option are configured. INITE bit of the reset status register (RSTAT) is set to "1" if an abnormality occurs during the initialization and configuration.
   See the Chapter 30 "Code Option" for details of the code option.
2. Peripheral circuits and special function registers (SFRs) with their initial values defined are initialized. See Appendix A "Registers" and chapters for respective functions for the initial values of the SFRs.
3. The CPU is initialized.
   - All the registers in the CPU are initialized.
   - The contents of addresses 0x0000, 0x0001 in segment 0 of the program memory are set to the stack pointer (SP).
   - The contents of addresses 0x0002, 0x0003 in segment 0 of the program memory are set to the program counter (PC).
4. Enters the program operation mode when the reset is canceled.

See "nX-U16/100 Core Instruction Manual" for details of registers (SP, PC) in the CPU and the BRK instruction.

[Note]
- **In system reset mode, the contents of data memory (RAM) and SFRs that have an undefined initial value are not initialized. Initialize them by the software.**

3.3.3 Reset Input Pin Reset

Input the "L" level to the reset input pin causes the reset state, as well as causing RSTR bit of the reset status register (RSTAT) to be set to "1". Then, input pin the "H" level to the reset input pin causes the reset to be released and the program begins to run.
To cause a reset to occur, input the "L" level which is longer than the reset activation pulse width (P_{RST}) specified in the datasheet.

3.3.4 Power-on Reset

A power-on reset occurs when the power supply is started or when the power supply voltage (V_{DD}) drops below the power-on reset generation voltage (V_{PORF}) and the power-on reset reaction time (P_{POR}) or more elapses. When a power-on reset occurs, POR bit of the reset status register (RSTAT) is set to "1".
When the power supply voltage (V_{DD}) reaches the power-on reset threshold voltage (V_{PORR}) or above, the reset is released and the CPU starts to run with low-speed clock.
See the data sheet of respective products for power-on reset specifications.

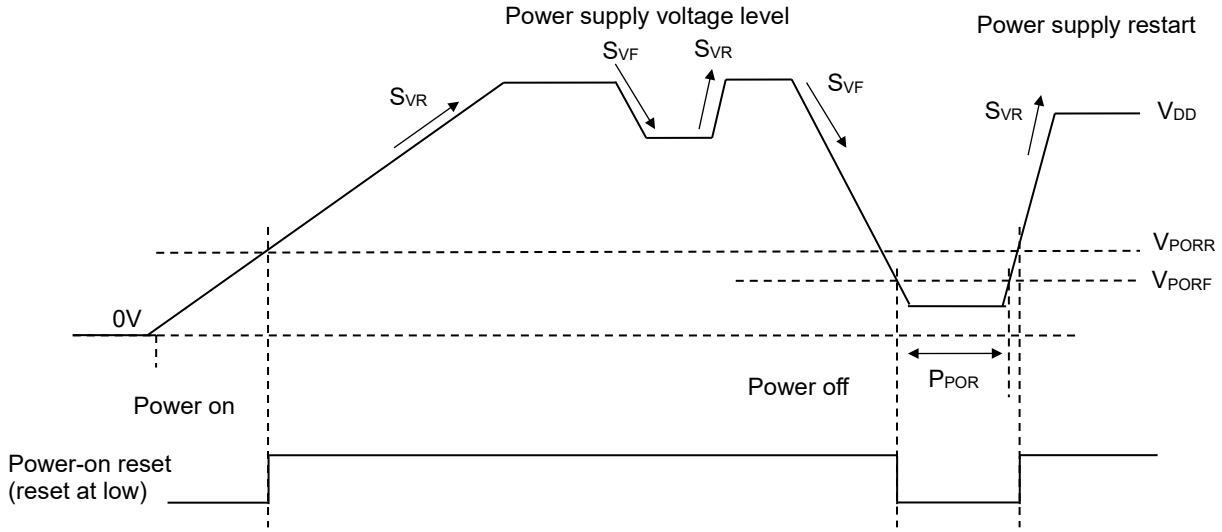


Figure 3-2 Power-on Reset Operation Waveforms

[Note]

- **In case of instantaneous power failure and a pulse shorter than the power-on reset reaction time is asserted to V_{DD}, MCU may not get reset and it may malfunction. In that case, please have preventive measures such as using bypass capacitor to avoid the instantaneous voltage drop or using pin reset to initialize MCU.**

Chapter 4 Power Management

4. Power Management

4.1 General Description

ML62Q2700 group has five power management modes and clock control and reset control for each peripheral circuit function to save the current consumption.

Figure 4-1 shows the general scheme of the regulator.
The regulator generates a voltage (V_{DDL}) for internal logic of constant voltage independent of V_{DD} fluctuations (1.8~5.5V) by using an amplifier.
The V_{DDL} generated by the regulator is supplied to peripheral circuits such as the internal logic circuit, flash memory, RAM, and oscillation circuit.
In order to stabilize the V_{DDL}, connect the VDDL pin to VSS via a capacitor (1 µF).

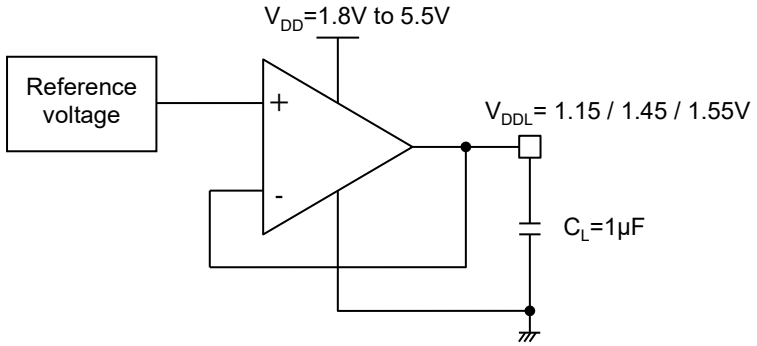


Figure 4-1 General Scheme of Regulator

4.1.1 Features

- 5 standby modes
  - HALT mode : The CPU stops executing instruction, peripheral circuits continue working.
  - HALT-H mode : The CPU stops executing instruction, high-speed clock oscillation stop and peripheral circuits continue working with low-speed clock only. A releasing time from standby mode is min. 60us.
  - HALT-D mode : The CPU stops executing instruction, high-speed clock oscillation stop and peripheral circuits continue working with low-speed clock. The internal logic voltage (V_{DDL}) goes down to reduce the power consumption (RAM data is retained).
  - STOP mode : The CPU stops executing instruction and all internal clocks stop.
  - STOP-D mode : The CPU stops executing instruction and all internal clocks stop. The internal logic voltage (V_{DDL}) goes down to reduce the power consumption (RAM data is retained).
- Stop code acceptor function to limit enter STOP/STOP-D mode.
- Data of RAM and SFR are retained even in all standby modes.
- Block clock control function that stops clock supply for each peripheral circuit and suppresses current consumption.
- Reset is controllable peripheral by peripheral by block reset control registers.
- Block reset control function that resets each peripheral circuit.
- Automatic controlling internal voltage by operating mode and code option.

Mode	V_{DDL}
STOP mode	1.55V / 1.45V
HALT mode	1.55V / 1.45V
HALT-H mode	1.55V / 1.45V
Program run mode	1.55V / 1.45V
HALT-D/STOP-D mode (RAM and SFR content can be retained)	1.15V

4.1.2 Configuration

Figure 4-2 shows the transition diagram of the operating state.
The bit symbols in the figure are assigned to the standby control register (SBYCON).

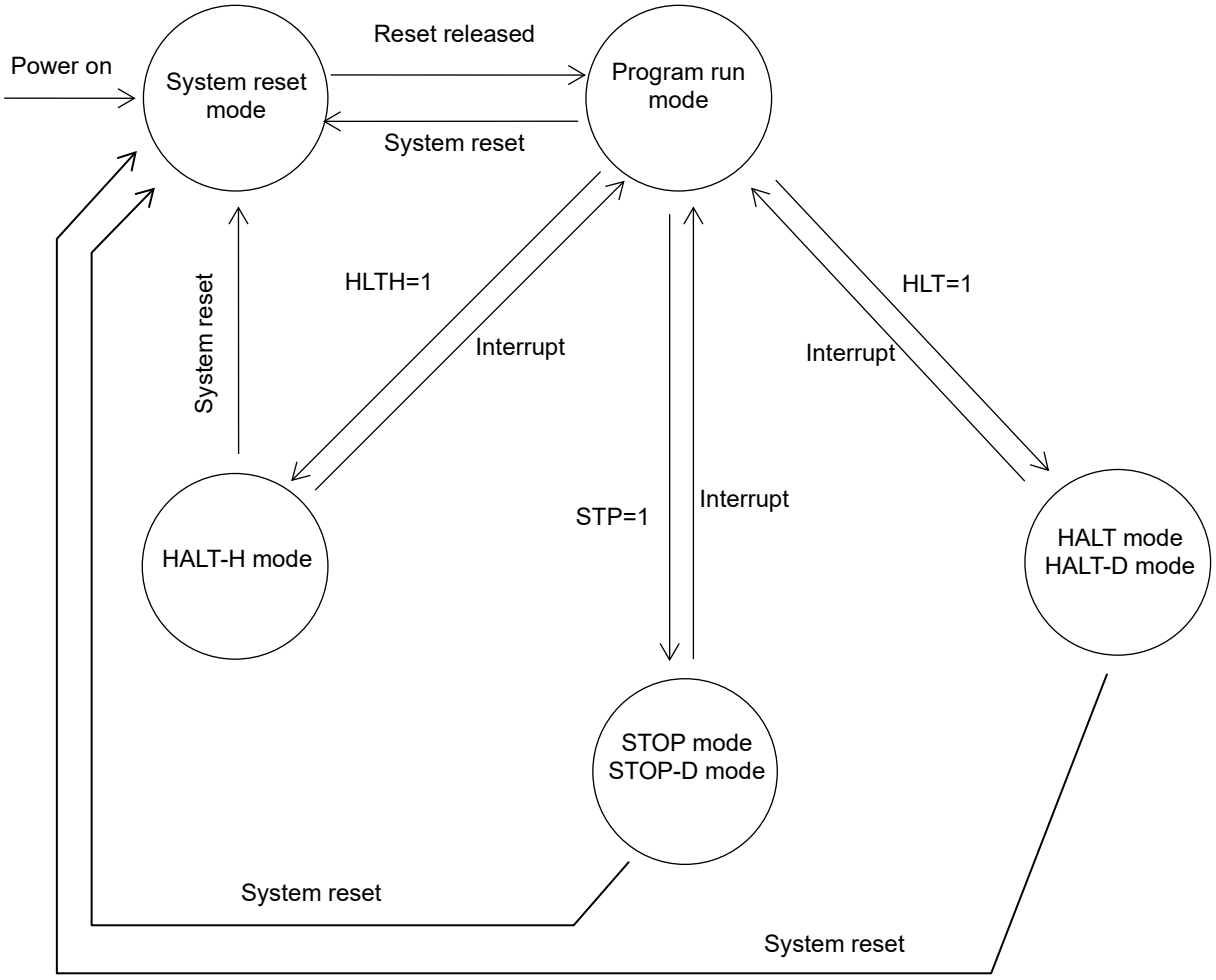


Figure 4-2 Operating State Transition Diagram

Figure 4-3 shows the configuration of the internal power supply.

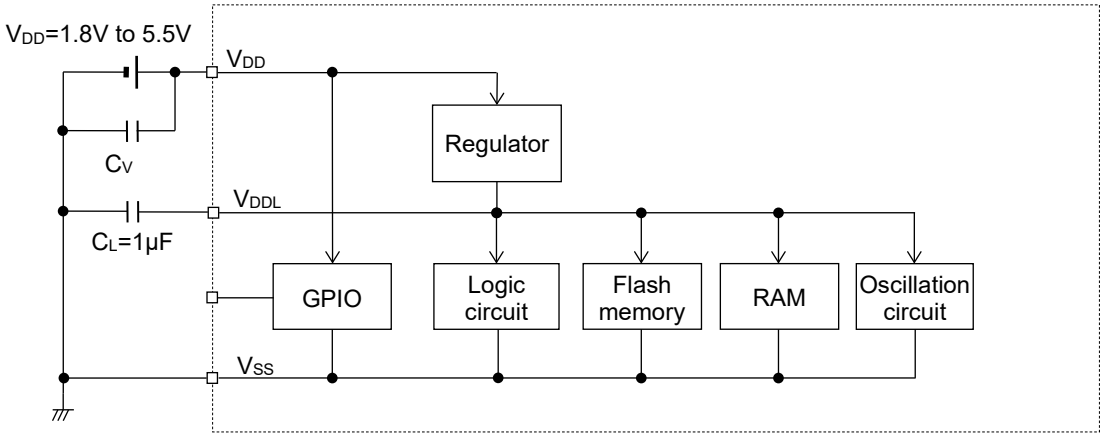


Figure 4-3 Internal Power Supply Configuration

4.1.3 List of Pins

In order to stabilize V_{DDL}, connect the VDDL pin to VSS via a capacitor (1μF).

Pin name	I/O	Function
VDDL	-	Positive power supply for the internal logic circuits (generate internally)

[Note]

- **In order to improve the noise immunity, place the inter-power supply bypass capacitor (C_V) and the internal logic voltage (V_{DDL}) capacitor (C_L : 1 μF) in the vicinity of LSI on the user board using the shortest possible wiring without passing through via holes.**
- **The internal logic voltage (VDDL pin output) is unavailable to use for an external device voltage supply.**

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF018	Stop code acceptor	STPACP	-	W	8	0x00
0xF019	Reserved	-	-	-	-	—
0xF01A	Standby control register	SBYCONL	SBYCON	W	8/16	0x00
0xF01B		SBYCONH		R/W	8	0x00
0xF01C	Standby prohibition flag register	SBYEFLG	-	R	8	0x00
0xF01D	Reserved	-	-	-	-	—
0xF05C	Software reset acceptor	SOFTRACP	-	W	8	0x00
0xF05D	Reserved	-	-	-	-	—
0xF05E	Software reset control register	SOFTRCON	-	R/W	8	0x00
0xF05F	Reserved	-	-	-	-	—
0xF070	Block clock control register 0	BCKCON0L	BCKCON0	R/W	8/16	0x7F
0xF071		BCKCON0H		R/W	8	0x01
0xF072	Block clock control register 1	BCKCON1L	BCKCON1	R/W	8/16	0xFF
0xF073		BCKCON1H		R/W	8	0x13
0xF074	Block clock control register 2	BCKCON2L	BCKCON2	R/W	8/16	0x7F
0xF075		BCKCON2H		R/W	8	0x18
0xF076	Block clock control register 3	BCKCON3L	BCKCON3	R/W	8/16	0x05
0xF077		BCKCON3H		R/W	8	0x77
0xF078	Block reset control register 0	BRECON0L	BRECON0	R/W	8/16	0x7F
0xF079		BRECON0H		R/W	8	0x01
0xF07A	Block reset control register 1	BRECON1L	BRECON1	R/W	8/16	0xFF
0xF07B		BRECON1H		R/W	8	0x13
0xF07C	Block reset control register 2	BRECON2L	BRECON2	R/W	8/16	0x7F
0xF07D		BRECON2H		R/W	8	0x18
0xF07E	Block reset control register 3	BRECON3L	BRECON3	R/W	8/16	0x05
0xF07F		BRECON3H		R/W	8	0x77

Table 4-1 shows Availability list of the SFR bit symbols.

Table 4-1 Availability of the SFR bit symbols in BCLCONn register and BRECONn register

Control register / bit				Available/Unavailable	
Word symbol	Bit symbol	Word symbol	Bit symbol	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702	ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725
BCKCON0	DCKTM0	BRECON0	RSETM0	●	●
	DCKTM1		RSETM1	●	●
	DCKTM2		RSETM2	●	●
	DCKTM3		RSETM3	●	●
	DCKTM4		RSETM4	●	●
	DCKTM5		RSETM5	-	●
	DCKTM6		RSETM6	-	●
	DCKTMX		RSETMX	●	●
BCKCON1	DCKFTM0	BRECON1	RSEFTM0	●	●
	DCKFTM1		RSEFTM1	●	●
	DCKFTM2		RSEFTM2	●	●
	DCKFTM3		RSEFTM3	●	●
	DCKFTM4		RSEFTM4	●	●
	DCKFTM5		RSEFTM5	●	●
	DCKFTM6		RSEFTM6	-	●
	DCKFTM7		RSEFTM7	-	●
	DCKI2CM0		RSEI2CM0	●	●
	DCKI2CM1		RSEI2CM1	●	●
	DCKI2CU0		RSEI2CU0	●	●

●:Available -:Not available

Control register / bit				Available/Unavailable	
Word symbol	Bit symbol	Word symbol	Bit symbol	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702	ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725
BCKCON2	DCKSIOF0	BRECON2	RSESIOF0	●	●
	DCKSIO0		RSESIO0	●	●
	DCKSIO1		RSESIO1	●	●
	DCKSIO2		RSESIO2	-	●
	DCKUA0		RSEUA0	●	●
	DCKUA1		RSEUA1	●	●
	DCKUA2		RSEUA2	-	●
	DCKCRC		RSECRC	●	●
BCKCON3	DCKVC0	BRECON3	RSEVC0	●	●
	DCKACC		RSEACC	●	●
	DCKSAD		RSESAD	●	●
	DCKLCD		RSELCD	●	●
	DCKESIO0		RSEESIO0	-	●
	DCKESIO1		RSEESIO1	-	●
	DCKESIO2		RSEESIO2	-	●
	DCKEUA0		RSEEUA0	-	●
	DCKEUA1		RSEEUA1	-	●
	DCKEUA2		RSEEUA2	-	●

●:Available -:Not available

4.2.2 Stop Code Acceptor (STPACP)

STPACP is a write-only SFR to permits to enter to STOP/STOP-D mode. This returns "0x00" for reading.

Address : 0xF018 (STPACP)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								STPACP							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

How to enter the STOP/STOP-D mode:

Procedure	How to specify the registers	Description
1	Write "0x5n" and "0xAn" (n=arbitrary in 0-F) in sequence into STPACP register.	Enables to enter the STOP/STOP-D mode only once.
2	Set STP bit of SBYCON register to"1".	STP=1 : Enter the STOP/STOP-D mode

Any other instructions can be executed between the instruction that writes "0x5n" to STPACP and the instruction that writes "0xAn". However, if write data other than "0xAn" after writing "0x5n", the procedure gets invalid, so need write "0x5n" again.

[Note]

- **Writing to the stop code acceptor is invalid on the condition both interrupts enable bits and interrupt request bits are "1", it will not get enabled for entering to the STOP/STOP-D mode.**

4.2.3 Standby Control Register (SBYCON)

SBYCON is a write-only SFR to select the standby mode.
This returns "0x0000" for reading.

Address : 0xF01A(SBYCONL/SBYCON), 0xF01B(SBYCONH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SBYCON															
Byte	SBYCONH								SBYCONL							
Bit	-	-	-	-	-	-	DPM	-	-	-	-	-	-	HLTH	STP	HLT
R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

When the WDT interrupt or an interrupt enabled in the interrupt enable registers (IE0 to IE7) is generated, each standby mode gets canceled and returns to program run mode.

Bit No.	Bit symbol name	Description
15 to 10	-	Reserved bits
9	DPM	Sets the deep power-down (VDDL degradation) mode. During the DPM bit is set to "1", setting the HLT bit to "1" enter HALT-D mode, and setting STP bit to "1" enter STOP-D mode. When the HLTH bit is set to "1", the DPM setting is invalid. DPM bit and HLT/STP bit can be set simultaneously. 0 : Disabled (Initial value) 1 : Enabled
8 to 3	-	Reserved bits
2	HLTH	Stop forcibly the high-speed oscillation and change the operating state into the HALT-H mode. Its wake-up time is shorter than HALT mode. An entering this mode is available if SYSCLK is high speed clock. When using HALT-H mode, set FHRDWN bit in the high-speed clock wake up time setting register too. See "6.3.2.3 HALT-H mode" for wake-up time from the HALT-H mode.
1	STP	Change the operating state into the STOP/STOP-D mode. When "1" is written in the STP bit after entering the STOP/STOP-D mode is allowed by using STPACP, the operating state enters the STOP/STOP-D mode.
0	HLT	Change the operating state into the HALT mode.

[Note]

- **The operating state does not enter the standby mode under some conditions. See “4.3.2.6 Note of entering to the standby mode” for detail conditions.**
- **When an interrupt enabled in the interrupt enable registers (IE0 to IE7) is generated on the condition of MIE flag of the program status word (PSW) is "0", it cancels the standby mode only and the CPU does not go to the interrupt routine. For more details about MIE flag, see "nX-U16/100 Core Instruction Manual".**
- **Insert two NOP instructions in the next to the instruction of that sets HLT, STP, HLTH and STPD bit to "1". The operation without the two NOP instructions is not guaranteed.**

4.2.4 Standby Prohibition Flag Register (SBYEFLG)

SBYEFLG is a read-only SFR to indicate availability of entering to standby mode.
See “4.3.2.6 Note of entering to the standby mode” for condition that each bit becomes to “1”

Address : 0xF01C (SBYEFLG)
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SBYEFLG							
Bit	-	-	-	-	-	-	-	-	-	-	-	FSTPD	FHLTD	FHLTH	FSTP	FHLT
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is a flag of an entering to a target standby mode
0: Available (Initial value)
1: Prohibited

Bit No.	Bit symbol name	Description
7 to 5	-	Reserved bits
4	FSTPD	STOP-D mode
3	FHLTD	HALT-D mode
2	FHLTH	HALT-H mode
1	FSTP	STOP mode
0	FHLT	HALT mode

4.2.5 Software Reset Acceptor (SOFTRACP)

SOFTRACP is a write-only SFR to enable writing to the SOFTCON register. This returns "0x00" for reading.

Address : 0xF05C (SOFTRACP)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SOFTRACP							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Peripheral circuit collective reset procedure :

Procedure	How to specify the registers	Description
1	Write "0x3n" and "0xCn" (n=arbitrary in 0-F) in sequence into the SOFTRACP register.	Enables SOFTR reset only once.
2	Set SOFTR bit of the SOFTRCON register to "1".	SOFTR reset state.

Any other instructions can be executed between the instruction that writes "0x3n" to SOFTRACP and the instruction that writes "0xCn". However, if write data other than "0xCn" after writing "0x3n", the procedure gets invalid, so need write "0x3n" again.

4.2.6 Software Reset Control Register (SOFTRCON)

SOFTRCON is a SFR to reset collectively the all peripheral circuits belong to the BRECONn register (n=0 to 3) and general ports.

Address : 0xF05E (SOFTRCON)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SOFTRCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SOFTR
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	SOFTR	Reset all peripherals and general-purpose ports in the BRECONn register at once. Execute the reset according to the procedure in "4.2.5 Soft Reset Acceptor (SOFTRACP)". When the reset is complete, SOFTR bit will automatically become "0". When setting again for the peripheral circuit to be reset, confirm that the reset is complete before setting.

[Note]

- **Do not enter the standby mode when the SOFTR bit is "1". Ensure the SOFTR bit is "0" before entering the standby mode.**

4.2.7 Block Clock Control Register 0 (BCKCON0)

BCKCON0 is a SFR to control supplying the system clock, high-speed clock, and low-speed clock to the peripheral circuits.
Stopping the clock supply for unused peripheral circuits reduce power consumption.

Address : 0xF070 (BCKCON0L/BCKCON0), 0xF071 (BCKCON0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x017F

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BCKCON0															
Byte	BCKCON0H								BCKCON0L							
Bit	-	-	-	-	-	-	-	DCKTMX	-	DCKTM6	DCKTM5	DCKTM4	DCKTM3	DCKTM2	DCKTM1	DCKTM0
R/W	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1

Common description of each bits :
It is configured supplying clocks to a target peripheral circuit.
0: Supply clock to a target peripheral circuit
1: Stop clock to a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15 to 9	-	Reserved bits
8	DCKTMX	16-bit timer X
7	-	Reserved bit
6	DCKTM6	16-bit timer 6
5	DCKTM5	16-bit timer 5
4	DCKTM4	16-bit timer 4
3	DCKTM3	16-bit timer 3
2	DCKTM2	16-bit timer 2
1	DCKTM1	16-bit timer 1
0	DCKTM0	16-bit timer 0

4.2.8 Block Clock Control Register 1 (BCKCON1)

BCKCON1 is a SFR to control supplying the system clock, high-speed clock, and low-speed clock to the peripheral circuits.
Stopping the clock supply for unused peripheral circuits reduce power consumption.

Address : 0xF072 (BCKCON1L/BCKCON1), 0xF073 (BCKCON1H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x1103

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BCKCON1															
Byte	BCKCON1H								BCKCON1L							
Bit	-	-	-	DCKI 2CU0	-	-	DCKI 2CM1	DCKI 2CM0	DCKF TM7	DCKF TM6	DCKF TM5	DCKF TM4	DCKF TM3	DCKF TM2	DCKF TM1	DCKF TM0
R/W	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1

Common description of each bits :
It is configured supplying clocks to a target peripheral circuit.
0: Supplied clock to a target peripheral circuit
1: Stop clock to a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15 to 13	-	Reserved bits
12	DCKI2CU0	I^2C Bus Unit 0
11,10	-	Reserved bits
9	DCKI2CM1	I^2C Bus Master 1
8	DCKI2CM0	I^2C Bus Master 0
7	DCKFTM7	Functional Timer 7
6	DCKFTM6	Functional Timer 6
5	DCKFTM5	Functional Timer 5
4	DCKFTM4	Functional Timer 4
3	DCKFTM3	Functional Timer 3
2	DCKFTM2	Functional Timer 2
1	DCKFTM1	Functional Timer 1
0	DCKFTM0	Functional Timer 0

4.2.9 Block Clock Control Register 2 (BCKCON2)

BCKCON2 is a SFR to control supplying the system clock, high-speed clock, and low-speed clock to the peripheral circuits.
Stopping the clock supply for unused peripheral circuits reduce power consumption.

Address : 0xF074 (BCKCON2L/BCKCON2), 0xF075 (BCKCON2H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0873

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BCKCON2															
Byte	BCKCON2H								BCKCON2L							
Bit	-	-	DCKACC	DCKVC0	DCKCRC	-	-	-	-	DCKUA2	DCKUA1	DCKUA0	DCKSIO2	DCKSIO1	DCKSIO0	DCKSIOF0
R/W	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1

Common description of each bits :
It is configured supplying clocks to a target peripheral circuit.
0: Supplied clock to a target peripheral circuit
1: Stop clock to a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15,14	-	Reserved bits
13	DCKACC	Multiplier/Divider An initial value of this bit is ”0”.
12	DCKVC0	Audio playback function
11	DCKCRC	CRC Calculator
10～7	-	Reserved bits
6	DCKUA2	UART 2
5	DCKUA1	UART 1
4	DCKUA0	UART 0
3	DCKSIO2	SSIO 2
2	DCKSIO1	SSIO 1
1	DCKSIO0	SSIO 0
0	DCKSIOF0	SSIOF0

[Note]
- **Set DCKACC bit to "0" when the multiplication/division library "muldivu8.lib" in Development Support tools is specified. See a manual of the multiplication/division library for how to use.**

4.2.10 Block Clock Control Register 3 (BCKCON3)

BCKCON3 is a SFR to control supplying the system clock, high-speed clock, and low-speed clock to the peripheral circuits.
Stopping the clock supply for unused peripheral circuits reduce power consumption.

Address : 0xF076 (BCKCON3L/BCKCON3), 0xF077 (BCKCON3H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x7705

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BCKCON3															
Byte	BCKCON3H								BCKCON3L							
Bit	-	DCKEUA2	DCKEUA1	DCKEUA0	-	DCKESIO2	DCKESIO1	DCKESIO0	-	-	-	-	-	DCKLCD	-	DCKSAD
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R	R/W
Initial value	0	1	1	1	0	1	1	1	0	0	0	0	0	1	0	1

Common description of each bits :
It is configured supplying clocks to a target peripheral circuit.
0: Supplied clock to a target peripheral circuit
1: Stop clock to a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15	-	Reserved bits
14	DCKEUA2	Extended UART2
13	DCKEUA1	Extended UART1
12	DCKEUA0	Extended UART0
11	-	Reserved bit
10	DCKESIO2	Extended SSIO2
9	DCKESIO1	Extended SSIO1
8	DCKESIO0	Extended SSIO0
7 to 3	-	Reserved bit
2	DCKLCD	LCD Driver
1	-	Reserved bit
0	DCKSAD	SA-ADC

4.2.11 Block Reset Control Register 0 (BRECON0)

BRECON0 is a SFR to control resetting the peripheral circuits.

Address : 0xF078(BRECON0L/BRECON0), 0xF079(BRECON0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x017F

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BRECON0															
Byte	BRECON0H								BRECON0L							
Bit	-	-	-	-	-	-	-	RSETMX	-	RSETM6	RSETM5	RSETM4	RSETM3	RSETM2	RSETM1	RSETM0
R/W	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1

Common description of each bits :
It is configured resetting to a target peripheral circuit.
0: Cancel reset to a target peripheral circuit
1: Resetting a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15 to 9	-	Reserved bits
8	RSETMX	16-bit timer X
7	-	Reserved bit
6	RSETM6	16-bit timer 6
5	RSETM5	16-bit timer 5
4	RSETM4	16-bit timer 4
3	RSETM3	16-bit timer 3
2	RSETM2	16-bit timer 2
1	RSETM1	16-bit timer 1
0	RSETM0	16-bit timer 0

4.2.12 Block Reset Control Register 1 (BRECON1)

BRECON1 is a SFR to control resetting the peripheral circuits corresponding to each bit.

Address : 0xF07A (BRECON1L/BRECON1), 0xF07B (BRECON1H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x13FF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BRECON1															
Byte	BRECON1H								BRECON1L							
Bit	-	-	-	RSEI 2CU0	-	-	RSEI 2CM1	RSEI 2CM0	RSEF TM7	RSEF TM6	RSEF TM5	RSEF TM4	RSEF TM3	RSEF TM2	RSEF TM1	RSEF TM0
R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	1

Common description of each bits :
It is configured resetting to a target peripheral circuit.
0: Cancel reset to a target peripheral circuit
1: Resetting reset a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15 to 13	-	Reserved bits
12	RSEI2CU0	I^2C Bus Unit 0
11,10	-	Reserved bits
9	RSEI2CM1	I^2C Bus Master 1
8	RSEI2CM0	I^2C Bus Master 0
7	RSEFTM7	Functional Timer 7
6	RSEFTM6	Functional Timer 6
5	RSEFTM5	Functional Timer 5
4	RSEFTM4	Functional Timer 4
3	RSEFTM3	Functional Timer 3
2	RSEFTM2	Functional Timer 2
1	RSEFTM1	Functional Timer 1
0	RSEFTM0	Functional Timer 0

4.2.13 Block Reset Control Register 2 (BRECON2)

BRECON2 is a SFR to control resetting the peripheral circuits corresponding to each bit.

Address : 0xF07C(BRECON2L/BRECON2), 0xF07D(BRECON2H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x187F

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BRECON2															
Byte	BRECON2H								BRECON2L							
Bit	-	-	RSEACC	RSEVC0	RSECRC	-	-	-	-	RSEUA2	RSEUA1	RSEUA0	RSESIO2	RSESIO1	RSESIO0	RSESIOF0
R/W	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1

Common description of each bits :
It is configured resetting to a target peripheral circuit.
0: Cancel reset a target peripheral circuit
1: Resetting a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15 to 14	-	Reserved bits
13	RSEACC	Multiplier/Divider An initial value of this bit is ”0”.
12	RSEVC0	Audio Playback function
11	RSECRC	CRC Calculator
10 to 7	-	Reserved bits
6	RSEUA2	UART 2
5	RSEUA1	UART 1
4	RSEUA0	UART 0
3	RSESIO2	SSIO 2
2	RSESIO1	SSIO 1
1	RSESIO0	SSIO 0
0	RSESIOF0	SSIOF0

[Note]
- **Set RSEACC bit to "0" when the multiplication/division library "muldivu8.lib" in Development Support tools is specified. See a manual of the multiplication/division library for how to use.**

4.2.14 Block Reset Control Register 3 (BRECON3)

BRECON3 is a SFR to control resetting the peripheral circuits corresponding to each bit.

Address : 0xF07E(BRECON3L/BRECON3), 0xF07F(BRECON3H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x7705

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BRECON3															
Byte	BRECON3H								BRECON3L							
Bit	-	RSEEUA2	RSEEUA1	RSEEUA0	—	RSEESIO2	RSEESIO1	RSEESIO0	-	-	-	-	-	RSELCD	-	RSESAD
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R	R/W
Initial value	0	1	1	1	0	1	1	1	0	0	0	0	0	1	0	1

Common description of each bits :
It is configured resetting to a target peripheral circuit.
0: Cancel reset a target peripheral circuit
1: Resetting reset a target peripheral circuit (Initial value)

Bit No.	Bit symbol name	Description (target peripheral)
15	-	Reserved bits
14	RSEEUA2	Extended UART2
13	RSEEUA1	Extended UART1
12	RSEEUA0	Extended UART0
11	-	Reserved bit
10	RSEESIO2	Extended SSIOF2
9	RSEESIO1	Extended SSIOF1
8	RSEESIO0	Extended SSIOF0
7 to 3	-	Reserved bits
2	RSELCD	LCD Driver
1	-	Reserved bit
0	RSESAD	SA-ADC

4.3 Description of Operation

4.3.1 Program Operating Mode

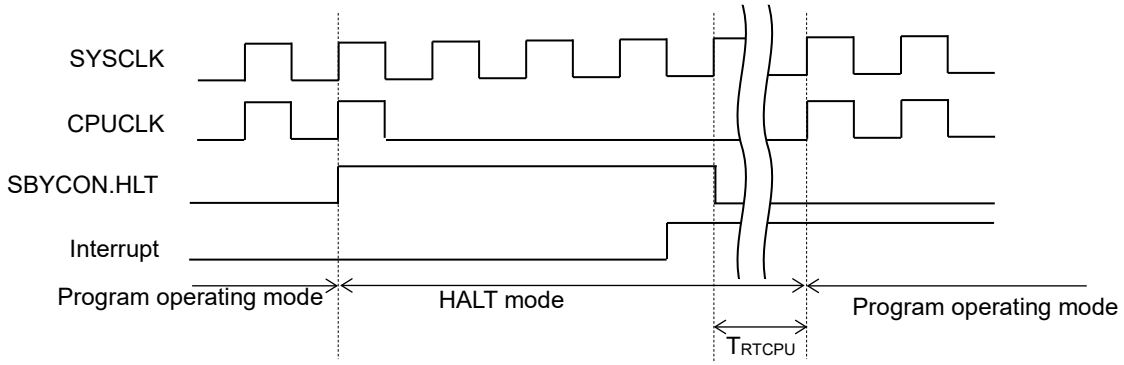
The program operating mode is the state where the CPU executes instructions sequentially.
When a reset occurs and then the reset is canceled, the operating state is shifted from the system reset mode to the program operating mode.
In addition, if an interrupt request is generated during standby mode, the mode shifts back to the program operating mode.
See Chapter 3 "Reset Function" for the system reset mode.

4.3.2 Standby Mode

4.3.2.1 HALT Mode

HALT mode is the state where the CPU stops and only the peripheral circuits keep operating with previous clock condition (LSCLK0 or HSCLK) for the system clock (SYSCLK) chosen before entering the HALT mode. See "4.3.2.8 Operation of Each Function in Standby Mode" for the operation of each function in the HALT mode.

When "1" is written to the HLT bit of the SBYCON register with DPM bit = “0”, shift to HALT mode. DPM bit and HLT bit can be set simultaneously.
When a WDT interrupt or an interrupt enabled by registers IE0 to IE7 occurs, the HALT mode is released at the rising edge of the next SYSCLK, and then the mode shifts back to the program operation mode.
Figure 4-4 shows operation waveforms in the HALT mode.



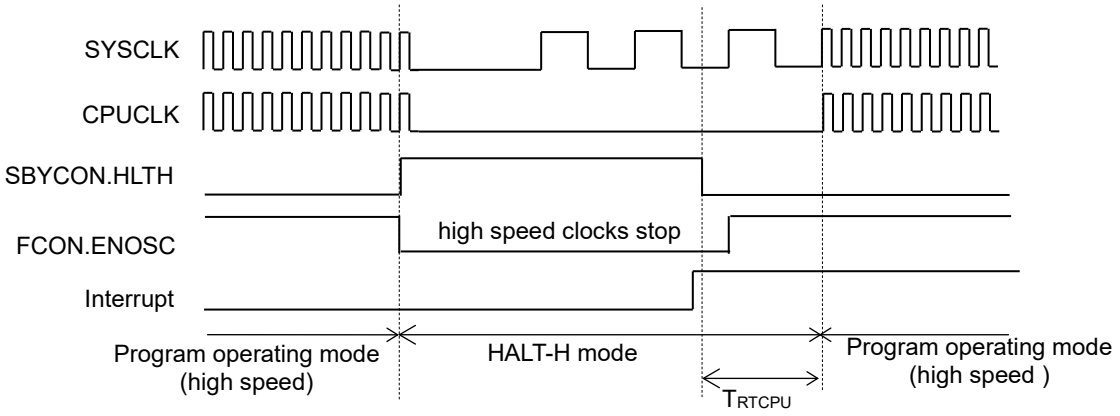
SBYCON : Standby control register
T_{RTCPU} : CPU clock restoring time (see Table 4-6)

Figure 4-4 Operation Waveforms in HALT Mode

4.3.2.2 HALT-H Mode

HALT-H mode is a state in which the high-speed clock (HSCLK/HSOCLK/HCKO) and CPU are stopped, SYSCLK is switched to a low speed, and only peripheral circuits are operating
This mode is suitable for short standby for intermittent operation. See "4.3.2.8 Operation of Each Function in Standby Mode" for operation of each function in the HALT-H mode.

When "1" is written in the HLTH bit of the SBYCON register, the operating state shift to HALT-H mode.
When a WDT interrupt or an interrupt enabled in registers IE0 to IE7 occurs, the HALT-H mode is released at the rising edge of the next SYSCLK, HSCLK is forcibly enabled, and the mode shifts back to the program run mode with the SYSCLK in the HSCLK state.
If the low-speed clock (LSCLK) is selected (SELSCLK="0") before entering the HALT-H mode, an entrying HALT-H is ignored.
Figure 4-5 shows operation waveforms in the HALT-H mode.

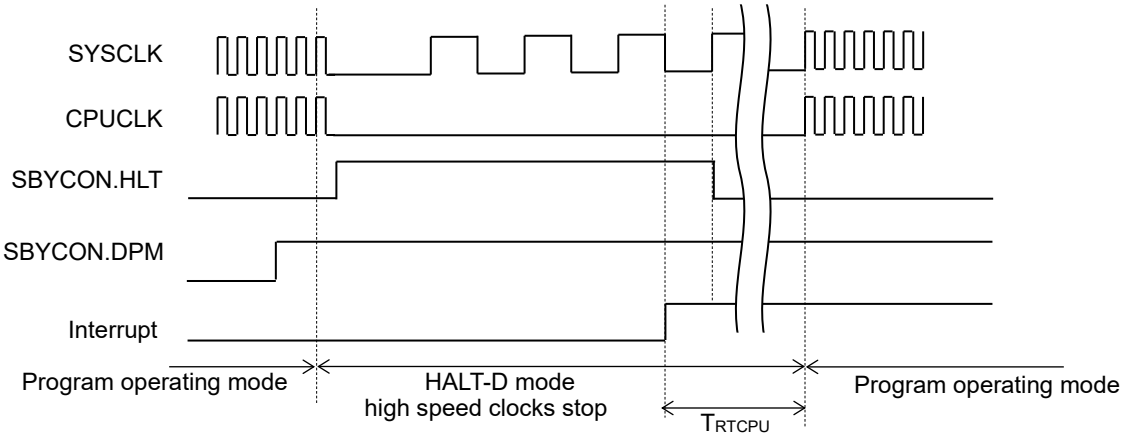


SBYCON : Standby control register
FCON : Frequency control register
T_{RTCPU} : CPU clock restoring time (see Table 4-6)

Figure 4-5 Operation Waveforms in HALT-H Mode

4.3.2.3 HALT-D Mode

HALT-D mode is a state in which the high speed clock, CPU, and some peripheral circuits are stopped, and the SYSCLK is switched to a low speed, and only peripheral circuits are operating.
This mode is suitable for a long standby.
See "4.3.2.8 Operation of Each Function in Standby Mode" for operation of each function in the HALT-D mode.
When "1" is written in the HLT bit of the SBYCON register with DPM bit = “1”, operating state shift to the HALT-D mode. DPM bit and HLT bit can be set simultaneously.
When WDT interrupt or an interrupt enabled by registers IE0 to IE7 occurs, the HALT mode is released at the rising edge of the next SYSCLK, and then the mode shifts back to the program operation mode.
Figure 4-6 shows operation waveforms in the HALT-D mode.



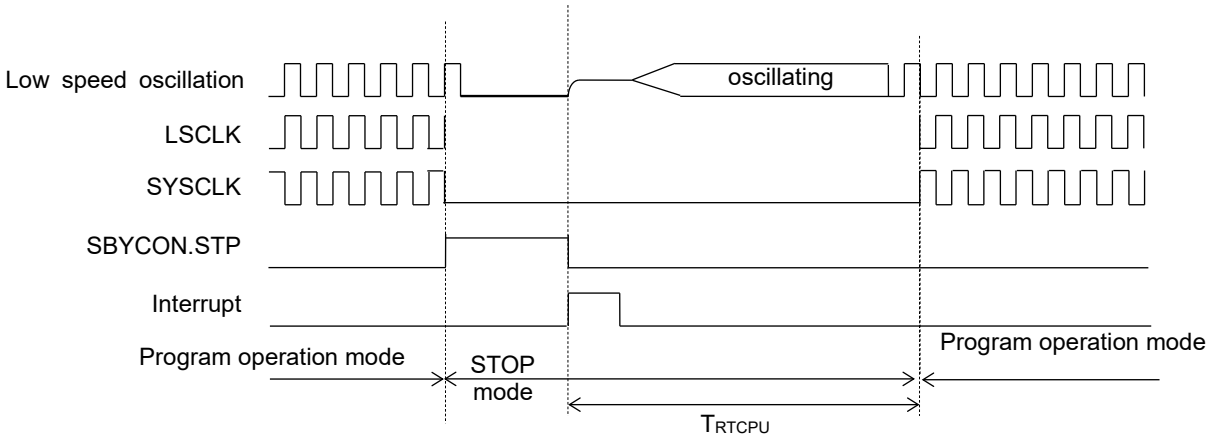
SBYCON : Standby control register
T_{RTCPU} : CPU clock restoring time (see Table 4-6)

Figure 4-6 Operation Waveforms in HALT-D Mode

4.3.2.4 STOP Mode

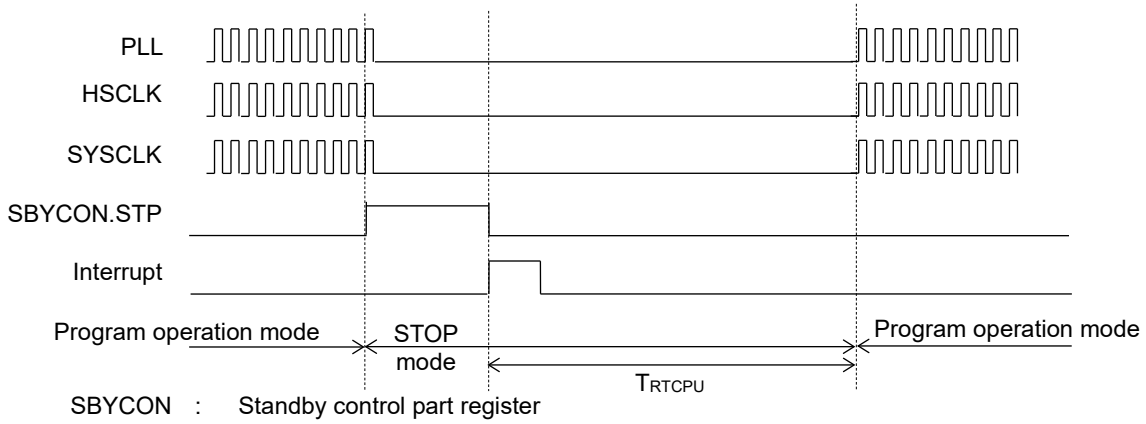
STOP mode is the state in which all clocks are forcibly stopped, and both CPU and all peripheral circuits that require clock input have stopped operating. See "4.3.2.8 Operation of Each Function in Standby Mode" for operation of each function in the STOP mode.
Write "1" to STP bit shifts to STOP mode after permitting shift to STOP mode by writing "0x5n" and "0xAn" (n = arbitrary) in this order to STPACP register.
DPM bit and STP bit can be set simultaneously.
STOP mode is released by interrupt requests from the external interrupt, voltage level monitoring function (VLS), or I^2C slave, and then the mode return to the program operation mode with same SYSCLK state as before shift to STOP mode.

Figure 4-7-1 and 4-7-2 shows STOP mode operation waveforms.



SBYCON : Standby control register
T_{RTCPU} : CPU clock wakeup time (see Table 4-6)

Figure 4-7-1 STOP Mode Operation Waveforms of Low-Speed Oscillation Circuit



SBYCON : Standby control part register
T_{RTCPU} : CPU clock wakeup time (see Table 4-6)

Figure 4-7-2 STOP Mode Operation Waveforms of PLL Oscillation Circuit

4.3.2.5 STOP-D Mode

STOP-D mode is the state that consumes less power than STOP mode because it lowers VDDL than STOP mode.
See "4.3.2.8 Operation of Each Function in Standby Mode" for operation of each function in the STOP-D mode.

To shift to STOP-D mode, follow the steps below.
1. Write "0x5n" and "0xAn" (n = arbitrary) sequentially to the STPACP register, and permit shifting to STOP mode.
2. Write “1” to DPM bit of the SBYCON register , and then write "1" to STP bit of the SBYCON register

DPM bit and STP bit can be set simultaneously.
The STOP-D mode is released by the external interrupts, voltage level supervisor (VLS), or interrupt requests from the I^2C bus unit (slave), and then the mode shift back to the program operation mode with same SYSCLK state as before shift to STOP-D mode.
The I^2C slave operation differs from STOP mode. See Chapter 13 “I^2C bus”.

4.3.2.6 Note of entering to the standby mode

In the conditions shown in the Table 4-2 , the mode does not shift to standby mode and continues the program operating mode.
An availability of shifting to standby mode is identified by monitoring each target bits in SBYEFLG register.
Table 4-2 shows availability of shifting to standby mode.

Table 4-2 availability of entering to standby mode (1 : not available, 0 : available)

Condition	Bit Status				
	FSTPD	FHLTD	FHLTH	FSTP	FHLT
When several bits of SBYCONL register are set simultaneously	0	0	0	0	0
When System clock is selected LSCLK0.	0	0	1	0	0
When requesting an interrupt to CPU. (Both interrupt enable register and interrupt request register bits are in the state of "1")	1	1	1	1	1
When accepter is disabled by SBYACP.	1	0	0	1	0
When A/D conversion of SA-ADC is in progress.	1	0	0	1	0
When operating single mode of VLS is in progress.	1	0	0	1	0
When waiting for stability time of supervisor mode of VLS.	1	0	0	1	0
When data flash memory erasing/programming is in progress.	1	1	1	1	0

If a peripheral circuit that uses a high-speed clock is transferred to HALT-H or the high-speed clock is stopped during operation, a unintending large current may flow depending on the timing of stopping (SA-ADC, PWM output by functional timer, etc.).

4.3.2.7 Note on shift back to Operating mode from Standby Mode

Returning from standby mode to operating mode differ each interrupt source shown below.

- interrupt level (ELEVEL) of the program status word (PSW)
- master interrupt enable flag (MIE),
- the contents of the register (IE0 to IE7),
- non-maskable interrupt
- maskable interrupt

See "nX-U16/100 Core Instruction Manual" for details of PSW
See Chapter 5 "Interrupts" for IE and IRQ registers respectively.

Tables 4-3-1 shows returning operating mode from standby mode in case of non-maskable interrupt
Tables 4-3-2 shows returning operating mode from standby mode in case of maskable interrupt

Table 4-3-1 Return Operation from Standby Mode (for Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Shift back operating mode from standby mode
X	X	-	0	Not returned from the standby mode.
3	X	-	1	After returning from the standby mode, the program operation restarts from the instruction next to the instruction that enters the standby mode. The program operation does not go to the interrupt routine.
0,1,2	X	-	1	After returning from the standby mode, the program operation restarts from the instruction next to the instruction that enters the standby mode. Then the program operation goes to the interrupt routine.

n=0 to 7, m=0 to 7. X: Value-independent

Table 4-3-2 Return Operation from Standby Mode (for Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from standby mode
X	X	X	0	Not returned from the standby mode.
X	X	0	1	
X	0	1	1	After returning from the standby mode, the program operation restarts from the instruction next to the instruction that enters the standby mode. The program operation does not go to the interrupt routine.
2,3	1	1	1	
0,1	1	1	1	After returning from the standby mode, the program operation restarts from the instruction next to the instruction that enters the standby mode. Then the program operation goes to the interrupt routine.

n=0 to 7, m=0 to 7. X: Value-independent

The ELEVEL of PSW has bits that indicate the state of interrupt process performed by the CPU It is set by the hardware when transferring to the interrupt process or returning from the interrupt.

Table 4-4 State of CPU-Processed Interrupt Indicated by ELEVEL

ELEVEL value	State of CPU-processed interrupt
0	Indicates that the CPU is not processing any interrupt (non-maskable interrupt, maskable interrupt, software interrupt).
1	Indicates that the CPU is processing a maskable or software interrupt.
2	Indicates that the CPU is processing a non-maskable interrupt.
3	Indicates that the CPU is processing an emulator-dedicated interrupt. Usually this is not used in the software.

[Note]

- **Since up to two instructions are executed during the period between the release of standby mode and a transition to interrupt processing, place two NOP instructions next to the instruction set for the standby mode. When a master interrupt enable (MIE) flag of the program status word (PSW) in the nX-U16/100 CPU core is "1", following the execution of the two NOP instructions, the interrupt transition cycle will be executed and execution of the instruction for interrupt routine begins. If MIE is "0", following the execution of the two NOP instructions, the instruction execution is continued from the one that follows the NOP instruction without transition to the interrupt.**

4.3.2.8 Operation of Each Function in Standby Mode

Table 4-5 shows the state of each function block in the standby mode.

Table 4-5 State of Each Function in Standby Mode
● : Operable, - : Not operable

Function blocks	HALT	HALT-H	HALT-D	STOP	STOP-D
Low speed oscillation (Internal RC oscillation)	●	●	●	-	-
Low speed oscillation (crystal or external input)	●	●	●	-	-
High speed oscillation (Internal PLL)	●	-	-	-	-
CPU	-	-	-	-	-
RAM	Retain	Retain	Retain	Retain	Retain
Watchdog timer(WDT)	●	●	●	-	-
External interrupt	●	●*2	●*2	●*1	●*1
Low-speed time base counter	●	●	●	-	-
16-bit timer	●	●	●	-*5	-*5
Functional timer	●	●	-*5	-*5	-*5
UART	●	●	-	-	-
SSIO (Master)	●	●*3	-	-	-
SSIO (Slave)	●	●	-*5	-*5	-*5
SSIO with FIFO (Master)	●	●*3	-	-	-
SSIO with FIFO (Slave)	●	●*3	-	-	-
I^2C bus unit (Master) / I^2C bus master	●	●*3	-	-	-
I^2C bus unit (Slave)	●	●	●*4	●*4	●*4
Successive approximation type A/D converter (SA-ADC)	●	●	-	-	-
Voltage Level Supervisor (VLS)	●	●	●	●*1	●*1
BGO operation (erasing/programming for data flash memory)	●	-	-	-	-
CRC calculator	●	●	-	-	-
Multiplier/Divider	-	-	-	-	-
LCD Driver	●	●	-*6	-*6	-*6
Audio playback function	●	●	-	-	-

*1 : If a sampling function is selected, it is forcibly disabled.
*2 : If a sampling function with high speed clock is selected, it is forcibly disabled.
*3 : System clock becomes low speed, so communication speed is influenced.
*4 : It is available to wake up by coincidence of slave address. A system clock supply is needed for communication after wake up.
*5 : Internal clocks is stop. If external clock is selected, the peripheral circuit operates. However its operation is not supported.
*6 : Before transferring to HALT-D, STOP, and STOP-D mode, stop LCD display by setting LMD1 bit and LMD0 bit of display control register (BIASCON) to “00”, and then turn off bias generation circuit by setting BSON bit of bias control register (BIASCON) to “0”.

4.3.2.9 Wake-up Time from Standby Mode

Table 4-6 shows the wake-up time (restoring time) from the standby modes.
See Chapter 6 "Clock Generation Circuit" for details of the FHWUPT register.

Table 4-6 Wake-up Time from Standby Mode (typ.)

Function	Condition	CPU clock recovering time [T_{RTCPU}]	Low-speed clock recovering time (Low-speed RC oscillation) [T_{RTLS}]	High-speed clock recovering time (PLL oscillation) [T_{RTPLL}]	
				FHWUPT=0x01	FHWUPT=0x00
HALT mode	Low-speed CPU clock High-speed clock OFF No CRC calculation	Approx.90µs	Continue Operation	Stop operation	
	Low-speed CPU clock High-speed clock ON or with CRC calculation	Approx.60µs		Continue Operation	
	High-speed CPU clock	-			
HALT-H mode	High-speed CPU clock No CRC calculation	T_{RTPLL}+15µs	Continue Operation	Approx.45µs	Max.2ms
	High-speed CPU clock With CRC calculation	T_{RTPLL}+15µs		Approx.60µs	Max.2ms
HALT-D mode	Low-speed CPU clock	Approx.300µs	Continue Operation	Approx.350µs	Max.2.5ms
	High-speed CPU clock	T_{RTPLL}			
STOP/ STOP-D mode	Low-speed CPU clock	T_{RTLS}	Approx.3ms	Approx.3ms	Max.4ms
	High-speed CPU clock	T_{RTPLL}			

[Note]

- **When FHWUPT register is set to "0x01", the frequency of PLL oscillation clock gradually increases and reaches the target frequency selected by the code option before approx. 2 ms elapse. The PLL oscillation clock during this time period can be used for the SYSCLK. However, accuracy of the frequency is not guaranteed.**

4.3.3 Block Control Function

ML62Q2700 group has the block clock control function, which stops clock supply for each peripheral circuit to reduce current consumption, and the block reset control function to reset each peripheral circuit.
When setting each bit of the BCKCONn registers (n=0 to 3) to "1", the clock supply to the corresponding peripheral circuits stops, and the current consumption is reduced.
When setting each bit of the BRECONn registers (n=0 to 3) to "1", the corresponding peripheral circuits are reset and those SFRs are set with initial values.
Table 4-7 shows the list of peripheral circuits controllable with the block control function and control registers.

Table 4-7 List of Peripheral Circuits and Control Registers

Peripheral circuit	Block clock control function		Block reset control function		Software reset function
	SFR word symbol	SFR bit symbol	SFR word symbol	SFR bit symbol	SFR bit symbol
16-bit timer 0	BCKCON0	DCKTM0	BRECON0	RSETM0	SOFTR*1
16-bit timer 1		DCKTM1		RSETM1	
16-bit timer 2		DCKTM2		RSETM2	
16-bit timer 3		DCKTM3		RSETM3	
16-bit timer 4		DCKTM4		RSETM4	
16-bit timer 5		DCKTM5		RSETM5	
16-bit timer 6		DCKTM6		RSETM6	
16 bit timer X		DCKTMX		RSETMX	
Functional timer 0	BCKCON1	DCKFTM0	BRECON1	RSEFTM0	
Functional timer 1		DCKFTM1		RSEFTM1	
Functional timer 2		DCKFTM2		RSEFTM2	
Functional timer 3		DCKFTM3		RSEFTM3	
Functional timer 4		DCKFTM4		RSEFTM4	
Functional timer 5		DCKFTM5		RSEFTM5	
Functional timer 6		DCKFTM6		RSEFTM6	
Functional timer 7		DCKFTM7		RSEFTM7	
I^2C bus master 0		DCKI2CM0		RSEI2CM0	
I^2C bus master 1		DCKI2CM1		RSEI2CM1	
I^2C bus unit 0		DCKI2CU0		RSEI2CU0	
SSIOF 0	BCKCON2	DCKSIOF0	BRECON2	RSESIOF0	
SSIO 0		DCKSIO0		RSESIO0	
SSIO 1		DCKSIO1		RSESIO1	
SSIO 2		DCKSIO2		RSESIO2	
UART 0		DCKUA0		RSEUA0	
UART 1		DCKUA1		RSEUA1	
UART 2		DCKUA2		RSEUA2	
CRC calculator		DCKCRC		RSECRC	
Audio playback		DCKVC0		RSEVC0	
Multiplier/Divider		DCKACC		RSEACC	

Peripheral circuit	Block clock control function		Block reset control function		Software reset function
	SFR word symbol	SFR bit symbol	SFR word symbol	SFR bit symbol	SFR bit symbol
Successive approximation type A/D converter	BCKCON3	DCKSAD	BRECON3	RSESAD	SOFTR*1
LCD Driver		DCKLCD		RSELCD	
Extended SSIO 0		DCKESIO0		RSEESIO0	
Extended SSIO 1		DCKESIO1		RSEESIO1	
Extended SSIO 2		DCKESIO2		RSEESIO2	
Extended UART 0		DCKEUA0		RESEEUA0	
Extended UART 1		DCKEUA1		RESEEUA1	
Extended UART 2		DCKEUA2		RESEEUA2	

*1 : SOFTR resets not only peripheral circuit but also general purpose ports setting.

After the system reset is released, operation of each peripheral circuit is disabled.
To enable the peripheral circuits, release the reset on the peripheral circuit by setting the bit of the BCKCONn register to "0", then setting the bit of the BRECONn register to "0".
Also, setting the bit of the BRECONn register to "1", only a reset can be generated while the clock is suppling, and each peripheral circuit can be initialized.

If the clock supply of each peripheral circuit is stopped or reset, writing to the SFR of the corresponding peripheral circuit is invalid. UARTs are also disabled for readout.

[Note]

- **If only the clock supply is stopped without resetting each peripheral circuit using the block control function, the output level of the pins is fixed, and excessive current may flow.**
  In addition, unexpected current may keep flowing while SA-ADC operation is stopped.

4.3.4 Internal Power Supply Voltage

After power-on, V_{DDL} becomes approximately 1.55V, and then V_{DDL} becomes approximately 1.45V after entering program run mode.
Power consumption is suppressed by controlling the voltage level and load capability depending on the operating state.
The code-option VLMD can fix the V_{DDL} to 1.55V except in the STOP-D/HALT-D mode.
Figure 4-8 shows the operation waveforms of the regulator. Table 4-8 shows V_{DDL} for operating mode.

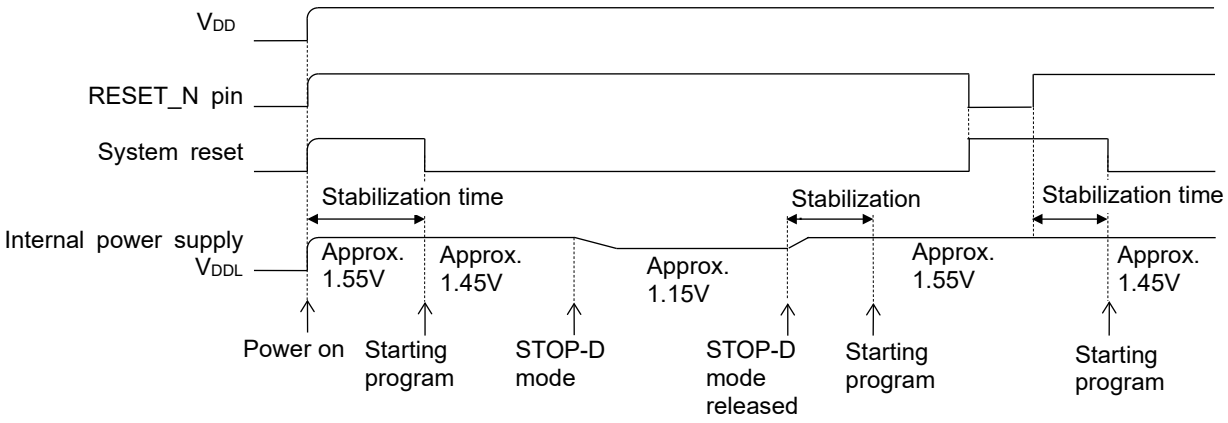


Figure 4-8 Regulator Operation Waveforms

Table 4-8 V_{DDL} for operating mode

Mode	V_{DDL} Voltage			
	VLMD=1			VLMD=0
	High speed clock off	High speed clock on with PLL1M mode	High speed clock on with PLL16/24M mode	
STOP mode	1.45V	1.45V	1.55V	1.55V
HALT mode	1.45V	1.45V	1.55V	1.55V
HALT-H mode	1.45V	1.45V	1.45V	1.55V
Program operating mode	1.45V	1.45V	1.55V	1.55V
HALT-D/STOP-D mode	1.15V	1.15V	1.15V	1.15V
At erasing/programming FLASH (FLASHSLF.FSELF=1)	-	1.55V	1.55V	1.55V

Chapter 5 Interrupts

5. Interrupt

5.1 General Description

ML62Q2700 group has the non-maskable interrupt, maskable interrupts and the software interrupt (SWI).
For details of each interrupt, see the corresponding Chapters.
See Chapter 29 "Safety Function" for the MCU status interrupt.
See "Table 1-2 Main Function List" to confirm the presence/absence of function in each product.

5.1.1 Features

- Master Interrupt Enable (MIE) flag enables or disables collectively the all maskable interrupts.
  For more details about MIE, see "nX-U16/100 Core Instruction Manual".
- IE0 to IE7 register enable or disable a maskable facto for each factor.
- The occurrence of interrupt request is confirmable by checking the request flag in interrupt requset register (IRQ).
- An interrupt is generatable by writing "1" to each bit of IRQ registers by the software.
- For maskable interrupts, four interrupt priorities of level 1 (low) to level 4 (high) are settable for each interrupt factor using the interrupt level control authorization register (ILEN), the current interrupt level control register (CIL), and the interrupt level control register 0 to 7 (ILC0 to 7).

5.2 Description of Registers

Writing to bits of unequipped interrupt is not available. They return 0x0 for reading. See to Table 5-1 for available interrupt.

5.2.1 List of Registers

Address	Name	Symbol name		R/W	Size	Initial value
		Byte	Word			
0xF020	Interrupt enable register 01	IE0	IE01	R/W	8/16	0x00
0xF021		IE1		R/W	8	0x00
0xF022	Interrupt enable register 23	IE2	IE23	R/W	8/16	0x00
0xF023		IE3		R/W	8	0x00
0xF024	Interrupt enable register 45	IE4	IE45	R/W	8/16	0x00
0xF025		IE5		R/W	8	0x00
0xF026	Interrupt enable register 67	IE6	IE67	R/W	8/16	0x00
0xF027		IE7		R/W	8	0x00
0xF028	Interrupt request register 01	IRQ0	IRQ01	R/W	8/16	0x00
0xF029		IRQ1		R/W	8	0x00
0xF02A	Interrupt request register 23	IRQ2	IRQ23	R/W	8/16	0x00
0xF02B		IRQ3		R/W	8	0x00
0xF02C	Interrupt request register 45	IRQ4	IRQ45	R/W	8/16	0x00
0xF02D		IRQ5		R/W	8	0x00
0xF02E	Interrupt request register 67	IRQ6	IRQ67	R/W	8/16	0x00
0xF02F		IRQ7		R/W	8	0x00
0xF030	Interrupt level control enable register	ILEN	-	R/W	8	0x00
0xF031	Reserved	-	-	-	-	-
0xF032	Current interrupt level management register	CIL	-	R/W	8	0x00
0xF033	Interrupt level mask register	MCIL	-	R/W	8	0x00
0xF034	Interrupt level control register 0	ILC00	ILC0	R/W	8/16	0x00
0xF035		ILC01		R/W	8	0x00
0xF036	Interrupt level control register 1	ILC10	ILC1	R/W	8/16	0x00
0xF037		ILC11		R/W	8	0x00
0xF038	Interrupt level control register 2	ILC20	ILC2	R/W	8/16	0x00
0xF039		ILC21		R/W	8	0x00
0xF03A	Interrupt level control register 3	ILC30	ILC3	R/W	8/16	0x00
0xF03B		ILC31		R/W	8	0x00
0xF03C	Interrupt level control register 4	ILC40	ILC4	R/W	8/16	0x00
0xF03D		ILC41		R/W	8	0x00
0xF03E	Interrupt level control register 5	ILC50	ILC5	R/W	8/16	0x00
0xF03F		ILC51		R/W	8	0x00
0xF040	Interrupt level control register 6	ILC60	ILC6	R/W	8/16	0x00
0xF041		ILC61		R/W	8	0x00
0xF042	Interrupt level control register 7	ILC70	ILC7	R/W	8/16	0x00
0xF043		ILC71		R/W	8	0x00

Table 5-1 shows presence/absence of interrupt source in each product.

Table 5-1 List of Interrupt Source

● : presence , - : absence

Register assignment			Interrupt source	Interrupt source symbol	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702	ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725
IRQ (interrupt request)	IE (interrupt enable)	ILC (interrupt level)				
IRQ0[0]	-	-	WDT Interrupt	WDTINT	●	●
IRQ0[6]	IE0[6]	ILC0[13:12]	VLS0 Interrupt	VLS0INT	●	-
IRQ0[7]	IE0[7]	ILC0[15:14]	-	-	-	●
IRQ1[0]	IE1[0]	ILC1[1:0]	External Interrupt 0	EXI0INT	●	●
IRQ1[1]	IE1[1]	ILC1[3:2]	External Interrupt 1	EXI1INT	●	●
IRQ1[2]	IE1[2]	ILC1[5:4]	External Interrupt 2	EXI2INT	●	●
IRQ1[3]	IE1[3]	ILC1[7:6]	External Interrupt 3	EXI3INT	●	●
IRQ1[4]	IE1[4]	ILC1[9:8]	External Interrupt 4	EXI4INT	●	●
IRQ1[5]	IE1[5]	ILC1[11:10]	External Interrupt 5	EXI5INT	●	●
IRQ1[6]	IE1[6]	ILC1[13:12]	External Interrupt 6	EXI6INT	●	●
IRQ1[7]	IE1[7]	ILC1[15:14]	External Interrupt 7	EXI7INT	●	●
IRQ2[0]	IE2[0]	ILC2[1:0]	Clock Backup Interrupt	CBUINT	●	-
IRQ2[1]	IE2[1]	ILC2[3:2]	-	-	-	●
IRQ2[2]	IE2[2]	ILC2[5:4]	MCU Status Interrupt	MCSINT	●	●
IRQ2[3]	IE2[3]	ILC2[7:6]	UART00 Interrupt	UA00INT	●	●
IRQ2[4]	IE2[4]	ILC2[9:8]	UART01 Interrupt	UA01INT	●	-
IRQ2[5]	IE2[5]	ILC2[11:10]	-	-	-	●
IRQ2[6]	IE2[6]	ILC2[13:12]	Successive Approximation type A-D Converter Interrupt (SA-ADC Interrupt)	SADINT	●	●
IRQ2[7]	IE2[7]	ILC2[15:14]	SSIOF0 Interrupt	SIOF0INT	●	●
IRQ3[0]	IE3[0]	ILC3[1:0]	SSIO0 Interrupt	SIO0INT	●	-
IRQ3[1]	IE3[1]	ILC3[3:2]	-	-	-	●
IRQ3[2]	IE3[2]	ILC3[5:4]	I^2C Bus Master 0 Interrupt	I2CM0INT	●	-
IRQ3[3]	IE3[3]	ILC3[7:6]	-	-	-	●
IRQ3[4]	IE3[4]	ILC3[9:8]	Functional Timer 0 Interrupt	FTM0INT	●	●
IRQ3[5]	IE3[5]	ILC3[11:10]	Functional Timer 1 Interrupt	FTM1INT	●	●
IRQ3[6]	IE3[6]	ILC3[13:12]	16-bit Timer 0 Interrupt	TM0INT	●	●
IRQ3[7]	IE3[7]	ILC3[15:14]	16-bit Timer 1 Interrupt	TM1INT	●	●
IRQ4[0]	IE4[0]	ILC4[1:0]	I^2C Bus Unit 0 Interrupt	I2CU0INT	●	●
IRQ4[1]	IE4[1]	ILC4[3:2]	UART10 Interrupt	UA10INT	●	●
IRQ4[2]	IE4[2]	ILC4[5:4]	UART11 Interrupt	UA11INT	●	-
IRQ4[3]	IE4[3]	ILC4[7:6]	-	-	-	●
IRQ4[4]	IE4[4]	ILC4[9:8]	Functional Timer 2 Interrupt	FTM2INT	●	●
IRQ4[5]	IE4[5]	ILC4[11:10]	Functional Timer3 Interrupt	FTM3INT	●	●

Register assignment			Interrupt source	Interrupt source symbol	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702	ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725
IRQ (interrupt request)	IE (interrupt enable)	ILC (interrupt level)				
IRQ4[6]	IE4[6]	ILC4[13:12]	16-bit Timer 2 Interrupt	TM2INT	●	●
IRQ4[7]	IE4[7]	ILC4[15:14]	16-bit Timer 3 Interrupt	TM3INT	●	●
IRQ5[0]	IE5[0]	ILC5[1:0]	UART20 Interrupt	UA20INT	-	●
IRQ5[1]	IE5[1]	ILC5[3:2]	UART21 Interrupt	UA21INT	-	●
IRQ5[2]	IE5[2]	ILC5[5:4]	Audio0 Interrupt	VC0INT	●	●
IRQ5[3]	IE5[3]	ILC5[7:6]	Audio PWM Fixing detection Interrupt	VPHDINT	●	●
IRQ5[4]	IE5[4]	ILC5[9:8]	Functional timer4 Interrupt	FTM4INT	●	●
IRQ5[5]	IE5[5]	ILC5[11:10]	Functional timer5 Interrupt	FTM5INT	●	●
IRQ5[6]	IE5[6]	ILC5[13:12]	16-bit Timer 4 Interrupt	TM4INT	●	●
IRQ5[7]	IE5[7]	ILC5[15:14]	16-bit Timer 5 Interrupt	TM5INT	-	●
IRQ6[0]	IE6[0]	ILC6[1:0]	SSIO1 Interrupt	SIO1INT	●	●
IRQ6[1]	IE6[1]	ILC6[3:2]	SSIO2 Interrupt	SIO2INT	-	●
IRQ6[2]	IE6[2]	ILC6[5:4]	Extended SIO Interrupt	XSIOINT	-	●
IRQ6[3]	IE6[3]	ILC6[7:6]	Extended UART Interrupt	XUAINT	-	●
IRQ6[4]	IE6[4]	ILC6[9:8]	Functional timer6 Interrupt	FTM6INT	-	●
IRQ6[5]	IE6[5]	ILC6[11:10]	Functional timer7 Interrupt	FTM7INT	-	●
IRQ6[6]	IE6[6]	ILC6[13:12]	16-bit Timer 6 Interrupt	TM6INT	-	-
IRQ6[7]	IE6[7]	ILC6[15:14]	-	-	-	-
IRQ7[0]	IE7[0]	ILC7[1:0]	-	-	-	●
IRQ7[1]	IE7[1]	ILC7[3:2]	16-bit Timer X Interrupt	TMXINT	●	●
IRQ7[2]	IE7[2]	ILC7[5:4]	Low-speed Time Base Counter 0 Interrupt	LTB0INT	●	●
IRQ7[3]	IE7[3]	ILC7[7:6]	Low-speed Time Base Counter 3 Interrupt	LTB3INT	●	●
IRQ7[4]	IE7[4]	ILC7[9:8]	Low-speed Time Base Counter 1 Interrupt	LTB1INT	●	●
IRQ7[5]	IE7[5]	ILC7[11:10]	Low-speed Time Base Counter 2 Interrupt	LTB2INT	●	-
IRQ7[6]	IE7[6]	ILC7[13:12]	-	-	-	-
IRQ7[7]	IE7[7]	ILC7[15:14]	-	-	-	

5.2.2 Interrupt Enable Register 01 (IE01)

IE01 is a SFR to enable or disable an interrupt for each interrupt request.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF020(IE0/IE01), 0xF021(IE1)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IE01															
Byte	IE1								IE0							
Bit	EPI7	EPI6	EPI5	EPI4	EPI3	EPI2	EPI1	EPI0	-	EVLS0	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured enable/disable a target interrupt
0: Disable a target interrupt (Initial value)
1: Enable a target interrupt

After the interrupt is accepted, the master interrupt enable flag (MIE) of the CPU is reset to "0", however, the each applicable flag of a bit of target interrupt is not reset and remains "1".

Bit No.	Bit symbol name	Description (target interrupt)
15	EPI7	external interrupt 7 (EXI7INT)
14	EPI6	external interrupt 6 (EXI6INT)
13	EPI5	external interrupt 5 (EXI5INT)
12	EPI4	external interrupt 4 (EXI4INT)
11	EPI3	external interrupt 3 (EXI3INT)
10	EPI2	external interrupt 2 (EXI2INT)
9	EPI1	external interrupt 1 (EXI1INT)
8	EPI0	external interrupt 0 (EXI0INT)
7	-	Reserved bit
6	EVLS0	VLS0 interrupt (VLS0INT)
5 to 0	-	Reserved bits

5.2.3 Interrupt Enable Register 23 (IE23)

IE23 is a SFR to enable or disable an interrupt for each interrupt request.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF022(IE2/IE23), 0xF023(IE3)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IE23															
Byte	IE3								IE2							
Bit	ETM1	ETM0	EFTM1	EFTM0	EI2CM1	EI2CM0	EEXTX	ESIO0	ESIOF0	ESAD	-	EUA01	EUA00	EMCS	-	ECBU
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured enable/disable a target interrupt
0: Disable a target interrupt (Initial value)
1: Enable a target interrupt

After the interrupt is accepted, the master interrupt enable flag (MIE) of the CPU is reset to "0", however, the each applicable flag of a bit of target interrupt is not reset and remains "1".

Bit No.	Bit symbol name	Description (target interrupt)
15	ETM1	16-bit Timer 1 interrupt (TM1INT)
14	ETM0	16-bit Timer 0 interrupt (TM0INT)
13	EFTM1	Functional Timer 1 interrupt (FTM1INT)
12	EFTM0	Functional Timer 0 interrupt (FTM0INT)
11	EI2CM1	I^2C Bus Master 1 interrupt (I2CM1INT)
10	EI2CM0	I^2C Bus Master 0 interrupt (I2CM0INT)
9	EEXTX	Extended External interrupt (EXTINT)
8	ESIO0	SSIO0 interrupt (SIO0INT)
7	ESIOF0	SSIOF0 interrupt (SIOF0INT)
6	ESAD	SA-ADC interrupt (SADINT)
5	-	Reserved bit
4	EUA01	UART01 interrupt (UA01INT)
3	EUA00	UART00 interrupt (UA00INT)
2	EMCS	MCU Status interrupt (MCSINT) See Chapter 29 "Safety Function" for more details.
1	-	Reserved bit
0	ECBU	Clock Backup interrupt (CBUINT) See Chapter 6 "Clock Generation Circuit" for more details.

5.2.4 Interrupt Enable Register 45 (IE45)

IE45 is a SFR to enable or disable an interrupt for each interrupt request.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF024(IE4/IE45), 0xF025(IE5)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IE45															
Byte	IE5								IE4							
Bit	ETM5	ETM4	EFTM5	EFTM4	EVPHD	EVC0	EUA21	EUA20	ETM3	ETM2	EFTM3	EFTM2	-	EUA11	EUA10	EI2CU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured enable/disable a target interrupt
0: Disable a target interrupt (Initial value)
1: Enable a target interrupt

After the interrupt is accepted, the master interrupt enable flag (MIE) of the CPU is reset to "0", however, the each applicable flag of a bit of target interrupt is not reset and remains "1".

Bit No.	Bit symbol name	Description (target interrupt)
15	ETM5	16-bit Timer 5 interrupt (TM4INT)
14	ETM4	16-bit Timer 4 interrupt (TM4INT)
13	EFTM5	Functional Timer 5 interrupt (FTM5INT)
12	EFTM4	Functional Timer 4 interrupt (FTM4INT)
11	EVPHD	Audio PWM Fixing detection Interrupt
10	EVC0	Audio 0 interrupt (VC0INT)
9	EUA21	UART21 interrupt (UA21INT)
8	EUA20	UART20 interrupt (UA20INT)
7	ETM3	16-bit Timer 3 interrupt (TM3INT)
6	ETM2	16-bit Timer 2 interrupt (TM2INT)
5	EFTM3	Functional Timer 3 interrupt (FTM4INT)
4	EFTM2	Functional Timer 2 interrupt (FTM4INT)
3	-	Reserved bit
2	EUA11	UART11 interrupt (UA11INT)
1	EUA10	UART10 interrupt (UA10INT)
0	EI2CU0	I^2C Bus Unit 0 interrupt (I2CU0INT)

5.2.5 Interrupt Enable Register 67 (IE67)

IE67 is a SFR to enable or disable an interrupt for each interrupt request.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF026(IE6/IE67), 0xF027(IE7)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IE67															
Byte	IE7								IE6							
Bit	-	-	ELTBC2	ELTBC1	ELTBC3	ELTBC0	ETMX	-	-	ETM6	EFTM7	EFTM6	EEUA	EESIO	ESIO2	ESIO1
R/W	R	R	R/W	R/W	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured enable/disable a target interrupt
0: Disable a target interrupt (Initial value)
1: Enable a target interrupt

After the interrupt is accepted, the master interrupt enable flag (MIE) of the CPU is reset to "0", however, the each applicable flag of a bit of target interrupt is not reset and remains "1".

Bit No.	Bit symbol name	Description (target interrupt)
15	-	Reserved bit
14	-	Reserved bit
13	ELTBC2	Low speed Time base counter 2 interrupt (LTB2INT)
12	ELTBC1	Low speed Time base counter 1 interrupt (LTB1INT)
11	ELTBC3	Low speed Time base counter 3 interrupt (LTB3INT)
10	ELTBC0	Low speed Time base counter 0 interrupt (LTB0INT)
9	ETMX	16-bit Timer X interrupt (TMXINT)
8	-	Reserved bit
7	-	Reserved bit
6	ETM6	16bit Timer 6 interrupt (TM6INT)
5	EFTM7	Functional Timer 7 interrupt (FTM7INT)
4	EFTM6	Functional Timer 6 interrupt (FTM6INT)
3	EEUA	Extended UART interrupt (XUAINT)
2	EESIO	Extended SIO interrupt (XSIOINT)
1	ESIO2	SSIO2 interrupt (SIO2INT)
0	ESIO1	SSIO1 interrupt (SIO1INT)

5.2.6 Interrupt Request Register 01 (IRQ01)

This is a SFR to request interrupts.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF028(IRQ0/IRQ01), 0xF029(IRQ1)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IRQ01															
Byte	IRQ1								IRQ0							
Bit	QPI7	QPI6	QPI5	QPI4	QPI3	QPI2	QPI1	QPI0	-	QVLS0	-	-	-	-	-	QWDT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is a flag of a target interrupt request
0: Not request a target interrupt (Initial value)
1: Request a target interrupt

QWDT bit of the IRQ01 register becomes "1" when the non-maskable Watch Dog Timer (WDT) interrupt occurs and the CPU goes to the interrupt routine regardless the value of the Master Interrupt Enable flag (MIE bit).
Each request flag of IRQ01 except for the QWDT bit becomes "1" when the interrupt request is generated, regardless of the values of the interrupt enable register 01(IE01) and master interrupt enable flag (MIE). At that time, it requests the interrupt to the CPU if the applicable flag of IE01 is "1" and the CPU accepts the interrupt if the MIE is "1" to goes to the interrupt routine.
Also, an interrupt can be generated by writing "1" to the request flag of IRQ01. In this case, the CPU goes to the interrupt routine immediately after the next one instruction is executed.
The applicable flag of IRQ01 becomes "0" automatically when the interrupt request is accepted by the CPU.

Bit No.	Bit symbol name	Description (target interrupt)
15	QPI7	external interrupt 7 (EXI7INT)
14	QPI6	external interrupt 6 (EXI6INT)
13	QPI5	external interrupt 5 (EXI5INT)
12	QPI4	external interrupt 4 (EXI4INT)
11	QPI3	external interrupt 3 (EXI3INT)
10	QPI2	external interrupt 2 (EXI2INT)
9	QPI1	external interrupt 1 (EXI1INT)
8	QPI0	external interrupt 0 (EXI0INT)
7	-	Reserved bit
6	QVLS0	VLS0 interrupt (VLS0INT)
5 to 1	-	Reserved bits
0	QWDT	external interrupt 7 (EXI7INT)

[Note]
- **There is a risk of clearing other request flags of This IRQ register, if writing to the specific bit of this register. Use the bit symbol to write to the specific bit.**
  See Section 5.3.8 "Writing to IRQ01/IRQ23/IRQ45/IRQ67" for more detail.

5.2.7 Interrupt Request Register 23 (IRQ23)

This is a SFR to request interrupts.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF02A(IRQ2/IRQ23), 0xF02B(IRQ3)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IRQ23															
Byte	IRQ3								IRQ2							
Bit	QTM1	QTM0	QFTM1	QFTM0	-	QI2CM0	-	QSIO0	QSIOF0	QSAD	-	QUA01	QUA00	QMCS	-	QCBU
R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is a flag of a target interrupt request
0: Not request a target interrupt (Initial value)
1: Request a target interrupt

Each request flag of IRQ23 becomes "1" when the interrupt request is generated, regardless of the values of the interrupt enable register 01(IE23) and master interrupt enable flag (MIE). At that time, it requests the interrupt to the CPU if the applicable flag of IE23 is "1" and the CPU accepts the interrupt if the MIE is "1" to goes to the interrupt routine.
Also, an interrupt can be generated by writing "1" to the request flag of IRQ23. In this case, the CPU goes to the interrupt routine immediately after the next one instruction is executed.
The applicable flag of IRQ23 becomes "0" automatically when the interrupt request is accepted by the CPU.

Bit No.	Bit symbol name	Description (target interrupt)
15	QTM1	16-bit Timer 1 interrupt (TM1INT)
14	QTM0	16-bit Timer 0 interrupt (TM0INT)
13	QFTM1	Functional Timer 1 interrupt (FTM1INT)
12	QFTM0	Functional Timer 0 interrupt (FTM0INT)
11	-	Reserved bit
10	QI2CM0	I^2C Bus Master 0 interrupt (I2CM0INT)
9	-	Reserved bit
8	QSIO0	SSIO0 interrupt (SIO0INT)
7	QSIOF0	SSIOF0interrupt (SIOF0INT)
6	QSAD	SA-ADC interrupt (SADINT)
5	-	Reserved bit
4	QUA01	UART01 interrupt (UA01INT)
3	QUA00	UART00 interrupt (UA00INT)
2	QMCS	MCU Status interrupt (MCSINT) See Chapter 29 "Safety Function" for more details.
1	-	Reserved bit
0	QCBU	Clock Backup interrupt (CBUINT) See Chapter 6 "Clock Generation Circuit" for more details.

[Note]
- **There is a risk of clearing other request flags of This IRQ register, if writing to the specific bit of this register. Use the bit symbol to write to the specific bit.**
  See Section 5.3.8 "Writing to IRQ01/IRQ23/IRQ45/IRQ67" for more detail.

5.2.8 Interrupt Request Register 45 (IRQ45)

This is a SFR to request interrupts.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF02C(IRQ4/IRQ45), 0xF02D(IRQ5)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IRQ45															
Byte	IRQ5								IRQ4							
Bit	-	QTM4	-	-	-	-	QUA21	QUA20	QTM3	QTM2	-	-	-	QUA11	QUA10	QI2CU0
R/W	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is a flag of a target interrupt request
0: Not request a target interrupt (Initial value)
1: Request a target interrupt

Each request flag of IRQ45 becomes "1" when the interrupt request is generated, regardless of the values of the interrupt enable register 01(IE45) and master interrupt enable flag (MIE). At that time, it requests the interrupt to the CPU if the applicable flag of IE45 is "1" and the CPU accepts the interrupt if the MIE is "1" to goes to the interrupt routine.
Also, an interrupt can be generated by writing "1" to the request flag of IRQ45. In this case, the CPU goes to the interrupt routine immediately after the next one instruction is executed.
The applicable flag of IRQ45 becomes "0" automatically when the interrupt request is accepted by the CPU.

Bit No.	Bit symbol name	Description (target interrupt)
15	-	Reserved bit
14	QTM4	16-bit Timer 4 interrupt (TM4INT)
13 to 10	-	Reserved bits
9	QUA21	UART21 interrupt (UA21INT)
8	QUA20	UART20 interrupt (UA20INT)
7	QTM3	16-bit Timer 3 interrupt (TM3INT)
6	QTM2	16-bit Timer 2 interrupt (TM2INT)
5 to 3	-	Reserved bit
2	QUA11	UART11 interrupt (UA11INT)
1	QUA10	UART10 interrupt (UA10INT)
0	QI2CU0	I^2C Bus Unit 0 interrupt (I2CU0INT)

[Note]
- **There is a risk of clearing other request flags of This IRQ register, if writing to the specific bit of this register. Use the bit symbol to write to the specific bit.**
  See Section 5.3.8 "Writing to IRQ01/IRQ23/IRQ45/IRQ67" for more detail.

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5.2.9 Interrupt Request Register 67 (IRQ67)

This is a SFR to request interrupts.
See to "Table.5-1 List of Interrupt Source" for available peripherals.

Address: 0xF02E(IRQ6/IRQ67), 0xF02F(IRQ7)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	IRQ67															
Byte	IRQ7								IRQ6							
Bit	-	-	QLTBC2	QLTBC1	QLTBC3	QLTBC0	QTMX	-	-	QTM6	QFTM7	QFTM6	QEUA	QESIO	QSIO2	QSIO1
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is a flag of a target interrupt request
0: Not request a target interrupt (Initial value)
1: Request a target interrupt

Each request flag of IRQ45 becomes "1" when the interrupt request is generated, regardless of the values of the interrupt enable register 01(IE45) and master interrupt enable flag (MIE). At that time, it requests the interrupt to the CPU if the applicable flag of IE45 is "1" and the CPU accepts the interrupt if the MIE is "1" to goes to the interrupt routine.
Also, an interrupt can be generated by writing "1" to the request flag of IRQ45. In this case, the CPU goes to the interrupt routine immediately after the next one instruction is executed.
The applicable flag of IRQ45 becomes "0" automatically when the interrupt request is accepted by the CPU.

Bit No.	Bit symbol name	Description (target interrupt)
15, 14	-	Reserved bits
13	QLTBC2	Low speed Time base counter 2 interrupt (LTB2INT)
12	QLTBC1	Low speed Time base counter 1 interrupt (LTB1INT)
11	QLTBC3	Low speed Time base counter 3 interrupt (LTB3INT)
10	QLTBC0	Low speed Time base counter 0 interrupt (LTB0INT)
9	QTMX	16-bit Timer X interrupt (TMXINT)
8, 7	-	Reserved bits
6	QTM6	16bit Timer 6 interrupt (RM5INT)
5	QFTM7	Functional Timer 7 interrupt (FTM7INT)
4	QFTM6	Functional Timer 6 interrupt (FTM6INT)
3	QEUA	Extended UART interrupt (XUAINT)
2	QESIO	Extended SIO interrupt (XSIOINT)
1	QSIO2	SSIO2 interrupt (SIO2INT)
0	QSIO1	SSIO1 interrupt (SIO1INT)

[Note]
- **There is a risk of clearing other request flags of This IRQ register, if writing to the specific bit of this register. Use the bit symbol to write to the specific bit.**
  See Section 5.3.8 "Writing to IRQ01/IRQ23/IRQ45/IRQ67" for more detail.
- **.**

5.2.10 Interrupt Level Control Enable Register (ILEN)

ILEN is a SFR to enable or disable the interrupt level control.

Address: 0xF030(ILEN)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								ILEN							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ILE
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 1	-	Reserved bits
0	ILE	This bit controls to enable or disable the interrupt level control. 0: Disable the interrupt (Initial value) 1: Enable the interrupt

[Note]

- **When disable the interrupt level control function, set the ILE bit to "0" after set the Interrupt level control register (ILC0 to ILC7) to "0x0000" and also after confirm the current interrupt request level register (CIL) is "0x00" in interrupt disabled state (IE01 to IE67 registers are "0x00").**
- **When enabling the interrupt level control function, set the ILE bit to "1" when the permission flag for the interrupt in the interrupt permit register (IE01~IE67) is "0" or the master interrupt enable flag (MIE) is "0". If an interrupt is written when the permission flag of the interrupt in IE0~IE7 is "1" and the MIE is "1", an interrupt may occur at an unintended interrupt level.**

5.2.11 Current Interrupt Level Management Register (CIL)

CIL is a SFR to manage the priority level of the interrupt currently being processed by the CPU.
See the Section 5.3.6 "How To describe Interrupt Processing When Interrupt Level Control Enabled".

Address: 0xF032(CIL)
Access: R/W
Access size: 8 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								CIL							
Bit	-	-	-	-	-	-	-	-	CILN	-	-	-	CILM 3	CILM 2	CILM 1	CILM 0
R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

After maskable or non-maskable interrupts to which the priority levels are specified by the interrupt level control registers (ILC0 to 7) is accepted by the CPU, corresponding bits of CIL are automatically set to "1", indicate the currently processing interrupt level.
Interrupts request to the CPU below the currently processed interrupt level will be disabled.
When the multiple bits are "1" in the CIL, it indicates the CPU is processing the multiple interrupts.

Each bit of CIL is automatically set to "1", so it has to be cleared by the software when the interrupt process has been ended. Clear the bit once by writing an arbitrary data at the last in the interrupt process, which resets a flag of CIL corresponding to the highest level.

Common description of each bits:
0: A target interrupt is not being processed (Initial value)
1: A target interrupt is being processed

Bit No.	Bit symbol name	Description (target interrupt)
7	CILN	Non-maskable interrupt
6 to 4	-	Reserved bits
3	CILM3	maskable interrupt with level 4
2	CILM2	maskable interrupt with level 3
1	CILM1	maskable interrupt with level 2
0	CILM0	maskable interrupt with level 1

5.2.12 Masking Interrupt Level Register (MCIL)

MCIL is a SFR to configure masking interrupt level.
It is writeable only when the interrupt level control is enabled by setting ILE bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF033(MCIL)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								MCIL							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	MCIL 3	MCIL 2	MCIL 1	MCIL 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The interrupt notification to the CPU is suspended if interrupt level specified by the ILC0 to ILC7 registers is equal or less than the level specified in the MCIL register.
The interrupt request is notified by lowering the setting value of MCIL register below the suspended interrupt level.

Common description of each bits :
0: A maskable interrupt of a target interrupt level is being processed (Initial value)
1: A maskable interrupt under a target interrupt level is being processed

Bit No.	Bit symbol name	Description (target interrupt level)
7 to 4	-	Reserved bits
3	MCIL3	Interrupt level 4
2	MCIL2	Interrupt level 3
1	MCIL1	Interrupt level 2
0	MCIL0	Interrupt level 1

5.2.13 Interrupt Level Control Register 0 (ILC0)

ILC0 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting ILE bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF034(ILC00/ILC0), 0xF035(ILC01)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC0															
Byte	ILC01								ILC00							
Bit	-	-	ILVLS0H	ILVLS0L	-	-	-	-	-	-	-	-	-	-	-	-
R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured a target interrupt level.
00: level 1 ; a priority is lower. (Initial value)
01: level 2
10: level 3
11: level 4 ; a priority is higher.

Bit No.	Bit symbol name	Description (target interrupt level)
15,14	-	Reserved bits
13,12	ILVLS0H, ILVLS0L	VLS0 interrupt (VLS0INT)
11 to 0	-	Reserved bits

[Note]
- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**

5.2.14 Interrupt Level Control Register 1 (ILC1)

ILC1 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting ILE bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF036(ILC10/ILC1), 0xF037(ILC11)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC1															
Byte	ILC11								ILC10							
Bit	ILPI 7H	ILPI 7L	ILPI 6H	ILPI 6L	ILPI 5H	ILPI 5L	ILPI 4H	ILPI 4L	ILPI 3H	ILPI 3L	ILPI 2H	ILPI 2L	ILPI 1H	ILPI 1L	ILPI 0H	ILPI 0L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured a target interrupt level.
00: level 1 ; a priority is lower. (Initial value)
01: level 2
10: level 3
11: level 4 ; a priority is higher.

Bit No.	Bit symbol name	Description (target interrupt level)
15,14	ILPI7H, ILPI7L	external interrupt 7 (EXI7INT)
13,12	ILPI6H, ILPI6L	external interrupt 6 (EXI6INT)
11,10	ILPI5H, ILPI5L	external interrupt 5 (EXI5INT)
9,8	ILPI4H, ILPI4L	external interrupt 4 (EXI4INT)
7,6	ILPI3H, ILPI3L	external interrupt 3 (EXI3INT)
5,4	ILPI2H, ILPI2L	external interrupt 2 (EXI2INT)
3,2	ILPI1H, ILPI1L	external interrupt 1 (EXI1INT)
1,0	ILPI0H, ILPI0L	external interrupt 0 (EXI0INT)

[Note]
- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**
-

5.2.15 Interrupt Level Control Register 2 (ILC2)

ILC2 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting IEL bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF038(ILC20/ILC2), 0xF039(ILC21)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC2															
Byte	ILC21								ILC20							
Bit	ILSIOF0H	ILSIOF0L	ILSADH	ILSADL	-	-	ILUA01H	ILUA01L	ILUA00H	ILUA00L	ILMCSH	ILMCSL	-	-	ILCBUH	ILCBUL
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured a target interrupt level.
00: level 1 ; a priority is lower. (Initial value)
01: level 2
10: level 3
11: level 4 ; a priority is higher.

Bit No.	Bit symbol name	Description (target interrupt level)
15,14	ILSIOF0H, ILSIOF0L	SSIOF0interrupt (SIOF0INT)
13,12	ILSADH, ILSADL	SA-ADC interrupt (SADINT)
11,10	-	Reserved bits
9,8	ILUA01H, ILUA01L	UART01 interrupt (UA01INT)
7,6	ILUA00H, ILUA00L	UART00 interrupt (UA00INT)
5,4	ILMCSH, ILMCSL	MCU Status interrupt (MCSINT) See Chapter 29 "Safety Function" for more details.
3,2	-	Reserved bit
1,0	ILCBUH, ILCBUL	Clock Backup interrupt (CBUINT) See Chapter 6 "Clock Generation Circuit" for more details.

[Note]
- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**
-

5.2.16 Interrupt Level Control Register 3 (ILC3)

ILC3 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting ILE bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF03A(ILC30/ILC3), 0xF03B(ILC31)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC3															
Byte	ILC31								ILC30							
Bit	ILTM1H	ILTM1L	ILTM0H	ILTM0L	ILFTM1H	ILFTM1L	ILFTM0H	ILFTM0L	ILI2CM1H	ILI2CM1L	ILI2CM0H	ILI2CM0L	ILEXTXH	ILEXTXL	ILSIO0H	ILSIO0L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured a target interrupt level.
00: level 1 ; a priority is lower. (Initial value)
01: level 2
10: level 3
11: level 4 ; a priority is higher.

Bit No.	Bit Symbol Name	Description (target interrupt level)
15,14	ILTM1H, ILTM1L	16-bit Timer 1 interrupt (TM1INT)
13,12	ILTM0H, ILTM0L	16-bit Timer 0 interrupt (TM0INT)
11,10	ILFTM1H, ILFTM1L	Functional timer 1 interrupt (FTM1INT)
9,8	ILFTM0H, ILFTM0L	Functional timer 0 interrupt (FTM0INT)
7,6	ILI2CM1H, ILI2CM1L	I^2C bus master 1 interrupt (I2CM1INT)
5,4	ILI2CM0H, ILI2CM0L	I^2C bus master 0 interrupt (I2CM0INT)
3,2	ILEXTXH, ILEXTXL	Extended external interrupt (EXTINT)
1,0	ILSIO0H, ILSIO0L	SSIO0 interrupt (SIO0INT)

[Note]
- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**
-

5.2.17 Interrupt Level Control Register 4 (ILC4)

ILC4 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting IEL bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF03C(ILC40/ILC4), 0xF03D(ILC41)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC4															
Byte	ILC41								ILC40							
Bit	ILTM3H	ILTM3L	ILTM2H	ILTM2L	ILFTM3H	ILFTM3L	ILFTM2H	ILFTM2L	-	-	ILUA11H	ILUA11L	ILUA10H	ILUA10L	ILI2CU0H	ILI2CU0L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured a target interrupt level.
00: level 1 ; a priority is lower. (Initial value)
01: level 2
10: level 3
11: level 4 ; a priority is higher.

Bit No.	Bit symbol name	Description (target interrupt level)
15,14	ILTM3H, ILTM3L	16-bit Timer 3 interrupt (TM3INT)
13,12	ILTM2H, ILTM2L	16-bit Timer 2 interrupt (TM2INT)
11,10	ILFTM3H, ILFTM3L	Functional Timer 3 interrupt (FTM3INT)
9,8	ILFTM2H, ILFTM2L	Functional Timer 2 interrupt (FTM2INT)
7,6	-	Reserved bits
5,4	ILUA11H, ILUA11L	UART11 interrupt (UA11INT)
3,2	ILUA10H, ILUA10L	UART10 interrupt (UA10INT)
1,0	ILI2CU0H, ILI2CU0L	I^2C Bus Unit 0 interrupt (I2CU0INT)

[Note]
- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**
-

5.2.18 Interrupt Level Control Register 5 (ILC5)

ILC5 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting IEL bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF03E(ILC50/ILC5), 0xF03F(ILC51)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC5															
Byte	ILC51								ILC50							
Bit	ILTM5H	ILTM5L	ILTM4H	ILTM4L	ILFTM5H	ILFTM5L	ILFTM4H	ILFTM4L	ILVPHDH	ILVPHDL	ILVC0H	ILVC0L	ILUA21H	ILUA21L	ILUA20H	ILUA20L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured a target interrupt level.
00: level 1 ; a priority is lower. (Initial value)
01: level 2
10: level 3
11: level 4 ; a priority is higher.

Bit No.	Bit symbol name	Description (target interrupt level)
15,14	ILTM5H, ILTM5L	16-bit Timer 5 interrupt (TM5INT)
13,12	ILTM4H, ILTM4L	16-bit Timer 4 interrupt (TM4INT)
11,10	ILFTM5H, ILFTM5L	Functional Timer 5 interrupt (FTM5INT)
9,8	ILFTM4H, ILFTM4L	Functional Timer 4 interrupt (FTM4INT)
7,6	ILVPHDH, ILVPHDL	Audio PWM Hold detect interrupt (VPHDINT)
5,4	ILVC0H, ILVC0L	Audio 0 interrupt (VC0INT)
3,2	ILUA21H, ILUA21L	UART21 interrupt (UA21INT)
1,0	ILUA20H, ILUA20L	UART20 interrupt (UA20INT)

[Note]

- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**

5.2.19 Interrupt Level Control Register 6 (ILC6)

ILC6 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting ILE bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF040(ILC60/ILC6), 0xF041(ILC61)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC6															
Byte	ILC61								ILC60							
Bit	-	-	ILTM6H	ILTM6L	ILFTM7H	ILFTM7L	ILFTM6H	ILFTM6L	ILEUAH	ILEUAL	ILESIOH	ILESIOL	ILSIO2H	ILSIO2L	ILSIO1H	ILSIO1L
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description (target interrupt level)
15,14	—	Reserved bits
13,12	ILTM6H, ILTM6L	16bit Timer 6 interrupt (TM6INT)
11,10	ILFTM7H, ILFTM7L	Functional Timer 7 interrupt (FTM7INT)
9,8	ILFTM6H, ILFTM6L	Functional Timer 6 interrupt (FTM6INT)
7,6	ILEUAH, ILEUAL	Extended UART interrupt (XUAINT9)
5,4	ILESIOH, ILESIOL	Extended SIO interrupt (XSIOINT)
3,2	ILSIO2H, ILSIO2L	SSIO2 interrupt (SIO2INT)

[Note]

- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**
-

5.2.20 Interrupt Level Control Register 7 (ILC7)

ILC7 is a SFR to set the interrupt level for each maskable interrupt source.
The bits of the unavailable peripheral circuits are not writeable. They return "0" for reading.
It is writeable only when the interrupt level control is enabled by setting IEL bit of the interrupt level control enable register (ILEN) to "1".

Address: 0xF042(ILC70/ILC7), 0xF043(ILC71)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ILC7															
Byte	ILC71								ILC70							
Bit	-	-	-	-	ILLTBC2H	ILLTBC2L	ILLTBC1H	ILLTBC1L	ILLTBC3H	ILLTBC3L	ILLTBC0H	ILLTBC0L	ILTMXH	ILTMXL	-	-
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured a target interrupt level.
00: level 1 ; a priority is lower. (Initial value)
01: level 2
10: level 3
11: level 4 ; a priority is higher.

Bit No.	Bit symbol name	Description (target interrupt level)
15,14	-	Reserved bits
13,12	-	Reserved bits
11,10	ILLTBC2H, ILLTBC2L	Low speed Time base counter 2 interrupt (LTB2INT)
9,8	ILLTBC1H, ILLTBC1L	Low speed Time base counter 1 interrupt (LTB1INT)
7,6	ILLTBC3H, ILLTBC3L	Low speed Time base counter 3 interrupt (LTB3INT)
5,4	ILLTBC0H, ILLTBC0L	Low speed Time base counter 0 interrupt (LTB0INT)
3,2	ILTMXH, ILTMXL	16-bit Timer X interrupt (TMXINT)
1,0	-	Reserved bits

[Note]
- **Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.**

5.3 Description of Operation

Enabling/disabling the maskable interrupt are controllable d by the master interrupt enable flag (MIE) of the CPU and each interrupt enable register (IE1 to 7).
A WDT interrupt (WDTINT) is unavailable to disable as it is a non-maskable interrupt.
When interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt transfer cycle starts to branch to the interrupt processing routine.

If multiple interrupts are generated concurrently when the interrupt level control function is disabled, they are processed starting from the interrupt with the highest priority (with a smallest interrupt source number). The lower- priority interrupts (with larger interrupt source numbers) remain pending.
If multiple interrupts are generated concurrently when the interrupt level control function is enabled, they are processed starting from the interrupt with both the highest interrupt level and the highest priority level. The lower- priority interrupts remain pending.

Table 5-2 lists the interrupt sources.
The interrupt vector address is an address of the interrupt vector defined in the program memory. See "nX-U16/100 Core Instruction Manual" for details of the interrupt vector address.

Table 5-2 List of interrupt sources

Interrupt source number (priority)	Register assignment			Interrupt vector address	Mask	External /internal source	Interrupt source	Symbol
	IRQ (interrupt request)	IE (interrupt enable)	ILC (interrupt level)					
1(high)	IRQ0[0]	-	-	0x0008	Disabled	Internal	WDT interrupt	WDTINT
2	-	-	-	0x000A	Disabled		-	-
3	IRQ0[6]	IE0[6]	ILC0[13:12]	0x000C	Enabled		VLS0 interrupt	VLS0INT
4	IRQ0[7]	IE0[7]	ILC0[15:14]	0x000E	Enabled		-	-
5	IRQ1[0]	IE1[0]	ILC1[1:0]	0x0010	Enabled	External	External interrupt 0	EXI0INT
6	IRQ1[1]	IE1[1]	ILC1[3:2]	0x0012	Enabled		External interrupt 1	EXI1INT
7	IRQ1[2]	IE1[2]	ILC1[5:4]	0x0014	Enabled		External interrupt 2	EXI2INT
8	IRQ1[3]	IE1[3]	ILC1[7:6]	0x0016	Enabled		External interrupt 3	EXI3INT
9	IRQ1[4]	IE1[4]	ILC1[9:8]	0x0018	Enabled		External interrupt 4	EXI4INT
10	IRQ1[5]	IE1[5]	ILC1[11:10]	0x001A	Enabled		External interrupt 5	EXI5INT
11	IRQ1[6]	IE1[6]	ILC1[13:12]	0x001C	Enabled		External interrupt 6	EXI6INT
12	IRQ1[7]	IE1[7]	ILC1[15:14]	0x001E	Enabled		External interrupt 7	EXI7INT
13	IRQ2[0]	IE2[0]	ILC2[1:0]	0x0020	Enabled	Internal	Clock backup interrupt	CBUINT
14	IRQ2[1]	IE2[1]	ILC2[3:2]	0x0022	Enabled		-	-
15	IRQ2[2]	IE2[2]	ILC2[5:4]	0x0024	Enabled		MCU status interrupt*1	MCSINT
16	IRQ2[3]	IE2[3]	ILC2[7:6]	0x0026	Enabled		UART00 interrupt	UA00INT
17	IRQ2[4]	IE2[4]	ILC2[9:8]	0x0028	Enabled		UART01 interrupt	UA01INT
18	IRQ2[5]	IE2[5]	ILC2[11:10]	0x002A	Enabled		-	-
19	IRQ2[6]	IE2[6]	ILC2[13:12]	0x002C	Enabled		SA-ADC interrupt	SADINT
20	IRQ2[7]	IE2[7]	ILC2[15:14]	0x002E	Enabled		SSIOF0 interrupt	SIOF0INT
21	IRQ3[0]	IE3[0]	ILC3[1:0]	0x0030	Enabled	Internal	SSIO0 interrupt	SIO0INT
22	IRQ3[1]	IE3[1]	ILC3[3:2]	0x0032	Enabled		Extended External interrupt	EXTINT
23	IRQ3[2]	IE3[2]	ILC3[5:4]	0x0034	Enabled		I^2C bus master 0 interrupt	I2CM0INT
24	IRQ3[3]	IE3[3]	ILC3[7:6]	0x0036	Enabled		I^2C bus master 1 interrupt	I2CM1INT
25	IRQ3[4]	IE3[4]	ILC3[9:8]	0x0038	Enabled		Functional Timer 0 interrupt	FTM0INT
26	IRQ3[5]	IE3[5]	ILC3[11:10]	0x003A	Enabled		Functional Timer 1 interrupt	FTM1INT
27	IRQ3[6]	IE3[6]	ILC3[13:12]	0x003C	Enabled		16-bit Timer 0 interrupt	TM0INT
28	IRQ3[7]	IE3[7]	ILC3[15:14]	0x003E	Enabled		16-bit Timer 1 interrupt	TM1INT
29	IRQ4[0]	IE4[0]	ILC4[1:0]	0x0040	Enabled	Internal	I^2C bus unit interrupt	I2CU0INT
30	IRQ4[1]	IE4[1]	ILC4[3:2]	0x0042	Enabled		UART10 interrupt	UA10INT
31	IRQ4[2]	IE4[2]	ILC4[5:4]	0x0044	Enabled		UART11 interrupt	UA11INT
32	IRQ4[3]	IE4[3]	ILC4[7:6]	0x0046	Enabled		-	-
33	IRQ4[4]	IE4[4]	ILC4[9:8]	0x0048	Enabled		Functional Timer 2 interrupt	FTM2INT
34	IRQ4[5]	IE4[5]	ILC4[11:10]	0x004A	Enabled		Functional Timer 1 interrupt	FTM1INT
35	IRQ4[6]	IE4[6]	ILC4[13:12]	0x004C	Enabled		16-bit Timer 2 interrupt	TM2INT
36	IRQ4[7]	IE4[7]	ILC4[15:14]	0x004E	Enabled		16-bit Timer 3 interrupt	TM3INT

Interrupt source number (priority)	Register assignment			Interrupt vector address	Mask	External /internal source	Interrupt source	Symbol
	IRQ (interrupt request)	IE (interrupt enable)	ILC (interrupt level)					
37	IRQ5[0]	IE5[0]	ILC5[1:0]	0x0050	Enabled	Internal	UART20 interrupt	UA20INT
38	IRQ5[1]	IE5[1]	ILC5[3:2]	0x0052	Enabled		UART21 interrupt	UA21INT
39	IRQ5[2]	IE5[2]	ILC5[5:4]	0x0054	Enabled		Audio 0 interrupt	VC0INT
40	IRQ5[3]	IE5[3]	ILC5[7:6]	0x0056	Enabled		Audio Hold Detection interrupt	VPHDINT
41	IRQ5[4]	IE5[4]	ILC5[9:8]	0x0058	Enabled		Functional Timer 4 interrupt	FTM4INT
42	IRQ5[5]	IE5[5]	ILC5[11:10]	0x005A	Enabled		Functional Timer 5 interrupt	FTM5INT
43	IRQ5[6]	IE5[6]	ILC5[13:12]	0x005C	Enabled		16-bit Timer 4 interrupt	TM4INT
44	IRQ5[7]	IE5[7]	ILC5[15:14]	0x005E	Enabled		16-bit Timer 5 interrupt	TM5INT
45	IRQ6[0]	IE6[0]	ILC6[1:0]	0x0060	Enabled	Internal	SSIO1 interrupt	SIO1INT
46	IRQ6[1]	IE6[1]	ILC6[3:2]	0x0062	Enabled		SSIO2 interrupt	SIO2INT
47	IRQ6[2]	IE6[2]	ILC6[5:4]	0x0064	Enabled		Extended SIO interrupt	XSIOINT
48	IRQ6[3]	IE6[3]	ILC6[7:6]	0x0066	Enabled		Extended UART interrupt	XUAINT
49	IRQ6[4]	IE6[4]	ILC6[9:8]	0x0068	Enabled		Functional timer 6 interrupt	FTM6INT
50	IRQ6[5]	IE6[5]	ILC6[11:10]	0x006A	Enabled		Functional timer 7 interrupt	FTM7INT
51	IRQ6[6]	IE6[6]	ILC6[13:12]	0x006C	Enabled		16 bit timer 6 interrupt	TM6INT
52	IRQ6[7]	IE6[7]	ILC6[15:14]	0x006E	Enabled		-	-
53	IRQ7[0]	IE7[0]	ILC7[1:0]	0x0070	Enabled	Internal	-	-
54	IRQ7[1]	IE7[1]	ILC7[3:2]	0x0072	Enabled		16-bit Timer X interrupt	TMXINT
55	IRQ7[2]	IE7[2]	ILC7[5:4]	0x0074	Enabled		Low speed time base counter 0 interrupt	LTB0INT
56	IRQ7[3]	IE7[3]	ILC7[7:6]	0x0076	Enabled		Low speed timer base counter 3 interrupt	LTB3INT
57	IRQ7[4]	IE7[4]	ILC7[9:8]	0x0078	Enabled		Low speed timer base counter 1 interrupt	LTB1INT
58	IRQ7[5]	IE7[5]	ILC7[11:10]	0x007A	Enabled		Low speed timer base counter 2 interrupt	LTB2INT
59	IRQ7[6]	IE7[6]	ILC7[13:12]	0x007C	Enabled		-	-
60(Low)	IRQ7[7]	IE7[7]	ILC7[15:14]	0x007E	Enabled		-	-

*1 The MCU status interrupt occurs when the following request is asserted.

- RAM parity error
- Automatic CRC calculation completion
- Data flash erasing/programming completion

These requests are configurable to enable/disable. See Chapter 29 “Safety Function” for detail.

[Note]

- **The WDT interrupt (WDTINT) is a non-maskable interrupt. If the non-maskable interrupt occurs while an interrupt processing is in progress, abort the interrupt processing and proceed with processing the non-maskable interrupt preferentially regardless of multiple interrupts enabled/disabled.**
- **For failsafe, define unused all interrupt vectors. If an unused interrupt occurs, it may indicate the possibility that the CPU went out of control. It is recommended to cause the WDT overflow reset to occur using the infinite loop to initialize the LSI.**

5.3.1 Maskable Interrupt Processing

When each interrupt occurs with the MIE set to "1", the following processing is executed by the hardware and the interrupt processing is shifted.

1. Save the program counter (PC) in ELR1.
2. Save CSR in ECSR1 (not processed if the program memory size is 64 Kbytes or less).
3. Save PSW in EPSW1.
4. Set ELEVEL of PSW to "1".
5. Reset the MIE flag to "0".
6. Set CSR to "0" (not processed if the program memory size is 64 Kbytes or less).
7. Transfer the value of the interrupt vector address to the program counter (PC).

5.3.2 Non-Maskable Interrupt Processing

When an interrupt occurs, the following process is executed by hardware and the CPU goes to the interrupt routine regardless of the value of MIE.

1. Save the program counter (PC) in ELR2.
2. Save CSR in ECSR2 (not processed if the program memory size is 64 Kbytes or less).
3. Save PSW fin EPSW2.
4. Set ELEVEL of PSW to "2".
5. Set CSR to "0" (not processed if the program memory size is 64 Kbytes or less).
6. Transfer the value of the interrupt vector address to the program counter (PC).

5.3.3 Software Interrupt Processing

The software interrupt is arbitrarily produced in software.
When the SWI instruction is performed within the software, a software interrupt occurs, and then the following process is performed by hardware, and the CPU goes to the software interrupt routine. The vector table is specified with the SWI instruction.

1. Save the program counter (PC) in ELR1.
2. Save CSR in ECSR1 (not processed if the program memory size is 64 Kbytes or less).
3. Save PSW in EPSW1.
4. Set ELEVEL of PSW to "1".
5. Set the MIE flag to "0".
6. Set CSR to "0" (not processed if the program memory size is 64 Kbytes or less).
7. Transfer the value of the interrupt vector address to the program counter (PC).

See "nX-U16/100 Core Instruction Manual" for MIE, the program counter (PC), ELR1, CSR, ECSR1, PSW, EPSW1, ELEVEL, ELR2, ECSR2, EPSW2 and vector table.

5.3.4 Notes on Interrupt Routine (with Interrupt Level Control Disabled)

The interrupt level control is disabled when writing "0" to the ILE bit of the interrupt level control enable register (ILEN).
The description below shows notes on each of the following states when the interrupt level control is not in use.

- When the sub routine is called/not called in the interrupt routine while the maskable interrupt is processing (defined as State A).
- When the sub routine is called/not called in the interrupt routine while the non-maskable interrupt is processing (defined as State B).

State A: Maskable interrupt is processing

A-1: In case of a subroutine is not called in the interrupt routine

A-1-1: in case of multiple interrupts are disabled

- Script is written in assembly language
  - Processing right after the start of interrupt routine execution
    No specific notes.
  - Processing at the end of interrupt routine execution
    Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.
- Script is written in C
  - Define the interrupt routine using the INTERRUPT pragma. Specify "1" in the category field. In this way, appropriate codes are produced through the C compiler.

Example of description: State A-1-1

For assembly language:

```
Intrpt_A-1-1;                ; State of A-1-1
DI                           ; Disable interrupt
  :
  :
  :
RTI                          ; Return PC from ELR
                             ; Return PSW form EPSW
                             ; End of interrupt routine
```

For C language:

```
static void Intrpt_A_1_1(void);
#pragma interrupt Intrpt_A_1_1 0x10 1
static void Intrpt_A_1_1(void)
{
_DI();                  /* Disable interrupt */
  :
}                       /* End of interrupt routine */
```

A-1-2: In case of multiple interrupts are enabled

- Script is written in the assembly language
  - Processing right after the start of interrupt routine execution
    Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
  - Processing at the end of interrupt routine execution
    Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.
- Script is written in C
  - Define the interrupt routine using the INTERRUPT pragma. Specify "2" in the category field. In this way, appropriate codes are produced through the C compiler.

Example of description: State A-1-2

For assembly language:

```
Intrpt_A-1-2;                ; Start
PUSH ELR, EPSW               ; Save ELR and EPSW at the beginning
  :
  :
EI                           ; Enable interrupt
  :
POP PSW, PC                  ; Return PC from the stack
                             ; Return PSW from the stack
                             ; End of interrupt routine
```

For C language:

```
static void Intrpt_A_1_2(void);
#pragma interrupt Intrpt_A_1_2 0x20 2
static void Intrpt_A_1_2(void)
{
_EI();                  /* Enable interrupt */
  :
}                       /* End of interrupt routine */
```

A-2: In case of subroutine is called in an interrupt routine

A-2-1: In case of multiple interrupts are disabled

•Script is written in the assembly language

- Processing immediately after the start of interrupt routine execution
  Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
- Processing at the end of interrupt routine execution
  Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

• Script is written in C

- Define the interrupt routine using the INTERRUPT pragma. Specify "1" in the category field. In this way, appropriate codes are produced through the C compiler.

Example of description: State A-2-1

For assembly language:

```
Intrpt_A-2-1;              ; Start
PUSH   LR                  ; Save ELR, EPSW, and LR at
                             the beginning
  :
  :
BL Sub_1                   ; Call subroutine Sub_1
  :
POP LR                     ; Return LR from the stack
RTI                        ; End of interrupt routine
```

```
Sub_1;          ;

RT              ; Return PC from LR
                ; End of subroutine
```

For C language:

```
static void Intrpt_A_2_1(void);
#pragma interrupt Intrpt_A_2_1 0x12 1
static void Intrpt_A_2_1(void)
{
  :
Sub_1();            /* Call subroutine Sub_1 */
  :
}                       /* End of interrupt routine */
```

```
void Sub_1(void)
{
:
:
}           /* End of subroutine */
```

[Note]

- **Do not enable interrupts in a subroutine called from an interrupt routine for which multiple interrupts are disabled. Otherwise, the program may runaway when multiple interrupts occur.**

A-2-2: In case of multiple interrupts are enabled

- Script is written in the assembly language
  - Processing immediately after the start of interrupt routine execution
    Specify "PUSH LR, ELR, EPSW, LR" to save the interrupt return address, the subroutine return address, and the EPSW1 status in the stack.
  - Processing at the end of interrupt routine execution
    Specify "POP PSW, PC, LR", instead of the RTI instruction, to return the saved data of the interrupt return address to PC, the saved data of EPSW1 to PSW, and the saved data of LR to LR.
- Script is written in C
  - Define the interrupt routine using the INTERRUPT pragma. Specify "2" in the category field. In this way, appropriate codes are produced through the C compiler.

Example of description: Status A-2-2

For assembly language:

```
Intrpt_A-2-2;                ; Start
PUSH ELR, EPSW, LR           ; Save ELR, EPSW, and LR at the beginning
  :
EI                           ; Enable interrupt
  :
  :
  :
BL Sub_1                     ; Call subroutine Sub_1
  :
POP PSW, PC, LR              ; Return PC from the stack
                             ; Return PSW from the stack
                             ; Return LR from the stack
                             ; End of interrupt routine
```

```
Sub_1;          ;
DI              ; Disable interrupt
  :               :
EI              ; Enable interrupt
RT              ; Return PC from LR
                ; End of subroutine
```

For C language:

```
static void Intrpt_A_2_2(void);
#pragma interrupt Intrpt_A_2_2 0x22 2
static void Intrpt_A_2_2(void)
{
  :
_EI();                  /* Enable interrupt */
  :
Sub_1();              /* Call subroutine Sub_1 */
  :
}                       /* End of interrupt routine */
```

```
void Sub_1(void)
{
_DI();          /* Disable interrupt */
  :
_EI();          /* Enable interrupt */
}               /* End of subroutine */
```

State B: Non-maskable interrupt is being processed

B-1: In case of subroutine is not called in an interrupt routine

- Script is written in the assembly language
  - Processing right after the start of interrupt routine execution
    Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
  - Processing at the end of interrupt routine execution
    Specify "POP PSW, PC" to return the contents of the stack to PC and PSW.
- Script is written in C
  Define the interrupt routine using the INTERRUPT pragma. Specify "2" in the category field. In this way, appropriate codes are produced through the C compiler.

Example of description: Status B-1

For assembly language:

```
Intrpt_B-1;                 ; Status B-1
PUSH ELR, EPSW              ; Save ELR and EPSW at the
                              beginning
  :
  :
POP PSW, PC                 ; Return PC from the stack
                            ; Return PSW from the stack
                            ; Return LR from the stack
                            ; End of interrupt routine
```

For C language:

```
static void Intrpt_B_1(void);
#pragma interrupt Intrpt_B_1 0x08 2
static void Intrpt_B_1(void)
{
  :
}                           /* End of interrupt routine */
```

B-2: In case of subroutine is called in an interrupt routine

- Script is written in the assembly language
  - ➢ Processing immediately after the start of interrupt routine execution
    Specify "PUSH ELR, EPSW, LR" to save the interrupt return address, the subroutine return address, and EPSW status in the stack.
  - ➢ Processing at the end of interrupt routine execution
    Specify "POP PSW, PC, LR" to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.
- Script is written in C
  - ➢ Define the interrupt routine by using INTERRUPT pragma and specify "2" in the category field. The C compiler generates the proper codes.

Example of description: Status B-2

For assembly language:

```
Intrpt_B-2;                 ; Start
  PUSH ELR, EPSW, LR        ; Save ELR, EPSW, and LR at
                              the beginning
   :
   :
BL Sub_1                    ; Call subroutine Sub_1
   :
POP PSW, PC, LR             ; Return PC from the stack
                            ; Return PSW from the stack
                            ; Return LR from the stack
                            ; End
```

```
Sub_1;


RT              ; Return PC from LR
                ; End of subroutine
```

For C language:

```
static void Intrpt_B_2(void);
#pragma interrupt Intrpt_B_2 0x08 2
static void Intrpt_B_2(void)
{
   :
Sub_1();            /* Call subroutine Sub_1 */
   :
}                   /* End of interrupt routine */
```

```
void Sub_1(void)
{
   :
   :
}           /* End of subroutine */
```

5.3.5 Flow Charts When Interrupt Level Control Is Enabled

Figure 5-1 shows flow charts of the software interrupt processing when multiple interrupts are disabled and enabled respectively with the interrupt level control enabled.
When multiple interrupts are enabled, save ELR1, ECSR (not processed for products with 64 Kbytes or less of program memory) and EPSW1 in the stack (RAM) so that they are not overwritten by the multiple interrupt. In addition, the EI and DI instructions enable the execution of multiple interrupts due to a high-level maskable interrupt request while "execution of the target process" is in progress.
If a non-maskable interrupt is occurred while the maskable interrupt is being processed, the transition to non-maskable interrupt takes place regardless of multiple interrupts enabled/disabled and the execution of the EI instruction.

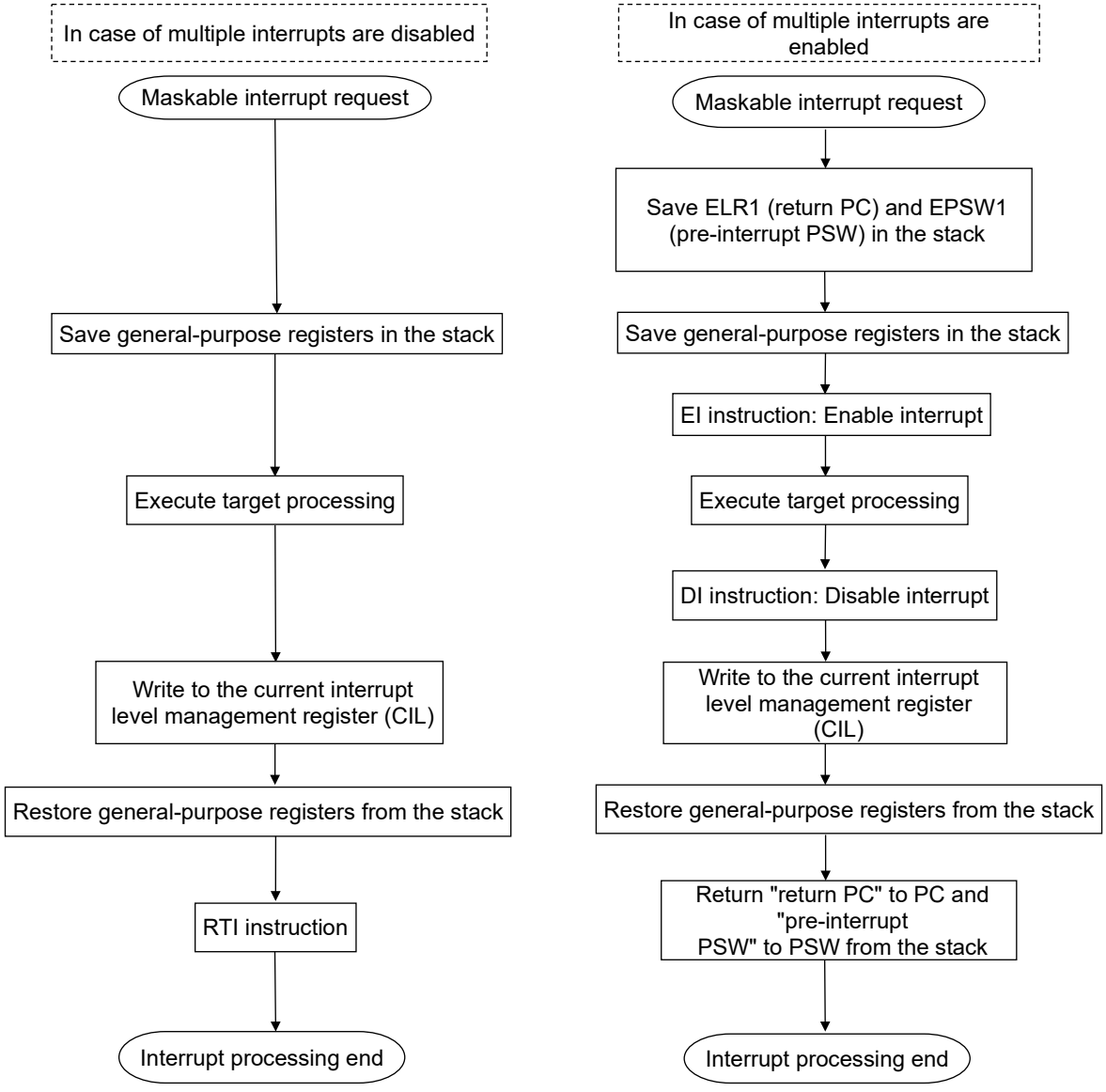


Figure 5-1 Maskable Interrupt Processing Flow

[Note]

- **For processing of non-maskable interrupt, follow the flow chart "In case of multiple interrupts are enabled". Registers that should be saved in the stack are ELR2 and EPSW2.**
- **When programming in C, it is not required to write program codes for saving/restoring registers because they are generated in the C compiler. However, program codes for enabling/disabling interrupts through EI and DI instructions and for writing to the current interrupt level management register (CIL) must be written. See Section 5.3.6 " How To describe Interrupt Processing When Interrupt Level Control Enabled" for the specific program description.**

5.3.6 How To describe Interrupt Processing When Interrupt Level Control Enabled

This section describes examples of program scripts of interrupt function when ILE of the interrupt level control enable register (ILEN) is set to enable the interrupt level control. See the programming guide of the C compiler for the detailed scripting method of and notes on interrupt processing.

5.3.6.1 Description of Interrupt Function to Disable Multiple Interrupts

To describe the interrupt function to disable multiple interrupts, specify 1 in the category field of the INTERRUPT pragma and SWI pragma. When built-in function _EI is called in the interrupt function to disable multiple interrupts, the C compiler displays an error.
After completion of the target interrupt processing, it is necessary to write to the CIL register and clear the highest current interrupt request level (CILMn bit) to "0". Otherwise, interrupts equivalent to or less than the current interrupt request level is unacceptable.

Example of description

```
static void intr_fn_0A (void);
#pragma interrupt intr_fn_0A 0x0A 1
volatile unsigned short TM1msec;
static void intr_fn_0A (void)
{
        TM1msec++;
        CIL = 0;    /*Clear the highest current interrupt request level*/
}
```

When described as in the example, intr_fn_0A is handled as an interrupt processing function to disable multiple interrupts. the C compiler outputs the assembly code as shown below.

Example of output

```
_intr_fn_0A       :
        push    er0
;;      TM1msec++;
        l       er0,      NEAR _TM1msec
        add     er0,       #1
        st      er0,       NEAR _TM1msec
;;}
;;      CIL = 0;
        mov     r0,        #00h
        st          r0,        0f022h
;;}
        pop     er0
        rti
```

In the interrupt function, the register (here, only ER0) that may be used in the interrupt routine is saved in the stack. "RTI" instruction is used to return from the interrupt function to disable multiple interrupts.
The example below shows how to call other functions from an interrupt function.

```
Example of description
  static void intr_fn_10 (void);
  #pragma interrupt intr_fn_10 0x10 1
  void func (void);
  static void intr_fn_10 (void)
  {
          func ( );
       CIL = 0;    /*Clear the highest current interrupt request level*/
  }

Example of output
  _intr_fn_10       :
      push    lr,     ea
      push    xr0
      l       r0,       DSR
      push    r0

  ;;  func();
      bl      _func

  ;;}
  ;;  CIL = 0;
      mov     r0,   #00h
      st      r0,   0f022h
  ;;}
      pop     r0
      st      r0,   DSR
      pop     xr0
      pop     ea,   lr
      rti
```

When another function is called from an interrupt function, the output code becomes redundant compared with the case where another function is not called from the interrupt function. Thus the processing time of the interrupt becomes also longer. This is because the C compiler does not know which registers the function func ( ) should use and it save the all registers that may be changed by calling the func ( ) in the stack.

[Note]

- **Do not enable interrupts in a function called from a function for which multiple interrupts are disabled. Otherwise, the program may run out of control when the multiple interrupts occur.**

5.3.6.2 Description of Interrupt Function to Enable Multiple Interrupts

When describing an interrupt function to enable multiple interrupts, specify "2" in the category field in INTERRUPT pragma and SWI pragma. Even if it is not specified in the category field, multiple interrupt are enabled. Built-in function _EI can be called in an interrupt function to enable multiple interrupts.

Example of description

```
static void intr_fn_20 (void);
volatile unsigned short TM2msec;
#pragma interrupt intr_fn_20 0x20 2
static void intr_fn_20 (void)
{
    _EI( );          /*Enable multiple interrupts*/
    TM2msec++;
    _DI( );          /*Disable multiple interrupts*/
    CIL = 0;         /*Clear the highest current interrupt request level*/
}
```

If described as in the example, intr_fn_20 ( ) is handled as an interrupt processing function to enable multiple interrupts. the C compiler outputs the assembly code as shown below.

Example of output

```
_intr_fn_20        :
    push    elr,   epsw
    push    er0

;;      _EI( );          /*Enable multiple interrupts*/
    ei

;;      TM1msec++;
    l       er0,  NEAR _TM2msec
    add     er0,  #1
    st      er0,  NEAR _TM2msec
;;      _DI( );      /*Disable multiple interrupts*/
    di
;;}
;;      CIL = 0;
    mov     r0,       #00h
    st      r0,       0f022h
;;}
    pop     er0
    pop         psw, pc
```

In an interrupt function to enable multiple interrupts, ELR and EPSW are saved in the stack so that they should not be destroyed by multiple interrupts. This is the difference from the interrupt function to disable multiple interrupts. To return from the interrupt function, "POP PSW, PC" is used instead of "RTI".

5.3.7 Interrupt Disable State

The interrupt disable state refers to an operating state where no interrupt is accepted even if the interrupt conditions are satisfied.
The following describes the interrupt disabled state and operation of interrupts in the situation.

State 1. Between the interrupt transfer cycle and the instruction at the beginning of the interrupt routine
When the interrupt conditions are satisfied here, an interrupt is generated immediately after the execution of the instruction at the beginning of the interrupt routine that corresponds to the interrupt already enabled.

State 2. Between the DSR prefix code and the next instruction
When the interrupt conditions are satisfied here, an interrupt is generated immediately after execution of the instruction following the DSR prefix code.

See "nX-U16/100 Core Instruction Manual" for the DSR prefix instruction.

5.3.8 Writing to IRQ01/IRQ23/IRQ45/IRQ67

Use the bit symbol to write to IRQ01/IRQ23/IRQ45/IRQ67 register.
The example below shows how to write "0" to the bit symbol QLTBC0.

Example of description

```
#define clear_bit(n)          ((n)) = 0)

clear bit (QLTBC0);
```

* "n" is the bit symbol name of user's manual.

Chapter 6 Clock generation Circuit

6. Clock Generation Circuit

6.1 General Description

The clock generation circuit generates following clocks and supplies them to the CPU and the peripheral circuits.

Table 6-1 Source Clocks

Clock Name	Symbol	Frequency	Description
Internal low-speed oscillation clock	RC32K	32.768kHz	Internal generated RC oscillating low-speed clock.
Crystal oscillation low-speed clock	XT32K	32.768kHz	low-speed clock with an external crystal unit.
External input low-speed clock input	EXT32K	32.768kHz	External low-speed clock input from XT1
Internal 1kHz clock	RC1K	1.024kHz	Internal generated RC oscillating clock (1.024 kHz) for WDTCLK and clock mutual monitor.
Internal high-speed clock	PLL	-	high-speed clock multiplied from LSCLK0. The frequencies selected from 1/16/24MHz by the code option.
	PLL24M	24.002560MHz	Multiplied by 732.5
	PLL16M	16.007168MHz	Multiplied by 488.5
	PLL1M	0.999424MHz	Multiplied by 30.5

Table 6-2 Clocks generated by the clock generation circuit

Clock Name	Symbol	Frequency	Description
Low speed clock 0	LSCLK0	32.768kHz	Supplies to system and peripheral circuits.
Low speed clock 1	LSCLK1	32.768kHz	Supplies to timer and LTBC.
Low speed clock output	LCKO	32.768kHz	Output LSCLK0 orLSCLK1 to port
High speed source clock	HSOCLK	1/16/24MHz	Supply to SA-ADC.
High speed clock	HSCLK	0.125 to 24MHz	Divided clock of HSOCLK. Supply to system and peripheral circuits.
High speed time base clock 0/1	HTBCLK0 HTBCLK1	HSCLK/1 to 8	Divided clock of HSCLK by 1, 2, 3, 4, 5, 6, 7, and 8. 2 channels. Supply to peripheral circuits.
High speed clock output	HCKO	0.125 to 8MHz	Divided clock of HSOCLK for Port output
System clock	SYSCLK	32.768kHz/ 0.125 to 24MHz	For system clock. selected from LSCLK0 or divided HSCLK. Supply to system and communication circuits. LSCLK is selected at start-up.
CPU clock	CPUCLK	SYSCLK	Supply to CPU. The clock is stopped during stand-by mode.
WDT clock	WDTCLK	1.024kHz	Supply to watchdog timer.
Audio playback function clock	VCLK	16MHz	Supply to Audio playback function circuit

6.1.1 Features

- Low-speed clock
  - Low-speed RC oscillation circuit
  - A crystal resonator is connectable
  - In case the low-speed crystal oscillation stopped, the clock is automatically switched to the low-speed RC oscillation (clock backup function).
  - low-speed external clock can be input to XT1 pin.
  - Selectable a clock different from system clock as timer clock.
  - Configurable stability time of crystal oscillation by the timer X.
- High-speed clock
  - Selectable PLL oscillation frequency from 1,16, and 24MHz by code option.
  - Selectable High-speed clock wake-up time
  - High-speed time base clock circuit that is divided HSCLK by 1 to 8; it is with 2 channels.
  - Equipped with 2 high-speed timebase counter circuits that divide HSCLK by 1/1~1/8
- WDT clock
  RC 1kHz oscillation circuit for WDT independent from system clock.

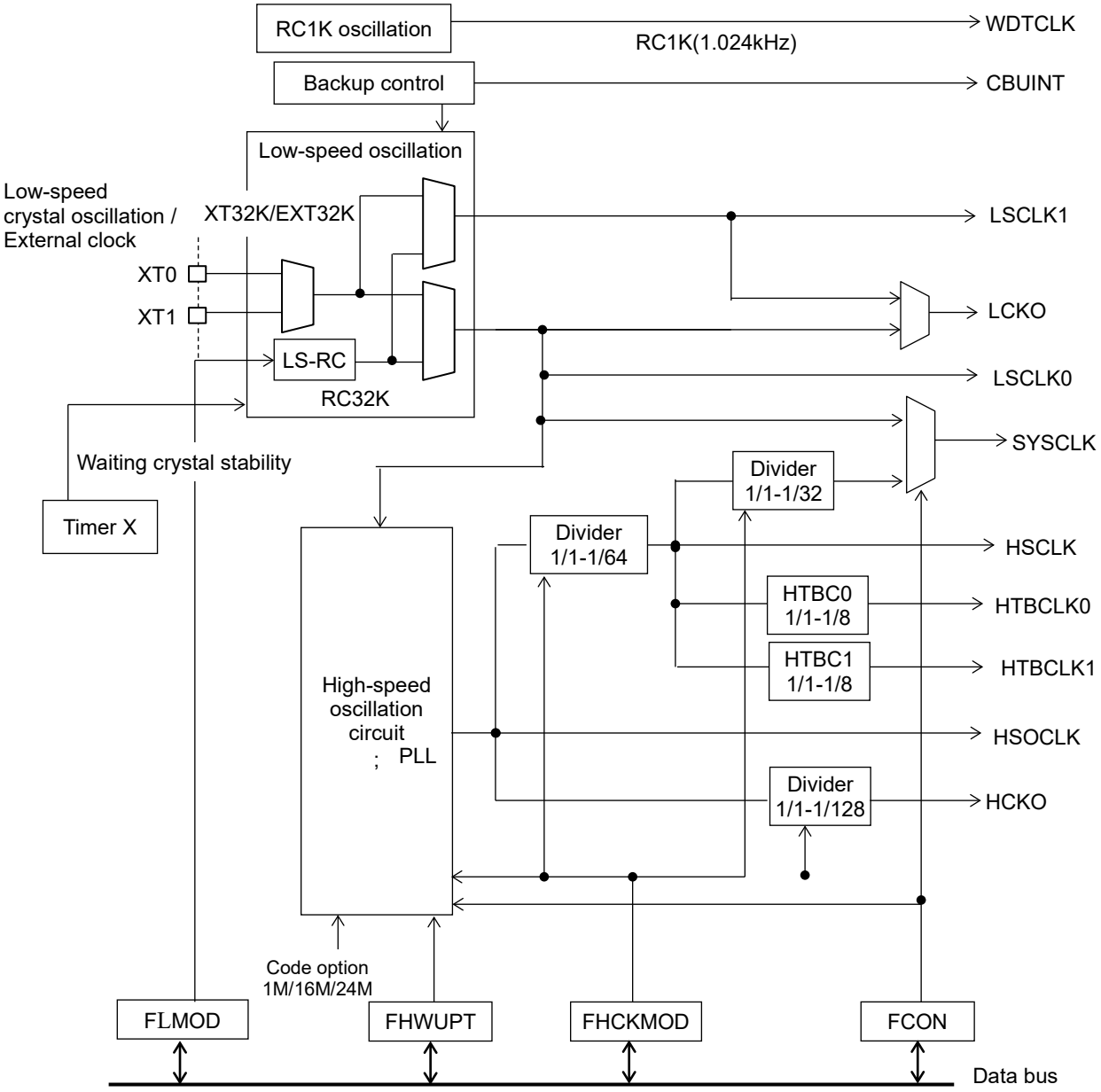
Table 6-3 shows relation of high-speed clocks and PLL frequency.
The CPU operation mode and the PLL oscillation reference frequency are selectable by the code option.
See Chapter 30 "Code Option" for more details.

Table 6-3 Frequency range for high-speed clock operation

PLL	Maximum operating frequency				output frequency (maximum)
	HSOCLK	HSCLK	SYSCLK		HCKO
			Wait mode	No wait mode	
24MHz	24MHz	0.375 to 24MHz	0.125-24MHz	0.125-6MHz	6MHz
16MHz	16MHz	0.250 to 16MHz	0.125-16MHz	0.125-8MHz	8MHz
1MHz	1MHz	0.125-1MHz	0.125-1MHz	0.125-1MHz	1MHz

6.1.2 Configuration

Figure 6-1 shows the configuration of the clock generation circuit.
Table 6-4 shows the list of operation clocks for each function.



FLMOD, FHCKMOD, FHWUPT, FCON : SFRs for control.
CBUINT*1 : Clock backup interrupt register

Figure 6-1 Configuration of Clock Generation Circuit

Table 6-4 Operating clock list in each function

Function	SYSCLK	LSCLK0	LSCLK1	HSCLK	HSOCLK	HTBCLK0	HTBCLK1	WDTCLK	VCLK
CPU/Data bus/CRC	●	-	-	-	-	-	-	-	-
RAM	●	-	-	-	-	-	-	-	-
Watchdog timer	-	-	-	-	-	-	-	●	-
External interrupt control	-	●*1	-	●*1	-	-	●*1	-	-
Low-speed time base counter	-	●	●	-	-	-	-	-	-
16-bit timer 0-4	-	●	●	●	-	●	●	-	-
16-bit timer X	-	●	●	●	-	●	●	-	-
Functional timer	-	●	-	●	-	●	●	-	-
SSIO	●	-	-	-	-	-	-	-	-
SSIOF	●	-	-	-	-	-	-	-	-
UART	●	●	-	●	-	-	-	-	-
I^2C bus unit I^2C bus master	●	-	-	-	-	-	-	-	-
SA type A/D converter	-	●	-	-	●	-	-	-	-
VLS	-	●*1	-	-	-	-	-	-	-
LCD driver	-	●	-	-	-	-	-	-	-
Audio playback function	●	-	-	-	-	-	-	-	●

● : supplied. - : not supplied.
*1 : for controlling to start or sampling.

[Note]
- **After power-on or system reset, LSCLK0 (32.768 kHz) is initially selected as SYSCLK.**

6.1.3 List of Pins

The output pins of the high-speed/low-speed clocks are assigned to the shared function of general purpose ports. Table 6-5 shows the list of the output ports and the register setting.

Pin name	I/O	Function
LCKO	O	Low-speed clock output
HCKO	O	High-speed clock output
XT0	I	Low-speed crystal resonator connect pin
XT1	O/I	Low-speed crystal resonator connect pin / Low-speed external clock input pin

Table 6-5 Clock output function port and the register setting

Pin name	Shared port		Setting register	Setting value	ML62Q2700 group
LCKO	P02	7th function	P0MOD2	0110_XXXX[*1]	●
	P21	7th function	P2MOD2	0110_XXXX[*1]	●
HCKO	P03	7th function	P0MOD3	0110_XXXX[*1]	●
	P22	7th function	P2MOD2	0110_XXXX[*1]	●

[*1] : XXXX determines the port output condition

XXXX	Port output condition
0010	CMOS output
1010	Nch open drain (without pull-up)
1111	Nch open drain (with pull-up)

[Note]

- **Assign HCKO function to one LSI pin only.**

6.2 Description of Registers

6.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF002	High-speed clock mode register	FHCKMODL	FHCKMOD	R/W	8/16	0x00
0xF003		FHCKMODH		R/W	8	0x43
0xF004	Low-speed clock mode register	FLMODL	FLMOD	R/W	8/16	0x00
0xF005		FLMODH		R/W	8	0x00
0xF006	Clock control register	FCON	FCONW	R/W	8/16	0x00
0xF007		FCON1	-	R/W	8	0x00
0xF008	Wake up time setting register for High-speed clock	FHWUPT	-	R/W	8	0x00
0xF009	Reserved	-	-	-	-	-
0xF00A	Reserved	-	-	-	-	-
0xF00B	Reserved	-	-	-	-	-
0xF00C	Backup Clock Status register	FBUSTAT	FBUSTATW	R/W	8/16	0x01
0xF00D		FBUSTATH	-	R	8	0x01
0xF080	Reserved	-	-	-	-	-
0xF086	High speed time base clock setting register	HTBDR	-	R/W	8	0x00
0xF087	Reserved	-	-	-	-	-
0xF0C4	Clock backup test mode acceptor	FBTACP	-	W	8	0x00
0xF0C5	Reserved	-	-	-	-	-
0xF0C6	Clock backup test mode register	FBTCON	-	R/W	8	0x00
0xF0C7	Reserved	-	-	-	-	-

6.2.2 High-Speed Clock Mode Register (FHCKMOD)

FHCKMOD is a SFR to select a PLL oscillation mode and the frequency.

Address : 0xF002(FHCKMODL/FHCKMOD), 0xF003(FHCKMODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x4300

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FHCKMOD															
Byte	FHCKMODH								FHCKMODL							
Bit	-	OUTC2	OUTC1	OUTC0	-	SYSC2	SYSC1	SYSC0	-	HSC2	HSC1	HSC0	-	-	-	-
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R
Initial value	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	-	Reserved bit
14 to 12	OUTC2 to OUTC0	Select divisions ratio of HCKO frequency. This clock frequencies is limited 8MHz or lower. 000 : HSOCLK 001 : 1/2 HSOCLK 010 : 1/4 HSOCLK 011 : 1/8 HSOCLK 100 : 1/16 HSOCLK (Initial value) 101 : 1/32 HSOCLK 110 : 1/64 HSOCLK 111 : 1/128 HSOCLK
11	-	Reserved bit
10 to 8	SYSC2 to SYSC0	Set frequency of high-speed system clock. SYSC2 bit is not writable if PLL mode is1M mode. Select a proper frequency specified in the Table 6-3 "Frequency range for high-speed clock operation". If the frequencies exceed the spec, the frequency will be corrected internally. However, the SFR read value is the written value. Refer to the Table 6-6 “HSC/SYSC setting and SYSCLK frequency” for detail.
7	-	Reserved bit

SYSC	PLL mode	
	24MHz/16MHz	1MHz
000	HSCLK *1	←
001	1/2 HSCLK *1	←
010	1/4 HSCLK	←
011	1/8 HSCLK (Initial value)	←
100	1/16 HSCLK	-
101	1/32 HSCLK	-
110	Do not use (1/32 HSCLK)	-
111	Do not use (1/32 HSCLK)	-

*1 : In no-wait mode, actual setting is changed to 1/1, 1/2, 1/4 HSCLK according to HSC setting

SYSC	HSC	PLL mode	Actual setting
000	000	24MHz	1/4 HSCLK (1/4 HSOCLK)
		16MHz	1/2 HSCLK (1/2 HSOCLK)
	001	24MHz	1/2 HSCLK (1/4 HSOCLK)
001	000	24MHz	1/4 HSCLK (1/4 HSOCLK)

Bit No.	Bit symbol name	Description
6 to 4	HSC2 to HSC0	Set frequency of HSCLK. These bits are writable when ENOSC=0. HSC2 bit is not writable if PLL1M mode.

HSC	PLL mode	
	24MHz/16MHz	1MHz
000	HSOCLK (Initial value)	←
001	1/2 HSOCLK	←
010	1/4 HSOCLK	←
011	1/8 HSOCLK	←
100	1/16 HSOCLK	-
101	1/32 HSOCLK	-
110	1/64 HSOCLK	-
111	Do not use (1/128 HSOCLK)	-

3 to 0	-	Reserved bits

Table 6-6 HSC/SYSC setting and SYSCLK frequency

PLL mode	SYSC \ HSC	000	001	010	011	100	101	110	Unit
24MHz	000	24(6)	12(6)	6	3	1.5	0.75	0.375	MHz
	001	12(6)	6	3	1.5	0.75	0.375	0.187	
	010	6	3	1.5	0.75	0.375	0.187	0.187	
	011	3	1.5	0.75	0.375	0.187	0.187	0.187	
	100	1.5	0.75	0.375	0.187	0.187	0.187	0.187	
	101	0.75	0.375	0.187	0.187	0.187	0.187	0.187	
16MHz	000	16(8)	8	4	2	1	0.5	0.25	
	001	8	4	2	1	0.5	0.25	0.125	
	010	4	2	1	0.5	0.25	0.125	0.125	
	011	2	1	0.5	0.25	0.125	0.125	0.125	
	100	1	0.5	0.25	0.125	0.125	0.125	0.125	
	101	0.5	0.25	0.125	0.125	0.125	0.125	0.125	
1MHz	000	1	0.5	0.25	0.125	-	-	-	
	001	0.5	0.25	0.125	0.125	-	-	-	
	010	0.25	0.125	0.125	0.125	-	-	-	
	011	0.125	0.125	0.125	0.125	-	-	-	

A value in () is frequency when no-wait mode.

6.2.3 Low-speed Clock Mode Register (FLMOD)

FLMOD is a SFR to control low speed clock.

Address : 0xF004(FLMODL/FLMOD), 0xF005(FLMODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FLMOD															
Byte	FLMODH								FLMODL							
Bit	OUTLS	-	-	-	-	L1CEN	LOSCMD1	LOSCMD0	LMOD1	LMOD0	-	LFLTSEL	-	L1SEL	-	L0SEL
R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	OUTLS	Selects the low-speed clock to be output to LCKO. This bit is initialized by all system reset. 0 : LSCLK0 (Initial value) 1 : LSCLK1
14 to 11	-	Reserved bits
10	L1CEN	Set enable/stop LSCLK1 oscillation. This is writable only when L1SEL is “0”. 0 : LSCLK1 oscillation stop (Initial value) 1 : LSCLK1 oscillation enable
9,8	LOSCMD1, LOSCMD0	Selects crystal oscillation or external input, and control crystal oscillation circuit. 00: Disabled the crystal oscillation circuit. (Initial) 01: Enabled the crystal oscillation circuit as crystal oscillation mode; XT32K mode 10: Enabled the crystal oscillation circuit as external clock input mode; EXT32K mode 11: invalid (Not use) When entering STOP/STOP-D mode with this bit set to "01"/"10", this bit is cleared to "00" and the crystal oscillation/low-speed external clock stops. Writing only “00” to these bits is enabled when these bits are “01”/”10”.
7,6	LMOD1, LMOD0	Select low-speed crystal oscillation operation mode. Writing to these bits are valid only when LOSCMD1-0 is "00". 00: Standard mode (Initial value) 01: Low power consumption mode (LP mode) 10: Tough mode 11: Ultra low power consumption mode (ULP mode) LP mode : reduces power consumption by lowering the oscillation margin than the standard mode. Tough mode : increases oscillation margin and enhance the resistance against leakage between the pins. However, power consumption is increased. ULP mode : Lower power consumption than LP mode.
5	-	Reserved bit
4	LFLTSEL	Set internal noise filter when low-speed crystal oscillation clock is selected. Writing to these bits are valid only when LOSCMD1-0 is "00". 0: Without noise filter (Initial value) 1: With noise filter
3	-	Reserved bit
2	L1SEL	Select clock source of LSLK1. Writing 1 to this bit is invalid when LOSCMD1-0 is “01 or 10” and “LOSCS=1 or LOSCB=1”. However it is writable when the backup function is disabled, even if LOSCB=1. This bit is cleared to "0" when LOSCMD1-0 is set to "00". 0 : RC32K (Initial value) 1 : XT32K/EXT32K (selected by LOSCMD1-0)
1	-	Reserved bits

Bit No.	Bit symbol name	Description
0	L0SEL	Select clock source of LSLK0. Writing 1 to this bit is invalid when LOSCMD1-0 is “01 or 10” and “LOSCS=1 or LOSCB=1”. This bit is cleared to "0" when LOSCMD1-0 is set to "00". 0 : RC32K (Initial value) 1 : XT32K/EXT32K (Clock selected by LOSCMD1-0)

6.2.4 Clock Frequency Control Register (FCONW)

FCONW is a SFR to control the clock generation circuit and select system clock.

Address : 0xF006 (FCON/FCONW), 0xF007 (FCON1)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FCONW															
Byte	FCON1								FCON							
Bit	ENRC1K	-	-	-	-	-	-	-	LPLL	-	-	-	-	-	ENOSC	SELSCLK
R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	ENRC1K	Enable RC1K oscillation regardless of code option which set WDT to unused. If it is enabled, keep ON state even during standby mode. However, WDTCLK follows the settings. Use it when mutual monitoring of low-speed clocks when WDT is not in use. 0 : Normal state (Initial value) 1 : Enabled
14 to 8		Reserved bits
7	LPLL	Indicates that the frequency of the PLL oscillation is within the target error. 0: The frequency of PLL oscillation is out of the target error or the PLL oscillation is stopped (Initial value) 1: The frequency of PLL oscillation is within the target error
6 to 2	-	Reserved bits
1	ENOSC	Enable/start or disable/stop the oscillation of the high-speed clock oscillation circuit. 0: Disabled/turn off the high-speed clock oscillation (Initial value) 1: Enabled/turn on the high-speed clock oscillation
0	SELSCLK	Select system clock. This bit is unwritable when ENOSC=0. This bit and ENOSC bit can be set “1” at same time. If ENOSC set to "0", SELSCLK bit also to be "0". 0: LSCLK0 (Initial value) 1: High-speed clock selected by the SYSC2 to SYSC0 bit

6.2.5 High-Speed Clock Wake-up Time Setting Register (FHWUPT)

FHWUPT is a SFR to select wakeup time of high speed clock. This is writable only when ENOSC=0.
See Table 4-6 "Wake-up Time from Standby Mode" in the Chapter 4 for details about the wake-up time from the standby modes.

Address : 0xF008 (FHWUPT)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FHWUPT							
Bit	-	-	-	-	-	-	-	-	-	FHRDWN	-	-	-	-	-	FHUT0
R/W	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7	-	Reserved bit
6	FHRDWN	Control PLL at wake-up from HALT-H. This function controls PLL to avoid abnormal frequency caused by temperature difference between stand-by enter and wake-up. This controls to prevent PLL frequency deviations due to temperature changes during HALT-H transition and return. Set to “1” if FHUT0=1 and the temperature at the wake-up from HALT-H up or down than the following value from at stand-by entry. PLL24M mode: 15°C PLL16M mode: 20°C No setting is required at FLL1M mode. 0 : Disabled (Initial value) 1 : Enabled
5 to 1	-	Reserved bits
0	FHUT0	Configures the timing of starting to supply the high-speed clock oscillation when ENOSC=1. 0 : After Locked; the frequency clock is stabilized. (Initial value) A system clock stops until the high-speed clock is locked, if SELSCLK is set to “1”. 1 : Soon after ENOSC=1; approx. 30μs. The accurate of the clock frequencies is not guaranteed as the specification, however it is useable for the system clock.

6.2.6 High speed Time Base Clock Setting Register (HTBDR)

HTBDR is a SFR to set frequency of high speed time base clock.

Address : 0xF086 (HTBDR)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								HTBDR							
Bit	-	-	-	-	-	-	-	-	-	HT1D2	HT1D1	HT1D0	-	HT0D2	HT0D1	HT0D0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7	-	Reserved bits
6 to 4	HT1D2 to HT1D0	Set frequency of HTBCLK1. 000 : HSCLK (Initial value) 001 : HSCLK / 2 010 : HSCLK / 3 011 : HSCLK / 4 100 : HSCLK / 5 101 : HSCLK / 6 110 : HSCLK / 7 111 : HSCLK / 8
3	-	Reserved bits
2 to 0	HT0D2 to HT0D0	Set frequency of HTBCLK0. 000 : HSCLK (Initial value) 001 : HSCLK / 2 010 : HSCLK / 3 011 : HSCLK / 4 100 : HSCLK / 5 101 : HSCLK / 6 110 : HSCLK / 7 111 : HSCLK / 8

6.2.7 Backup Clock Status Register (FBUSTATW)

FBUSTATW is a SFR to indicate status of low speed clock.

Address : 0xF00C (FBUSTAT/FBUSTATW), 0xF00D (FBUSTATH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0101

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FBUSTATW															
Byte	FBUSTATH								FBUSTAT							
Bit	-	-	-	-	L1XT	L1RC	L0XT	L0RC	-	-	-	-	-	-	LOSCB	LOSCS
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R
Initial value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

Bit No.	Bit symbol name	Description
15 to 12	-	Reserved bits
11	L1XT	Indicates that LSCLK1 is operating with XT32K/EXT32K.
10	L1RC	Indicates that LSCLK1 is operating with RC32K.
9	L0XT	Indicates that LSCLK0 is operating with XT32K/EXT32K.
8	L0RC	Indicates that LSCLK0 is operating with RC32K.
1	LOSCB	Indicates that XT32K oscillation stop detection. This is cleared to “0” when writing “1” to this bit. 0 : Not stop detection or after clearing flag (Initial value). 1 : Stop detection. Then LSCLK0 is changed to RC32K by backup function. The backup of LSCLK1 depends on setting to code option. At once, the clock backup interrupt; QCBU bit of IRQ23 register is asserted. This function is enabled at the following conditions: - selected XT32K/EXT32K to LSCLK0; L0SEL=1, - selected XT32K/EXT32K to LSCLK1; L1SEL=1
0	LOSCS	Indicate the status of XT32K/EXT32K oscillation clock. When setting XT32K/EXT32K mode with LOSCMD1-0 bits of FLMOD register, this bit is changed to “0” after 16-bit timer X interrupt occurred. This interrupt occurs when the timer X count by XT32K/EXT32K clock coincides with TMHXD value. This bit becomes to “1” on the following conditions. - When the crystal oscillation turn off by the software (LOSCMD1-0=“00”). The interrupt does not occur in this time. - At entry to the STOP/STOP-D mode. The interrupt does not occur in this time. - At detected oscillation stopping. The interrupt; QCBU of IRQ23, occurs in this time. 0 : XT32K/EXT32K is enabled; stable. 1 : XT32K/EXT32K is disabled; not stable/malfunction stopping (Initial value)

6.2.8 Clock Backup Test Mode Acceptor (FBTACP)

FBTACP is a write-only SFR to enable writing to Clock Backup Test Mode register (FBTCON).
This is used to prevent erroneous writing to the FBTCON register.

Address : 0xF0C4 (FBTACP)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FBTACP							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

When "0xFA" and "0xF5" are written in the order to the FBTACP register, writing to the FBTCON is allowed only once. It requires writing "0xFA" and "0xF5" in the order every time to enable the continuous writes to the FBTCON.
Any other instructions can be executed between the instruction that writes "0xFA" to STPACP and the instruction that writes "0xF5". However, if write data other than "0xF5" after writing "0xFA", the procedure gets invalid, so needs write "0xFA" again.

6.2.9 Clock Backup Test Mode Register (FBTCON)

FBTCON is a SFR to control the clock backup test mode. The clock backup test mode can create purposely the state that stops the low-speed crystal oscillation (XT32K/EXT32K).

Address : 0xF0C6 (FBTCON)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FBTCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LOSCL	LOSCT
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 2	-	Reserved bits
1	LOSCL	Select fixed level of low-speed crystal oscillation clock when LOSCT=1. When the LOSCT bit is set to "1", the LOSCL bit determines the fixed level of low-speed crystal oscillation clock. 0: Fixed to "L" level (Initial value) 1: Fixed to "H" level
0	LOSCT	Set the clock backup test mode 0: Normal mode (Initial value) 1: Clock backup test mode. Use in XT32K/EXT32K mode

6.3 Description of Operation

6.3.1 Low-Speed Clock

The low-speed clock generation circuit supply LSCLK0/LSCLK1 that is selected the following clock source by the L0SEL/L1SEL bit of FLMOD register.

- Low-speed RC oscillation mode (RC32K)
- Low-speed crystal oscillation mode (XT32K) / external clock input mode (EXT32K)

The low-speed clock can be output from a port as LCKO. It is selected from LSCLK0 or LSCLK1 by OUTLS bit of FLMOD register.
See Table 1-3 pin list for assignment port function.
When the system reset is released, the CPU starts when the source clock selected for LSCLK0 counts 512.
The LSCLK0 is RC32K when the power on reset or pin reset is released.

Figure 6-2 shows the low-speed clock generation circuit configuration.

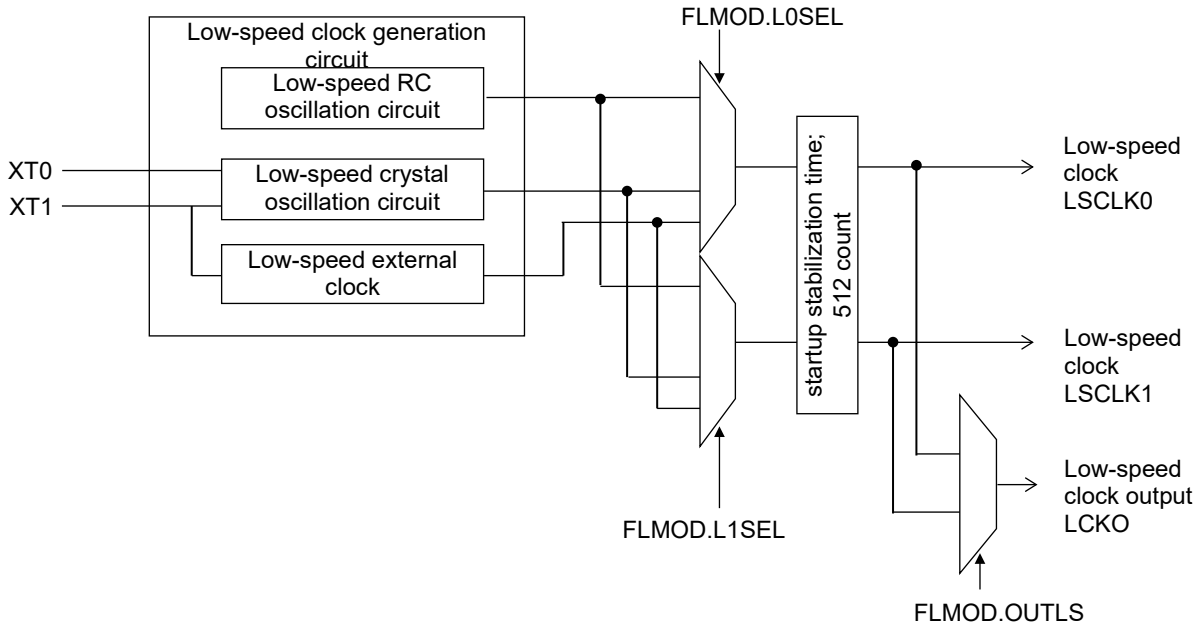


Figure 6-2 Configuration of Low-speed Clock Generation Circuit

[Note]

- **The LCKO output operation is not guaranteed in the HALT-D mode.**

6.3.1.1 Low-Speed RC Oscillation Circuit

The low-speed RC oscillation clock is selected as system clock at the power on.
When a system reset is released, the low-speed clock (LSCLK0, LSCLK1) is output and the CPU runs a program after 512 counts of clock chosen for LSCLK0.
When the STOP/STOP-D mode is released, the low-speed clock (LSCLK0, LSCLK1) is output after the low-speed RC oscillation start time (TRCL) + stabilization time has elapsed, and the CPU executes the program.
Figure 6-3 shows the configuration of the low-speed RC oscillation circuit.
Figure 6-4 shows the operation waveforms at the start of the low-speed RC oscillation circuit and in the STOP/STOP-D mode.

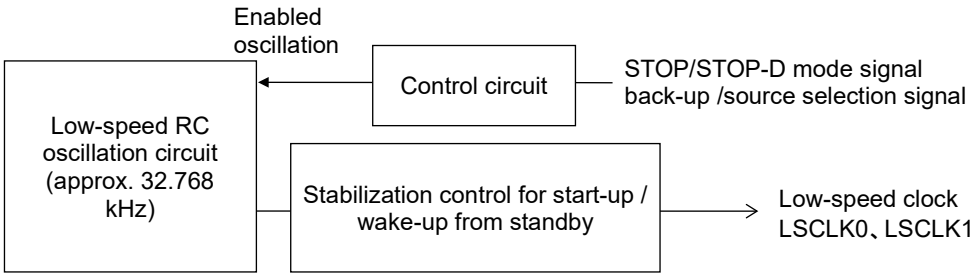


Figure 6-3 Configuration of Low-Speed RC Oscillation Circuit

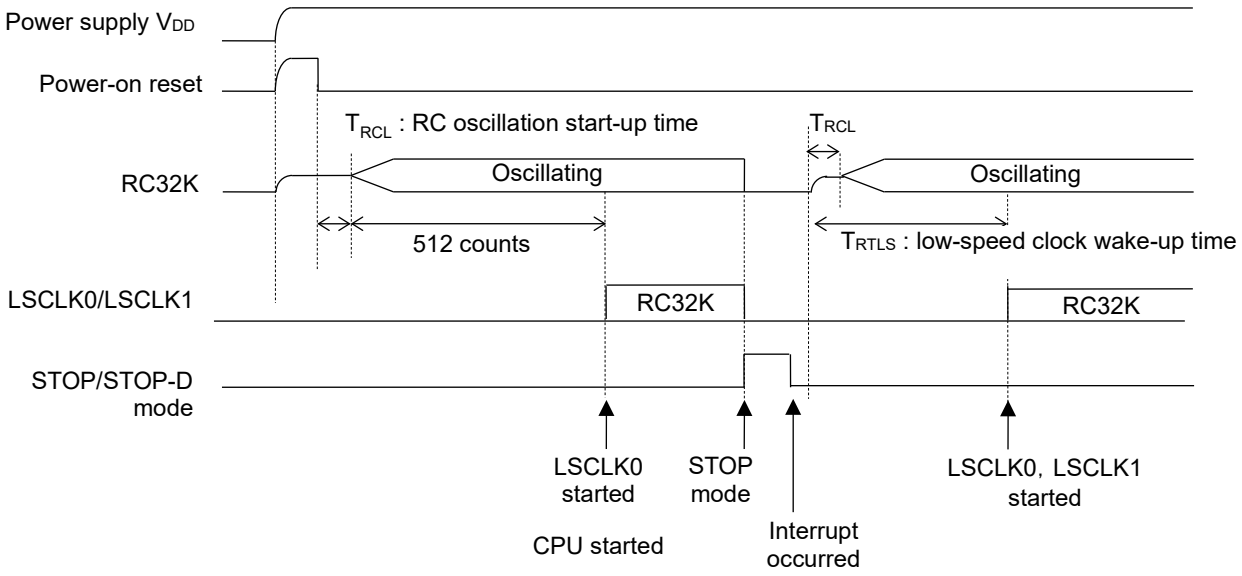


Figure 6-4 Low-speed Clock Operation Waveforms at Start of Low-speed RC Oscillation Circuit and in STOP/STOP-D Mode

6.3.1.2 Low-Speed Crystal Oscillation Circuit

Figure 6-5 shows a configuration of the low-speed crystal oscillation circuit.
By the low-speed clock mode register (FLMOD), select XT32K mode using 32.768 kHz crystal unit or EXT32K mode that input from XT1 pin .
In XT32K mode, the setting of PXTMOD01 register is ignored. As general-purpose input port, it is the same as the high-impedance setting.
In EXT32K mode, the setting of PXTMOD1 register is ignored. As general-purpose input port, it is the same as the high-impedance setting.
To supply XT32K/EXT32K as LSCLK0/1, it is necessary to complete the oscillation stabilization wait using timer X.
Timer X can be used as a normal timer after the oscillation stabilization wait is completed.
Both modes have a function (backup function) that constantly monitors oscillation and switches the low-speed clock to the low-speed RC oscillation clock when oscillation stop is detected.
The switching to RC oscillation for LSCLK1 can be invalid by code option, and it can only indicate the stop detection.
This oscillation circuit stops when STOP/STOP-D mode entry.

In the case of LSCLK1, the code option does not switch to RC32K, and only oscillation stop detection can be indicated.
When entering the STOP/STOP-D mode, the low-speed crystal oscillator circuit stops operating.

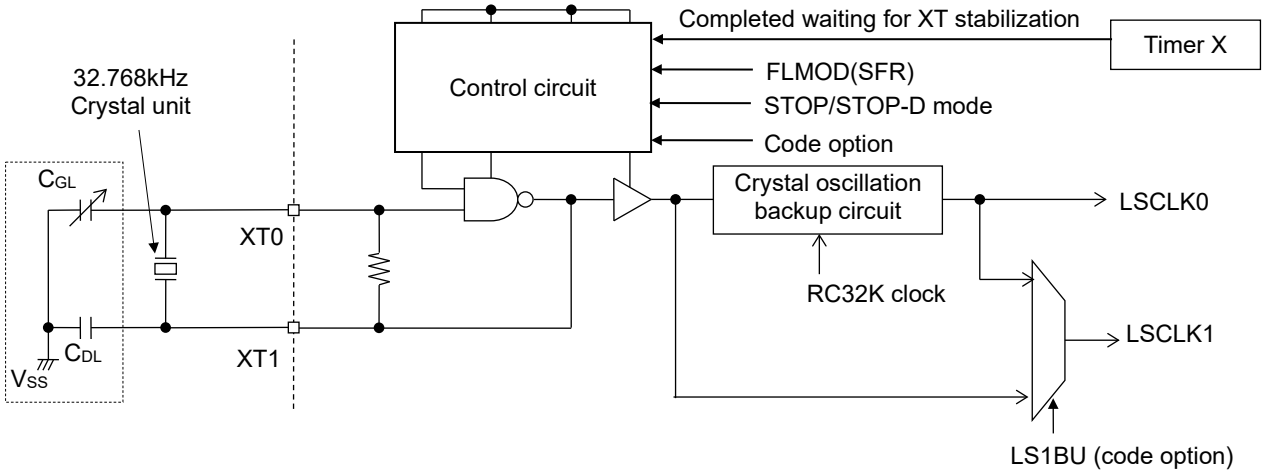


Figure 6-5-1 Circuit Configuration of XT32K mode

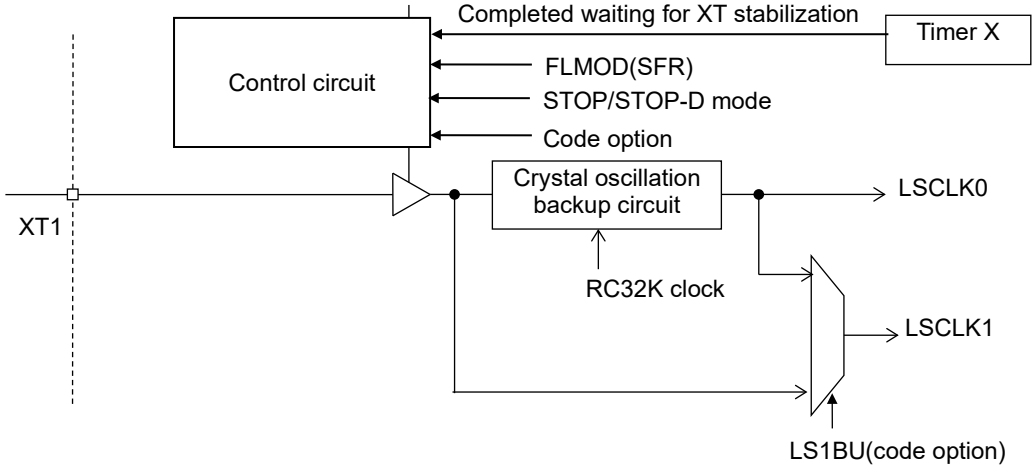


Figure 6-5-2 Circuit Configuration of EXT32K mode

[Note]
- **Place the crystal resonator as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal and its wiring.**
- **Note that oscillation may stop due to condensation.**
- **When switching to the low speed crystal oscillation clock, ensure to use the interrupt referring to the Section 6.3.1.3 "Low-Speed Clock Control".**

Figure 6-6 shows the backup mode waveforms when the low-speed crystal oscillator circuit starting up and in STOP mode.
The low-speed crystal oscillator circuit operates when the low-speed RC oscillator circuit starts operation after the power is turned on, and when the LOSCMD 1,0 bit is set to "01" in the low-speed clock mode register (FLMOD) after the CPU starts running. Since the FLMOD register is initialized only with power-on reset and pin reset, oscillation continues even if other resets occur after XT32K mode/EXT32K mode is selected.
After waiting for the oscillation stabilization time in timer X, XT32K/EXT32K clock is supplied to LSCLK0/LSCLK1 by setting L0SEL/L1SEL to "1". The oscillation stabilization time can be adjusted by changing the count value of timer X.
In addition, the low-speed crystal oscillation circuit turns off when entering the STOP/STOP-D mode. When the STOP/STOP-D mode is released by external interrupts and etc., LSCLK0/1 oscillation is in the RC32K mode.

See Chapter 4 "Power Management" for the STOP/STOP-D mode.
See the data sheet for the low-speed oscillation start time (T_{XTL}).

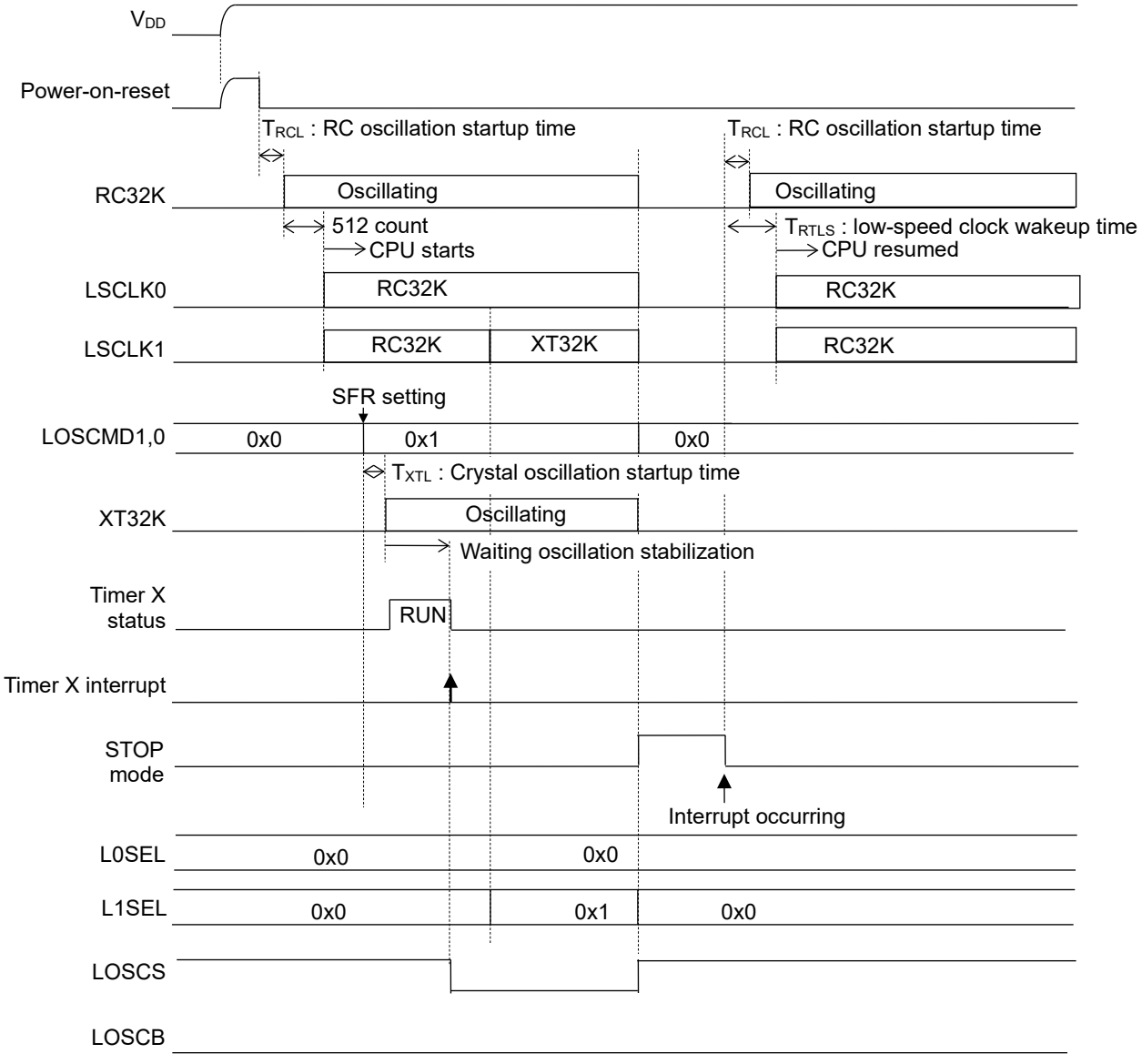


Figure 6-6 Low-speed Crystal Oscillation Circuit Operation (At startup and in the STOP mode)

Figure 6-7 shows operation waveform in the backup mode after the startup of the low-speed crystal oscillation circuit. When the crystal oscillation clock stops after the low-speed crystal oscillation started, it shifts to the backup mode about 2ms(typ.) later, and then the clock backup interrupt (CBUINT) occurs.

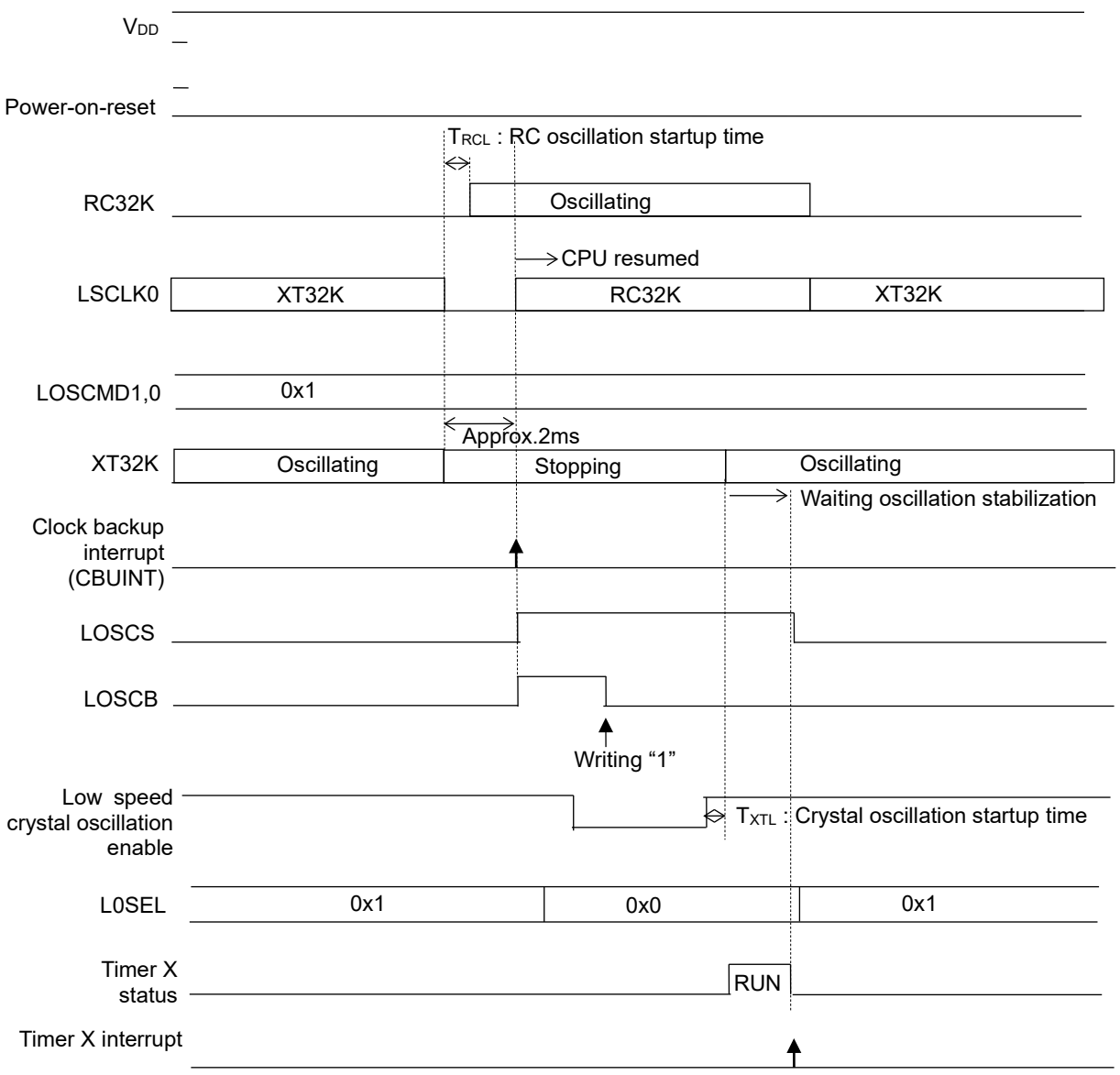


Figure 6-7 Low-speed Oscillation Circuit Operation in the backup mode

Figure 6-8 shows the operation waveforms when a reset occurs in the XT32K/EXT32K mode. The crystal oscillation circuit is not reset by anything other than power-on-reset and pin reset.
See Chapter 3 "Reset Function" for details of resetting.

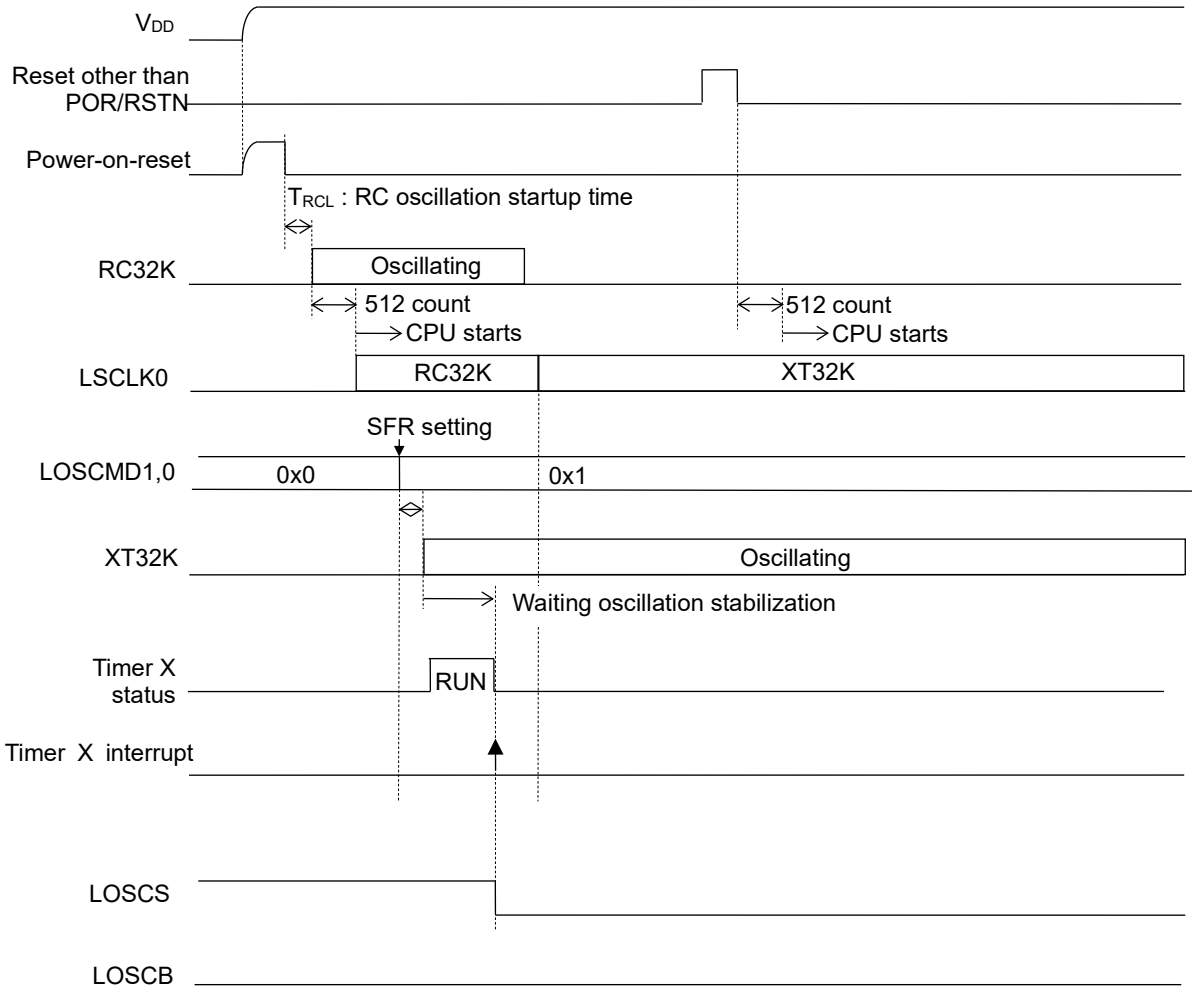
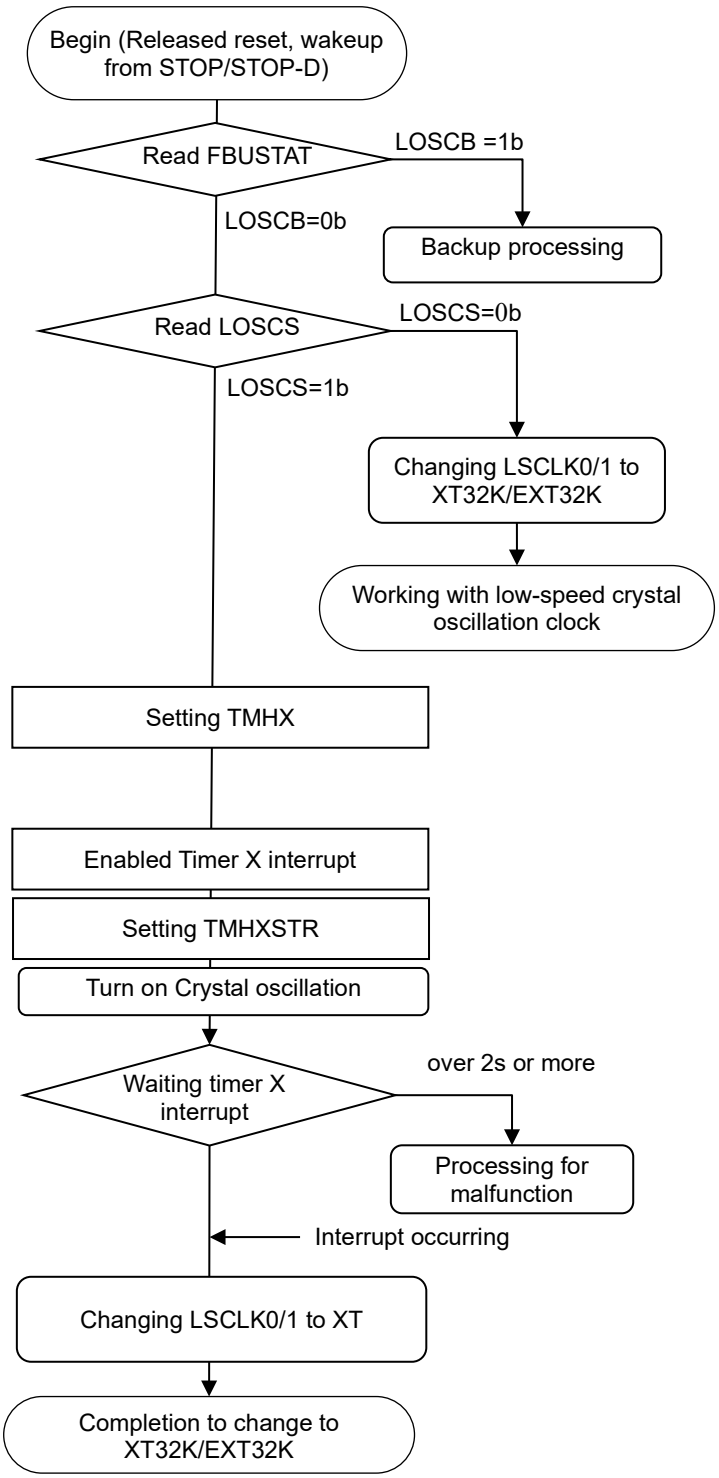


Figure 6-8 Low-speed Oscillation Circuit Operation (at System Reset after the crystal oscillation turned on)

6.3.1.3 Low-Speed Clock Control

Figure 6-9 shows a flow of the low-speed clock setting; from RC32K to XT32K/EXT32K. Use the flow at the wake up from STOP/STOP-D mode.
If switch the system clock to a high speed, switch the low-speed clock to a low-speed crystal oscillation clock(XT32K) or a low-speed external clock(EXT32K) at first.
See chapter 8 “16-bit Timer” for timer function.



Confirm LSCLK status for reading LOSCB bit of FBUSTAT.

LOSCB=1 : It is state the crystal oscillation stop is detected. Do backup processing.

LOSCS=0 : It is state the crystal oscillation stabilization wait is completed. If L0SEL/L1SEL is “0”, set it to “1” and switch to crystal oscillation.

LOSCB=0,LOSCS=1 : It is state the crystal oscillation stabilization wait is not completed.
Do crystal oscillation stabilization with Timer X.

Set stabilization wait cycles for TMHXD in the Timer X. (where, the number of cycles is the number of halves of the XT32K clocks.)
Clear TMHC and set to TMHXCON ;
TLXOST=1 : one-shot mode
THXCK=4 : low-speed crystal oscillation
THXDIV=arbitrary : set when the number of cycles is insufficient.

Enabled Timer-X interrupt.
Clear QTMX bit and Set “1” to ETMX bit.
Set THXRUN=1 to enable timer operation.
Write 1 or 2 to LOSCMD1-0 bits of FLMOD, and the wait oscillation stabilization.

If XT32K stops before the stabilizes , the Timer-X interrupt does not occur, so set timeout and handle appropriately for the application.

Change LSCLK0/LSCLK1 with L0SEL/L1SEL bit of FLMOD, after the timer X interrupt occurs.

Timer X can be in use as general timer, after completion to wait oscillation stabilization.

Figure 6-9 Procedure to change the low-speed clock from RC32K to XT32K/EXT32K

Handle appropriately for the application at the backup processing in Figure 6-9. Figure 6-10 shows the procedure to rechange LSCLK to RC32K.
Clear the LOSCB bit with referring to Figure 6-10, when the L1SEL=1 and backup function is enabled, or when L0SEL=1. Then handle the procedure in the Figure 6-9 if it will use the XT32K/EXT32K mode again.

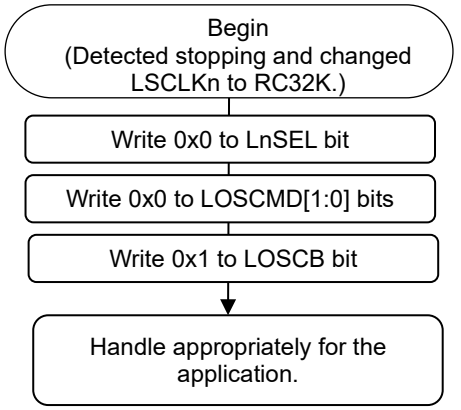
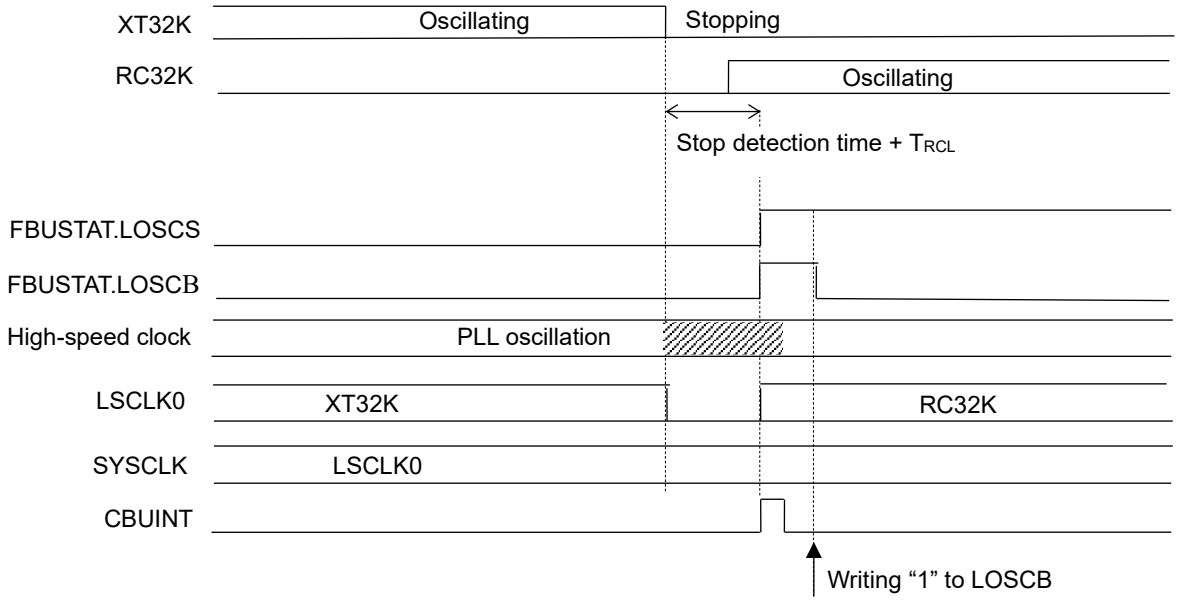


Figure 6-10 Backup procedure

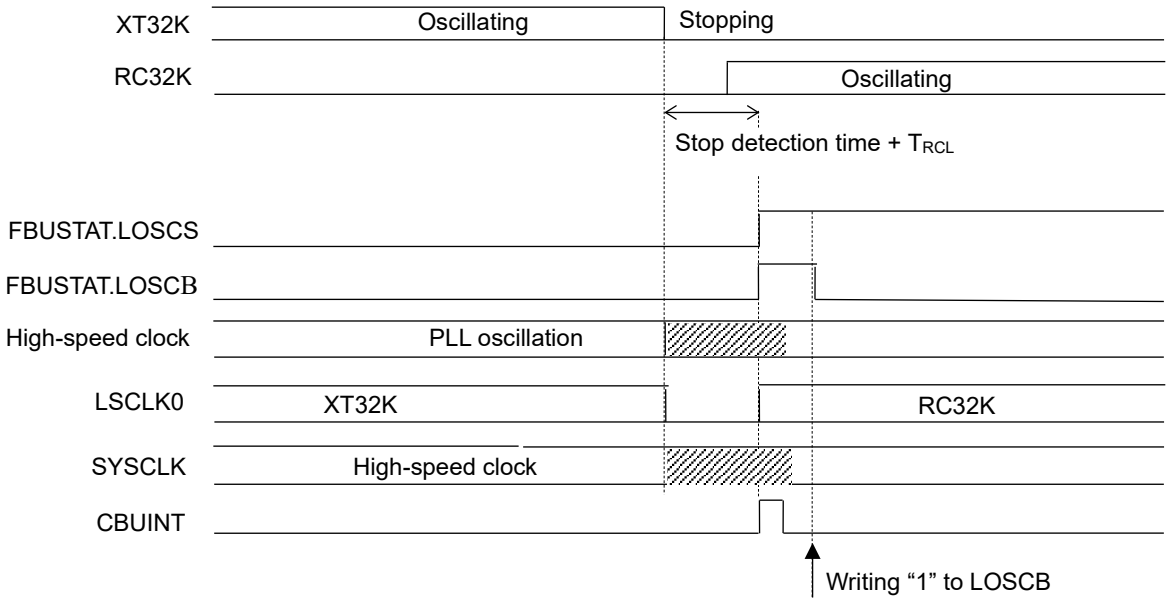
The clock backup interrupt occurs at stop detection, even if the LSCLK1 is used without backup function in the XT32K/EXT32K mode. Then newer interrupt does not occur until the LOSCB bit is cleared.

6.3.1.4 Oscillation Stop Detection and Back-up Function

When the XT32K stop detected after LSCLK0/LSCLK1 is set to XT32K, the LSCLK0/LSCLK1 is switched to the RC32K. It is clock backup function.
The stop detection time is approx. 4ms (typ.) when not in the HALT-D mode, and approx. 5ms (typ.) in the HALT-D mode.
Figure 6-11 and 6-12 show the operation of XT32K stop detection under each condition.
In case of LSCLK0=XT32K, LSCLK1=XT32K/OFF :
When the XT32K stops, the LSCLK0 also stops, and the high-speed clock frequency is not guaranteed. When the stop is detected for a certain period of time, the RC32K is turned on and the stop detection process is performed. The LSCLK0 is supplied again with RC32K and recovers the high-speed clock frequency.
If the system clock is low-speed, the SYSCLK stops too; Figure 6-11(1).
If the system clock is high-speed, the SYSCLK does not stop; Figure 6-11(2)



(1) In case of SYSCLK=LSCLK0=XT32K

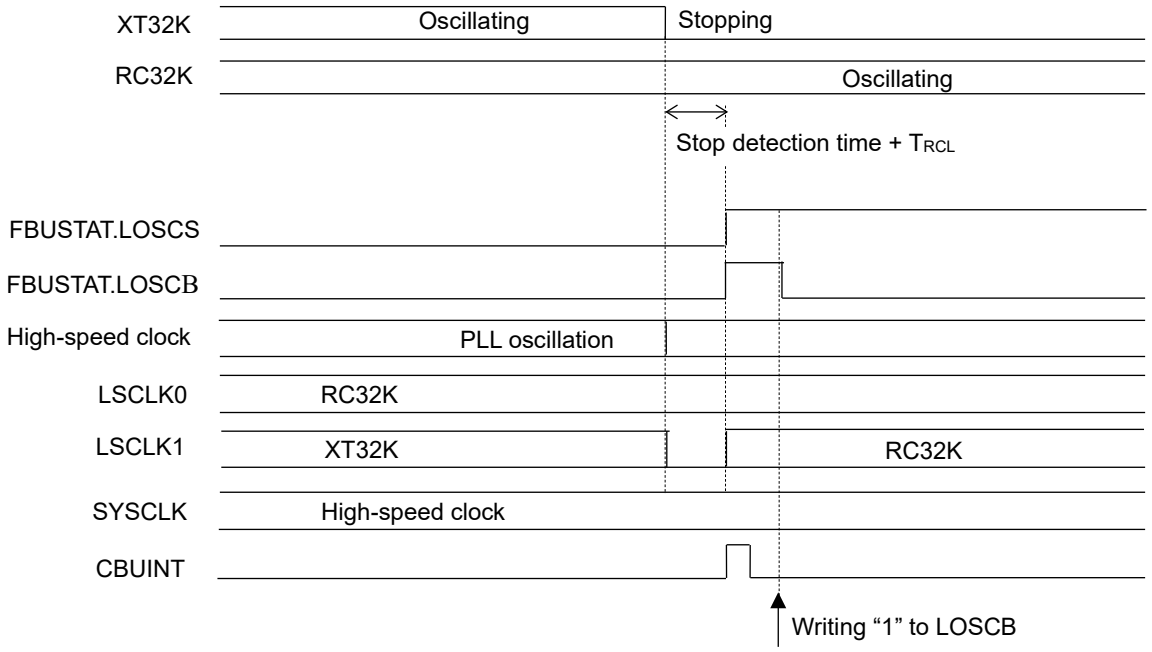


(2) In case of SYSCLK=HSCLK, LSCLK0=XT32K

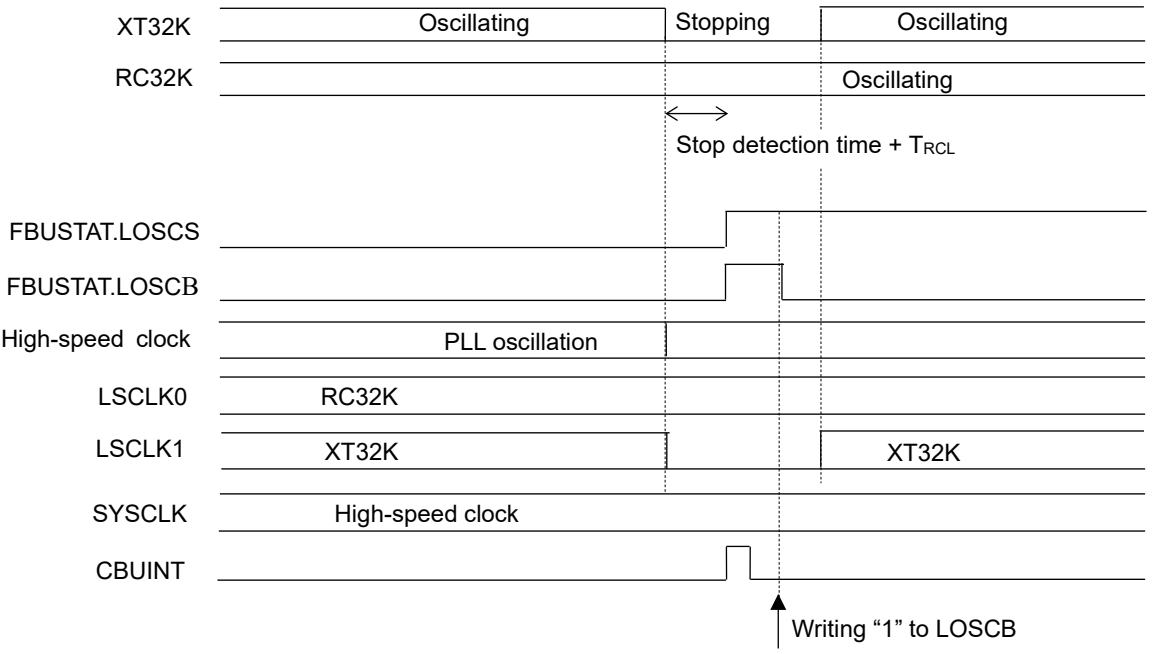
: The PLL frequency is not guaranteed between from stopping XT32K to locked PLL based RC32K.

Figure 6-11 Stop detection for the crystal oscillating: 1 (LSCLK0=XT32K, LSCLK1=XT32K)

In case of LSCLK1=XT32K, LSCLK0=RC32K :
The LSCLK1 stops when XT32K stops. The SYSCLK/High-speed clock do not stop. When the stopping continues in a certain time, the stop detection occurs.
If enabled backup, LSCLK1 becomes to RC32K; Figure 6-12-1(1).
If disabled backup, LSCLK1 is kept XT32K even if stop detection occurs; Figure 6-12-1(2). LSCLK1 stops when XT32K stops, also LSCK1 oscillates when XT32K oscillates again. The clock backup interrupt occurs when the stop detection occurs.



(1) Enabled backup; LS1BU=1



(2) Disabled backup; LS1BU=0

Figure 6-12-1 Stop detection for the crystal oscillating: 2
(SYSCLK=HSCLK, LSCLK0=RC32K, LSCLK1=XT32K)

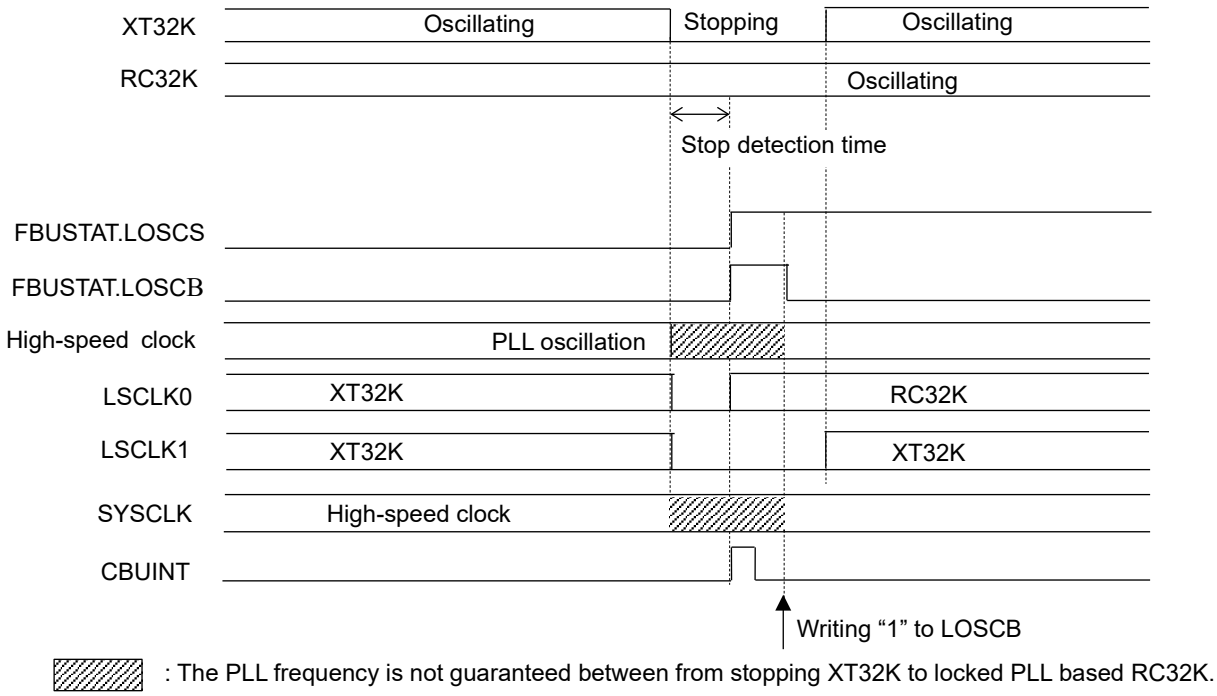


Figure 6-12-2 Stop detection for the crystal oscillating: 3
(SYSCLK=HSCLK, LSCLK0=XT32K, LSCLK1=XT32K)

6.3.1.5 Status of XT32K/EXT32K Mode

Table 6-6 shows relationship of each setting and status in the XT32K mode. As for EXT32K mode, change the reading "LOSCMD0" to "LOSCMD1", "XT32K" to "EXT32K".

Table 6-7 Status of LSCLK (XT32K)

LOSCMD0	L1CEN	LS1BU	L1SEL	L0SEL	LOSCB	LOSCS	LSCLK1	LSCLK0
1	1	1	0	0	0	0	RC32K(CW)	RC32K(CW)
1	1	1	0	0	0	1	RC32K(SW)	RC32K(SW)
1	1	1	0	0	1	1	RC32K	RC32K
1	1	1	0	1	0	0	RC32K	XT32K
1	1	1	0	1	1	1	RC32K	RC32K(BU)
1	1	1	1	0	0	0	XT32K	RC32K
1	1	1	1	0	1	1	RC32K(BU)	RC32K
1	1	1	1	1	0	0	XT32K	XT32K
1	1	1	1	1	1	1	RC32K(BU)	RC32K(BU)
1	1	0	0	0	0	0	off	RC32K(CW)
1	1	0	0	0	0	1	off	RC32K(SW)
1	1	0	0	0	1	1	off	RC32K
1	1	0	1	0	0	0	XT32K	RC32K
1	1	0	1	0	1	1	XT32K(SS)	RC32K
1	1	0	1	1	0	0	XT32K	XT32K
1	1	0	1	1	1	1	XT32K(SS)	RC32K(BU)

Character in () means the following:
BU=Backup state, SW=Waiting stability of XT32K, CW=Completion of waiting stability of XT32K, SS=Detected stop
* : LOSCB state is a state before clearing, so it does not show state in the backup procedure.

6.3.2 High-speed Clock

The PLL oscillation circuit generates the high-speed clock; HSOCLK by multiplying the LSCLK0.
The PLL frequency is configured to 24MHz/16MHz/1MHz by the code option.
The high-speed output clock divided the HSOCLK ; HCKO is output from LSI pins. See Table 1-3 for pin assignment.

6.3.2.1 PLL Oscillation Circuit

The PLL oscillation circuit generates the high-speed clock; HSOCLK by multiplying the LSCLK0. The multiplying by 732.5 is 24MHz of PLL frequency, and the multiplying by 488.5 is 16MHz of PLL frequency, and the multiplying by 30.5 is 16MHz of PLL frequency.
After high-speed clock oscillation is enabled, the high-speed clocks; HSCLK/HSCOCLK/HCKO is output by continuing count operation until the PLL oscillation clock is stabilized.

When set “1” to the FHUT0 bit of FHWUPT register, the clock supply is started approximately 30 μs after the high-speed clock oscillation is enabled. The clock frequency reaches to the target approximately 1 ms after the high-speed clock oscillation is enabled. Although the frequency within the 1 ms is not guaranteed, it can be used for the system clock.when set “0” to the FHUT0 bit, the clock supply is started approximately 1ms after it is enabled.

In addition, the PLL oscillation circuit stops oscillation when entering the HALT-H/HALT-D/STOP/STOP-D mode. Its oscillation is output, after wakeup from standby and waiting stabilization.

Figure 6-13 shows the PLL oscillation circuit configuration.

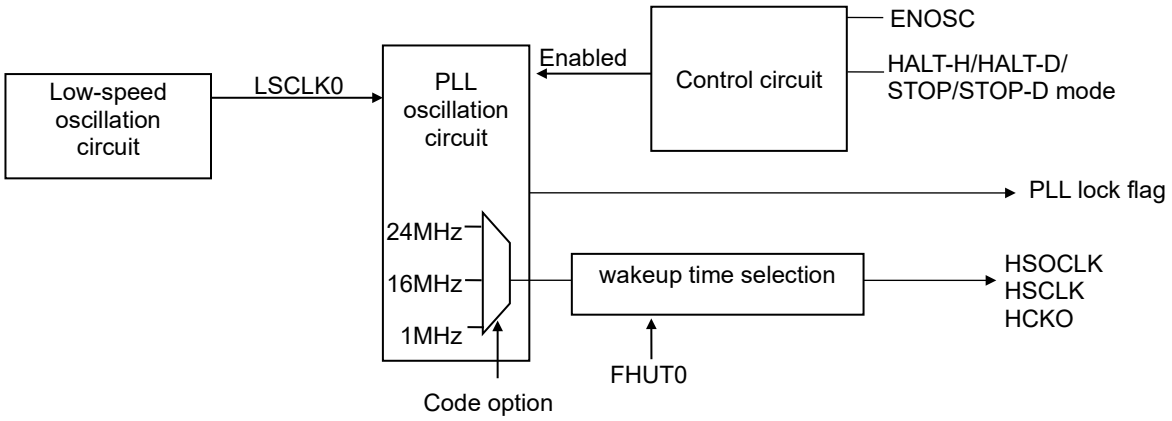


Figure 6-13 PLL Oscillation Circuit Configuration

Figure 6-14 show the high-speed clock operation waveforms at startup PLL circuit, in the standby mode.
See Table 4-6 for the time for wakeup from the HALT-H mode. See Chapter 4 “Power Management” for details of the STOP/STOP-D mode.

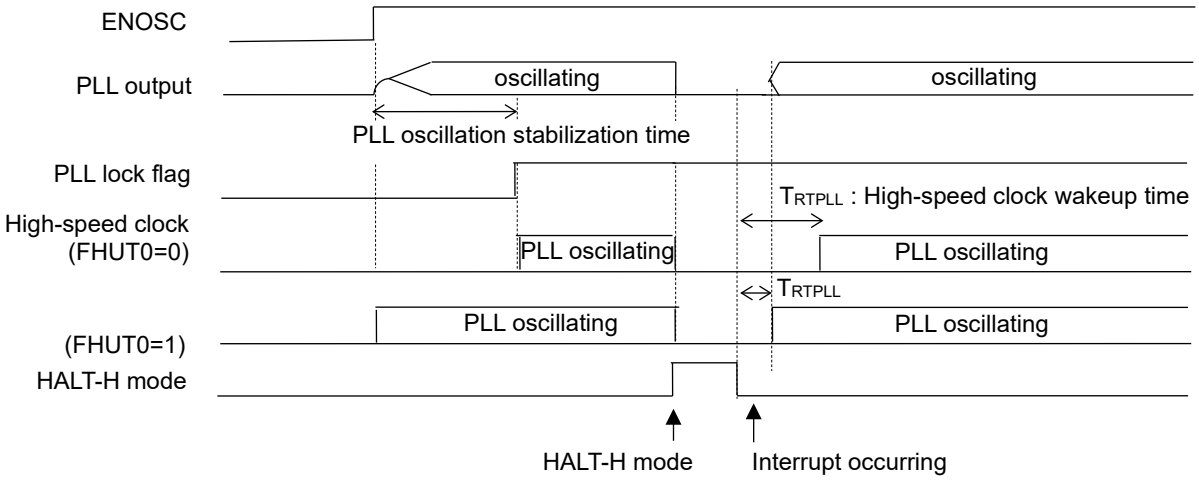


Figure 6-14-1 High-speed clock operation at startup PLL circuit and in HALT-H mode

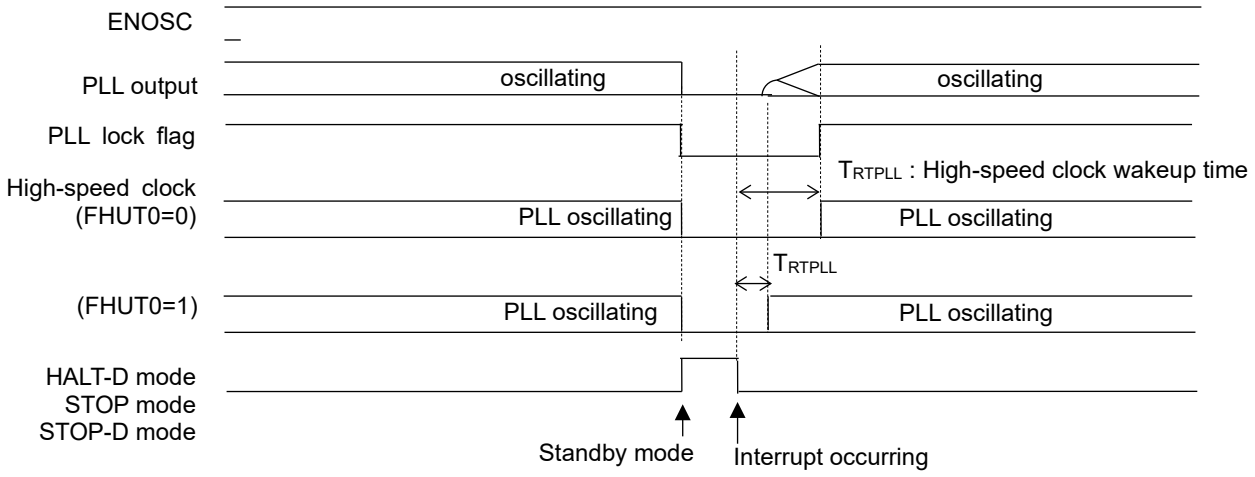


Figure 6-14-2 High-speed clock operation in the HALT-D/STOP/STOP-D mode

6.3.2.2 High-speed Clock Control

The following is a procedure to control high-speed clock.

(1) Set dividing HSCLK by FHCKMODL.
(2) Set with or without waiting stabilization by FHWUPT.
(3) Set enabled PLL oscillation by ENOSC=1. SELSCLK bit can be set to "1" at once.
The system clock stops until the high-speed clock oscillates when SELSCLK=1.

In the case of without waiting stabilization; FHUT0=1: Although the high-speed clock frequency is not guaranteed just after setting ENOSC=1, it can be used for the system clock and peripheral clocks. If specific frequency is required, wait stabilization time; LPLL=1.
In the case of with waiting stabilization; FHUT0=0: The clock is supplied after LPLL bit becomes to "1".

The control flow when the high-speed clock before stabilization with LSCLK0=RC32K, is used for the initialization processing and the high-speed clock after stabilization with LSCLK0=XT32K is used for the main processing as the system clock is shown below.

(1) Set dividing HSCLK by FHCKMODL.
(2) Set without waiting stabilization by FHWUPT. Because the high-speed clock output pauses when switching of (5) if FHUT0=0.
(3) Set enabled PLL oscillation by ENOSC=1 and changing system clock by SELSCLK=1 at once.
(4) Set enabled XT32K oscillation by FLMOD, and then execute a procedure to wait crystal oscillation stabilization and wait LOSCS=0 .Execute initialization for user program during waiting LOSCS=0.
(5) Set "1" to the L0SEL bit of FLMOD, so that LSCLK0 is changed from RC32K to XT32K.
(6) To wait PLL frequency stabilization, wait for LPLL=1 after 156μs elapse from (5).

Set "0" to ENOSC bit to turn off high-speed clock by the software. Then SELSCLK is cleared at once, and the system clock is switched to low-speed clock.
If high-speed clock is kept on, do not set "0" to ENOSC bit, and set "0" to SELSCLK bit only.

[Note]
- **When the XT32K is used for LSCLK0, the high-speed clock may become an unintended frequency due to external factors such as noise, and the MCU may operates abnormally. Please evaluate enough the apparatus/system which implemented this product.**

6.3.2.3 HALT-H mode

The high-speed clock is stopped when entry to HALT-H mode, and the clock is automatically turned on when wake-up. The PLL frequency stability time is due to temperature difference between the HALT-H mode enter and wake-up. It takes up to 2ms for the high-speed clock to be supplied if FTUT0=0.

The PLL frequency accuracy is about ±5% in 300μs when the temperature difference is as follows in each mode.

PLL mode	temperature difference range [°C]	Other conditions
24M mode	-22 ~ +16	Code option VLMD=0
16M mode	-17 ~ +13	Code option VLMD=0
1M mode	-13 ~ + 10	-

If no waiting locked PLL; FHUT0=1, the PLL frequency may exceed the operating range depending on the temperature difference. Therefore, control with FHRDWN bit to avoid it. See “6.2.5 High-Speed Clock Wake-up Time Setting Register” for the FHRDWN bit, and “30.2.3 Code Option 1” for code option VLMD.

6.3.3 Internal 1kHz clock (RC1K)

The internal 1kHz clock is oscillation that frequency is 1.024kHz typ. It is supplied to the WDT, 16-bit timer, functional timer.
In the case of the WDT operation is enabled by setting code option; WDTMD=1 :
RC1K is oscillating after system reset is released. It turns off at entry to STOP/STOP-D mode, and then it turns on at wakeup from standby. In the HALT-D mode, it stops only when WDTPWMD1=0 is selected by setting code option. The clock wakeup time is approx. 2ms.
In the case of WDTMD = 0 :
RC1K has stopping after system reset is released. RC1K oscillation is enable by the ENRC1K bit of FCONW register becomes “1”, and the clock is supplied after approx. 2.5ms.

The RC1K oscillation does not stop in the standby mode if ENRC1K=1. However a suppling WDTCLK depends on code options. Also, a suppling RC1K to 16-bit timer/functional timer stops in the STOP/STOP-D mode.
Set ENRC1K=1 before the standby entry if the RC1K oscillating will be required quickly after wakeup from stand-by.
See Chapter 30 “Code Option” for how to set code options.

Figure 6-15 shows configuration of internal RC1K oscillation.
Figure 6-16 shows an operation of RC1K and WDTCLK at startup and wakeup from STOP mode.

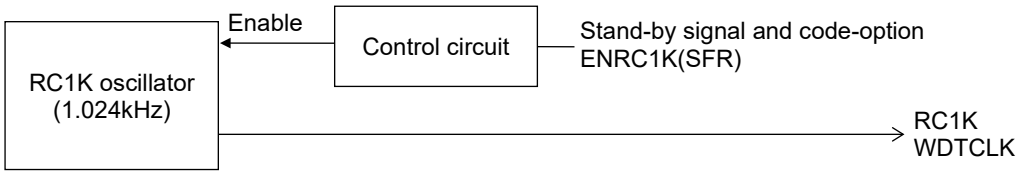


Figure 6-15 Configuration of internal 1kHz oscillator

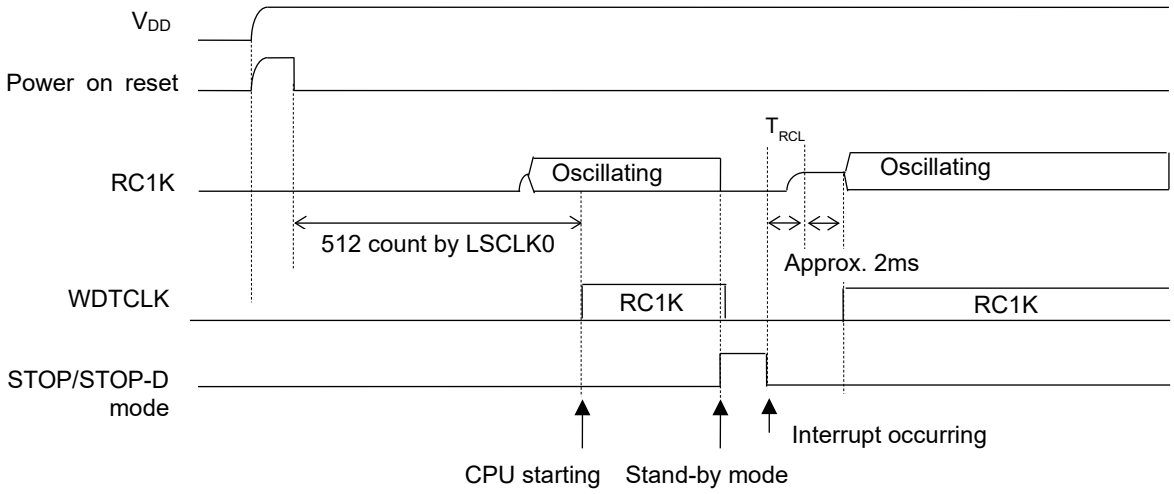


Figure 6-16-1 Startup and Wakeup from STOP mode of RC1K oscillator (ENRC1K=0)

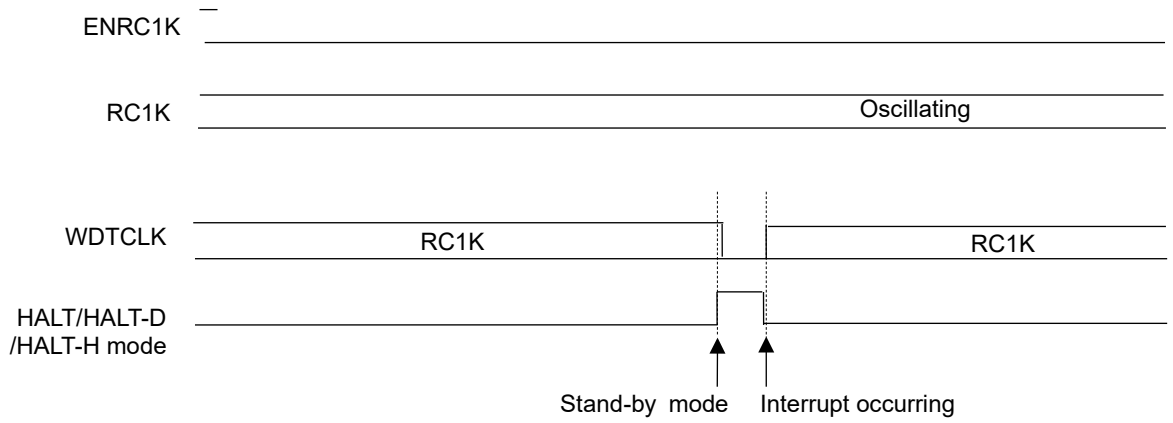


Figure 6-16-2 HALT/HALT-H/HALT-D mode (ENRC1K=0)

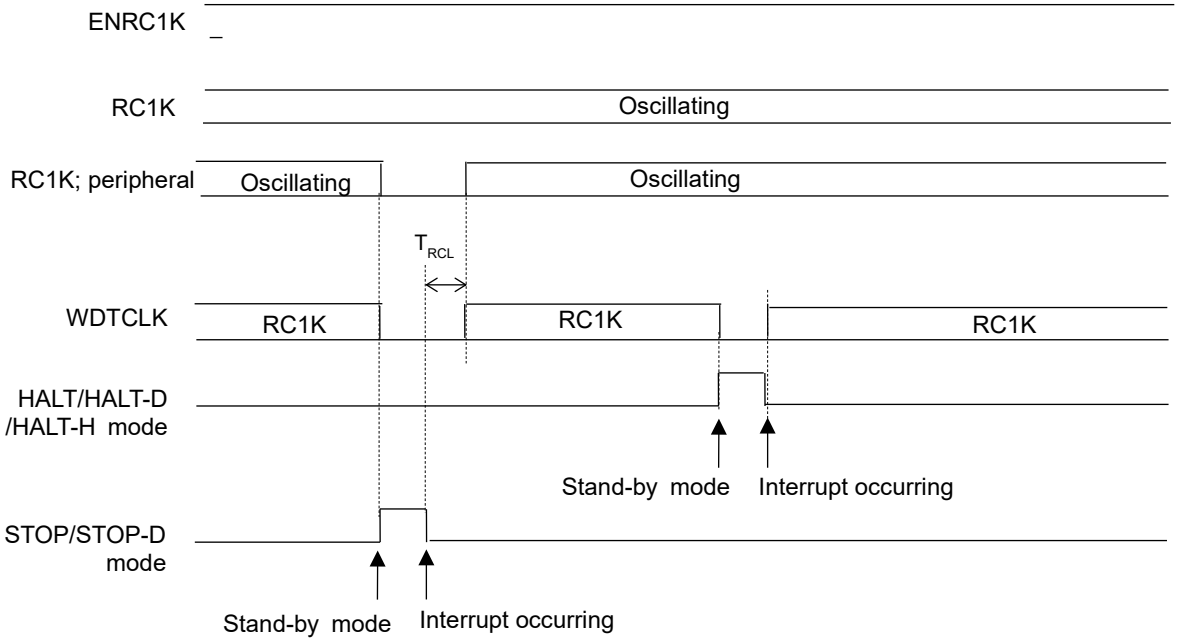


Figure 6-16-3 Stand-by mode (ENRC1K=1)

6.3.4 System Clock

A system clock is LSCLK0 with RC32K after power-on-reset/pin reset. The source clock of LSCLK0 is configured L0SEL after another system reset.
A system clock can be dynamically switched the high-speed system clock or LSCLK0 by SELSCLK bit. The high-speed system clock can be dynamically changed dividing value by SYSC bits.
There are 2 types as system clock; CPUCLK supplied to CPU and SYSCLK supplied to peripherals.
The CPUCLK stops in all stand-by mode. The SYSCLK normally supplies in the HALT/HALT-H mode, however it does not supply to some peripherals in the HALT-D mode. See Chapter 4 “Power Management” for detail.

[Note]

- **While the CPU is running with the low-speed clock, if running the peripheral circuits with the high-speed clock which can frequently generate interrupts, the operation may fail to function properly due to the CPU becoming incapable of processing interrupts in time. If interrupts frequently occur for reasons such as short interrupt cycles of peripheral circuits, take into account the operating frequency of the CPU so that it can process interrupts in time.**

6.3.5 Interrupt

The clock control circuit has a interrupt vector of clock backup interrupt.
The clock buck-up interrupt is generated when the crystal oscillating or external clock input stop in the XT32K/EXT32K mode.
At this interrupt generated, LOSCB becomes to “1”. Write “1” to LOSCB bit to clear this flag.
New interrupt request does not occur until the LOSCB bit is cleared.

To wait crystal oscillation stability, use 16-bit timer X interrupt.

6.3.6 Clock Back-up Test

The clock back-up test function can make purposely the condition that stops the low-speed crystal oscillation. Figure 6-17 shows the test procedure.

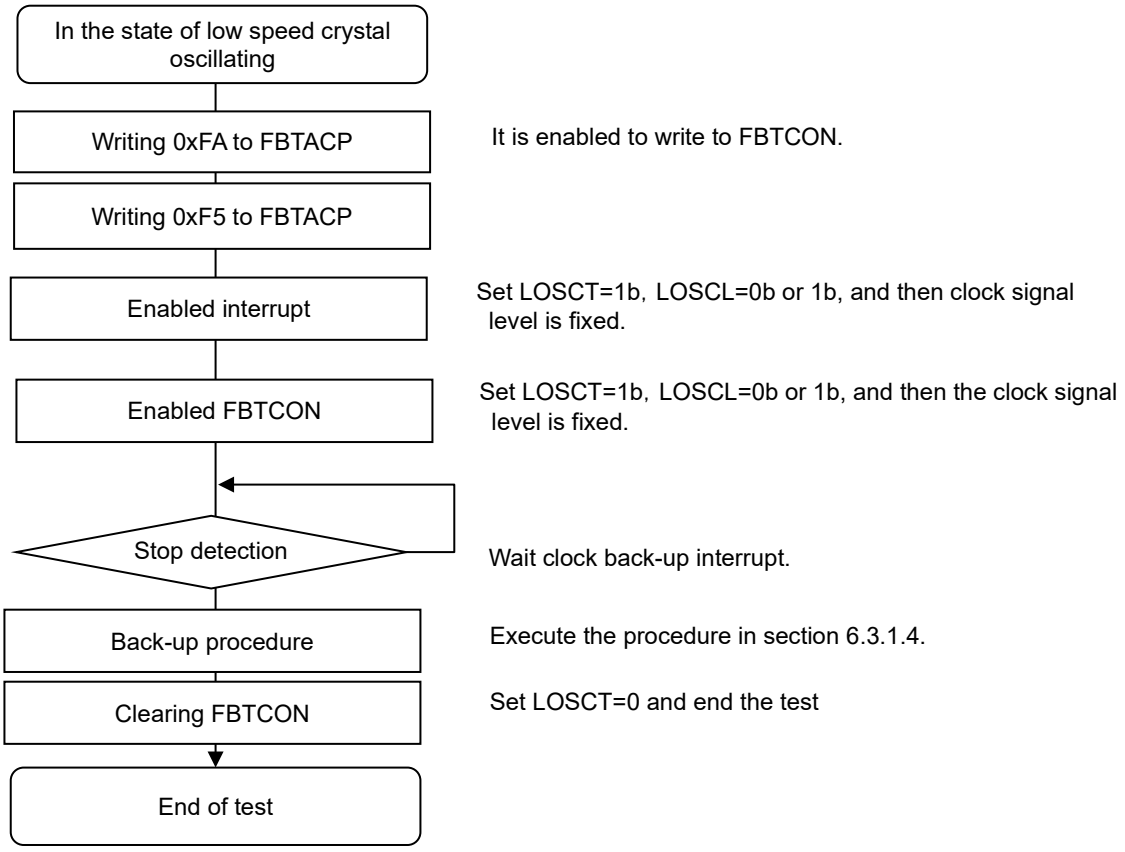


Figure 6-17 Clock Back-up Test Procedure

Chapter 7 Low Speed Time Base Counter

7. Low Speed Time Base Counter

7.1 General Description

The low speed time base counter enables following functions.

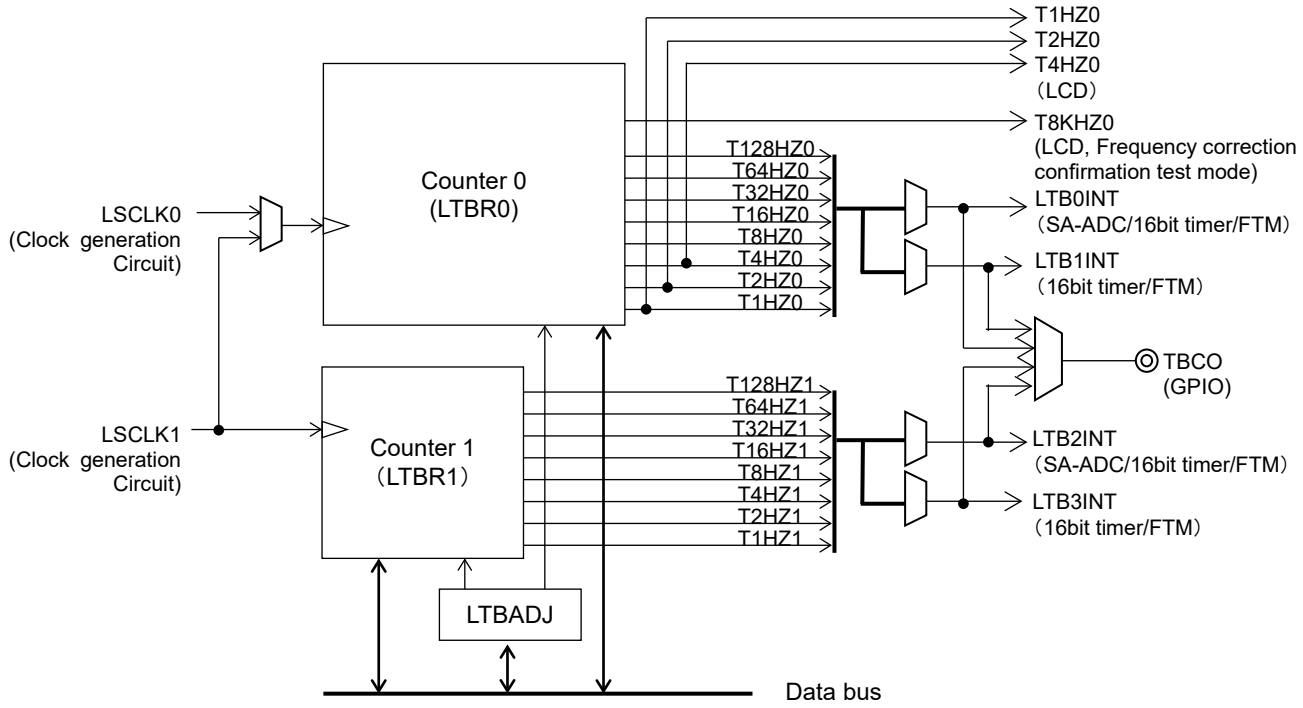
- Generate periodical interrupt requests
- Output periodical pulse signals to the general ports

7.1.1 Features

- Generate eight type of pulse signals (128Hz, 64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz and 1Hz) by dividing the low-speed clock (LSCLK0 or LSCLK1)
- Four interrupt requests are selectable among eight periodical interrupt requests
- One of a pulse configured as interrupt requests is outputable from general ports
- An interrupt request is usable as a trigger event source of the Successive Approximation type A-D Converter, 16-bit timer and functional timer.
- Adjustable in a range approx.-488ppm to +488ppm with the resolution approx.0.48ppm.

7.1.2 Configuration

Figure 7-1 shows the configuration of the low speed time base counter.



LTBADJ	:	Low speed time base counter frequency adjustment register
T1HZ0 to T128HZ0	:	Time base counter 0 output signal
T1HZ1 to T128HZ1	:	Time base counter 1 output signal
LTB3INT	:	Low speed time base counter 3 interrupt request
LTB2INT	:	Low speed time base counter 2 interrupt request
LTB1INT	:	Low speed time base counter 1 interrupt request
LTB0INT	:	Low speed time base counter 0 interrupt request
TBCO	:	GPIO output as LTBC clock

Figure 7-1 Configuration of Low Speed Time Base Counter

7.1.3 List of Pins

The output pins of the low speed time base counter are assigned to the shared function of general purpose ports.

Signal name	I/O	Function
TBCO	O	The low speed time base counter output signal

Table 7-1 shows the list of the output ports and the register setting.

Table 7-1 Low speed time base counter function port and the register setting

Pin name	Shared port		Setting register	Setting value	ML62Q2700 Group				
					48pin product	54pin product	64pin product	80pin product	100pin product
TBCO	P20	7th function	P2MOD0	0110_XXXX*1	●	●	●	●	●
	P27	7th function	P2MOD7	0110_XXXX*1	●	●	●	●	●
	P31	7th function	P3MOD1	0110_XXXX*1	●	●	●	●	●
	P43	7th function	P4MOD3	0110_XXXX*1	●	●	●	●	●

●: Available - : Unavailable

*1 : XXXX determines the port output condition

XXXX	Port output condition
0010	CMOS output
1010	Nch open drain (without pull-up)
1111	Nch open drain (with pull-up)

7.2 Description of Registers

7.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF3A0	Low-speed Time Base Counter register	LTBR0	LTBR01	R/W	8/16	0x00
0xF3A1		LTBR1		R/W	8	0x00
0xF3A2	Low-speed Time Base Counter Control register	LTBCON0	LTBCON	R/W	8/16	0x03
0xF3A3		LTBCON1		R/W	8	0x02
0xF3A4	Reserved register	-	-	-	-	-
0xF3A5	Reserved register	-	-	-	-	-
0xF3A6	Low-speed Time Base Counter Frequency Adjustment register	LTBADJL	LTBADJ	R/W	8/16	0x00
0xF3A7		LTBADJH		R/W	8	0x00
0xF3A8	Low-speed Time Base Counter Interrupt selection register	LTBINTL	LTBINT	R/W	8/16	0x60
0xF3A9		LTBINTH		R/W	8	0x71

7.2.2 Low Speed Time Base Counter Register (LTBR01)

LTBR01 is a SFR to read the value of the low speed time base counter.
Writing any value to the LTBR0, the all bits of T128HZ0 to T1HZ0 are initialized to "0". Writing any value to the LTBR1, the all bits of T128HZ1 to T1HZ1 are initialized to "0". Writing any value to the LTBR01, the both are initialized to “0”.

Address: 0xF3A0(LTBR0/LTBR01), 0xF3A1(LTBR1)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	LTBR01															
Byte	LTBR1								LTBR0							
Bit	T1HZ1	T2HZ1	T4HZ1	T8HZ1	T16HZ1	T32HZ1	T64HZ1	T128HZ1	T1HZ0	T2HZ0	T4HZ0	T8HZ0	T16HZ0	T32HZ0	T64HZ0	T128HZ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

T128HZ0 to T1HZ0 / T128HZ1 to T1HZ1 signals have "0" level in the first half cycle and "1" level in the second half cycle. For example, T1HZ0 signal gets reset to "0" by writing any data to LTBR0 and it get to "1" about 0.5sec later and returns to "0" about 1sec later from the reset. The low-speed time base counter interrupt occurs at the falling edge ("1" to "0") of the signal. See Figure 7-4 "Low speed time base counter interrupt timing and reset timing of reset by writing to LTBR0" for details of the T128HZ0 to T1HZ0 / T128HZ1 to T1HZ1 waveform.

[Note]
- **A time base counter interrupt may occur depending on the timing to write to the LTBR01. See the program example for initializing described in Section 7.3.1 "Low Speed Time Base Counter Operation".**
- **Read the LTBR01 register twice to verify the data to prevent reading uncertain data while counting-up.**

7.2.3 Low Speed Time Base Counter Control Register (LTBCON)

LTBCON is a SFR to control the function of the time base counter.

Address: 0xF3A2(LTBCON0/LTBCON01), 0xF3A3(LTBCON1)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0203

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	LTBCON															
Byte	LTBCON1								LTBCON0							
Bit	TBOSEL1	TBOSEL0	-	-	TB1ADJEN	TB0ADJEN	TB1CK	TB0CK	-	-	-	-	-	-	TB1RUN	TB0RUN
R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1

Bit No.	Bit symbol name	Description
15,14	TBOSEL1 to 0	Select a signal as TBCO output. 00: LTB0INT (Initial value) 01: LTB1INT 10: LTB2INT 11: LTB3INT
13 to 12	-	Reserved bits
11	TB1ADJEN	Enable or disable adjustment of LTBR1. 0: Disabled (Initial value) 1: Enabled
10	TB0ADJEN	Enable or disable adjustment of LTBR0. 0: Disabled (Initial value) 1: Enabled
9	TB1CK	Not configurable. A clock of LTBR1 is LSCLK1. 1: LSCLK1 (Fixed)
8	TB0CK	Choose a clock of LTBR0. 0: LSCLK0 (Initial value) 1: LSCLK1
7 to 2	-	Reserved bits
1	TB1RUN	Control run/stop counter LTBR1. 0: Stop 1: Run (Initial value)
0	TB0RUN	Control run/stop counter LTBR0. 0: Stop 1: Run (Initial value)

[Note]
- **Stop counter LTBR0 (i.e. set 0 to TB0RUN bit) before TB0CK bit is configured.**

7.2.4 Low Speed Time base counter frequency adjustment register (LTBADJ)

LTBADJ is a SFR to set adjustment value for the frequency of time bask clock.

Address: 0xF3A6(LTBADJL/LTBADJ), 0xF3A7(LTBADJH)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	LTBADJ															
Byte	LTBADJH								LTBADJL							
Bit	-	-	-	-	-	LADJ10	LADJ9	LADJ8	LADJ7	LADJ6	LADJ5	LADJ4	LADJ3	LADJ2	LADJ1	LADJ0
R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 11	-	Reserved bits
10 to 0	LADJ10 to LADJ0	Specify the frequency adjustment ratio. See 7.3.2 "Time Base Counter Frequency Adjustment Function" for the relation of the setting data and the adjustable ppm.

7.2.5 Low Speed Time Base Counter Interrupt Selection Register (LTBINT)

LTBINT is a SFR to specify the low-speed time base clock to be used as an interrupt signal.

Address: 0xF3A8(LTBINTL/LTBINT), 0xF3A9(LTBINTH)
Access: R/W
Access size: 8/16 bit
Initial value: 0x7160

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	LTBINT															
Byte	LTBINTH								LTBINTL							
Bit	-	LTI3S2	LTI3S1	LTI3S0	-	LTI2S2	LTI2S1	LTI2S0	-	LTI1S2	LTI1S1	LTI1S0	-	LTI0S2	LTI0S1	LTI0S0
R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	1	1	1	0	0	0	1	0	1	1	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	-	Reserved bit
14 to 12	LTI3S2 to LTI3S0	Select the signal to be assigned to the time base counter interrupt 3 (LTB3INT). 000: T128HZ1 100: T8HZ1 001: T64HZ1 101: T4HZ1 010: T32HZ1 110: T2HZ1 011: T16HZ1 111: T1HZ1 (Initial value)
11	-	Reserved bit
10 to 8	LTI2S2 to LTI2S0	Select the signal to be assigned to the time base counter interrupt 2 (LTB2INT). 000: T128HZ1 100: T8HZ1 001: T64HZ1 (Initial value) 101: T4HZ1 010: T32HZ1 110: T2HZ1 011: T16HZ1 111: T1HZ1
7	-	Reserved bit
6 to 4	LTI1S2 to LTI1S0	Select the signal to be assigned to the time base counter interrupt 1 (LTB1INT). 000: T128HZ0 100: T8HZ0 001: T64HZ0 101: T4HZ0 010: T32HZ0 110: T2HZ0 (Initial value) 011: T16HZ0 111: T1HZ0
3	-	Reserved bit
2 to 0	LTI0S2 to LTI0S0	Select the signal to be assigned to the time base counter interrupt 0 (LTB0INT). 000: T128HZ0 (Initial value) 100: T8HZ0 001: T64HZ0 101: T4HZ0 010: T32HZ0 110: T2HZ0 011: T16HZ0 111: T1HZ0

[Note]

- **A time base counter interrupt may occur depending on a write timing to the LTBINT. See the program example for initializing described in 7.3.1 "Low Speed Time Base Counter Operation".**

7.3 Description of Operation

7.3.1 Low Speed Time Base Counter Operation

The low speed time base counter (LTBC) starts counting up from 0x0000 at the falling edge of the low-speed clock after releasing the system reset, then generates T128HZ0 to T1HZ0 / T128HZ1 to T1HZ1 signals. Two factors can be chosen from T128HZ0 to T1HZ0 signals, and two factors can be chosen from T128HZ1 to T1HZ1 signals. There are to generate periodical low-speed time base counter interrupt requests.
Values of T128HZ0 to T1HZ0 / T128HZ1 to T1HZ1 signals can be read from the LTBR01 register.
The low-speed time base counter interrupt request is generated at the falling edge of a signal chosen in the LTBINT register.

When changing the assignment of interrupt signals in the LTBINT register, low-speed time base counter interrupt requests (LTBnINT) may be generated depending on write timing to the register. Therefore, change the value in the LTBINT register with the interrupt disabled in the IE67 register before changing the assignment of interrupt signals, and clear the generated low-speed time base counter interrupt request bit (QLTBCn) to "0". (n = 0 to 3)

Figure 7-2 shows a sample program for changing the assignment of low-speed time base counter signals.

```
ELTBC0 = 0;       // Disable LTBC0 interrupt
ELTBC1 = 0;       // Disable LTBC1 interrupt
ELTBC2 = 0;       // Disable LTBC2 interrupt
ELTBC3 = 0;       // Disable LTBC3 interrupt
LTBINT = 0x0741;// Change assignment of interrupt signal
__asm("NOP");     // Waiting time
QLTBC0 = 0;       // Clear QLTBC0
QLTBC1 = 0;       // Clear QLTBC1
QLTBC2 = 0;       // Clear QLTBC2
QLTBC3 = 0;       // Clear QLTBC3
ELTBC0 = 1;       // Enable LTBC0 interrupt
ELTBC1 = 1;       // Enable LTBC1 interrupt
ELTBC2 = 1;       // Enable LTBC2 interrupt
ELTBC3 = 1;       // Enable LTBC3 interrupt
```

Figure 7-2 Sample Program for Changing Assignment of Low-speed Time Base Counter Signals

The time equivalent to one clock of the system clock is required for the low-speed time base counter interrupt request bit (QLTBCn bit of IRQ67 register, n=0 to 3) to become "1" after changing the LTBINT register . Therefore, place two NOP instruction after changing the LTBINT register.

When writing arbitrary data to the LTBR0 register, T128HZ0 to T1HZ0 signals of the LTBR01 register are all initialized to "0". When writing arbitrary data to the LTBR1 register, T128HZ1 to T1HZ1 signals of the LTBR01 register are all initialized to "0". When writing arbitrary data to the LTBR01 register, all bits of LTBR01 register are initialized to “0”. Depending on timing to write to the LTBR register, the signal assigned to the LTBINT register may change from "1" to "0". Also a low-speed time base counter interrupt request may occur. Therefore, with the low-speed time base counter interrupt disabled in the IE67 register, following writing to the LTBR register, clear the generated low-speed time base counter interrupt request bit (the QLTBCn bit of the IRQ67 register) to "0". (n = 0 to 3)

Figure 7-3 shows a sample program for initializing the LTBR0 register.

```
__DI();           // Disable interrupt (MIE=0)
LTBR0 = 0x00;     // Reset LTBR0
__asm("NOP");     // Waiting time
__asm("NOP");     // Waiting time
QLTBC0 = 0;       // Clear QLTBC0
QLTBC1 = 0;       // Clear QLTBC1
__EI();           // Enable interrupt (MIE=1)
```

Figure 7-3 Sample Program for Initializing LTBR0 Register

It takes one cycle of the system clock for QLTBCn to become "1" from writing to the LTBR register. Therefore, place two NOP instruction after writing to the LTBR01 register.

Figure 7-4 shows the low-speed time base counter interrupt request generation timing when choosing T128HZ0, T16HZ0, and T2HZ0 as interrupt factors in the LTBINT register, and shows the reset timing by writing to LTBR0.

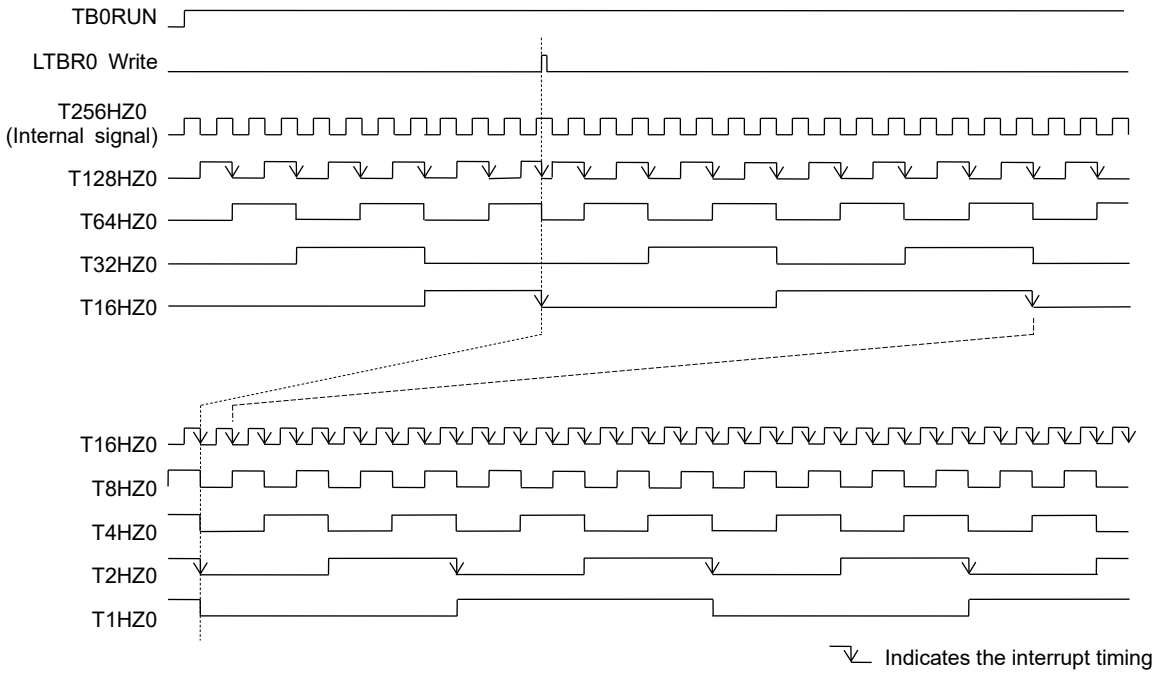


Figure 7-4 Low-speed Time Base Counter Interrupt Timing and Reset Timing by Writing to LTBR0 Register

[Note]

- **After writing to the LTBR01 register, the time by which the first low-speed time base counter interrupt request is generated is not guaranteed. If measuring the time using the low-speed time base counter interrupt, do so with reference to the interrupt generation interval.**

7.3.2 Low Speed Time Base Counter Frequency Adjustment Function

For T128HZ0 to T1HZ0 / T128HZ1 and T1HZ1 of the low-speed time base counter, the frequency can be adjusted using the low-speed time base counter frequency adjustment register (LTBADJ). Measure the signal output from the TBCO pin, then adjust the frequency using the LTBADJ register. The adjustment range and resolution are as follows:

- Adjustment range : Approx. -488 ppm to +488 ppm
- Adjustment resolution : Approx. 0.477 ppm

The following is available to confirm the adjusted frequency:

Frequency adjustment mode	Description
Normal frequency adjustment mode	This is used to confirm that 64 seconds includes exactly 128 cycles (or 64 cycles) of T2HZ0/T2HZ1 (or T1HZ0/T1HZ1),which is output form pin as TBCO under operating with actual adjusted low-speed clock.

Table 7-2 shows the frequency adjustment value set in the LTBADJ and adjustment ratio.

Table 7-2 Frequency adjustment value set in the LTBADJ and Adjustment ratio

LADJ10-0											Hex.	Frequency adjustment ratio (ppm)
0	1	1	1	1	1	1	1	1	1	1	3FFH	+487.80
0	1	1	1	1	1	1	1	1	1	0	3FEH	+487.33
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	1	1	003H	+1.43
0	0	0	0	0	0	0	0	0	1	0	002H	+0.95
0	0	0	0	0	0	0	0	0	0	1	001H	+0.48
0	0	0	0	0	0	0	0	0	0	0	000H	0
1	1	1	1	1	1	1	1	1	1	1	7FFH	-0.48
1	1	1	1	1	1	1	1	1	1	0	7FEH	-0.95
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	1	401H	-487.80
1	0	0	0	0	0	0	0	0	0	0	400H	-488.28

The correction values (LADJ10 to LADJ0) set in the LTBADJ register can be calculated using the following formula.

Correction value = Frequency adjustment ratio x 2097152 (decimal)
= Frequency adjustment ratio x 200000h (hexadecimal)

Example 1: When adjusting +15.0 ppm (when the clock loses)
Correction value = +15.0 ppm x 2097152 (decimal)
= $+15.0 \times 10^{-6} \times 2097152$
= +31.45728 (decimal)
≈ 1Fh (hexadecimal)

Example 2: When adjusting -25.5 ppm (when the clock gains)
Correction value = -25.5 ppm x 2097152 (decimal)
= $-25.5 \times 10^{-6} \times 2097152$
= -53.477376 (decimal)
≈ 7CBh (hexadecimal)

[Note]

- **The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the low-speed oscillation (32.768 kHz) due to temperature variations.**

Chapter 8 16-Bit Timer

8. 16-Bit Timer

8.1 General Description

The 16-bit timer enables following functions.

- Generate periodical interrupts in an arbitrary period
- Generate one shot interrupts in an arbitrary period
- Output pulse signals with an arbitrary frequency to the general ports
- Output one shot pulse signals to the general ports

The timer X is shared function for stability controlling of crystal oscillation. When un-used crystal oscillation, it is used as normal 16-bit timer.
See Chapter 6 "Clock generation circuit" for function for stability controlling of crystal oscillation.

Table 8-1 shows the number of channels.

Table 8-1 Number of 16-bit Timer channels

Product	Channel Number	Timer X
ML62Q2747	0 to 6	•
ML62Q2746		
ML62Q2745		
ML62Q2737		
ML62Q2736		
ML62Q2735		
ML62Q2727		
ML62Q2726		
ML62Q2725		
ML62Q2723	0 to 4	
ML62Q2722		
ML62Q2713		
ML62Q2712		
ML62Q2703		
ML62Q2702		

8.1.1 Features

Operation mode	Description
Repeat mode	Count-able to the max. 0xffff Repeat the specified operation until stop by the software.
One shot mode	Count-able to the max. 0xffff Run the specified operation once and stop it.

- Selectable counter clock from various sources (divided by 1 to 8 of LSCLK0, LSCLK1, HSCLK, HTBCLK0, HTBCLK1, RC1K, external clock, LTBC interrupt, functional timer triggers)
- A timer interrupt request is generated when the value of the timer counter register value coincides with that of the 16-bit timer n data register
- A port output is reversed when the value of the timer counter register value coincides with that of the 16-bit timer n data register
- The initial level of the port can be slected by a register.

8.1.2 Configuration

Figure 8-1 shows configuration of the 16-bit timer

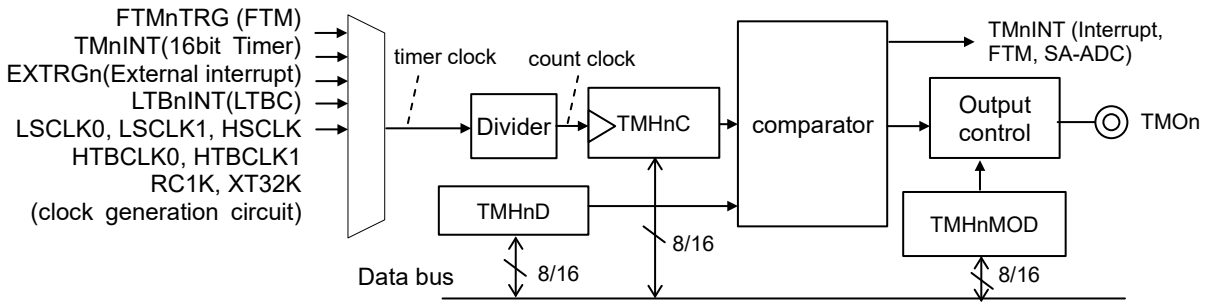


Figure 8-1 Configuration of the timer

TMnINT	: 16-bit timer n interrupt request
EXTRGn	: EXIn pin input (come through the noise filter of the external interrupt function)
TMHnD	: 16-bit timer n data register
TMHnC	: 16-bit timer n counter register
TMHnMOD	: 16-bit timer n mode register

8.1.3 List of Pin

The I/O pins of the 16-bit timer are assigned to the shared function of the general ports.

Pin name	I/O	Description
EXIn	I	External clock (used as EXTRGn). The max input frequency is 3MHz.
TMO0	O	16-bit timer channel 0 output
TMO1	O	16-bit timer channel 1 output
TMO2	O	16-bit timer channel 2 output
TMO3	O	16-bit timer channel 3 output
TMO4	O	16-bit timer channel 4 output
TMO5	O	16-bit timer channel 5 output
TMO6	O	16-bit timer channel 6 output
TMOX	O	16-bit timer channel X output

Table 8-2 shows the list of the general ports used in the 16-bit timer and the register settings of the ports.

Table 8-2 Ports used in the 16-bit timer and the register settings

Pin name	Shared port		Register	Setting value	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702			ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725		
					48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
EXI0	Ports assigned for external interrupt. See Chapter 18 External interrupt.				●	●	●	●	●	●
EXI1					●	●	●	●	●	●
EXI2					●	●	●	●	●	●
EXI3					●	●	●	●	●	●
EXI4					●	●	●	●	●	●
EXI5					●	●	●	●	●	●
EXI6					●	●	●	●	●	●
EXI7					●	●	●	●	●	●
TMO0	P04	6th Func.	P0MOD4	0101_XXXX*1	●	●	●	●	●	●
TMO1	P13	6th Func.	P1MOD3	0101_XXXX*1	●	●	●	●	●	●
TMO2	P23	6th Func.	P2MOD3	0101_XXXX*1	●	●	●	●	●	●
TMO3	P13	7th Func.	P1MOD3	0110_XXXX*1	●	●	●	●	●	●
	P33	6th Func.	P3MOD3	0101_XXXX*1	●	●	●	●	●	●
TMO4	P12	6th Func.	P1MOD2	0101_XXXX*1	●	●	●	●	●	●
TMO5	P16	6th Func.	P1MOD6	0101_XXXX*1	-	-	-	●	●	●
TMO6	P70	6th Func.	P7MOD0	0101_XXXX*1	-	-	-	●	●	●
TMOX	P54	6th Func.	P5MOD4	0101_XXXX*1	-	-	●	●	●	●

●: Available to use -: Unavailable

*1 : "XXXX" determines the condition of the port output

XXXX	Condition of the port output
0010	CMOS output
1010	Nch open drain output (without the pull-up)
1111	Nch open drain output (with the pull-up)

8.2 Description of Registers

8.2.1 List of Registers

Registers for unequipped channels are not available to use. They return 0x0000 for reading.

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF300	16-bit timer 0 data register	TMH0DL	TMH0D	R/W	8/16	0xFF
0xF301		TMH0DH		R/W	8	0xFF
0xF302	16-bit timer 0 counter register	TMH0CL	TMH0C	R/W	8/16	0x00
0xF303		TMH0CH		R/W	8	0x00
0xF304	16-bit timer 0 mode register	TMH0MODL	TMH0MOD	R/W	8/16	0x00
0xF305		TMH0MODH		R/W	8	0x00
0xF306	Reserved register	-	-	-	-	-
0xF307						
0xF308	16-bit timer 1 data register	TMH1DL	TMH1D	R/W	8/16	0xFF
0xF309		TMH1DH		R/W	8	0xFF
0xF30A	16-bit timer 1 counter register	TMH1CL	TMH1C	R/W	8/16	0x00
0xF30B		TMH1CH		R/W	8	0x00
0xF30C	16-bit timer 1 mode register	TMH1MODL	TMH1MOD	R/W	8/16	0x00
0xF30D		TMH1MODH		R/W	8	0x00
0xF30E	Reserved register	-	-	-	-	-
0xF30F						
0xF310	16-bit timer 2 data register	TMH2DL	TMH2D	R/W	8/16	0xFF
0xF311		TMH2DH		R/W	8	0xFF
0xF312	16-bit timer 2 counter register	TMH2CL	TMH2C	R/W	8/16	0x00
0xF313		TMH2CH		R/W	8	0x00
0xF314	16-bit timer 2 mode register	TMH2MODL	TMH2MOD	R/W	8/16	0x00
0xF315		TMH2MODH		R/W	8	0x00
0xF316	Reserved register	-	-	-	-	-
0xF317						
0xF318	16-bit timer 3 data register	TMH3DL	TMH3D	R/W	8/16	0xFF
0xF319		TMH3DH		R/W	8	0xFF
0xF31A	16-bit timer 3 counter register	TMH3CL	TMH3C	R/W	8/16	0x00
0xF31B		TMH3CH		R/W	8	0x00
0xF31C	16-bit timer 3 mode register	TMH3MODL	TMH3MOD	R/W	8/16	0x00
0xF31D		TMH3MODH		R/W	8	0x00
0xF31E	Reserved register	-	-	-	-	-
0xF31F						
0xF320	16-bit timer 4 data register	TMH4DL	TMH4D	R/W	8/16	0xFF
0xF321		TMH4DH		R/W	8	0xFF
0xF322	16-bit timer 4 counter register	TMH4CL	TMH4C	R/W	8/16	0x00
0xF323		TMH4CH		R/W	8	0x00
0xF324	16-bit timer 4 mode register	TMH4MODL	TMH4MOD	R/W	8/16	0x00
0xF325		TMH4MODH		R/W	8	0x00
0xF326	Reserved register	-	-	-	-	-
0xF327						

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF328	16-bit timer 5 data register	TMH5DL	TMH5D	R/W	8/16	0xFF
0xF329		TMH5DH		R/W	8	0xFF
0xF32A	16-bit timer 5 counter register	TMH5CL	TMH5C	R/W	8/16	0x00
0xF32B		TMH5CH		R/W	8	0x00
0xF32C	16-bit timer 5 mode register	TMH5MODL	TMH5MOD	R/W	8/16	0x00
0xF32D		TMH5MODH		R/W	8	0x00
0xF32E	Reserved register	-	-	-	-	-
0xF32F						
0xF330	16-bit timer 6 data register	TMH6DL	TMH6D	R/W	8/16	0xFF
0xF331		TMH6DH		R/W	8	0xFF
0xF332	16-bit timer 6 counter register	TMH6CL	TMH6C	R/W	8/16	0x00
0xF333		TMH6CH		R/W	8	0x00
0xF334	16-bit timer 6 mode register	TMH6MODL	TMH6MOD	R/W	8/16	0x00
0xF335		TMH6MODH		R/W	8	0x00
0xF336	Reserved register	-	-	-	-	-
0xF337						
0xF340	16-bit timer start register	TMHSTRL	TMHSTR	W	8/16	0x00
0xF341		TMHSTRH		W	8	0x00
0xF342	16-bit timer stop register	TMHSTPL	TMHSTP	W	8/16	0x00
0xF343		TMHSTPH		W	8	0x00
0xF344	16-bit timer status register	TMHSTATL	TMHSTAT	R	8/16	0x00
0xF345		TMHSTATH		R	8	0x00
0xF346	Reserved register	-	-	-	-	-
0xF347						
0xF350	16-bit timer X data register	TMHXDL	TMHXD	R/W	8/16	0xFF
0xF351		TMHXDH		R/W	8	0xFF
0xF352	16-bit timer X counter register	TMHXCL	TMHXC	R/W	8/16	0x00
0xF353		TMHXCH		R/W	8	0x00
0xF354	16-bit timer X mode register	TMHXMODL	TMHXMOD	R/W	8/16	0x00
0xF355		TMHXMODH		R/W	8	0x00
0xF356	Reserved register	-	-	-	-	-
0xF357						
0xF358	16-bit timer X start register	TMHXSTR	-	W	8	0x00
0xF359	Reserved register	-	-	-	-	-
0xF35A	16-bit timer X stop register	TMHXSTP	-	W	8	0x00
0xF35B	Reserved register	-	-	-	-	-
0xF35C	16-bit timer X status register	TMHXSTAT	-	R	8	0x00
0xF35D	Reserved register	-	-	-	-	-
0xF35E	Reserved register	-	-	-	-	-
0xF35F						

8.2.2 16-Bit Timer n Data Register (TMHnD: n=0 to 6, X)

TMHnD is a SFR to set the comparison value with the 16-bit timer n counter register (TMHnC).

Address: 0xF300(TMH0DL/TMH0D), 0xF301(TMH0DH), 0xF308(TMH1DL/TMH1D), 0xF309(TMH1DH)
0xF310(TMH2DL/TMH2D), 0xF311(TMH2DH), 0xF318(TMH3DL/TMH3D), 0xF319(TMH3DH)
0xF320(TMH4DL/TMH4D), 0xF321(TMH4DH), 0xF328(TMH5DL/TMH5D), 0xF329(TMH5DH)
0xF330(TMH6DL/TMH6D), 0xF331(TMH6DH),
0xF350(TMHXDL/TMHXD), 0xF351(TMHXDH)
Access : R/W
Access size : 8/16 bit
Initial value : 0xFFFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	TMHnD															
Byte	TMHnDH								TMHnDL							
Bit	THnD15	THnD14	THnD13	THnD12	THnD11	THnD10	THnD9	THnD8	THnD7	THnD6	THnD5	THnD4	THnD3	THnD2	THnD1	THnD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

[Note]

- **Set TMHnD register when the 16-bit timer n is stopped (THnSTATL bits of TMHSTAT register are "0"). If the register is changed during operation, the operation is not guaranteed.**
- **When "0x0000" is written in TMHnD in the 16-bit timer mode, "0x0001" is set in TMHnD.**
- **Set TMHnD so that the timer output frequency is 4MHz or less, when timer output is used.**
  The count clock frequency [MHz] / (TMHnD value + 1) x 2 ≤ 4 [MHz] , so that
  TMHnD value ≥ (count clock frequency [MHz] / 2 / 4) – 1 .

8.2.3 16-Bit Timer n Counter Register (TMHnC: n=0 to 6, X)

TMHnC is a SFR that functions as a 16-bit binary counter.
This is reset to 0x0000 at the reset function and also when the following event occurred.

- When an arbitrary value is written in this register
- When the value of TMHnD register coincides with that of the TMHnC register

Address : 0xF302(TMH0C/TMH0CL), 0xF303(TMH0CH), 0xF30A(TMH1C/TMH1CL), 0xF30B(TMH1CH)
0xF312(TMH2C/TMH2CL), 0xF313(TMH2CH), 0xF31A(TMH3C/TMH3CL), 0xF31B(TMH3CH)
0xF322(TMH4C/TMH4CL), 0xF323(TMH4CH), 0xF32A(TMH5C/TMH5CL), 0xF32B(TMH5CH)
0xF332(TMH6C/TMH6CL), 0xF333(TMH6CH),
0xF352(TMHXC/TMHXCL), 0xF353(TMHXCH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	TMHnC															
Byte	TMHnCH								TMHnCL							
Bit	THnC15	THnC14	THnC13	THnC12	THnC11	THnC10	THnC9	THnC8	THnC7	THnC6	THnC5	THnC4	THnC3	THnC2	THnC1	THnC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This data is counted up synchronizing at the rising edge of the count clock.
Reading value is always available if timer clock source is as same as system clock source.

An available condition:

System clock	Timer clock
LSCLK0	LSCLK0
	LSCLK1 where the source clock is as same as one of LSCLK0.
	LTBnINT where the source clock is as same as one of LSCLK0.
HSCLK or divided HSCLK	HSCLK
	HTBCLK0
	HTBCLK1

[Note]

- **Read TMHnC register twice to verify the valid data to prevent reading uncertain data while counting-up, if a source of timer clock is as different as one of system clock.**
  In case of SYSCLK frequency = 250kHz, the count clock frequency = 3MHz:
  If first read value is 0x0007, second read value is more than 0x0012. Valid bits are 11 bits of THnC15-5. It depend on reading interval time.

8.2.4 16-Bit Timer n Mode Register (TMHnMOD: n=0 to 6, X)

TMHnMOD is a SFR to control the operation mode of 16-bit timer.

Address : 0xF304(TMH0MODL/TMH0MOD), 0xF305(TMH0MODH),
0xF30C(TMH1MODL/TMH1MOD), 0xF30D(TMH1MODH),
0xF314(TMH2MODL/TMH2MOD), 0xF315(TMH2MODH),
0xF31C(TMH3MODL/TMH3MOD), 0xF31D(TMH3MODH),
0xF324(TMH4MODL/TMH4MOD), 0xF325(TMH4MODH),
0xF32C(TMH5MODL/TMH5MOD), 0xF32D(TMH5MODH),
0xF334(TMH6MODL/TMH6MOD), 0xF335(TMH6MODH),
0xF354(TMHXMODL/TMHXMOD), 0xF355(TMHXMODH),
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	TMHnMOD															
Byte	TMHnMODH								TMHnMODL							
Bit	-	-	-	-	-	THn NEG	THn OST	-	-	-	THn DIV1	THn DIV0	THnCK 3	THnCK 2	THnC K1	THnCK 0
R/W	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 11	-	Reserved bits
10	THnNEG	Select the output polarity of timer out (TMOn). 0: Positive logic (initial level is "L") (Initial value) 1: Negative logic (initial level is "H")
9	TLnOST	Select the operation mode. 0: Repeat mode (Initial value) 1: One-shot mode
8 to 6	-	Reserved bits
5 to 4	THnDIV1 to THnDIV0	Select frequency dividing ratio for the count clock 00: No dividing (Initial value) 01: Divided by 2 10: Divided by 4 11: Divided by 8
3 to 0	THnCK3 to THnCK0	Select the timer clock source. See Table 8-3 for detail. THXCK3 of timer X is reserved bit that is fixed 0.

Table 8-3 timer clock list

THnCLK3-0	0	1	2	3	4	5	6	X
0000	LSCLK0	LSCLK0	LSCLK0	LSCLK0	LSCLK0	LSCLK0	LSCLK0	LSCLK0
0001	HSCLK	HSCLK	HSCLK	HSCLK	HSCLK	HSCLK	HSCLK	HSCLK
0010	LSCLK1	LSCLK1	LSCLK1	LSCLK1	LSCLK1	LSCLK1	LSCLK1	LSCLK1
0011	HTBCLK0	HTBCLK0	HTBCLK0	HTBCLK0	HTBCLK0	HTBCLK0	HTBCLK0	HTBCLK0
0100	HTBCLK1	HTBCLK1	HTBCLK1	HTBCLK1	HTBCLK1	HTBCLK1	HTBCLK1	XT32K for stability.
0101	LTB1INT	LTB1INT	LTB1INT	LTB1INT	LTB1INT	LTB1INT	LTB1INT	RC1K
0110	LTB2INT	LTB2INT	LTB2INT	LTB2INT	LTB2INT	LTB2INT	LTB2INT	rsvd
0111	LTB3INT	LTB3INT	LTB3INT	LTB3INT	LTB3INT	LTB3INT	LTB3INT	-
1000	EXTRG0	EXTRG0	FTM0TRG	FTM0TRG	FTM0TRG	FTM0TRG	FTM0TRG	-
1001	EXTRG1	EXTRG1	FTM1TRG	FTM1TRG	FTM1TRG	FTM1TRG	FTM1TRG	-
1010	EXTRG2	EXTRG2	EXTRG2	EXTRG2	EXTRG2	TM0INT	TM0INT	-
1011	EXTRG3	EXTRG3	EXTRG3	EXTRG3	EXTRG3	TM1INT	TM1INT	-
1100	EXTRG4	TM0INT	TM0INT	EXTRG4	EXTRG4	EXTRG4	EXTRG4	-
1101	TM1INT	EXTRG5	TM1INT	EXTRG5	EXTRG5	EXTRG5	EXTRG5	-
1110	TM2INT	TM2INT	EXTRG6	EXTRG6	EXTRG6	EXTRG6	EXTRG6	-
1111	TM3INT	TM3INT	TM3INT	EXTRG7	EXTRG7	EXTRG7	EXTRG7	-

LTBnINT : Low speed time base counter interrupt
EXTRGn : External interrupt trigger output
TMnINT : 16bit timer trigger output
FTMnTRG : Functional timer trigger output
RC1K : RC1K clock output
XT32K for stability : It is divided by 2 of XT32K/EXT32K. It is used to count for stability time only.

[Note]

- **Set TMHnMOD when the timer n is stopped (THnSTAT bits of TMHSTAT/TMHXSTAT register are "0"). If it is changed while it is operating, the operation is not guaranteed.**

8.2.5 16-Bit Timer Start Register (TMHSTR)

TMHSTR is a SFR to control to start counting the 16-bit timer n.
This is a write-only register and returns always "0x0000"for reading.

Address : 0xF340
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	TMHSTR															
Byte	TMHSTRH								TMHSTRL							
Bit	-	-	-	-	-	-	-	-	-	TH6RUN	TH5RUN	TH4RUN	TH3RUN	TH2RUN	TH1RUN	TH0RUN
R/W	R	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is used to start a target timer.
Writing "0": Invalid
Writing "1": Start counting

Bit No.	Bit symbol name	Description (target)
15 to7	-	Reserved bits
6	TH6RUN	16-bit timer 6
5	TH5RUN	16-bit timer 5
4	TH4RUN	16-bit timer 4
3	TH3RUN	16-bit timer 3
2	TH2RUN	16-bit timer 2
1	TH1RUN	16-bit timer 1
0	TH0RUN	16-bit timer 0

8.2.6 16-Bit Timer Stop Register (TMHSTP)

TMHSTP is a SFR to control to stop counting the 16-bit timer n.
This is a write-only register and returns always "0x0000"for reading.

Address : 0xF342
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	TMHSTP															
Byte	TMHSTPH								TMHSTPL							
Bit	-	-	-	-	-	-	-	-	-	TH6STP	TH5STP	TH4STP	TH3STP	TH2STP	TH1STP	TH0STP
R/W	R	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is used to stop a target timer.
Writing "0": Invalid
Writing "1": Stop counting

Bit No.	Bit symbol name	Description (target)
15 to 7	-	Reserved bits
6	TH6STP	16-bit timer 6
5	TH5STP	16-bit timer 5
4	TH4STP	16-bit timer 4
3	TH3STP	16-bit timer 3
2	TH2STP	16-bit timer 2
1	TH1STP	16-bit timer 1
0	TH0STP	16-bit timer 0

8.2.7 16-Bit Timer Status Register (TMHSTAT)

TMHSTAT is a SFR to indicate the status of the 16-bit timer n.

Address : 0xF344
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	TMHSTAT															
Byte	TMHSTATH								TMHSTATL							
Bit	-	-	-	-	-	-	-	-	-	TH6STAT	TH5STAT	TH4STAT	TH3STAT	TH2STAT	TH1STAT	TH0STAT
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is used to indicate an operating status of a target timer
0: A counting of target timer is stopped (Initial value)
1: A counting of target timer is progress

Bit No.	Bit symbol name	Description (target)
15 to 7	-	Reserved bits
6	TH6STAT	16-bit timer 6
5	TH5STAT	16-bit timer 5
4	TH4STAT	16-bit timer 4
3	TH3STAT	16-bit timer 3
2	TH2STAT	16-bit timer 2
1	TH1STAT	16-bit timer 1
0	TH0STAT	16-bit timer 0

8.2.8 16-Bit Timer X Start Register (TMHXSTR)

TMHXSTR is a SFR to control to start counting the 16-bit timer X.
This is a write-only register and returns always "0x0000"for reading.

Address : 0xF358
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								TMHXSTR							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	THXRUN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	THXRUN	Start timer X. Writing "0":Invalid Writing "1":Start counting

8.2.9 16-Bit Timer X Stop Register (TMHXSTP)

TMHXSTP is a SFR to control to stop counting the 16-bit timer X.
This is a write-only register and returns always "0x0000"for reading.

Address : 0xF35A
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								TMHXSTP							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	THXSTP
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	THXSTP	Stop timer X. Writing "0":Invalid Writing "1":Stop counting

8.2.10 16-Bit Timer X Status Register (TMHXSTAT)

TMHXSTAT is a SFR to indicate the status of the 16-bit timer X.

Address : 0xF35C
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								TMHXSTAT							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	THXSTAT
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	THXSTAT	Indicate an operating status of timer X. 0: A counting of target timer is stopped (Initial value) 1: A counting of target timer is progress

8.3 Description of Operation

8.3.1 Operation Mode

Writing "1" to THnRUN bit causes the 16-bit counter n to start counting up in synchronization with the rising edges of the count clock.
If output of the general-purpose port is enabled by choosing the timer output (TMOn) through the shared function setting of the port, the output of the port is reversed when the timer count value matches with TMHnD register value. In addition, writing "1" to THnSTP bit during counting causes the counting to stop in synchronization with the count clock and the output of the port is reset to the initial value. For the initial value of the port, "H" and "L" levels can be chosen through THnNEG bit of TMHnMOD register.

Following two operation modes are available:

- Repeat mode
- One-shot mode

8.3.1.1 Repeat Mode

Figure 8-2 shows the repeat mode operation.

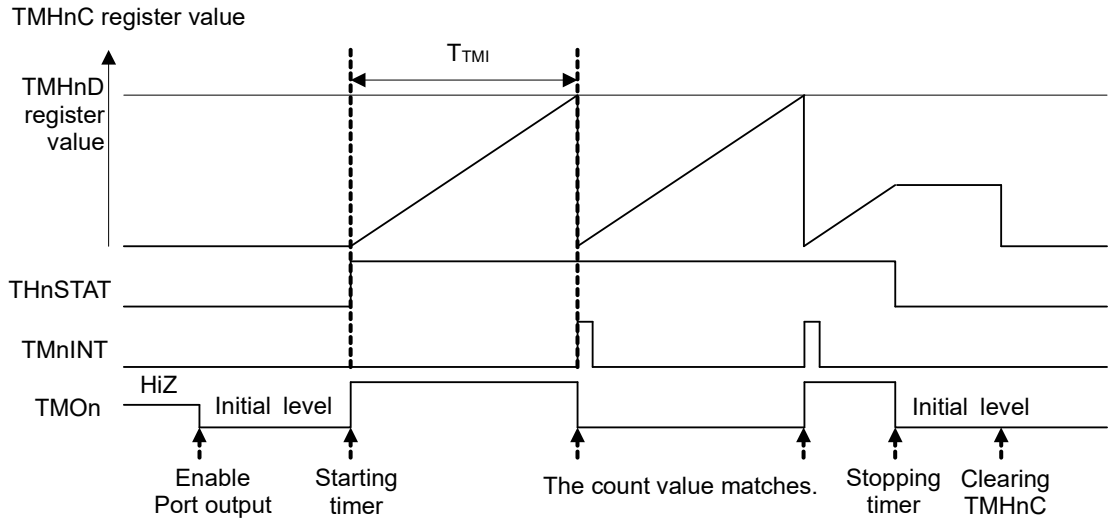


Figure 8-2 Repeat Mode Operation Timing

In the repeat mode, when the timer count value matches with TMHnD register, 16-bit timer n interrupt request (TMnINT) is generated and the output of the port is reversed. Then, the timer count value automatically is reset to "0x0000" and the counting up operation is continued.
TMnINT generation cycle and the port output reverse cycle can be expressed in the following formula:

$$TTMI = \frac{TMHnD + 1}{fTHnCK \quad (Hz)} \qquad (n=0 \text{ to } 6, X)$$

TMHnD : TMHnD register setting value (0x0001 to 0xFFFF)
fTHnCK : Count clock frequency chosen in TMHnMOD register

See Section 8.3.2 "Start/Stop Timing" for the timing of the timer start/stop and counting up.

8.3.1.2 One-shot Mode

Figure 8-3 shows the one-shot mode operation

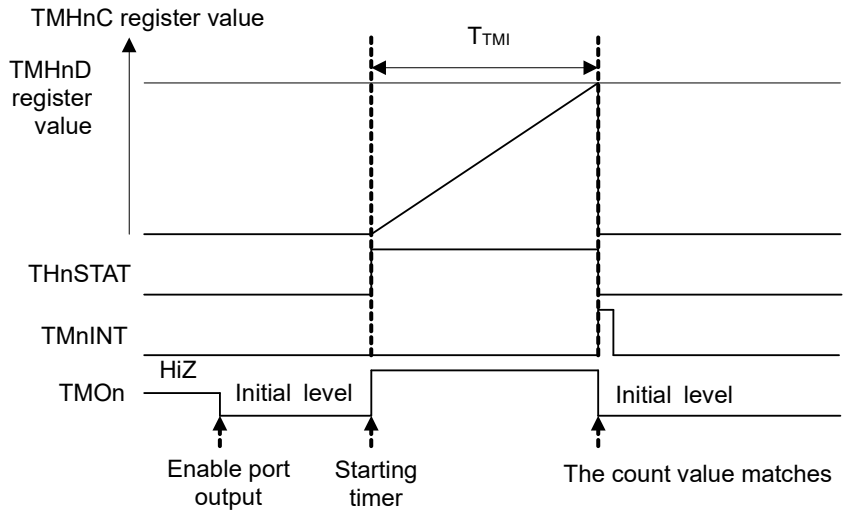


Figure 8-3 One-shot Mode Operation Timing

In the one-shot mode, when the timer count value matches with TMHnD register, 16-bit timer n interrupt (TMnINT) is generated and the value of the port is reversed. Then, the timer count value is reset to "0x0000" and the counting is stopped.
TMnINT generation cycle and the port output reverse cycle are the same as those in the repeat mode. The same applies to the timer start/stop timing and counting up timing.

8.3.2 Start/Stop Timing

Writing "1" to THnRUN bit of TMHSTR register causes the counting operation to start at the rising edge of the timer clock after the falling edge of the timer clock.
Figure 8-4 shows the timer start timing when the timer clock setting (THnCK3 to 0) is 0000 to 0111 and frequency dividing ratio of the count clock is 1/2 of the timer clock.

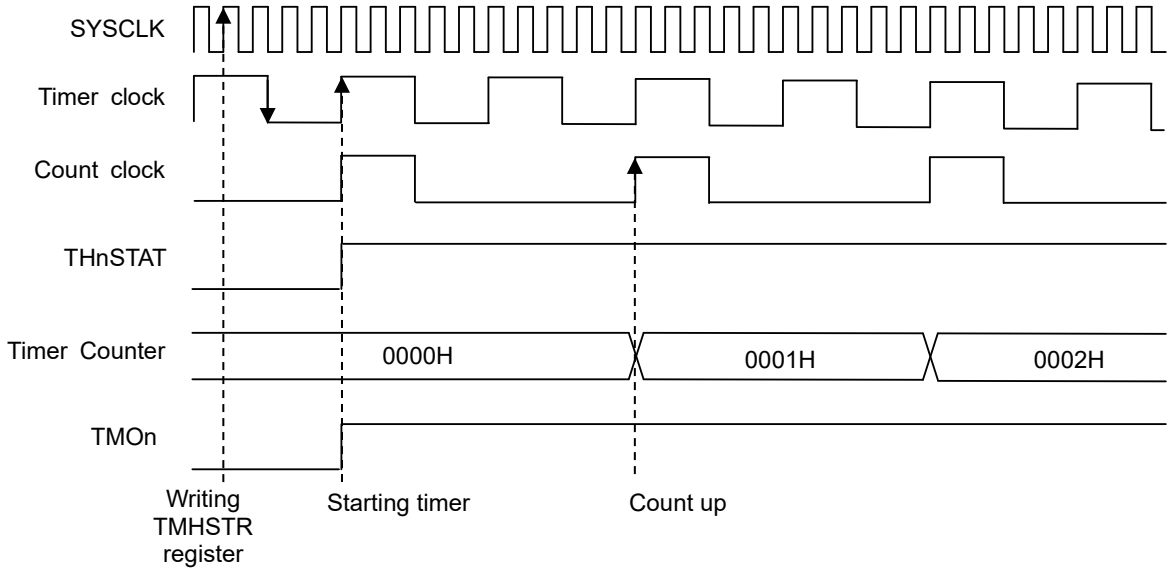


Figure 8-4 Start Timing (in case of THnCK3-0 = 0000 to 0111)

Figure 8-5 shows the timer start timing when the timer clock setting (THnCK3-0) is 1000~1111 and the count clock is set to divide by 2.

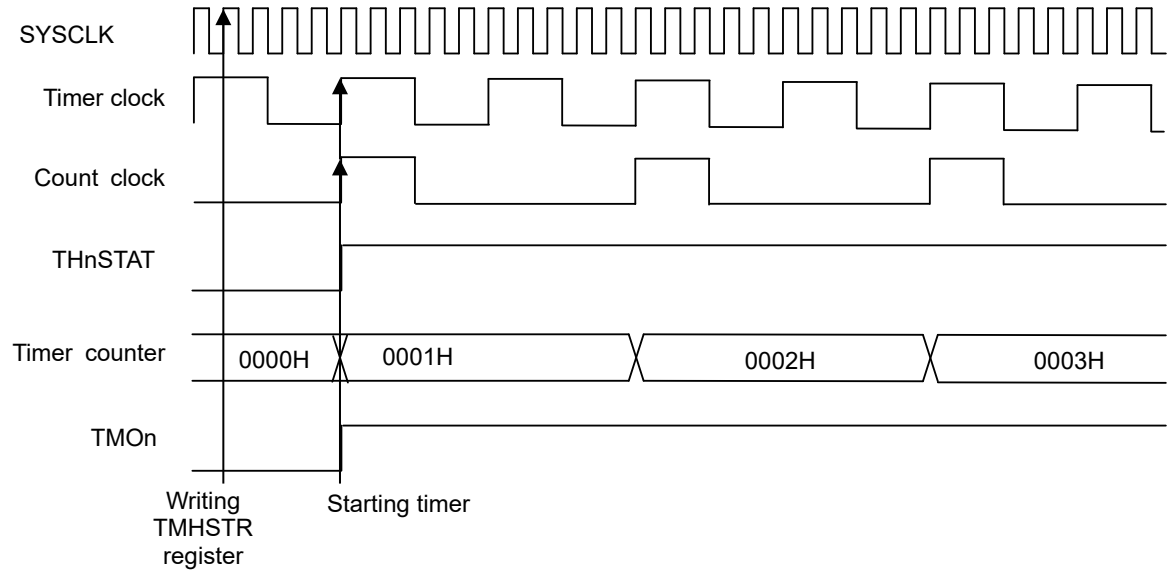


Figure 8-5 Start Timing (in case of THnCK3-0 = 1000 to 1111)

Writing "1" to THnSTP bit of TMHSTP register causes the counting operation to stop at the rising edge of the timer clock that follows.
Figure 8-6 shows the timer stop timing when the timer clock is LSCLK0 and frequency dividing ratio of the count clock is 1/2 of the timer clock.

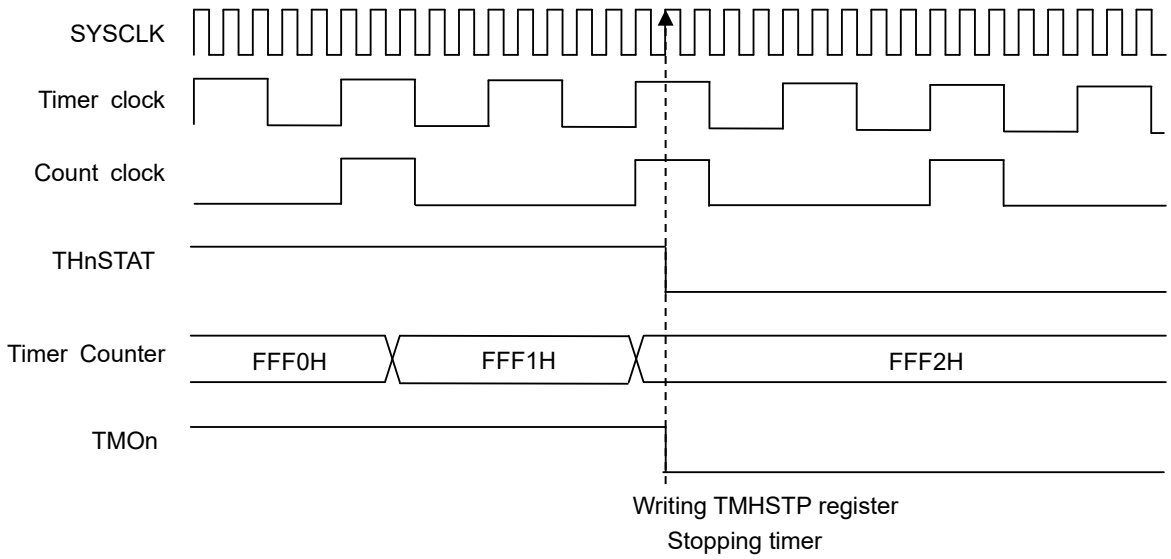


Figure 8-6 Stop Timing

[Note]

- **After THnRUN bit is set to "1", the first interrupt has a time error equivalent to maximum of one clock of the timer clock because the counting operation starts in synchronization with the timer clock. The 2nd timer interrupt or later interrupts have constant cycles.**
- **After THnSTP bit is set to "1", a 16-bit timer n interrupt (TMnINT) may be generated depending on the stop timing because the counting operation stops in synchronization with the timer clock.**

8.3.3 Setting Example

Figure 8-7 shows a setting example.

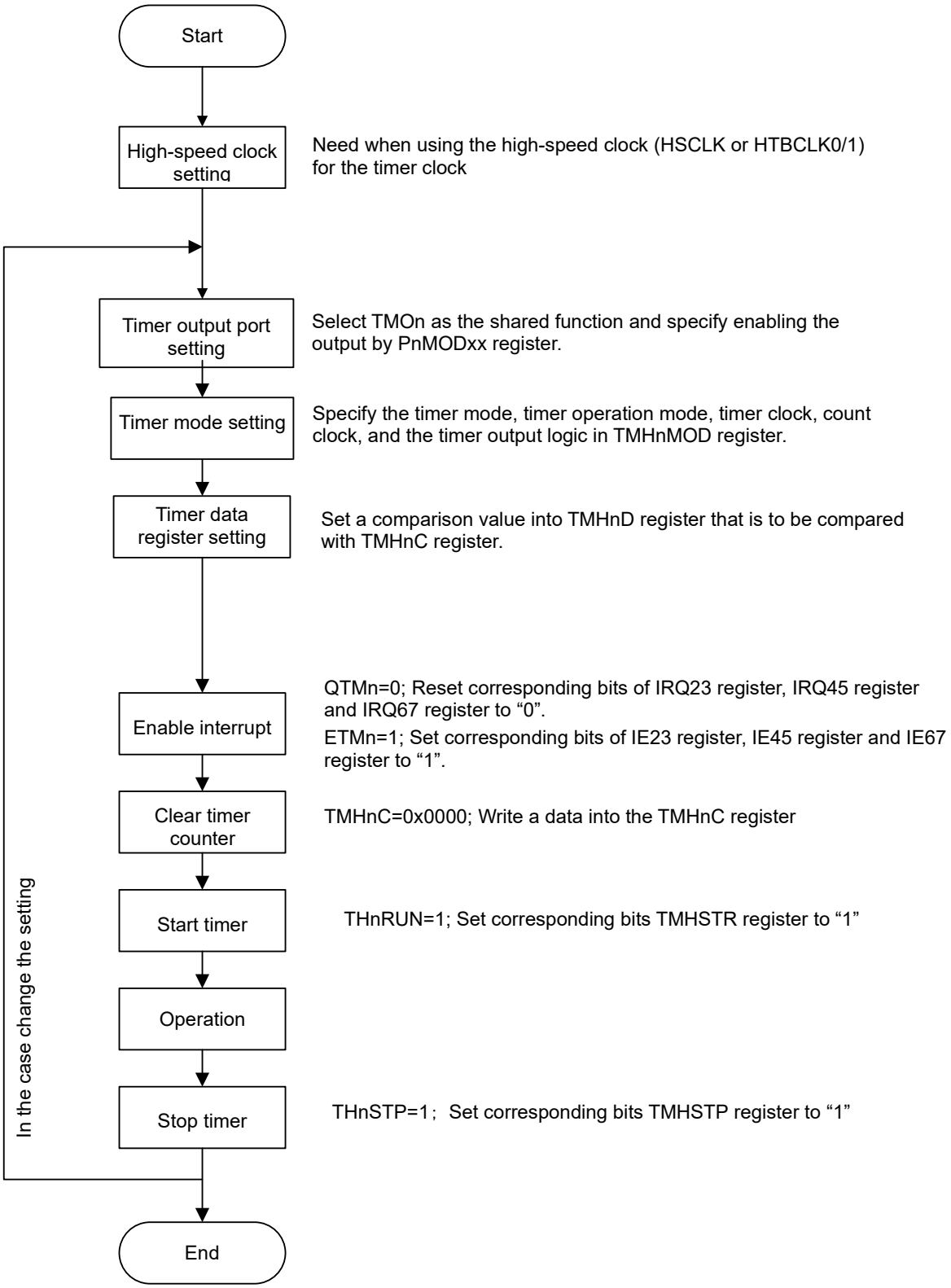


Figure 8-7 Setting Example

8.3.4 Using 16-bit Timer X for Crystal Oscillation Stability

It is necessary to use Timer X when using a crystal oscillation/external clock input for the low-speed clock. It can be used as a normal timer when the oscillation stabilization waiting is completed.

16-bit Timer X operates as counter of crystal oscillation stability time with THXCK2-0=4.
In the mode, an interrupt timing is at LOSCS becomes "0".
In other mode, the timing is at coinciding TMHXD value and TMHXC value.
See Chapter 6 "Clock Generation Circuit" for how to use.

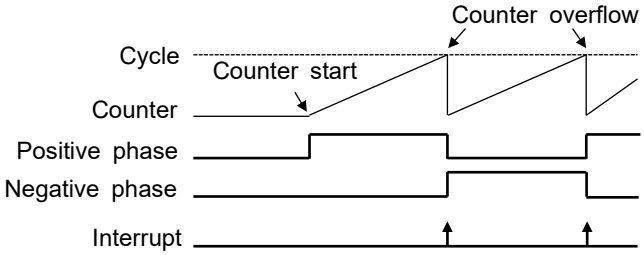
Chapter 9 Functional Timer (FTM)

9. Functional Timer

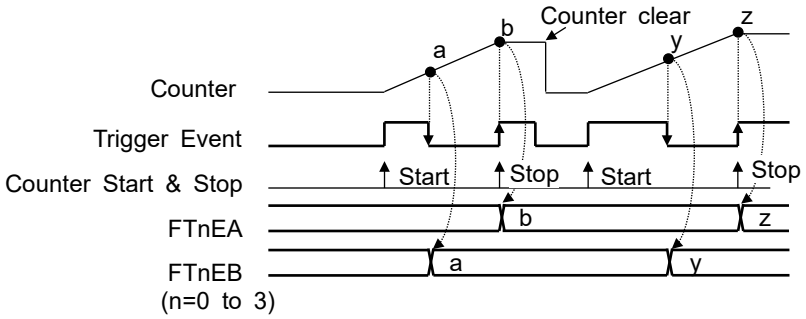
9.1 General Description

The Functional timer enables following functions in four operation modes (TIMER/CAPTURE/PWM1/PWM2).

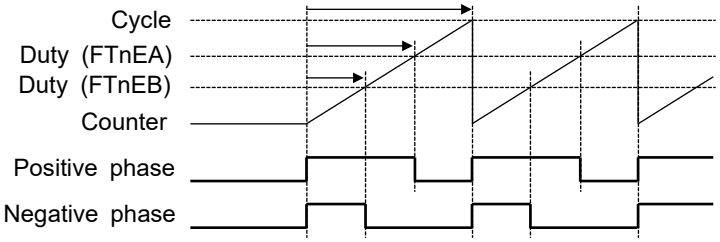
TIMER mode:
In this mode, the Functional Timer generates pulse signals, levels of which are reversed in sync with the counter start and the counter overflow. Also, it generates the interrupt when the counter overflows.



CAPTURE mode:
In this mode, the Functional Timer stores the value of counter into FTnEA register at the rising edge of a trigger event, into FTnEB register at the falling edge of a trigger event.



PWM1 mode:
In this mode, the Functional Timer generates two types of PWM waveform that have the same cycle and the start timing. The setting value of FTnEA register makes the duty of the positive phase output and the setting value of FTnEB register makes the duty of the negative phase output.



PWM2 mode:
In this mode, the Functional Timer generates the complimentary PWM waveform of which the positive phase output and the negative phase output works exclusively. The setting of FTnEA register makes the duty of the positive phase output. Also, a dead time can be configured by setting FTnDT register.

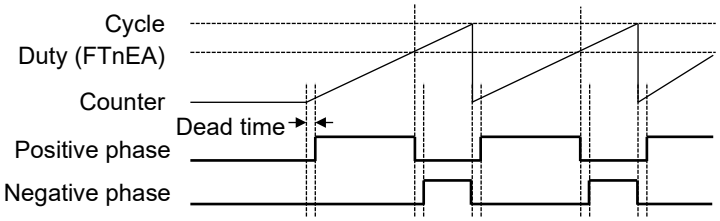


Table 9-1 shows the number of channels.

Table 9-1 Number of Functional Timer channels

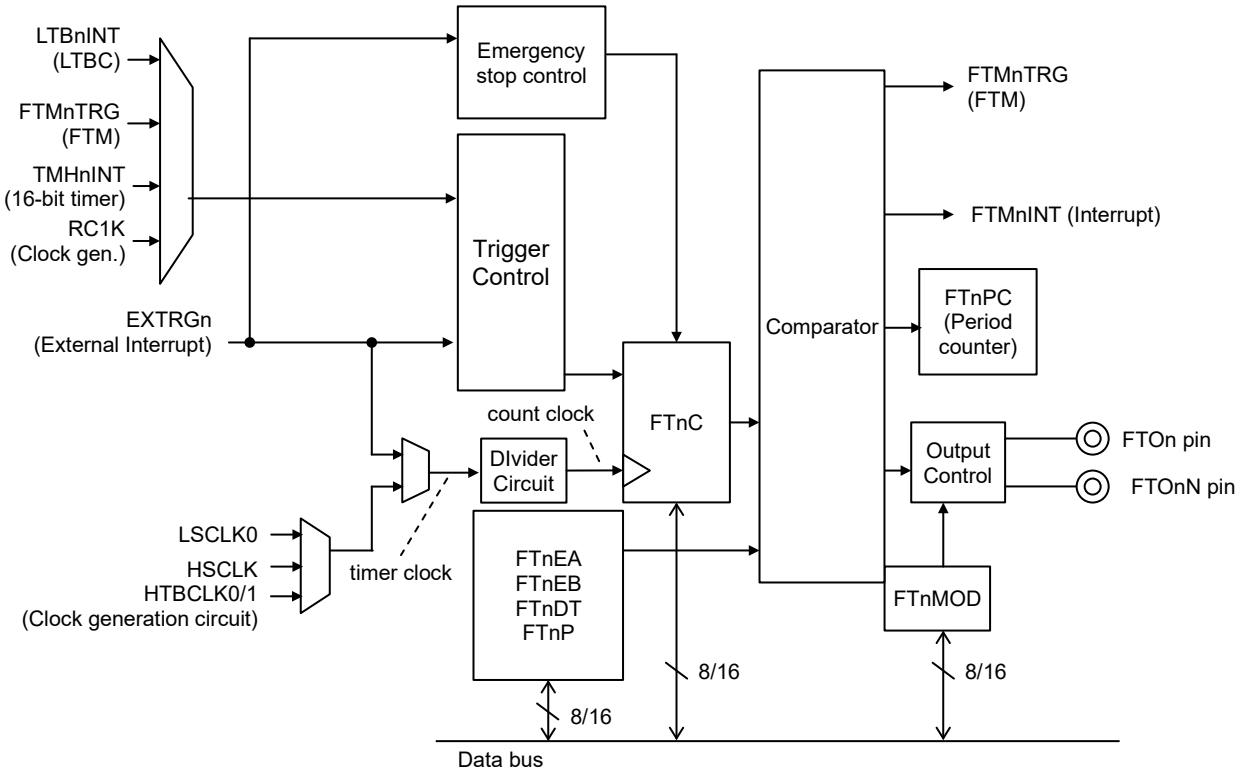
Product Name	Channel No.(n)
ML62Q2747	0 to 7
ML62Q2746	
ML62Q2745	
ML62Q2737	
ML62Q2736	
ML62Q2735	
ML62Q2727	
ML62Q2726	
ML62Q2725	
ML62Q2723	0 to 5
ML62Q2722	
ML62Q2713	
ML62Q2712	
ML62Q2703	
ML62Q2702	

9.1.1 Features

- Timer/Capture/PWM functions using the 16-bit counter
- Selectable counter clock from various sources (divided by 1 to 128 of LSCLK0, HSCLK, HTBCLK0/1, and external clock
- Logical switching (Positive logic or Negative logic) of timer output is available
- Generate a cyclic interrupt, a duty interrupt and a coincident interrupt with the setting value
- One-shot mode
- Start/stop/clear the timer by an external trigger input or a timer interrupt request (event triggers)
- Emergency stop and emergency stop interrupt by an external trigger input
- Two types of PWM output with the same cycle and different duties, and complementary PWM output with the dead time
- Input signal duty/cycle measurement by the capture function
- Interrupt source to be notified can be set

9.1.2 Configuration

Figure 9-1 shows the configuration of the FTM circuit.



FTnEA : FTMn event A register
FTnEB : FTMn event B register
FTnDT : FTMn dead time register
FTnP : FTMn cycle register
FTnC : FTMn counter register
FTnMOD : FTMn mode register
FTMnTRG : Functional Timer n trigger
(n=0 to 7)
EXTRGn : External trigger n / external clock n (n=0 to 7)
LTBnINT : Low speed time base counter interrupt n (n=1 to 3)
TMHnINT : 16-bit Timer n interrupt (n=0 to 6, X)

Figure 9-1 Configuration of the Functional Timer

9.1.3 List of Pins

The I/O pins of the Functional timer are assigned to the shared function of the general ports.

Pin name	I/O	Description
EXIn	I	External trigger/clock (used as EXTRGn). The max input frequency is 3MHz.
FTOn	O	Functional timer channel n output P
FTOnN	O	Functional timer channel n output N

n=0 to 7

Table 9-2 shows the list of the general ports used for the Functional timer and the register settings of the ports.

Table 9-2 Ports used in the Functional timer and the register settings

Pin name	Shared port		Register	Setting value	ML62Q2723, ML62Q2722 ML62Q2713, ML62Q2712 ML62Q2703, ML62Q2702			ML62Q2747, ML62Q2746 ML62Q2745, ML62Q2737 ML62Q2736, ML62Q2735 ML62Q2727, ML62Q2726 ML62Q2725		
					48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
EXI0	Ports assigned for external interrupt. See Chapter 18 External interrupt.				●	●	●	●	●	●
EXI1					●	●	●	●	●	●
EXI2					●	●	●	●	●	●
EXI3					●	●	●	●	●	●
EXI4					●	●	●	●	●	●
EXI5					●	●	●	●	●	●
EXI6					●	●	●	●	●	●
EXI7					●	●	●	●	●	●
FTO0	P02	5th Func.	P0MOD2	0100_XXXX*1	●	●	●	●	●	●
FTO0N	P03	5th Func.	P0MOD3	0100_XXXX*1	●	●	●	●	●	●
FTO1	P17	5th Func.	P1MOD7	0100_XXXX*1	●	●	●	●	●	●
	P47	5th Func.	P4MOD7	0100_XXXX*1	-	●	●	●	●	●
FTO1N	P20	5th Func.	P2MOD0	0100_XXXX*1	●	●	●	●	●	●
	P46	5th Func.	P4MOD6	0100_XXXX*1	-	-	●	●	●	●
FTO2	P21	5th Func.	P2MOD1	0100_XXXX*1	●	●	●	●	●	●
FTO2N	P22	5th Func.	P2MOD2	0100_XXXX*1	●	●	●	●	●	●
FTO3	P26	5th Func.	P2MOD6	0100_XXXX*1	●	●	●	●	●	●
FTO3N	P27	5th Func.	P2MOD7	0100_XXXX*1	●	●	●	●	●	●
	P44	5th Func.	P4MOD4	0100_XXXX*1	-	-	●	●	●	●
FTO4	P63	5th Func.	P6MOD3	0100_XXXX*1	●	●	●	●	●	●
FTO4N	P62	5th Func.	P6MOD2	0100_XXXX*1	●	●	●	●	●	●
FTO5	P64	5th Func.	P6MOD4	0100_XXXX*1	●	●	●	●	●	●
FTO5N	P65	5th Func.	P6MOD5	0100_XXXX*1	●	●	●	●	●	●
FTO6	P66	5th Func.	P6MOD6	0100_XXXX*1	-	-	-	●	●	●
	P93	5th Func.	P9MOD3	0100_XXXX*1	-	-	-	-	●	●
FTO6N	P67	5th Func.	P6MOD7	0100_XXXX*1	-	-	-	●	●	●
	P94	5th Func.	P9MOD4	0100_XXXX*1	-	-	-	-	●	●
FTO7	P54	5th Func.	P5MOD4	0100_XXXX*1	-	-	-	●	●	●
	P86	5th Func.	P8MOD6	0100_XXXX*1	-	-	-	-	-	●
	PA3	5th Func.	PAMOD3	0100_XXXX*1	-	-	-	-	●	●
FTO7N	P55	5th Func.	P5MOD5	0100_XXXX*1	-	-	-	●	●	●
	P87	5th Func.	P8MOD7	0100_XXXX*1	-	-	-	-	-	●
	PA4	5th Func.	PAMOD4	0100_XXXX*1	-	-	-	-	●	●

*1 : "XXXX" determines the condition of the port output

XXXX	Condition of the port output
0010	CMOS output
1010	N-ch open drain output (without the pull-up)
1111	N-ch open drain output (with the pull-up)

9.2 Description of Registers

9.2.1 List of Registers

Registers for unequipped channels are not available to use. They return 0x0000 for reading.

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF380	FTM common update register	FTCUD	-	W	8	0x00
0xF381	Reserved register	-	-	-	-	-
0xF382	FTM common control register	FTCCONL	FTCCON	R/W	8/16	0x00
0xF383		FTCCONH		R/W	8	0x00
0xF384	FTM common start register	FTCSTRL	FTCSTR	W	8/16	0x00
0xF385		FTCSTRH		W	8	0x00
0xF386	FTM common stop register	FTCSTPL	FTCSTP	W	8/16	0x00
0xF387		FTCSTPH		W	8	0x00
0xF388	FTM common status register	FTCSTATL	FTCSTAT	R	8/16	0x00
0xF389		FTCSTATH		R	8	0x00
0xF38A to 0xF38F	Reserved registers	-	-	-	-	-
0xF400	FTM0 cycle register	FT0PL	FT0P	R/W	8/16	0xFF
0xF401		FT0PH		R/W	8	0xFF
0xF402	FTM0 event A register	FT0EAL	FT0EA	R/W	8/16	0x00
0xF403		FT0EAH		R/W	8	0x00
0xF404	FTM0 event B register	FT0EBL	FT0EB	R/W	8/16	0x00
0xF405		FT0EBH		R/W	8	0x00
0xF406	FTM0 event B register	FT0DTL	FT0DT	R/W	8/16	0x00
0xF407		FT0DTH		R/W	8	0x00
0xF408	FTM0 counter register	FT0CL	FT0C	R/W	8/16	0x00
0xF409		FT0CH		R/W	8	0x00
0xF40A	FTM0 status register	FT0STAT	-	R	8	0x30
0xF40B	Reserved register	-	-	-	-	-
0xF40C	FTM0 mode register	FT0MODL	FT0MOD	R/W	8/16	0x00
0xF40D		FT0MODH		R/W	8	0x40
0xF40E	FTM0 clock register	FT0CLKL	FT0CLK	R/W	8/16	0x00
0xF40F		FT0CLKH		R/W	8	0x00
0xF410	FTM0 trigger register 0	FT0TRG0L	FT0TRG0	R/W	8/16	0x00
0xF411		FT0TRG0H		R/W	8	0x00
0xF412	FTM0 trigger register 1	FT0TRG1L	FT0TRG1	R/W	8/16	0x00
0xF413		FT0TRG1H		R/W	8	0x00
0xF414	FTM0 interrupt enable register	FT0INTEL	FT0INTE	R/W	8/16	0x00
0xF415		FT0INTEH		R/W	8	0x00
0xF416	FTM0 interrupt status register	FT0INTSL	FT0INTS	R	8/16	0x00
0xF417		FT0INTSH		R	8	0x00
0xF418	FTM0 interrupt clear register（L/H）	FT0INTCL	-	W	8	0x00
0xF419		FT0INTCH		W	8	0x00
0xF41A to 0xF41F	Reserved registers	-	-	-	-	-
0xF420	FTM1 cycle register	FT1PL	FT1P	R/W	8/16	0xFF
0xF421		FT1PH		R/W	8	0xFF
0xF422	FTM1 event A register	FT1EAL	FT1EA	R/W	8/16	0x00
0xF423		FT1EAH		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF424	FTM1 event B register	FT1EBL	FT1EB	R/W	8/16	0x00
0xF425		FT1EBH		R/W	8	0x00
0xF426	FTM1 dead time register	FT1DTL	FT1DT	R/W	8/16	0x00
0xF427		FT1DTH		R/W	8	0x00
0xF428	FTM1 counter register	FT1CL	FT1C	R/W	8/16	0x00
0xF429		FT1CH		R/W	8	0x00
0xF42A	FTM1 status register	FT1STAT	-	R	8	0x30
0xF42B	Reserved register	-	-	-	-	-
0xF42C	FTM1 mode register	FT1MODL	FT1MOD	R/W	8/16	0x00
0xF42D		FT1MODH		R/W	8	0x40
0xF42E	FTM1 clock register	FT1CLKL	FT1CLK	R/W	8/16	0x00
0xF42F		FT1CLKH		R/W	8	0x00
0xF430	FTM1 trigger register 0	FT1TRG0L	FT1TRG0	R/W	8/16	0x00
0xF431		FT1TRG0H		R/W	8	0x00
0xF432	FTM1 trigger register 1	FT1TRG1L	FT1TRG1	R/W	8/16	0x00
0xF433		FT1TRG1H		R/W	8	0x00
0xF434	FTM1 interrupt enable register	FT1INTEL	FT1INTE	R/W	8/16	0x00
0xF435		FT1INTEH		R/W	8	0x00
0xF436	FTM1 interrupt status register	FT1INTSL	FT1INTS	R	8/16	0x00
0xF437		FT1INTSH		R	8	0x00
0xF438	FTM1 interrupt clear register	FT1INTCL	-	W	8	0x00
0xF439		FT1INTCH		W	8	0x00
0xF43A to 0xF43F	Reserved registers	-	-	-	-	-
0xF440	FTM2 cycle register	FT2PL	FT2P	R/W	8/16	0xFF
0xF441		FT2PH		R/W	8	0xFF
0xF442	FTM2 event A register	FT2EAL	FT2EA	R/W	8/16	0x00
0xF443		FT2EAH		R/W	8	0x00
0xF444	FTM2 event B register	FT2EBL	FT2EB	R/W	8/16	0x00
0xF445		FT2EBH		R/W	8	0x00
0xF446	FTM2 dead time register	FT2DTL	FT2DT	R/W	8/16	0x00
0xF447		FT2DTH		R/W	8	0x00
0xF448	FTM2 counter register	FT2CL	FT2C	R/W	8/16	0x00
0xF449		FT2CH		R/W	8	0x00
0xF44A	FTM2 status register	FT2STAT	-	R	8	0x30
0xF44B	Reserved register	-	-	-	-	-
0xF44C	FTM2 mode register	FT2MODL	FT2MOD	R/W	8/16	0x00
0xF44D		FT2MODH		R/W	8	0x40
0xF44E	FTM2 clock register	FT2CLKL	FT2CLK	R/W	8/16	0x00
0xF44F		FT2CLKH		R/W	8	0x00
0xF450	FTM2 trigger register 0	FT2TRG0L	FT2TRG0	R/W	8/16	0x00
0xF451		FT2TRG0H		R/W	8	0x00
0xF452	FTM2 trigger register 1	FT2TRG1L	FT2TRG1	R/W	8/16	0x00
0xF453		FT2TRG1H		R/W	8	0x00
0xF454	FTM2 interrupt enable register	FT2INTEL	FT2INTE	R/W	8/16	0x00
0xF455		FT2INTEH		R/W	8	0x00
0xF456	FTM2 interrupt status register	FT2INTSL	FT2INTS	R	8/16	0x00
0xF457		FT2INTSH		R	8	0x00
0xF458	FTM2 interrupt clear register	FT2INTCL	-	W	8	0x00
0xF459		FT2INTCH		W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF45A to 0xF45F	Reserved registers	-	-	-	-	-
0xF460	FTM3 cycle register	FT3PL	FT3P	R/W	8/16	0xFF
0xF461		FT3PH		R/W	8	0xFF
0xF462	FTM3 event A register	FT3EAL	FT3EA	R/W	8/16	0x00
0xF463		FT3EAH		R/W	8	0x00
0xF464	FTM3 event B register	FT3EBL	FT3EB	R/W	8/16	0x00
0xF465		FT3EBH		R/W	8	0x00
0xF466	FTM3 dead time register	FT3DTL	FT3DT	R/W	8/16	0x00
0xF467		FT3DTH		R/W	8	0x00
0xF468	FTM3 counter register	FT3CL	FT3C	R/W	8/16	0x00
0xF469		FT3CH		R/W	8	0x00
0xF46A	FTM3 status register	FT3STAT	-	R	8	0x30
0xF46B	Reserved register	-	-	-	-	-
0xF46C	FTM3 mode register	FT3MODL	FT3MOD	R/W	8/16	0x00
0xF46D		FT3MODH		R/W	8	0x40
0xF46E	FTM3 clock register	FT3CLKL	FT3CLK	R/W	8/16	0x00
0xF46F		FT3CLKH		R/W	8	0x00
0xF470	FTM3 trigger register 0	FT3TRG0L	FT3TRG0	R/W	8/16	0x00
0xF471		FT3TRG0H		R/W	8	0x00
0xF472	FTM3 trigger register 1	FT3TRG1L	FT3TRG1	R/W	8/16	0x00
0xF473		FT3TRG1H		R/W	8	0x00
0xF474	FTM3 interrupt enable register	FT3INTEL	FT3INTE	R/W	8/16	0x00
0xF475		FT3INTEH		R/W	8	0x00
0xF476	FTM3 interrupt status register	FT3INTSL	FT3INTS	R	8/16	0x00
0xF477		FT3INTSH		R	8	0x00
0xF478	FTM3 interrupt clear register	FT3INTCL	-	W	8	0x00
0xF479		FT3INTCH		W	8	0x00
0xF47A to 0xF47F	Reserved register	-	-	-	-	-
0xF480	FTM4 cycle register	FT4PL	FT4P	R/W	8/16	0xFF
0xF481		FT4PH		R/W	8	0xFF
0xF482	FTM4 event A register	FT4EAL	FT4EA	R/W	8/16	0x00
0xF483		FT4EAH		R/W	8	0x00
0xF484	FTM4 event B register	FT4EBL	FT4EB	R/W	8/16	0x00
0xF485		FT4EBH		R/W	8	0x00
0xF486	FTM4 dead time register	FT4DTL	FT4DT	R/W	8/16	0x00
0xF487		FT4DTH		R/W	8	0x00
0xF488	FTM4 counter register	FT4CL	FT4C	R/W	8/16	0x00
0xF489		FT4CH		R/W	8	0x00
0xF48A	FTM4 status register	FT4STAT	-	R	8	0x30
0xF48B	Reserved register	-	-	-	-	-
0xF48C	FTM4 mode register	FT4MODL	FT4MOD	R/W	8/16	0x00
0xF48D		FT4MODH		R/W	8	0x40
0xF48E	FTM4 clock register	FT4CLKL	FT4CLK	R/W	8/16	0x00
0xF48F		FT4CLKH		R/W	8	0x00
0xF490	FTM4 trigger register 0	FT4TRG0L	FT4TRG0	R/W	8/16	0x00
0xF491		FT4TRG0H		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF492	FTM4 trigger register 1	FT4TRG1L	FT4TRG1	R/W	8/16	0x00
0xF493		FT4TRG1H		R/W	8	0x00
0xF494	FTM4 interrupt enable register	FT4INTEL	FT4INTE	R/W	8/16	0x00
0xF495		FT4INTEH		R/W	8	0x00
0xF496	FTM4 interrupt status register	FT4INTSL	FT4INTS	R	8/16	0x00
0xF497		FT4INTSH		R	8	0x00
0xF498	FTM4 interrupt clear register	FT4INTCL	-	W	8	0x00
0xF499		FT4INTCH		W	8	0x00
0xF49A to 0xF49F	Reserved register	-	-	-	-	-
0xF4A0	FTM5 cycle register	FT5PL	FT5P	R/W	8/16	0xFF
0xF4A1		FT5PH		R/W	8	0xFF
0xF4A2	FTM5 event A register	FT5EAL	FT5EA	R/W	8/16	0x00
0xF4A3		FT5EAH		R/W	8	0x00
0xF4A4	FTM5 event B register	FT5EBL	FT5EB	R/W	8/16	0x00
0xF4A5		FT5EBH		R/W	8	0x00
0xF4A6	FTM5 dead time register	FT5DTL	FT5DT	R/W	8/16	0x00
0xF4A7		FT5DTH		R/W	8	0x00
0xF4A8	FTM5 counter register	FT5CL	FT5C	R/W	8/16	0x00
0xF4A9		FT5CH		R/W	8	0x00
0xF4AA	FTM5 status register	FT5STAT	-	R	8	0x30
0xF4AB	Reserved register	-	-	-	-	-
0xF4AC	FTM5 mode register	FT5MODL	FT5MOD	R/W	8/16	0x00
0xF4AD		FT5MODH		R/W	8	0x40
0xF4AE	FTM5 clock register	FT5CLKL	FT5CLK	R/W	8/16	0x00
0xF4AF		FT5CLKH		R/W	8	0x00
0xF4B0	FTM5 trigger register 0	FT5TRG0L	FT5TRG0	R/W	8/16	0x00
0xF4B1		FT5TRG0H		R/W	8	0x00
0xF4B2	FTM5 trigger register 1	FT5TRG1L	FT5TRG1	R/W	8/16	0x00
0xF4B3		FT5TRG1H		R/W	8	0x00
0xF4B4	FTM5 interrupt enable register	FT5INTEL	FT5INTE	R/W	8/16	0x00
0xF4B5		FT5INTEH		R/W	8	0x00
0xF4B6	FTM5 interrupt status register	FT5INTSL	FT5INTS	R	8/16	0x00
0xF4B7		FT5INTSH		R	8	0x00
0xF4B8	FTM5 interrupt clear register	FT5INTCL	-	W	8	0x00
0xF4B9		FT5INTCH		W	8	0x00
0xF4BA to 0xF4BF	Reserved register	-	-	-	-	-
0xF4C0	FTM6 cycle register	FT6PL	FT6P	R/W	8/16	0xFF
0xF4C1		FT6PH		R/W	8	0xFF
0xF4C2	FTM6 event A register	FT6EAL	FT6EA	R/W	8/16	0x00
0xF4C3		FT6EAH		R/W	8	0x00
0xF4C4	FTM6 event B register	FT6EBL	FT6EB	R/W	8/16	0x00
0xF4C5		FT6EBH		R/W	8	0x00
0xF4C6	FTM6 dead time register	FT6DTL	FT6DT	R/W	8/16	0x00
0xF4C7		FT6DTH		R/W	8	0x00
0xF4C8	FTM6 counter register	FT6CL	FT6C	R/W	8/16	0x00
0xF4C9		FT6CH		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF4CA	FTM6 status register	FT6STAT	-	R	8	0x30
0xF4CB	Reserved register	-	-	-	-	-
0xF4CC	FTM6 mode register	FT6MODL	FT6MOD	R/W	8/16	0x00
0xF4CD		FT6MODH		R/W	8	0x40
0xF4CE	FTM6 clock register	FT6CLKL	FT6CLK	R/W	8/16	0x00
0xF4CF		FT6CLKH		R/W	8	0x00
0xF4D0	FTM6 trigger register 0	FT6TRG0L	FT6TRG0	R/W	8/16	0x00
0xF4D1		FT6TRG0H		R/W	8	0x00
0xF4D2	FTM6 trigger register 1	FT6TRG1L	FT6TRG1	R/W	8/16	0x00
0xF4D3		FT6TRG1H		R/W	8	0x00
0xF4D4	FTM6 interrupt enable register	FT6INTEL	FT6INTE	R/W	8/16	0x00
0xF4D5		FT6INTEH		R/W	8	0x00
0xF4D6	FTM6 interrupt status register	FT6INTSL	FT6INTS	R	8/16	0x00
0xF4D7		FT6INTSH		R	8	0x00
0xF4D8	FTM6 interrupt clear register	FT6INTCL	-	W	8	0x00
0xF4D9		FT6INTCH		W	8	0x00
0xF4DA to 0xF4DF	Reserved register	-	-	-	-	-
0xF4E0	FTM7 cycle register	FT7PL	FT7P	R/W	8/16	0xFF
0xF4E1		FT7PH		R/W	8	0xFF
0xF4E2	FTM7 event A register	FT7EAL	FT7EA	R/W	8/16	0x00
0xF4E3		FT7EAH		R/W	8	0x00
0xF4E4	FTM7 event B register	FT7EBL	FT7EB	R/W	8/16	0x00
0xF4E5		FT7EBH		R/W	8	0x00
0xF4E6	FTM7 dead time register	FT7DTL	FT7DT	R/W	8/16	0x00
0xF4E7		FT7DTH		R/W	8	0x00
0xF4E8	FTM7 counter register	FT7CL	FT7C	R/W	8/16	0x00
0xF4E9		FT7CH		R/W	8	0x00
0xF4EA	FTM7 status register	FT7STAT	-	R	8	0x30
0xF4EB	Reserved register	-	-	-	-	-
0xF4EC	FTM7 mode register	FT7MODL	FT7MOD	R/W	8/16	0x00
0xF4ED		FT7MODH		R/W	8	0x40
0xF4EE	FTM7 clock register	FT7CLKL	FT7CLK	R/W	8/16	0x00
0xF4EF		FT7CLKH		R/W	8	0x00
0xF4F0	FTM7 trigger register 0	FT7TRG0L	FT7TRG0	R/W	8/16	0x00
0xF4F1		FT7TRG0H		R/W	8	0x00
0xF4F2	FTM7 trigger register 1	FT7TRG1L	FT7TRG1	R/W	8/16	0x00
0xF4F3		FT7TRG1H		R/W	8	0x00
0xF4F4	FTM7 interrupt enable register	FT7INTEL	FT7INTE	R/W	8/16	0x00
0xF4F5		FT7INTEH		R/W	8	0x00
0xF4F6	FTM7 interrupt status register	FT7INTSL	FT7INTS	R	8/16	0x00
0xF4F7		FT7INTSH		R	8	0x00
0xF4F8	FTM7 interrupt clear register	FT7INTCL	-	W	8	0x00
0xF4F9		FT7INTCH		W	8	0x00
0xF4FA to 0xF4FF	Reserved register	-	-	-	-	-

9.2.2 FTMn Cycle Register (FTnP :n=0 to 7)

FTnP is a SFR to set the cycle (clock count) of FTMn.
Set this register after setting the operation mode using FTnMD1 to 0 bits of FTnMOD register.

Address : 0xF400(FT0PL/FT0P), 0xF401(FT0PH), 0xF420(FT1PL/FT1P), 0xF421(FT1PH),
0xF440(FT2PL/FT2P), 0xF441(FT2PH), 0xF460(FT3PL/FT3P), 0xF461(FT3PH),
0xF480(FT4PL/FT4P), 0xF481(FT4PH), 0xF4A0(FT5PL/FT5P), 0xF4A1(FT5PH),
0xF4C0(FT6PL/FT6P), 0xF4C1(FT6PH), 0xF4E0(FT7PL/FT7P), 0xF4E1(FT7PH)

Access : R/W
Access size : 8/16 bit
Initial value : 0xFFFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnP															
Byte	FTnPH								FTnPL							
Bit	FTnP15	FTnP14	FTnP13	FTnP12	FTnP11	FTnP10	FTnP9	FTnP8	FTnP7	FTnP6	FTnP5	FTnP4	FTnP3	FTnP2	FTnP1	FTnP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit no.	Bit symbol name	Description
15 to 0	FTnP15 to FTnP0	0x0001 to 0xFFFF: Set one cycle as the setting value in FTnP register + 1 clocks.

[Note]
- **When 0x0000 is written in this register, 0x0001 is set and the read value is also 0x0001.**
- **Set FTnP so that the functional timer output frequency is 4MHz or less, when its output is used.**
  The count clock frequency [MHz] / (FTnP value + 1) ≤ 4 [MHz] , so that
  FTnP value ≥ (count clock frequency [MHz] / 4) – 1 .

9.2.3 FTMn Event A Register (FTnEA: n=0 to 7)

FTnEA is a SFR to set the event timing of FTMn or display the capture data.
Set this register after setting the operation mode using FTnMD1 to 0 bits of FTnMOD register.
In the CAPTURE mode, the FTnEA is a read-only register and it is invalid to write to this register.

Address : 0xF402(FT0EAL/FT0EA), 0xF403(FT0EAH), 0xF422(FT1EAL/FT1EA), 0xF423(FT1EAH), 0xF442(FT2EAL/FT2EA), 0xF443(FT2EAH), 0xF462(FT3EAL/FT3EA), 0xF463(FT3EAH), 0xF482(FT4EAL/FT4EA), 0xF483(FT4EAH), 0xF4A2(FT5EAL/FT5EA), 0xF4A3(FT5EAH), 0xF4C2(FT6EAL/FT6EA), 0xF4C3(FT6EAH), 0xF4E2(FT7EAL/FT7EA), 0xF4E3(FT7EAH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnEA															
Byte	FTnEAH								FTnEAL							
Bit	FTnEA 15	FTnEA 14	FTnEA 13	FTnEA 12	FTnEA 11	FTnEA 10	FTnEA 9	FTnEA 8	FTnEA 7	FTnEA 6	FTnEA 5	FTnEA 4	FTnEA 3	FTnEA 2	FTnEA 1	FTnEA 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 0	FTnEA15 to FTnEA0	-TIMER mode 0x0000 to 0xFFFF: Set a count value to generate an interrupt. The Interrupt timing is FTnEA setting value + 1. -CAPTURE mode 0x0000 to 0xFFFF: The captured count value is stored. When it is read, FTnFLGA bit of FTMn status register (FTnSTAT) and FTnISA bit of FTMn interrupt status register (FTnINTS) is cleared after one timer clock. However, the FTnFLGA bit is cleared only when FTnTGEN=1. For information on clearing FTnFLGA, see Section 9.3.4.2. Writing to the FTnEA register is invalid. -PWM1 mode 0x0000 to 0xFFFF: Sets the duty of the positive phase output signal. The duty is the FTnEA register value + 1. If set to 0xFFFF, the duty will be 0%. When set to the same value as the periodic register (FTnP), the duty is 100%. When FTnP is 0xFFFF, duty cannot be set to 100%. Setting a value lager than a period register other than 0xFFFF is prohibited. -PWM2 mode 0x0000 to 0xFFFF: Sets the duty of the positive and negative phase output signals. The duty is the FTnEA register value + 1. If set to 0xFFFF, the duty will be 0%. When set to the same value as the periodic register (FTnP), the duty is 100%. When FTnP is 0xFFFF, duty cannot be set to 100%. . Setting a value lager than a period register other than 0xFFFF is prohibited

[Note]
- **In timer mode, a data set in the FTnEA register must be less than that set in the FTnP register.**
- **In PWM1 mode PWM2 mode, a data set in the FTnEA register must be 0xFFFF or less than that set in the FTnP register.**

9.2.4 FTMn Event B Register (FTnEB: n=0 to 7)

FTnEB is a SFR to set the event timing of FTMn or display the capture data.
Set this register after setting the operation mode using FTnMD1 to 0 bits of FTnMOD register.
In the CAPTURE mode, the FTnEA is a read-only register and it is invalid to write to this register.

Address : 0xF404(FT0EBL/FT0EB), 0xF405(FT0EBH), 0xF424(FT1EBL/FT1EB), 0xF425(FT1EBH), 0xF444(FT2EBL/FT2EB), 0xF445(FT2EBH), 0xF454(FT3EBL/FT3EB), 0xF455(FT3EBH), 0xF484(FT4EBL/FT4EB), 0xF485(FT4EBH), 0xF4A4(FT5EBL/FT5EB), 0xF4A5(FT5EBH), 0xF4C4(FT6EBL/FT6EB), 0xF4C5(FT6EBH), 0xF4E4(FT7EBL/FT7EB), 0xF4E5(FT7EBH)

Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnEB															
Byte	FTnEBH								FTnEBL							
Bit	FTnEB 15	FTnEB 14	FTnEB 13	FTnEB 12	FTnEB 11	FTnEB 10	FTnEB 9	FTnEB 8	FTnEB 7	FTnEB 6	FTnEB 5	FTnEB 4	FTnEB 3	FTnEB 2	FTnEB 1	FTnEB 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 0	FTnEB15 to FTnEB0	-TIMER mode 0x0000 to 0xFFFF: Set a count value to generate an interrupt. The Interrupt timing is FTnEB setting value + 1. -CAPTURE mode 0x0000 to 0xFFFF: The captured count value is stored. When it is read, FTnFLGB bit of FTMn status register (FTnSTAT) and FTnISA bit of FTMn interrupt status register (FTnINTS) is cleared after one timer clock. However, the FTnFLGB bit is cleared only when FTnTGEN=1. For information on clearing FTnFLGB, see Section 9.3.4.2. Writing to the FTnEB register is invalid. -PWM1 mode 0x0000 to 0xFFFF: Set the duty of the positive phase output. The duty in the PWM cycle becomes [the value set in this register +1]. The duty 0% is configurable when FTnEB = 0xFFFF. The duty 100% is configurable when FTnP = FTnEB. Do not set value more than one of FTnP except 0xFFFF. The duty becomes 0% when FTnP = 0xFFFF. -PWM2 mode Set 0x0000 only.

[Note]
- **In timer mode, a data set in the FTnEB register must be less than that set in the FTnP register.**
- **In PWM1 mode, a data set in the FTnEB register must be 0xFFFF or less than that set in the FTnP register.**

9.2.5 FTMn Dead Time Register (FTnDT :n=0 to 7)

FTnDT is a SFR to set the dead time of output signal.
Set this register after setting the operation mode using FTnMD1 to 0 bits of FTnMOD register.

Address : 0xF406(FT0DTL/FT0DT), 0xF407(FT0DTH), 0xF426(FT1DTL/FT1DT), 0xF427(FT1DTH), 0xF446(FT2DTL/FT2DT), 0xF447(FT2DTH), 0xF466(FT3DTL/FT3DT), 0xF467(FT3DTH), 0xF486(FT4DTL/FT4DT), 0xF487(FT4DTH), 0xF4A6(FT5DTL/FT5DT), 0xF4A7(FT5DTH), 0xF4C6(FT6DTL/FT6DT), 0xF4C7(FT6DTH), 0xF4E6(FT7DTL/FT7DT), 0xF4E7(FT7DTH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnDT															
Byte	FTnDTH								FTnDTL							
Bit	FTnDT 15	FTnDT 14	FTnDT 13	FTnDT 12	FTnDT 11	FTnDT 10	FTnDT 9	FTnDT 8	FTnDT 7	FTnDT 6	FTnDT 5	FTnDT 4	FTnDT 3	FTnDT 2	FTnDT 1	FTnDT 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 0	FTnDT15 to FTnDT0	-TIMER, PWM1/2 mode 0x0000 to 0xFFFF: Set the dead time of the Positive Phase Output / Negative Phase Output (FTnDT register setting value +1 timing) Enabled when the FTnDTENP bit or FTnDTENN bit of the FTnMOD register is "1". -CAPTURE mode This is invalid.

[Note]
- **In the PWM2 mode, the data set in the FTnDT register must be less than that set in the FTnEA register.**
- **In the PWM2 mode, the sum of setting data in the FTnDT register and the FTnEA register must be less than that set in the FTnP register.**

9.2.6 FTMn Counter Register (FTnC :n=0 to 7)

FTnC is a SFR to display the counter value of FTMn. When writing to this register, the counter is cleared to "0x0000" in one clock of the count clock.

Address : 0xF408(FT0CL/FT0C), 0xF409(FT0CH), 0xF428(FT1CL/FT1C), 0xF429(FT1CH),
0xF448(FT2CL/FT2C), 0xF449(FT2CH), 0xF468(FT3CL/FT3C), 0xF469(FT3CH),
0xF488(FT4CL/FT4C), 0xF489(FT4CH), 0xF4A8(FT5CL/FT5C), 0xF4A9(FT5CH),
0xF4C8(FT6CL/FT6C), 0xF4C9(FT6CH), 0xF4E8(FT7CL/FT7C), 0xF4E9(FT7CH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnC															
Byte	FTnCH								FTnCL							
Bit	FTnC15	FTnC14	FTnC13	FTnC12	FTnC11	FTnC10	FTnC9	FTnC8	FTnC7	FTnC6	FTnC5	FTnC4	FTnC3	FTnC2	FTnC1	FTnC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

In case of the following table, Reading value is available. In other case, do reading this register twice and confirm those equivalence.

System clock	Timer clock
LSCLK0	LSCLK0
HSCLK	HSCLK, HTBCLK0, HTBCLK1

[Note]

- **Read FTnC register twice to verify the data to prevent reading uncertain data while counting-up according to need.Read the FTnC register twice to verify the valid data to prevent reading uncertain data while counting-up, if a source of timer clock is as different as one of system clock.**
  In case of SYSCLK frequency = 250kHz, the count clock frequency = 3MHz:
  If first read value is 0x0007, second read value is more than 0x0012. Valid bits are 11 bits of FTnC15-5. It depend on reading interval time.

9.2.7 FTMn Status Register (FTnSTAT :n=0 to 7)

FTnSTAT is a read-only SFR to indicate the state of FTMn.

Address : 0xF40A(FT0STAT), 0xF42A(FT1STAT),
0xF44A(FT2STAT), 0xF46A(FT3STAT),
0xF48A(FT4STAT), 0xF4AA(FT5STAT),
0xF4CA(FT6STAT), 0xF4EA(FT7STAT)
Access : R
Access size : 8 bit
Initial value : 0x30

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FTnSTAT							
Bit	-	-	-	-	-	-	-	-	FTnSTA	FTnFLGC	FTnFLGB	FTnFLGA	-	-	-	FTnUD
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bit no.	Bit symbol name	Description
7	FTnSTA	Indicate the operation state of FTMn. 0: The counter is stopped (Initial value) 1: The counter is running
6	FTnFLGC	Indicate whether the next event start is enable or disable while a counter chosen by FTnCST bit of FTnTRG0 register is begin stopped. This is cleared by reading FTnC register automatically. 0: Starting by event trigger is enabled. (Initial value) 1: Starting by event trigger is disabled.
5	FTnFLGB	Indicate the state of event timing B. -TIMER/PWM1 mode 0: Counter value < value of FTMn event B register 1: Counter value ≥ value of FTMn event B register (Initial value) -CAPTURE mode 0: There is no captured data 1: There is captured data. To be cleared by reading the FTnEB register. To be cleared by reading the FTnEB register. However, FTnFLGB is cleared only when FTnTGEN=1. See section 9.3.4.2 as for clearing FTnFLGB. -PWM2 mode Fixed 0.
4	FTnFLGA	Indicate the state of event timing A. -TIMER/PWM1/PWM2 mode 0: Counter value < value of FTMn event A register 1: Counter value ≥ value of FTMn event A register (Initial value) -CAPTURE mode 0: There is no captured data 1: There is captured data. To be cleared by reading the FTnEA register. To be cleared by reading the FTnEA register. However, FTnFLGA is cleared only when FTnTGEN=1. See section 9.3.4.2 as for clearing FTnFLGA.
3 to 1	-	Reserved bits
0	FTnUD	Indicate the state of the completion after generating an update request of the FTnP or FTnEA/FTnEB/FTnDT register by writing "1" to FTCUDn bit of FTCUD register. When the transfer is completed, this bit is cleared automatically. 0: The update is completed (Initial value) 1: Requesting the update

9.2.8 FTMn Mode Register (FTnMOD :n=0 to 7)

FTnMOD is a SFR to set the FTOn and FTOnN pin output function and the operation mode.

Address : 0xF40C(FT0MODL/FT0MOD), 0xF40D(FT0MODH),
0xF42C(FT1MODL/FT1MOD), 0xF42D(FT1MODH),
0xF44C(FT2MODL/FT2MOD), 0xF44D(FT2MODH),
0xF46C(FT3MODL/FT3MOD), 0xF46D(FT3MODH),
0xF48C(FT4MODL/FT4MOD), 0xF48D(FT4MODH),
0xF4AC(FT5MODL/FT5MOD), 0xF4AD(FT5MODH),
0xF4CC(FT6MODL/FT6MOD), 0xF4CD(FT6MODH),
0xF4EC(FT7MODL/FT7MOD), 0xF4ED(FT7MODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x4000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnMOD															
Byte	FTnMODH								FTnMODL							
Bit	FTnOSL1	FTnOSL0	FTnOSNN	FTnOSNP	rsvd	rsvd	FTnSTSYN	FTnSTPO	FTnOST	-	FTnDTENN	FTnDTENP	-	-	FTnMD1	FTnMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	FTnOSL1	Select the phase of signal output at FTOnN pin. 0: Output Negative phase (Initial value) 1: Output Positive phase
14	FTnOSL0	Select the phase of signal output at FTOn pin. 0: Output Negative phase 1: Output Positive phase (Initial value)
13	FTnOSNN	Reverse the FTOnN pin output signal. It reverses the output signal chosen by FTnOSL1 bit (bit15). 0: Does not reverse the output. (Initial value) 1: Reverses the output
12	FTnOSNP	Reverse the FTMnP pin output signal. It reverses the output signal chosen by FTnOSL0 bit (bit14). 0: Does not reverse the output. (Initial value) 1: Reverses the output
11, 10	rsvd	Reserved bits. Set "0" always
9	FTnSTSYN	Set stop timing. 0: Just when writing stop register or receiving a stop trigger. 1: When an end of cycle after writing stop register or receiving a stop trigger. This function is available for stopping from software or trigger. It is not active for the emergency stop trigger If a start event occurs between the time the stop event occurs and the end of the cycle when this bit is “1”, the count operation will continue without stopping at the end of the cycle.
8	FTnSTPO	Set the output state of negative phase signal and the positive phase signal while the FTMn is stopped. -TIMER/PWM1/PWM2 mode 0: The output holds level "L" while the FTMn is stopped. (Initial value) When restarting the FTMn without clearing the counter, the output level is held until the next cycle. 1: The output holds the current level while the FTMn is stopped. When restarting the FTMn without clearing the counter, the output depends on the counter value. The output level becomes "L" when the counter is cleared while FTMn is stopped. -CAPTURE mode This bit is invalid.

Bit no.	Bit symbol name	Description
7	FTnOST	Set the repeat/one-shot mode of FTMn. -TIMER/PWM1/PWM2 mode 0: Repeat mode (Initial value) 1: One-shot mode -CAPTURE mode 0: Auto mode Even if the capture is performed once, data of the FTnEA and FTnEB register are overwritten (updated) when the next capture is performed. When the counter goes round, it restarts from 0. 1: Single mode Once captured into the FTnEA or FTnEB register, the next capture is not performed until reading the data. When the counter goes round, it stops.
6	-	Reserved bit
5	FTnDTENN	Enable the dead time of negative phase output. -TIMER/PWM1/PWM2 mode 0: Dead time is disabled (Initial value) 1: Dead time is enabled -CAPTURE mode This bit is invalid
4	FTnDTENP	Enable the dead time of positive phase output. -TIMER/PWM1/PWM2 mode 0: Dead time is disabled (Initial value) 1: Dead time is enabled -CAPTURE mode This bit is invalid
3, 2	-	Reserved bits
1, 0	FTnMD1, FTnMD0	Select the mode of FTMn. 00: TIMER mode (Initial value) 01: CAPTURE mode 10: PWM1 mode 11: PWM2 mode

[Note]
- **Set the FTnMOD register when the FTMn is stopped.**
- **When switching modes after operating once, initialize this peripheral circuit by block reset.**

9.2.9 FTMn Clock Register (FTnCLK :n=0 to 7)

FTnCLK is a SFR to set the timer clock and count clock of the FTMn.

Address : 0xF40E(FT0CLKL/FT0CLK), 0xF40F(FT0CLKH), 0xF42E(FT1CLKL/FT1CLK), 0xF42F(FT1CLKH), 0xF44E(FT2CLKL/FT2CLK), 0xF44F(FT2CLKH), 0xF46E(FT3CLKL/FT3CLK), 0xF46F(FT3CLKH), 0xF48E(FT4CLKL/FT4CLK), 0xF48F(FT4CLKH), 0xF4AE(FT5CLKL/FT5CLK), 0xF4AF(FT5CLKH), 0xF4CE(FT6CLKL/FT6CLK), 0xF4CF(FT6CLKH), 0xF4EE(FT7CLKL/FT7CLK), 0xF4EF(FT7CLKH)

Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnCLK															
Byte	FTnCLKH								FTnCLKL							
Bit	-	-	-	-	-	-	-	-	-	FTnCKD2	FTnCKD1	FTnCKD0	FTnCK3	FTnCK2	FTnCK1	FTnCK0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 7	-	Reserved bits
6 to 4	FTnCKD2 to FTnCKD0	Configure count clock frequency; divided timer source clock. 000: No dividing (Initial value) 001: Divided the timer clock by 2 010: Divided the timer clock by 4 011: Divided the timer clock by 8 100: Divided the timer clock by 16 101: Divided the timer clock by 32 110: Divided the timer clock by 64 111: Divided the timer clock by 128
3 to 0	FTnCK3 to FTnCK0	Select timer clock source. 0000: LSCLK0 (Initial value) 0001: HSCLK 0010: HTBCLK0 0011: HTBCLK1 0100: Do not use (LSCLK1) 0101: Do not use (HSCLK) 0110: Do not use (HTBCLK0) 0111: Do not use (HTBCLK1) 1000: External clock 0 input (EXTRG0) 1001: External clock 1 input (EXTRG1) 1010: External clock 2 input (EXTRG2) 1011: External clock 3 input (EXTRG3) 1100: External clock 4 input (EXTRG4) 1101: External clock 5 input (EXTRG5) 1110: External clock 6 input (EXTRG6) 1111: External clock 7 input (EXTRG7)

9.2.10 FTMn Trigger Register 0 (FTnTRG0 :n=0 to 7)

FTnTRG0 is a SFR to set the trigger function of FTMn.

Address : 0xF410 (FT0TRG0L/FT0TRG0), 0xF411 (FT0TRG0H),
0xF430 (FT1TRG0L/FT1TRG0), 0xF431 (FT1TRG0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnTRG0															
Byte	FTnTRG0H								FTnTRG0L							
Bit	-	FTnEST1	FTnEST0	FTnSTSS	FTnSTS3	FTnSTS2	FTnSTS1	FTnSTS0	FTnDCLD	FTnDCLH	FTnCST	-	FTnSPC	FTnSP	FTnSTC	FTnST
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	-	Reserved bit
14, 13	FTnEST1, FTnEST0	Select the emergency stop trigger source of FTMn. They are enabled only when FTnEMGEN bit of FTCCON register is "1". 00: External trigger 0 input (EXTRG0) (initial value) 01: External trigger 4 input (EXTRG4) 10: Reserved 11: Reserved
12 to 8	FTnSTSS, FTnSTS3 to FTnSTS0	Select the source of the trigger event for FTMn. When selecting the source of the trigger event, select something other than the target of the interrupt (other than FTM0 in the FTM0 setting). -TIMER/CAPTURE/PWM1/PWM2 mode 00000: External trigger 0 input (EXTRG0) (Initial value) 00001: External trigger 1 input (EXTRG1) 00010: External trigger 2 input (EXTRG2) 00011: External trigger 3 input (EXTRG3) 00100: External trigger 4 input (EXTRG4) 00101: External trigger 5 input (EXTRG5) 00110: External trigger 6 input (EXTRG6) 00111: External trigger 7 input (EXTRG7) 010XX: Reserved 01100: RC1K 01101: Low speed time base counter interrupt 1 (LTB1INT) 01110: Low speed time base counter interrupt 2 (LTB2INT) 01111: Low speed time base counter interrupt 3 (LTB3INT) X : Either 0 or 1. -TIMER/PWM1/PWM2 mode 10000: 16-bit timer 0 interrupt (TMH0INT) 10001: 16-bit timer 1 interrupt (TMH1INT) 10010: 16-bit timer 2 interrupt (TMH2INT) 10011: 16-bit timer 3 interrupt (TMH3INT) 10100: 16-bit timer 4 interrupt (TMH4INT) 10101: 16-bit timer X interrupt (TMHXINT) 10110: Reserved 10111: Reserved 11000: Functional timer 0 trigger (FTM0TRG) 11001: Functional timer 1 trigger (FTM1TRG) 11010: Reserved 11011: Reserved 11100: Reserved 11101: Reserved 11110: Reserved 11111: Reserved

Bit no.	Bit symbol name	Description
7	FTnDCLD	Select the operation of the "L" output section due to dead time when FTnDCLH is set to "1". ・TIMER/PWM1/PWM2 mode 0: Enabled during dead time (Initial value) 1: Disabled during dead time
6	FTnDCLH	Disable the counter clear by a trigger event when positive phase output is “H” level. -TIMER/PWM1/PWM2 mode 0: The counter clear is enabled regardless the positive phase output (initial value) 1: The counter clear is disabled when the positive phase output is "H" level. -CAPTURE mode This bit is invalid
5	FTnCST	Select the operation mode for starting the count by a trigger event. 0: A trigger event always can start the counter when the counter stops except for emergency stop (Initial value) 1: A trigger event does not start the counter until reading FTnC register when the counter stops except for emergency stop
4	-	Reserved bit
3	FTnSPC	Select whether to enable clearing the counter when a trigger event for counter-stop occurs (only when the edge is chosen by the FTnTRM2-0 bits). The setting of this bit is valid regardless of the setting of the FTnSP bit. If an update request of FTnP, FTnEA, FTnEB and FTnDT by the FTCUDn bit of FTCUD register is generated when the trigger event occurs, the FTnP, FTnEA, FTnEB and FTnDT register gets updated at the same time as the counter clear. 0: Disabled (Initial value) 1: Enabled However, the counter is not cleared/updated regardless of this bit in the following cases. When the emergency stop occurs. When Setting FTnTRM2-0 bits to “000” or “011”. When Setting 16bit timer or functional timer as trigger event source.
2	FTnSP	Select whether to enable stopping the counter by a trigger event. 0: Disabled (Initial value) 1: Enabled
1	FTnSTC	Select whether to enable clearing the counter when a trigger event for counter-start occurs (only when the edge is chosen by the FTnTRM2-0 bits). The setting of this bit is valid regardless of the setting of the FTnST bit. If an update request of FTnP, FTnEA, FTnEB and FTnDT by the FTCUDn bit of FTCUD register is generated when the trigger event occurs, the FTnP, FTnEA, FTnEB and FTnDT register gets updated at the same time as the counter clear. 0: Disabled (Initial value) 1: Enabled However, the counter is not cleared regardless of this bit in the following cases. When the emergency stop occurs. When Setting FTnTRM2-0 bits to “000” or “011”. When Setting TMHnINT or FTMnTRG as trigger event source.
0	FTnST	Select whether to enable starting the counter by a trigger event. 0: Disabled (Initial value) 1: Enabled

[Note]

- **The input pulse width must have two timer clocks or longer if FTnSTSS=0.**
- **The counter forcibly stops and does not run when the emergency stop trigger source is the same as the trigger event source with the FTnETG = 1 and FTnEMGEN = 1.**

9.2.11 FTMn Trigger Register 1 (FTnTRG1 :n=0 to 7)

FTnTRG1 is a SFR to set the trigger function of FTMn.

Address : 0xF412(FT0TRG1L/FT0TRG1), 0xF413(FT0TRG1H),
0xF432(FT1TRG1L/FT1TRG1), 0xF433(FT1TRG1H),
0xF452(FT2TRG1L/FT2TRG1), 0xF453(FT2TRG1H),
0xF472(FT3TRG1L/FT3TRG1), 0xF473(FT3TRG1H),
0xF492(FT4TRG1L/FT4TRG1), 0xF493(FT4TRG1H),
0xF4B2(FT5TRG1L/FT5TRG1), 0xF4B3(FT5TRG1H),
0xF4D2(FT6TRG1L/FT6TRG1), 0xF4D3(FT6TRG1H),
0xF4F2(FT7TRG1L/FT7TRG1), 0xF4F3(FT7TRG1H)

Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnTRG1															
Byte	FTnTRG1H								FTnTRG1L							
Bit	-	-	-	-	-	-	-	-	-	-	-	FTnEMGES	-	FTnTRM2	FTnTRM1	FTnTRM0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 5	-	Reserved bits
4	FTnEMGES	Select the edge of the emergency stop trigger of FTMn. 0: Rising edge (initial value) 1: Falling edge
3	-	Reserved bit
2 to 0	FTnTRM2 to FTnTRM0	Select the edge or the level of the trigger event of FTMn. These are enabled only when FTnSTSS bit is 0. In other cases, it is fixed to the rising edge. Counter start / Counter stop 000: Rising edge / Rising edge (Initial value) 001: Falling edge / Rising edge 010: Rising edge / Falling edge 011: Falling edge / Falling edge 1X0: "H" level / "L" level 1X1: "L" level / "H" level X: either "0" or "1".

[Note]

- **If a level setting is selected for the condition of the counter start and condition is matched, the count operation continues (restart the count-up from 0) even if a stop condition is satisfied in the one-shot mode.**
- **The trigger may occur immediately after setting the FTnTRG1 register in the trigger event enabled.**

9.2.12 FTMn Interrupt Enable Register (FTnINTE :n=0 to 7)

FTnINTE is a SFR to control the interrupt and trigger output of FTMn.
When each bit of FTnINTEL is set to "1", the interrupt is enabled and notified to the interrupt controller.
When each bit of FTnINTEH is set to "1", trigger output is enabled and notified to other channels of FTMn.

Address : 0xF414(FT0INTEL/FT0INTE), 0xF415(FT0INTEH),
0xF434(FT1INTEL/FT1INTE), 0xF435(FT1INTEH),
0xF454(FT2INTEL/FT2INTE), 0xF455(FT2INTEH),
0xF474(FT3INTEL/FT3INTE), 0xF475(FT3INTEH),
0xF494(FT4INTEL/FT4INTE), 0xF495(FT4INTEH),
0xF4B4(FT5INTEL/FT5INTE), 0xF4B5(FT5INTEH),
0xF4D4(FT6INTEL/FT6INTE), 0xF4D5(FT6INTEH),
0xF4F4(FT7INTEL/FT7INTE), 0xF4F5(FT7INTEH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnINTE															
Byte	FTnINTEH								FTnINTEL							
Bit	-	-	-	-	-	FTnIOB	FTnIOA	FTnIOP	-	-	-	FTnIETR	FTnIETS	FTnIEB	FTnIEA	FTnIEP
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is used to set enable/disable a target function.
0: Disabled (Initial value)
1: Enabled

Bit no.	Bit symbol name	Description (Target function)
15 to 11	-	Reserved bits
10	FTnIOB	Enable FTMnTRG output in event timing B of FTMn. When it's enabled, the FTMnTRG is output when the data of FTnC register and FTnEB register matched or a data is captured into the FTnEB register.
9	FTnIOA	Enable FTMnTRG output in event timing A of FTMn. When it's enabled, the FTMnTRG is output when the data of FTnC register and FTnEA register matched or a data is captured into the FTnEA register.
8	FTnIOP	Enable FTMnTRG output related to the FTnP register. When it's enabled, the FTMnTRG is output when the data of FTnC register and FTnP register matched.
7 to 5	-	Reserved bits
4	FTnIETR	Trigger counter start interrupt of FTMn
3	FTnIETS	Trigger counter stop interrupt of FTMn
2	FTnIEB	-TIMER/PWM1/CAPTURE mode The event timing B interrupt -PWM2 mode Write always "0"
1	FTnIEA	Event timing A interrupt of FTMn
0	FTnIEP	Cyclic interrupt of FTMn

9.2.13 FTMn Interrupt Status Register (FTnINTS :n=0 to 7)

FTnINTS is a read-only SFR to indicate the interrupt status of FTMn.
The bit 5 to bit 0 is reset to "0" by writing "1" to the same number of bit in the FTnINTC register.

Address : 0xF416(FT0INTSL/FT0INTS), 0xF417(FT0INTSH),
0xF436(FT1INTSL/FT1INTS), 0xF437(FT1INTSH),
0xF456(FT2INTSL/FT2INTS), 0xF457(FT2INTSH),
0xF476(FT3INTSL/FT3INTS), 0xF477(FT3INTSH),
0xF496(FT4INTSL/FT4INTS), 0xF497(FT4INTSH),
0xF4B6(FT5INTSL/FT5INTS), 0xF4B7(FT5INTSH),
0xF4D6(FT6INTSL/FT6INTS), 0xF4D7(FT6INTSH),
0xF4F6(FT7INTSL/FT7INTS), 0xF4F7(FT7INTSH)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTnINTS															
Byte	FTnINTSH								FTnINTSL							
Bit	-	-	-	-	-	-	-	-	-	-	FTnISES	FTnISTR	FTnISTS	FTnISB	FTnISA	FTnISP
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is used to indicate a target interrupt status.
0: Target interrupt has not occurred. (Initial value)
1: Target interrupt has occurred.

Bit no.	Bit symbol name	Description (Target interrupt)
15 to 6	-	Reserved bits
5	FTnISES	Emergency stop interrupt of FTMn This is cleared when writing 1 to FTnICES bit of FTnINTC register.
4	FTnISTR	Trigger counter start interrupt of FTMn It is set when counter-starting by trigger event or counter-clear by trigger event for counter-starting occur. This is cleared when writing 1 to FTnICTR bit of FTnINTC register.
3	FTnISTS	Trigger counter stop interrupt of FTMn It is set when counter-stopping by trigger event or counter-clear by trigger event for counter-stopping occur. This is cleared when writing 1 to FTnICTS bit of FTnINTC register.
2	FTnISB	Event timing B interrupt of FTMn This is cleared when writing “1” to FTnICB bit of FTnINTC register. It indicates that the captured data is stored to the FTnEB register in the CAPTURE mode. This is cleared when reading the FTnEB register in the CAPTURE mode.
1	FTnISA	Event timing A interrupt of FTMn This is cleared when writing “1” to FTnICA bit of FTnINTC register. It indicates that the captured data is stored to the FTnEA register in the CAPTURE mode. This is cleared when reading the FTnEA register in the CAPTURE mode.
0	FTnISP	Cyclic interrupt of FTMn This is cleared when writing "1" to FTnICP bit of FTnINTC register.

[Note]
- **If the FTnINTS register is not zero, a request to interrupt controller is not given when a new interrupt occurs. Clear the FTnINTS register with the FTnINTC register before that time.**

9.2.14 FTMn Interrupt Clear Register L/H (FTnINTCL, FTnINTCH : n=0 to 7)

FTnINTCL, FTnINTCH is a SFR to clear the interrupt status of FTMn. If the bit 5 to bit 0 is set to "1", the interrupt request indicated by the same number of bit in the FTnINTS register gets cleared. This register always returns 0x0000 for reading.

Address : 0xF418(FT0INTCL), 0xF419(FT0INTCH),
0xF438(FT1INTCL), 0xF439(FT1INTCH),
0xF458(FT2INTCL), 0xF459(FT2INTCH),
0xF478(FT3INTCL), 0xF479(FT3INTCH),
0xF498(FT4INTCL), 0xF499(FT4INTCH),
0xF4B8(FT5INTCL), 0xF4B9(FT5INTCH),
0xF4D8(FT6INTCL), 0xF4D9(FT6INTCH),
0xF4F8(FT7INTCL), 0xF4F9(FT7INTCH)
Access : W
Access size : 8 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	FTnINTCH								FTnINTCL							
Bit	FTnIR	-	-	-	-	-	-	-	-	-	FTnICES	FTnICTR	FTnICTS	FTnICB	FTnICA	FTnICP
R/W	W	R	R	R	R	R	R	R	R	R	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits (bit 5-0) :
It is used to clear target interrupt status flag.
Writing "0" : Invalid
Writing "1" : Clear a target interrupt status flag.

Bit no.	Bit symbol name	Description (Target interrupt)
15	FTnIR	An interrupt request bit of FTMn. Write "1" to this bit at the end of an interrupt routine. Writing "0":Invalid Writing "1":If there is any unhandled interrupt source, the interrupt request is generated again.
14 to 6	-	Reserved bits
5	FTnICES	Emergency stop interrupt of FTMn
4	FTnICTR	Trigger counter start interrupt of FTMn
3	FTnICTS	Trigger counter stop interrupt of FTMn
2	FTnICB	Event timing B interrupt of FTMn
1	FTnICA	Event timing A interrupt of FTMn
0	FTnICP	Cyclic interrupt of FTMn

9.2.15 FTM Common Update Register (FTCUD)

FTCUD is a SFR to update FTnP, FTnEA, FTnEB and FTnDT registers while they are running.
The FTCUD is a common SFR to each channel. The bit n corresponds to channel n.
It is unavailable to write to the bits for unequipped channels.

Address : 0xF380 (FTCUD)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FTCUD							
Bit	-	-	-	-	-	-	-	-	FTCUD7	FTCUD6	FTCUD5	FTCUD4	FTCUD3	FTCUD2	FTCUD1	FTCUD0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 8		Reserved bits
7 to 0	FTCUD7 to FTCUD0	Write-only bits to update FTnP, FTnEA, FTnEB and FTnDT registers while they are running. After setting the FTnP, FTnEA, FTnEB and FTnDT registers, the setting value is transferred to the internal buffers of FTnP, FTnEA, FTnEB and FTnDT at the end of the cycle by writing "1" to the corresponding bit for the FTMn. Writing "0": Invalid Writing "1": Update request occur

9.2.16 FTM Common Control Register (FTCCON)

FTCCON is a SFR to set the function of FTMn.
This is a common SFR to each channel. The bit n corresponds to channel n.
It is unavailable to write to the bits for unequipped channels.

Address : 0xF382 (FTCCONL/FTCCON), 0xF383 (FTCCONH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTCCON															
Byte	FTCCONH								FTCCONL							
Bit	FT7SDN	FT6SDN	FT5SDN	FT4SDN	FT3SDN	FT2SDN	FT1SDN	FT0SDN	FT7EMGEN	FT6EMGEN	FT5EMGEN	FT4EMGEN	FT3EMGEN	FT2EMGEN	FT1EMGEN	FT0EMGEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 8	FT7SDN to FT0SDN	Enable controlling the positive phase/negative phase output. -TIMER/PWM1/PWM2 mode 0: Enabled (Initial value) 1: Disabled (The output is fixed to "L" level) -CAPTURE mode This bit is invalid
7 to 0	FT7EMGEN to FT0EMGEN	Enable the emergency stop on the FTMn. 0: Disabled (Initial value) 1: Enabled

9.2.17 FTM Common Start Register (FTCSTR)

FTCSTR is a SFR to set the function of FTMn. This is an SFR common to each channel. The bit n corresponds to channel n.
It is unavailable to write to the bits for unequipped channels.

Address : 0xF384 (FTCSTRL/FTCSTR), 0xF385 (FTCSTRH)
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTCSTR															
Byte	FTCSTRH								FTCSTRL							
Bit	FT7ETG	FT6ETG	FT5ETG	FT4ETG	FT3ETG	FT2ETG	FT1ETG	FT0ETG	FT7STR	FT6STR	FT5STR	FT4STR	FT3STR	FT2STR	FT1STR	FT0STR
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 8	FT7ETG to FT0ETG	Enable trigger operation; counting stop/start by a trigger event. Control by the FTCSTP register to disable it. For clearing the counter by the trigger event, control it by FTnSTC bit and FTnSPC bit of FTnTRG0 register. Trigger operation is disabled in the initial state at the power-on. Writing "0": Invalid Writing "1": Trigger operation (stop/start count) is enabled
7 to 0	FT7STR to FT0STR	Start counting the FTMn by the software. When "1" is written in these bits, the count starts. In the initial state at the power-on, the counting is stopped. Writing "0": Invalid Writing "1": Start counting by software

9.2.18 FTM Common Stop Register (FTCSTP)

FTCSTP is a SFR to set the function of FTMn. This is a common SFR to each channel. The bit n corresponds to channel n.
It is unavailable to write to the bits for unequipped channels.

Address : 0xF386 (FTCSTPL/FTCSTP), 0xF387 (FTCSTPH)
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTCSTP															
Byte	FTCSTPH								FTCSTPL							
Bit	FT7DTG	FT6DTG	FT5DTG	FT4DTG	FT3DTG	FT2DTG	FT1DTG	FT0DTG	FT7STP	FT6STP	FT5STP	FT4STP	FT3STP	FT2STP	FT1STP	FT0STP
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 8	FT7DTG to FT0DTG	Disable trigger operation, counting stop/start by a trigger event. Control by the FTCSTR register to enable it. Trigger operation is enabled in the initial state at the power-on. Writing "0": Invalid Writing "1": Trigger operation is disabled. The counting is stopped when it is operated by a trigger event.
7 to 0	FT7STP to FT0STP	Stop counting the FTMn by the software. When "1" is written in these bits, the count stops. In the initial state at the power-on, the counting is stopped. Writing "0": Invalid Writing "1": Counting is stopped by the software

9.2.19 FTM Common Status Register (FTCSTAT)

FTCSTAT is a SFR to indicate the state of FTMn. This is a common SFR to each channel. The bit n corresponds to channel n.

Address : 0xF388 (FTCSTATL/FTCSTAT), 0xF389 (FTCSTATH)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FTCSTAT															
Byte	FTCSTATH								FTCSTATL							
Bit	FT7TGEN	FT6TGEN	FT5TGEN	FT4TGEN	FT3TGEN	FT2TGEN	FT1TGEN	FT0TGEN	FT7RUN	FT6RUN	FT5RUN	FT4RUN	FT3RUN	FT2RUN	FT1RUN	FT0RUN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 8	FT7TGEN to FT0TGEN	Ceck the setting status of FTMn. The trigger operation is disabled in the initial state at the power-on. 0: Trigger operation (counting stop/start) is disabled (initial value) 1: Trigger operation (counting stop/start) is enabled
7 to 0	FT7RUN to FT0RUN	Indicate the counting status of FTMn. This bit indicates the same information as FTnSTA bit. In the initial state at the power-on, counting is stopped. 0: Counting is stopped (initial value) 1: Counting is in progress

9.3 Description of Operation

Four types of operation modes are available for the functional timer:

- TIMER mode
- CAPTURE mode
- PWM1 mode
- PWM2 mode

9.3.1 Common Sequence (Initial setting for All Modes)

FTMn starts operating by setting the FTCSTR register after the setting steps from 1 to 6 below.
During operation, the hardware states such as interrupt status can be checked and the cycle/event settings are updateable.

1: Mode setting (FTnMOD register)
Choose the TIMER/CAPTURE/PWM1/PWM2 mode using the FTnMOD register.
In addition, set the repeat mode/one-shot mode.

2: Clock setting (FTnCLK register)
Choose the timer clock and the count clock; dividing ratio can also be set.

3: Trigger setting (FTnTRG0 register, FTnTRG1 register)
Use this setting when starting/stopping the counter by an event trigger.
In the FTnTRG0 register, choose the event trigger source and the action. In the FTnTRG1 register, choose the edge of the event trigger/emergency stop.

4: Interrupt setting (FTnINTE register)
Set the interrupt source.
Choose from cycle/event (counter coincidence, duty, capture) and trigger start/stop interrupt.

5: Cycle/event setting (FTnP register, FTnEA register, FTnEB register, FTnDT register)
Set the cycle, data for counter coincidence, duty, dead time, etc.

Table 9-3 the register settings

	TIMER mode	CAPTURE mode	PWM1 mode	PWM2 mode
FTnP register	Cycle in repeat mode or timeout period in one-shot mode			
FTnEA register	Coincident interrupt setting value	(Capturing data)	Positive phase output duty	Duty
FTnEB register	Coincident interrupt setting value		Negative phase output duty	(Unused)
FTnDT register	Dead time for output	(Unused)	Dead time for output	Dead time for output

The cycle is calculated as follows:

$$T_{period} = \frac{FTnP + 1}{\text{The count clock frequency [Hz]}} \quad \text{(FTnP: 0x0001 to 0xFFFF)}$$

6: Choice of the external output signal
FTnOSL1 and FTnOSL0 bits of FTnMOD register are used to choose output driven to the FTOn pin or FTOnN pin.
See “9.3.3 Output Control” for detail.

7: Control start/stop
Allow the software start, or event trigger reception, emergency stop setting.
The counter operates at the rising edge of the count clock.
Since the software start/stop is synchronized with the count clock, the FTnSTA bit becomes "1" at the start after four cycle of the timer clock and the counter operation starts.
When the operation is stopped, the count operation stops and the FTnSTA bit becomes "0". Then the count value is maintained.
If started again, it restarts after four cycle.
If clearing the counter, write an arbitrary value to the FTnC register.

8: Operation process in progress

The state under operation can be checked by the FTnSTAT, FTCSTAT, and FTnINTS registers.

To change the waveform of PWM, etc., set the applicable bit of the FTMUD register after setting the cycle/event. The waveform will be updated in the next cycle.

In addition, setting the FTnSDN bit of the FTCCON register forces the output to be fixed to "L" level.

9.3.2 Counter Operation (for All Modes)

The operation of FTM's internal counter is common to each mode.
It counts up to the setting value of the FTnP register.
In the repeat mode; the FTnOST bit of the FTnMOD register is "0", the counter is cleared at the time of overflow, then continues the counting operation again.
In the one-shot mode; the FTnOST bit of the FTnMOD register is "1", the counter is cleared at the time of overflow, and then stops the counting operation.
Starting/stopping/Clearing the counting operation can be executed through the software or a trigger event.

9.3.2.1 Starting/Stopping Counting by Software

When writing "1" to the FTnSTR bit of the FTCSTR register, the FTnSTA bit of the FTnSTAT register showing the count status becomes "1", and the counting operation is started.
In the one-shot mode; the FTnOST bit of the FTnMOD register is "1", the counting operation is stopped by overflow. The FTnSTA bit of the FTnSTAT register showing the count status automatically becomes "0".

When writing "1" to the FTnSTP bit of the FTCSTP register while the counter operation is in progress (the FTnSTA bit of the FTnSTAT register showing the count status is "1"), the counter stops its operation. If the FTnSTSYN bit is “1”, its counting stops at end of cycle.
To confirm the stop of the counter, check by the software that the FTnSTA bit of the FTnSTAT register is reset to "0". The counter value is maintained while the counter is not working.
After the counter is stopped, if "1" is written to the FTnSTR bit of the FTCSTR register again, it continues counting from the value at the time it stopped.
To clear the counter, execute writing to the FTnC register while it is stopped.
If subsequently restarting the counter, confirm that the FTnC register is reset to "0x0000", then write "1" to the FTnSTR bit of the FTCSTR register.

Update timing of the relevant registers:
If writing the registers when the timer stops and the counter is "0", they are updated at the timer start.
If writing the registers while the timer is running, they are updated in the next cycle of that the update is requested by FTCUDn bit of FTCUD register.
If writing the registers when the timer stops and the counter is not "0", the registers are not updated until the update is requested by FTCUDn bit. Update the registers by one of following two ways.

- Write the relevant registers after clearing the counter by setting the FTnCL register.
- Request updating the relevant registers by setting the FTCUDn bit of FTCUD register.

9.3.2.2 Starting/Stopping Counting by Trigger Event

Writing "1" to the FTnETG bit of the FTCSTR register enables the counter operation to be controlled by triggers.
Trigger choice, etc. can be executed through the configuration of FTnTRG0 and FTnTRG1 registers.
The source of a trigger event can be chosen from EXTRG0 to EXTRG7, LTB1INT to LTB3INT, TMH0INT to TMH4INT, TMHXINT or FTM0TRG to FTMnTRG.
Depending on the chosen trigger event, an operation (counter start, counter stop, counter start/stop and counter clearing) can be selected. If the FTnSTSYN bit is “1”, its counting stops at end of cycle.

9.3.2.3 Clearing Counter

A counter can be cleared by the software or trigger-event. A clearing by software is writing any data to FTnC.
A clearing by trigger-event is done when occurred start-trigger with FTnSTC=1 or stop-trigger with FTnSPC=1. See the bit-explanation for detail condition.
Set the clear invalid section by setting the FTnDCLH, FTnDCLD.

- FTnDCLH=1, FTnDCLD=x : no clear invalid section
- FTnDCLH=1, FTnDCLD=0 : clear invalid during positive phase outputs high-level. However it’s valid during the dead-time.
- FTnDCLH=1, FTnDCLD=1 : clear invalid during positive phase outputs high-level.

9.3.3 Output Control

Two types of signals can be output from FTOn/FTOnN pins.
FTnOSL1 and FTnOSL0 bits of FTnMOD register are used to choose the phase of the output signal driven to the FTOn/FTOnN pins. FTnOSNP bit is for reversing the output to the FTMnP pin. FTnOSNN bit is for reversing the output to the FTOnN pin.
If the dead time is enabled, the "L" level output is maintained from the start of counting through the dead time period. Also a setting FTnSDN bit forces the positive/negative phase output to be "L" level. See the explain of each mode for output during operation.

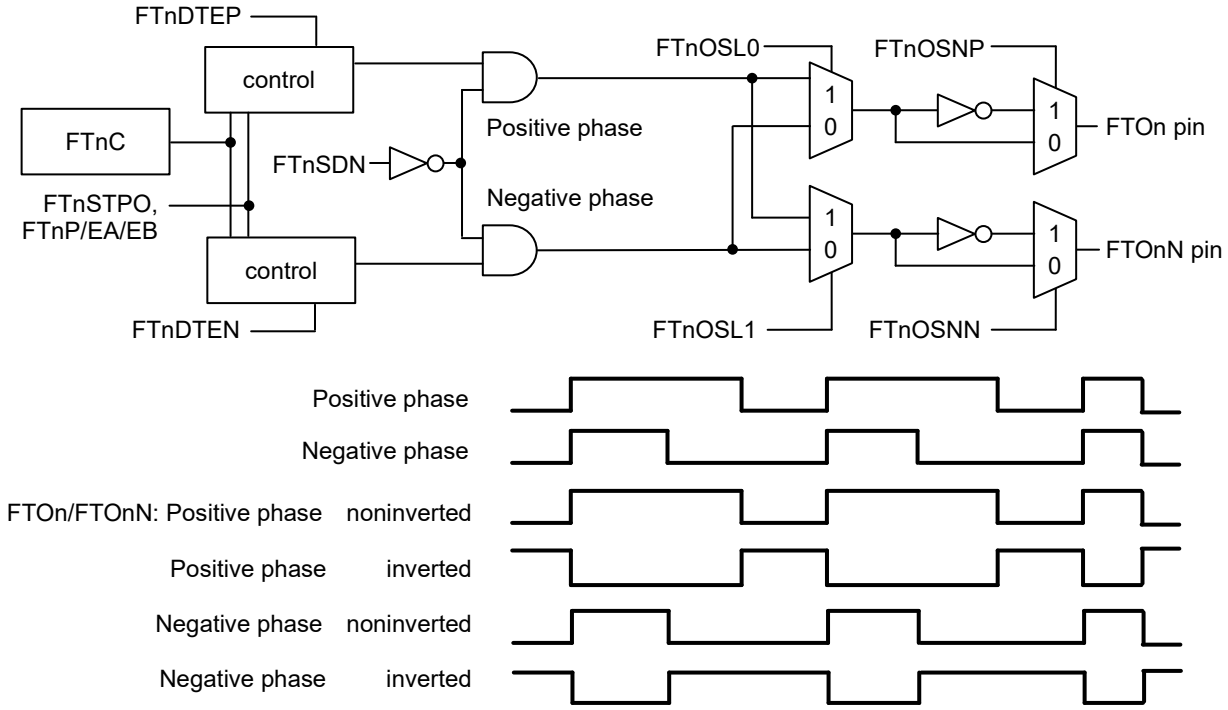
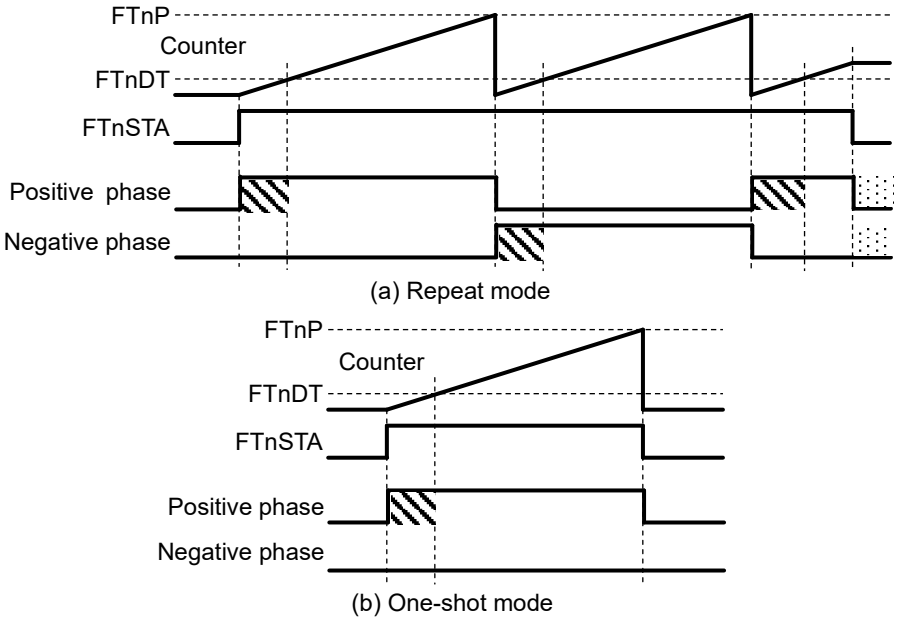


Figure 9-2 Output Control

9.3.3.1 TIMER Mode

The TIMER mode function generates interrupt of counter over-flow and controls output.
When writing "1" to the FTnSTR bit of the FTCSTR register with the counter set to "0x0000", the positive phase output starts with "H" level and the negative phase output starts with "L" level.
In the repeat mode, the output repeats to toggle the signal level synchronizing with the start of count and the overflow.
In the one-shot mode, the positive phase output remains "H" level for one cycle of the timer and then the count stops. The negative phase output is fixed to "L".
Figure 9-3 shows waveforms of the positive phase/negative phase output.



L-level while the dead-time is set by FTnDT if FTnDTENP/FTnDTENN=1.
L-level if FTnSTPO=0. the level according to the counter value if FTnSTPO=1.

Figure 9-3 Waveforms of the positive phase/negative phase output in the Timer mode

9.3.3.2 PWM1 Mode

The PWM1 mode generates pulse with the cycle configured by FTnP register. The duty of positive phase output is configured by FTnEA register. The duty of negative phase output is configured by FTnEB register.
In the repeat mode, the initial values for each of Positive phase/Negative phase outputs are "L" level, and they become "H" level at start. Each of them becomes "L" level depending on the duty value. They resume "H" level in the next cycle. This pattern repeats until the operation is stopped. In the one-shot mode, they automatically stop after one cycle becoming "L" level. In addition, if the dead time is enabled, the "L" level output is maintained from the start of counting through the dead time period.
Figure 9-4 shows waveforms of the positive phase/negative phase output in the repeat PMW1 mode.

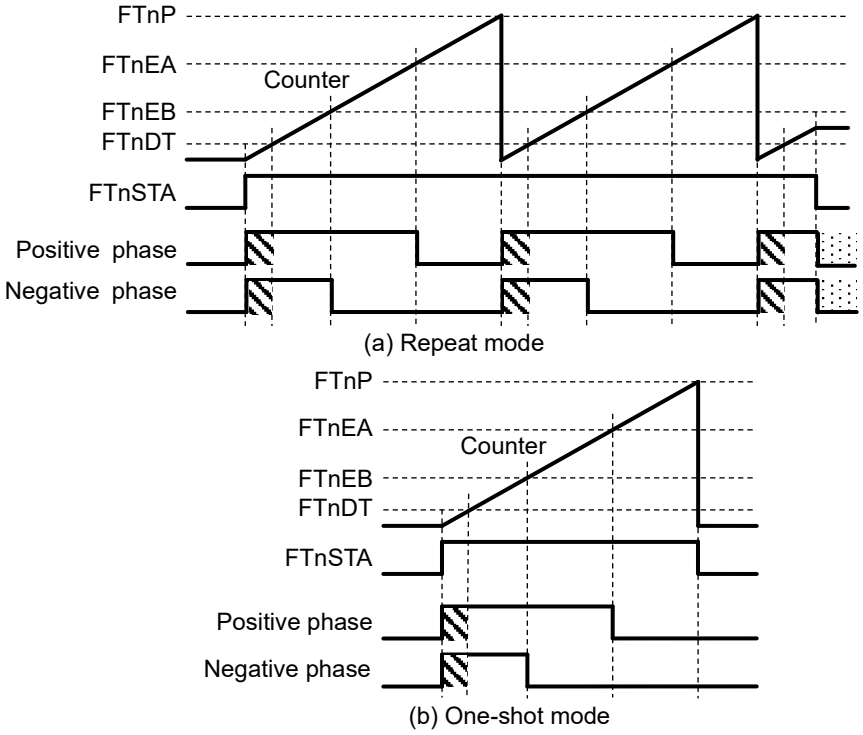


Figure 9-4 Waveforms of the positive phase/negative phase output in the PWM1 mode

9.3.3.3 PWM2 Mode

The PWM2 mode generates a complementary output pulse with the cycle configured by FTnP register. The duty of positive/negative phase output is configured by FTnEA register. The FTnEB register is not used.
In the repeat mode, "L" level is the initial value for each of Positive phase/Negative phase output, and the positive phase becomes "H" level at start. The positive phase output becomes "L" level and the negative phase output becomes "H" level depending on the duty value. In the next cycle, the positive phase output becomes "H" level and the negative phase output becomes "L" level again. This pattern repeats until the operation is stopped. In the one-shot mode, they automatically stop after one cycle becoming "L" level.
In addition, if the dead time is enabled, the "L" level output is maintained, from the start of counting for the positive phase output and from duty coincidence for the negative phase output, through the dead time period.

Figure 9-5 shows waveforms of the positive phase/negative phase output in the repeat PMW2 mode.

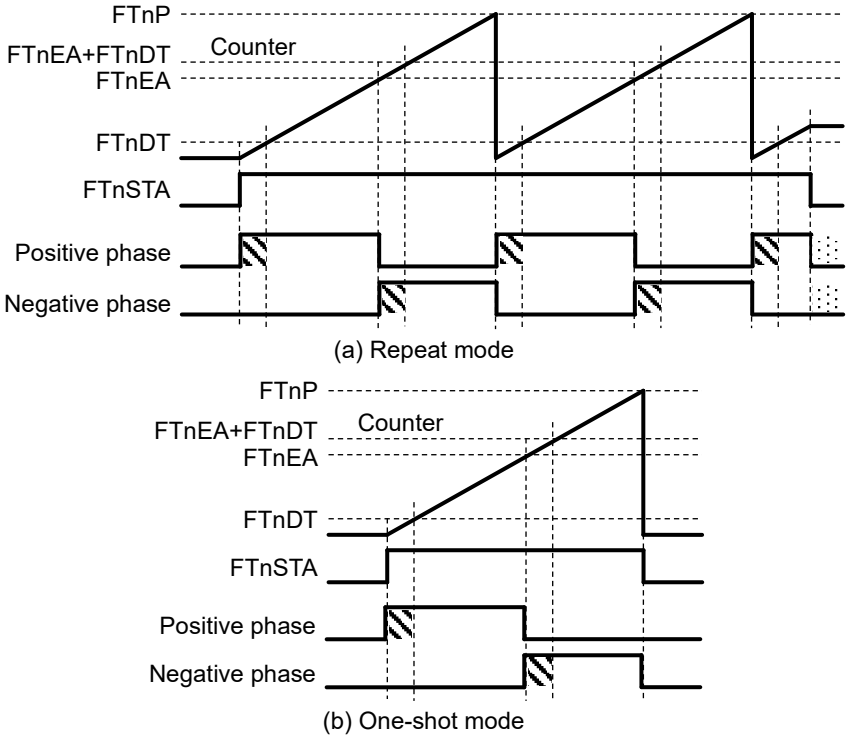


Figure 9-5 Waveforms of the positive phase/negative phase output in the PWM2 mode

9.3.3.4 Output at Counter Stop

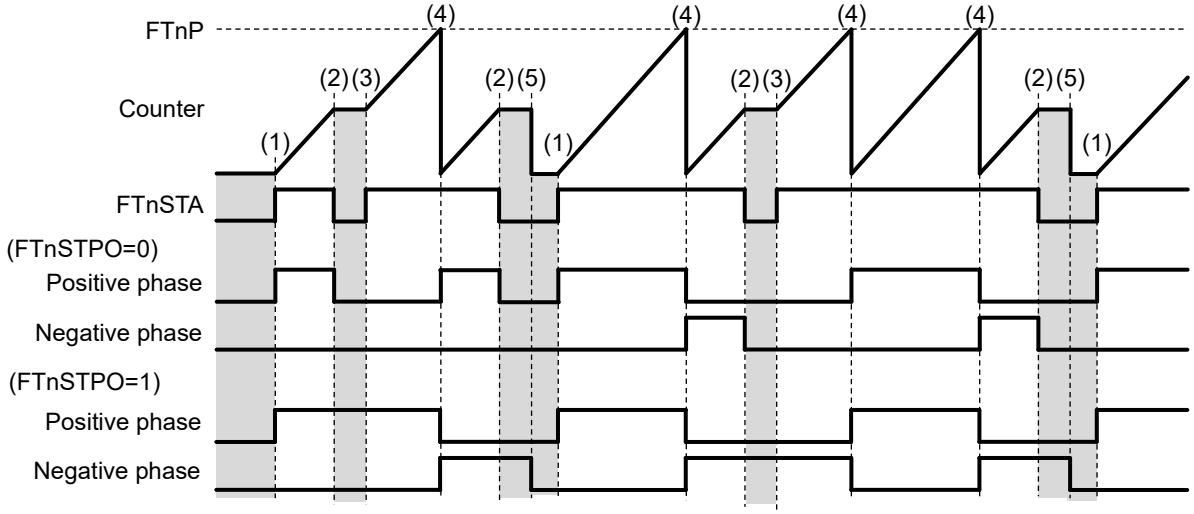
The state of Positive/Negative phase output when the counter is stopped by the software or the event trigger input is determined by the FTnSTPO bit setting of the FTnMOD register.

(1) If the FTnSTPO bit is "0":
The Positive/Negative phase outputs become "L" level as soon as the counter is stopped. If the counter is restarted in this state, the Positive/Negative phase output remains at "L" level during the present cycle and changes according to the count value from the next cycle.

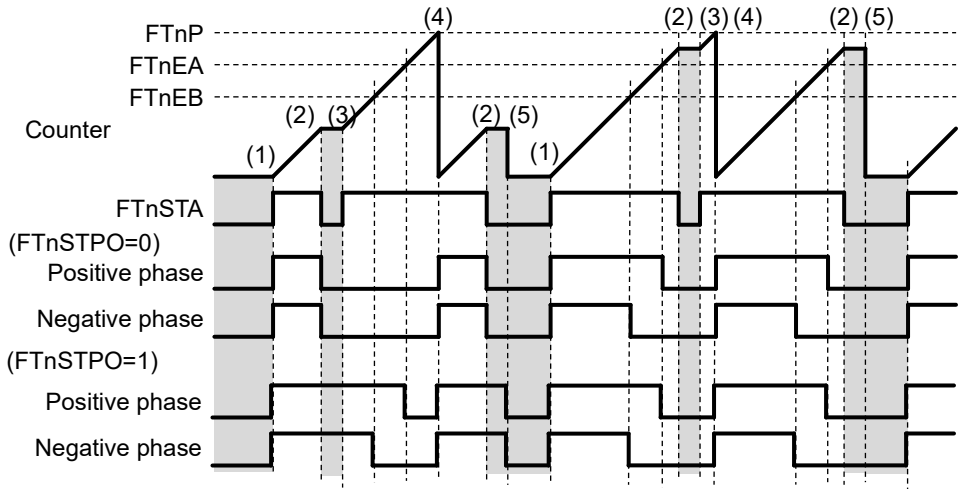
(2) If the FTnSTPO bit is "1":
The Positive/Negative phase output remains the state at the time the counter is stopped. When counting is restarted, the state changes according to the count value.

If writing "1" to the FTnSTC bit of the FTnTRG0 register or clearing the counter by the software after the counting operation is stopped, the counter value is counted up from "0x0000", and the output varies depending on the count value.

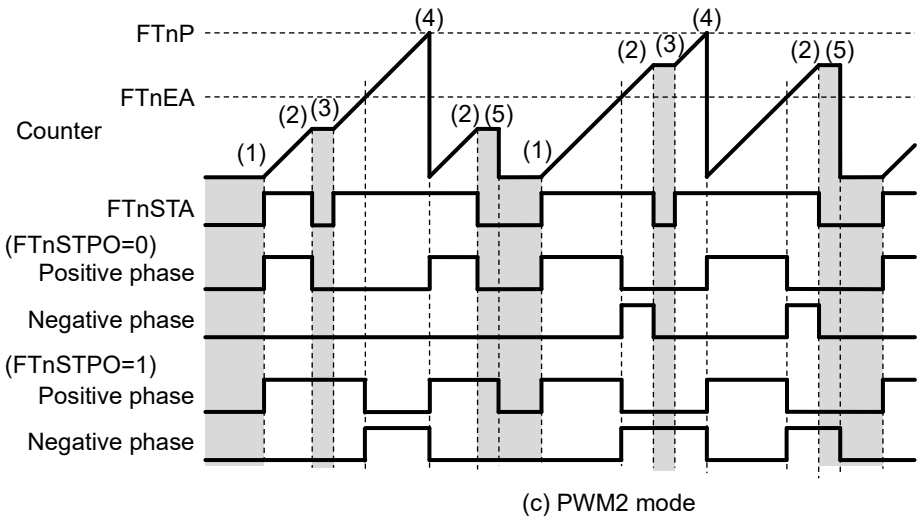
FTnSTPO bit of FTnMOD register is used to choose output conditions when the counter stops.
Figure 9-6 shows output waveforms of each mode when the FTnSTPO bit of the FTnMOD register is "0" / "1".



(a) TIMER mode



(b) PWM1 mode



(c) PWM2 mode

Counter operation
(1) Counter start
(2) Counter stop
(3) Counter restart without clear the counter
(4) Counter overflow
(5) Counter clear

Stopping counter

Figure 9-6 Waveforms of the positive phase/negative phase output with counter stop

9.3.3.5 Output with DUTY=100%,0%

PWM output waveforms is configured to duty 0% and 100% by the FTnEA/EB registers setting in the PWM1/PWM2 mode.
When FTnEA/FTnEB value is the same as FTnP value, the duty is 100%. When FTnEA/FTnEB value is 0xFFFF, the duty is 0%. When both FTnP and FTnEA/EB is 0xFFFF, the duty is 0%.
When setting to the duty = 100% with deadtime enabled, the dead time apply at first cycle only.
Figure 9-7 shows output waveforms with 0% and 100% in the PWM1 mode.

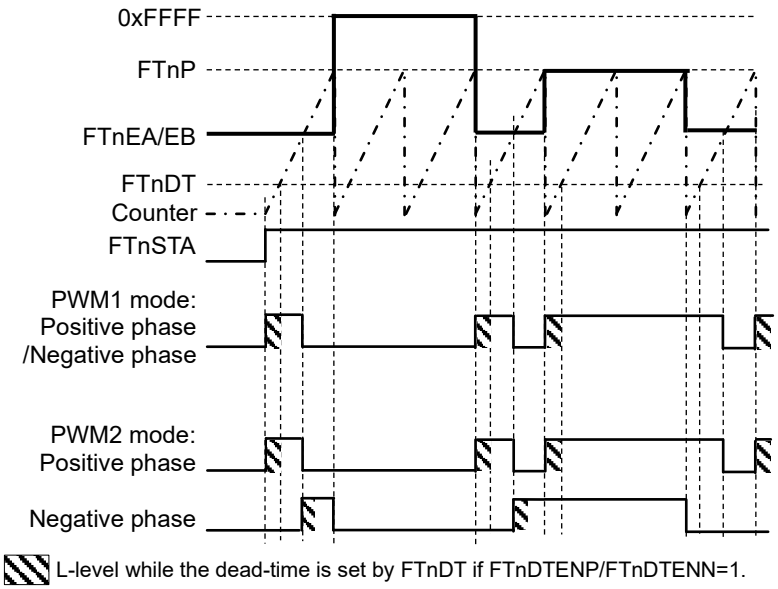


Figure 9-7 Waveforms of the positive phase/negative phase output with the duty is 0% and 100%

9.3.4 CAPTURE Mode

The CAPTURE mode stores the count value, which was obtained when an event trigger source was generated, in the FTnEA or FTnEB register.
The event trigger source for the capture is common to that used for counter start/stop.

Stored data in FTnEA register	Count value at the time when an event trigger rising edge is generated
Stored data in FTnEB register	Count value at the time when an event trigger falling edge is generated

9.3.4.1 Operation Example in CAPTURE Mode

The following example shows the operation of one cycle and duty of the PWM signal input from the EXTRG0 pin in the CAPTURE mode using the counter start/stop through trigger events.
Set each register in the following steps before measuring.

Step 1: Write "01" to the FTnMD1 and FTnMD0 bits of the FTnMOD register to choose the CAPTURE mode.
Step 2: When using an interrupt, write "1" to the FTnIETS bit of the FTnINTE register to enable the trigger counter stop interrupt.
Step 3: Write "0" to the FTnSTSS bit of the FTnTRG0 register, "0000" to FTnSTS3 to FTnSTS0 bits to set the source of the trigger event to "EXTRG0". Write "1" to the FTnST bit to enable the start function of the counter. Write "1" to the FTnSP bit to enable the stop function of the counter.
Step 4: Write "000" to FTnTRM2 to FTnTRM0 bits of the FTnTRG1 register to choose the trigger through the rising edge for both of counter start/stop.
Step 5: Write "1" to the FTnETG bit of the FTCSTR register to enable the trigger operation of capturing.

Figure 9-8 shows the time chart in this example.

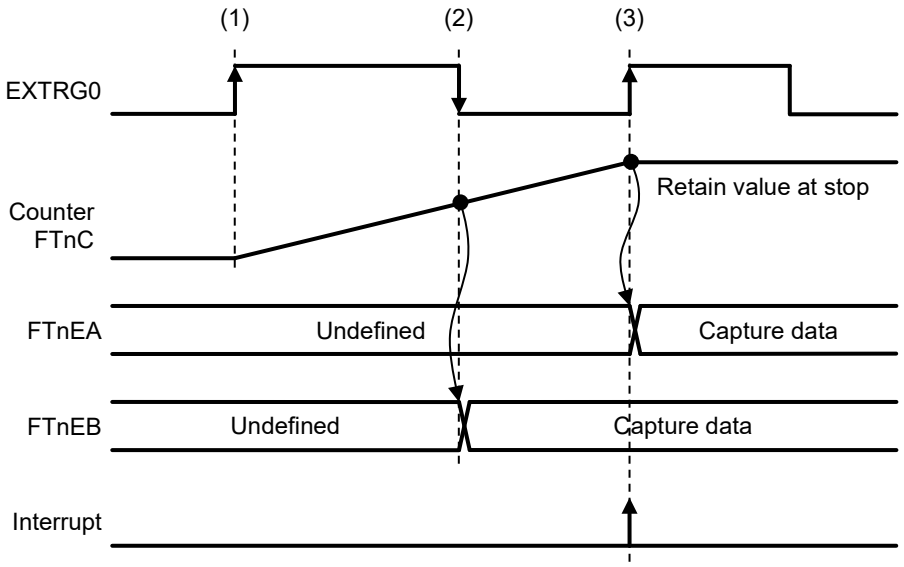


Figure 9-8 Operation Example to measure cycle and duty of PWM signal (one cycle)

(1) The counter starts operating at the rising edge of the signal input from the EXTRG0 pin.
(2) The value of the FTMn counter register FTnC is stored into the FTnEB register at the falling edge of the EXTRG0 pin.
(3) The value of the FTMn counter register FTnC is stored into the FTnEA register at the rising edge of the EXTRG0 pin. The counter stop the operation and the interrupt is generated.
(4) The counter stops and the interrupt occurs.

The value of the FTnEA register corresponds to the cycle of the PWM signal input from the EXTRG0 pin, and the value of the FTnEB register corresponds to the duty.

This is an example for measuring the cycle and duty of the PWM signal input from the EXTRG0 pin by the start/stop of a trigger event. Configure registers as follows before the measurement.

Step 1: Choose the CAPTURE mode by writing "01" to FTnMD1 and FTnMD0 bits of FTnMOD register.
Step 2: When using the interrupt, set FTnIEA bit of FTnINTE register to "1" to enable the event timing A interrupt.
Step 3: Set FTnSTSS bit of FTnTRG0 register to "0"and set FTnSTS3 to FTnSTS0 bits to "0000" to configure the EXTRG0 as the trigger event source. Set FTnST bit to "1" to enable the start function of the counter. Set FTnSTC bit to "1" to enable the counter clear when the trigger event of counter start occurs.
Step 4: Set FTnTRM2 to FTnTRM0 bits of FTnTRG1 register to "000" to choose the rising edge as the trigger for both the counter start and stop.
Step 5: Set FTnETG bit of FTCSTR register to "1" to enable the trigger operation.

Figure 9-9 shows the time chart in this example.

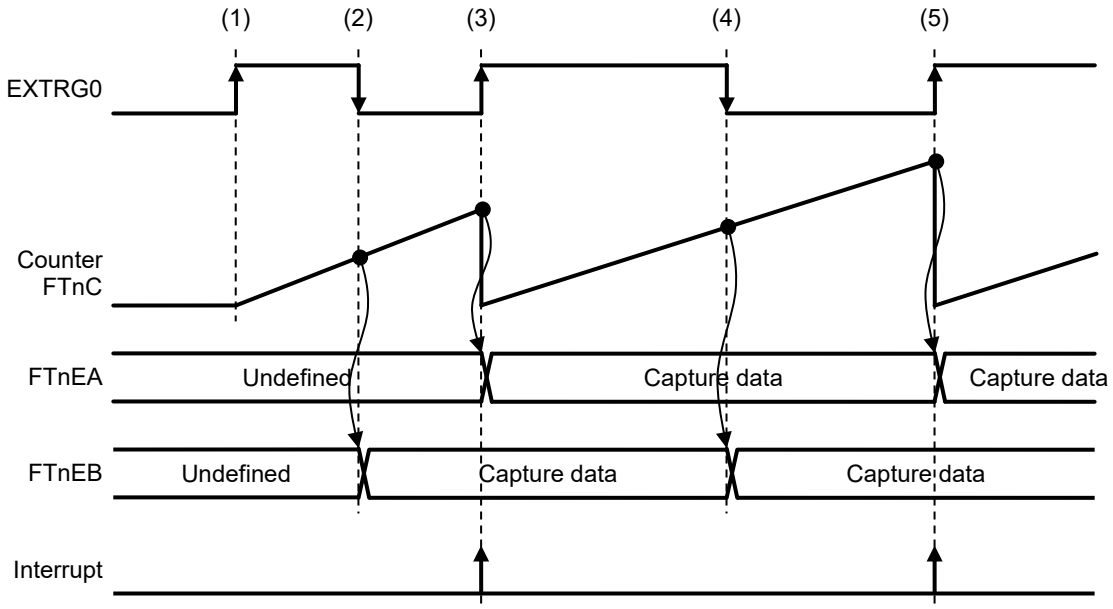


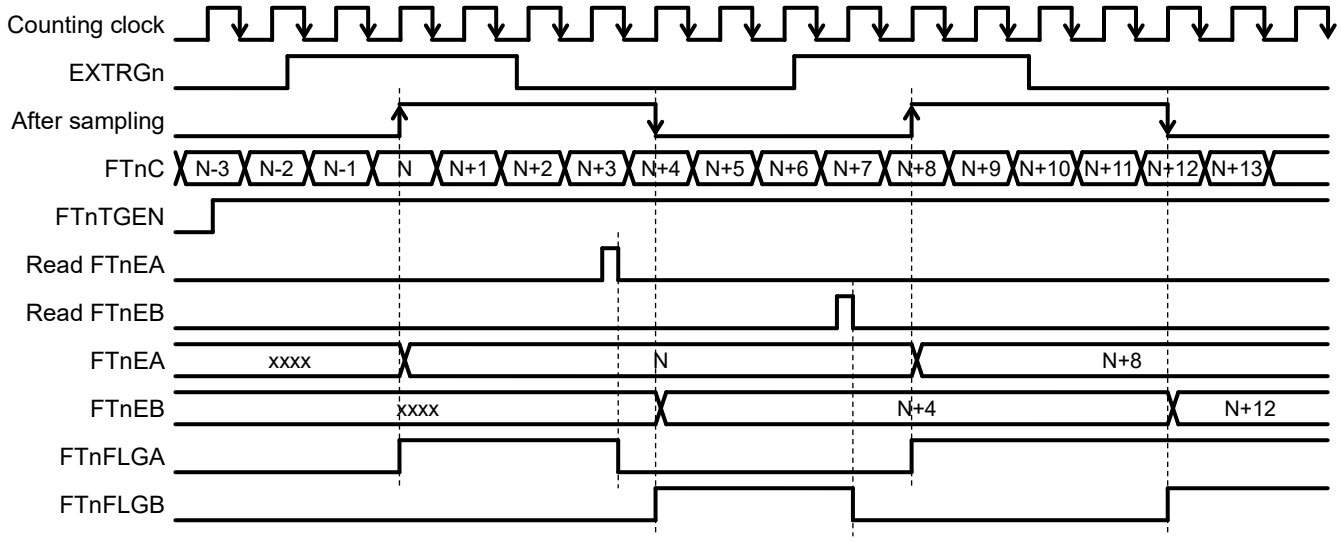
Figure 9-9 Operation Example to measure cycle and duty of PWM signal (repeat cycle)

(1) The counter starts operating at the rising edge of the signal input from the EXTRG0 pin.
(2) The value of the FTMn counter register; FTnC is stored into the FTnEB register at the falling edge of the EXTRG0 pin.
(3) The value of the FTnC is stored into the FTnEA register at the rising edge of the EXTRG0 pin. The counter is cleared and the interrupt is generated. The count operation continues.
(4) The value of the FTnC is stored into the FTnEB register at the falling edge of the EXTRG0 pin.
(5) The value of the FTnC is stored into the FTnEA register at the rising edge of the EXTRG0 pin. The counter is cleared and the interrupt is generated. The count operation continues.

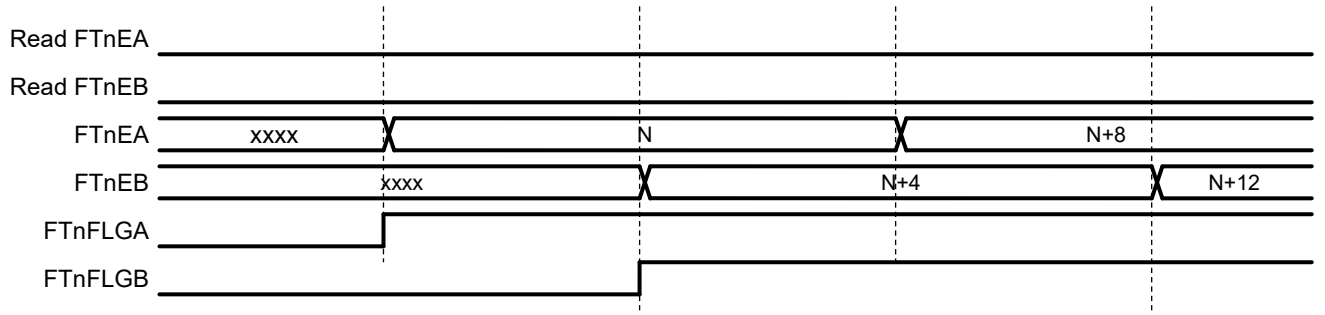
The value of the FTnEA register corresponds to the cycle of the PWM signal input from the EXTRG0 pin, and the value of the FTnEB register corresponds to the duty.

In addition, the operation following the capturing is depending on the setting value in the FTnOST bit of the FTnMOD register.

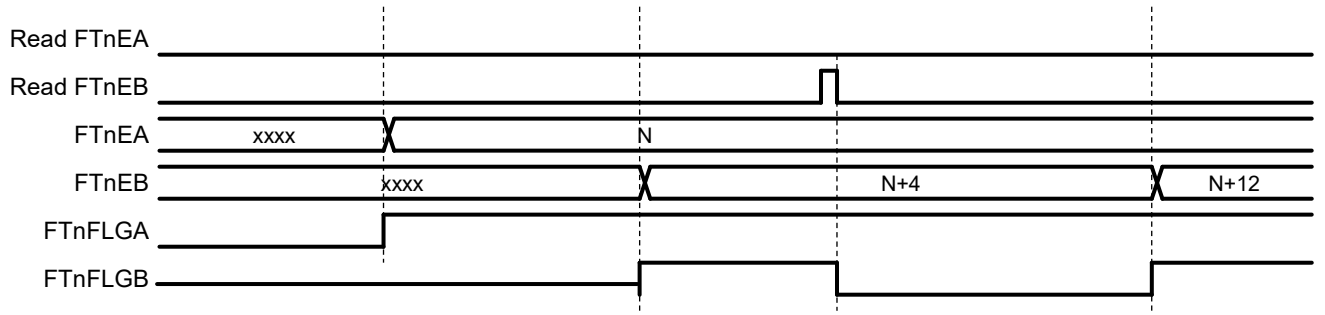
- In the auto mode (FTnOST=0)
  The value of the FTnEA register is updated when the counter is restarted with the signal rising again.
- In the single mode (FTnOST=1)
  The value of the FTnEA register is not updated when the counter is restarted with the signal rising again.



(a) When read the register before the next trigger (common to FTnOST = 0,1)



(b) When not read the register before the next trigger (FTnOST = 0)



(c) When not read the register before the next trigger (FTnOST = 1)

Figure 9-10 Operation Timing in CAPTURE Mode

9.3.4.2 Clearing FTnFLGA/FTnFLGB bit

In single mode(FTnOST=1), FTnEA/FTnEB data is not updated if FTnFLGA/FTnFLGB is 1 each.
The FTnFLGA/FTnFLGB is cleared by reading FTnEA/FTnEB, respectively. However it is invalid when FTnTGEN=0.
Even if FTnFLGA/FTnFLGB is cleared and FTnTGEN is set to 0, a trigger may be entered during control and FTnFLGA/FTnFLGB may be set to 1.

To avoid this, set FTnTGEN to 0 after making sure that FTnFLGA/FTnFLGB is 0 with no trigger input. For example, set FTnST to 0 and stop the trigger start. Or initialize this peripheral circuit by block reset after setting FTnTGEN to 0.

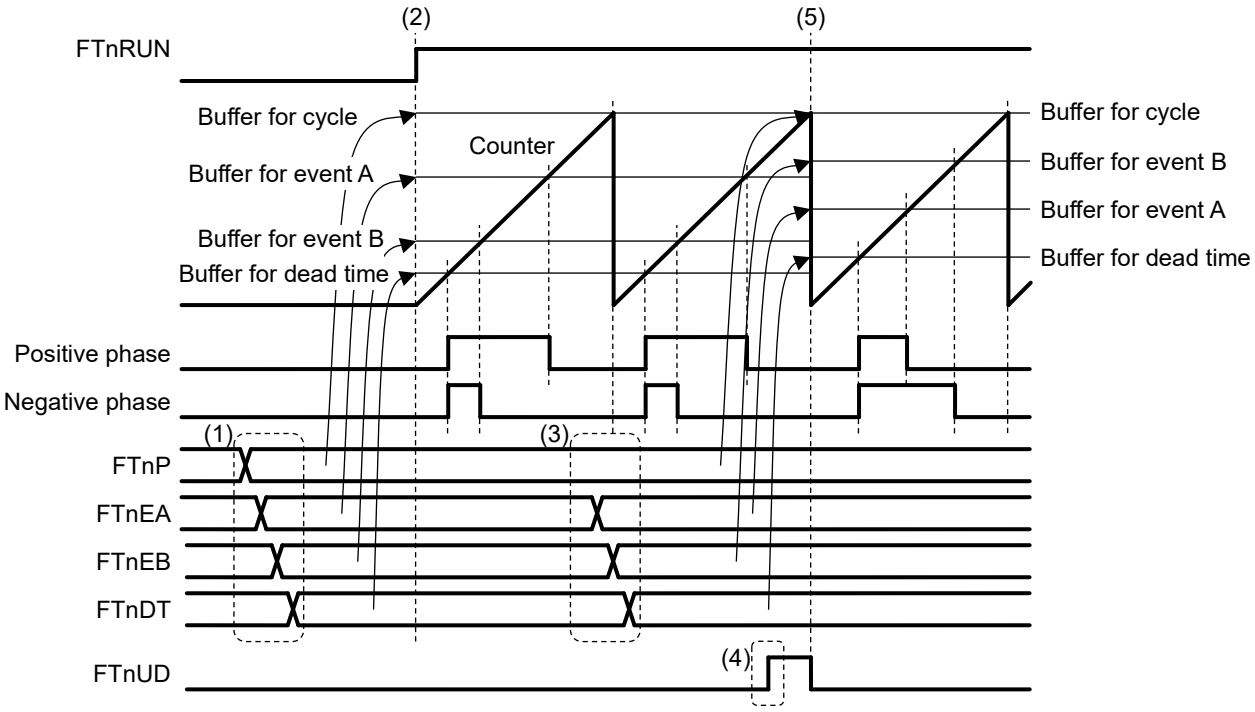
9.3.5 Changing Cycle, Event A/B, and Dead Time during Operation

The cycle, event A/B, and dead time can be updated by setting FTnP/ FTnEA/ FTnEB/ FTnDT registers.
The update timing is depending on the counter operation status and the counter value when writing data to the registers.

Table 9-4 Update timing

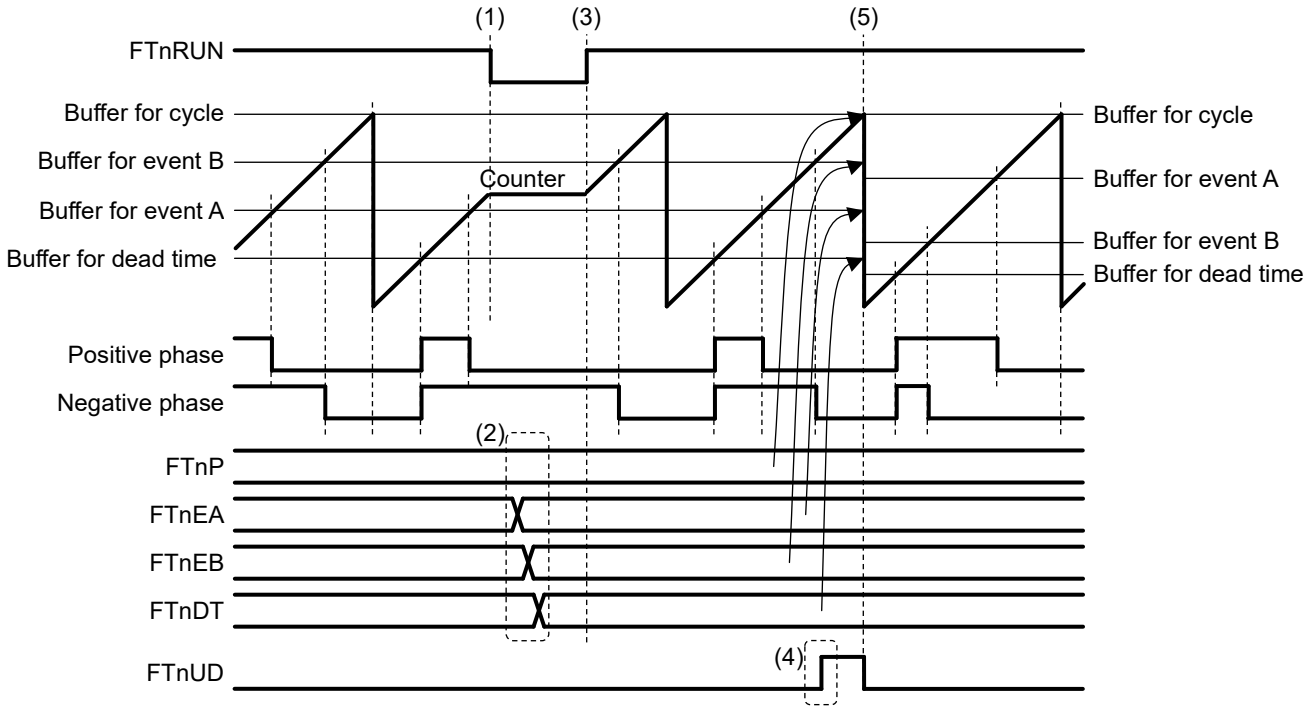
Counter operation status when setting the register	Counter value when setting the register	Update timing
Stop	0x0000	Updated at the counter start
Stop	Other than 0x0000	Updated at the start of cycle while the counter has been restarting and FTCUDn bit is set to "1".
Operating	Any value	Updated at the start of cycle while the counter is operating and FTCUDn bit is set to "1".
Trigger clear	0x0000	Cleared with trigger when the counter is running and FTCUDn =1.

Figure 9-11 shows the operating waveforms when the registers are updated while the counter stops (counter value is 0x0000) or the counter is operating.
Figure 9-12 shows the operating waveforms when the registers are updated while the counter stops (counter value is other than 0x0000).



(1) Update the registers while the counter stops (counter value is 0x0000)
(2) Each buffer is update at the start of counter operation
(3) Update the registers while the counter is operating
(4) Set FTnCUDn bit to "1"
(5) Each buffer is updated at the start of cycle and the FTnUD bit gets cleared

Figure 9-11 Update timing while the counter stops (counter value is 0x0000) or the counter is operating



(1) The counter stops
(2) Update the registers while the counter stops (counter value is other than 0x0000)
(3) The counter operation restarts (Each buffer is not updated at this timing)
(4) Set FTCUDn bit to "1"
(5) Each buffer is updated at the start of cycle and the FTnUD bit gets cleared

Figure 9-12 Update timing while the counter stops(counter value is other than 0x0000)

9.3.6 External clock input/Event Trigger/Emergency Stop Trigger Control

The functional timer can accept external clock input and two types of trigger signal: event trigger and emergency stop trigger.
The external clock input selected in the EXTRG0 to EXTRG7 is used as the count clock.
The event trigger is used as counter start/stop or trigger for capture. The trigger source can be chosen from EXTRG0 to EXTRG7, LTB1INT to LTB3INT, TMH0INT to TMH4INT, TMHXINT, FTMnTRG or RC1K.
The emergency stop trigger stops the timer operation. It stops the counter and makes the Positive/Negative output "L" level. The trigger source can be chosen from EXTRG0 and EXTRG4.

The EXTRG0 to EXTRG7 are output of sampling controller of the external interrupt function. They are connected to functional timer as event trigger or external clock input.
These input signals are delayed 2 clocks of the timer clock.

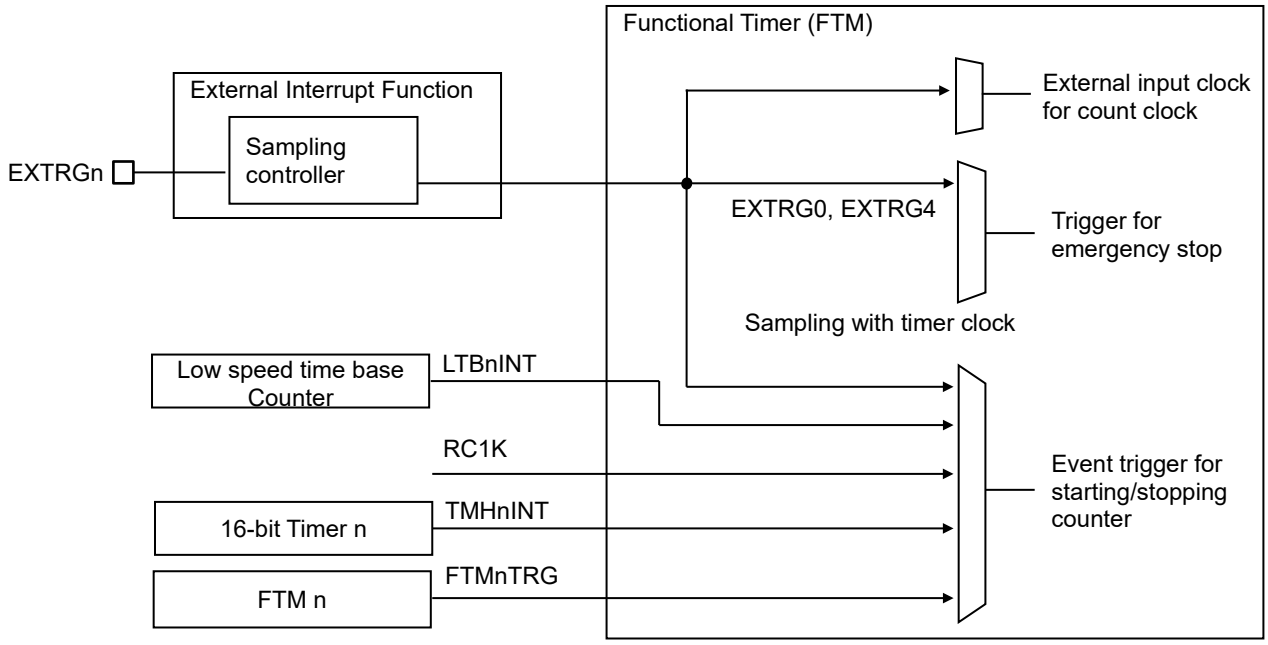


Figure 9-13 Input Path of Trigger Signal

9.3.6.1 Start/Stop Operations by Event Trigger

Here is the setting used to control the counter by event triggers.
First, before controlling the counter, set the following configuration by FTnTRG0 and FTnTRG1 registers.

Choose "no division" as the timer clock.
If using HSCLK as the system clock, write "1" to the FTnCK0 bit of the FTnCLK register, and "000" to FTnCKD2 to FTnCKD0 bits.

Setting the FTnTRG0 register
- Enable/disable counter start/stop with event triggers
- Clear/not clear the counter when starting/stopping with event triggers
- Accept/not accept the next counter start after stopping with event triggers
- Accept/not accept the counter clear if the Positive phase output is "H" level when clearing the counter with event triggers.
- Event trigger source (EXTRG0 to EXTRG7, LTB1INT to LTB3INT, TMH0INT to TMH4INT, TMHXINT, FTMnTRG)

Setting the FTnTRG1 register
The edge/level of the event trigger causing counter start
The edge/level of the event trigger causing counter stop

Setting the timer clock used
Select the timer clock and count clock in the FTnCLK register.

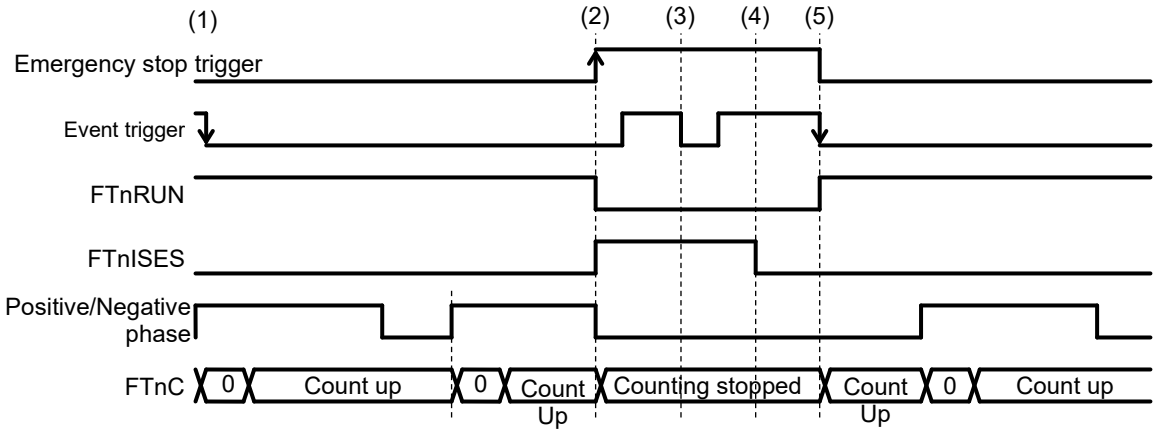
Once the configuration above is completed, control the counter by the FTCSTR register. The procedure is as follows:

(1) Make the waiting state for an event trigger
Write "1" to the FTnETG bit to make the waiting state for an event trigger. If the level setting is applied for trigger start and the level is applicable, the counter operation is started as soon as the FTnTGEN bit of the FTCSTAT register becomes "1".
(2) Start the timer counting by the software
If writing "1" to the FTnETG bit, and writing "1" to the FTnSTR bit with the trigger operation enabled, the timer counting is started by the software.
If writing "0" to the FTnSTP bit of the FTCSTP register while counter operation is in progress, the timer counting is stopped by the software.

9.3.6.2 Emergency Stop Operation

The emergency stop function is enabled by writing "1" to the FTnEMGEN bit of the FTCCON register. Set the FTnEMGEN bit after the trigger source is chosen in the FTnEST bit of the FTnTRG0 register.

If the emergency stop trigger input (rising edge) is present, the counter is stopped, brings Positive/Negative phase output to "L" level, and generates an emergency stop interrupt.
To restart the counter operation, write "1" to the FTnICES bit of the FTnINTC register to clear the emergency stop interrupt status.
Figure 9-14 shows the operation timing at emergency stop.



(1) The counter operation starts by the event trigger (falling edge).
(2) The counter stops at by the emergency stop trigger (rising edge). The emergency stop interrupt occurs.
(3) The event trigger is disabled due to the emergency stop in progress.
(4) Clear the emergency stop interrupt to enable the operation.
(5) The counter operation restarts by the event trigger (falling edge).
(The counter is not cleared in this example, so pulse output is restarted after one cycle)

Figure 9-14 Operation Timing Diagram at Emergency Stop

Once the emergency stop occurs, the counter is stopped after two clocks of the timer clock, and the FTnISES bit of the FTnINTS register becomes "1" (see (2) in Figure 9-14).
When the FTnISES bit is "1", even if the event trigger of counter start is generated, it is not accepted. If the event trigger for the counter start is generated after the FTnISES bit is cleared (see (4) in Figure 9-14), counting up is restarted (see (5) in Figure 9-14).
To restart the counting operation by the software, make sure that the FTnISES bit becomes "0".

9.3.7 Interrupt

This section describes the interrupt source and how to clear it.
Writing "1" to the corresponding bit (FTnIE*) of the FTnINTE register causes each interrupt request to be enabled.
Note that permission of the emergency stop interrupt is not available. If the emergency stop function is enabled, the interrupt are also enabled.
For the source which caused the interrupt status to become "1", write "1" to each interrupt status clear bit (FTnIC*) to clear each interrupt status bit (FTnIS*).
If using an interrupt, clear each interrupt status bit (FTnIS*) at the end of the interrupt routine.

Confirm that there is no unhandled interrupt before stopping FTM. The interrupt status is not cleared when you stop FTM while there are some unhandled interrupts.

Table 9-5 Interrupt status

Name	Status	Mode	How to set	How to clear
Cyclic interrupt	FTnISP bit	All modes	When FTnC = FTnP	Write "1" to FTnICP bit
Event timing A interrupt	FTnISA bit	TIMER/PWM1/ PWM2	When FTnC = FTnEA	Write "1" to FTnICA bit
		CAPTURE	When stored capture data into FTnEA	Write "1" to FTnICA bit, or read the FTnEA register
Event timing B interrupt	FTnISB bit	TIMER/PWM1	When FTnC = FTnEB	Write "1" to FTnICB bit
		CAPTURE	When stored capture data into FTnEB	Write "1" to FTnICB bit, or read the FTnEB register
Trigger stop interrupt	FTnISTS bit	All modes	Counter stop/clear by trigger-stop event	Write "1" to FTnICTS bit
Trigger start interrupt	FTnISTR bit	All modes	Counter start/clear by trigger-start event	Write "1" to FTnICTR bit
Emergency stop interrupt	FTnISES bit	All modes	Occurring emergency stop	Write "1" to FTnICES bit

The cyclic interrupt/event timing A interrupt/event timing B interrupt can be chosen as the interrupt trigger output.

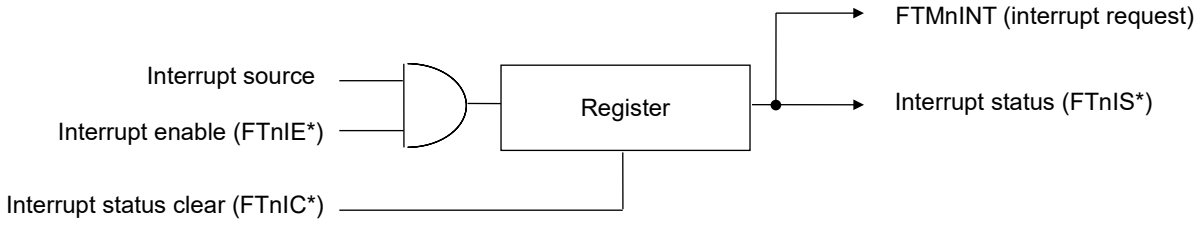


Figure 9-15 Interrupt Control Signal

Chapter 10 Watchdog Timer

10. Watchdog Timer

10.1 General Description

The watchdog timer (WDT) is equipped with the following functions and can detect the runaway state of program or the undefined state of the CPU by generating an interrupt or reset when an abnormality occurs.

- If the counter is not cleared for more than a certain time period in program operation and overflows, the WDT interrupt is generated in the first overflow and the WDT reset in the second overflow (if the window function is disabled).
- If the counter is not cleared for more than a certain time period in program operation and overflow occurs, the WDT reset is generated in the first overflow (if the window function is enabled).
- If the counter is cleared in the unexpected time period, the WDT invalid clear reset is generated (if the window function is enabled).

The window function refers to the function through which "the time period during which WDT counter clear is enabled" = "the time period during which the window is opened" and
"the time period in which WDT counter clear is disabled" = "the time period in which the window is closed" can be set.

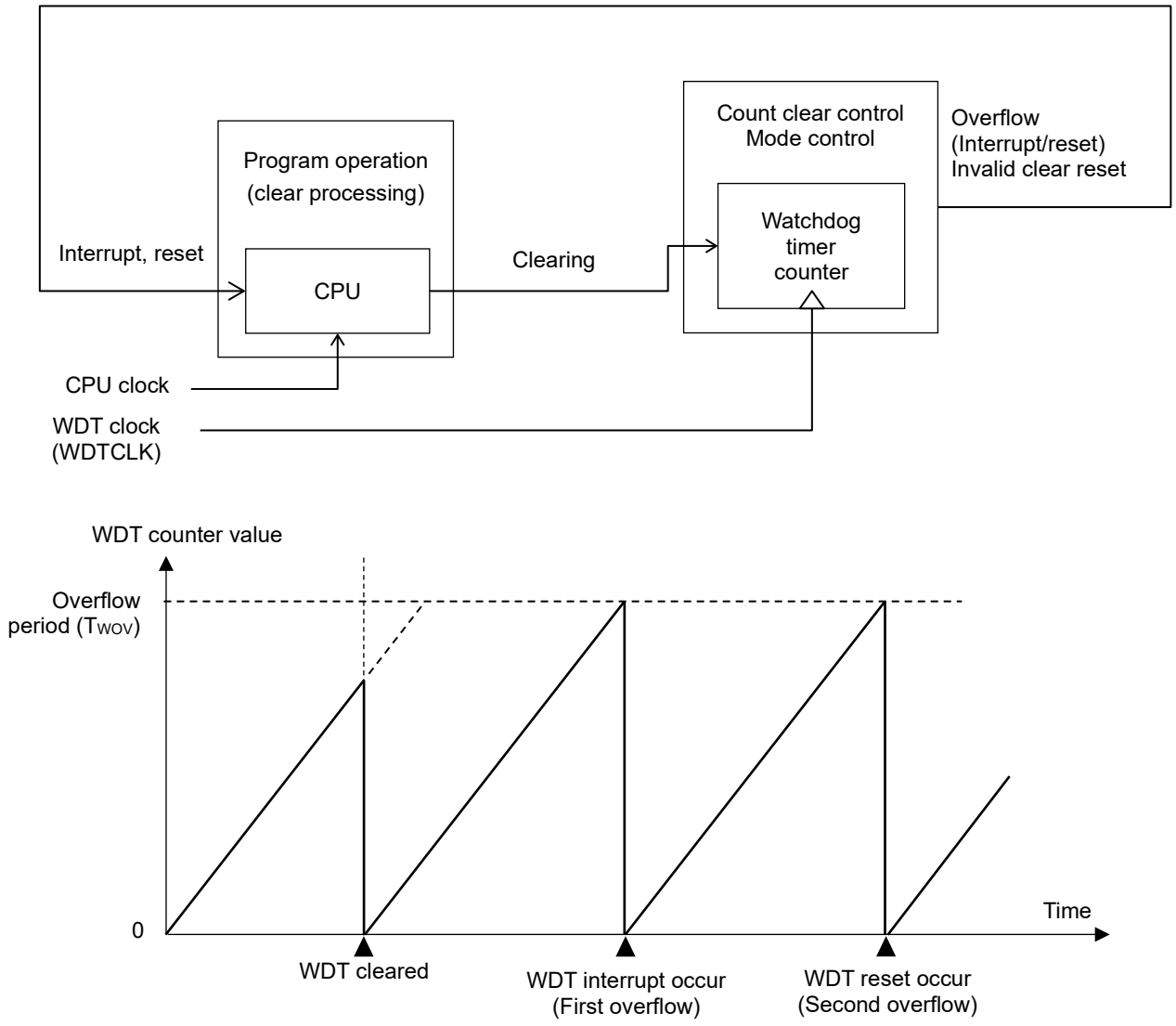


Figure10-1 Watchdog Timer Overview (With the Window Function Disabled)

10.1.1 Features

- Eight types of overflow periods are selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2s, or 8s)
- Two ways to use:
  - Window function disabled mode
    The WDT counter can always be cleared. The WDT interrupt is generated when the first counter overflow occurs, and the WDT reset is generated when the second counter overflow occurs.
  - Window function enabled mode
    The periods during which WDT counter clear is enabled and disabled respectively can be set. The WDT reset is generated when the first counter overflow occurs, and the WDT invalid clear reset is generated when the counter is cleared in the period during which WDT counter clear is disabled.

Table 10-1 Watchdog Timer Operation Modes

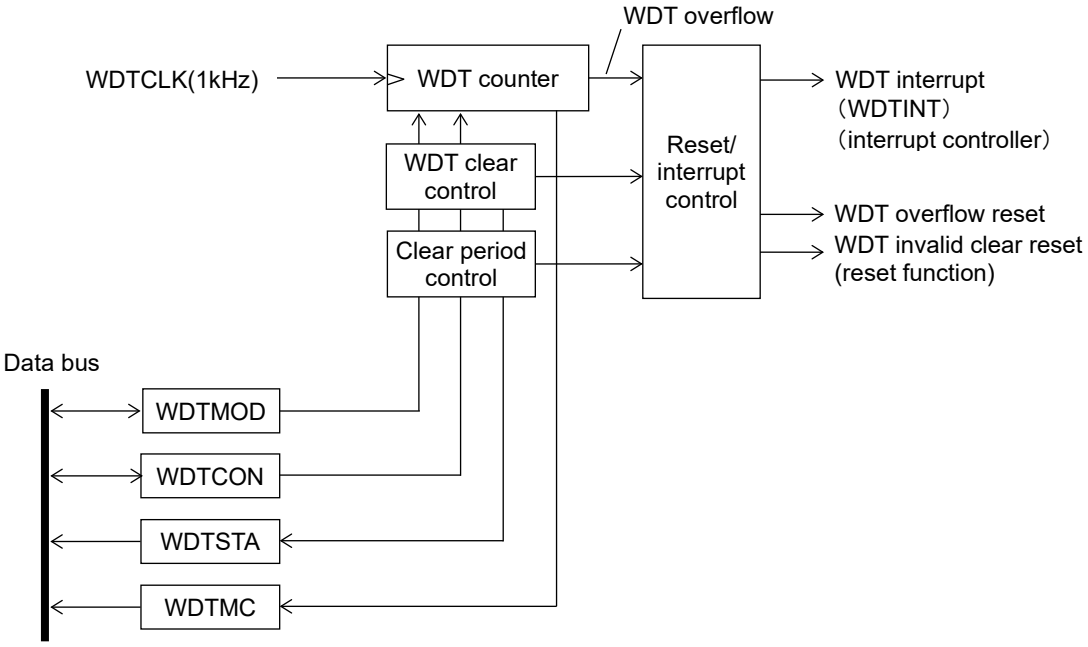
Mode	overflow		WDT invalid clear reset
	First	Second	
Window function disabled mode	WDT Interrupt	WDT Reset	-
Window function enabled mode	WDT Reset	-	Generatable

- The following items are selectable by the code option. See the Chapter 30 "Code Option" for details.
  - Enabling/disabling the WDT timer operation
  - Enable/Disable WDT timer operation for each HALT/HALT-D mode
- Dedicated internal RC oscillating clock (frequency accuracy is ± 10%)

[Note]
- **There is a limit to the abnormal operation that the watchdog timer can detect. Even if the CPU goes out of control, the watchdog timer is undetectable to the abnormality in the operation state in which the WDT counter is cleared.**
- **As fail safe, WDT counter clear at one place in the main loop of the program is recommended.**

10.1.2 Configuration

The following diagram shows the configuration of the watchdog timer.



WDTCON : Watchdog timer control register
WDTMOD : Watchdog timer mode register
WDTMC : Watchdog timer counter register
WDTSTA : Watchdog timer status register

Figure 10-2 Configuration of Watchdog Timer

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol name		R/W	Size	Initial value
		byte	Word			
0xF010	Watchdog timer control register	WDTCON	-	R/W	8	0x00
0xF011	Reserved register	-	-	-	-	-
0xF012	Watchdog timer mode register	WDTMOD	-	R/W	8	0x06
0xF013	Reserved register	-	-	-	-	-
0xF014	Watchdog timer counter register	WDTMCL	WDTMC	R	8/16	0x00
0xF015		WDTMCH		R	8	0x00
0xF016	Watchdog timer status register	WDTSTA	-	R	8	0x01
0xF017	Reserved register	-	-	-	-	-

10.2.2 Watchdog timer control register (WDTCON)

WDTCON is a SFR to clear the WDT counter.

Address: 0xF010 (WDTCON)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								WDTCON							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 0	d7 to d0	Clear the WDT counter by writing "0x5A" with the WDP bit "0" and then writing "0xA5" with the WDP bit "1". In the window mode, WDT counter is cleared during the WDT clearing disabled period, a WDT invalid clear reset will occur.
0	WDP	Read the value of the WDT bit internal pointer. WDP bit is reset to "0" during system reset and WDT counter overflow, and is inverted when data is written to the WDTCON register, regardless of the data written.

[Note]

- **In the WDT interrupt routine (when the interrupt level (ELEVEL) of the CPU program status word (PSW) is "2"), the WDT counter is unable to get cleared.**

10.2.3 Watchdog Timer Mode Register (WDTMOD)

WDTMOD register is a SFR to set the overflow period and the clear enabled period of the WDT counter.

Address: 0xF012 (WDTMOD)
Access: R/W
Access size: 8 bit
Initial value: 0x06

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								WDTMOD							
Bit	-	-	-	-	-	-	-	-	-	-	WOVF1	WOVF0	-	WDT2	WDT1	WDT0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit No.	Bit symbol name	Description
7, 6, 3	-	Reserved bits
5, 4	WOVF1, WOVF0	Set the mode of WDT. 00: Window function disabled (initial value) 01: Window function enabled mode 1 (the clear enabled period is approximately 75% of the overflow period) 10: Window function enabled mode 2 (the clear enabled period is approximately 50% of the overflow period) 11: Setting disabled (setting of window function enabled mode 2) If the overflow period of the WDT counter is set to 62.5 ms or less in WDT2 to 0 bits, the window function is disabled regardless of setting values of WOVF1 and WOVF0 bits.
2 to 0	WDT2 to WDT0	Set the overflow period (T_{WOV}) of the WDT counter. 000: Approx. 7.8 ms 001: Approx. 15.6 ms 010: Approx. 31.3 ms 011: Approx. 62.5 ms 100: Approx. 125 ms 101: Approx. 500 ms 110: Approx. 2 s (initial value) 111: Approx. 8 s where frequency of WDTCLK is 1.024kHz.

[Note]

- **See ML62Q2700 data sheet for accuracy of WDTCLK .**

10.2.4 Watchdog Timer Counter Register (WDTMC)

WDTMC is a SFR to read the WDT counter value.

Address: 0xF014
Access: R
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	WDTMC															
Byte	WDTMCH								WDTMCL							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 0	d15 to d0	Read the WDT counter value. By confirming that the values of the WDT counters read periodically are different, it is confirmable that WDT counters are counting normally.

10.2.5 Watchdog Timer Status Register (WDTSTA)

WDTSTA is a read-only special function register (SFR) to indicate the WDT counter clearing state.

Address: 0xF016 (WDTSTA)
Access: R
Access size: 8 bit
Initial value: 0x01

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								WDTSTA							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	WDTWIN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	WDTWIN	Indicate the status of enabling/disabling WDT counter clearing. It is always “1” when a window function is disabled 0: Clearing is disabled. 1: Clearing is enabled (initial value).

10.3 Description of Operation

When the system reset is cleared while enable operating is selected in the code option, the WDT counter starts counting up at the rising edge of the operating clock (WDTCLK) of the WDT counter also selected in the code option.

The WDT counter is cleared by writing "0x5A" to the WDTCON register with the WDP bit is in "0" state and then writing "0xA5" to the WDTCON register with the WDP bit is in "1" state while WDT counter clearing is enabled.
The WDP bit is reset to "0" during system reset and WDT counter overflow, and is inverted each time it is written to the WDTCON register.

Window function disabled mode and Window function enabled mode are available.

- Window function disabled mode
  The WDT counter can be cleared at all the time. The WDT interrupt is occurred when the counter overflows for the first time, and the WDT reset is occurred when the counter overflows a second time.
- Window function enabled mode
  The periods during which WDT counter clear is enabled and disabled respectively can be set. The WDT reset is occurred when the counter overflows for the first time, and the WDT invalid clear reset is occurred when the counter is cleared in the period during which WDT counter clear is disabled.

Table 10-2 Watchdog Timer Operation Modes

Mode	Overflow		WDT invalid clear reset
	First	Second	
Window function disabled mode	WDT Interrupt	WDT Reset	-
Window function enabled mode	WDT Reset	-	Reset

The WDT counter overflow period (T_{WOV}) and the WDT counter clear enabled period (T_{WCL}) are selectable through the WDTMOD register.

The following items are selectable with the code option. See Chapter 30 "Code Option" for details on how to set the code option.

- Enabling/disabling the WDT timer operation
- Enabling/disabling the WDT timer operation in the HALT/HALT-H mode
- Enabling/disabling the WDT timer operation in the HALT-D mode

10.3.1 How to Clear WDT Counter

The WDT counter is cleared by writing "0x5A" to the WDTCON register with the WDP bit set to "0" and then writing "0xA5" to the WDTCON register with the WDP bit set to "1" while WDT counter clearing is enabled.
The WDP bit is reset to "0" during system reset and WDT counter overflow, and is inverted each time it is written to the WDTCON register.

The following shows the WDT counter clearing timing chart.

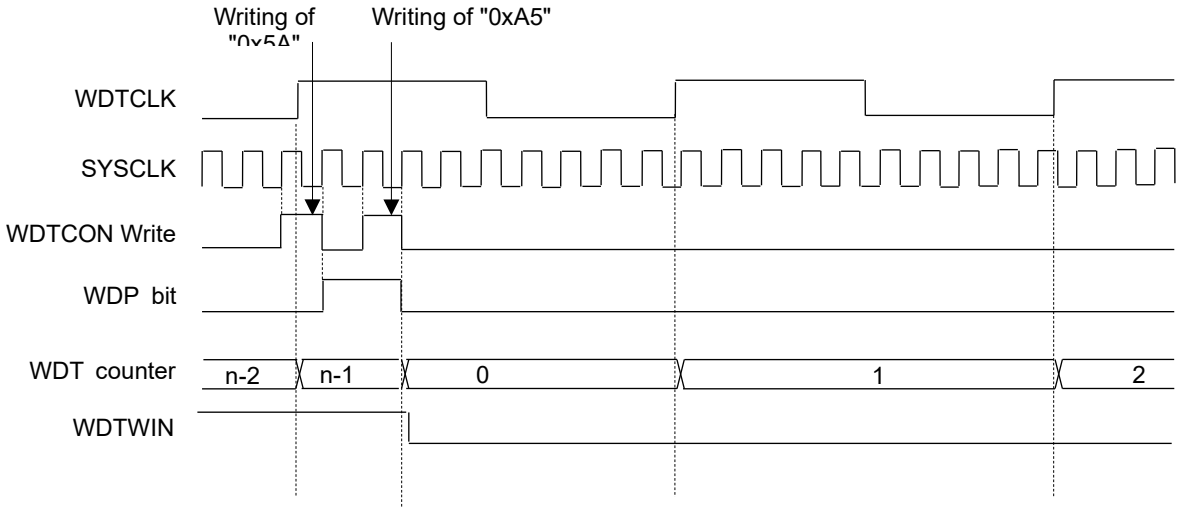


Figure 10-3 WDT Counter Clearing Timing Chart

The following description shows a sample program script of the watchdog timer.

```
void wdt_clear( void )
  {
    unsigned char pswval;

    if(WDTCLR1 == 1) {                  // Checking presence of pending clearing process
      return;
    };
    if(WDTCLR2== 1) {                   // Checking whether clearing process is pending or completed
      return;
    };

    pswval = s_drvcommon_getPSW();      // Saving PSW
    _DI();                              // Interrupt disabled (clearing MIE bit)
    do {
        WDTCON = 0x5A;                  // WDT counter clearing
      } while (WDP != 1 );
    WDTCON = 0xA5;
    if ((pswval & 0x08) != 0) {         // Confirming MIE bit
      _EI();                            // Interrupt enabled (setting MIE bit)
    }

    static unsigned char s_drvcommon_getPSW( void ){
      #pragma asm
      mov r0,psw
      rt
      #pragma endasm
    }
```

Figure 10-4 Sample Program Script of Watchdog Timer

[Note]
- **In the STOP/STOP-D mode, the WDT timer is stopped.**

10.3.2 Window Function Disabled Mode

In the window function disabled mode, if the WDT counter is not available to clear within the WDT counter overflow period (T_{WOV}) and the counter overflows for the first time, a WDT interrupt is generated. If the WDT counter is not cleared even by the software processing after the WDT interrupt, and overflows again, a WDT reset occurs.
The WDTR bit of the RSTAT register is set to "1" when the WDT reset occurs, and the state on the LSI is transferred to the system reset mode. See Chapter 3 "Reset Function" for details of the RSTAT register.

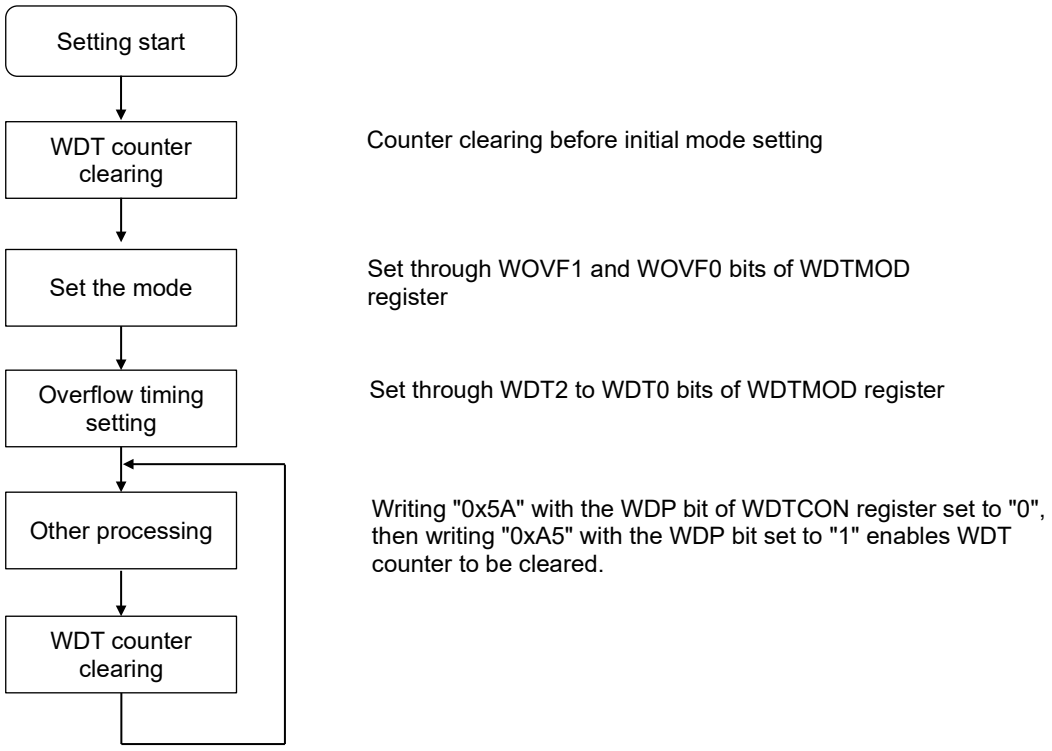


Figure 10-5 Procedure to Use WDT (in Window Function Disabled Mode)

The following shows an operation timing overview of the window function disabled mode.

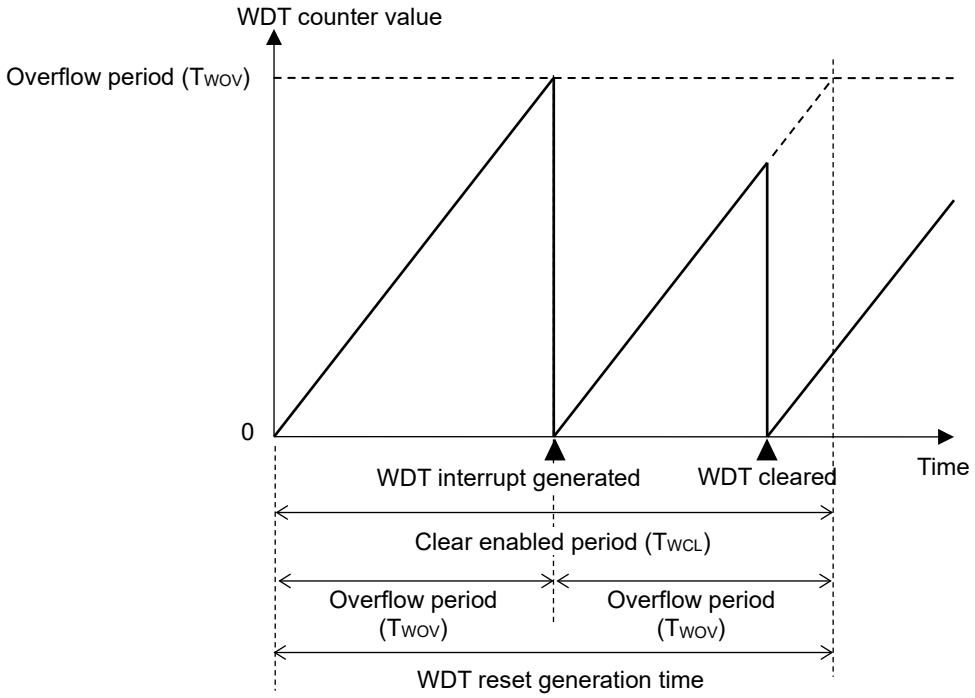


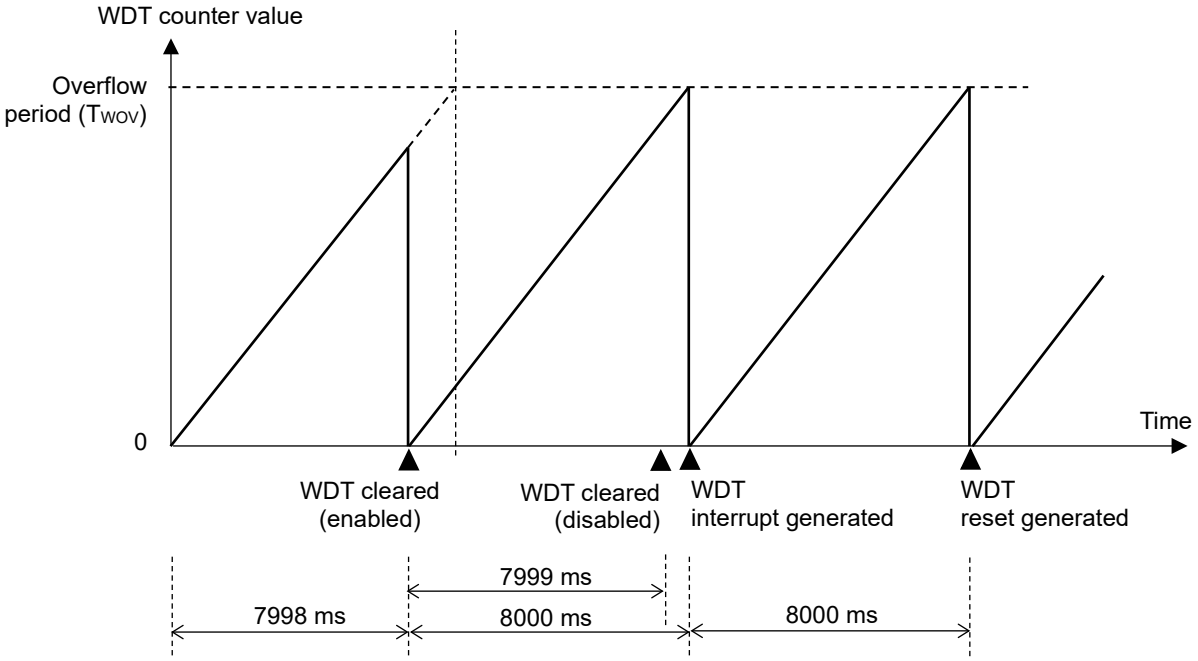
Figure 10-6 Overview of Operation Timing in Window Function Disabled Mode

The following table shows the WDT counter clear enabled period in the window function disabled mode.

Table 10-3 WDT Counter Clear Enabled Period in Window Function Disabled Mode

WDT2	WDT1	WDT0	Overflow period (T_{WOV})*1	WDT reset generation time*1	WDT counter clear enabled period (T_{WCL})*1
0	0	0	7.8 ms	15.6 ms	≈ Overflow period
0	0	1	15.6 ms	31.3 ms	≈ Overflow period
0	1	0	31.3 ms	62.5 ms	≈ Overflow period
0	1	1	62.5 ms	125 ms	≈ Overflow period
1	0	0	125 ms	250 ms	≈ Overflow period
1	0	1	500 ms	1000 ms	≈ Overflow period
1	1	0	2000 ms	4000 ms	≈ Overflow period
1	1	1	8000 ms	16000 ms	≈ Overflow period

*1: where the WDTCLK frequency is 1.024kHz(typ.) that is not included a significant error.



Design the WDT clear timing with margin to the timing.

Figure 10-7 Example of Operation Timing in Window Function Disabled mode (When Overflow Period=8000 ms)

The following figure shows details of operation timing in the window function disabled mode.

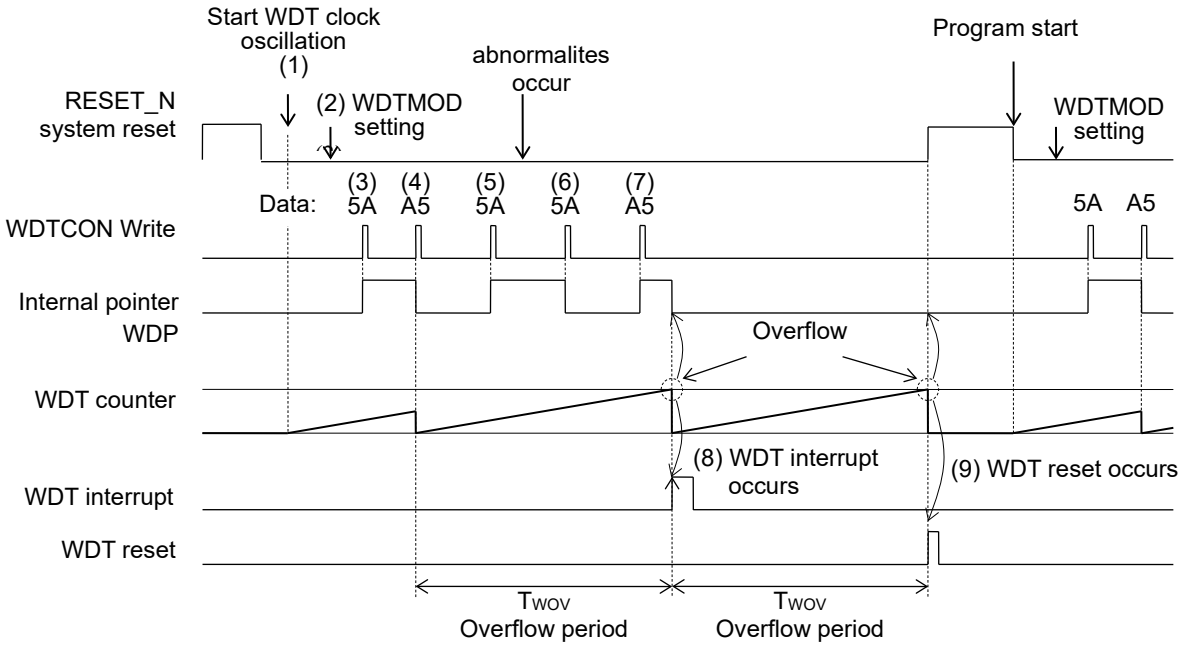


Figure 10-8 Details of Operation Timing in Window Function Disabled Mode

(1) After the system reset is released, the WDT counter starts counting up.
(2) The WDT counter overflow period (TWOV) is set to the WDTMOD register.
(3) "0x5A" is written to the WDTCON register. (Internal pointer WDP: 0 →1)
(4) "0xA5" is written to the WDTCON register to clear the WDT counter. (Internal pointer WDP: 1→0)
(5) "0x5A" is written to the WDTCON register. (Internal pointer WDP: 0 →1)
(6) When "0x5A" is written to the WDTCON register after an abnormality occurred, it is not accepted because the internal pointer WDP is "1". (Internal pointer WDP: 1 →0)
(7) Although "0xA5" is written to the WDTCON register, the WDT counter is not cleared because the internal pointer WDP is "0" and writing of "0x5A" is not accepted in (6). (Internal pointer WDP: 0 →1)
(8) The WDT counter overflows and a WDT interrupt request is generated. (Internal pointer WDP: 1 →0)
Following cleared due to the overflow, the WDT counter continues counting up.
(9) If the WDT counter is not cleared even by the software processing after the WDT interrupt and it overflows again, a WDT reset occurs and the shift to the system reset mode takes place.

10.3.3 Window Function Enabled Mode

In the window function enabled mode, if WDT counter is not available to clear within WDT clear enabled period and the counter overflows first time, WDT reset is occurred.
In addition, if WDT counter is cleared in the period the counter clear is not enabled, WDT invalid clear reset is occurred.

WDTR bit of RSTAT register is set to "1" when WDT overflow reset is occurred, and the state on the LSI is enter to the system reset mode.
WDTWR bit of RSTAT register is set to "1" when WDT invalid clear reset is occurred, and the state on the LSI is enter to the system reset mode.
See Chapter 3 "Reset Function" for details of RSTAT register.

In the window function enabled mode, two types of modes can be chosen through the WDTMOD register:

- Window function enabled mode 1 (the clear enabled period is approximately 75% of the overflow period)
- Window function enabled mode 2 (the clear enabled period is approximately 50% of the overflow period)

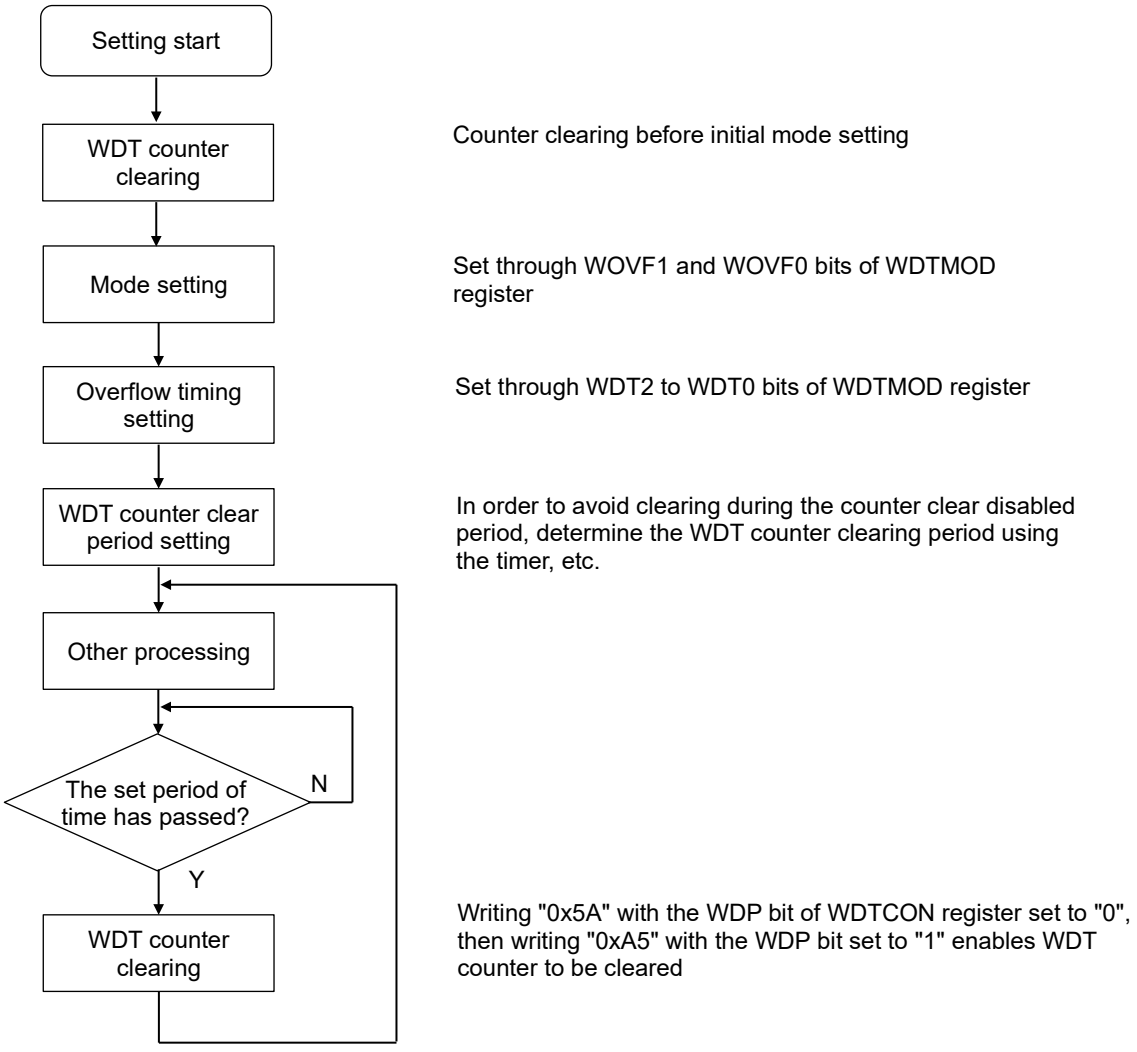


Figure 10-9 Procedure to Use WDT (in Window Function Enabled Mode)

Overviews of the operation of each mode are shown below.

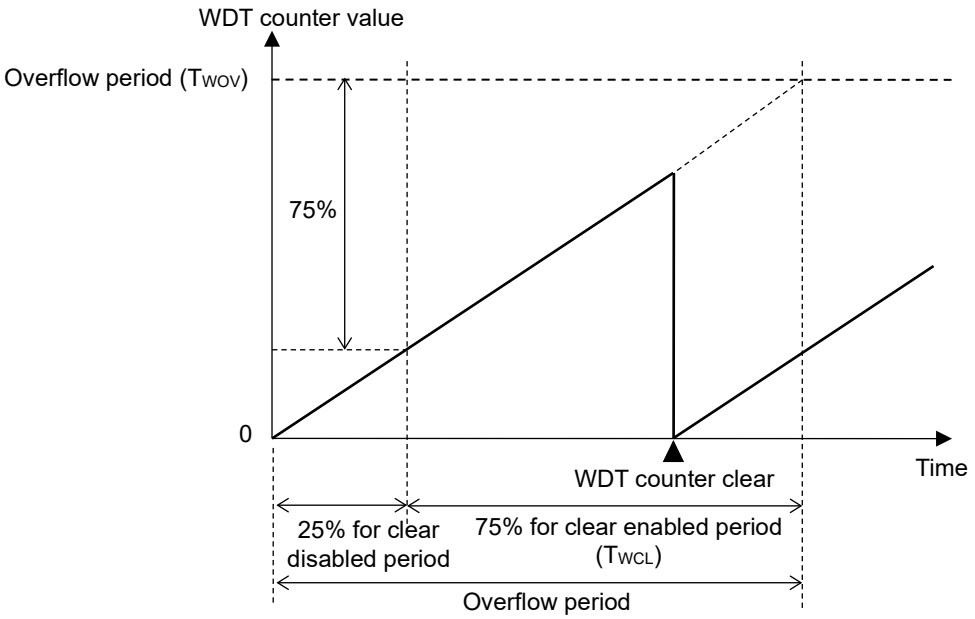


Figure 10-10 Window Function Enabled Mode 1 Operation Overview

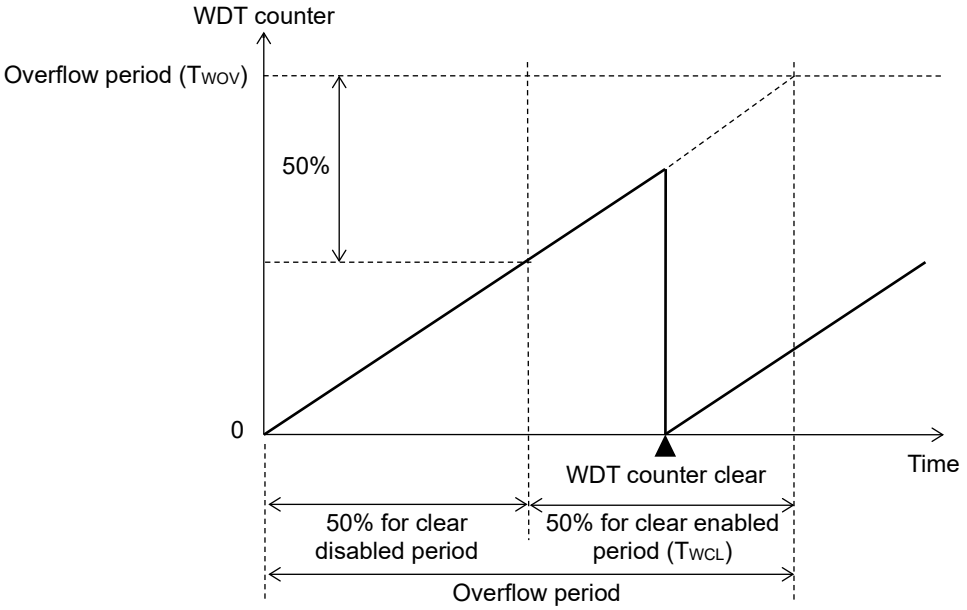


Figure 10-11 Window Function Enabled Mode 2 Operation Overview

The following table shows WDT counter clear enabled periods.
If the overflow period of WDT counter is set to 62.5 ms or less in WDT2 to 0 bits, the window function is disabled regardless of setting values of WOVF1 and WOVF0 bits.

Table 10-4 WDT Clear Enabled Period in Window Function Enabled Mode 1

WDT2	WDT1	WDT0	Overflow period (T_{WOV})*1	WDT reset generation time*1	WDT clear enabled period (T_{WCL})*1
0	0	0	Approx. 7.8 ms	Approx. 7.8 ms	≈ Overflow period
0	0	1	Approx. 15.6 ms	Approx. 15.6 ms	≈ Overflow period
0	1	0	Approx. 31.3 ms	Approx. 31.3 ms	≈ Overflow period
0	1	1	Approx. 62.5 ms	Approx. 62.5 ms	≈ Overflow period
1	0	0	Approx. 125 ms	Approx. 125 ms	≈ 75% of overflow period
1	0	1	Approx. 500 ms	Approx. 500 ms	≈ 75% of overflow period
1	1	0	Approx. 2000 ms	Approx. 2000 ms	≈ 75% of overflow period
1	1	1	Approx. 8000 ms	Approx. 8000 ms	≈ 75% of overflow period

*1: where the WDTCLK frequency is 1.024kHz(typ.) that is not included a significant error.

Table 10-5 WDT Counter Clear Enabled Period in Window Function Enabled Mode 2

WDT2	WDT1	WDT0	Overflow period (T_{WOV})*1	WDT reset generation time*1	WDT clear enabled period (T_{WCL})*1*2
0	0	0	Approx. 7.8 ms	Approx. 7.8 ms	≈ Overflow period
0	0	1	Approx. 15.6 ms	Approx. 15.6 ms	≈ Overflow period
0	1	0	Approx. 31.3 ms	Approx. 31.3 ms	≈ Overflow period
0	1	1	Approx. 62.5 ms	Approx. 62.5 ms	≈ Overflow period
1	0	0	Approx. 125 ms	Approx. 125 ms	≈ 50% of overflow period
1	0	1	Approx. 500 ms	Approx. 500 ms	≈ 50% of overflow period
1	1	0	Approx. 2000 ms	Approx. 2000 ms	≈ 50% of overflow period
1	1	1	Approx. 8000 ms	Approx. 8000 ms	≈ 50% of overflow period

*1: where the WDTCLK frequency is 1.024kHz(typ.) that is not included a significant error.

[Note]

- **When using the window function enabled mode, always define a WDT interrupt function even though no WDT interrupt occurs.**

The following shows details of operation timing in the window function enabled mode.

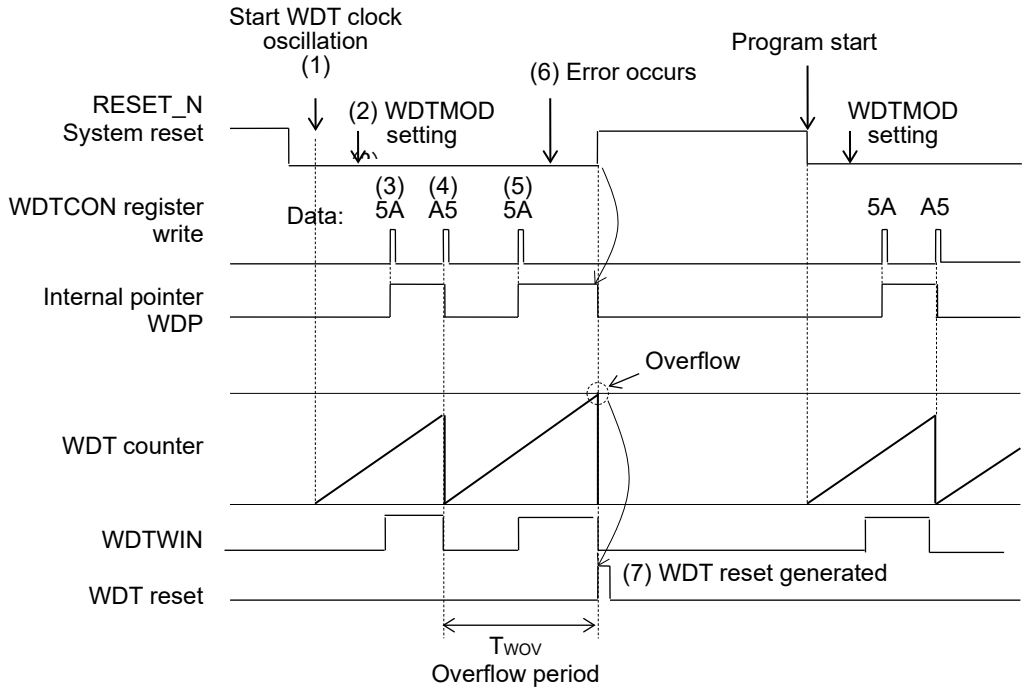


Figure 10-12 Details of Operation Timing in Window Function Enabled Mode

(1) After the system reset is released, WDT counter starts counting up.
(2) WDTMOD register is set with WDT counter overflow period (T_{WOV}) and WDT clear enabled period.
(3) "0x5A" is written to WDTCON during WDT clear enabled period. (Internal pointer WDP: 0 →1)
(4) "0xA5" is written to WDTCON register to clear WDT counter. (Internal pointer WDP: 1 →0)
(5) "0x5A" is written to WDTCON during WDT clear enabled period. (Internal pointer WDP: 0 →1)
(6) Occurrence of abnormality
(7) WDT counter overflows and WDT reset occurs. (Internal pointer WDP: 1 →0)

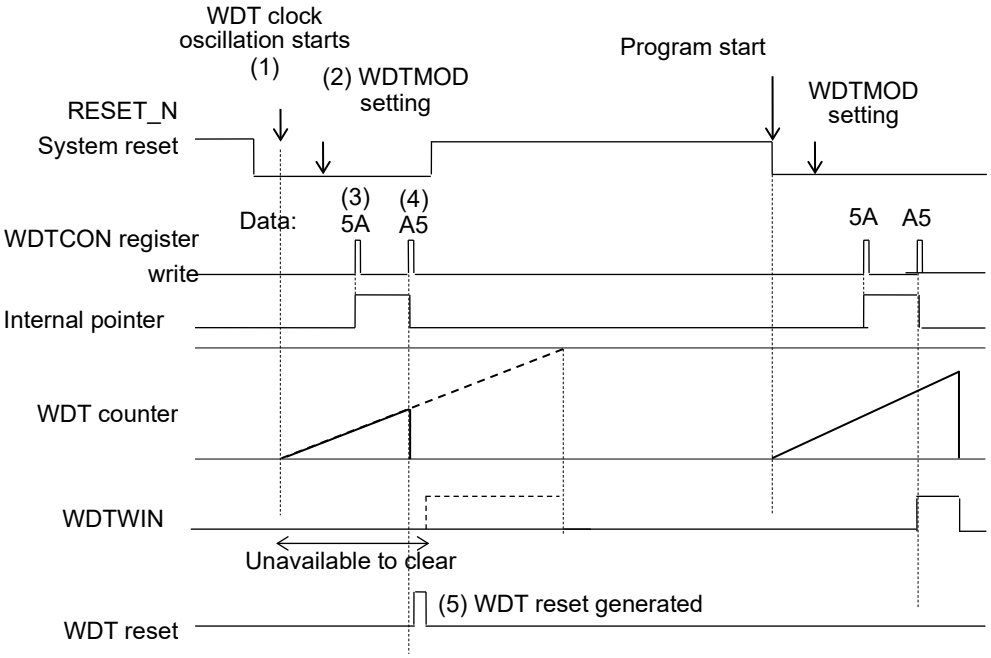


Figure 10-13 WDT invalid clear reset

(1) After the system reset is released, WDT counter starts counting up.
(2) WDTMOD register is set with WDT counter overflow period (T_{WOV}) and WDT clear enabled period.
(3) "0x5A" is written to WDTCON. (Internal pointer WDP: 0 →1)
(4) "0xA5" is written to WDTCON register to clear tWDT counter. (Internal pointer WDP: 1 →0)
(5) WDT invalid clear reset is occurred by clear processing during WDT clear disabled period.

[Note]

- **In the watchdog timer (WDT) interrupt function, as the interrupt level (ELEVEL) of the CPU program status word (PSW) becomes "2", WDT counter is unable to get cleared. Clear the WDT when ELEVEL is "0" or "1". It is recommended that WDT counter is cleared at one place in the main loop of the program as a fail-safe.**

Chapter 11 Synchronous Serial Port (SSIO)

11. Synchronous Serial Port

11.1 General Description

ML62Q2700 group has built-in communication functions for 8-bit/16-bit synchronous serial port (SSIO) and extended synchronous serial port (ESSIO).

Table 11-1 shows the number of channels.

Table 11-1 Number of SSIO and ESSIO channels

Product name	SSIO Channel No. (n)	ESSIO Channel No. (n)
ML62Q2747	0 to 2	0 to 2
ML62Q2746		
ML62Q2745		
ML62Q2737		
ML62Q2736		
ML62Q2735		
ML62Q2727		
ML62Q2726		
ML62Q2725		
ML62Q2723	0 to 1	-
ML62Q2722		
ML62Q2713		
ML62Q2712		
ML62Q2703		
ML62Q2702		

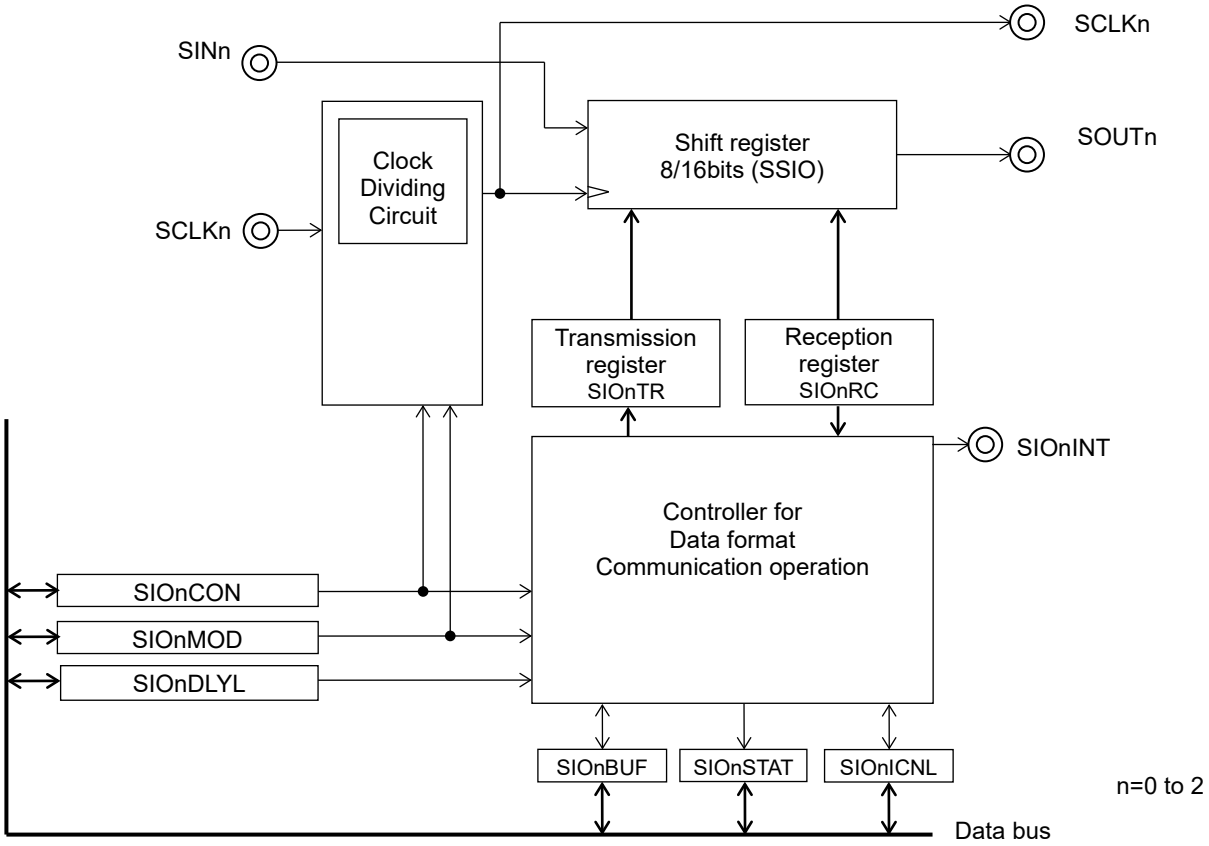
- : Unavailable

11.1.1 Features

- Selectable from Master mode / Slave mode
- Selectable from MSB first / LSB first
- Selectable from 8bit / 16bit data length
- Self-test function using the master and slave modes. For the self-test functions, see Chapter 29 "Safety Function."

11.1.2 Configuration

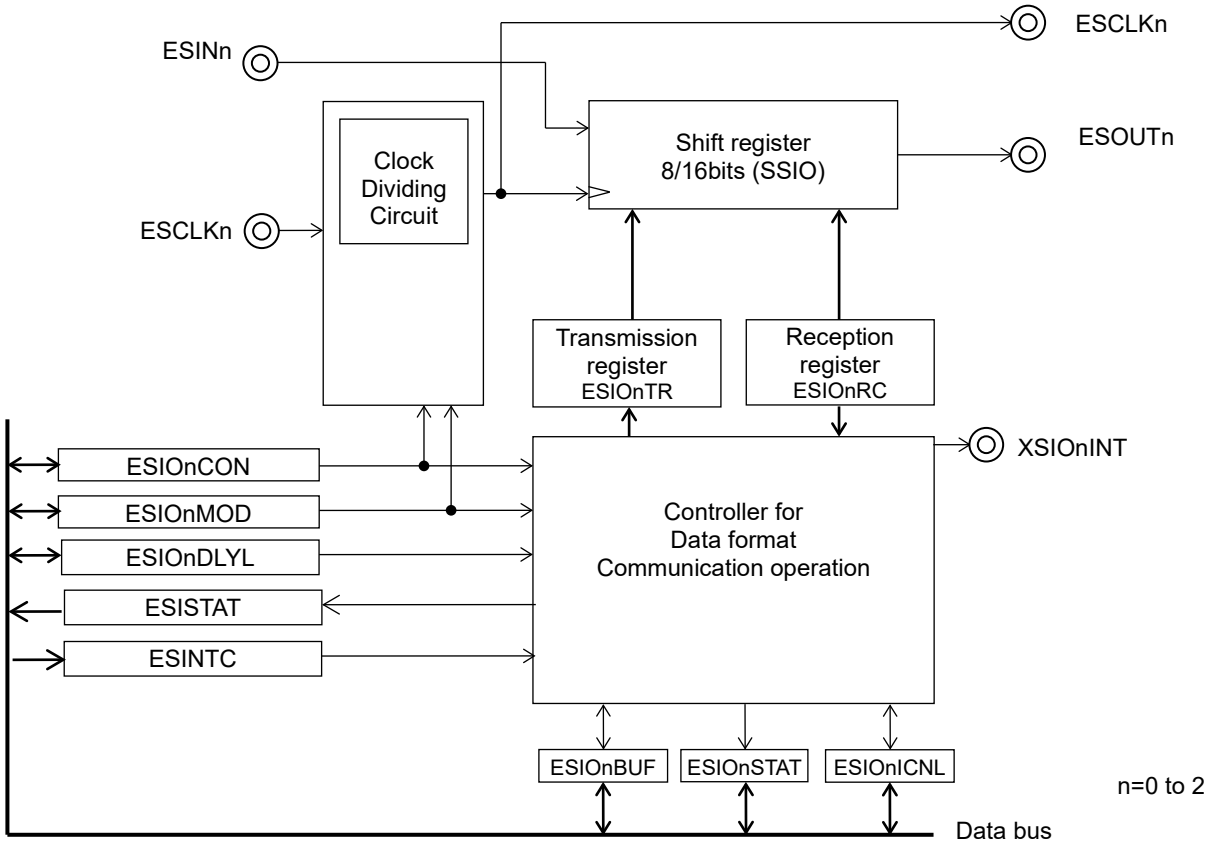
Figure 11-1(a) shows configuration of the SSIO.



SIOnBUF : Serial port n transmission/reception buffer
SIOnMOD : Serial port n mode register
SIOnCON : Serial port n control register
SIOnDLYL : Serial port n interval setting register
SIOnSTAT : Serial port n status register
SIOnICNL : Serial port n interrupt control register
SIOnINT : SSIO n interrupt

Figure 11-1(a) Configuration of SSIO

Figure 11-1(b) shows configuration of the ESSIO.



ESIOnBUF : Extended Serial port n transmission/reception buffer
ESIOnMOD : Extended Serial port n mode register
ESIOnCON : Extended Serial port n control register
ESIOnDLYL : Extended Serial port n interval setting register
ESIOnSTAT : Extended Serial port n status register
ESIOnICNL : Extended Serial port n interrupt control register
ESISTAT : Extended Serial port interrupt status register
ESINTC : Extended Serial port interrupt status clear register
ESIOnINT : Extended SSIO n interrupt

Figure 11-1(b) Configuration of ESSIO

11.1.3 List of Pins

The I/O pins of the SSIO are assigned to the shared function of the general ports.

Pin name	I/O	Description
SCLKn	I/O	Synchronous clock input/output of SSIOn
SOUTn	O	Transmission data output of SSIOn
SINn	I	Reception data input of SSIOn
ESCLKn	I/O	Synchronous clock input and output of ESSIOn
ESOUTn	O	Transmission data output of ESSIOn
ESINn	I	Receive data input of ESSIOn

(n=2 to 0)

Table 11-2 shows the register setting and the general ports used for SSIO and ESSIO.

Table 11-2 Register setting and the general ports used for SSIO and ESSIO

Channel No.	Pin name	General port		Setting register	Setting value	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702			ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725		
						48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
0	SIN0	P02	2nd Function	P0MOD2	0001_XXXX*1	●	●	●	●	●	●
		P12	2nd Function	P1MOD2	0001_XXXX*1	●	●	●	●	●	●
	SCLK0	P04	2nd Function	P0MOD4	0001_XXXX*3	●	●	●	●	●	●
		P11	2nd Function	P1MOD1	0001_XXXX*3	●	●	●	●	●	●
		P47	2nd Function	P4MOD7	0001_XXXX*3	-	●	●	●	●	●
	SOUT0	P03	2nd Function	P0MOD3	0001_XXXX*2	●	●	●	●	●	●
		P13	2nd Function	P1MOD3	0001_XXXX*2	●	●	●	●	●	●
1	SIN1	P21	2nd Function	P2MOD1	0001_XXXX*1	●	●	●	●	●	●
		P24	2nd Function	P2MOD4	0001_XXXX*1	●	●	●	●	●	●
	SCLK1	P16	2nd Function	P1MOD6	0001_XXXX*3	●	●	●	●	●	●
		P23	2nd Function	P2MOD3	0001_XXXX*3	●	●	●	●	●	●
	SOUT1	P22	2nd Function	P2MOD2	0001_XXXX*2	●	●	●	●	●	●
		P25	2nd Function	P2MOD5	0001_XXXX*2	●	●	●	●	●	●
2	SIN2	P05	2nd Function	P0MOD5	0001_XXXX*1	-	-	-	●	●	●
		P56	2nd Function	P5MOD6	0001_XXXX*1	-	-	-	-	●	●
	SCLK2	P07	2nd Function	P0MOD7	0001_XXXX*3	-	-	-	●	●	●
		PA3	2nd Function	PAMOD3	0001_XXXX*3	-	-	-	-	●	●
	SOUT2	P06	2nd Function	P0MOD6	0001_XXXX*2	-	-	-	●	●	●
		P57	2nd Function	P5MOD7	0001_XXXX*2	-	-	-	-	●	●

Channel No.	Pin name	General port		Setting register	Setting value	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702			ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725		
						48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
0	ESIN0	P64	2nd Function	P6MOD4	0001_XXXX*1	-	-	-	●	●	●
	ESCLK0	P66	2nd Function	P6MOD6	0001_XXXX*3	-	-	-	●	●	●
	ESOUT0	P65	2nd Function	P6MOD5	0001_XXXX*2	-	-	-	●	●	●
1	ESIN1	P30	2nd Function	P3MOD0	0001_XXXX*1	-	-	-	●	●	●
		P80	2nd Function	P8MOD0	0001_XXXX*1	-	-	-	-	●	●
		P93	2nd Function	P9MOD3	0001_XXXX*1	-	-	-	-	●	●
	ESCLK1	P32	2nd Function	P3MOD2	0001_XXXX*3	-	-	-	●	●	●
		P82	2nd Function	P8MOD2	0001_XXXX*3	-	-	-	-	●	●
		P95	2nd Function	P9MOD5	0001_XXXX*3	-	-	-	-	●	●
	ESOUT1	P31	2nd Function	P3MOD1	0001_XXXX*2	-	-	-	●	●	●
		P81	2nd Function	P8MOD1	0001_XXXX*2	-	-	-	-	●	●
		P94	2nd Function	P9MOD4	0001_XXXX*2	-	-	-	-	●	●
2	ESIN2	P60	2nd Function	P6MOD0	0001_XXXX*1	-	-	-	●	●	●
		PB2	2nd Function	PBMOD2	0001_XXXX*1	-	-	-	-	●	●
	ESCLK2	P62	2nd Function	P6MOD2	0001_XXXX*3	-	-	-	●	●	●
		PB4	2nd Function	PBMOD4	0001_XXXX*3	-	-	-	-	●	●
	ESOUT2	P61	2nd Function	P6MOD1	0001_XXXX*2	-	-	-	●	●	●
		PB3	2nd Function	PBMOD3	0001_XXXX*2	-	-	-	-	●	●

●:available -:Not available

*1 : “XXXX” determines the condition of the port input

XXXX	Condition of the port input
0001	Input (without an internal pull-up resistor)
0101	Input (with an internal pull-up resistor)

*2 : “XXXX” determines the condition of the port output

XXXX	Condition of the port output
0010	CMOS output
1010	Nch open drain output (without the pull-up)
1111	Nch open drain output (with the pull-up)

*3 : XXXX determines the condition of the port input/output
In the master mode, see to *2 for use as output.
In the slave mode, see to *1 for use as input.

11.1.4 Combination of SSIO port

SINn, SOUTn, SCLKn, ESINn, ESOUTn, and ESCLKn are assign to several functions of each general ports. So the following combinations are required in use.

Table 11-3 Combination of the SSIO port and ESSIO port

combination	Peripheral circuits	Channel No.	Input/output pin			ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702			ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725		
			SIN /ESIN*	SOUT /ESOUT*	SCLK /ESCLK*	48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
1	SSIO	0	P02	P03	P04	●	●	●	●	●	●
2			P02	P03	P47	-	●	●	●	●	●
3			P12	P13	P11	●	●	●	●	●	●
4		1	P21	P22	P16	●	●	●	●	●	●
5			P24	P25	P23	●	●	●	●	●	●
6			P21	P22	P23	●	●	●	●	●	●
7		2	P05	P06	P07	-	-	-	●	●	●
8			P56	P57	PA3	-	-	-	-	●	●
9	ESSIO	0	P64	P65	P66	-	-	-	●	●	●
10		1	P30	P31	P32	-	-	-	●	●	●
11			P80	P81	P82	-	-	-	-	●	●
12			P93	P94	P95	-	-	-	-	●	●
13		2	P60	P61	P62	-	-	-	●	●	●
14			PB2	PB3	PB4	-	-	-	-	●	●

*: n=channel No.
●: available　－: Not available

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF500	Serial port 0 transmission/reception buffer	SIO0BUFL	SIO0BUF	R/W	8/16	0x00
0xF501		SIO0BUFH		R/W	8	0x00
0xF502	Serial port 0 status register	SIO0STATL	SIO0STAT	R	8/16	0x00
0xF503		SIO0STATH		W	8	0x00
0xF504	Serial port 0 control register	SIO0CONL	SIO0CON	R/W	8/16	0x00
0xF505		SIO0CONH		R/W	8	0x00
0xF506	Serial port 0 mode register	SIO0MODL	SIO0MOD	R/W	8/16	0x00
0xF507		SIO0MODH		R/W	8	0x00
0xF508	Serial port 0 interval setting register	SIO0DLYL	-	R/W	8	0x00
0xF509	Reserved register	-	-	-	-	-
0xF50A	Serial port 0 interrupt control register	SIO0ICNL	-	R/W	8	0x00
0xF50B to 0xF50F	Reserved register	-	-	-	-	-
0xF510	Serial port 1 transmission/reception buffer	SIO1BUFL	SIO1BUF	R/W	8/16	0x00
0xF511		SIO1BUFH		R/W	8	0x00
0xF512	Serial port 1 status register	SIO1STATL	SIO1STAT	R	8/16	0x00
0xF513		SIO1STATH		W	8	0x00
0xF514	Serial port 1 control register	SIO1CONL	SIO1CON	R/W	8/16	0x00
0xF515		SIO1CONH		R/W	8	0x00
0xF516	Serial port 1 mode register	SIO1MODL	SIO1MOD	R/W	8/16	0x00
0xF517		SIO1MODH		R/W	8	0x00
0xF518	Serial port 1 interval setting register	SIO1DLYL	-	R/W	8	0x00
0xF519	Reserved register	-	-	-	-	-
0xF51A	Serial port 1 interrupt control register	SIO1ICNL	-	R/W	8	0x00
0xF51B to 0xF51F	Reserved register	-	-	-	-	-
0xF520	Serial port 2 transmission/reception buffer	SIO2BUFL	SIO2BUF	R/W	8/16	0x00
0xF521		SIO2BUFH		R/W	8	0x00
0xF522	Serial port 2 status register	SIO2STATL	SIO2STAT	R	8/16	0x00
0xF523		SIO2STATH		W	8	0x00
0xF524	Serial port 2 control register	SIO2CONL	SIO2CON	R/W	8/16	0x00
0xF525		SIO2CONH		R/W	8	0x00
0xF526	Serial port 2 mode register	SIO2MODL	SIO2MOD	R/W	8/16	0x00
0xF527		SIO2MODH		R/W	8	0x00
0xF528	Serial port 2 interval setting register	SIO2DLYL	-	R/W	8	0x00
0xF529	Reserved register	-	-	-	-	-
0xF52A	Serial port 2 interrupt control register	SIO2ICNL	-	R/W	8	0x00
0xF52B to 0xF52F	Reserved register	-	-	-	-	-
0xF530	Extended Serial port 0 transmission/reception buffer	ESIO0BUFL	ESIO0BUF	R/W	8/16	0x00
0xF531		ESIO0BUFH		R/W	8	0x00
0xF532	Extended Serial port 0 status register	ESIO0STATL	ESIO0STAT	R	8/16	0x00
0xF533		ESIO0STATH		W	8	0x00
0xF534	Extended Serial port 0 control register	ESIO0CONL	ESIO0CON	R/W	8/16	0x00
0xF535		ESIO0CONH		R/W	8	0x00
0xF536	Extended Serial port 0 mode register	ESIO0MODL	ESIO0MOD	R/W	8/16	0x00
0xF537		ESIO0MODH		R/W	8	0x00
0xF538	Extended Serial port 0 interval setting register	ESIO0DLYL	-	R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF539	Reserved register	-	-	-	-	-
0xF53A	Extended Serial port 0 interrupt control register	ESIO0ICNL	—	R/W	8	0x00
0xF53B to 0xF53F	Reserved register	-	-	-	-	-
0xF540	Extended Serial port 1 transmission/reception buffer	ESIO1BUFL	ESIO1BUF	R/W	8/16	0x00
0xF541		ESIO1BUFH		R/W	8	0x00
0xF542	Extended Serial port 1 status register	ESIO1STATL	ESIO1STAT	R	8/16	0x00
0xF543		ESIO1STATH		W	8	0x00
0xF544	Extended Serial port 1 control register	ESIO1CONL	ESIO1CON	R/W	8/16	0x00
0xF545		ESIO1CONH		R/W	8	0x00
0xF546	Extended Serial port 1 mode register	ESIO1MODL	ESIO1MOD	R/W	8/16	0x00
0xF547		ESIO1MODH		R/W	8	0x00
0xF548	Extended Serial port 1 interval setting register	ESIO1DLYL	-	R/W	8	0x00
0xF549	Reserved register	-	-	-	-	-
0xF54A	Extended Serial port 1 interrupt control register	ESIO1ICNL	-	R/W	8	0x00
0xF54B to 0xF54F	Reserved register	-	-	-	-	-
0xF550	Extended Serial port 2 transmission/reception buffer	ESIO2BUFL	ESIO2BUF	R/W	8/16	0x00
0xF551		ESIO2BUFH		R/W	8	0x00
0xF552	Extended Serial port 2 status register	ESIO2STATL	ESIO2STAT	R	8/16	0x00
0xF553		ESIO2STATH		W	8	0x00
0xF554	Extended Serial port 2 control register	ESIO2CONL	ESIO2CON	R/W	8/16	0x00
0xF555		ESIO2CONH		R/W	8	0x00
0xF556	Extended Serial port 2 mode register	ESIO2MODL	ESIO2MOD	R/W	8/16	0x00
0xF557		ESIO2MODH		R/W	8	0x00
0xF558	Extended Serial port 2 interval setting register	ESIO2DLYL	-	R/W	8	0x00
0xF559	Reserved register	-	-	-	-	-
0xF55A	Extended Serial port 2 interrupt control register	ESIO2ICNL	-	R/W	8	0x00
0xF55B to 0xF55F	Reserved register	-	-	-	-	-
0xF5E0	Extended Serial Port Interrupt Status Register	ESISTAT	-	R	8	0x00
0xF5E1	Reserved register	-	-	-	-	-
0xF5E2	Extended Serial Port Interrupt Status Clear Register	ESINTCL	ESINTC	W	8/16	0x00
0xF5E3		ESINTCH		W	8	0x00

11.2.2 Serial Port n Transmission/Reception Buffer (SIOnBUF)

SIOnBUF is a SFR to store transmission/ reception data.

Address : 0xF500 (SIO0BUFL/SIO0BUF), 0xF501 (SIO0BUFH),
0xF510 (SIO1BUFL/SIO1BUF), 0xF511 (SIO1BUFH),
0xF520 (SIO2BUFL/SIO2BUF), 0xF521 (IO2BUFH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SIOnBUF															
Byte	SIOnBUFH								SIOnBUFL							
Bit	SnB15	SnB14	SnB13	SnB12	SnB11	SnB10	SnB9	SnB8	SnB7	SnB6	SnB5	SnB4	SnB3	SnB2	SnB1	SnB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Writing to SIOnBUF register writes data to the transmit register (SIOnTR).
When SIOnBUF register is read, the contents of the receive register (SIOnRC) are read.
When SnEN bit of SIOnCON is "1" and SnFUL bit of SIOnSTATL is "0", in 8-bit mode,
Start sending and receiving with SIOnBUFL write. SIOnBUFH is not used.
When SnEN bit of SIOnCON is "1" and SnFUL bit of SIOnSTATL is "0", in 16-bit mode,
Start transferring and receiving by writing to SIOnBUFH.

The transmission data is 0xFF/0xFFFF when transmission data buffer is empty in the slave mode.

Bit No.	Bit symbol name	Description
15 to 8	SnB15 to SnB8	Transmission/Reception data buffer for the upper side 8 bit. If writing data into this register, the data is stored into the transmission register (SIOnTR). If reading data, the data in the reception data (SIOnRC) is read out. These bits are unused and not writable in an 8-bit mode.
7 to 0	SnB7 to SnB0	Transmission/Reception data buffer for the lower side 8 bit. If writing data into this register, the data is stored into the transmission register (SUnTR). If reading data, the data in the reception data (SUnRC) is read out.

11.2.3 Serial Port n Status Register (SIOnSTAT)

SIOnSTAT is a SFR to indicate the state of the transmission/reception operation.

Address : 0xF502 (SIO0STATL/SIO0STAT) ,0xF502 (SIO0STATH),
0xF512 (SIO1STATL/SIO1STAT) ,0xF512 (SIO1STATH),
0xF522 (SIO2STATL/SIO2STAT) ,0xF522 (SIO2STATH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SIOnSTAT															
Byte	SIOnSTATH								SIOnSTATL							
Bit	-	-	-	-	-	SnTOC	SnROC	SnTUC	-	SnRFUL	-	SnTXF	SnFUL	SnTOER	SnROER	SnTUER
R/W	R	R	R	R	R	W	W	W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 11	-	Reserved bits
10	SnTOC	Clear SnTOER bit of SIOnSTATL. Writing “0”: Invalid Writing “1”: clear SnTOER bit.
9	SnROC	Clear SnROER bit of SIOnSTATL. Writing “0”: Invalid Writing “1”: clear SnROER bit.
8	SnTUC	Clear SnTUER bit of SIOnSTATL. Writing “0”: Invalid Writing “1”: clear SnTUER bit.
7	-	Reserved bit
6	SnRFUL	Indicate a state of reception buffer. SnRFUL bit becomes "1" when there is data in the receive buffer. When SIOnBUF is read, it becomes "0". 0: No data in Reception buffer. (Initial value) 1: Data in Reception buffer. When the next data is received with SnRFUL bit set to "1", the receive overrun error (SnROER) becomes "1". Incoming data will be overwritten.
5	-	Reserved bits
4	SnTXF	Indicate communication state. 0: communication is stop and idle state. (Initial value) 1: communication is active; transmitting / receiving.
3	SnFUL	Indicate state of the transmission buffer (SIOnBUF). In 8-bit mode, writing data to SIOnBUFL register sets "1". In 16-bit mode, writing data to SIOnBUFH register sets "1". When start transferring the written data, it becomes "0". In master mode, data is transmitted when the SnFUL bit is "1" and SnEN bit of SIOnCON register is "1". If data is written to SIOnBUF register with SnFUL bit set to "1", the transmit overrun error (SnTOER) becomes "1". The value of SIOnBUF register is overwritten. It is reset to "0" by writing "1" to SnTFC bit of SIOnCON register. 0: No data in Transmission buffer (initial value) 1: Data in Transmission buffer
2	SnTOER	Indicate a transmission overrun error. If writing a data to SIOnBUF register when SnFUL bit is “1”, SnTOER bit is set to “1”. To reset SnTOER bit, write “1” to SnTOC bit. 0: There was no transmission overrun error (Initial value) 1: There was a transmission overrun error
1	SnROER	Indicate a reception overrun error. If receiving the next data before reading the data in SIOnBUF register. To reset SnROER bit, write “1” to SnROC bit. 0: There was no reception overrun error (Initial value) 1: There was a reception overrun error

Bit no.	Bit symbol name	Description
0	SnTUER	Indicate a transmission underrun error. This bit is set to “1” by transmitting start when the SnFUL bit is “0” and SnEN bit is “1”, where Transmitting data is 0xFF/0xFFFF. To reset SnTUER bit, write “1” to SnTUC bit. 0: There was no transmission underrun error (Initial value) 1: There was a transmission underrun error

11.2.4 Serial Port n Control Register (SIOnCON)

SIOnCON is a SFR to control the SSIO.

Address : 0xF504 (SIO0CONL/SIO0CON), 0xF505 (SIO0CONH),
0xF514 (SIO1CONL/SIO1CON), 0xF515 (SIO1CONH),
0xF524 (SIO2CONL/SIO2CON), 0xF525 (SIO2CONH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SIOnCON															
Byte	SIOnCONH								SIOnCONL							
Bit	-	-	-	SnTFC	-	-	-	-	-	-	-	-	-	-	-	SnEN
R/W	R	R	R	W	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 13	-	Reserved bits
12	SnTFC	When "1" is written, the transmission register (SIOnTR) is cleared (initialized to 0xFFFF). It also clears (initializes to 0) the SnFUL bit of the SIOnSTAT register. Writing “0”: Invalid Writing “1”: clear the SnFUL bit and initialize the SIOnTR.
11 to 1	-	Reserved bits
0	SnEN	Enable serial communication. 0: Disabled (Initial value) 1: Enabled

11.2.5 Serial Port n Mode Register (SIOnMOD)

SIOnMOD is a SFR to set a mode of the SSIO n.

Address : 0xF506 (SIO0MODL/SIO0MOD), 0xF507 (SIO0MODH),
0xF516 (SIO1MODL/SIO1MOD), 0xF517 (SIO1MODH),
0xF526 (SIO2MODL/SIO2MOD), 0xF527 (SIO2MODH)

Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SIOnMOD															
Byte	SIOnMODH								SIOnMODL							
Bit	-	SnNEG	SnCKT	-	SnCK3	SnCK2	SnCK1	SnCK0	-	-	-	-	SnLG	-	-	SnDIR
R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	-	Reserved bit
14	SnNEG	Select the edge of sampling clock. 0: Positive edge (Initial value) 1: Negative edge
13	SnCKT	Select the phase of transfer clock. 0: Clock type 0: (Initial value) 1st edge is used to shift a data, 2nd edge is used to sample a data. Repeat thereafter. 1: Do not use
12	-	Reserved bit
11 to 8	SnCK3 to SnCK0	Select the transfer clock. When the internal clock is selected as the transfer clock, it enters master mode, and when the external clock is selected, it enters slave mode. In the master mode, set these bits to 4MHz or slower. In the slave mode, maximum frequency of external clock is within the spec specified in the data sheet and also is 1/4 frequency of the system clock. 0000: 1/1 SYSCLK (Initial value) 0001: 1/2 SYSCLK 0010: 1/4 SYSCLK 0011: 1/8 SYSCLK 0100: 1/16 SYSCLK 0101: 1/32 SYSCLK 0110: 1/64 SYSCLK 0111: 1/128 SYSCLK 1000: External clock (Slave mode) Others: External clock (Slave mode)
7 to 4	-	Reserved bits
3	SnLG	Select the bit length of the transmission/reception data. 0: 8-bit length (Initial value) 1: 16-bit length
2 to 1	-	Reserved bits
0	SnDIR	Select the data direction. 0: LSB first (Initial value) 1: MSB first

[Note]

- **Set the SIOnMOD register while communication is stopped (SnEN=0). If it is rewritten during communication, data may not be transmitted or received normally.**

11.2.6 Serial Port n Interval Setting Register (SIOnDLYL)

SIOnDLYL is a SFR to set the frame interval of serial communication. It is used for the slave device to wait for a data reception process when continuously transmitting the serial data.
This is available in the master mode.

Address : 0xF508 (SIO0DLYL)
0xF518 (SIO1DLYL),
0xF528 (SIO2DLYL)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SIOnDLYL							
Bit	-	-	-	-	-	-	-	-	SnDLY7	SnDLY6	SnDLY5	SnDLY4	SnDLY3	SnDLY2	SnDLY1	SnDLY0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 0	SIOnDLY7 to SIOnDLY0	Set the frame interval. 0x00 : no interval (Initial value) Others : frame interval = (clock period of SCLKn) × (SIOnDLYL value +1)

11.2.7 Serial Port n Interrupt Control Register (SIOnICNL)

SIOnICNL is a SFR to control interrupt of SSIO.

Address : 0xF50A (SIO0ICNL)
0xF51A (SIO1ICNL),
0xF52A (SIO2ICNL)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SIOnICNL							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	SnRIE	SnFIE	SnTIE
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 3	-	Reserved bits
2	SnRIE	Select enable or disable of transfer end interrupt. 0: Disabled (Initial value) 1: Enabled
1	SnFIE	Select enable or disable of the transmission/reception completion interrupt. This interrupt occurs when transmission/reception is finished with transmission buffer is empty (SnFUL="0"). 0: Disabled (Initial value) 1: Enabled
0	SnTIE	Select enable/disable the transmission buffer empty interrupt. This interrupt occurs when transmission buffer becomes empty (SnFUL="0"). 0: Disabled (Initial value) 1: Enabled

11.2.8 Extended Serial Port n Transmission/Reception Buffer (ESIOnBUF)

ESIOnBUF is a SFR to store transmission/ reception data.

Address : 0xF530 (ESIO0BUFL/ESIO0BUF), 0xF531 (ESIO0BUFH),
0xF540 (ESIO1BUFL/ESIO1BUF), 0xF541 (ESIO1BUFH),
0xF550 (ESIO2BUFL/ESIO2BUF), 0xF551 (ESIO2BUFH)

Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ESIOnBUF															
Byte	ESIOnBUFH								ESIOnBUFL							
Bit	ESnB 15	ESnB 14	ESnB 13	ESnB 12	ESnB 11	ESnB 10	ESnB 9	ESnB 8	ESnB 7	ESnB 6	ESnB 5	ESnB 4	ESnB 3	ESnB 2	ESnB 1	ESnB 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Writing to ESIOnBUF register writes data to the transmit register (ESIOnTR).
When ESIOnBUF register is read, the contents of the receive register (ESIOnRC) are read.
When ESnEN bit of ESIOnCON is "1" and ESnFUL bit of ESIOnSTATL is "0", in 8-bit mode,
Start sending and receiving with ESIOnBUFL write. ESIOnBUFH is not used.
When ESnEN bit of ESIOnCON is "1" and ESnFUL bit of ESIOnSTATL is "0", in 16-bit mode,
Start transferring and receiving by writing to ESIOnBUFH.

The transmission data is 0xFF/0xFFFF when transmission data buffer is empty in the slave mode.

Bit No.	Bit symbol name	Description
15 to 8	ESnB15 to ESnB8	Transmission/Reception data buffer for the upper side 8 bit. If writing data into this register, the data is stored into the transmission register (ESIOnTR). If reading data, the data in the reception data (ESIOnRC) is read out. These bits are unused and not writable in an 8-bit mode.
7 to 0	ESnB7 to ESnB0	Transmission/Reception data buffer for the lower side 8 bit. If writing data into this register, the data is stored into the transmission register (ESUnTR). If reading data, the data in the reception data (ESUnRC) is read out.

11.2.9 Extended Serial Port n Status Register (ESIOnSTAT)

ESIOnSTAT is a SFR to indicate the state of the transmission/reception operation.

Address : 0xF532 (ESIO0STATL/ESIO0STAT), 0xF532 (ESIO0STATH),
0xF542 (ESIO1STATL/ESIO1STAT), 0xF542 (ESIO1STATH),
0xF552 (ESIO2STATL/ESIO2STAT), 0xF552 (ESIO2STATH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ESIOnSTAT															
Byte	ESIOnSTATH								ESIOnSTATL							
Bit	–	–	–	–	–	ESnTOC	ESnROC	ESnTUC	–	ESnRFUL	–	ESnTXF	ESnFUL	ESnTOER	ESnROER	ESnTUER
R/W	R	R	R	R	R	W	W	W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 11	-	Reserved bits
10	ESnTOC	Clear ESnTOER bit of ESIOnSTATL. Writing “0”: Invalid Writing “1”: clear ESnTOER bit.
9	ESnROC	Clear ESnROER bit of ESIOnSTATL. Writing “0”: Invalid Writing “1”: clear ESnROER bit.
8	ESnTUC	Clear ESnTUER bit of ESIOnSTATL. Writing “0”: Invalid Writing “1”: clear ESnTUER bit.
7	-	Reserved bits
6	ESnRFUL	Indicate a state of reception buffer. ESnRFUL bit becomes "1" when there is data in the receive buffer. When ESIOnBUF is read, it becomes "0". 0: No data in Reception buffe. (Initial value) 1: Data in Reception buffer. When the next data is received with ESnRFUL bit set to "1", the receive overrun error (ESnROER) becomes "1". Incoming data will be overwritten.
5	-	Reserved bits
4	ESnTXF	Indicate communication state. 0: communication is stop and idle state. (Initial value) 1: communication is active; transmitting / receiving.
3	ESnFUL	Indicate state of the transmission buffer (ESIOnBUF). In 8-bit mode, writing data to ESIOnBUFL register sets "1". In 16-bit mode, writing data to ESIOnBUFH register sets "1". When start transferring the written data, it becomes "0". In master mode, data is transmitted when the ESnFUL bit is "1" and the ESnEN bit of the ESIOnCON register is "1". If data is written to ESIOnBUF register with ESnFUL bit set to "1", the transmit overrun error (ESnTOER) becomes "1". The value of ESIOnBUF register is overwritten. It is reset to "0" by writing "1" to ESnTFC bit of ESIOnCON register. 0: No data in Transmission buffer (initial value) 1: Data in Transmission buffer
2	ESnTOER	Indicate a transmission overrun error. If writing a data to ESIOnBUF register when ESnFUL bit is “1”, ESnTOER bit is set to “1”. To reset ESnTOER bit, write “1” to ESnTOC bit. 0: There was no transmission overrun error (Initial value) 1: There was a transmission overrun error
1	ESnROER	Indicate a reception overrun error. If receiving the next data before reading the data in ESIOnBUF register. To reset ESnROER bit, write “1” to ESnROC bit. 0: There was no reception overrun error (Initial value) 1: There was a reception overrun error

Bit no.	Bit symbol name	Description
0	ESnTUER	Indicate a transmission underrun error. This bit is set to “1” by transmitting start when ESnFUL bit is “0” and ESnEN bit is “1”, where Transmitting data is 0xFF/0xFFFF. To reset the ESnTUER bit, write “1” to ESnTUC bit. 0: There was no transmission underrun error (Initial value) 1: There was a transmission underrun error

11.2.10 Extended Serial Port n Control Register (ESIOnCON)

ESIOnCON is a SFR to control the SSIO.

Address : 0xF534 (ESIO0CONL/ESIO0CON), 0xF535 (ESIO0CONH),
0xF544 (ESIO1CONL/ESIO1CON), 0xF545 (ESIO1CONH),
0xF554 (ESIO2CONL/ESIO2CON), 0xF555 (ESIO2CONH)

Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ESIOnCON															
Byte	ESIOnCONH								ESIOnCONL							
Bit	-	-	-	ESnTFC	-	-	-	-	-	-	-	-	-	-	-	ESnEN
R/W	R	R	R	W	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 13	-	Reserved bits
12	ESnTFC	When "1" is written, the transmission register (ESIOnTR) is cleared (initialized to 0xFFFF). It also clears (initializes to 0) the SnFUL bit of ESIOnSTAT register. Writing “0”: Invalid Writing “1”: clear the SnFUL bit and initialize ESIOnTR.
11 to 1	-	Reserved bits
0	ESnEN	Enable serial communication. 0: Disabled (Initial value) 1: Enabled

11.2.11 Extended Serial Port n Mode Register (ESIOnMOD)

ESIOnMOD is a SFR to set a mode of the ESSIO n.

Address : 0xF536 (ESIO0MODL/ESIO0MOD), 0xF537 (ESIO0MODH),
0xF546 (ESIO1MODL/ESIO1MOD), 0xF547 (ESIO1MODH),
0xF556 (ESIO2MODL/ESIO2MOD), 0xF557 (ESIO2MODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ESIOnMOD															
Byte	ESIOnMODH								ESIOnMODL							
Bit	–	ESnNEG	ESnCKT	–	ESnCK3	ESnCK2	ESnCK1	ESnCK0	–	–	–	–	ESnLG	–	–	ESnDIR
R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	-	Reserved bit
14	ESnNEG	Select the edge of sampling clock. 0: Positive edge (Initial value) 1: Negative edge
13	ESnCKT	Select the phase of transfer clock. 0: Clock type 0: (Initial value) 1st edge is used to shift a data, 2nd edge is used to sample a data. Repeat thereafter. 1: Do not use
12	-	Reserved bit
11 to 8	ESnCK3 to ESnCK0	Select the transfer clock. When the internal clock is selected as the transfer clock, it enters master mode, and when the external clock is selected, it enters slave mode. In the master mode, set these bits to 4MHz or slower. In the slave mode, maximum frequency of external clock is within the spec specified in the data sheet and also is 1/4 frequency of the system clock. 0000: 1/1 SYSCLK (Initial value) 0001: 1/2 SYSCLK 0010: 1/4 SYSCLK 0011: 1/8 SYSCLK 0100: 1/16 SYSCLK 0101: 1/32 SYSCLK 0110: 1/64 SYSCLK 0111: 1/128 SYSCLK 1000: External clock (Slave mode) Others: External clock (Slave mode)
7 to 4	-	Reserved bits
3	ESnLG	Select the bit length of the transmission/reception data. 0: 8-bit length (Initial value) 1: 16-bit length
2 to 1	-	Reserved bits
0	ESnDIR	Select the data direction. 0: LSB first (Initial value) 1: MSB first

[Note]

- **Set ESIOnMOD register while communication is stopped (ESnEN=0). If it is rewritten during communication, data may not be transmitted or received normally.**

11.2.12 Extended Serial Port n Interval Setting Register (ESIOnDLYL)

ESIOnDLYL is a SFR to set the frame interval of serial communication. It is used for the slave device to wait for a data reception process when continuously transmitting the serial data.
This is available in the master mode.

Address : 0xF538 (ESIO0DLYL)
0xF548 (ESIO1DLYL),
0xF558 (ESIO2DLYL)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								ESIOnDLYL							
Bit	-	-	-	-	-	-	-	-	ESnDLY7	ESnDLY6	ESnDLY5	ESnDLY4	ESnDLY3	ESnDLY2	ESnDLY1	ESnDLY0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 0	ESIOnDLY7 to ESIOnDLY0	Set the frame interval. 0x00 : no interval (Initial value) Others : frame interval = (clock period of ESCLKn) × (ESIOnDLYL value +1)

11.2.13 Extended Serial Port n Interrupt Control Register (ESIOnICNL)

ESIOnICNL is a SFR to control interrupt of SSIO.

Address : 0xF53A (ESIO0ICNL)
0xF54A (ESIO1ICNL),
0xF55A (ESIO2ICNL)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								ESIOnICNL							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	ESnRIE	ESnFIE	ESnTIE
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15 to 3	-	Reserved bits
2	ESnRIE	Select enable or disable of transfer end interrupt. 0: Disabled (Initial value) 1: Enabled
1	ESnFIE	Select enable or disable of the transmission/reception completion interrupt. This interrupt occurs when transmission/reception is finished with transmission buffer is empty (ESnFUL="0"). 0: Disabled (Initial value) 1: Enabled
0	ESnTIE	Select enable/disable the transmission buffer empty interrupt. This interrupt occurs when transmission buffer becomes empty (ESnFUL="0"). 0: Disabled (Initial value) 1: Enabled

11.2.14 Extended Serial port Interrupt Status Register (ESISTAT)

ESISTAT is a SFR to indicate extended serial port interrupt status.
ESISTAT is a read only register.
ESI2S to ESI0S bits are initialized to “0” by writing "1" to the same bit in ESINTC register in addition to the reset function.

Address : 0xF5E0（ESISTAT）
Access : R
Access size : 8bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	—															
Byte	—								ESISTAT							
Bit	—	—	—	—	—	—	—	—	—	—	—	—	—	ESI2S	ESI1S	ESI0S
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 3	-	Reserved bits
2	ESI2S	Indicate Extended Serial port 2 interrupt (ESIO2INT) status. 0: No interrupt occurs (initial value) 1: interrupt occur
1	ESI1S	Indicate Extended Serial port 1 interrupt (ESIO1INT) status. 0: No interrupt occurs (initial value) 1: interrupt occur
0	ESI0S	Indicate Extended Serial port 0 interrupt (ESIO0INT) status. 0: No interrupt occurs (initial value) 1: interrupt occur

11.2.15 Extended Serial port interrupt clear register (ESINTC)

ESINTC is a SFR to clear extended serial port interrupt status.
Writing "1" to ESI2C to ESI0C bits clears the interrupt status of the same bit in ESISTAT register.
Readout 0x0000 always.

Address : 0xF5E2(ESINTCL/ESINTC), 0xF5E3(ESINTCH)
Access : W
Access size : 8bit/16bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ESINTC															
Byte	ESINTCH								ESINTCL							
Bit	ESIR	—	—	—	—	—	—	—	—	—	—	—	—	ESI2C	ESI1C	ESI0C
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	ESIR	Request extended serial port interrupt. Write "1" before the interrupt routine completes and after writing to the IRQ01/IRQ23/IRQ45/IRQ67 registers. Writing "0": invalid Writing "1": If there is an outstanding interrupt factor, issue the interrupt request again.
14 to 3	—	Reserved bit
2	ESI2C	Clear extended serial port 2 interrupt (ESIO2INT) status bit (ESI2S). Writing "0": invalid Writing "1": clear interrupt status
1	ESI1C	Clear extended serial port 1 interrupt (ESIO1INT) status bit (ESI1S). Writing "0": invalid Writing "1": clear interrupt status
0	ESI0C	Clear extended serial port 0 interrupt (ESIO0INT) status bit (ESI0S). Writing "0": invalid Writing "1": clear interrupt status

[Note]
- **Do not set ESIR bit and "ESI2C to ESI0C" bits simultaneously.**
- **When the CPU writes to the interrupt request register (IRQ01, IRQ23, IRQ45, IRQ67) at the timing of the extended external interrupt occurs, the extended serial port interrupt status register (ESISTAT) is set, but the interrupt request bit of the extended serial port interrupt (bit 2 of the QESIO = IRQ67 register) is not set and the CPU may not be notified of the interrupt.**
- **When writing to IRQ01, IRQ23, IRQ45, and IRQ67, set the ESIR bit of ESINTC to 1 after writing and re-request the interrupt.**
- **Refer to the Fig 11-9 for Extended serial port interrupt setting flow.**

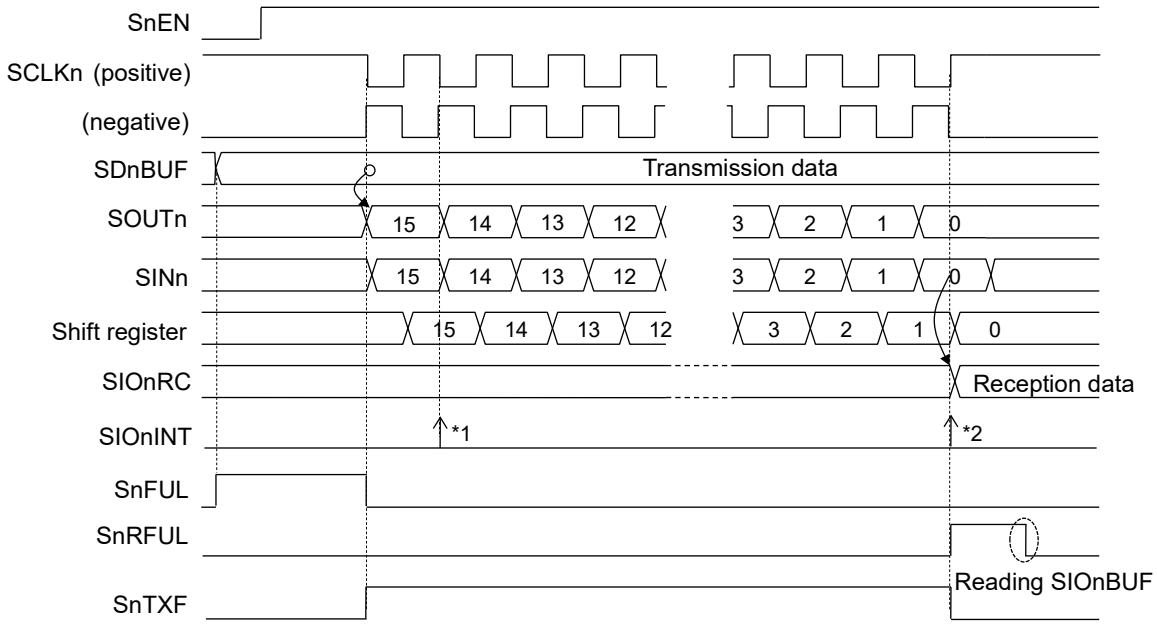
11.3 Description of Operation

The following describes SSIO's case, but it also applies to ESSIO's case.

11.3.1 Communication Timing (Master/Slave)

SOUTn at the end of the transfer maintains the last output state when clock type 0 is set.
If there is next transmit data, it maintains the leading data of next transmit data.
If there is no next transmit data, it maintains the leading data of the transferred data.
If the transmission / reception operation is stopped by writing "0" to SnEN during the transmission / reception operation, SOUTn will maintain the output state when the transmission / reception operation is stopped.

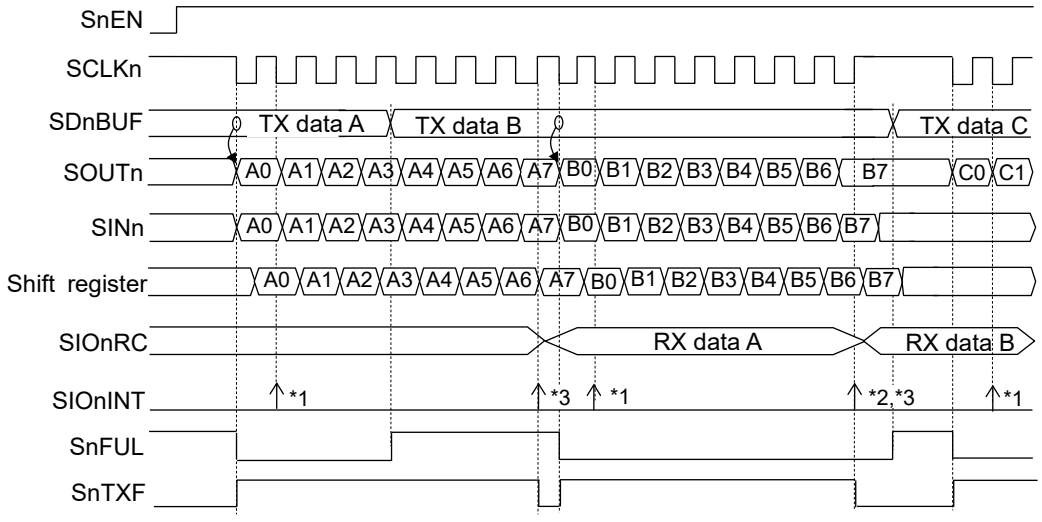
Figure 11-2 shows operation waveforms for clock type 0; with 16-bit length, MSB first.



*1: Transmission buffer empty interrupt, *2: Transfer completion interrupt

Figure 11-2 Waveform for Clock Type 0 with 16-bit length, MSB first

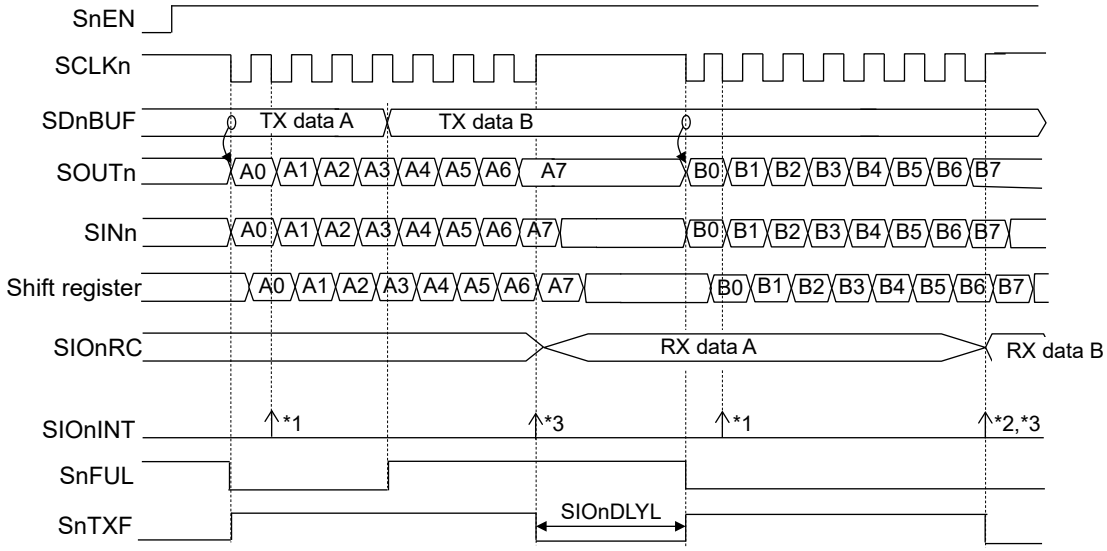
Figure 11-3 shows the continuous transmit and receive operation waveforms of clock type 0 (when SIOnDRY is set to 0x00 in master mode or continuous transfer in slave mode).



*1: Transmission buffer empty interrupt, *2: Transfer completion interrupt
*3 : End interrupt of one frame transfer.

Figure 11-3 Clock type 0 (positive logic) continuous transmit and receive operation waveform (When 0x00 is set in the transmission interval register)

Figure 11-4 shows the continuous transmission and reception operation waveforms of clock type 0 (when SIOnRULE is set to a non-0x00 in master mode or when the transfer interval is set in slave mode).



*1: Transmission buffer empty interrupt, *2: Transfer completion interrupt
*3 : End interrupt of one frame transfer.

Figure 11-4 Waveforms of multi-frames with clock type 0, positive and frame interval

Figure 11-5 shows operation waveforms when writing “0” to SnEN bit during transmission/reception in the clock type 0.

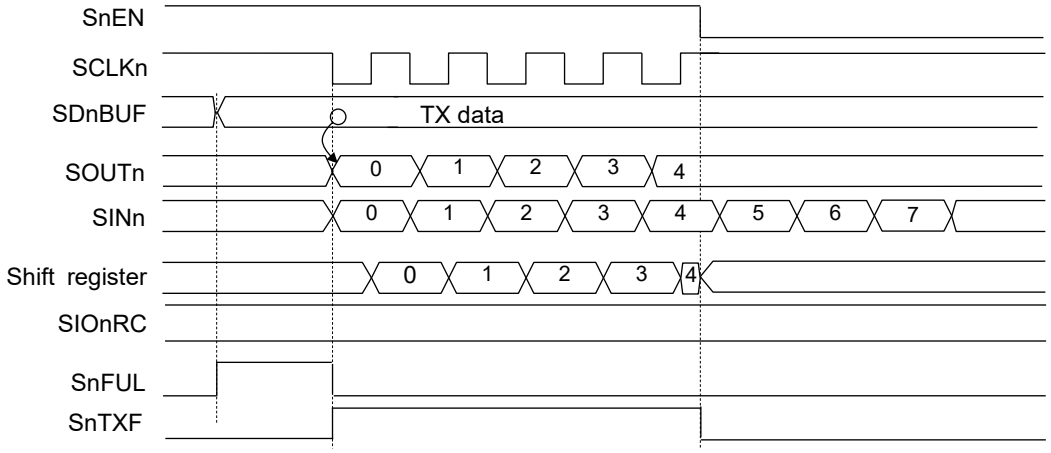


Figure 11-5 Waveforms when writing “0” to SnEN during communication

11.3.2 Interrupt Timing

Table 11-4 shows interrupt timing of SSIO.
The interrupt source is determined by SIOnSTAT register.

- Transmission buffer empty : SnTXF=1 & SnFUL=0
- Transfer completion : SnTXF=0 & SnFUL=0

Table 11-4-1 Interrupt Timing in the master mode

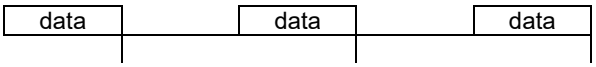
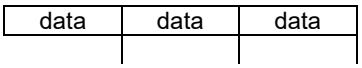
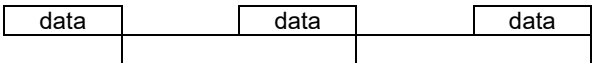
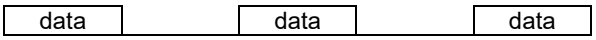
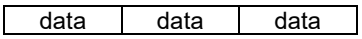
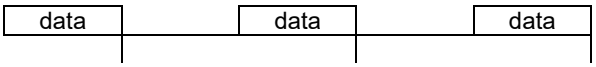
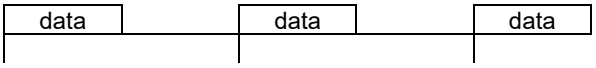
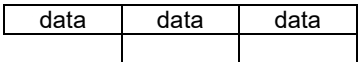
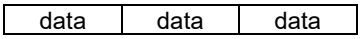
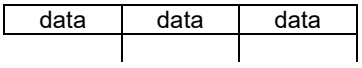
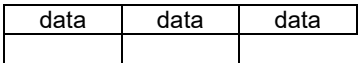
Enabled Interrupt	Frame Interval	SnFUL when end of one frame transfer	Interrupt Timing
End interrupt of one frame transfer	with	1	
	without	1	
	with/without	0	
Transfer completion Interrupt	with	1	
	without	1	
	with/without	0	
Transmission buffer empty Interrupt	with/without	1	

Table 11-4-2 Interrupt Timing in the slave mode

Enabled Interrupt	Frame Interval	SnFUL when end of one frame transfer	Interrupt Timing
End interrupt of one frame transfer	-	-	
Transfer completion Interrupt	-	1	
	-	0	
Transmission buffer empty Interrupt	-	-	

11.3.3 Example of setting

Figure 11-6 shows an example of setting for transmission and reception in the master mode.

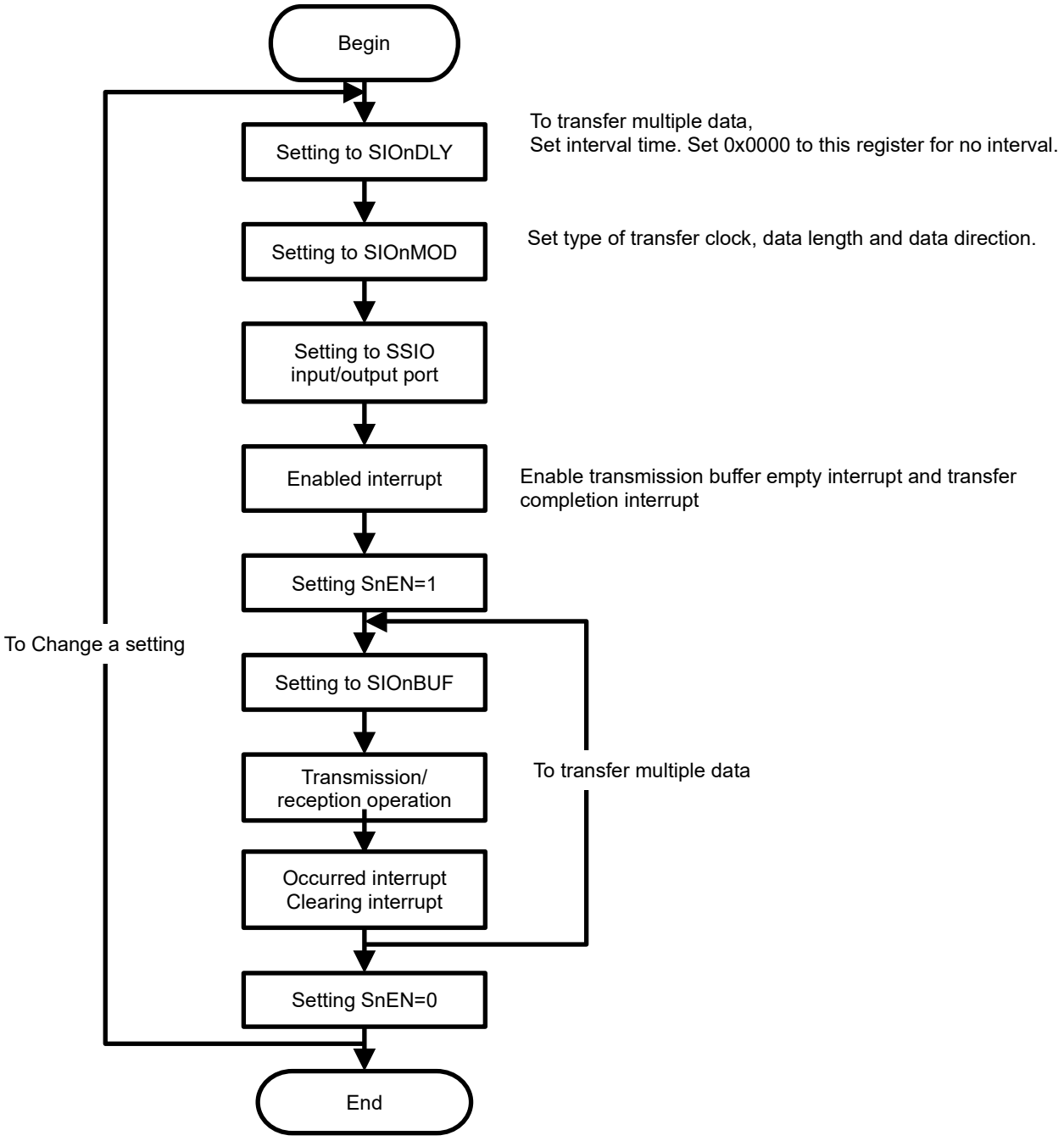


Figure 11-6 Example of setting for transmission/reception in the master mode

Figure 11-7 shows an example of setting for transmission and reception in the slave mode.

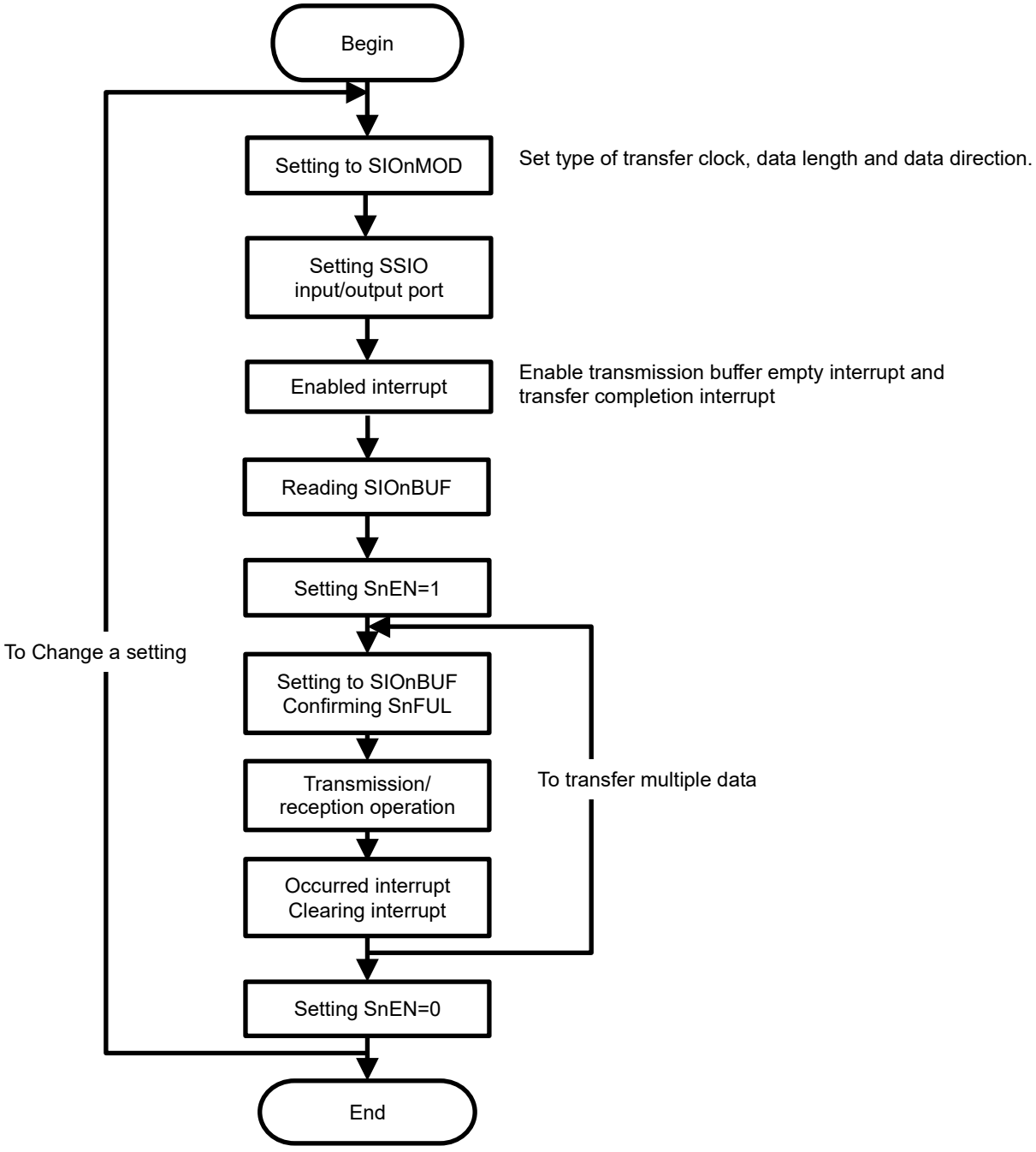
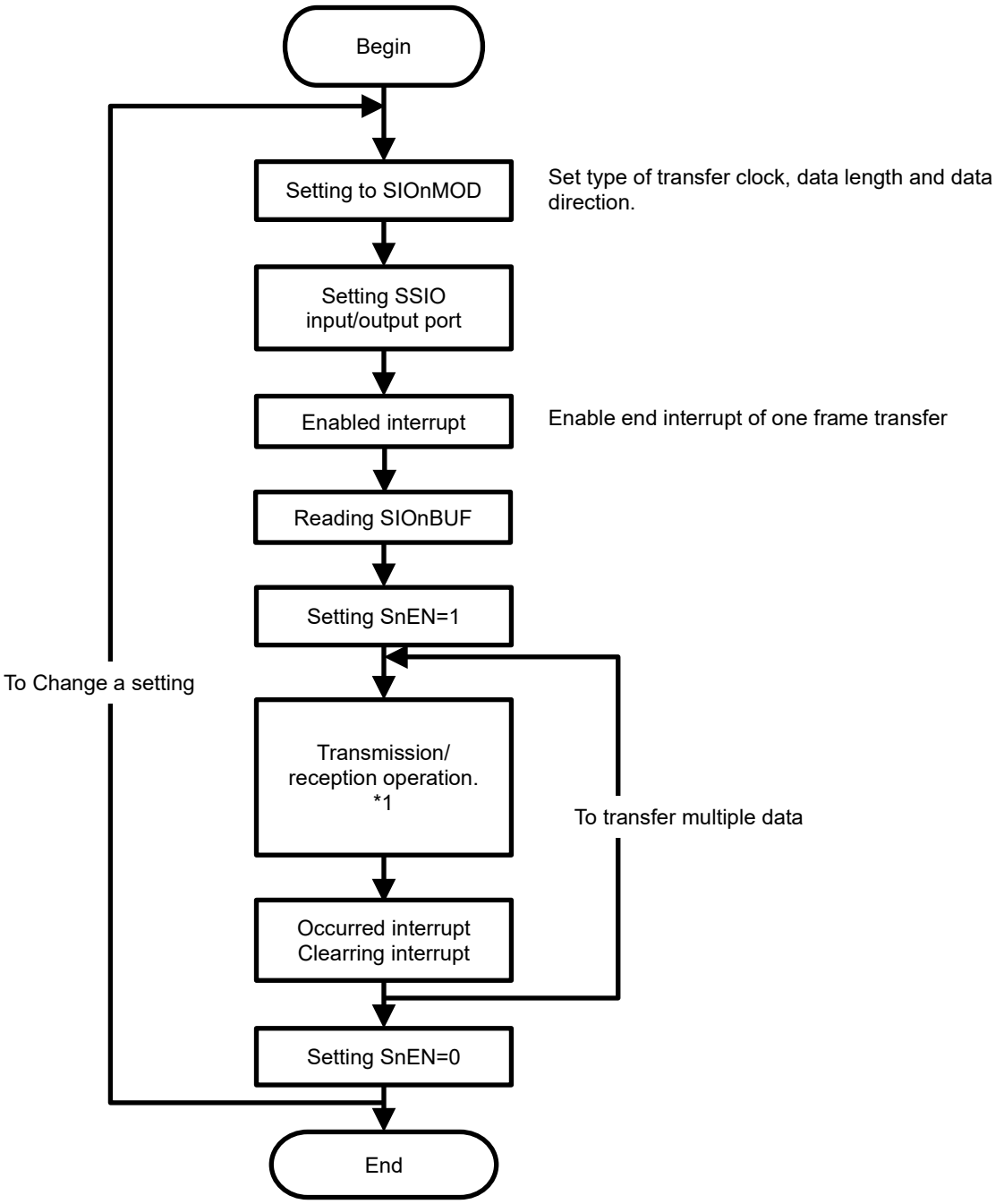


Figure 11-7 Example of setting for transmission/reception in the slave mode

[Note]

- **To prevent an overrun error after the first reception, read the SIOnBUF register before setting the SnEN bit to "1".**

Figure 11-8 shows an example of setting for reception only in the slave mode.



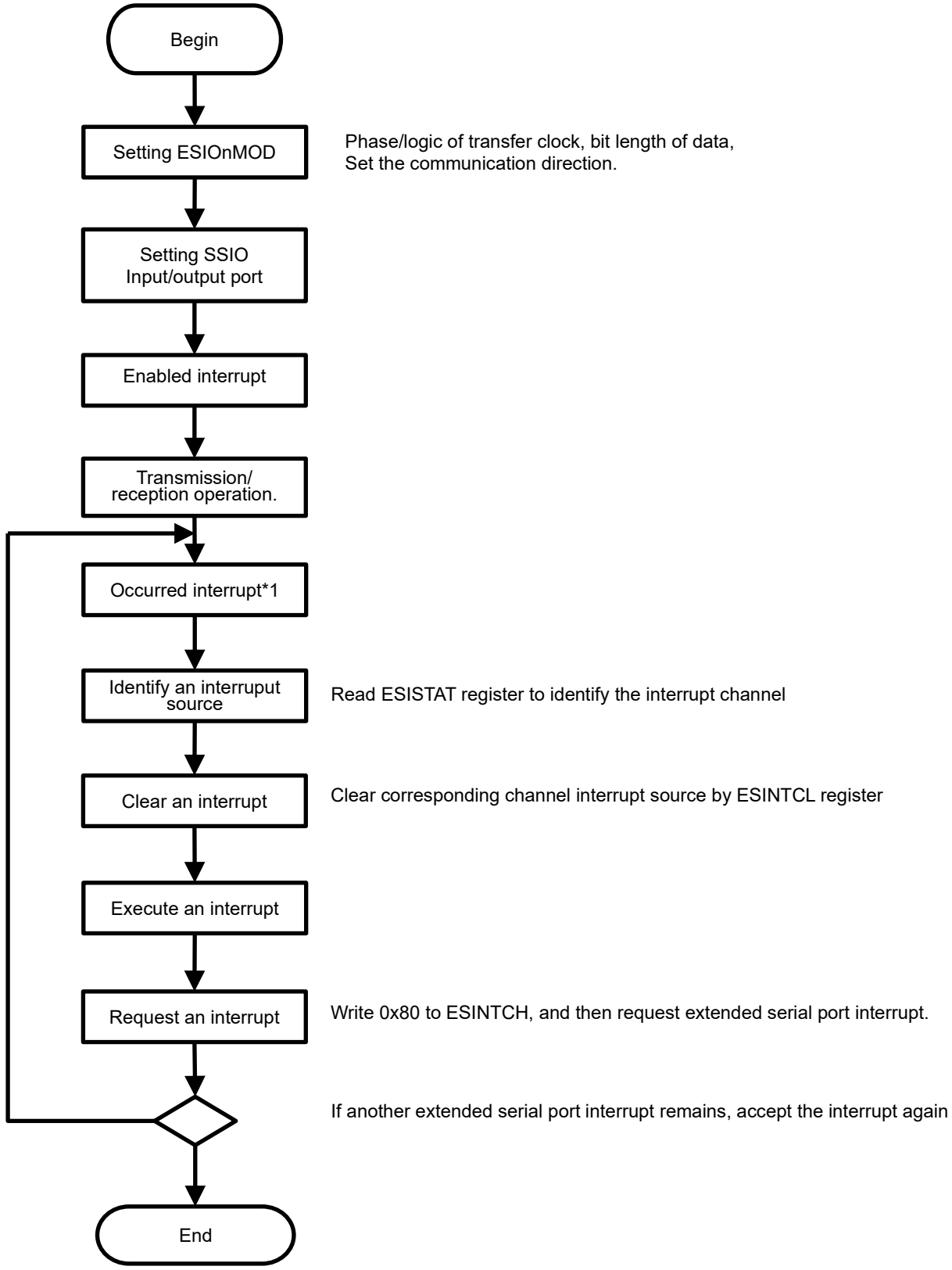
*1 : the transmission data is latest written data. The data is null data (All1) if the SIOnBUF has never been written.

Figure 11-8 Example of setting for reception in the slave mode

[Note]

- **To prevent an overrun error after the first reception, read the SIOnBUF register before setting the SnEN bit to "1".**

Figure 11-19 shows an example of setting for extended serial port interrupt



*1: When writing to IRQ01/IRQ23/IRQ45/IRQ67 from CPU, write "1" to ESIR bit of ESINTC register and rerequest the interrupt.

Figure 11-9 Example of Extended Serial port interrupt setting

11.3.4 Timing of Transmission Underrun Error (SnTUER)

A transmission underrun error (SnTUER) occurs in slave mode only. In master mode, SnTUER is not set to “1” because the transmission is executed when SnFUL=”1”.
Figure 11-9 shows a detection timing of transmission underrun error.

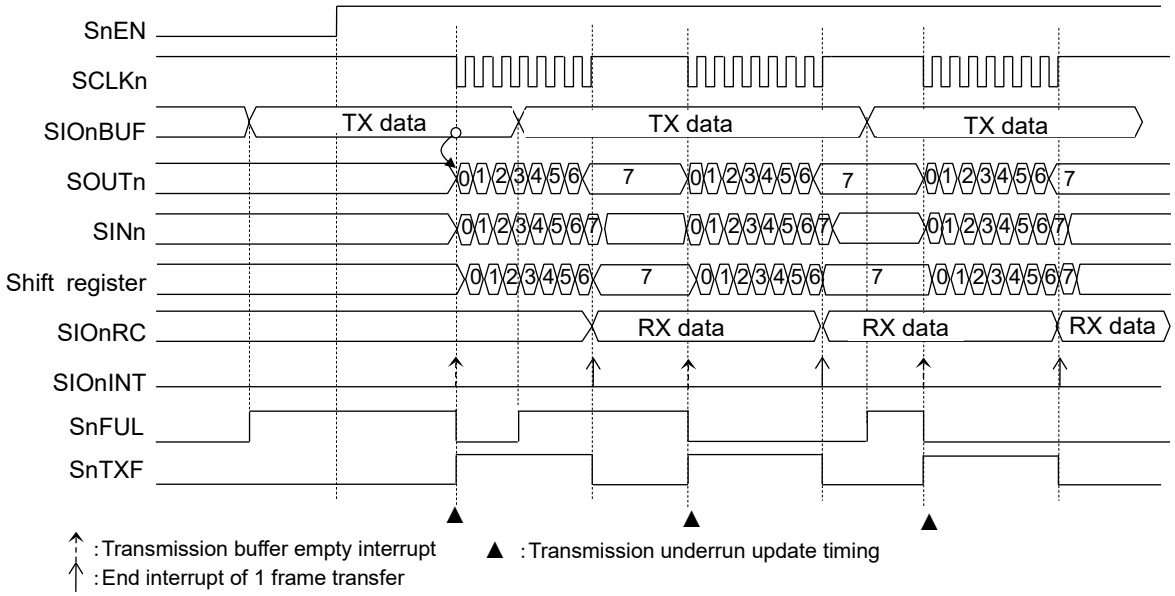


Figure 11-10 clock type 0 with positive

Chapter 12 Synchronous Serial Port with FIFO (SSIOF)

12. Synchronous Serial Port with FIFO (SSIOF)

12.1 General Description

This SSIOF communicate with peripherals and other MCUs.
Table 12-1 shows the number of channels.

Table 12-1 Number of the SSIOF

Channel No.	ML62Q2700 group
0	●

●: Available - : Unavailable

12.1.1 Features

- Full-duplex data transfer
- Selectable from Master mode or Slave mode
- Separate Built-in 4-stage FIFO on transmit-side and receive-side.
- Selectable transfer size (8 bits (byte) or 16 bits (word)).
- Configurable interrupt based on the number of received words (1 to 4 words) of the received FIFO.
- Configurable interrupt based on the number of remain words (0 to 3 words) of the received FIFO.
- Selectable from LSB first or MSB first.
- Selectable Serial Clock Polarity and Phase
- In master mode, the SYSCLK divide-by-2~2046 clock is selectable as the synchronous clock (1023 types)
- In Master mode, the interval before/after transfer is controllable.
- Status bit to indicate transmission/receive complete and FIFO state
- If the transmit FIFO is full state and write more to the FIFO, a SF0SRC error is detected
- Interrupts are generated by factors such as the specific state of the transmit and receive FIFOs
- Self-test function using the master and slave modes. For the self-test functions, see Chapter 29 "Safety Function."

12.1.2 Configuration

Figure 12-1 shows configuration of the SSIOF.

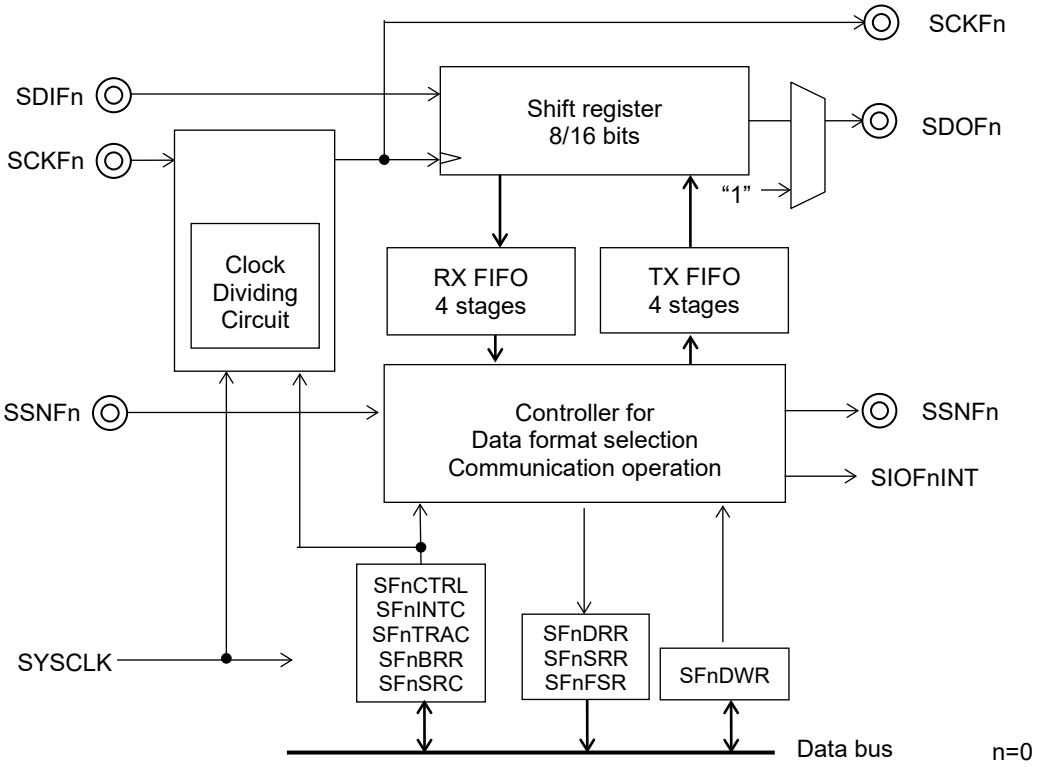


Figure 12-1 Configuration of SSIOF

12.1.3 List of Pins

The I/O pins of the SSIOF are assigned to the shared function of the general ports.

Pin name	I/O	Description
SDOF0	O	SSIOF0 master serial output / slave serial output
SDIF0	I	SSIOF0 master serial input / slave serial input
SCKF0	I/O	SSIOF0 baud rate clock
SSNF0	I/O	SSIOF0 slave selection

Table 12-2 shows the list of the general ports used for the SSIOF and the register settings of the ports.

Table 12-2 Ports used for the SSIOF and the register settings

Channel No.	Pin name	General port		Setting register	Setting value	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702			ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725		
						48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
0	SDIF0	P14	2nd function	P1MOD4	0001_XXXX*1	●	●	●	●	●	●
		P52	2nd function	P5MOD2	0001_XXXX*1	—	—	●	●	●	●
	SDOF0	P16	3rd function	P1MOD6	0010_XXXX*1	●	●	●	—	—	—
		P51	2nd function	P5MOD1	0001_XXXX*2	—	●	●	●	●	●
		P55	2nd function	P5MOD5	0001_XXXX*2	—	—	●	●	●	●
	SCKF0	P50	2nd function	P5MOD0	0001_XXXX*3	●	●	●	●	●	●
		P54	2nd function	P5MOD4	0001_XXXX*3	—	—	●	●	●	●
	SSNF0	P15	2nd function	P1MOD5	0001_XXXX*3	●	●	●	●	●	●
		P53	2nd function	P5MOD3	0001_XXXX*3	—	—	●	●	●	●

●: available - : Not available

*1 : "XXXX" determines the condition of the port input

XXXX	Condition of the port
0001	Input (without an internal pull-up resistor)
0101	Input (with an internal pull-up resistor)

*2 : "XXXX" determines the condition of the port output

XXXX	Condition of the port
0010	CMOS output
1010	Nch open drain output (without the pull-up)
1111	Nch open drain output (with the pull-up)

*3 : "XXXX" determines the condition of the port input / output
In the master mode, see to *2 for use as output.
In the slave mode, see to *1 for use as input.

12.1.4 Combination of SSIOF port

SDOF0, SDIF0, SCKF0, SSNF0 are assigned to multiple general ports.
Be sure to use the ports in following combinations.

Table 12-3 Combination of the SSIOF

Combination	Channel No.	IO pin				ML62Q2700 group				
		SDIF0*	SDOF0*	SCKF0*	SSNF0*	48pin product	52pin product	64pin product	80pin product	100pin product
1	0	P52	P51	P50	P53	-	-	●	●	●
2		P14	P55	P54	P15	-	-	●	●	●
3		P14	P51	P50	P15	-	●	-	-	-
4		P14	P16	P50	P15	●	-	-	-	-

* :n=channel number. ●: Available to use, -: Unavailable

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF580	SIOF0 control register	SF0CTRLL	SF0CTRL	R/W	8/16	0x00
0xF581		SF0CTRLH		R/W	8	0x00
0xF582	SIOF0 interrupt control register	SF0INTCL	SF0INTC	R/W	8/16	0x00
0xF583		SF0INTCH		R/W	8	0x00
0xF584	SIOF0 transfer interval control register	SF0TRACL	SF0TRAC	R/W	8/16	0x02
0xF585		SF0TRACH		R/W	8	0x00
0xF586	SIOF0 baud rate register	SF0BRRL	SF0BRR	R/W	8/16	0x02
0xF587		SF0BRRH		R/W	8	0x50
0xF588	SIOF0 status register	SF0SRRL	SF0SRR	R	8/16	0x00
0xF589		SF0SRRH		R	8	0x14
0xF58A	SIOF0 status clear register (L/H)	SF0SRCL	-	W	8	0x00
0xF58B		SF0SRCH		W	8	0x00
0xF58C	SIOF0 FIFO status register	SF0FSRL	SF0FSR	R	8/16	0x00
0xF58D		SF0FSRH		R	8	0x00
0xF58E	SIOF0 writing data register	SF0DWRL	SF0DWR	R/W	8/16	0x00
0xF58F		SF0DWRH		R/W	8	0x00
0xF590	SIOF0 reading data register	SF0DRRL	SF0DRR	R	8/16	0x00
0xF591		SF0DRRH		R	8	0x00

12.2.2 SIOF0 Control Register (SF0CTRL)

SF0CTRL is a SFR to control SSIOF0 operation.

Address : 0xF580 (SF0CTRLL /SF0CTRL), 0xF581 (SF0CTRLH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0CTRL															
Byte	SF0CTRLH								SF0CTRLL							
Bit	-	-	-	-	-	-	-	SF0FICL	-	SF0CPOL	SF0CPHA	SF0LSB	-	SF0SIZ	SF0MST	SF0SPE
R/W	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 9	-	Reserved bits
8	SF0FICL	Clear FIFO status. 0: No operation (Initial value) 1: Clear frame counts of reception/transmission
7	-	Reserved bits
6	SF0CPOL	Select edge of transfer clock. 0: 1st edge is positive; the clock level is “L” during the idling. (Initial value) 1: 1st edge is negative; the clock level is “H” during the idling.
5	SF0CPHA	Select the phase of transfer clock. 0: Clock type 1: (Initial value) 1st edge is used to sample a data, 2nd edge is used to shift a data. Repeat thereafter. 1: Clock type 0: 1st edge is used to shift a data, 2nd edge is used to sample a data. Repeat thereafter.
4	SF0LSB	Select transfer data direction. 0: LSB first (Initial value) 1: MSB first
3	-	Reserved bits
2	SF0SIZ	Select transfer size of 1 frame. 0: 8 bit (Initial value) 1: 16 bit
1	SF0MST	Select master/slave mode. 0: Slave mode (Initial value) 1: Master mode
0	SF0SPE	Select enable/disable transfer of the SSIOF. 0: Disabled (Initial value) 1: Enabled

12.2.3 SIOF0 Interrupt Control Register (SF0INTC)

SF0INTC is a SFR to control interrupt operation for SSIOF0.

Address : 0xF582 (SF0INTCL/SF0INTC), 0xF583 (SF0INTCH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0INTC															
Byte	SF0INTCH								SF0INTCL							
Bit	-	-	SF0RFIC1	SF0RFIC0	-	-	SF0TFIC1	SF0TFIC0	-	-	-	-	SF0ORIE	SF0FIE	SF0RFIE	SF0TFIE
R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 14	-	Reserved bits
13 to 12	SF0RFIC1 to SF0RFIC0	Selects the receive FIFO interrupt control. 00: Interrupt occurs at 1 frame reception (initial value) 01: Interrupt occurs when receiving 2 frames 10: Interrupt occurs on 3-frame reception 11: Interrupt occurs on 4-frame reception
11 to 10	-	Reserved bits
9 to 8	SF0TFIC1 to SF0TFIC0	Select the interrupt control of remaining byte number of bits in the transmit FIFO. 00: Interrupt occurs when transmitting 0 remaining frames (initial value) 01: Interrupt occurs with one frame remaining 10: Interrupt occurs with 2 frames remaining 11: Interrupt occurs on transmission of 3 frames remaining
7 to 4	-	Reserved bits
3	SF0ORIE	Select overrun error interrupt request. 0: Disabled (Initial value) 1: Enabled
2	SF0FIE	Select transfer completion interrupt request. 0: Disabled (Initial value) 1: Enabled
1	SF0RFIE	Select reception interrupt request. 0: Disabled (Initial value) 1: Enabled
0	SF0TFIE	Select transmission interrupt request. 0: Disabled (Initial value) 1: Enabled

12.2.4 SIOF0 Transfer Interval Control Register (SF0TRAC)

SF0TRAC is a SFR to set the minimum data transfer interval in Master mode.
See 12.3.6 “Transfer Interval Setting” for details.

Address : 0xF584 (SF0TRACL/SF0TRAC), 0xF585 (SF0TRACH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0002

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0TRAC															
Byte	SF0TRACH								SF0TRACL							
Bit	-	-	-	-	-	-	-	SF0DTL8	SF0DTL7	SF0DTL6	SF0DTL5	SF0DTL4	SF0DTL3	SF0DTL2	SF0DTL1	SF0DTL0
R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

12.2.5 SIOF0 Baud Rate Register (SF0BRR)

SF0BRR is a SFR to set the operation mode.
Do not change the setting of this register during transfer. The behavior is not guaranteed if changed during transfer

Address : 0xF586 (SF0BRRL/SF0BRR), 0xF587 (SF0BRRH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x5002

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0BRR															
Byte	SF0BRRH								SF0BRRL							
Bit	SF0LAG1	SF0LAG0	SF0LEAD1	SF0LEAD0	-	-	SF0BR9	SF0BR8	SF0BR7	SF0BR6	SF0BR5	SF0BR4	SF0BR3	SF0BR2	SF0BR1	SF0BR0
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0

Bit No.	Bit symbol name	Description
15 to 14	SF0LAG1 to SF0LAG0	Select the interval between SCKF0 and SSNF0 (H). 00: 0.5 × SCKF0 01: 0.5 × SCKF0 (Initial value) 10: 1.0 × SCKF0 11: 1.5 × SCKF0
13 to 12	SF0LEAD1 to SF0LEAD0	Select the interval between SSNF0 (L) and SCKF0. 00: 0.5 × SCKF0 01: 0.5 × SCKF0 (Initial value) 10: 1.0 × SCKF0 11: 1.5 × SCKF0
11 to 10	-	Reserved bits
9 to 0	SF0BR9 to SF0BR0	Configure the baud rate. (valid in the master mode) $f_{SCK}=f_{SYSCLK}/(2 \times SF0BR9\text{-}0)$ f_{SYSCLK} : SYSCLK frequency 0000000000: 2 dividing 0000000001: 2 dividing 0000000010: 4 dividing (Initial value) 0000000011: 6 dividing : 1111111111: 2046 dividing In the master mode, max frequency of transfer clock is 4MHz; See section ELECTRICAL CHARACTERISTICS in ML62Q2700 data sheet for the detail.

[Note]
The maximum transfer frequency of SIOF is 4MHz, so set it so that it does not exceed 4MHz.

12.2.6 SIOF0 Status Register (SF0SRR)

SF0SRR is a SFR to indicate the data transfer state and error state of the SSIOF0.

Address : 0xF588 (SF0SRRL/SF0SRR), 0xF589 (SF0SRRH)
Access : R
Access size : 8/16 bit
Initial value : 0x1400

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0SRR															
Byte	SF0SRRH								SF0SRRL							
Bit	-	-	SF0SSF	SF0RFE	SF0RFF	SF0TFE	SF0TFF	SF0WOF	-	-	SF0SPIF	-	SF0ORF	SF0FI	SF0RFI	SF0TFI
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 14	-	Reserved bits
13	SF0SSF	Indicates the state of the slave select signal (SSNF0).. 0: “H” level (Initial value) 1: “L” level; communicating
12	SF0RFE	Indicate the reception FIFO empty. 0: Not empty 1: Empty; No interrupt is generated (Initial value)
11	SF0RFF	Indicate the reception FIFO full. 0: Not full (Initial value) 1: Full; No interrupt is generated
10	SF0TFE	Indicate the transmission FIFO empty. 0: Not empty 1: Empty; No interrupt is generated (Initial value)
9	SF0TFF	Indicate the transmission FIFO full. 0: Not full (Initial value) 1: Full; No interrupt is generated
8	SF0WOF	Indicate the write overflow of transmission FIFO 0: Not occurred (Initial value) 1: Occurred; No interrupt is generated
7 to 6	-	Reserved bits
5	SF0SPIF	Indicate the completion of 1 frame transfer. 0: Not completed (Initial value) 1: Completed
4	-	Reserved bits
3	SF0ORF	Indicate the overrun flag. 0: Not occurred (Initial value) 1: Occurred; interrupt is generated
2	SF0FI	Indicate the transfer completion interrupt. It occurs when transfer last frame data is completed in condition of that transmission FIFO is empty. 0: No interrupt request (Initial value) 1: Interrupt request
1	SF0RFI	Indicate the reception interrupt. It occurs when the number of data in the reception FIFO is equal or more frame count configured with SF0RFIC1 to 0. 0: No interrupt request (Initial value) 1: Interrupt request
0	SF0TFI	Indicate the transmission interrupt. It occurs when the remaining data in the transmission FIFO matches the frame count configured with SF0TFIC1 to 0. 0: No interrupt request (Initial value) 1: Interrupt request

12.2.7 SIOF0 Status Clear Register L/H (SF0SRCL, SF0SRCH)

SF0SRCL, SF0SRCH is a SFR to clear the data transfer state and error state of the SSIOF.

Address : 0xF58A (SF0SRCL), 0xF58B (SF0SRCH)
Access : W
Access size : 8 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	SF0SRCH								SF0SRCL							
Bit	SF0IRQ	-	-	-	-	-	-	SF0WOFC	-	-	SF0SPIFC	-	SF0ORFC	SF0FC	SF0RFC	SF0TFC
R/W	W	R	R	R	R	R	R	W	R	R	W	R	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	SF0IRQ	Issue the interrupt request again by writing “1” in case there is an outstanding interrupt source.
14 to 9	-	Reserved bits
8	SF0WOFC	Clears write overflow. Writing 1 clears the write overflow flag (SF0WOF).
7 to 6	-	Reserved bits
5	SF0SPIFC	Clears the end of a 1 frame transmission. Writing 1 clears the end-of-transfer flag (SF0SPIF).
4	-	Reserved bits
3	SF0ORFC	Clears the interrupt request of overrun error flag. Writing 1 clears the interrupt request. For interrupt requests, check the SF0ORF bit of SF0SRR.
2	SF0FC	Clears the transfer completion interrupt request. Writing 1 clears the interrupt request. For interrupt requests, check the SF0FI bit of SF0SRR.
1	SF0RFC	Clears the reception interrupt request. Writing 1 clears the interrupt request. For interrupt requests, check the SF0RFI bit of SF0SRR.
0	SF0TFC	Clears the transmission interrupt request. Writing 1 clears the interrupt request. For interrupt requests, check the SF0TFI bit of SF0SRR.

[Note]

- **Write "1" to SF0IRQ bit while there is any unprocessed interrupt source and processing all the interrupt sources before exiting the interrupt vector will cause re-entry to the interrupt vector with no interrupt source after exiting the interrupt vector. Ensure to write "1" before exiting the interrupt vector.**

12.2.8 SIOF0 FIFO Status Register (SF0FSR)

SF0FSR is a SFR to indicate the remaining frame counts in transmission/reception FIFO.

Address : 0xF58C (SF0FSRL/SF0FSR), 0xF58D (SF0FSRH)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0FSR															
Byte	SF0FSRH								SF0FSRL							
Bit	-	-	-	-	-	SF0RFD2	SF0RFD1	SF0RFD0	-	-	-	-	-	SF0TFD2	SF0TFD1	SF0TFD0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 11	-	Reserved bits
10 to 8	SF0RFD2 to SF0RFD0	Indicate the number of bytes (Word) received in the reception FIFO. 000: Empty (default) 001: 1 byte/1 word 010: 2 bytes/2 words 011: 3 bytes/3 words100: 4 bytes/4 words (full)
7 to 3	-	Reserved bits
2 to 0	SF0TFD2 to SF0TFD0	Indicate the number of unsent Byte (Word) in the transmission FIFO. 000: Empty (default) 001: 1Byte/1Word 010: 2Byte/2Word 011: 3Byte/3Word 100: 4Byte/4Word（Full）

12.2.9 SIOF0 Writing Data Register (SF0DWR)

This SF0DWR is a SFR to write transmission data.

Address : 0xF58E (SF0DWRL/SF0DWR), 0xF58F (SF0DWRH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0DWR															
Byte	SF0DWRH								SF0DWRL							
Bit	SF0WD15	SF0WD14	SF0WD13	SF0WD12	SF0WD11	SF0WD10	SF0WD9	SF0WD8	SF0WD7	SF0WD6	SF0WD5	SF0WD4	SF0WD3	SF0WD2	SF0WD1	SF0WD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

For write access to this register, follow the below according to the transmission size.
8-bit length data write access to SF0DWRL for 8 bit transmission; SF0SIZ=0.
16-bit length data write access to SF0DWR for 16 bit transmission; SF0SIZ=1.

12.2.10 SIOF0 Reading Data Register (SF0DRR)

SF0DRR is a SFR to read reception data.

Address : 0xF590 (SF0DRRL/SF0DRR), 0xF591 (SF0DRRH)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SF0DRR															
Byte	SF0DRRH								SF0DRRL							
Bit	SF0RD15	SF0RD14	SF0RD13	SF0RD12	SF0RD11	SF0RD10	SF0RD9	SF0RD8	SF0RD7	SF0RD6	SF0RD5	SF0RD4	SF0RD3	SF0RD2	SF0RD1	SF0RD0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

For read access to this register, follow the below according to the reception size.
8-bit length data read access to SF0DRRL for 8 bit reception; SF0SIZ=0.
16-bit length data read access to SF0DRR for 16 bit reception; SF0SIZ=1.

12.3 Description of Operation

12.3.1 Master Mode / Slave Mode

Master mode and Slave mode are available as transmission / reception mode. It is selectable by SF0MST bit of SIOF0 control register.

The SF0BR9-0 (baud rate), SF0LEAD1-0 (SSNF0-SCKF0 delay interval), SF0LAG1-0 (SCKF0-SSNF0 delay interval) of the SIOF0 baud rate register, and SF0DTL8-0 (minimum data transfer interval) of SIOF0 transfer interval control register are valid only during master operation, and the operation of SCKF0 and SSNF0 is determined by them.
Each bit of SF0CPOL, SF0CPHA, SF0LSB and SF0SIZ bits need to have the same value for master and slave.

12.3.2 Serial Clock Baud Rate (Master Mode)

A baud rate is configured by SF0BR9-0 bits of SF0BRR register. This is only valid in the master mode. The baud rate clock SCKF0 is generated by dividing SYSCLK.
The baud rate (fSCK) is calculated as follows:

$f_{SCK} = f_{SYSCLK} / (2 \times SF0BR9\text{-}0)$

f_{SCK} : A frequency of baud rate clock
f_{SYSCLK} : A frequency of system clock
SF0BR9-0 : Value set in SF0BR9-0 of SF0BRR (1 to 1023)
If 0 is set SF0BR register, it is processed as 1.
It can be selected from 1023 dividing types (2 to 2046)

12.3.3 Control of Polarity and Phase of Serial Clock

SF0CPOL bit of SF0CTRL register controls the clock polarity. SF0CPHA bit of SF0CTRL register controls the clock phase and determines the shift timing of transmit data and the sampling timing of received data. The master and slave which communicate with each other must have the same setting values for SF0CPOL bit and SF0CPHA bit.

12.3.4 Data Transfer Timing

Figure 12-2 shows the data transfer timing when SF0CPHA bit is "0". SSF0 is the slave selection input in Slave mode. In Master mode, the transfer is started when data is written to the SF0DWR register. In Slave mode, the transfer is started at the SSF0 falling edge. The received data is sampled at the rising-edge of SCKF0 in SF0CPOL is “0” and the falling-edge of SCKF0 in SF0CPOL is “1”. The transmitted data is shifted at the falling-edge of SCKF0 in SF0CPOL is “0” and the rising-edge of SCKF0 in SF0CPOL is “1”.

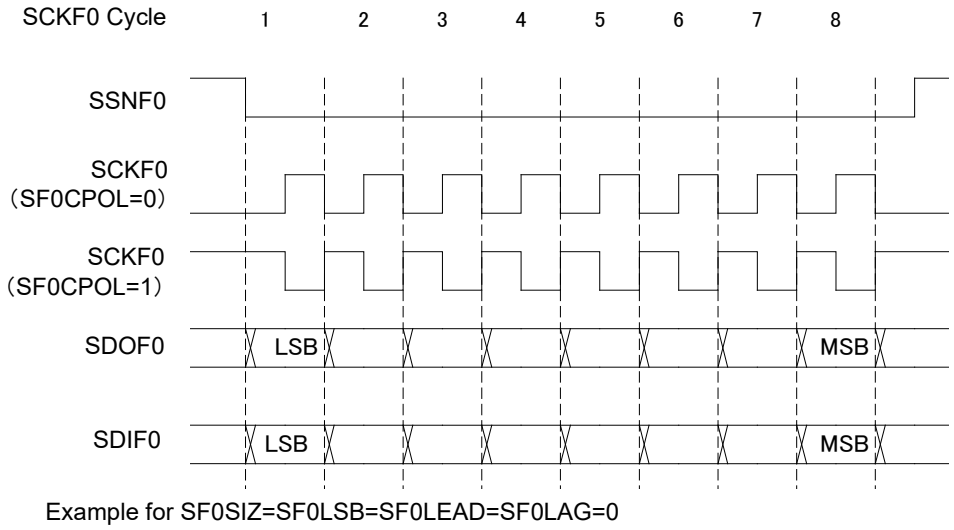


Figure 12-2 8-bit length data transfer at SF0CPHA=0

Figure 12-3 shows the data transfer timing when SF0CPHA bit is "1". SSF0 is the slave selection input in Slave mode. In Master mode, the transfer is started when data is written to SF0DWR. In Slave mode, the transfer is started at the first edge of SCKF0. The received data is sampled at the falling-edge of SCKF0 in SF0CPOL is “0” and the rising-edge of SCKF0 in SF0CPOL is “1”. The transmitted data is shifted at the rising-edge of SCKF0 in SF0CPOL is “0” and the falling-edge of SCKF0 in SF0CPOL is “1”.

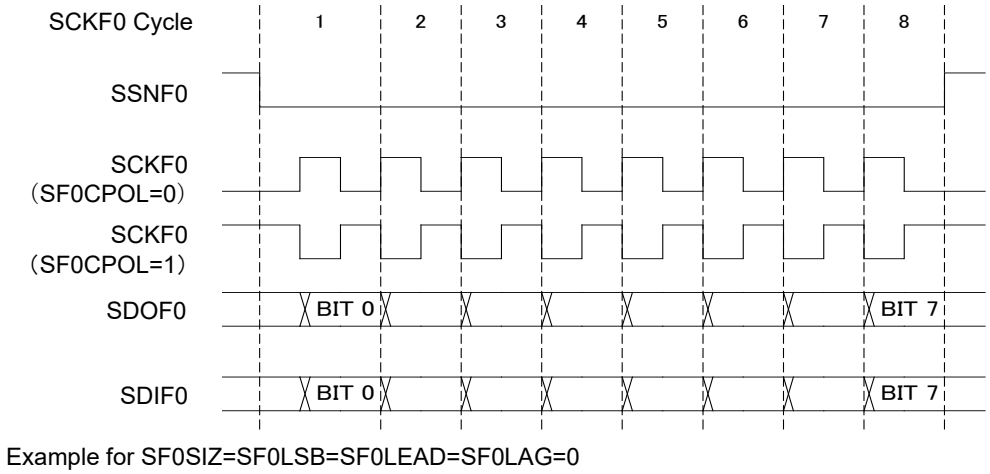


Figure 12-3 8-bit length data transfer at SF0CPHA=1

12.3.5 Transfer Size

The transfer size is selectable from 8 bit (byte) or 16 bit (word) .
Transfer data read/write must be coincided to the transfer size. As the number of FIFO stages is the same for both byte and word, the number of transfers is the same. The master and slaves which communicate with each other must have the same value for SF0SIZ.

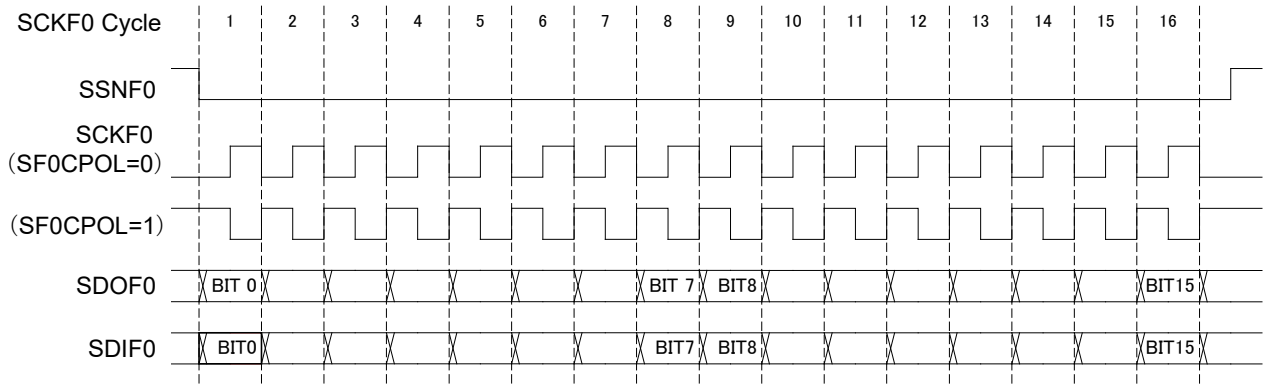


Figure 12-4 SSIOF Bus Waveform with SF0CPHA=0, SF0SIZ=1

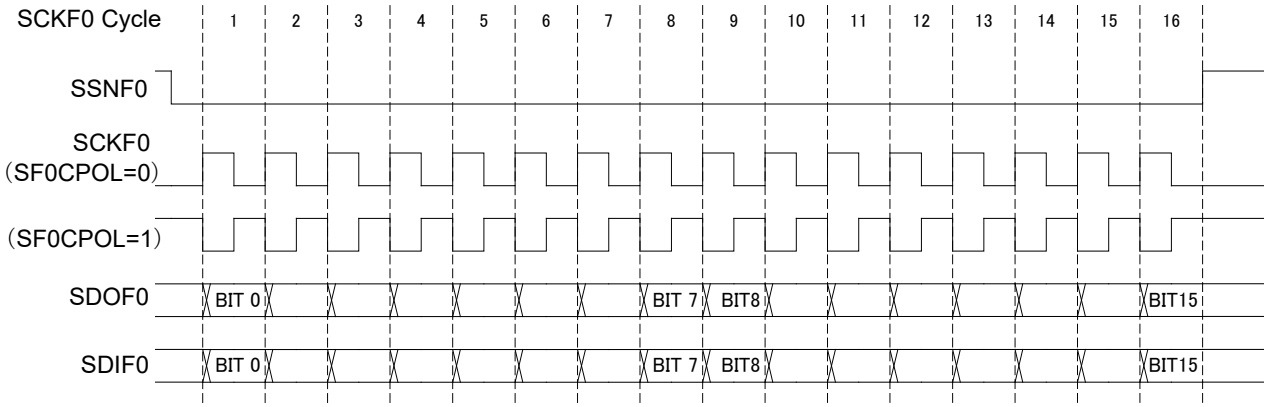


Figure 12-5 SSIOF Bus Waveform with SF0CPHA=1, SF0SIZ=1

12.3.6 Transfer Interval Setting (Master Mode)

LEAD; SSF0-SCKF0 time, LAG; SCKF0-SSF0(H) time, and TDTL; SSF0(H)-SSF0(H) is configurable to adjust the speed to the slave. This setting is only valid in Master mode. It is ignored in Slave mode. Setting during transferring is invalid.

1) LEAD
   A value from 0.5 to 1.5 SCKF0 are valid to set.
2) LAG
   A value from 0.5 to 1.5 SCKF0 are valid to set.
3) TDTL
   The minimum transfer interval is controllable in unit of SCKF0 clocks by setting SF0DTL bit of the SF0TRAC register. If there is any transfer data in FIFO, the time set by this setting (SSF0) changes to "1" during byte/word transfer. If there is no transfer data in FIFO, this is "1" until any transmitted data is written. If SF0DTL bit of SF0TRAC register is set to 0, the interval after transfer (TDTL) disappears and a continuous transfer is performed. SSF0 is held to 0 and returns to 1 after the transfer is finished.

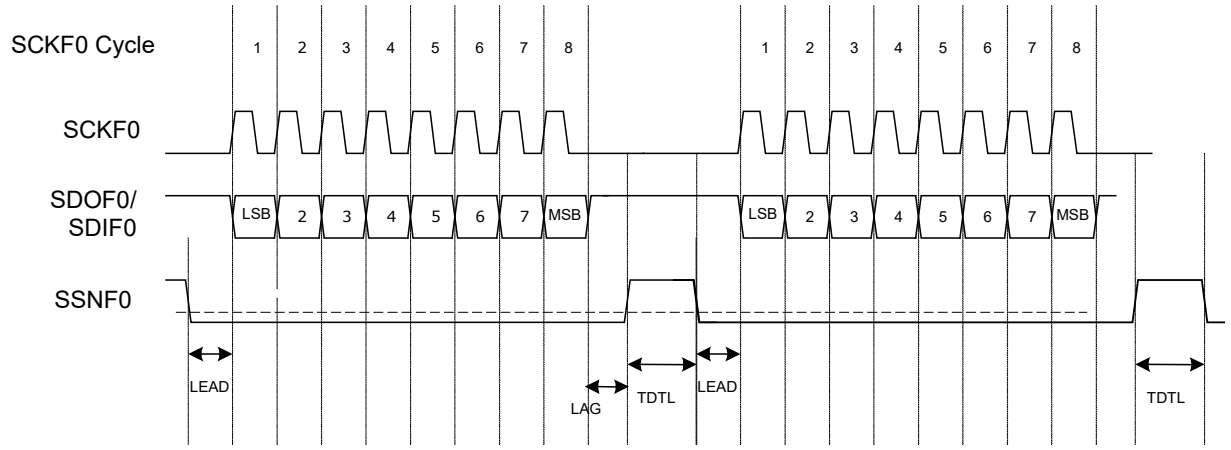


Figure 12-6 Transfer Interval without SF0DTL = "0"

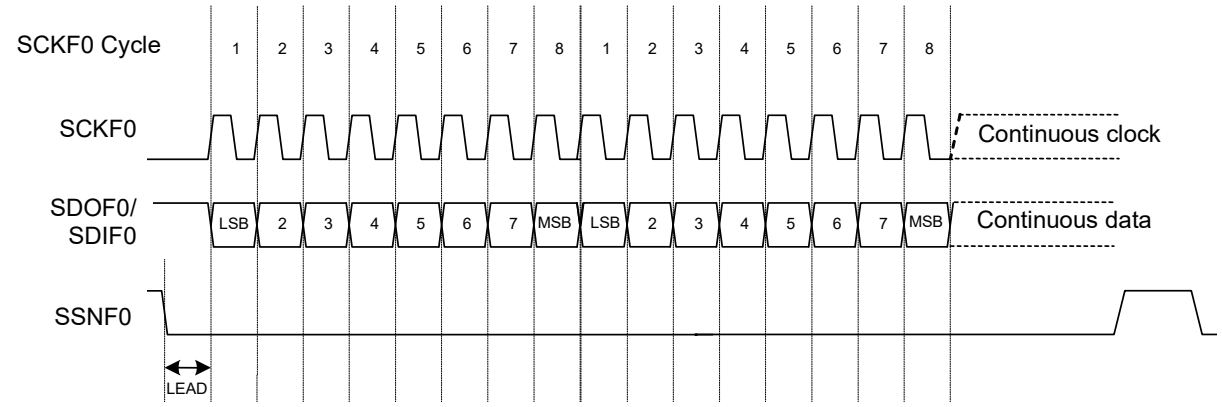


Figure 12-7 Transfer Interval with SF0DTL = "0"

12.3.7 Transmission Operation (Master Mode)

(1) Write the necessary values to SF0CTRL, SF0INTC, SF0BRR, and SF0TRAC, set SF0MST bit to Master mode, and set SF0SPE bit to enable SSIOF transfer.
(2) When the transmitted data is written to SF0DWR, the transmit FIFO Empty flag changes to 0 (SF0TFE = 0). SSIOF starts the automatic transmission and outputs the transmitted data from LSB or MSB on SDOF0 pin according to SF0LSB setting.
(3) The synchronization clock set by SF0CPOL, SF0CPHA, and SF0BRR registers is output from SCKF0 pin.
(4) The transmitted data is writable to SF0DWR sequentially. However, if further writes are performed in the Full state of the transmit FIFO (SF0TFF=1), a write overflow occurs (SF0WOF=1). No interrupt occurs.
(5) The SF0SPIF bit is set each time the transfer of 1 frame is completed. (SF0SPIF=1)
(6) A transmission interrupt occurs if the remaining data in the transmit FIFO matches the frame count selected with SF0TFIC. (SF0TFI=1)
(7) If the transmit FIFO becomes empty and the transfer of the last frame is completed, a transfer completion interrupt is occurred. (SF0FI=1)

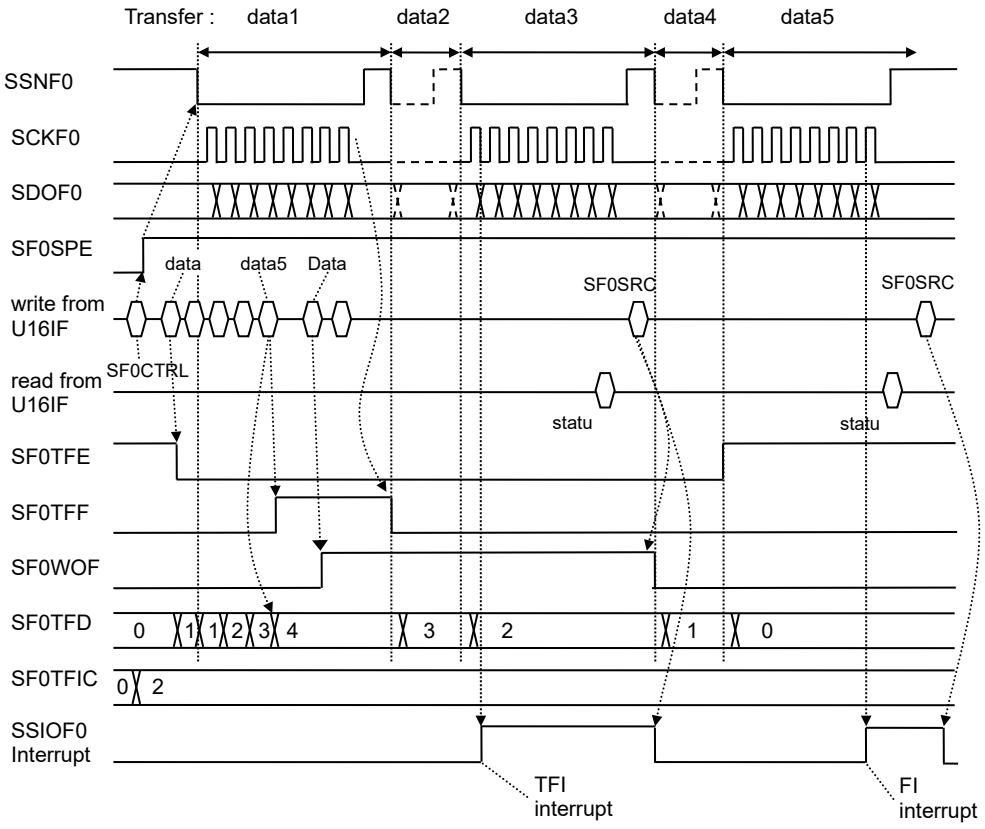


Figure 12-8 Transmission Operation in the Master Mode

12.3.8 Reception Operation (Master Mode)

The master mode of the synchronous serial with FIFO starts by setting data in a transmission buffer. The Data needs to be set into a transmission buffer even master mode reception only.

(1) Write the necessary values to SF0CTRL, SF0INTC, SF0BRR and SF0TRAC, and then set SF0MST bit to the master mode, and set SF0SPE bit to enable the SSIOF transfer.
(2) When the data is written to SF0DWR, SSIOF transfer is started.
(3) The synchronous clock, which was set by SF0CPOL, SF0CPHA, and SF0BRR0-1 registers, is output from the SCKF0 pin.
(4) On the SINF0 pin, the received data is sampled from LSB or MSB according to SF0LSB setting and stored in the reception FIFO. The reception FIFO empty flag changes to 0 (RFE = 0).
(5) SF0SPIF bit is set each time the transfer of 1 frame is completed. (SF0SPIF=1)
(6) If the number of data received in the reception FIFO is equal to or more than matches following the frame count selected with SF0RFIC of SF0CR, SF0RFI of SF0SRR is set to generate a reception interrupt. (SF0RFI=1)
(7) When the reception FIFO becomes full, the subsequent reception is disabled. If the reception is performed in this state, an overrun error interrupt is generated. (SF0ORF=1)
(8) If the temporary data of transmission FIFO becomes empty and the transfer of the last frame is completed, a transfer completion interrupt is generated. (SF0FI=1)

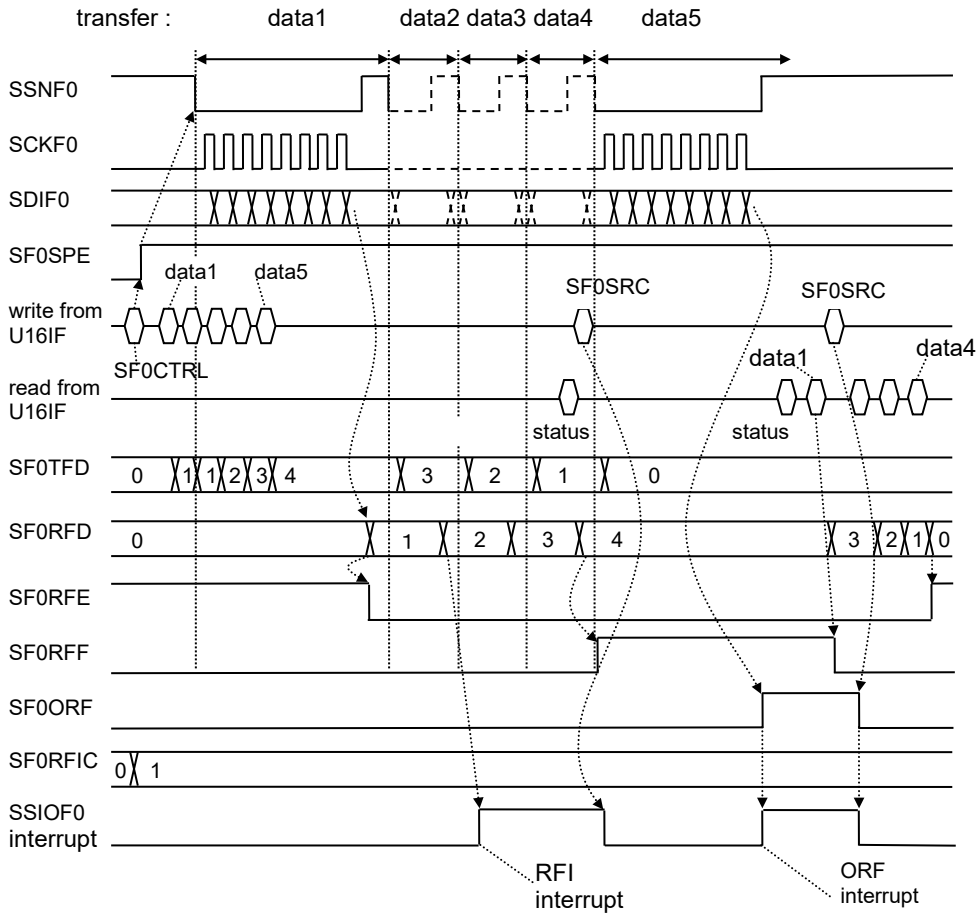


Figure 12-9 Reception Operation in the Master Mode

12.3.9 FIFO Operation

SSIOF includes the receive FIFO of 4 words and the transmit FIFO of 4 words. FIFO state is indicated in SF0TFF, SF0TFE, SF0RFF, and SF0RFE bits of SF0SRR, and SF0TFD2-0 and SF0RFD2-0 bit of SF0FSR.
There are three FIFO states, Full (SF0TFF and SF0RFF), Empty (SF0TFE and SF0RFE), and Depth (SF0TFD and SF0RFD).

12.3.10 Writing Overflow for Transmission

If further writes are performed in the Full state of the transmit FIFO (SF0TFF=1), a write overflow occurs (SF0WOF=1). However, No interrupt occur even when a write overflow occurs.
SF0WOF is cleared when write “1” in SF0WOFC bit of SF0SRCH.

12.3.11 Overrun Error for Reception

If further reception is performed in the Full state of the reception FIFO (SF0RFF = 1), an overrun error occurs. (SF0ORF=1)
If the overrun error occurs, SF0ORF bit of SF0SRR is set, and an overrun error interrupt occur. The newly received data is not held.
Read the content of the reception FIFO to clear SF0RFF bit, then write "1" in SF0ORFC bit to clear SF0ORFC bit.

12.3.12 FIFO Clearing

The transmission/reception counter control of FIFO is initialized to the initial setting state (SF0TFF=0, SF0TFE=1, SF0RFF=0, and SF0RFE=1 in the SF0SRR register and SF0TFD2-0=000 and SF0RFD2-0=000 in the SF0FSR register) by setting SF0FICL bit of SF0CTRL register to 1.
Set SF0FICL bit of SF0CTRL to 0 before next transfer operation.
Even if SF0FICL bit of SF0CTRL register is set to 1, the interrupt for SF0RFIC, SF0TFIC, SF0ORIE, SF0FIE, SF0RFIE, and SF0TFIE of the SF0INTC register, and SF0ORF, SF0FI, SF0RFI, and SF0TFI of the SF0SRR register are not changed
This bit is usable to discard the data of FIFO when the communication is aborted.

12.3.13 Transfer When Slave has different number of FIFO Transfer Frame

1) The master sends data only when the transmission data is already written in FIFO.
As the slave's transmission data count is determined by the master, data is transferred as follows if the number of FIFO transfer frame of slave is different from that of the master.
2) If the transmission data is not written in the slave's FIFO, a 0xFF ((0xFFFF) for word) is sent, including the state after a reset.

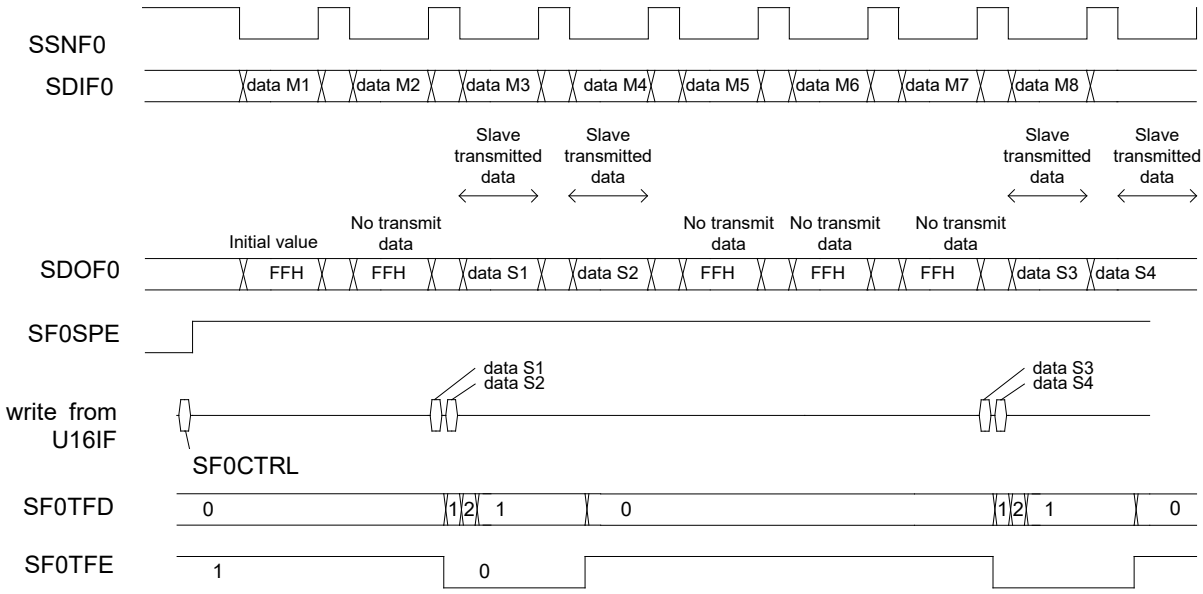


Figure 12-10 Transfer When Slave Has Different Number of FIFO Transfer Frame

12.3.14 Interrupt

12.3.14.1 SSIOF Interrupt Source

There are the following four types.

- Overrun
  If an overrun occurs, SF0ORF bit of SF0SRR register is set, and the overrun error interrupt occurs.
- Transmission FIFO threshold
  If the remaining data of the transmission FIFO matches the frame count selected with SF0TFIC bit of SF0INTC register, SF0TFI bit of SF0SRR register is set and occurs a transmission interrupt.
- Reception FIFO threshold
  If the number of data received in the reception FIFO is equal to or more than following the frame count selected with SF0RFIC bit of SF0CR register, SF0RFI bit of SF0SRR register is set and occurs a reception interrupt.
- Transfer completion
  If the transmission FIFO becomes empty and the transfer of the last frame is completed, SF0FI bit of SF0SRR register is set and occur a transfer completion interrupt.

12.3.14.2 Clearing SSIOF Interrupt

An interrupt request is cleared by writing 1 to each interrupt bit (SF0TFC, SF0RFC, SF0FC, SF0ORFC, SF0MDFC, SF0SPIFC, and SF0WOFC) of the SF0SRC .

12.3.14.3 SSIOF Interrupt Timing

Figure 12-11 shows the interrupt timing.
The transmission interrupt (TFI) generates an interrupt in 3 to 4 SYSCLK after the shift clock of the second bit in the master mode, in 3 to 5 SYSCLK after the shift clock of the second bit in the slave mode.
For reception interrupt (RFI), transfer completion interrupt (FI), and overrun (ORF), an interrupt occurs in 2 to 3 SYSCLK after the sampling clock at the MSB in the master mode, in 2 to 4 SYSCLK after the sampling clock at the MSB in the slave mode.

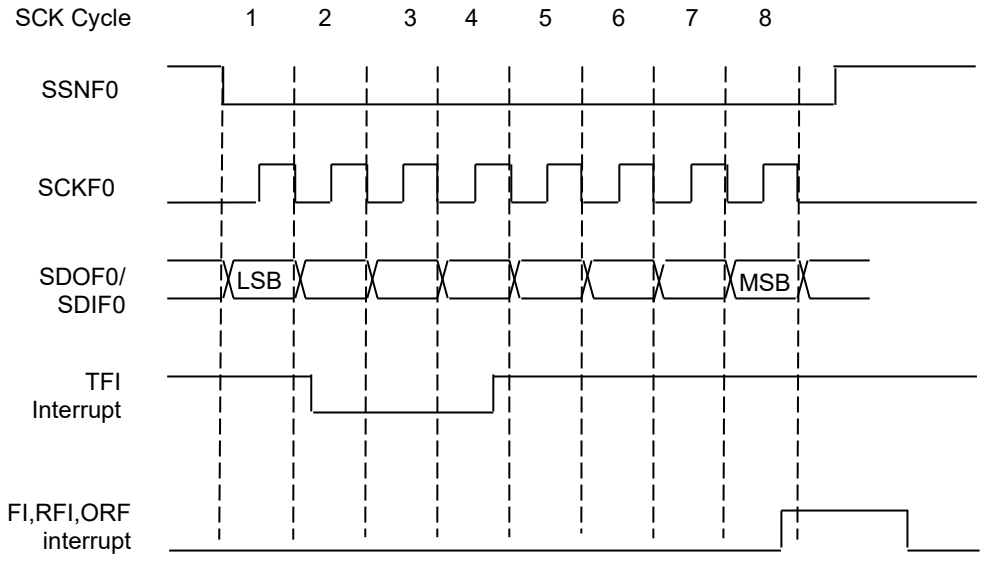


Figure 12-11 Interrupt Timing

12.3.14.4 Interrupt processing flow

Figure 12-12 show the processing flow in the receiving operation of the slave mode.

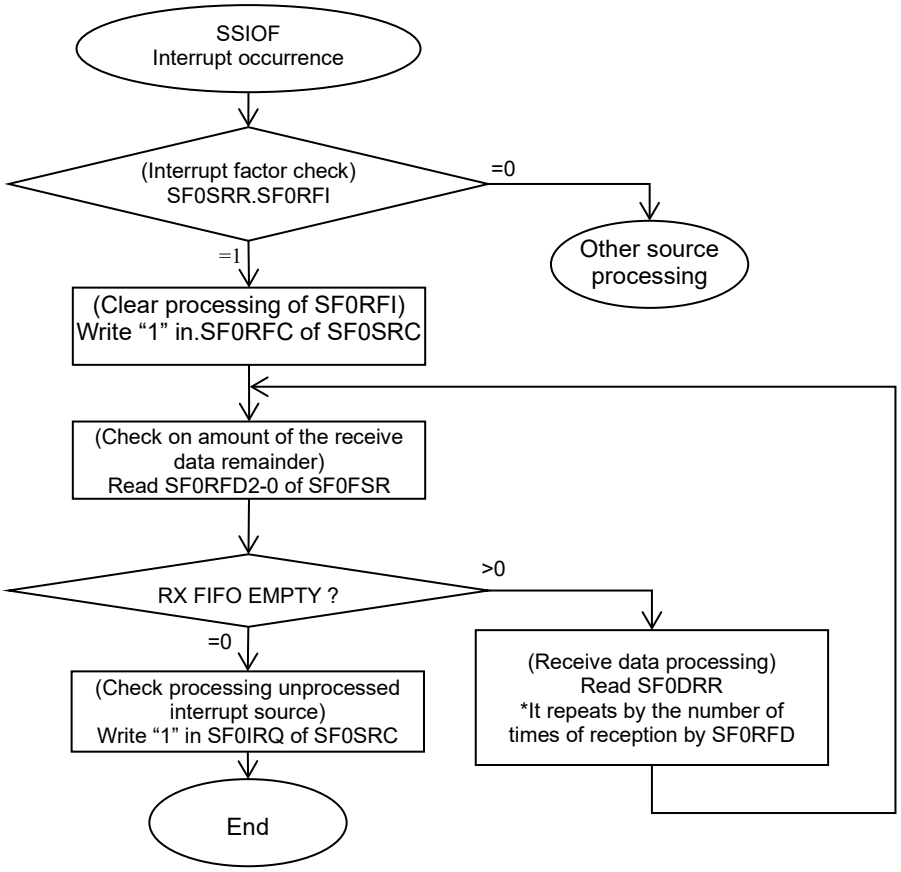


Figure 12-12 Example of the interrupt control flow

Chapter 13 I^2C Bus

13. I²C Bus

13.1 General Description

ML62Q2700 group where complies with I²C specifications has one channel of I²C bus unit that supports both master and slave function and two channels of I²C bus master that support only the master function.
I²C bus unit is used by selecting either the master function or the slave function. The master function and the slave functions cannot be used at the same time.

13.1.1 Features

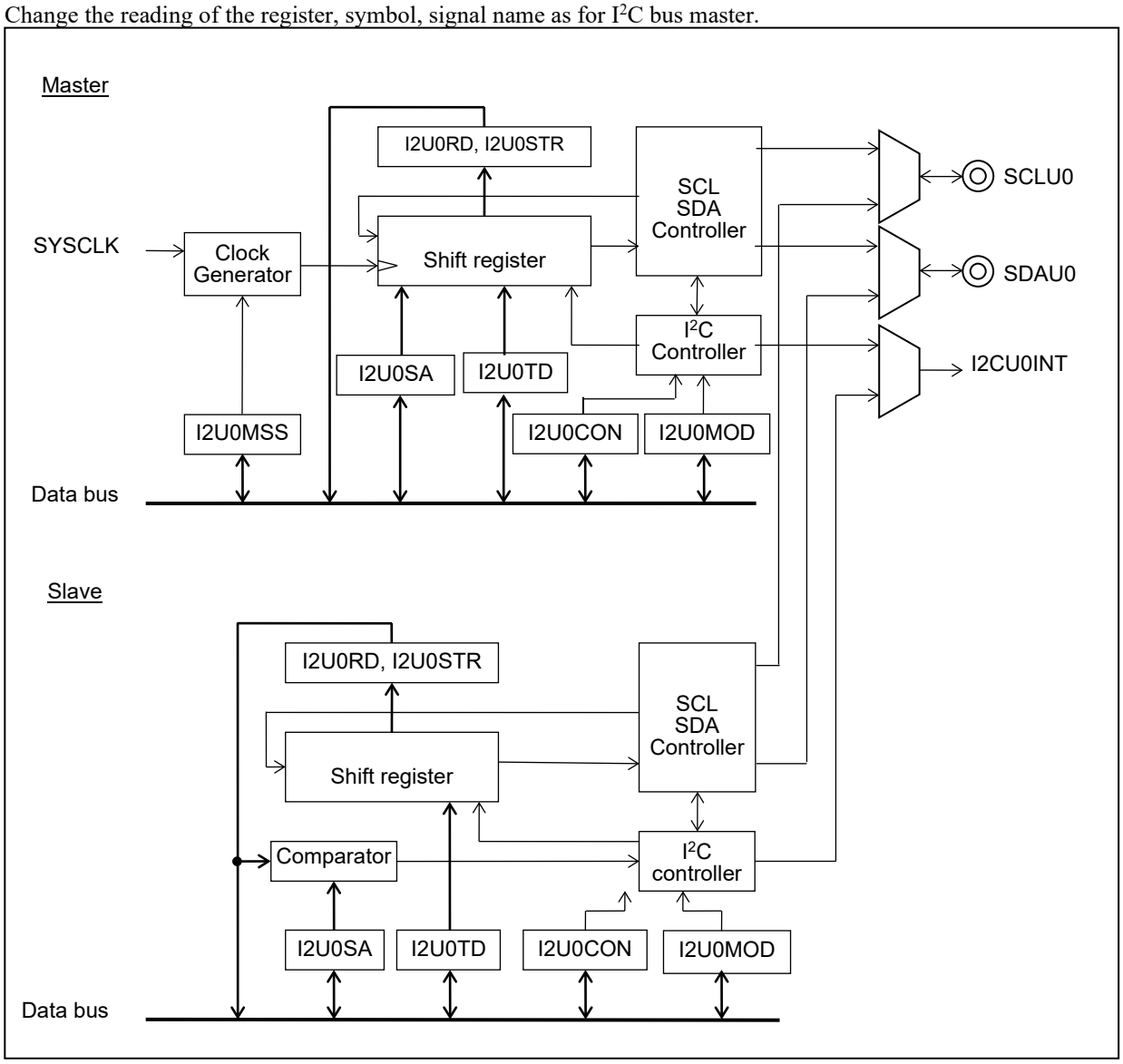
Table 13-1 shows features of I²C bus unit and I²C bus master.

Table 13-1 Features of I²C bus

Function	Operation mode	Features
I²C bus unit	Master function	- Communication speed: Standard mode (100 kbps), fast mode (400 kbps), and a proprietary standard 1 Mbps mode (1Mbps) - Support clock stretch function for the Slave - 7-bit address format (allows 10-bit address format) - Self-test function by reading data transmitted to the I²C bus (Safety function)
	Slave function	- Communication speed: Standard mode (100 kbps), fast mode (400 kbps), and proprietary standard 1 Mbps mode (1Mbps) - Clock stretch function - 7-bit address format - Wake-up from STOP/STOP-D/HALT-D mode by matching slave address
I²C bus master	Master function only	- Communication speed: Standard mode (100 kbps), fast mode (400 kbps), and proprietary standard 1 Mbps mode (1Mbps) - Support clock stretch function for the Slave - 7-bit address format (allows 10-bit address format) - Self-test function by reading data transmitted to the I2C bus (Safety function)

13.1.2 Configuration

Figure 13-1 shows the configuration diagram of the I²C bus unit circuit.
Change the reading of the register, symbol, signal name as for I²C bus master.



SCLU0 : Serial clock
SDAU0 : Serial data
I2U0MSS : I²C bus unit 0 mode register
I2U0RD : I²C bus unit 0 receive register
I2U0SA : I²C bus unit 0 slave address register
I2U0TD : I²C bus unit 0 transmit data register
I2U0CON : I²C bus unit 0 control register
I2U0MOD : I²C bus unit 0 mode register
I2U0STR : I²C bus unit 0 status register
I2U0SCLR : I²C bus unit 0 status clear register

Figure 13-1 Configuration of I²C Bus Unit

13.1.3 List of Pins

The I/O pins of the I²C bus unit are assigned to the shared function of the general ports.

Pin name	I/O	Description
SDAU0	I/O	I²C bus unit 0 data I/O pin
SCLU0	I/O	I²C bus unit 0 clock I/O pin
SDAM0	I/O	I²C bus master n data I/O pin
SCLM0	I/O	I²C bus master n clock I/O pin

(n = 0 to 7)

Table 13-2 shows port used in the I²C and the register settings.
In addition to the mode setting of the shared function, choose "Enable Input, Enable Output, N-ch open drain output and without pull-up" by setting following data to the port n mode register m (PnMODm).

Table 13-2 Port used in the I²C and the register settings

Channel No.	Pin name	General port		Setting register	Setting value	ML62Q2700 group				
						48pin product	52pin product	64pin product	80pin product	100pin product
0	SDAU0	P03	4th function	P0MOD3	0011_1011	●	●	●	●	●
		P15	4th function	P1MOD5	0011_1011	●	●	●	●	●
		P26	4th function	P2MOD6	0011_1011	●	●	●	●	●
		P46	4th function	P4MOD6	0011_1011	-	-	●	●	●
	SCLU0	P02	4th function	P0MOD2	0011_1011	●	●	●	●	●
		P04	4th function	P0MOD4	0011_1011	●	●	●	●	●
		P16	4th function	P1MOD6	0011_1011	●	●	●	●	●
		P27	4th function	P2MOD7	0011_1011	●	●	●	●	●
		P47	4th function	P4MOD7	0011_1011	-	-	●	●	●
	SDAM0	P06	4th function	P0MOD6	0011_1011	●	●	●	●	●
		P22	4th function	P2MOD2	0011_1011	●	●	●	●	●
	SCLM0	P07	4th function	P0MOD7	0011_1011	●	●	●	●	●
		P23	4th function	P2MOD3	0011_1011	●	●	●	●	●
	SDAM1	P61	4th function	P6MOD1	0011_1011	●	●	●	●	●
	SCLM1	P60	4th function	P6MOD0	0011_1011	●	●	●	●	●

●: Available -: Not available

13.1.4 Combination of I²C Bus Port

SDAU0/SCLU0/SDAMn/SCLMn pins are assigned to multiple general ports.
Be sure to use the ports in following combinations.

Combination	Peripheral circuit	Channel No.	IO pin		ML62Q2700 group				
			SDAU0/ SDAMn	SCLU0/ SCLMn	48pin product	52pin product	64pin product	80pin product	100pin product
1	I²C BUS unit	0	P03	P04	●	●	●	●	●
2			P15	P16	●	●	●	●	●
3			P26	P27	●	●	●	●	●
4			P03	P02	●	●	●	●	●
5			P46	P47	-	-	●	●	●
6	I²C BUS master	0	P06	P07	●	●	●	●	●
7			P22	P23	●	●	●	●	●
8		1	P61	P60	●	●	●	●	●

n=0 to 1

●: Available -: Not available

[Note]

- **Connect appropriate External pull-up resistors to SDAU0 pin, SCLU0, SDAMn, and SCLMn1 pins according to the I²C bus specification. The internal pull-up resistors does not meet the I²C bus specification. See the data sheet for the value of internal pull-up resistors.**
- **If power off this LSI during slave mode is in use, it disables communications of other devices on the I²C bus. Keep this LSI powered on while it works as a slave mode until the master device is powered off.**
- **Do not connect multiple master devices on the I²C bus when using the master function.**

13.2 Description of Registers

13.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF780	I²C bus unit 0 mode register	I2U0MSS	-	R/W	8	0x00
0xF781	Reserved register	-	-	-	-	-
0xF782	I²C bus unit 0 receive register	I2U0RD	-	R	8	0x00
0xF783	Reserved register	-	-	-	-	-
0xF784	I²C bus unit 0 slave address register	I2U0SA	-	R/W	8	0x00
0xF785	Reserved register	-	-	-	-	-
0xF786	I²C bus unit 0 transmit data register	I2U0TD	-	R/W	8	0x00
0xF787	Reserved register	-	-	-	-	-
0xF788	I²C bus unit 0 control register	I2U0CON	-	R/W	8	0x00
0xF789	Reserved register	-	-	-	-	-
0xF78A	I²C bus unit 0 mode register	I2U0MODL	I2U0MOD	R/W	8/16	0x00
0xF78B		I2U0MODH		R/W	8	0x02
0xF78C	I²C bus unit 0 status register	I2U0STAT	I2U0STR	R	8/16	0x00
0xF78D		I2U0ISR		R	8	0x00
0xF78E	I²C bus unit 0 status clear register	I2U0SCLRL	I2U0SCLR	W	8/16	0x00
0xF78F		I2U0SCLRH		W	8	0x00
0xF790 to 0xF7C1	Reserved register	-	-	-	-	-
0xF7C2	I²C bus master 0 receive register	I2M0RD	-	R	8	0x00
0xF7C3	Reserved register	-	-	-	-	-
0xF7C4	I²C bus master 0 slave address register	I2M0SA	-	R/W	8	0x00
0xF7C5	Reserved register	-	-	-	-	-
0xF7C6	I²C bus master 0 transmit data register	I2M0TD	-	R/W	8	0x00
0xF7C7	Reserved register	-	-	-	-	-
0xF7C8	I²C bus master 0 control register	I2M0CON	-	R/W	8	0x00
0xF7C9	Reserved register	-	-	-	-	-
0xF7CA	I²C bus master 0 mode register	I2M0MODL	I2M0MOD	R/W	8/16	0x00
0xF7CB		I2M0MODH		R/W	8	0x02
0xF7CC	I²C bus master 0 status register	I2M0STAT	I2M0STR	R	8/16	0x00
0xF7CD		I2M0ISR		R	8	0x00
0xF7CE	I²C bus master 0 status clear register	I2M0SCLRL	I2M0SCLR	W	8/16	0x00
0xF7CF		I2M0SCLRH		W	8	0x00
0xF7D0	Reserved register	-	-	-	-	-
0xF7D1	Reserved register	-	-	-	-	-
0xF7D2	I²C bus master 1 receive register	I2M1RD	-	R	8	0x00
0xF7D3	Reserved register	-	-	-	-	-
0xF7D4	I²C bus master 1 slave address register	I2M1SA	-	R/W	8	0x00
0xF7D5	Reserved register	-	-	-	-	-
0xF7D6	I²C bus master 1 transmit data register	I2M1TD	-	R/W	8	0x00
0xF7D7	Reserved register	-	-	-	-	-
0xF7D8	I²C bus master 1 control register	I2M1CON	-	R/W	8	0x00
0xF7D9	I²C bus master 1 receive register	-	-	-	-	-
0xF7DA	I²C bus master 1 mode register	I2M1MODL	I2M1MOD	R/W	8/16	0x00
0xF7DB		I2M1MODH		R/W	8	0x02
0xF7DC	I²C bus master 1 status register	I2M1STAT	I2M1STR	R	8/16	0x00
0xF7DD		I2M1ISR		R	8	0x00
0xF7DE	I²C bus master 1 status clear register	I2M1SCLRL	I2M1SCLR	W	8/16	0x00

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF7DF		I2M1SCLRH		W	8	0x00
0xF7E0	Reserved register	-	-	-	-	-
0xF7E1	Reserved register	-	-	-	-	-

13.2.2 I²C Bus Unit 0 Mode Register (I2U0MSS)

I2U0MSS is a SFR to select the Master mode or Slave mode of the I2C bus unit 0.

Address : 0xF780 (I2U0MSS)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0MSS							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	I2U0MD
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	I2U0MD	Select the Master mode or Slave mode of the I²C but unit. 0: Master mode (Initial value) 1: Slave mode

[Note]

- **All SFRs are shared in master mode and slave mode. If switching master/slave mode, stop the operation by setting "0" to I2U0EN bit of I2UMOD register, then change the mode and reconfigure each SFRs.**
- **When using the master function, do not connect multiple master devices on the I²C bus.**
- **If power of this LSI is cut off during slave mode is in use, it disables communications of other devices on the I2C bus. Keep this LSI powered on while it works as a slave mode until the master device is powered off.**

13.3 Description of Registers for Master function

This section describes about master mode of I²C bus unit and I²C bus master.
In this section, word symbol, byte symbol and bit symbol are write down with.
A prefix of symbol for I²C bus unit 0 is I2U. A prefix of symbol for I²C bus master 0 is I2M.
All SFRs are shared in master mode and slave mode. Set master mode in I2U0MSS register in advance.

13.3.1 I²C Bus Unit 0 Receive Register (I2U0RD), I²C Bus Master 0 Receive Register (I2M0RD)

I2U0RD and I2M0RD are read-only SFR used to store the received data.
These are initialized by reset function and by writing "0" to I2U0EN/I2M0EN bit in I2U0MOD/I2M0MOD register.

Address : 0xF782(I2U0RD), 0xF7C2(I2M0RD)
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0RD							
Bit	-	-	-	-	-	-	-	-	I2U0R7	I2U0R6	I2U0R5	I2U0R4	I2U0R3	I2U0R2	I2U0R1	I2U0R0
Word	-															
Byte	-								I2M0RD							
Bit	-	-	-	-	-	-	-	-	I2M0R7	I2M0R6	I2M0R5	I2M0R4	I2M0R3	I2M0R2	I2M0R1	I2M0R0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 0	I2U0R7 to I2U0R0/ I2M0R7 to I2M0R0	Store the received data. Slave address data is received when the slave address matches. The data is updated at coinciding slave-address and data reception. The data is updated after completion of each reception. Reading this register enables the following confirmation. - Read out the data received ➢ Confirm the received data. - Read out the slave address or the transmitting data: ➢ Verify the transmission data was surely transmitted.

13.3.2 I²C Bus Unit 0 Slave Address Register (I2U0SA), I²C Bus Master 0 Slave Address Register (I2M0SA)

I2U0SA and I2M0SA are SFR to set the address and transmission/reception mode of the slave device.
These are initialized by reset function and by writing "0" to I2U0EN/I2M0EN bit in I2U0MOD/I2M0MOD register.

Address : 0xF784(I2U0SA), 0xF7C4(I2M0SA)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0SA							
Bit	-	-	-	-	-	-	-	-	I2U0A6	I2U0A5	I2U0A4	I2U0A3	I2U0A2	I2U0A1	I2U0A0	I2U0RW
Word	-															
Byte	-								I2M0SA							
Bit	-	-	-	-	-	-	-	-	I2M0A6	I2M0A5	I2M0A4	I2M0A3	I2M0A2	I2M0A1	I2M0A0	I2M0RW
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	I2U0A6 to I2U0A0/ I2M0A6 to I2M0A0	Set the address of the slave to be communicated.
0	I2U0RW/ I2M0RW	Select the direction of the data communication. 0: Data transmission mode (Initial value) 1: Data reception mode

13.3.3 I²C Bus Unit 0 Transmit Data Register (I2U0TD), I²C Bus Master 0 Transmit Data Register (I2M0TD)

I2U0TD and I2M0TD are SFR to set the transmission data.
These are initialized by reset function and by writing "0" to I2U0EN/I2M0EN bit in I2U0MOD/I2M0MOD register.

Address : 0xF786(I2U0TD), 0xF7C6(I2M0TD)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0TD							
Bit	-	-	-	-	-	-	-	-	I2U0T7	I2U0T6	I2U0T5	I2U0T4	I2U0T3	I2U0T2	I2U0T1	I2U0T0
Word	-															
Byte	-								I2M0TD							
Bit	-	-	-	-	-	-	-	-	I2M0T7	I2M0T6	I2M0T5	I2M0T4	I2M0T3	I2M0T2	I2M0T1	I2M0T0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 0	I2U0T7 to I2U0T0/ I2M0T7 to I2M0T0	Set the transmission data.

13.3.4 I²C Bus Unit 0 Control Register (I2U0CON), I²C Bus Master 0 Control Register (I2M0CON)

I2U0CON and I2M0CON are SFR to control transmission and reception operations.
These are initialized by reset function and by writing “0” to I2U0EN/I2M0EN bit in I2U0MOD/I2M0MOD register.

Address : 0xF788(I2U0CON), 0xF7C8(I2M0CON)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0CON							
Bit	-	-	-	-	-	-	-	-	I2U0ACT	-	-	-	-	I2U0RS	I2U0SP	I2U0ST
Word	-															
Byte	-								I2M0CON							
Bit	-	-	-	-	-	-	-	-	I2M0ACT	-	-	-	-	I2M0RS	I2M0SP	I2M0ST
R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R	W	W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7	I2U0ACT/ I2M0ACT	Set the acknowledgment data to be output at completion of reception. 0: Acknowledgment data "0" (Initial value) 1: Acknowledgment data "1"
6 to 3	-	Reserved bits
2	I2U0RS/ I2M0RS	Write-only bit, and it requests restart. When "1" is written to this bit during data communication, enter to the restart condition, and the communication restarts from the slave address. "1" can be written to this bit only while communication is active (I2U0ST /I2M0ST = "1"). This bit always returns "0" for reading. 0: No restart request (Initial value) 1: Restart request
1	I2U0SP/ I2M0SP	Write-only bit, and it requests stop condition. When "1" is written to this bit, the module shifts to the stop condition and the communication stops. This bit always returns "0" for reading. 0: No stop condition request (Initial value) 1: Stop condition request
0	I2U0ST/ I2M0ST	Control the communication operation of this module. When "1" is written to this bit during I2U0ST/I2M0ST bit is “0”, the communication starts. When "1" is overwritten to this bit in a next data transmission/reception wait state after transmission/reception of acknowledgment, the data transmission/reception restarts. When "0" is written to this bit, the communication is stopped forcibly. When "1" is written to this bit, the I2U0ST/I2M0ST bit is reset to “0”. 0: Stops communication (Initial value) 1: Starts communication

[Note]
- **Update I2U0ACT/I2MnACT without bit access instructions in the control register setting wait state.**
- **When the I2U0ST/I2M0ST bit is "1", write other bits of I2U0CON/I2M0CON register in the control register setting wait state.**

13.3.5 I²C Bus Unit 0 Mode Register (I2U0MOD), I²C Bus Master 0 Mode Register (I2M0MOD) (I2MnMOD : n=0 to 1)

I2U0MOD and I2M0MOD are SFR to set the operation mode.
See Table 13-3 in "13.5.4 Operation Waveforms" for detail of communication speed.

Address : 0xF78A(I2U0MODL/I2U0MOD), 0xF78B(I2U0MODH),
0xF7CA(I2M0MODL/I2M0MOD), 0xF7CB(I2M0MODH)
0xF7DA(I2M1MODL/I2M0MOD), 0xF7DB(I2M1MODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0200

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	I2U0MOD															
Byte	I2U0MODH								I2U0MODL							
Bit	I2U0TI2	I2U0TI1	I2U0TI0	-	-	-	I2U0CD1	I2U0CD0	-	-	I2U0MD4	I2U0MD3	I2U0MD2	I2U0MD1	I2U0MD0	I2U0EN
Word	I2M0MOD															
Byte	I2M0MODH								I2M0MODL							
Bit	I2M0TI2	I2M0TI1	I2M0TI0	-	-	-	I2M0CD1	I2M0CD0	-	-	I2M0MD4	I2M0MD3	I2M0MD2	I2M0MD1	I2M0MD0	I2M0EN
R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 13	I2U0TI2 to I2U0TI0/ I2M0TI2 to I2M0TI0	Select the timing parameter for the I²C communication rate. Select one which frequency will be less than or equal to the system clock. 000: parameter for SYSCLK = 24MHz (Initial value) 001: parameter for SYSCLK = 16MHz 010: parameter for SYSCLK = 12MHz 011: parameter for SYSCLK = 8MHz 100: parameter for SYSCLK = 1MHz 101: parameter for SYSCLK = LSCLK0 110: Not use (for SYSCLK = 24MHz) 111: Not use (for SYSCLK = 24MHz)
12 to 10	-	Reserved bits
9 to 8	I2U0CD1 to I2U0CD0/ I2M0CD1 to I2M0CD0	Select the I²C operation clock. 00: SYSCLK 01: 1/2 SYSCLK 10: 1/4 SYSCLK (Initial value) 11: 1/8 SYSCLK See "13.5.4 Operation Waveforms" about communication speed.
7, 6	-	Reserved bits
5	I2U0MD4/ I2M0MD4	Select whether the clock stretch (handshake) function is used or not. When this function is used, the I²C bus is monitored. Therefore, the communication speed decreases depending on the load on the I²C bus. 0: Not use the clock stretch function (Initial value) 1: Use the clock stretch function
4, 3	I2U0MD3, I2U0MD2/ I2M0MD3, I2M0MD2	Set the I²C Bus unit communication speed reduction rate. Adjust the communication speed by these bits to not to exceed the speed configured by I2U0MD1, I2U0MD0 bit / I2MnMD1, I2MnMD0 bit as 100kbps/400kbps/1Mbps. When the parameter for LSCLK0 or 1MHz is selected by the I2U0TI2-0/I2M0TI2-0 bits, "No communication speed reduction" is selected regardless this setting. See Table 13-3 of "13.5.4 Operation Waveforms" for detail. 00: No communication speed reduction (Initial value) 01: Approx. 10% reduction of communication speed 10: Approx. 17% reduction of communication speed 11: Approx. 24% reduction of communication speed

Bit No.	Bit symbol name	Description
2, 1	I2U0MD1, I2U0MD0/ I2M0MD1, I2M0MD0/	Set the communication speed mode. 00: Standard mode (Initial value) (100 kbps*) 01: Fast mode (400 kbps*) 10: 1Mbps mode (1Mbps*) 11: 1Mbps mode (1Mbps*) * : When System clock=24 or 16 MHz and I2U0CD1-0/I2M0CD1-0 = “00” and I2U0MD4/I2M0MD4 = “0” and I2U0TI2-0/I2M0TI2-0 = “000/001” and I2U0MD3-2/I2M0MD3-2 = “00”.
0	I2U0EN/ I2M0EN	Enable the master operation. When "1" is written to I2U0EN/I2NnST bit, start I2C master operation, and then I2U0ST/I2M0ST bits becomes configurable. When "0" is written to this bit, the I²C master stops operation and the I2U-RD/I2M0RD, I2U0SA/I2M0SA, I2U0TD/I2M0TD, I2U0CON/I2M0CON and I2U0STR/I2M0STR are initialized. If “0” is written to I2U0EN/I2MnEN during the communication, and stop the operation, initialize and re-setting I²C Bus unit /I²C Bus master. 0: Stop the I²C master operation (Initial value) 1: Enable the I²C master operation

13.3.6 I²C Bus Unit 0 Status Register (I2U0STR), I²C Bus Master 0 Status Register (I2M0STR)

I2U0STR and I2M0STR are SFR to indicate the state of the I²C bus unit / master.
These are initialized by reset function and by writing “0” to I2U0EN/I2M0EN bit in I2U0MOD/I2M0MOD register.
Each bit is also initialized to "0" by writing "1" to the corresponding bit in the I2U0SCLR/I2MnSCLR register.

Address : 0xF78C(I2U0STAT/I2U0STR), 0xF78D(I2U0ISR)
0xF7CC(I2M0STAT/I2M0STR), 0xF7CD(I2M0ISR)
0xF7DC(I2M1STAT/I2M1STR), 0xF7DD(I2M1ISR)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	I2U0STR															
Byte	I2U0ISR								I2U0STAT							
Bit	-	-	-	-	-	I2U0SPS	I2U0DS	I2U0AS	rsvd	-	-	-	-	I2U0ER	I2U0ACR	-
Word	I2M0STR															
Byte	I2M0ISR								I2M0STAT							
Bit	-	-	-	-	-	I2M0SPS	I2M0DS	I2M0AS	rsvd	-	-	-	-	I2M0ER	I2M0ACR	-
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 11	-	Reserved bits
10	I2U0SPS/ I2M0SPS	Indicate the usage status of the I²C bus. These bits are set to "1" when transmitting the stop condition on the I²C bus. To reset these bits to “0”, write "1" to I2U0CSPS/ I2M0CSP bit of I2U0SCLR/I2M0SCLR register. 0: The stop condition has not been transmitted (Initial value) 1: The stop condition has been transmitted
9	I2U0DS/ I2M0DS	Indicate the usage state of the I²C bus. These bits are set to "1" when transmitting data or receiving data has been completed on the I²C bus. To reset these bits to “0”, write "1" toI2U0CDS/ I2M0CDS bit of I2U0SCLR/I2M0SCLR register. 0: The transmission/reception has not been completed (Initial value) 1: The transmission/reception has been completed
8	I2U0AS/ I2M0AS	Indicate the usage state of the I²C bus. These bits are set to "1" when transmitting the start condition and 7bit slave address have been completed on the I²C bus. To reset these bits to “0”, write "1" to I2U0CAS/ I2M0CAS bit of I2U0SCLR/I2M0SCLR register. 0: The start condition and the slave address have not been transmitted (Initial value) 1: The start condition and the slave address have been transmitted
7	rsvd	Reserved bit
6 to 3	-	Reserved bits
2	I2U0ER/ I2M0ER	Indicate a transmission error. When a bit of transmission data does not coincide with the value on SDAU0/SDAM0 pin, "1" is set to these bits. To reset these bits to “0”, write "1" to I2U0CER/ I2M0CER bit of I2U0SCLR/I2M0SCLR register. When these bits are set to "1" and the clock stretch function is used (I2U0MD4/ I2M0MD4 = "1"), SDAU0/SDAM0 pin output is disabled until the subsequent byte data communication terminates. Even if these bits are set to "1" and the clock stretch function is not used (I2U0MD4/ I2M0MD4 = "0"), SDAU0/SDAM0 pin output continues until the subsequent byte data communication terminates. 0: There was no transmission error (Initial value) 1: There was a transmission error

Bit No.	Bit symbol name	Description
1	I2U0ACR/ I2M0ACR	Store the acknowledgment signal received. Acknowledgment signals are received for each slave address is transmitted and the data transmission/reception is completed. To reset these bits, write "1" to I2U0CACR/ I2M0CACR bit of I2U0SCLR/I2M0SCLR register.. 0: Received acknowledgment "0" (Initial value) 1: Received acknowledgment "1"
0	-	Reserved bit

13.3.7 I²C Bus Unit 0 Status Clear Register (I2U0SCLR), I²C Bus Master 0 Status Clear Register (I2M0SCLR)

I2U0SCLR and I2M0SCLR are SFR to clear the state of the I²C bus unit / master.
When Each bit is written "1", a corresponding bit of I2U0STR/I2M0STR register is initialized to "0".

Address : 0xF78E(I2U0SCLRL/I2U0SCLR), 0xF78F(I2U0SCLRH)
0xF7CE(I2M0SCLRL/I2M0SCLR), 0xF7CF(I2M0SCLRH)
0xF7DE(I2M1SCLRL/I2M1SCLR), 0xF7DF(I2M1SCLRH)
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	I2U0SCLR															
Byte	I2U0SCLRH								I2U0SCLRL							
Bit	-	-	-	-	-	I2U0CSPS	I2U0CDS	I2U0CAS	-	-	-	-	-	I2U0CER	I2U0CACR	-
Word	I2M0SCLR															
Byte	I2M0SCLRH								I2M0SCLRL							
Bit	-	-	-	-	-	I2M0CSPS	I2M0CDS	I2M0CAS	-	-	-	-	-	I2M0CER	I2M0CACR	-
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is used to clear an applicable status.
Writing "0": Invalid
Writing "1": clear a target interrupt

Bit No.	Bit symbol name	Description (target)
15 to 11	-	Reserved bits
10	I2U0CSPS/ I2M0CSPS	I2U0SPS bit of I2U0STR register/ I2M0SPS bit of I2M0STR register
9	I2U0CDS/ I2M0CDS	I2U0DS bit of I2U0STR register/ I2M0DS bit of I2M0STR register
8	I2U0CAS/ I2M0CAS	I2U0AS bit of I2U0STR register/ I2M0AS bit of I2M0STR register
7 to 3	-	Reserved bits
2	I2U0CER/ I2M0CER	I2U0ER bit of I2U0STR register/ I2M0ER bit of I2M0STR register
1	I2U0CACR/ I2M0CACR	I2U0ACR bit of I2U0STR register/ I2M0ACR bit of I2M0STR register
0	-	Reserved bit

13.4 Description of Registers for Slave function

This section describes about slave mode of I²C bus unit 0.
A prefix of symbol for I²C bus unit 0 is I2U. A prefix of symbol for I²C bus master 0 is I2M.
Set I²C bus unit to slave mode with I2U0MSS registers.
I²C bus master is fixed in master mode.

13.4.1 I²C Bus Unit 0 Receive Register (I2U0RD)

I2U0RD is a read-only SFR to store the received data.

Address : 0xF782(I2U0RD)
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0RD							
Bit	-	-	-	-	-	-	-	-	I2U0R7	I2U0R6	I2U0R5	I2U0R4	I2U0R3	I2U0R2	I2U0R1	I2U0R0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 0	I2U0R7 to I2U0R0	Store the received data. This data is updated at coinciding slave-address and data reception. Receive the data at coinciding slave-address and data reception. The data is updated every end of data reception. Reading this register enables following confirmation. - Reading when receiving data: Confirm the received data. - Reading when transmitting data: Confirm the transmission data is surely transmitted.

13.4.2 I²C Bus Unit 0 Slave Address Register (I2U0SA)

I2U0SA is a SFR to set the slave address.

Address : 0xF784(I2U0SA)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0SA							
Bit	-	-	-	-	-	-	-	-	I2U0A6	I2U0A5	I2U0A4	I2U0A3	I2U0A2	I2U0A1	I2U0A0	-
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	I2U0A6 to I2U0A0	Set the slave address when the slave mode is selected.
0	-	Reserved bit

13.4.3 I²C Bus Unit 0 Transmit Data Register (I2U0TD)

I2U0TD is a SFR to set the transmission data.

Address : 0x786(I2U0TD)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0TD							
Bit	-	-	-	-	-	-	-	-	I2U0T7	I2U0T6	I2U0T5	I2U0T4	I2U0T3	I2U0T2	I2U0T1	I2U0T0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 0	I2U0T7 to I2U0T0	Set the transmission data when the slave mode is selected.

13.4.4 I²C Bus Unit 0 Control Register (I2U0CON)

I2U0CON is a SFR to control transmission and reception operations.

Address : 0xF788(I2U0CON)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								I2U0CON							
Bit	-	-	-	-	-	-	-	-	I2U0ACT	-	I2U0WT	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R	R/W	R	W	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7	I2U0ACT	Set the acknowledgment data to be output at completion of reception in the slave mode. 0: Acknowledgment data "0" (Initial value) 1: Acknowledgment data "1"
6	-	Reserved bit
5	I2U0WT	Release the communication wait state ("L" level output on the SCLU0 pin) in the slave mode. Writing "1" to this bit during the communication wait state releases the state ("L" level output of the SCLU0 pin is released). This bit is a write-only bit and always returns "0" for reading. 0: Not release the communication wait state (Initial value) 1: Release the communication wait state
4 to 0	-	Reserved bits

[Note]
- **If system clock is extremely slower than the communication speed, the data transmission/reception may not be succeeded.**
- **Before releasing the communication wait state, set the system clock speed to appropriate speed for the communication.**

13.4.5 I²C Bus Unit 0 Mode Register (I2U0MOD)

I2U0MOD is a SFR to set the operation mode.

Address : 0xF78A(I2U0MODL/I2U0MOD), 0xF78B(I2U0MODH),
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	I2U0MOD															
Byte	I2U0MODH								I2U0MODL							
Bit	-	-	-	-	-	-	-	-	-	I2U0MD5	I2U0MD4	I2U0MD3	I2U0MD2	I2U0MD1	-	I2U0EN
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 7	-	Reserved bits
6	I2U0MD5	Enable or disable the start condition interrupt in the slave mode. 0: Disabled (Initial value) 1: Enabled
5	I2U0MD4	Enable or disable the stop condition interrupt in the slave mode. 0: Disabled (Initial value) 1: Enabled
4	I2U0MD3	Enable or disable the interrupt when another slave is selected under restart conditions when communicating with the master. This is executed by detecting the I2US0SAA bit state. When enabling the interrupt by setting I2U0MD3 to “1”, do not clear the I2US0SAA bit by the software. 0: Disabled (Initial value) 1: Enabled
3	I2U0MD2	Enables or disables the communication waiting function of the I²C bus unit ("L" level output to the SCLU0 pin) function when acknowledging data "1" is received from the master when transmitting to the master. Set this bit to "1" to release the communication wait state ("L" level output to the SCLU0 pin). 0: Disabled (Initial value) 1: Enabled
2	I2U0MD1	Enable the slave operation of the I²C Bus unit. This is executed by detecting the I2US0SAA bit state. When enabling the interrupt by setting I2U0MD3 to “1”, do not clear the I2US0SAA bit by the software. 0: The interrupt occurs while the master is communicating with self-slave or other slaves (Initial value) 1: The interrupt occurs while the master is communicating with only self-slave
1	-	Reserved bit
0	I2U0EN	Enable the slave operation of the I²C bus unit. Writing "1" to the I2U0EN bit enables I²C bus 0 operation. Writing "0" to this bit, all the bits of the I²C bus status register (I2US0STR) are initialized to "0", and the operation of the I²C bus unit 0 is stopped. 0: Stop the I²C slave operation (Initial value) 1: Enable the I²C slave operation

[Note]

- **In case if disabling the waking up from STOP mode/STOP-D mode/HALT-D mode by slave address matching, stop operation by setting I2U0EN to "0" before switching to STOP mode/STOP-D mode/HALT-D mode.**

13.4.6 I²C Bus Unit 0 Status Register (I2U0STR)

I2U0STR is a SFR to indicate the state of the I²C bus unit.
Each bit is initialized by reset function and by writing “0” to I2U0EN/I2M0EN bit in I2U0MOD/I2M0MOD register.

Address : 0xF78C(I2U0STAT/I2U0STR), 0xF78D(I2U0ISR)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	I2U0STR															
Byte	I2U0ISR								I2U0STAT							
Bit	-	-	I2U0ASNA	I2U0RAS	I2U0STS	I2U0SPS	I2U0DS	I2U0AS	-	-	-	I2U0TR	I2U0SAA	I2U0ER	I2U0ACR	-
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 14	-	Reserved bits
13	I2U0ASNA	Indicate that the acknowledgment "H" level is output even if the slave address coincident. It is set to "1" when canceled by slave address matching in STOP-D/HALT-D mode standby state. To reset this bit, write "1" to I2U0CASNA bit of I2U0SCLR register. 0: Not acknowledgment "H" level output by slave address match (initial value) 1: Acknowledgment "H" level output with slave address match
12	I2U0RAS	Indicate the status of the interrupt when enabling the start condition interrupt (I2U0MD3 bit = 1). To reset this bit, write "1" to I2U0CRAS bit of I2U0SCLR register. 0: Not unmatched the slave address is detected after the start condition (Initial value) 1: Unmatched the slave address is detected after the start condition
11	I2U0STS	Indicate the status of transmission and reception. This bit is set to "1" when receiving the start condition. This bit is reset to “0” by writing "1" to the I2U0CSTS bit of the I2U0SCLR register. This bit is enabled when I2U0MD5 bit is “1”. 0: Not reception completion status of start condition (Initial value) 1: Reception completion status of start condition
10	I2U0SPS	Indicate status of transmission and receive. This bit is set to "1" when receiving the stop condition. It is reset by writing "1" to the I2U0CSPS bit of the I2U0SCLR register. It is available when I2U0MD4 bit is “1”. To reset this bit, write "1" to I2U0CSPS bit of I2U0SCLR register. 0: Not reception completion status of stop condition (Initial value) 1: Reception completion status of stop condition
9	I2U0DS	Indicate status of transmission and reception. This bit is set to "1" when the data is transmitting/receiving while the slave addresses match. However, when waking up from STOP-D/HALT-D mode by slave address matching, "1" is not set even if the address matching. To reset this bit, write "1" to I2U0CDS bit of I2U0SCLR register. 0: Not transmission and reception completion status of the data (Initial value) 1: transmission and reception completion status of the data
8	I2U0AS	Indicate status of transmission and reception. This bit is set to "1" when the slave address is received and it matches. To reset this bit, write "1" to I2U0CAS bit of I2U0SCLR register. 0: Not reception completion status of slave address match (Initial value) 1: Reception completion status of slave address match
7 to 5	-	Reserved bits

Bit No.	Bit symbol name	Description
4	I2U0TR	Indicate the transmitting or receiving state. This bit is set to "1" when "1" (data reception mode) is detected in the R/W bit when receiving a slave address. This bit is reset to "0" when a stop condition is detected or "0" (data transmission mode) is detected in the R/W bit. To reset this bit, write "1" to I2U0CTR bit of I2U0SCLR register. 0: Receiving state (Initial value) 1: Transmitting state
3	I2U0SAA	Indicate that this LSI is specified as a slave address. This bit is set to "1" when the content of the slave address output by the master device coincides with the contents of I2US0SA register. However, when waking up from STOP-D/HALT-D mode by slave address matching, "1" is not set even if the address matching. Alternatively writing "1" to the I2U0CSAA bit of I2U0SCLR register resets it to "0". If the I2U0MD3 or I2U0MD1 bit is "1", do not clear it in software. 0: Not coincide with the slave address (Initial value) 1: Coincides with the slave address
2	I2U0ER	Indicate a transmission error. When the value of the bit transmitted and the value of the SDAU0 pin do not coincide, this bit is set to "1". When this bit is set to "1", the SDAU0 pin output is disabled until the subsequent byte data communication terminates. To reset this bit, write "1" toI2U0CER bit of I2U0SCLR register. 0: No transmission error (Initial value) 1: With transmission error
1	I2U0ACR	Store an acknowledgment signal received. The acknowledgment signal is received each time the slave address is transmitted and data transmission is completed.. To reset this bit, write "1" to I2U0CTR bit of I2U0SCLR register. 0: Received the acknowledgment "0" (Initial value) 1: Received the acknowledgment "1"
0	-	Reserved bit

13.4.7 I²C Bus Unit 0 Status Clear Register (I2U0SCLR)

I2U0SCLR is a SFR to clear the state of the I²C bus unit.
When Each bit is written "1", a corresponding bit of I2U0STR register is initialized to "0".

Address : 0xF78E(I2U0SCLRL/I2U0SCLR), 0xF78F(I2U0SCLRH)
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	I2U0SCLR															
Byte	I2U0SCLRH								I2U0SCLRL							
Bit	-	-	I2U0CASNA	I2U0CRAS	I2U0CSTS	I2U0CSPS	I2U0CDS	I2U0CAS	-	-	-	I2U0CTR	I2U0CSAA	I2U0CER	I2U0CACR	-
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is used to clear a target status.
Writing "0": Invalid
Writing "1": clear a target interrupt

Bit No.	Bit symbol name	Description (Target status)
15 to 14	-	Reserved bits
13	I2U0CASNA	I2U0ASNA bit of I2U0STR register
12	I2U0CRAS	I2U0RAS bit of I2U0STR register
11	I2U0CSTS	I2U0STS bit of I2U0STR register
10	I2U0CSPS	I2U0SPS bit of I2U0STR register
9	I2U0CDS	I2U0DS bit of I2U0STR register
8	I2U0CAS	I2U0AS bit of I2U0STR register
7 to 5	-	Reserved bits
4	I2U0CTR	I2U0TR bit of I2U0STR register
3	I2U0CSAA	I2U0SAA bit of I2U0STR register
2	I2U0CER	I2U0ER bit of I2U0STR register
1	I2U0CACR	I2U0ACR bit of I2U0STR register
0	-	Reserved bit

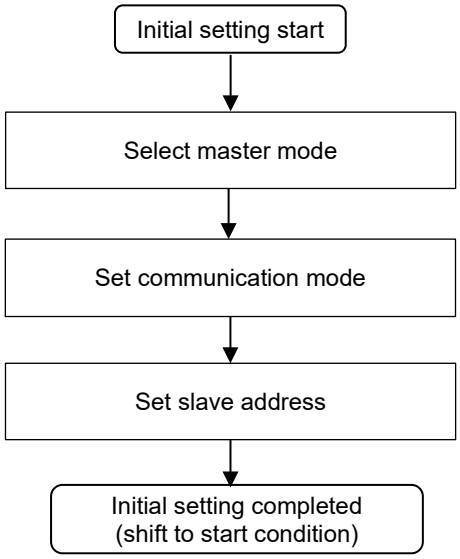
13.5 Description of Operation for Master function

The following explains for I²C bus unit 0. Change the reading of the register, symbol, signal name as for I²C bus master.

13.5.1 Control Procedures

The following flow charts describe procedures of each operation in the master mode.

13.5.1.1 Initial Setting of Communication Operation

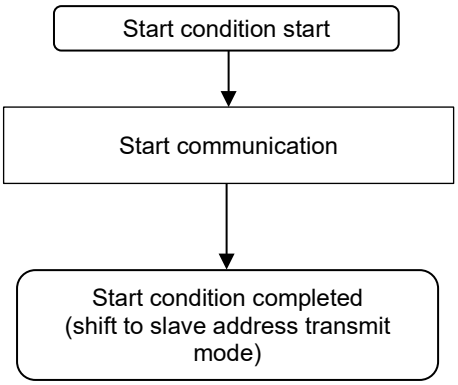


Set I2U0MD=0 in the I2U0MSS register

Set I2U0EN=1 in the I2U0MOD register

Set I2U0A6 to I2U0A0 bits and I2U0RW bit in the I2U0SA register

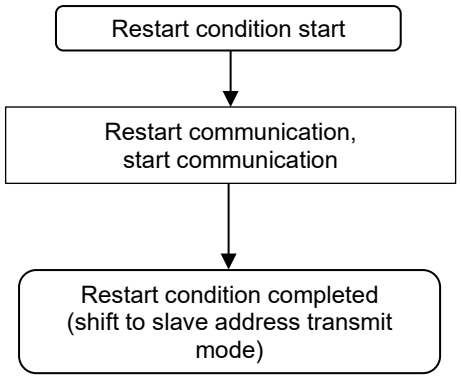
13.5.1.2 Start Condition



Set I2U0ST bit of I2U0CON register to “1”.

Output the start condition waveforms to SDAU0 and SCLU0 pins.

13.5.1.3 Restart Condition

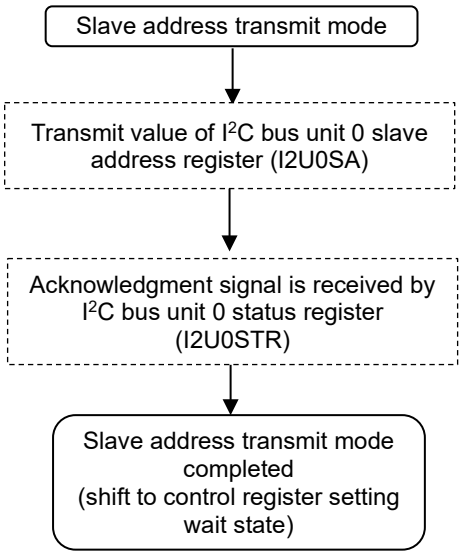


Communication in progress (I2U0ST=1)

Set I2U0RS=1 and I2U0ST=1 in the I2U0CON register

Output restart condition waveforms to SDAU0 and SCLU0 pins.

13.5.1.4 Slave Address Transmission Mode

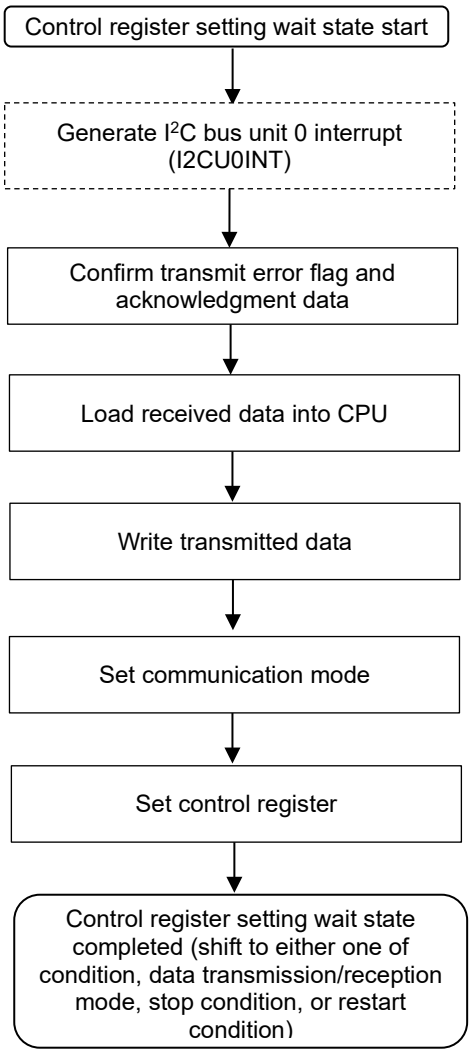


The value is transmitted from SDAU0 pin in MSB first through hardware following the start condition
I2U0A6 to I2U0A0 bits: Slave address
I2U0RW: Data direction (transmission/reception)
Value transmitted from the SDAU0 pin is stored in the I2U0RD register

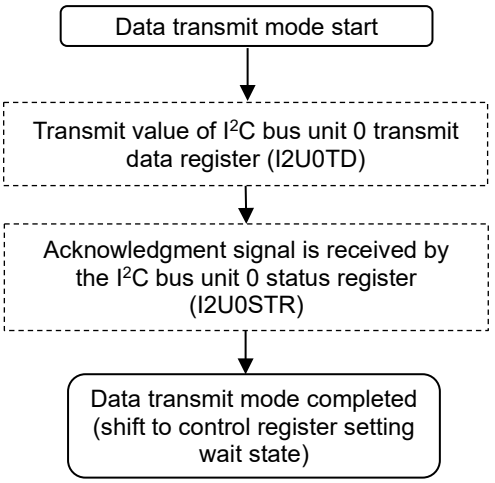
Acknowledgment signal is received through hardware
I2UM0ACR bit: Acknowledgment data

I²C bus 0 control register (I2UM0CON) setting wait state

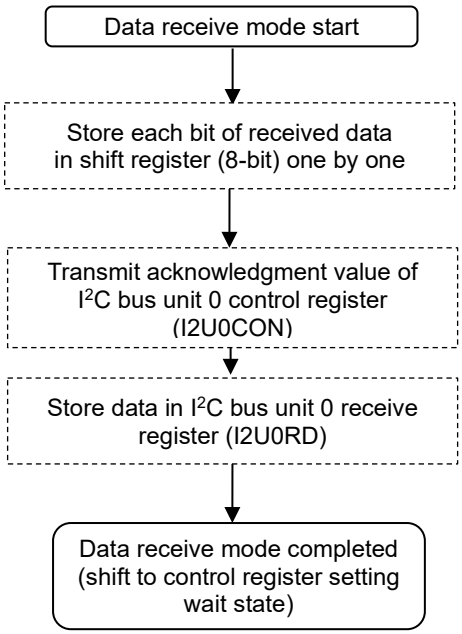
13.5.1.5 Control Register Setting Wait State



13.5.1.6 Data Transmission Mode



13.5.1.7 Data Reception Mode



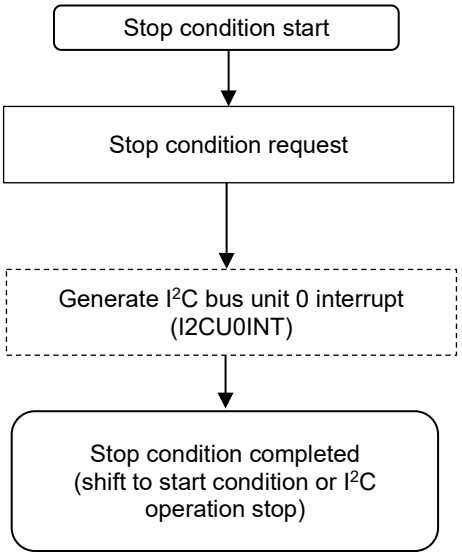
Value (received data) input to SDAU0 pin is stored in synchronization with rising edge of transfer clock input to SCLU0 pin in MSB first

Acknowledgment signal is transmitted through hardware
I2U0ACT bit: Acknowledgment value
Transmitted acknowledgment value is stored in the I2U0ACR bit of the I2U0STA register

Received data is stored from the shift register after acknowledgment signal is transmitted
I2U0R7 to I2U0R0 bits: 8-bit receive data

I²C bus unit 0 control register (I2U0CON) setting wait state

13.5.1.8 Stop Condition



Set I2U0SP bit of I2U0CON register to “1”.

Output stop condition waveforms to SDAU0 and SCLU0 pins.

After the stop condition waveform is output, an interrupt is generated through hardware

Shift to start condition or I²C operation stop (I2U0EN = 0)

13.5.2 Communication Operation Timing

Figures 13-2 to 13-4 show the operation timing and control method for each communication mode during the master operation.

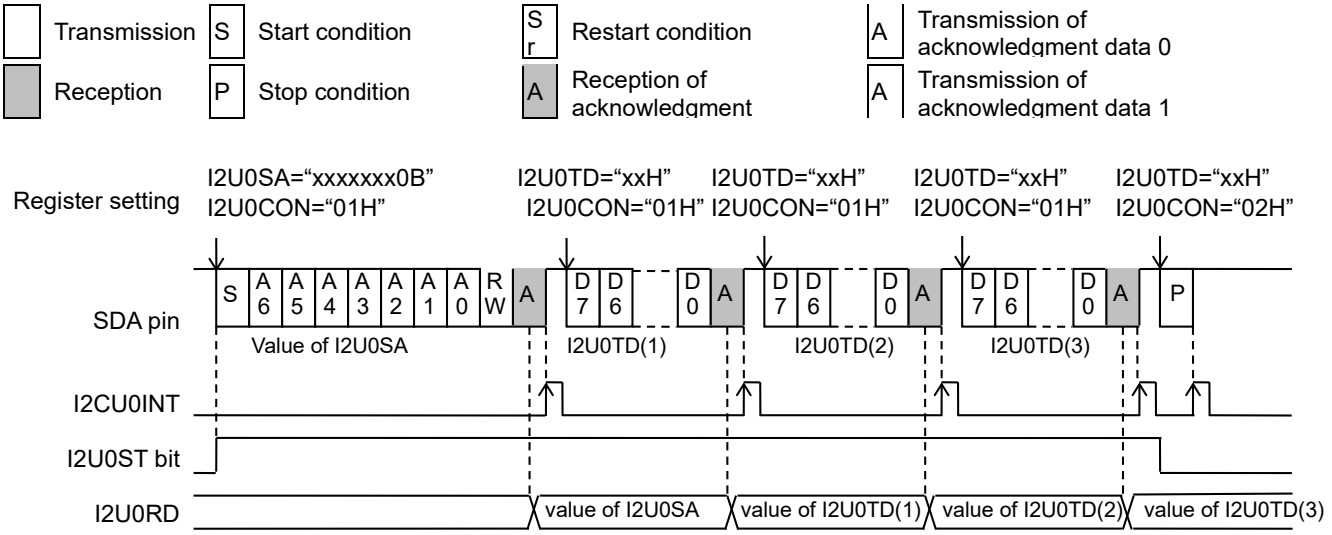


Figure 13-2 Operation timing during data transmission in the master mode

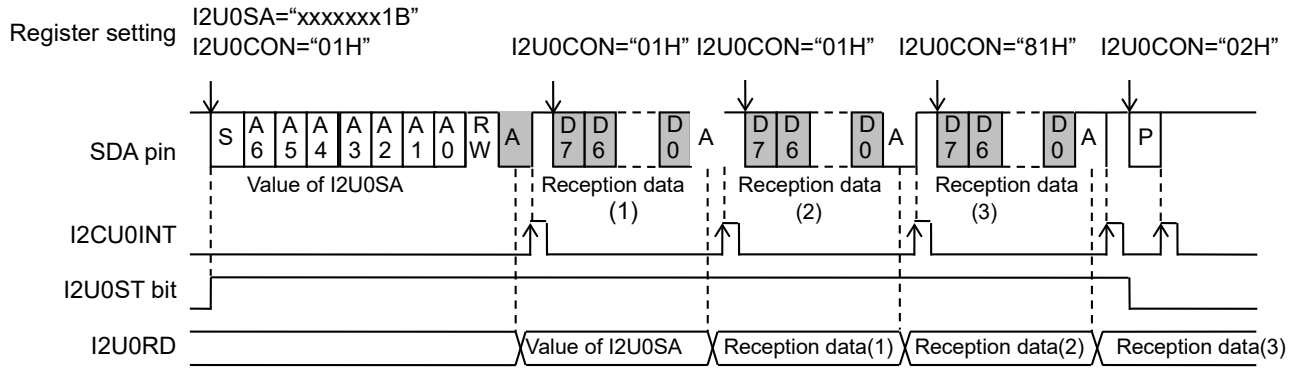


Figure 13-3 Operation timing during data reception in the master mode

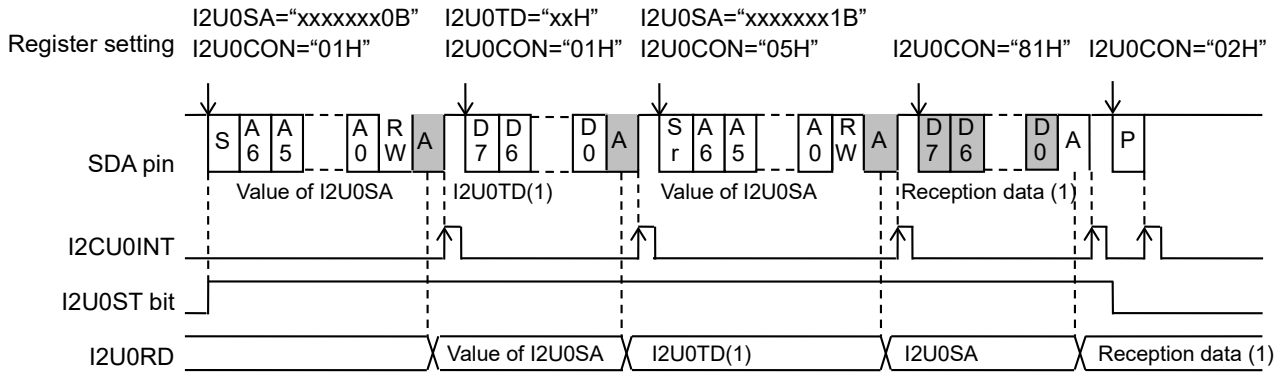


Figure 13-4 Operation timing during data transmission/ reception in the master mode

Figure 13-5 shows the operation timing and control method when an acknowledgment error occurs.

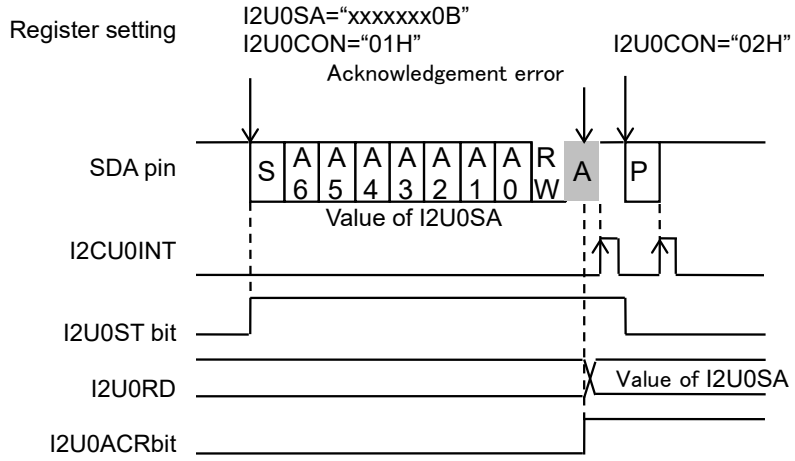


Figure 13-5 Operation suspend timing at occurrence of acknowledgment error in the master mode

When the clock stretch function is used, if the transmitted bit and the value of SDAU0 pin do not coincide, I2U0ER bit of the I²C bus unit 0 status register (master side) (I2U0STR) becomes "1", and the output of SDAU0 pin is disabled until the end of byte data communication thereafter.

Figure 13-6 shows the operation timing and control method when transmission fails.

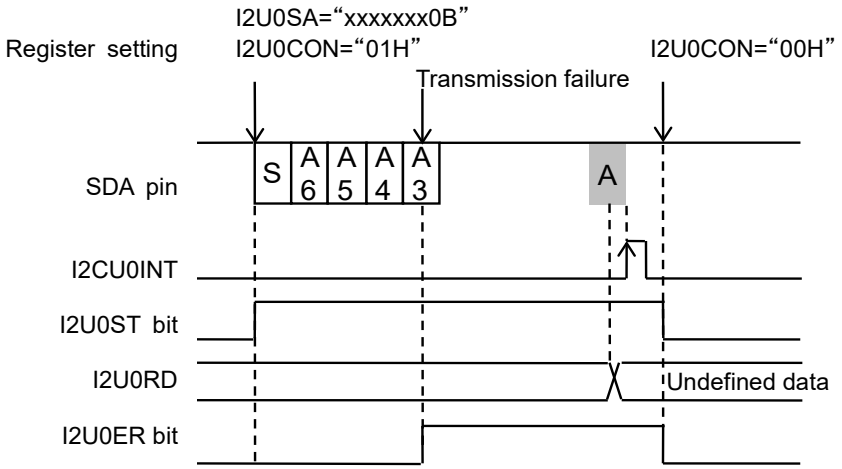


Figure 13-6 Operation timing when transmission fails in the master mode

13.5.3 Interrupt

The following is interrupt causes in master operation.

Interrupt causes	Timing that the interrupt is occurred
Transmission of a slave address	At shift to control register setting wait state after end of slave address transmission mode
Data transmission	At shift to control register setting wait state after end of data transmission mode
Data reception	At shift to control register setting wait state after end of data reception mode
Output stop condition	After output stop condition waveform and passing tBUF.

13.5.4 Operation Waveforms

Figure 13-7 shows the operation waveforms of SDAU0 and SCLU0 pins. Table 13-3 shows the relations between communication speeds and I²C operation clock counts.

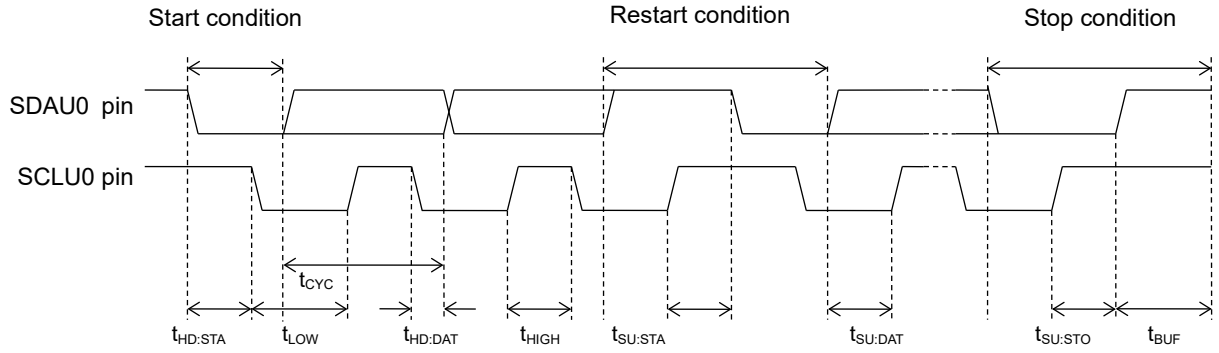


Figure 13-7 Operation Waveforms of SDAU0 and SCLU0 Pins

Table 13-3 relations between communication speeds and I²C operation clock counts

I2U0MOD register			AC timing [I²C operation clock counts]									I²C operation frequency and communication speed [kHz]			
I2U0TI2-0	I2U0MD1-0	I2U0MD3-2	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}	24MHz	16MHz	1MHz	LSCLK
0	0	0	240	108	132	24	108	132	108	108	132	100.0	66.7	4.2	0.1
0	0	1	264	120	144	24	120	144	120	120	144	90.9	60.6	3.8	0.1
0	0	2	288	132	156	24	132	156	132	132	156	83.3	55.6	3.5	0.1
0	0	3	312	144	168	24	144	168	144	144	168	76.9	51.3	3.2	0.1
0	1	0	60	24	36	12	24	36	24	24	36	400.0	266.7	16.7	0.5
0	1	1	66	27	39	12	27	39	27	27	39	363.6	242.4	15.2	0.5
0	1	2	72	30	42	12	30	42	30	30	42	333.3	222.2	13.9	0.5
0	1	3	78	33	45	12	33	45	33	33	45	307.7	205.1	12.8	0.4
0	2	0	24	10	14	4	10	14	10	10	14	1000.0	666.7	41.7	1.4
0	2	1	26	11	15	4	11	15	11	11	15	923.1	615.4	38.5	1.3
0	2	2	29	13	16	4	13	16	12	13	16	827.6	551.7	34.5	1.1
0	2	3	31	14	17	4	14	17	13	14	17	774.2	516.1	32.3	1.1
1	0	0	160	72	88	16	72	88	72	72	88	150.0	100.0	6.3	0.2
1	0	1	176	80	96	16	80	96	80	80	96	136.4	90.9	5.7	0.2
1	0	2	192	88	104	16	88	104	88	88	104	125.0	83.3	5.2	0.2
1	0	3	208	96	112	16	96	112	96	96	112	115.4	76.9	4.8	0.2
1	1	0	40	14	26	12	14	26	14	14	26	600.0	400.0	25.0	0.8
1	1	1	44	16	28	12	16	28	16	16	28	545.5	363.6	22.7	0.7
1	1	2	48	18	30	12	18	30	18	18	30	500.0	333.3	20.8	0.7
1	1	3	52	20	32	12	20	32	20	20	32	461.5	307.7	19.2	0.6
1	2	0	16	6	10	4	6	10	6	6	10	1500.0*	1000.0	62.5	2.0
1	2	1	18	7	11	4	7	11	7	7	11	1333.3*	888.9	55.6	1.8
1	2	2	19	8	11	4	8	11	7	8	11	1263.2*	842.1	52.6	1.7
1	2	3	21	9	12	4	9	12	8	9	12	1142.9*	761.9	47.6	1.6
2	0	0	120	54	66	12	54	66	54	54	66	200.0	133.3	8.3	0.3
2	0	1	132	60	72	12	60	72	60	60	72	181.8	121.2	7.6	0.2

I2U0MOD register			AC timing [I²C operation clock counts]									I²C operation frequency and communication speed [kHz]			
I2U0T12-0	I2U0MD1-0	I2U0MD3-2	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}	24MHz	16MHz	1MHz	LSCLK
2	0	2	144	66	78	12	66	78	66	66	78	166.7	111.1	6.9	0.2
2	0	3	156	72	84	12	72	84	72	72	84	153.8	102.6	6.4	0.2
2	1	0	30	12	18	6	12	18	12	12	18	800.0	533.3	33.3	1.1
2	1	1	33	14	19	6	14	19	13	14	19	750.0	500.0	31.3	1.0
2	1	2	36	15	21	6	15	21	15	15	21	666.7	444.4	27.8	0.9
2	1	3	39	17	22	6	17	22	16	17	22	631.6	421.1	26.3	0.9
2	2	0	12	5	7	2	5	7	5	5	7	2000.0*	1333.3*	83.3	2.7
2	2	1	13	6	7	2	6	7	5	6	7	2000.0*	1333.3*	83.3	2.7
2	2	2	14	6	8	2	6	8	6	6	8	1714.3*	1142.9*	71.4	2.3
2	2	3	15	7	8	2	7	8	6	7	8	1600.0*	1066.7*	66.7	2.2
3	0	0	80	36	44	8	36	44	36	36	44	300.0	200.0	12.5	0.4
3	0	1	88	40	48	8	40	48	40	40	48	272.2	181.8	11.4	0.4
3	0	2	96	44	52	8	44	52	44	44	52	250.0	166.7	10.4	0.3
3	0	3	104	48	56	8	48	56	48	48	56	230.8	153.8	9.6	0.3
3	1	0	20	7	13	6	7	13	7	7	13	1200.0*	800.0	50.0	1.6
3	1	1	22	8	14	6	8	14	8	8	14	1090.9*	727.3	45.5	1.5
3	1	2	24	9	15	6	9	15	9	9	15	1000.0	666.7	41.7	1.4
3	1	3	26	10	16	6	10	16	10	10	16	923.1	615.4	38.5	1.3
3	2	0	8	3	5	2	3	5	3	3	5	3000.0*	2000.0*	125.0	4.1
3	2	1	9	4	5	2	4	5	3	4	5	3000.0*	2000.0*	125.0	4.1
3	2	2	10	4	6	2	4	6	4	4	6	2666.7*	1777.8*	111.1	3.6
3	2	3	11	5	6	2	5	6	4	5	6	2400.0*	1600.0*	100.0	3.3
4	0	**	10	5	5	1	5	5	4	5	5	2400.0*	1600.0*	100.0	3.3
4	1	**	4	2	2	1	2	2	1	2	2	6000.0*	4000.0*	250.0	8.2
4	2	**	4	2	2	1	2	2	1	2	2	6000.0*	4000.0*	250.0	8.2
5	0	**	16	8	8	1	8	8	7	8	8	1500.0*	1000.0*	62.5	2.0
5	1	**	8	4	4	1	4	4	3	4	4	3000.0*	2000.0*	125.0	4.1
5	2	**	4	2	2	1	2	2	1	2	2	6000.0*	4000.0*	250.0	8.2

*: The operation is not guaranteed when over 1MHz speed.
**: The setting is invalid.

These clock counts are in case of I2U0CD1-0/I2M0CD1-0 bits = “00”. If 1/2 to 1/8SYSCLK is selected with I2U0CD1 to I2U0CD0/I2MnCD1 to I2MnCD0 bits, the clock count increases in proportion to the divider ratio.

[Note]

- **When the slave device uses the clock stretch function which holds the SCLU0 pin at "L" level, the t_{CYC} and t_{LOW} period are extended.**

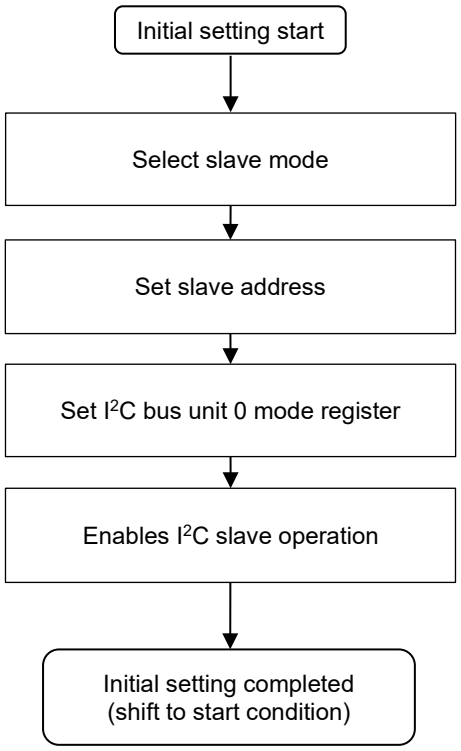
13.6 Description of Operation for Slave function

I²C bus unit 0 only have slave function.

13.6.1 Procedures

The following flow charts describe procedures of each operation in the slave mode.

13.6.1.1 Initial Setting of Communication Operation



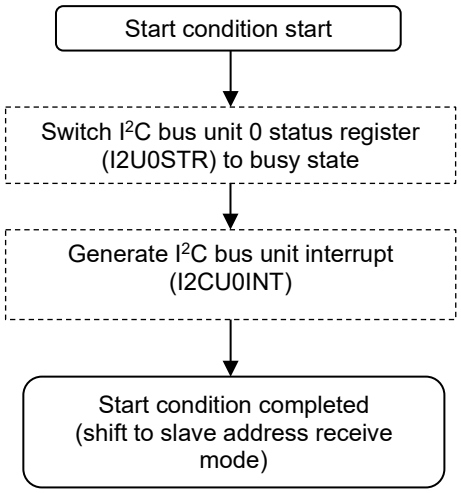
Select I2U0MD=1 in the I2U0MSS register

Set I2U0A6 to I2U0A0 bits in the I2U0SA register

Set the I2U0MD register
I2U0MD5 bit: Enable/disable start condition interrupt
I2U0MD4 bit: Enable/disable stop condition interrupt

Set I2U0EN=1 with the I2U0MD register

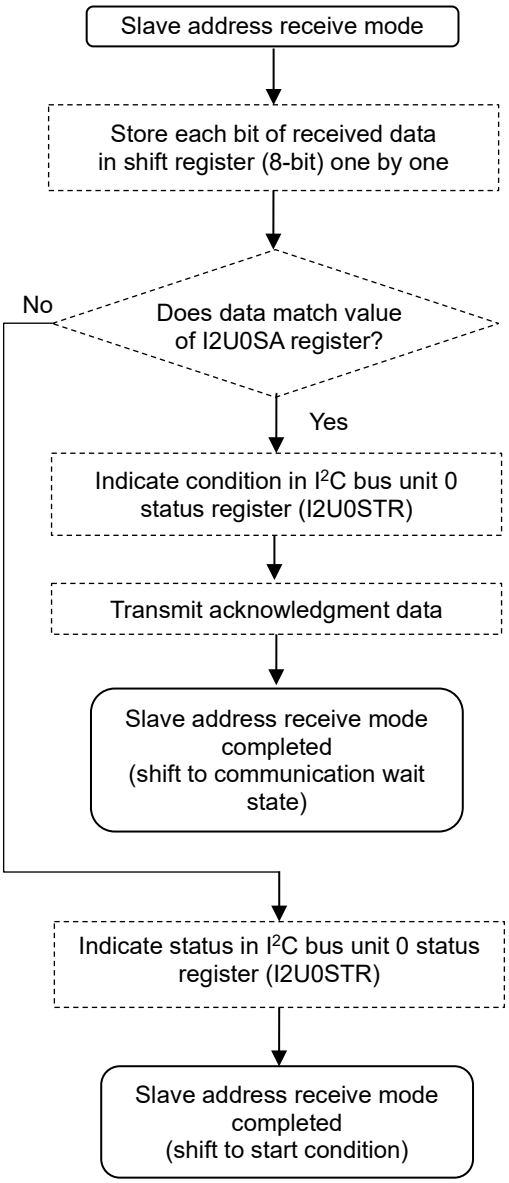
13.6.1.2 Start Condition



Value of the following bit becomes "1" when start condition waveforms are input to SDAU0 and SCLU0 pins

<Only when I2U0MD5=1>
Start condition interrupt is generated

13.6.1.3 Slave Address Reception Mode



Value (slave address, data direction bit) input to SDAU0 pin is stored in synchronization with rising edge of transfer clock input to SCLU0 pin in MSB first

Compare slave address stored in shift register with slave address of I2U0SA

I2U0SAA bit: Data matches slave address (I2U0SAA=1)
I2U0TR bit: Transmit state/receive state

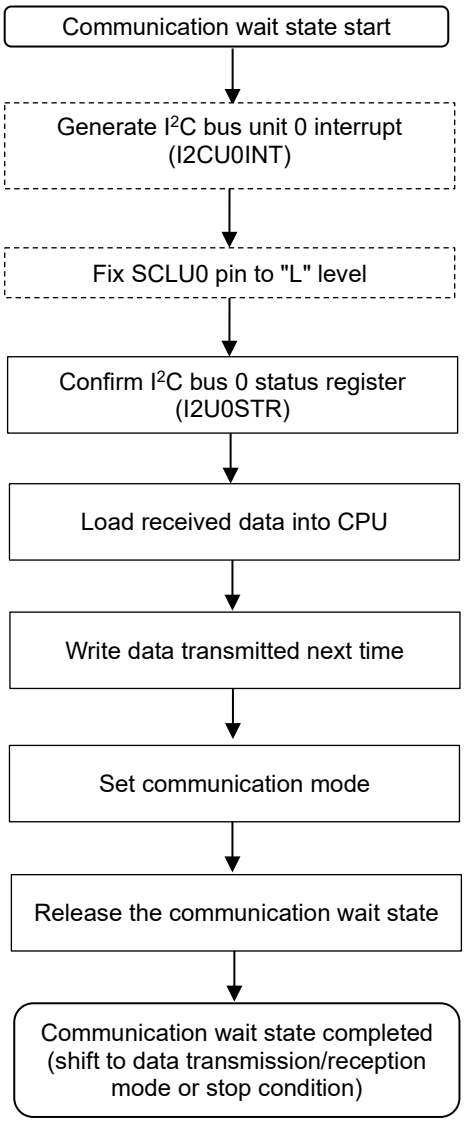
Acknowledgment data ("L" level) is output

Shift to the communication wait state after detection of falling edge of transfer clock which was input to SCLU0 pin transmitting acknowledgment data

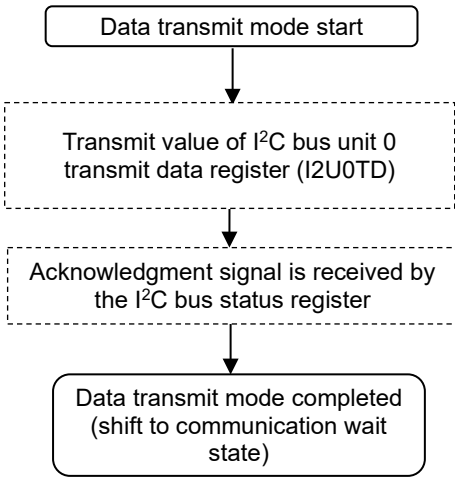
I2U0SAA bit: Data does not match slave address (I2U0SAA=0)

If not match, neither acknowledgment nor interrupt is generated

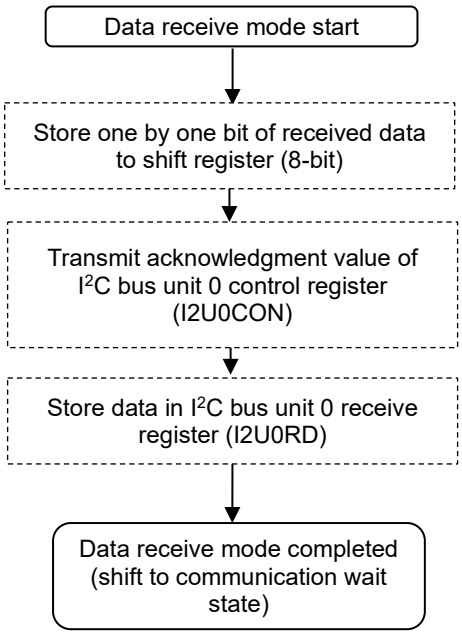
13.6.1.4 Communication Wait State



13.6.1.5 Data Transmission Mode



13.6.1.6 Data Reception Mode



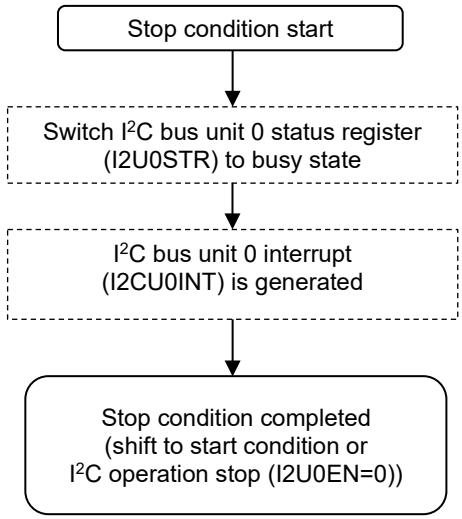
Value (received data) input to SDAU0 pin is stored in synchronization with rising edge of transfer clock input to SCLU0 pin in MSB first

Acknowledgment signal is transmitted through hardware
I2U0ACT bit: Acknowledgment value
Transmitted acknowledgment value is stored in the I2U0ACR bit of the I2U0STR register

Received data is stored from the shift register after acknowledgment signal is transmitted
I2U0R7 to I2U0R0 bits: 8-bit receive data

Shift to communication wait state after detection of falling edge of transfer clock which was input to SCLU0 pin transmitting acknowledgment data

13.6.1.7 Stop Condition

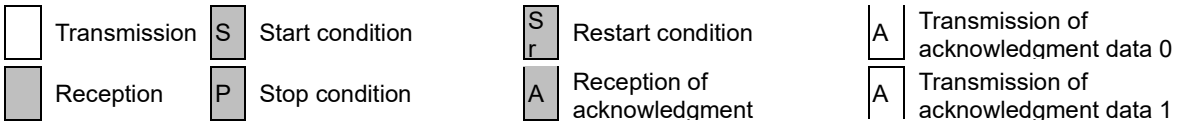


Value of the following bit becomes "0" when stop condition waveforms are input to SDAU0 and SCLU0 pins.

<Only when I2U0MD4=1>
Stop condition interrupt is generated

13.6.2 Communication Operation Timing

Figures 13-8 to 13-10 show the operation timing and control method for each communication mode.



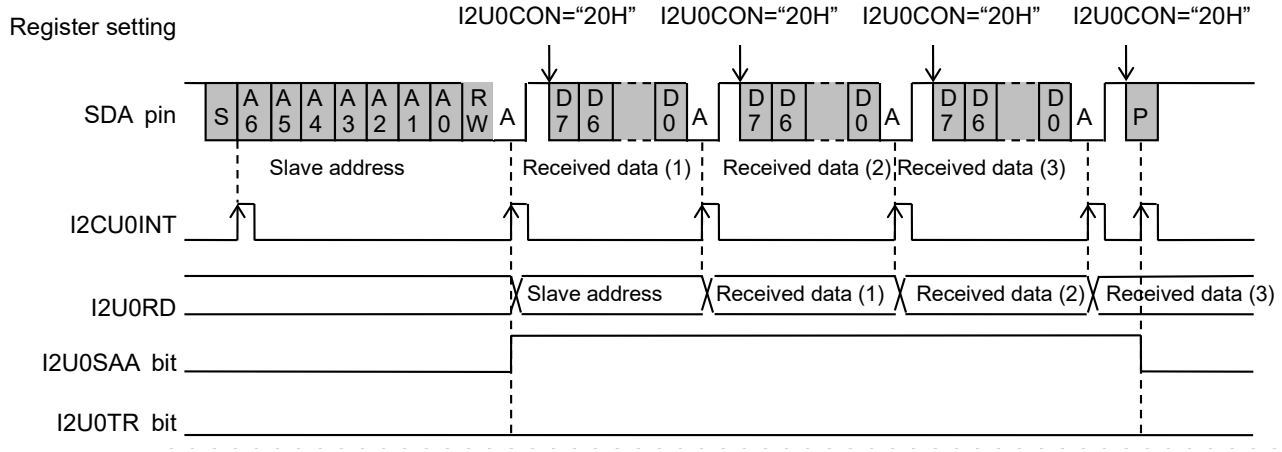


Figure 13-8 Operation Timing in Data Reception Mode When Slave Mode is Chosen

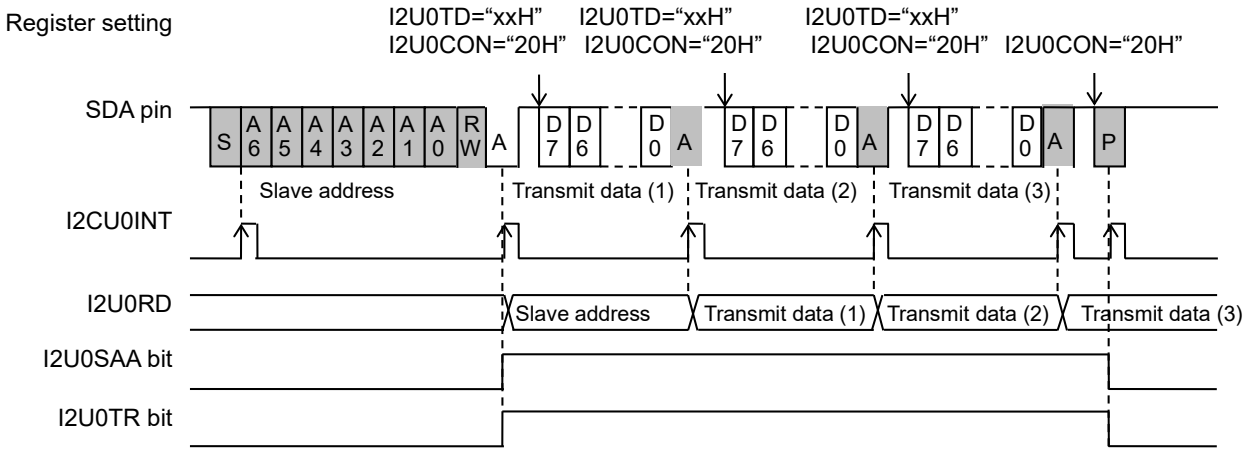


Figure 13-9 Operation Timing in Data Transmission Mode When Slave Mode is Chosen

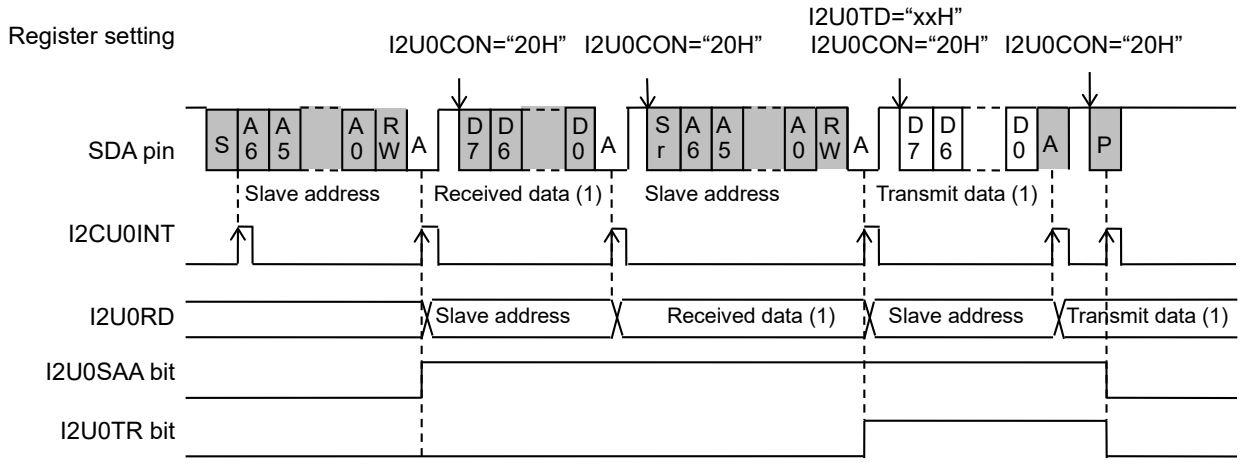


Figure 13-10 Operation Timing at Data Transmission/Reception Mode Switching When Slave Mode is Chosen

When the values of the transmitted bit and the SDAU0 pin do not coincide, the I2U0ER bit of the I²C bus unit 0 status register (I2U0STR) is set to "1" and the SDAU0 pin output is disabled until termination of the subsequent byte data communication.
Figure 13-11 shows the operation timing and control method when transmission fails.

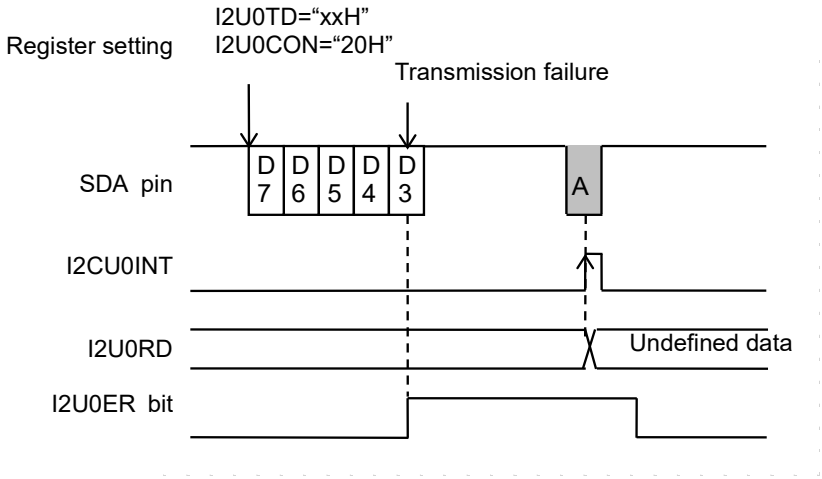


Figure 13-11 Operation Timing When Transmission Fails When Slave Mode is Chosen

[Note]
- **If entering to the STOP/STOP-D mode while the slave mode is enabled, first make sure that communication is not in progress (from coincidence of address to reception of stop condition).**

13.6.3 Interrupt

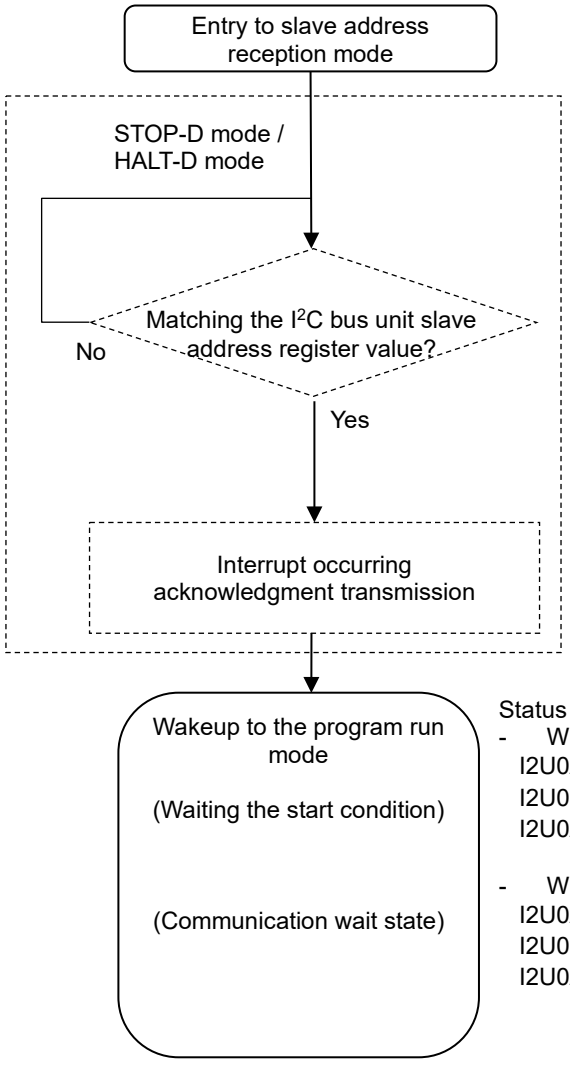
Table 13-4 shows interrupt causes in slave operation.

Table 13-4 List of slave interrupt

Interrupt causes	Setting to enable	Status flag in the I2U0STR register	Timing that the interrupt is occurred
Start condition	I2U0MD5=1	I2U0STS=1	After output start condition waveform.
Coinciding Slave Address	-	I2U0AS=1	At entry to control register setting wait state with coinciding slave-address after end of slave address reception mode
Coinciding Slave Address (in the HALT-D／STOP-D mode)	-	I2U0ASNA=1	At output "H" as acknowledge with coinciding slave-address after end of slave address reception mode.
Data transmission	-	I2U0DS=1	At entry to control register setting wait state after end of data transmission mode
Data reception	-	I2U0DS=1	At entry to control register setting wait state after end of data reception mode
Stop condition	I2U0MD4=1	I2U0SPS=1	At detecting stop-condition waveform.
Re-start condition, and then the master selects another slave.	I2U0MD3=1	I2U0RAS=1	At end of slave-address reception mode without coinciding slave-address after detected re-start condition with I2USAA=1.
Detect stop-condition for another slave.	I2U0MD4=1, I2U0MD1=0	I2U0SPS=1, I2U0AS=1	At detecting stop-condition waveform with I2U0SAA=1.

13.6.4 Wake-up from STOP-D/HALT-D mode by the Slave Address Coinciding

The LSI wake up from stand-by mode to program run mode by matching slave address.
In the HALT/HALT-H/STOP mode, the acknowledge data “L” level is output. In the STOP-D/HALT-D, the acknowledge data “H” level is output.
When acknowledge data “H” level is output, the communication can be executed by retransmitting from the start condition.
Depending on the timing of an entry to the STOP-D/HALT-D mode and slave address reception, it may wakeup with acknowledge data “L” level output. The I2U0STR register indicates these states. See Section 13.6.3 "Interrupt" for detail.



Enter to STOP-D/HALT-D mode after initial setup.

It compares the slave address stored in the shift register with the I2U0SA data.

If the results do not match, The standby mode is kept. and the interrupt does not occur.

The interrupt occurs and the LSI wakeups from STOP-D/HALT-D mode.
“H” level data is sent as the acknowledgement.
“L” level data may be sent if the entry to standby and slave address reception timing are close.

Status in the I2U0STR register after wakeup by slave address matching.

- When Acknowledgement “H” level is sent:
  I2U0ASNA＝1
  I2U0SAA＝0
  I2U0AS＝0

- When Acknowledgement “H” level is sent:
  I2U0ASNA＝0
  I2U0SAA＝1
  I2U0AS＝1

Figure 13-12 Wakeup from STOP-D/HALT-D mode by a coinciding slave address

[Note]

- **The master device should Wait for the SYSCLK to be supplied in order to transmit the start condition after wakeup from the STOP-D/HALT-D mode by slave address matching.**
- **It is supported the Fast mode (up to 400 kbps) in the STOP-D／HALT-D mode.**

Chapter 14 UART

14. UART

14.1 General Description

ML62Q2700 group has full-duplexed serial interface universal asynchronous receiver transmitter (UART : Universal Asynchronous Receiver Transmitter) and Extended synchronous serial interface with interrupt sharing UART Synchronous serial interface UART are referred to as UART and extended synchronous serial interface UART are referred to as extended UART, and Table 14-1 shows the channels for which UART/extended UART for each product.

Table 14-1 Channel No. for UART / Extended UART

Product Name	UART Channel No. (n)	Extended UART Channel No. (n)
ML62Q2747	0 to 2	0 to 2
ML62Q2746		
ML62Q2745		
ML62Q2737		
ML62Q2736		
ML62Q2735		
ML62Q2727		
ML62Q2726		
ML62Q2725		
ML62Q2723	0 to 1	-
ML62Q2722		
ML62Q2713		
ML62Q2712		
ML62Q2703		
ML62Q2702		

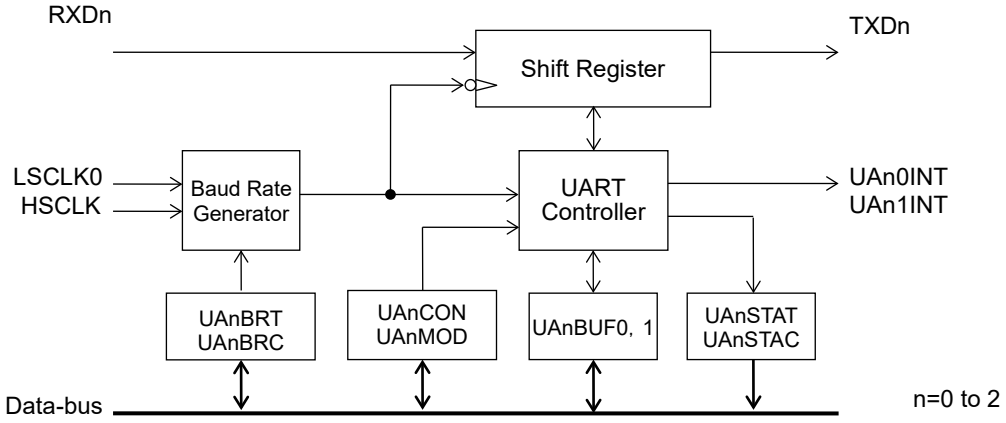
-: Not available

14.1.1 Features

- Selectable from 5 to 8bit data length
- Selectable from parity or no parity, odd parity or even parity
- Selectable from 1 stop bit or 2 stop bits
- Status flags I available: parity error, overrun error, framing error, transmission buffer
- Signal level : positive, negative
- Data direction : LSB first or MSB first
- Wide range of communication speed
  - 1bps to 4,800bps (Clock frequency is 32.768kHz)
  - 300bps to 2Mbps (Clock frequency is 16MHz)
  - 600bps to 3Mbps (Clock frequency is 24MHz)
- Built-in baud rate generator for each channel
- Self-test function using transmission and reception. See Chapter 29 "Safety Function." for the self-test functions.

14.1.2 Configuration

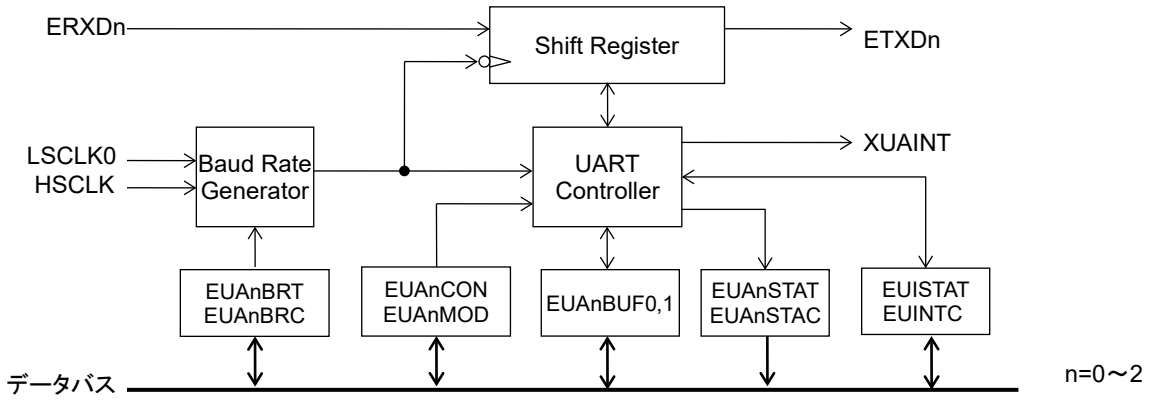
Figure 14-1 (a) shows configuration of the UART.



UAnBUF0,1	:	UARTn transmission/reception buffer0, 1
UAnBRT	:	UARTn baud rate register
UAnBRC	:	UARTn baud rate adjustment register
UAnCON	:	UARTn control register
UAnMOD	:	UARTn mode register
UAnSTAT, UAnSTAC	:	UARTn status register, UARTn status clear register

Figure 14-1(a) Configuration of UART

Figure 14-1 (b) shows configuration of the extended UART.



EUAnBUF0,1	:	Extended UARTn transmission/reception buffer 0, 1
EUAnBRT	:	Extended UARTn baud rate register
EUAnBRC	:	Extended UARTn baud rate adjustment register
EUAnCON	:	Extended UARTn control register
EUAnMOD	:	Extended UARTn mode register
EUAnSTAT, EUAnSTAC	:	Extended UARTn status register, UARTn status clear register

Figure 14-1(b) Configuration of extended UART

14.1.3 List of Pins

The I/O pins of the UART are assigned to the shared function of the general ports.

Pin name	I/O	Description
RXDn	I	Reception data input of UART n
TXDn	O	Transmission data output of UART n
ERXDn	I	Extended Reception data input of UART n
ETXDn	O	Extended Transmission data output of UART n

Table 14-2 shows the list of the general ports used for the UART and the register settings of the ports.

Table 14-2 Ports used for the UART and the register settings

Channel No.	Pin Name	Shared port		Setting register	Setting value	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702			ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725		
						48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
0	RXD0	P02	3rd Function	P0MOD2	0010_XXXX*1	●	●	●	●	●	●
		P07	3rd Function	P0MOD7	0010_XXXX*1	●	●	●	●	●	●
		P12	3rd Function	P1MOD2	0010_XXXX*1	●	●	●	●	●	●
		P17	3rd Function	P1MOD7	0010_XXXX*1	●	●	●	●	●	●
	TXD0	P03	3rd Function	P0MOD3	0010_XXXX*2	●	●	●	●	●	●
		P10	3rd Function	P1MOD0	0010_XXXX*2	●	●	●	●	●	●
		P13	3rd Function	P1MOD3	0010_XXXX*2	●	●	●	●	●	●
		P20	3rd Function	P2MOD0	0010_XXXX*2	●	●	●	●	●	●
1	RXD1	P21	3rd Function	P2MOD1	0010_XXXX*1	●	●	●	●	●	●
		P24	3rd Function	P2MOD4	0010_XXXX*1	●	●	●	●	●	●
		P26	3rd Function	P2MOD6	0010_XXXX*1	●	●	●	●	●	●
		P32	3rd Function	P3MOD2	0010_XXXX*1	●	●	●	●	●	●
	TXD1	P22	3rd Function	P2MOD2	0010_XXXX*2	●	●	●	●	●	●
		P25	3rd Function	P2MOD5	0010_XXXX*2	●	●	●	●	●	●
		P27	3rd Function	P2MOD7	0010_XXXX*2	●	●	●	●	●	●
		P33	3rd Function	P3MOD3	0010_XXXX*2	●	●	●	●	●	●
2	RXD2	P54	3rd Function	P5MOD4	0010_XXXX*1	-	-	-	●	●	●
		P56	3rd Function	P5MOD6	0010_XXXX*1	-	-	-	●	●	●
	TXD2	P55	3rd Function	P5MOD5	0010_XXXX*2	-	-	-	●	●	●
		P57	3rd Function	P5MOD7	0010_XXXX*2	-	-	-	●	●	●

●: Available
- : Not available

Channel No.	Pin Name	Shared port		Setting register	Setting value	ML62Q2723 ML62Q2722 ML62Q2713 ML62Q2712 ML62Q2703 ML62Q2702			ML62Q2747 ML62Q2746 ML62Q2745 ML62Q2737 ML62Q2736 ML62Q2735 ML62Q2727 ML62Q2726 ML62Q2725		
						48pin product	52pin product	64pin product	64pin product	80pin product	100pin product
0	ERXD0	P64	3rd Function	P6MOD4	0010_XXXX*1	-	-	-	●	●	●
		P67	3rd Function	P6MOD7	0010_XXXX*1	-	-	-	●	●	●
	ETXD0	P42	3rd Function	P4MOD2	0010_XXXX*2	-	-	-	●	●	●
		P65	3rd Function	P6MOD5	0010_XXXX*2	-	-	-	●	●	●
1	ERXD1	P44	3rd Function	P4MOD4	0010_XXXX*1	-	-	-	●	●	●
		P52	3rd Function	P5MOD2	0010_XXXX*1	-	-	-	●	●	●
		P80	3rd Function	P8MOD0	0010_XXXX*1	-	-	-	-	●	●
		P93	3rd Function	P9MOD3	0010_XXXX*1	-	-	-	-	●	●
	ETXD1	P45	3rd Function	P4MOD5	0010_XXXX*2	-	-	-	●	●	●
		P53	3rd Function	P5MOD3	0010_XXXX*2	-	-	-	●	●	●
		P81	3rd Function	P8MOD1	0010_XXXX*2	-	-	-	-	●	●
		P94	3rd Function	P9MOD4	0010_XXXX*2	-	-	-	-	●	●
2	ERXD2	P41	3rd Function	P4MOD1	0010_XXXX*1	-	-	-	●	-	●
		P83	3rd Function	P8MOD3	0010_XXXX*1	-	-	-	-	-	●
		PB2	3rd Function	PBMOD2	0010_XXXX*1	-	-	-	-	●	●
		PB5	3rd Function	PBMOD5	0010_XXXX*1	-	-	-	-	●	●
	ETXD2	P40	3rd Function	P4MOD0	0010_XXXX*2	-	-	-	●	●	●
		P84	3rd Function	P8MOD4	0010_XXXX*2	-	-	-	-	-	●
		PB3	3rd Function	PBMOD3	0010_XXXX*2	-	-	-	-	●	●

●: Available
- : Not available

*1 : "XXXX" determines the condition of the port input

XXXX	Condition of the port input
0001	Input (without an internal pull-up resistor)
0101	Input (with an internal pull-up resistor)

*2 : "XXXX" determines the condition of the port output

XXXX	Condition of the port output
0010	CMOS output
1010	N-ch open drain output (without the pull-up)
1111	N-ch open drain output (with the pull-up)

14.2 Description of Registers

14.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF600	UART0 reception buffer	UA0BUF0	-	R	8	0x00
0xF601	UART0 transmission buffer	UA0BUF1	-	R/W	8	0x00
0xF602	UART0 status register	UA0STAT	-	R	8	0x00
0xF603	UART0 status clear register	UA0STAC	-	W	8	0x00
0xF604	UART0 control register	UA0CON	-	R/W	8	0x00
0xF605	Reserved register	-	-	-	-	-
0xF606	UART0 mode registers	UA0MODL	UA0MOD	R/W	8/16	0x00
0xF607		UA0MODH		R/W	8	0x00
0xF608	UART0 interrupt enable register	UA0INTE	-	R/W	8	0x00
0xF609	Reserved register	-	-	-	-	-
0xF60A	UART0 baud rate registers	UA0BRTL	UA0BRT	R/W	8/16	0xFF
0xF60B		UA0BRTH		R/W	8	0x0F
0xF60C	UART0 baud rate adjustment register	UA0BRC	-	R/W	8	0x00
0xF60D to 0xF60F	Reserved registers	-	-	-	-	-
0xF610	UART1 reception buffer	UA1BUF0	-	R	8	0x00
0xF611	UART1 transmission buffer	UA1BUF1	-	R/W	8	0x00
0xF612	UART1 status register	UA1STAT	-	R	8	0x00
0xF613	UART1 status clear register	UA1STAC	-	W	8	0x00
0xF614	UART1 control register	UA1CON	-	R/W	8	0x00
0xF615	Reserved register	-	-	-	-	-
0xF616	UART1 mode registers	UA1MODL	UA1MOD	R/W	8/16	0x00
0xF617		UA1MODH		R/W	8	0x00
0xF618	UART1 interrupt enable register	UA1INTE	-	R/W	8	0x00
0xF619	Reserved register	-	-	-	-	-
0xF61A	UART1 baud rate registers	UA1BRTL	UA1BRT	R/W	8/16	0xFF
0xF61B		UA1BRTH		R/W	8	0x0F
0xF61C	UART1 baud rate adjustment register	UA1BRC	-	R/W	8	0x00
0xF61D to 0xF61F	Reserved registers	-	-	-	-	-
0xF620	UART2 reception buffer	UA2BUF0	-	R	8	0x00
0xF621	UART2 transmission buffer	UA2BUF1	-	R/W	8	0x00
0xF622	UART2 status register	UA2STAT	-	R	8	0x00
0xF623	UART2 status clear register	UA2STAC	-	W	8	0x00
0xF624	UART2 control register	UA2CON	-	R/W	8	0x00
0xF625	Reserved register	-	-	-	-	-
0xF626	UART2 mode registers	UA2MODL	UA2MOD	R/W	8/16	0x00
0xF627		UA2MODH		R/W	8	0x00
0xF628	UART2 interrupt enable register	UA2INTE	-	R/W	8	0x00
0xF629	Reserved register	-	-	-	-	-
0xF62A	UART2 baud rate registers	UA2BRTL	UA2BRT	R/W	8/16	0xFF
0xF62B		UA2BRTH		R/W	8	0x0F
0xF62C	UART2 baud rate adjustment register	UA2BRC	-	R/W	8	0x00
0xF62D to 0xF62F	Reserved registers	-	-	-	-	-
0xF630	Extended UART0 reception buffer	EUA0BUF0	-	R	8	0x00
0xF631	Extended UART0 transmission buffer	EUA0BUF1	-	R/W	8	0x00
0xF632	Extended UART0 status register	EUA0STAT	-	R	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF633	Extended UART0 status clear register	EUA0STAC	-	W	8	0x00
0xF634	Extended UART0 control register	EUA0CON	-	R/W	8	0x00
0xF635	Reserved register	-	-	-	-	-
0xF636	Extended UART0 mode registers	EUA0MODL	EUA0MOD	R/W	8/16	0x00
0xF637		EUA0MODH		R/W	8	0x00
0xF638	Extended UART0 interrupt enable register	EUA0INTE	-	R/W	8	0x00
0xF639	Reserved register	-	-	-	-	-
0xF63A	Extended UART0 baud rate registers	EUA0BRTL	EUA0BRT	R/W	8/16	0xFF
0xF63B		EUA0BRTH		R/W	8	0x0F
0xF63C	Extended UART0 baud rate adjustment register	EUA0BRC	-	R/W	8	0x00
0xF63D to 0xF63F	Reserved registers	-	-	-	-	-
0xF640	Extended UART1 reception buffer	EUA1BUF0	-	R	8	0x00
0xF641	Extended UART1 transmission buffer	EUA1BUF1	-	R/W	8	0x00
0xF642	Extended UART1 status register	EUA1STAT	-	R	8	0x00
0xF643	Extended UART1 status clear register	EUA1STAC	-	W	8	0x00
0xF644	Extended UART1 control register	EUA1CON	-	R/W	8	0x00
0xF645	Reserved registers	-	-	-	-	-
0xF646	Extended UART1 mode registers	EUA1MODL	EUA1MOD	R/W	8/16	0x00
0xF647		EUA1MODH		R/W	8	0x00
0xF648	Extended UART1 interrupt enable register	EUA1INTE	-	R/W	8	0x00
0xF649	Reserved registers	-	-	-	-	-
0xF64A	Extended UART1 baud rate registers	EUA1BRTL	EUA1BRT	R/W	8/16	0xFF
0xF64B		EUA1BRTH		R/W	8	0x0F
0xF64C	Extended UART1 baud rate adjustment register	EUA1BRC	-	R/W	8	0x00
0xF64D to 0xF64F	Reserved registers	-	-	-	-	-
0xF650	Extended UART2 reception buffer	EUA2BUF0	-	R	8	0x00
0xF651	Extended UART2 transmission buffer	EUA2BUF1	-	R/W	8	0x00
0xF652	Extended UART2 status register	EUA2STAT	-	R	8	0x00
0xF653	Extended UART2 status clear register	EUA2STAC	-	W	8	0x00
0xF654	Extended UART2 control register	EUA2CON	-	R/W	8	0x00
0xF655	Reserved registers	-	-	-	-	-
0xF656	Extended UART2 mode registers	EUA2MODL	EUA2MOD	R/W	8/16	0x00
0xF657		EUA2MODH		R/W	8	0x00
0xF658	Extended UART2 interrupt enable register	EUA2INTE	-	R/W	8	0x00
0xF659	Reserved registers	-	-	-	-	-
0xF65A	Extended UART2 baud rate registers	EUA2BRTL	EUA2BRT	R/W	8/16	0xFF
0xF65B		EUA2BRTH		R/W	8	0x0F
0xF65C	Extended UART2 baud rate adjustment register	EUA2BRC	-	R/W	8	0x00
0xF680	Extended UART interrupt status register	EUISTAT	-	R	8	0x00
0xF681	Reserved register	-	-	-	-	-
0xF682	Extended UART interrupt status clear registers	EUINTCL	EUINTC	W	8	0x00
0xF683		EUINTCH		W	8/16	0x00

[Note]

- **When the DCKUAn of Block control register 2 (BCKCON2) is “1”, the SFR readout value of the corresponding channel is "0x00/0x0000". However, the settings themselves are retained. When DCKUAn is set back to "0", the SFR readout value is the set value. For information about block control registers, see Chapter 4 Power Management.**

14.2.2 UARTn Reception Buffer (UAnBUF0)

UAnBUF0 is a SFR to store reception data.

Address : 0xF600(UA0BUF0),0xF610(UA1BUF0),0xF620(UA2BUF0),
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								UAnBUF0							
Bit	-	-	-	-	-	-	-	-	UnRD 7	UnRD 6	UnRD 5	UnRD 4	UnRD 3	UnRD 2	UnRD 1	UnRD 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 0	UnRD7 to UnRD0	Store the data received at the end of reception in UAnBUF0. UARTn0 interrupt at the end of reception is used to read UAnBUF0. In the case of continuous reception, UAnBUF0 is updated at each end of reception. Also, when the data length of 5 to 7bit is selected, unused bits return “0”.

14.2.3 UARTn Transmission Buffer (UAnBUF1)

UAnBUF1 is a SFR to store transmission data.

Address : 0xF601(UA0BUF1),0xF611(UA1BUF1),0xF621(UA2BUF1),
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								UAnBUF1							
Bit	-	-	-	-	-	-	-	-	UnTD 7	UnTD 6	UnTD 5	UnTD 4	UnTD 3	UnTD 2	UnTD 1	UnTD 0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 0	UnTD7 to UnTD0	Write transmission data to this. For continuous transmitting, write the next transmission data to this register after checking UnFUL bit of UAnSTAT is “0”. The written data in this register can be read out. Write the data to be sent to UAnBUF1. For continuous transmission, confirm that the UnFUL flag in the transmission status register (UAnSTAT) becomes "0" before writing the next transmission data to UAnBUF1. It is also enable to read the value written to UAnBUF1 Also, when the data length of 5 to 7bit is selected, unused bits are invalid.

14.2.4 UARTn Status Register (UAnSTAT)

UAnSTAT is a SFR to indicate states of the transmission/reception operation.

Address : 0xF602(UA0STAT),0xF612(UA1STAT),0xF622(UA2STAT)
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								UAnSTAT							
Bit	-	-	-	-	-	-	-	-	-	-	UnRXF	UnTXF	UnFUL	UnPER	UnOER	UnFER
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 6	-	Reserved bits
5	UnRXF	Indicate UARTn data reception state. 0: Data reception is stopped (Initial value) 1: Data reception is in progress
4	UnTXF	Indicate UARTn data transmission state. 0: Data transmission is stopped (Initial value) 1: Data transmission is in progress
3	UnFUL	Indicate transmission buffer state. This bit is set to “1” by writing a data to UAnBUF1 and reset to “0” when the data is transferred to shift register. To transmit data successively, check that UnFUL bit is "0" before writing the next transmission data to UAnBUF1.This bit is forcibly reset to "0" by writing “1” to the UnFULC bit of UAnSTAC register. 0: Transmission buffer has no data (Initial value) 1: Transmission buffer has data
2	UnPER	Indicate a parity error. The parity of the received data and the parity bit added to the data are compared and if they do not match, this bit is set to "1". This bit is forcibly reset to "0" by writing “1” to UnPERC bit of UAnSTAC register. 0: The parity error has not occurred. (Initial value) 1: The parity error has occurred.
1	UnOER	Indicate a reception overrun error. This bit is set to "1" if the next data is received before reading the previous receive data in reception buffer (UAnBUFL). Even if reception is stopped by the UnEN bit and then reception is re-started, this bit is set to “1” unless the previously received data is not read. Therefore, reading the data is required from the reception buffer every reception completion even if the data is not required. This is forcibly reset to "0" by writing “1” to UnOERC bit of UAnSTAC register. 0: The overrun error has not occurred (Initial value) 1: The overrun error has occurred
0	UnFER	Indicate a framing error. This bit is set to "1" when an error occurs in the start/stop bit. Un0FER bit is forcibly reset to "0" by writing “1” to UnFERC bit of UAnSTARC register. 0: The framing error has not occurred (Initial value) 1: The framing error has occurred

14.2.5 UARTn Status Clear Register (UAnSTAC)

UAnSTAC is a write-only SFR to clear states of the transmission/reception operation.

Address : 0xF603(UA0STAC),0xF613(UA1STAC),0xF623(UA2STAC)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								UAnSTAC							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	UnFULC	UnPERC	UnOERC	UnFERC
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 3	-	Reserved bits
3	UnFULC	Clear the state (UnFUL) of UARTn transmit buffer. Writing “0” : Invalid Writing “1” : Clear UnFUL bit
2	UnPERC	Clear the parity error bit (UnPER) of UARTn. Writing “0” : Invalid Writing “1” : Clear UnPER bit.
1	UnOERC	Clear the UARTn overrun error bit (UnOER). Writing “0” : Invalid Writing “1” : Clear UnOER bit.
0	UnFERC	Clear the framing error bit (UnFER) of UARTn. Writing “0” : Invalid Writing “1” : Clear UnFER bit.

14.2.6 UARTn Control Register (UAnCON)

UAnCON is a SFR to control enable/disable communication.

Address : 0xF604(UA0CON),0xF614(UA1CON),0xF624(UA2CON)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								UAnCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	UnEN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	UnEN	Enable UARTn communication. See Section 14.3.4 "Transmission Operation" for details. A both of transmission and reception are enabled when UnEN = 1. Set “0” to this bit if communication is stopped. 0: communication is Disabled (Initial value) 1: communication is Enabled

[Note]

- **Set the mode/baud rate of the pin and UART before setting the UnEN bit to "1".**

14.2.7 UARTn Mode Register (UAnMOD)

UAnMOD is a SFR to set the transfer mode.

Address : 0xF606(UA0MODL/UA0MOD),0xF607(UA0MODH),
0xF616(UA1MODL/UA1MOD),0xF617(UA1MODH),
0xF626(UA2MODL/UA2MOD),0xF627(UA2MODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	UAnMOD															
Byte	UAnMODH								UAnMODL							
Bit	UnDIR	UnNEG	UnSTP	UnPT2	UnPT1	UnPT0	UnLG1	UnLG0	-	UnRSS	-	-	-	-	UnCK0	-
R/W	R/W	R/W	R/W	R/W	R/w	R/w	R/W	R/W	R	R/W	R	R	R	R	R/W	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	UnDIR	Select UARTn LSB first or MSB first . 0: LSB first (Initial value) 1: MSB first
14	UnNEG	Select UARTn positive logic or negative logic. 0: Positive logic (Initial value) 1: Negative logic
13	UnSTP	Select UARTn stop bit length. 0: 1 stop bit (Initial value) 1: 2 stop bit
12 to 10	UnPT2 to UnPT0	Selects UARTn parity bit from even, odd, 0 fixed, 1 fixed, or no parity bit. 000: No parity bit (Initial value) 001: Odd parity 010: No parity bit 011: Even parity 100: No parity bit 101: Parity bit is fixed to “1” 110: No parity bit 111: Parity bit is fixed to “0”
9 to 8	UnLG1 to UnLG0	Select UARTn communication data length. 00: 8-bit length (Initial value) 01: 7-bit length 10: 6-bit length 11: 5-bit length
7	-	Reserved bit
6	UnRSS	Select UARTn sampling timing of the reception data input. 0: (Values set to UAn0BRT registers)/2 (Initial value) 1: {(Values set to UAn0BRT registers)/2} -1
5~2	-	Reserved bits
1	UnCK0	Selects the clock of UARTn baud rate generator 0: LSCLK0 (Initial value) 1: HSCLK
0	-	Reserved bit

[Note]

- **Set UAnMOD register while communication is stopped, and do not rewrite it while communicating.**

14.2.8 UARTn Interrupt Enable Register (UAnINTE)

UAnINTE is a SFR to enable interrupt requests.

Address : 0xF608 (UA0INTE),0xF618 (UA1INTE),0xF628 (UA2INTE)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								UAnINTE							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	UnFIE	UnTIE	UnRIE
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured enable/disable a target interrupt
0: Disable a target interrupt (Initial value)
1: Enable a target interrupt

Bit no.	Bit symbol name	Description
7 to 3	-	Reserved bits
2	UnFIE	Transmission completion interrupt The interrupt occurs when transmission data is transmitted in the condition of transmission buffer empty.
1	UnTIE	Transmission buffer empty interrupt. The interrupt occurs when transmission buffer becomes empty.
0	UnRIE	Reception interrupt. The interrupt occurs when data is received.

14.2.9 UARTn Baud Rate Register (UAnBRT)

UAnBRT is a SFR to set the count value of the baud rate generator in UARTn.
For details of relation between the count value of the baud rate generator and the baud rate, see Section 14.3.3 “Baud Rate”.

Address : 0xF60A (UA0BRTL/UA0BRT), 0xF60B (UA0BRTH),
0xF61A (UA1BRTL/UA1BRT), 0xF61B (UA1BRTH),
0xF62A (UA2BRTL/UA2BRT), 0xF62B (UA2BRTH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0FFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	UAnBRT															
Byte	UAnBRTH								UAnBRTL							
Bit	UnBR 15	UnBR 14	UnBR 13	UnBR 12	UnBR 11	UnBR 10	UnBR 9	UnBR 8	UnBR 7	UnBR 6	UnBR 5	UnBR 4	UnBR 3	UnBR 2	UnBR 1	UnBR 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

[Note]
Set UAnBRC register while communication is stopped, and do not rewrite it while communicating.

14.2.10 UARTn Baud Rate Adjustment Register (UAnBRC)

UAnBRC is a SFR to adjust the count value of the baud rate generator in UARTn.
For details of relation between the value of UAnBRC and the correction value, see Section 14.3.3 “Baud Rate”.

Address : 0xF60C(UA0BRC),0xF61C(UA1BRC),0xF62C(UA2BRC)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								UAnBRC							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	UnBR C2	UnBR C1	UnBR C0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
- **Set UAnBRT register while communication is stopped, and do not rewrite it while communicating.**

14.2.11 Extended UARTn Reception Buffer (EUAnBUF0)

EUAnBUF0 is a SFR to store reception data.

Address : 0xF630(EUA0BUF0),0xF640(EUA1BUF0),0xF650(EUA2BUF0),
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUAnBUF0							
Bit	-	-	-	-	-	-	-	-	EUnRD7	EUnRD6	EUnRD5	EUnRD4	EUnRD3	EUnRD2	EUnRD1	EUnRD0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 0	EUnRD7 to EUnRD0	Store the data received at the end of reception in EUAnBUF0. UARTn0 interrupt at the end of reception is used to read EUAnBUF0. In the case of continuous reception, EUAnBUF0 is updated at each end of reception. Also, when the data length of 5 to 7bit is selected, unused bits return “0”.

14.2.12 Extended UARTn Transmission Buffer (EUAnBUF1)

EUAnBUF1 is a SFR to store transmission data.

Address : 0xF631(EUA0BUF1),0xF641(EUA1BUF1),0xF651(EUA2BUF1),
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUAnBUF1							
Bit	-	-	-	-	-	-	-	-	EUnTD7	EUnTD6	EUnTD5	EUnTD4	EUnTD3	EUnTD2	EUnTD1	EUnTD0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 0	EUnTD7 to EUnTD0	Write transmission data to this. For continuous transmitting, write the next transmission data to this register after checking EUnFUL bit of EUAnSTAT is “0”. The written data in this register can be read out. Write the data to be sent to EUAnBUF1. For continuous transmission, confirm that EUnFUL flag in the transmission status register (EUAnSTAT) becomes "0" before writing the next transmission data to EUAnBUF1. It is also enabled to read the value written to EUAnBUF1 Also, when the data length of 5 to 7bit is selected, unused bits are invalid.

14.2.13 Extended UARTn Status Register (EUAnSTAT)

EUAnSTAT is a SFR to indicate states of the transmission/reception operation.

Address : 0xF632(EUA0STAT),0xF642(EUA1STAT),0xF652(EUA2STAT)
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUAnSTAT							
Bit	-	-	-	-	-	-	-	-	-	-	EUnRXF	EUnTXF	EUnFUL	EUnPER	EUnOER	EUnFER
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 6	-	Reserved bits
5	EUnRXF	Indicate Extended UARTn data reception state. 0: Data reception is stopped (Initial value) 1: Data reception is in progress
4	EUnTXF	Indicate Extended UARTn data transmission state. 0: Data transmission is stopped (Initial value) 1: Data transmission is in progress
3	EUnFUL	Indicate transmission buffer state. This bit is set to “1” by writing a data to EUAnBUF1 and reset to “0” when the data is transferred to shift register. To transmit data successively, check that EUnFUL bit is "0" before writing the next transmission data to EUAnBUF1.This bit is forcibly reset to "0" by writing “1” to the EUnFULC bit of EUAnSTAC register. 0: Transmission buffer has no data (Initial value) 1: Transmission buffer has data
2	EUnPER	Indicate a parity error. The parity of the received data and the parity bit added to the data are compared and if they do not match, this bit is set to "1". This bit is forcibly reset to "0" by writing “1” to the EUnPERC bit of EUAnSTAC register. 0: The parity error has not occurred. (Initial value) 1: The parity error has occurred.
1	EUnOER	Indicate a reception overrun error. This bit is set to "1" if the next data is received before reading the previous receive data in reception buffer (EUAnBUFL). Even if reception is stopped by EUnEN bit and then reception is re-started, this bit is set to “1” unless the previously received data is not read. Therefore, reading the data is required from the reception buffer every reception completion even if the data is not required. This is forcibly reset to "0" by writing “1” to the EUnOERC bit of EUAnSTAC register. 0: The overrun error has not occurred (Initial value) 1: The overrun error has occurred
0	EUnFER	Indicate a framing error. This bit is set to "1" when an error occurs in the start/stop bit. EUn0FER bit is forcibly reset to "0" by writing “1” to the UnFERC bit of EUAnSTARC register. 0: The framing error has not occurred (Initial value) 1: The framing error has occurred

14.2.14 Extended UARTn Status Clear Register (EUAnSTAC)

EUAnSTAC is a write-only SFR to clear states of the transmission/reception operation.

Address : 0xF633(EUA0STAC),0xF643(EUA1STAC),0xF653(EUA2STAC)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUAnSTAC							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	EUnFULC	EUnPERC	EUnOERC	EUnFERC
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 3	-	Reserved bits
3	EUnFULC	Clear the state (EUnFUL) of the EUARTn transmit buffer. Writing “0” : Invalid Writing “1” : Clear the UnFUL bit
2	EUnPERC	Clear the parity error bit (EUnPER) of EUARTn. Writing “0” : Invalid Writing “1” : Clear the EUnPER bit.
1	EUnOERC	Clear the EUARTn overrun error bit (EUnOER). Writing “0” : Invalid Writing “1” : Clear the EUnOER bit.
0	EUnFERC	Clear the framing error bit (EUnFER) of EUARTn. Writing “0” : Invalid Writing “1” : Clear the EUnFER bit.

14.2.15 Extended UARTn Control Register (EUAnCON)

EUAnCON is a SFR to control enable/disable communication.

Address : 0xF634(EUA0CON),0xF644(EUA1CON),0xF654E(UA2CON)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUAnCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EUnEN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	EUnEN	Enable the Extended UARTn communication. See section 14.3.4 "Transmission Operation" for details. A both of transmission and reception are enabled when EUnEN = 1. Set “0” to this bit if communication is stopped. 0: communication is Disabled (Initial value) 1: communication is Enabled

[Note]

- **Set the mode/baud rate of the pin and Extended UART before setting the EUnEN bit to "1".**

14.2.16 Extended UARTn Mode Register (EUAnMOD)

EUAnMOD is a SFR to set the transfer mode.

Address : 0xF636(EUA0MODL/EUA0MOD),0xF637(EUA0MODH),
0xF646(EUA1MODL/EUA1MOD),0xF647(EUA1MODH),
0xF656(EUA2MODL/EUA2MOD),0xF657(EUA2MODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EUAnMOD															
Byte	EUAnMODH								EUAnMODL							
Bit	EUnDIR	EUnNEG	EUnSTP	EUnPT2	EUnPT1	EUnPT0	EUnLG1	EUnLG0	-	EUnRSS	-	-	-	-	EUnCK0	-
R/W	R/W	R/W	R/W	R/W	R/w	R/w	R/W	R/W	R	R/W	R	R	R	R	R/W	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	EUnDIR	Select Extended UARTn LSB first or MSB first . 0: LSB first (Initial value) 1: MSB first
14	EUnNEG	Select Extended UARTn positive logic or negative logic. 0: Positive logic (Initial value) 1: Negative logic
13	EUnSTP	Select Extended UARTn stop bit length. 0: 1 stop bit (Initial value) 1: 2 stop bit
12 to 10	EUnPT2 to EUnPT0	Selects Extended UARTn parity bit from even, odd, 0 fixed, 1 fixed, or no parity bit. 000: No parity bit (Initial value) 001: Odd parity 010: No parity bit 011: Even parity 100: No parity bit 101: Parity bit is fixed to “1” 110: No parity bit 111: Parity bit is fixed to “0”
9 to 8	UnLG1 to UnLG0	Select Extended UARTn communication data length. 00: 8-bit length (Initial value) 01: 7-bit length 10: 6-bit length 11: 5-bit length
7	-	Reserved bit
6	UnRSS	Select Extended UARTn sampling timing of the reception data input. 0: (Values set to UAn0BRT registers)/2 (Initial value) 1: {(Values set to UAn0BRT registers)/2} -1
5~2	-	Reserved bits
1	UnCK0	Selects the clock of Extended UARTn baud rate generator 0: LSCLK0 (Initial value) 1: HSCLK
0	-	Reserved bit

[Note]

- **Set EUAnMOD register while communication is stopped, and do not rewrite it while communicating.**

14.2.17 Extended UARTn Interrupt Enable Register (EUAnINTE)

EUAnINTE is a SFR to enable interrupt requests.

Address : 0xF638 (EUA0INTE),0xF648 (EUA1INTE),0xF658 (EUA2INTE)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUAnINTE							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	EUnFIE	EUnTIE	EUnRIE
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits :
It is configured enable/disable a target interrupt
0: Disable a target interrupt (Initial value)
1: Enable a target interrupt

Bit no.	Bit symbol name	Description
7 to 3	-	Reserved bits
2	EUnFIE	Transmission completion interrupt The interrupt occurs when transmission data is transmitted in the condition of transmission buffer empty.
1	EUnTIE	Transmission buffer empty interrupt. The interrupt occurs when transmission buffer becomes empty.
0	EUnRIE	Reception interrupt. The interrupt occurs when data is received.

14.2.18 Extended UARTn Baud Rate Register (EUAnBRT)

EUAnBRT is a SFR to set the count value of the baud rate generator in Extended UARTn.
For details of relation between the count value of the baud rate generator and the baud rate, see Section 14.3.3 “Baud Rate”.

Address : 0xF63A (EUA0BRTL/EUA0BRT), 0xF63B (EUA0BRTH),
0xF64A (EUA1BRTL/EUA1BRT), 0xF64B (EUA1BRTH),
0xF65A (EUA2BRTL/EUA2BRT), 0xF65B (EUA2BRTH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0FFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EUAnBRT															
Byte	EUAnBRTH								EUAnBRTL							
Bit	EUnBR15	EUnBR14	EUnBR13	EUnBR12	EUnBR11	EUnBR10	EUnBR9	EUnBR8	EUnBR7	EUnBR6	EUnBR5	EUnBR4	EUnBR3	EUnBR2	EUnBR1	EUnBR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

[Note]
Set EUAnBRC register while communication is stopped, and do not rewrite it while communicating.

14.2.19 EUARTn Baud Rate Adjustment Register (EUAnBRC)

EUAnBRC is a SFR to adjust the count value of the baud rate generator in UARTn.
For details of relation between the value of EUAnBRC and the correction value, see Section 14.3.3 “Baud Rate”.

Address : 0xF63C(EUA0BRC),0xF64C(EUA1BRC),0xF65C(EUA2BRC)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUAnBRC							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	EUnBRC2	EUnBRC1	EUnBRC0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Note]
Set EUAnBRT register while communication is stopped, and do not rewrite it while communicating.

14.2.20 Extended UART Interrupt Status Register (EUISTAT)

EUISTAT is a read-only SFR to indicates the interrupt status of the extended UART.
ESI2S to ESI0S bits are initialized to "0" by writing "1" to the same bit in ESINTC register in addition to the reset function.

Address : 0xF680(EUISTAT)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								EUISTAT							
Bit	-	-	-	-	-	-	-	-	-	-	EUI21S	EUI20S	EUI11S	EUI10S	EUI01S	EUI00S
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
7 to 6	-	Reserved bits
5	EUI21S	Indicate the status of Extended UART2 transmission interrupt (EUA21INT) 0: No interrupt occurs (initial value) 1: Interrupt occurs
4	EUI20S	Indicate the status of Extended UART2 reception interrupt (EUA20INT) 0: No interrupt occurs (initial value) 1: Interrupt occurs
3	EUI11S	Indicate the status of Extended UART1 transmission interrupt (EUA11INT) 0: No interrupt occurs (initial value) 1: Interrupt occurs
2	EUI10S	Indicate the status of Extended UART1 reception interrupt (EUA10INT) 0: No interrupt occurs (initial value) 1: Interrupt occurs
1	EUI01S	Indicate the status of Extended UART0 transmission interrupt (EUA01INT) 0: No interrupt occurs (initial value) 1: Interrupt occurs
0	EUI00S	Indicate the status of Extended UART0 reception interrupt (EUA00INT) 0: No interrupt occurs (initial value) 1: Interrupt occurs

14.2.21 Extended UART Interrupt Clear Register (EUINTC)

EUINC is a SFR to indicate states of the transmission/reception operation.

Address : 0xF602(UA0STAT),0xF612(UA1STAT),0xF622(UA2STAT)
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EUINTC															
Byte	EUINTCL								UAnSTAT							
Bit	EUIR	-	-	-	-	-	-	-	-	-	EUI21C	EUI20C	EUI11C	EUI10C	EUI01C	EUI00C
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit no.	Bit symbol name	Description
15	EUIR	Request extended UART interrupt. Write “1” before interrupts routine complete and write to IRQ01/IRQ23/IRQ45/IRQ67 registers. “0” writing: invalid “1” writing: Issue the interrupt request again if there is an interrupt factor outstanding for writing.
14 to 6	-	Reserved bits
5	EUI21C	Clear status bit (EUI21S) of extended UART2 transmission interrupt (EUA21INT) “0” writing: invalid “1” writing: clear interrupt status
4	EUI20C	Clear status bit (EUI20S) of extended UART2 transmission interrupt (EUA20INT) “0” writing: invalid “1” writing: clear interrupt status
3	EUI11C	Clear status bit (EUI11S) of extended UART2 transmission interrupt (EUA11INT) “0” writing: invalid “1” writing: clear interrupt status
2	EUI10C	Clear status bit (EUI10S) of extended UART2 transmission interrupt (EUA10INT) “0” writing: invalid “1” writing: clear interrupt status
1	EUI01C	Clear status bit (EUI01S) of extended UART2 transmission interrupt (EUA01INT) “0” writing: invalid “1” writing: clear interrupt status
0	EUI00C	Clear status bit (EUI00S) of extended UART2 transmission interrupt (EUA00INT) “0” writing: invalid “1” writing: clear interrupt status

[Note]

- **Do not set EUIR bit and EUI21C to EUI00C bits simultaneously.**
- **When the CPU writes to the interrupt request register (IRQ01, IRQ23, IRQ45, IRQ67) when an extended external interrupt occurs, the extended UART interrupt status register (EUISTAT) is set, but the interrupt request bit of the extended UART interrupt (QEUA = bit 3 of the IRQ67 register) is not set and the CPU may not be notified of an interrupt.**
- **When writing to IRQ01, IRQ23, IRQ45, or IRQ67, set the EUIR bit of EUINTC register to 1 after the writing and rerequest the interrupt.**
- **Refer to figure 14-12 for extended UART interrupt setting flow.**

14.3 Description of Operation

14.3.1 Frame Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, the following are selectable: 5 to 8 bits for the data bit, even/odd/ fixed to "1", or fixed to "0" for the parity bit, 1 stop bit or 2 stop bit for the stop bit, LSB first or MSB first for the transfer direction, and positive logic or negative logic for the logic of the serial input/output.
All of these are set in the UARTn0 mode register (UAnMOD).
Figure 14-2 shows the input/output format.

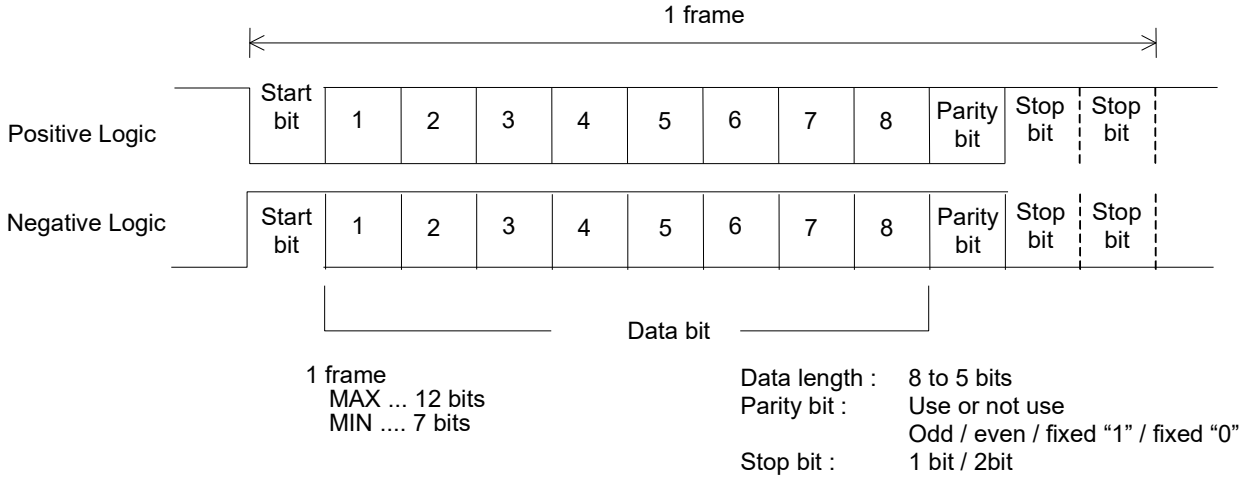
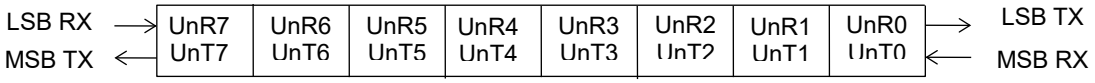


Figure 14-2 Format of Input/Output

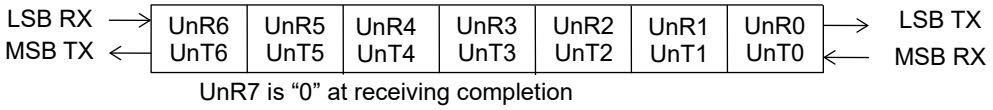
14.3.2 Data Direction

Figure 14-3 shows the relation between the transmission/reception buffer and the data.

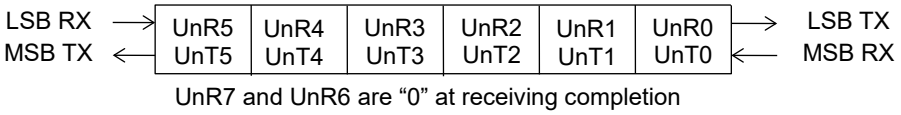
- 8-bit length data



- 7-bit length data



- 6-bit length data



- 5-bit length data

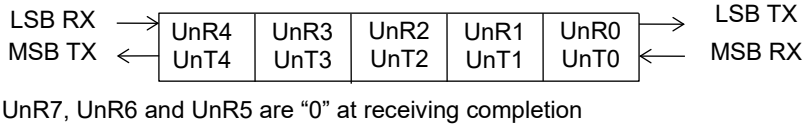


Figure 14-3 Relationship between the Transmission/Reception Buffer and Data

14.3.3 Baud Rate

The baud rate generator generates a baud rate using the base clock selected in UARTn mode register (UAnMOD). The setting values for UARTn baud rate register (UAnBRT) and UARTn baud rate adjustment register (UAnBRC) can be calculated by the following formulae.

UAnBRT = ROUNDDOWN (Base clock frequency (Hz) / Baud rate (bps)) – 1 + Carryover of UAnBRC
UAnBRC = ROUND ((Base clock frequency (Hz) % Baud rate (bps)) × 8 / Baud rate (bps))

where is ROUNDDOWN: Round down, ROUND: Rounded the decimal part, %:Surplus.
Setting range of UAnBRC is 0 to 7. If the calculated value of UAnBRC is 8, add 1 to UAnBRT and set 0 to UAnBRC.

Example (1) : Base clock frequency: Approx.24 MHz (24.002560MHz), Baud rate ideal value: 115,200 bps
24.002560MHz ／ 115,200bps - 1 = 208.35555⋯ - 1 = 207 (round down)
= 0x00CF
(24.002560MHz % 115,200bps) × 8 ／ 115,200bps = 40960 × 8 ／ 115,200
= 2.84444⋯ = 3 (Rounded the decimal part)
= 0x03
UAnBRT = 0x00CF, UAnBRC = 0x03

Example (2) : Base clock frequency: Approx.16MHz (16.007168MHz), Baud rate ideal value:115,200bps
16.007168MHz ／ 115,200bps - 1 = 137.95111⋯ - 1 = 137 (rounding down to the nearest integer)
= 0x0089
(16.007168MHz % 115,200bps) × 8 ／ 115,200bps = 109568 × 8 ／ 115,200
= 7.60888⋯ = 8 (Rounded the decimal part)
= 0x08 UAnBRC carrier over occurred
UAnBRT = 0x0089+1 = 0x008A, UAnBRC = 0x08 = 0x00

The actual baud rate calculated from the setting value for the baud rate can be expressed by the following formula:

Actual baud rate (bps) = [Base clock frequency] / {(UAnBRT + 1) + (UAnBRC / 8)}

Example: Base clock frequency: Approx.24 MHz (23.986176 MHz), Baud rate ideal value: 1200 bps
Actual baud rate (bps) = 24.002560MHz / {(0x4E21 + 1)} + (0x01 / 8)} ≈ 1199.99

Table 14-3 lists the count values for typical baud rates.

Table 14-3 Count Values for Typical Baud Rates

Base clock	Baud rate	UAnBRT	UAnBRC	Actual baud rate
PLL 24MHz (Approx. 24.0025600MHz)	1,200bps	0x4E21	0x01	1200.00bps
	2,400bps	0x2710	0x01	2399.99bps
	4,800bps	0x1387	0x04	4800.03bps
	9,600bps	0x09C3	0x02	9600.06bps
	19,200bps	0x04E1	0x01	19200.13bps
	38,400bps	0x0270	0x01	38396.42bps
	57,600bps	0x019F	0x06	57594.63bps
	115,200bps	0x00CF	0x03	115189.25bps
PLL 16MHz (Approx. 16.007168MHz)	300bps	0xD06C	0x02	300.00bps
	1,200bps	0x341A	0x02	1200.01bps
	2,400bps	0x1A0C	0x05	2400.01bps
	4,800bps	0x0D05	0x07	4799.93bps
	9,600bps	0x0682	0x03	9600.22bps
	19,200bps	0x0340	0x06	19199.00bps
	38,400bps	0x019F	0x07	38398.00bps
	57,600bps	0x0114	0x07	57605.64bps
	115,200bps	0x008A	0x00	115159.48bps
PLL 1MHz (Approx. 0.999424MHz)	300bps	0x0D02	0x03	300.00bps
	1,200bps	0x033F	0x07	1199.97bps
	2,400bps	0x019F	0x03	2400.30bps
	4,800bps	0x00CF	0x02	4799.16bps
	9,600bps	0x0067	0x01	9598.31bps
	19,200bps	0x0033	0x00	19219.69bps
	38,400bps	0x0019	0x00	38439.39bps
	57,600bps	0x0010	0x03	57520.81bps
	115,200bps	0x0007	0x05	115875.25bps
32.768kHz	200bps	0x00A2	0x07	199.95bps
	300bps	0x006C	0x02	299.93bps
	1,200bps	0x001A	0x02	1202.49bps
	2,400bps	0x000C	0x05	2404.99bps
	4,800bps	0x0005	0x07	4766.25bps

14.3.4 Transmission Operation

Transmission is started by setting UnEN bit of UARTn control register (UAnCON) to "1" and set transfer data to UAnBUF1. UAnEN setting and UAnBUF1 setting are random order.
Figure 14-4 shows the operation timing for transmission.

When UnEN bit is set to "1", the transmission status; UnTXF is set to “1” after 2 cycles of the system clock. (at (1))
An internal transfer clock of baud rate supplies after 2 cycles of the base clock (LSCLK0/HSCLK), and then the start bit is output the TXD pin. (at (2)) Subsequently, the transmitted data, a parity bit, and a stop bit are output.
When the start bit is output, the transmission buffer status flag; UnFUL is return to “0” and the transmission interrupt is requested on the rising edge of the internal transfer clock. (at (3)) In UARTn transmission interrupt routine, the next data to be transmitted is written to the transmission buffer (UAnBUF1). Then UnFUL is set to "1". It is same as (2) after transmission of the stop bit (at (4)). At this time if the UART transmission interrupt routine is terminated without writing the next data to the transmit buffer; it means the stop-bit is sent when UnFUL is not set to “1”, transmission is stop. Then UnTXF bit is reset to "0", and the UART transmission interrupt is requested. (at (5))
The valid period for the next transmission data to be written to the transmission buffer is from when UnFUL bit becomes “0” after the interrupt occurs to the termination of stop bit transmission. (at (6))

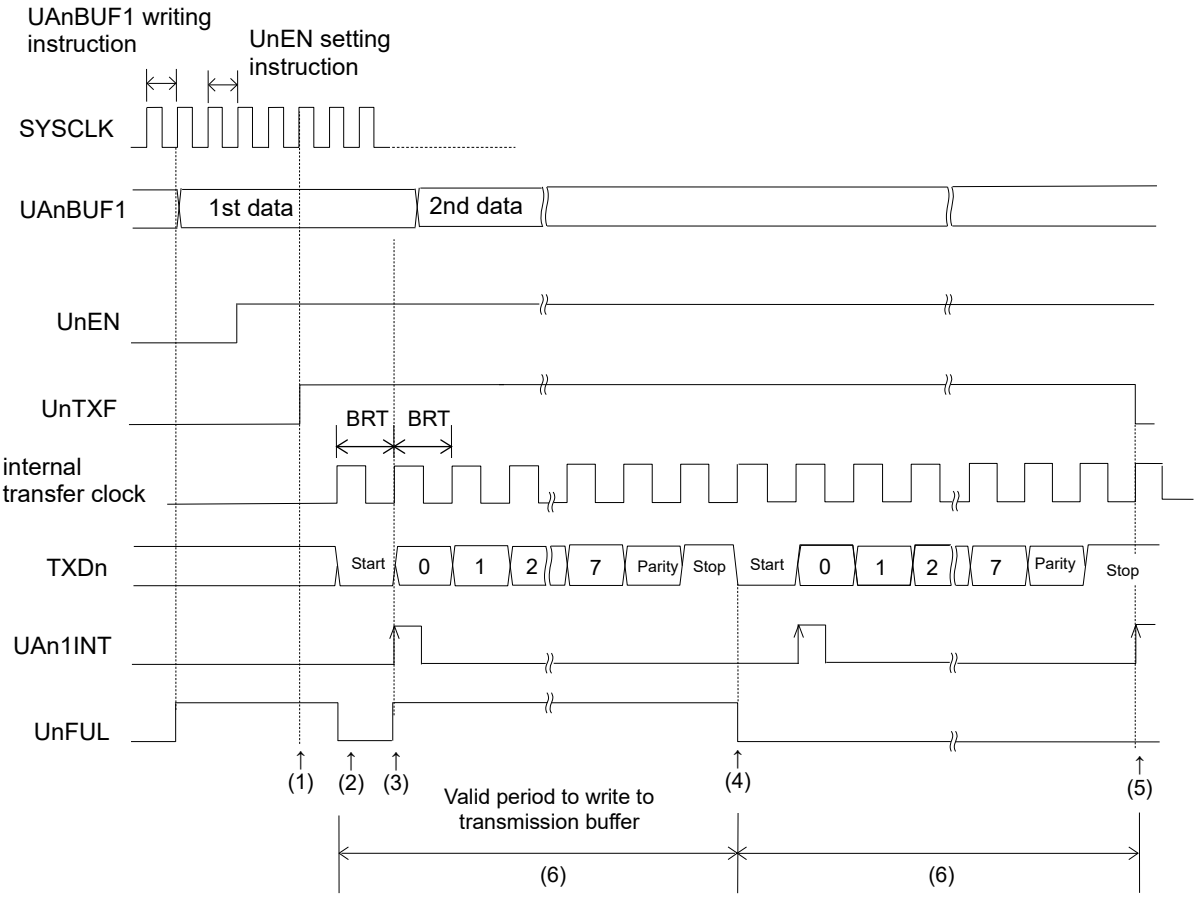


Figure 14-4 Transmission Timing

[Note]

- **When UnFUL bit of UARTn status register (UAnSTAT) is set to "1" and UnEN bit of UARTn control register (UAnCON) is written to "1", transmission starts immediately. If the transmission data is not ready in UARTn transmit buffer (UAnBUF1), or if reception is allowed first, write "1" to the UnFUL bit of UAnSTAC, reset UnFUL bit, and then write "1" to UnEN bit of UAnCON to allow transmission and reception.**

14.3.5 Reception Operation

A reception is started by setting UnEN bit of UART n control register (UAnCON) to "1".
Figure 14-5 shows the operation timing for reception.

When a reception starts, this module checks the data sent to the input pin RXD and waits for the arrival of a start bit. When detecting a start bit ((2) in Figure 14-5), It generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs reception operation.
The shift register shifts in the data input to RXD on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit received data is transferred to the reception buffer (UAnBUF0) concurrently with the falling edge of the internal transfer clock of (3) in Figure 14-5.
This module requests a UART reception interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched ((4) in Figure 14-5) and checks for a stop bit error and a parity bit error. When an error is detected, this module sets the corresponding bit of the UART n status register (UAnSTAT) to "1".

Parity error : UnPER ="1"
Overrun error: UnOER ="1"
Framing error: UnFER ="1"

As shown in Figure 14-5, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
A reception continues until the UnEN bit is reset to "0" by the program. When the UnEN bit is reset to "0" during reception, the received data may be destroyed. When the UnEN bit is reset to "0" during the "UnEN reset enable period" in Figure 14-5, the received data is protected.

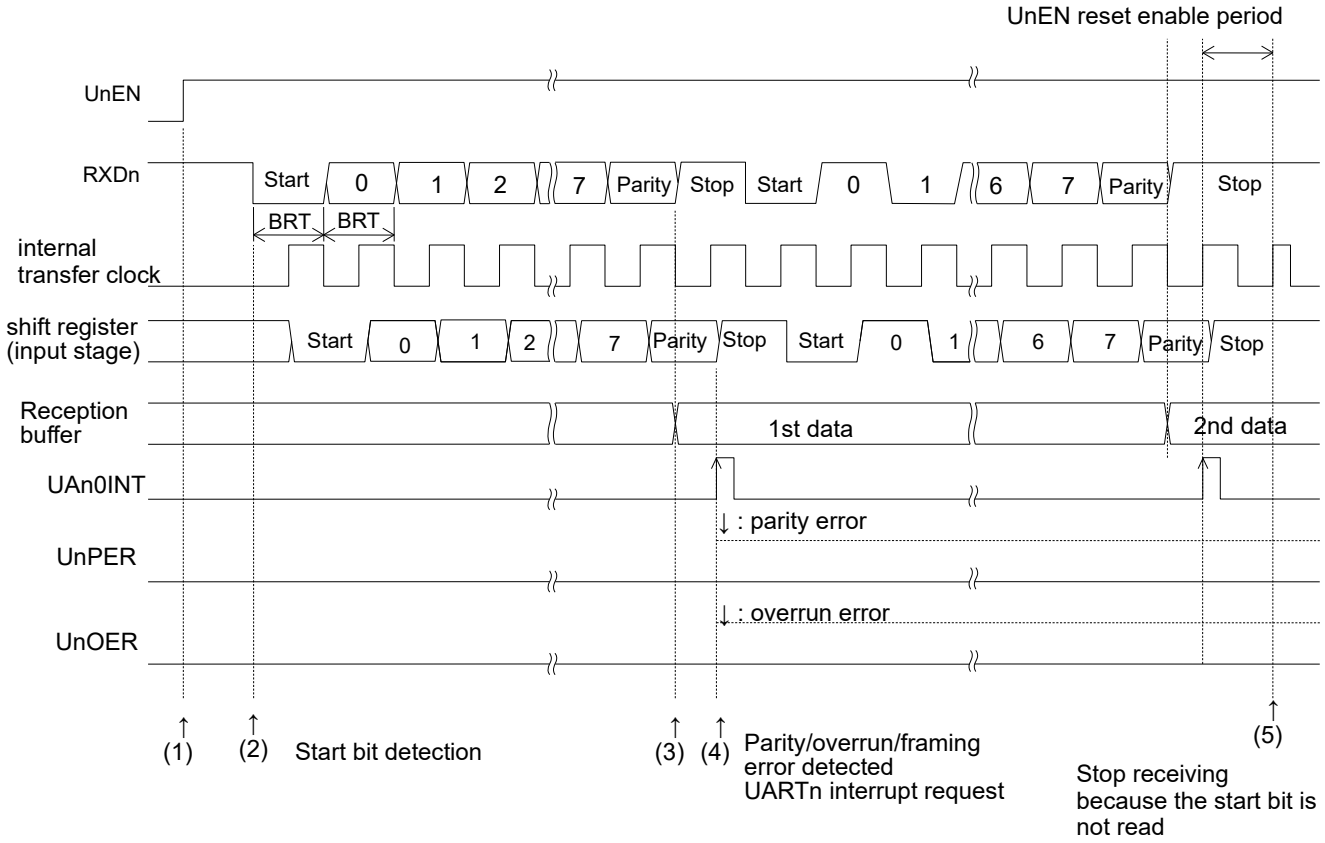


Figure 14-5 Reception Timing

14.3.5.1 Detection of Start Bit

The start bit is sampled with the baud rate generator clock selected by the UnCK0 bit of the UAnMOD register. Therefore, the start bit detection may be delayed for one cycle of the baud rate generator clock at the maximum. Figure 14-6 shows the start bit detection timing.

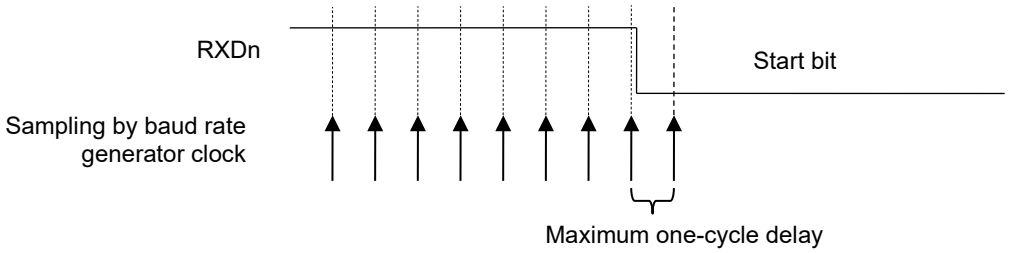
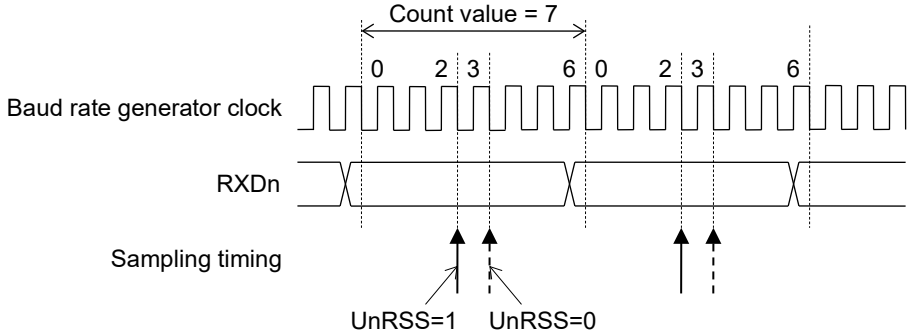


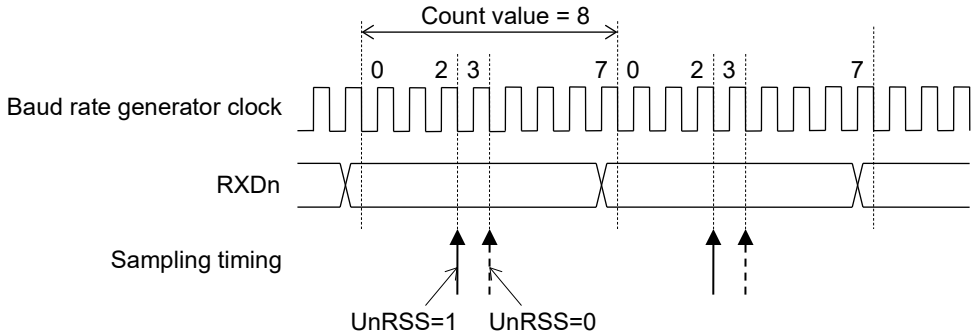
Figure 14-6 Start Bit Detection Timing (with Positive Logic)

14.3.5.2 Sampling Timing

When the start bit is detected, the received data that was input to RXDn is sampled almost at the center of the baud rate, and then loaded to the shift register.
This sampling timing the shift register uses to load data can be adjusted for one clock of the baud rate generator clock in the UnRSS bit of the UART n mode register (UAnMOD).
Figure 14-7 shows the relationship between the UnRSS bit and the sampling timing.



(1) When the baud rate generator count value is "7" (odd)



(2) When the baud rate generator count value is "8" (even)

Figure 14-7 Relationship between UnRSS Bit and Sampling Timing

14.3.5.3 Receiving Margin

If there is an error between the sender baud rate and the receiver baud rate generated by the baud rate generator, the error accumulates until the last stop bit loading in one frame, decreasing the reception margin.
Figure 14-8 shows the baud rate errors and reception margin waveforms.

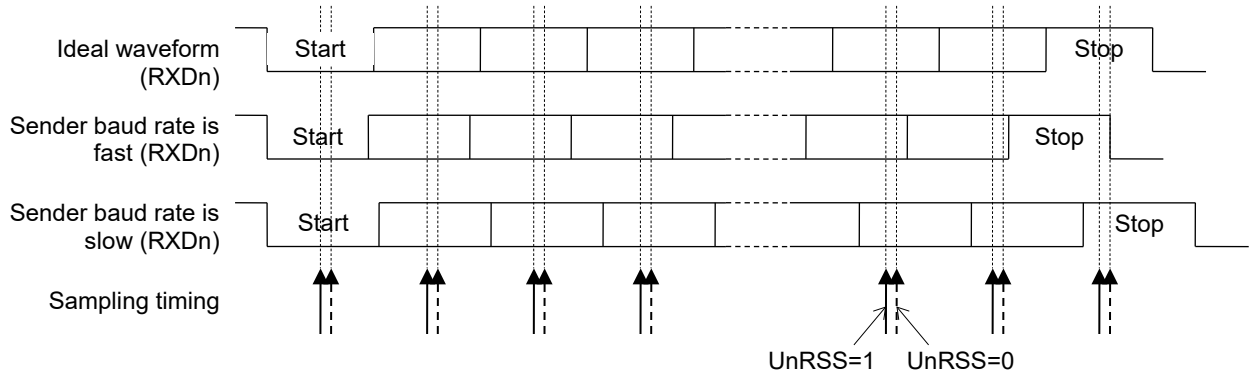


Figure 14-8 Baud Rate Errors and Reception Margin

[Note]

- **When designing the system, consider the difference of the baud rate between the transmission side and reception side, a delay of the start bit detection, signal degradation and noise influence, then adjust the baud rate and reception timing to ensure sufficient receiving margin.**

14.3.5.4 Reception Filter

This unit has reception data filter for a noise reduction. Figure 14-9 shows the RXD0 waveform before/after noise reduction.

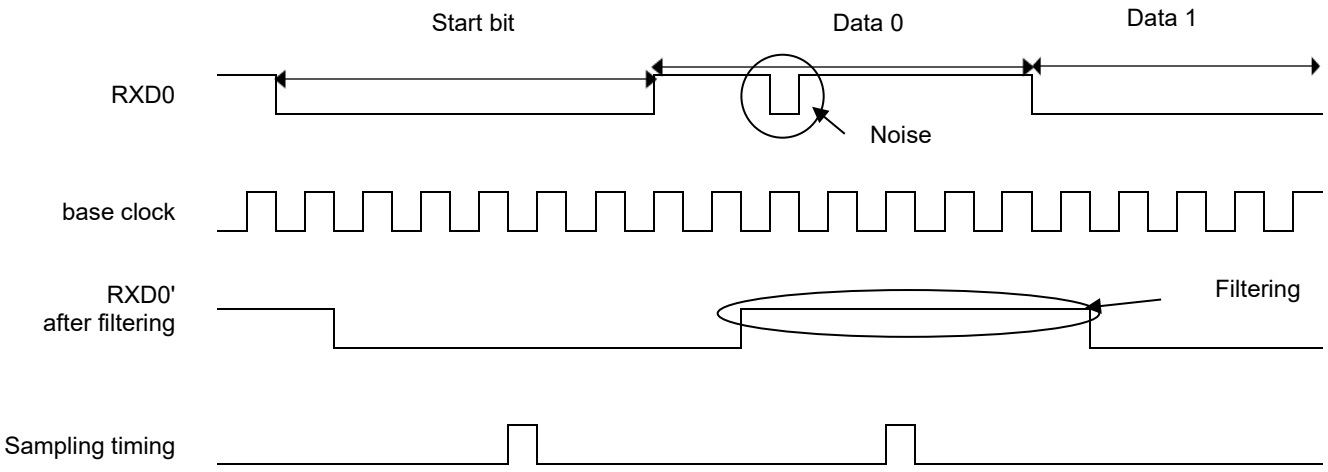


Figure 14-9 Noise reduction

14.3.6 Interrupt

Figure 14-10 shows the interrupt timing.
The transmission empty interrupt is occurred as UAn1INT at the end of start-bit after a transmission buffer becomes empty. The status is UnFUL=0 and UnTXF=1.
The transmission completion interrupt is occurred as UAn1INT when a transmission is completed in condition of that the transmission buffer is empty. The status is UnFUL=0, UnTXF=0.
The reception interrupt is occurred as UAn0INT when reception data is stored in the buffer.

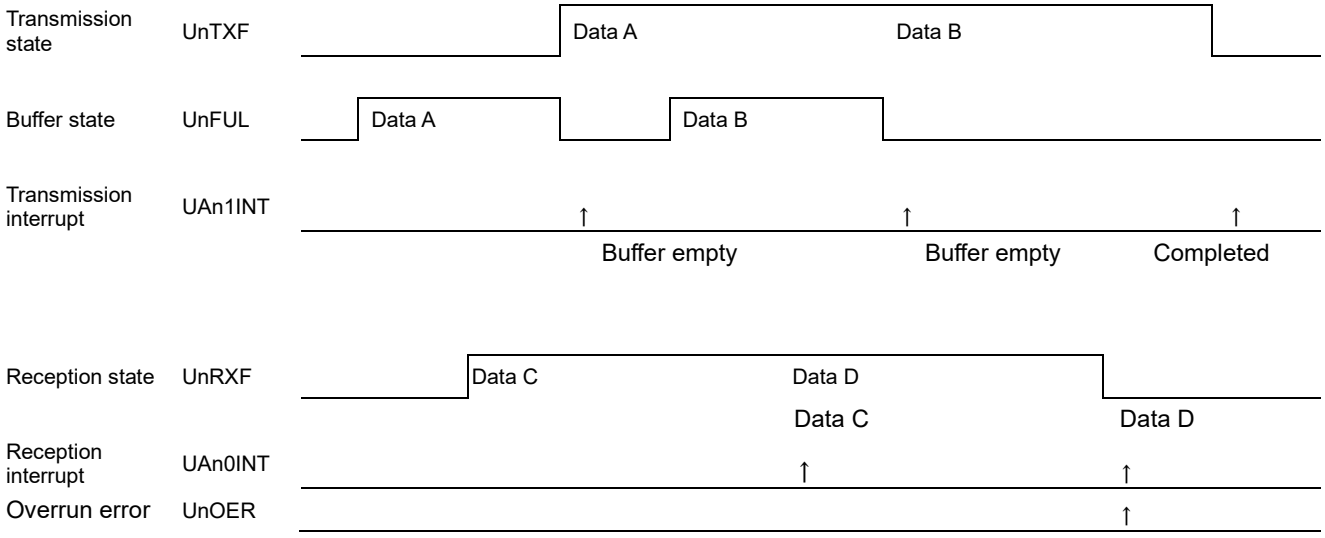
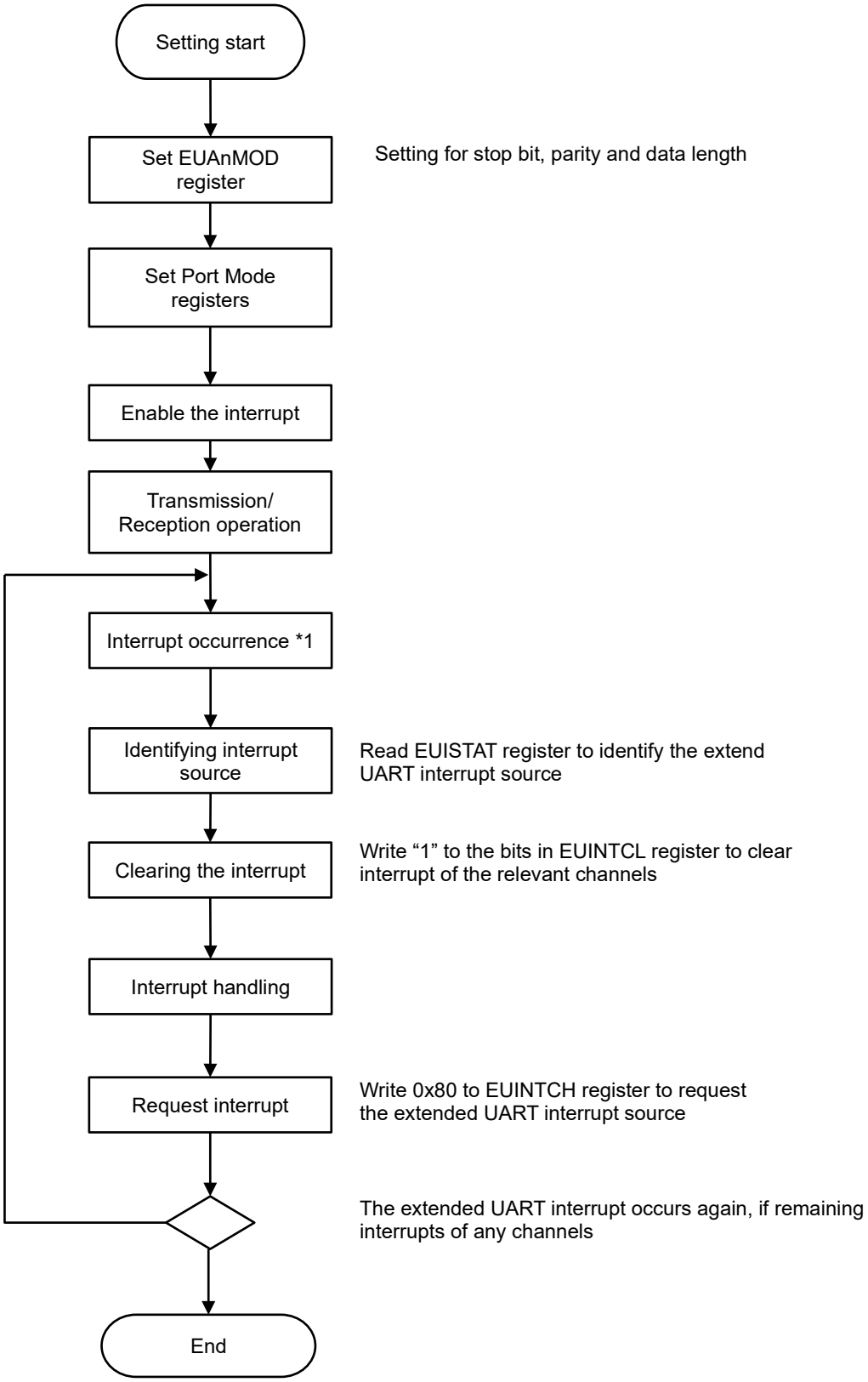


Figure 14-10 Interrupt Timing

Figure 14-11 shows a setting flow of the extend UART interrupt.



*1: Re-request interrupt by writing “1” to EUIR bit of the EUINTC register when interrupt request register (IRQ01, IRQ23, IRQ45, IRQ67) are written by CPU while extended UART interrupt is enabled.

Figure14-11 Extended UART Interrupt Setting Flow

Chapter 17 GPIO

17. GPIO

17.1 General Description

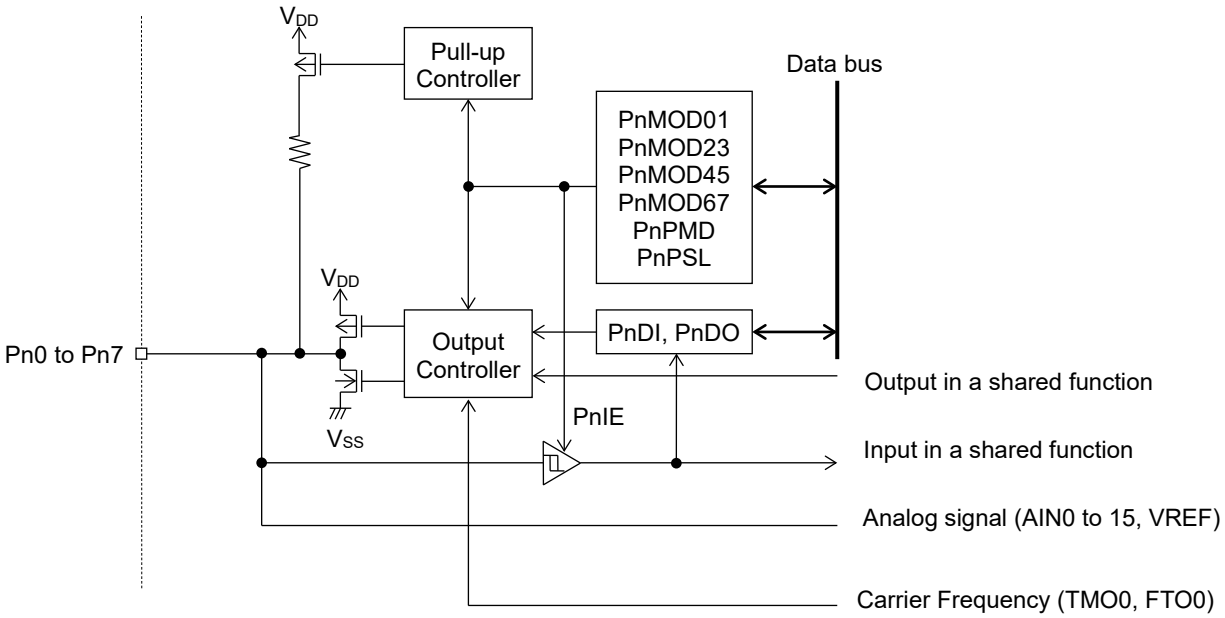
There are two type of general purpose port (GPIO): input only port (GPI) and input/output port (GPI/O).
The general purpose input/output port is capable of switching the input/output direction for each terminal.
In addition, up to 8 terminals can be read out and output levels can be changed simultaneously. General-purpose input/output ports combine multiple functions.
See "1.3.2 List of Pins" or "1.3.3 Description of Pins" for more detail.
The general purpose input port is an input-only port that can also be used as a crystal connection terminal and a debug/ISP interface.
The number of general purpose ports varies depending on the product.
See Table 17-1 "List of Pins".

17.1.1 Features

- Input or output is selectable for each pin
- Pull-up resistor is selectable for each pin
- CMOS output or N-channel open drain output is selectable for each pin
- Direct driving LEDs is supported when the N-channel open drain output is selected
- Carrier frequency output function
- Port output level test function

17.1.2 Configuration

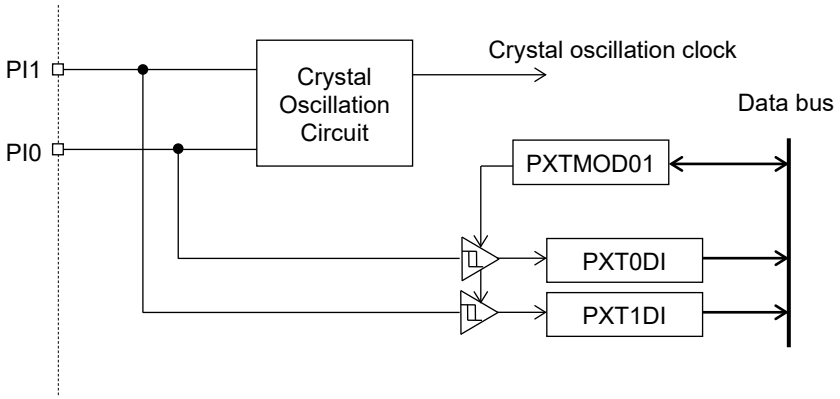
Figure 17-1 shows the configuration of the general purpose port. See "17.2.1 List of registers" for available pins and registers.



PnDI : Port n data register (bit 7 to 0)
PnDO : Port n data register (bit 15 to 8)
PnMOD01 : Port n mode register 01
PnMOD23 : Port n mode register 23
PnMOD45 : Port n mode register 45
PnMOD67 : Port n mode register 67
PnPMD : Port n pulse mode register
PnPSL : Port n pulse selection register

Figure 17-1 Configuration of GPI/O port n

Figure 17-2 shows the configuration of the GPI; PI0/PI1.



PXT0DI : PORTXT data input register (bit 0)
PXT1DI : PORTXT data input register (bit 1)
PXTMOD01 : PORTXT mode register01

Figure 17-2 Configuration of GPI; PI0/PI1

17.1.3 List of Pins

Table 17-1 List of Pins (●: available, -: Not available)

Pin Name	Primary Function	ML62Q2700 group				
		48pin product	52pin product	64pin product	80pin product	100pin product
XT0	GPI(PI0) / Crystal resonator connection	●	●	●	●	●
XT1	GPI(PI1) / Crystal resonator connection	●	●	●	●	●
P01/TEST0	Input port	●	●	●	●	●
P02	I/O port / EXI0	●	●	●	●	●
P03	I/O port / EXI1	●	●	●	●	●
P04	I/O port / EXI2	●	●	●	●	●
P05	I/O port	●	●	●	●	●
P06	I/O port	●	●	●	●	●
P07	I/O port	●	●	●	●	●
P10	I/O port	●	●	●	●	●
P11	I/O port /EXI1	●	●	●	●	●
P12	I/O port /EXI6	●	●	●	●	●
P13	I/O port /EXI7	●	●	●	●	●
P14	I/O port /EXI2	●	●	●	●	●
P15	I/O port	●	●	●	●	●
P16	I/O port	●	●	●	●	●
P17	I/O port /EXI3	●	●	●	●	●
P20	I/O port	●	●	●	●	●
P21	I/O port /EXI4	●	●	●	●	●
P22	I/O port	●	●	●	●	●
P23	I/O port /EXI5	●	●	●	●	●
P24	I/O port	●	●	●	●	●
P25	I/O port	●	●	●	●	●
P26	I/O port /EXI6	●	●	●	●	●
P27	I/O port /EXI7	●	●	●	●	●
P30	I/O port	●	●	●	●	●
P31	I/O port /EXI1	●	●	●	●	●
P32	I/O port	●	●	●	●	●
P33	I/O port /EXI2	●	●	●	●	●
P40	I/O port	-	-	●	●	●
P41	I/O port /EXI0	-	●	●	●	●
P42	I/O port	-	-	●	●	●
P43	I/O port /EXI7	●	●	●	●	●
P44	I/O port /EXI2	-	-	●	●	●
P45	I/O port /EXI3	-	-	●	●	●
P46	I/O port /EXI4	-	-	●	●	●
P47	I/O port /EXI5	-	●	●	●	●
P50	I/O port /EXI8	●	●	●	●	●
P51	I/O port /EXI3	-	●	●	●	●
P52	I/O port /EXI4	-	-	●	●	●
P53	I/O port /EXI5	-	-	●	●	●
P54	I/O port /EXI0	-	-	●	●	●
P55	I/O port /EXI1	-	-	●	●	●

Pin Name	Primary Function	ML62Q2700 group				
		48pin product	52pin product	64pin product	80pin product	100pin product
P56	I/O port	-	●	●	●	●
P57	I/O port	-	-	●	●	●
P60	I/O port	●	●	●	●	●
P61	I/O port /EXI3	●	●	●	●	●
P62	I/O port	●	●	●	●	●
P63	I/O port /EXI4	●	●	●	●	●
P64	I/O port /EXI9	●	●	●	●	●
P65	I/O port /EXI5	●	●	●	●	●
P66	I/O port	●	●	●	●	●
P67	I/O port /EXI6	-	-	●	●	●
P70	I/O port /EXI0	-	-	●	●	●
P76	I/O port /EXI10	-	-	-	●	●
P77	I/O port	-	-	-	-	●
P80	I/O port /EXI6	-	-	-	●	●
P81	I/O port /EXI7	-	-	-	●	●
P82	I/O port	-	-	-	●	●
P83	I/O port	-	-	-	-	●
P84	I/O port	-	-	-	-	●
P85	I/O port	-	-	-	-	●
P86	I/O port	-	-	-	-	●
P87	I/O port	-	-	-	-	●
P90	I/O port	-	-	-	-	●
P91	I/O port	-	-	-	-	●
P92	I/O port	-	-	-	-	●
P93	I/O port	-	-	-	●	●
P94	I/O port	-	-	-	●	●
P95	I/O port	-	-	-	●	●
P96	I/O port	-	-	-	●	●
P97	I/O port	-	-	-	-	●
PA0	I/O port	-	-	-	-	●
PA1	I/O port	-	-	-	-	●
PA2	I/O port	-	-	-	-	●
PA3	I/O port /EXI11	-	-	-	●	●
PA4	I/O port	-	-	-	●	●
PA5	I/O port	-	-	-	-	●
PA6	I/O port	-	-	-	-	●
PA7	I/O port	-	-	-	-	●
PB0	I/O port	-	-	-	-	●
PB1	I/O port	-	-	-	-	●
PB2	I/O port	-	-	-	●	●
PB3	I/O port	-	-	-	●	●
PB4	I/O port	-	-	-	●	●
PB5	I/O port	-	-	-	●	●
PB6	I/O port	-	-	-	-	●
PB7	I/O port	-	-	-	-	●

17.2 Description of Registers

17.2.1 List of Registers

Writing to SFRs of unequipped port is not available. PnDI return 0xFF for reading. Other SFRs return 0x0000/0x00 for reading.

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF200	Port 0 data register	P0DI	P0D	R	8/16	0xFF
0xF201		P0DO		R/W	8	0x00
0xF202	Reserved register	-	-	-	-	-
0xF203	Port 0 mode register 1	P0MOD1	-	R/W	8/16	0x05
0xF204	Port 0 mode register 23	P0MOD2	P0MOD23	R/W	8/16	0x00
0xF205		P0MOD3		R/W	8	0x00
0xF206	Port 0 mode register 45	P0MOD4	P0MOD45	R/W	8/16	0x00
0xF207		P0MOD5		R/W	8	0x00
0xF208	Port 0 mode register 67	P0MOD6	P0MOD67	R/W	8/16	0x00
0xF209		P0MOD7		R/W	8	0x00
0xF20A	Port 0 pulse mode register	P0PMDL	P0PMD	R/W	8/16	0x00
0xF20B		P0PMDH		R/W	8	0x00
0xF20C	Port 0 pulse selection register	P0PSLL	P0PSL	R/W	8/16	0x00
0xF20D		P0PSLH		R/W	8	0x00
0xF20E	Reserved register	-	-	-	-	-
0xF20F						
0xF210	Port 1 data register	P1DI	P1D	R	8/16	0xFF
0xF211		P1DO		R/W	8	0x00
0xF212	Port 1 mode register 01	P1MOD0	P1MOD01	R/W	8/16	0x00
0xF213		P1MOD1		R/W	8	0x00
0xF214	Port 1 mode register 23	P1MOD2	P1MOD23	R/W	8/16	0x00
0xF215		P1MOD3		R/W	8	0x00
0xF216	Port 1 mode register 45	P1MOD4	P1MOD45	R/W	8/16	0x00
0xF217		P1MOD5		R/W	8	0x00
0xF218	Port 1 mode register 67	P1MOD6	P1MOD67	R/W	8/16	0x00
0xF219		P1MOD7		R/W	8	0x00
0xF21A	Port 1 pulse mode register	P1PMDL	P1PMD	R/W	8/16	0x00
0xF21B		P1PMDH		R/W	8	0x00
0xF21C	Port 1 pulse selection register	P1PSLL	P1PSL	R/W	8/16	0x00
0xF21D		P1PSLH		R/W	8	0x00
0xF21E	Reserved register	-	-	-	-	-
0xF21F						
0xF220	Port 2 data register	P2DI	P2D	R	8/16	0xFF
0xF221		P2DO		R/W	8	0x00
0xF222	Port 2 mode register 01	P2MOD0	P2MOD01	R/W	8/16	0x00
0xF223		P2MOD1		R/W	8	0x00
0xF224	Port 2 mode register 23	P2MOD2	P2MOD23	R/W	8/16	0x00
0xF225		P2MOD3		R/W	8	0x00
0xF226	Port 2 mode register 45	P2MOD4	P2MOD45	R/W	8/16	0x00
0xF227		P2MOD5		R/W	8	0x00
0xF228	Port 2 mode register 67	P2MOD6	P2MOD67	R/W	8/16	0x00
0xF229		P2MOD7		R/W	8	0x00
0xF22A	Port 2 pulse mode register	P2PMDL	P2PMD	R/W	8/16	0x00
0xF22B		P2PMDH		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF22C	Port 2 pulse selection register	P2PSLL	P2PSL	R/W	8/16	0x00
0xF22D		P2PSLH		R/W	8	0x00
0xF22E	Reserved register	-	-	-	-	-
0xF22F						
0xF230	Port 3 data register	P3DI	P3D	R	8/16	0xFF
0xF231		P3DO		R/W	8	0x00
0xF232	Port 3 mode register 01	P3MOD0	P3MOD01	R/W	8/16	0x00
0xF233		P3MOD1		R/W	8	0x00
0xF234	Port 3 mode register 23	P3MOD2	P3MOD23	R/W	8/16	0x00
0xF235		P3MOD3		R/W	8	0x00
0xF236 to 0xF29	Reserved register	-	-	-	-	-
0xF23A	Port 3 pulse mode register	P3PMDL	P3PMD	R/W	8/16	0x00
0xF23B		P3PMDH		R/W	8	0x00
0xF23C	Port 3 pulse selection register	P3PSLL	P3PSL	R/W	8/16	0x00
0xF23D		P3PSLH		R/W	8	0x00
0xF23E	Reserved register	-	-	-	-	-
0xF23F						
0xF240	Port 4 data register	P4DI	P4D	R	8/16	0xFF
0xF241		P4DO		R/W	8	0x00
0xF242	Port 4 mode register 01	P4MOD0	P4MOD01	R/W	8/16	0x00
0xF243		P4MOD1		R/W	8	0x00
0xF244	Port 4 mode register 23	P4MOD2	P4MOD23	R/W	8/16	0x00
0xF245		P4MOD3		R/W	8	0x00
0xF246	Port 4 mode register 45	P4MOD4	P4MOD45	R/W	8/16	0x00
0xF247		P4MOD5		R/W	8	0x00
0xF248	Port 4 mode register 67	P4MOD6	P4MOD67	R/W	8/16	0x00
0xF249		P4MOD7		R/W	8	0x00
0xF24A to 0xF24F	Reserved register	-	-	-	-	-
0xF250	Port 5 data register	P5DI	P5D	R	8/16	0xFF
0xF251		P5DO		R/W	8	0x00
0xF252	Port 5 mode register 01	P5MOD0	P5MOD01	R/W	8/16	0x00
0xF253		P5MOD1		R/W	8	0x00
0xF254	Port 5 mode register 23	P5MOD2	P5MOD23	R/W	8/16	0x00
0xF255		P5MOD3		R/W	8	0x00
0xF256	Port 5 mode register 45	P5MOD4	P5MOD45	R/W	8/16	0x00
0xF257		P5MOD5		R/W	8	0x00
0xF258	Port 5 mode register 67	P5MOD6	P5MOD67	R/W	8/16	0x00
0xF259		P5MOD7		R/W	8	0x00
0xF25A to 0xF25F	Reserved register	-	-	-	-	-
0xF260	Port 6 data register	P6DI	P6D	R	8/16	0xFF
0xF261		P6DO		R/W	8	0x00
0xF262	Port 6 mode register 01	P6MOD0	P6MOD01	R/W	8/16	0x00
0xF263		P6MOD1		R/W	8	0x00
0xF264	Port 6 mode register 23	P6MOD2	P6MOD23	R/W	8/16	0x00
0xF265		P6MOD3		R/W	8	0x00
0xF266	Port 6 mode register 45	P6MOD4	P6MOD45	R/W	8/16	0x00
0xF267		P6MOD5		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF268	Port 6 mode register 67	P6MOD6	P6MOD67	R/W	8/16	0x00
0xF269		P6MOD7		R/W	8	0x00
0xF26A to 0xF26F	Reserved register	-	-	-	-	-
0xF270	Port 7 data register	P7DI	P7D	R	8/16	0xFF
0xF271		P7DO		R/W	8	0x00
0xF272	Port 7 mode register 01	P7MOD0	P7MOD01	R/W	8/16	0x00
0xF273 to 0xF277	Reserved register	-	-	-	-	-
0xF278	Port 7 mode register 67	P7MOD6	P7MOD67	R/W	8/16	0x00
0xF279		P7MOD7		R/W	8	0x00
0xF27A to 0xF27F	Reserved register	-	-	-	-	-
0xF280	Port 8 data register	P8DI	P8D	R	8/16	0xFF
0xF281		P8DO		R/W	8	0x00
0xF282	Port 8 mode register 01	P8MOD0	P8MOD01	R/W	8/16	0x00
0xF283		P8MOD1		R/W	8	0x00
0xF284	Port 8 mode register 23	P8MOD2	P8MOD23	R/W	8/16	0x00
0xF285		P8MOD3		R/W	8	0x00
0xF286	Port 8 mode register 45	P8MOD4	P8MOD45	R/W	8/16	0x00
0xF287		P8MOD5		R/W	8	0x00
0xF288	Port 8 mode register 67	P8MOD6	P8MOD67	R/W	8/16	0x00
0xF289		P8MOD7		R/W	8	0x00
0xF28A to 0xF28F	Reserved register	-	-	-	-	-
0xF290	Port 9 data register	P9DI	P9D	R	8/16	0xFF
0xF291		P9DO		R/W	8	0x00
0xF292	Port 9 mode register 01	P9MOD0	P9MOD01	R/W	8/16	0x00
0xF293		P9MOD1		R/W	8	0x00
0xF294	Port 9 mode register 23	P9MOD2	P9MOD23	R/W	8/16	0x00
0xF295		P9MOD3		R/W	8	0x00
0xF296	Port 9 mode register 45	P9MOD4	P9MOD45	R/W	8/16	0x00
0xF297		P9MOD5		R/W	8	0x00
0xF298	Port 9 mode register 67	P9MOD6	P9MOD67	R/W	8/16	0x00
0xF299		P9MOD7		R/W	8	0x00
0xF29A to 0xF29F	Reserved register	-	-	-	-	-
0xF2A0	Port A data register	PADI	PAD	R	8/16	0xFF
0xF2A1		PADO		R/W	8	0x00
0xF2A2	Port A mode register 01	PAMOD0	PAMOD01	R/W	8/16	0x00
0xF2A3		PAMOD1		R/W	8	0x00
0xF2A4	Port A mode register 23	PAMOD2	PAMOD23	R/W	8/16	0x00
0xF2A5		PAMOD3		R/W	8	0x00
0xF2A6	Port A mode register 45	PAMOD4	PAMOD45	R/W	8/16	0x00
0xF2A7		PAMOD5		R/W	8	0x00
0xF2A8	Port A mode register 67	PAMOD6	PAMOD67	R/W	8/16	0x00
0xF2A9		PAMOD7		R/W	8	0x00
0xF2AA to 0xF2AF	Reserved register	-	-	-	-	-
0xF2B0	Port B data register	PBDI	PBD	R	8/16	0xFF
0xF2B1		PBDO		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF2B2	Port B mode register 01	PBMOD0	PBMOD01	R/W	8/16	0x00
0xF2B3		PBMOD1		R/W	8	0x00
0xF2B4	Port B mode register 23	PBMOD2	PBMOD23	R/W	8/16	0x00
0xF2B5		PBMOD3		R/W	8	0x00
0xF2B6	Port B mode register 45	PBMOD4	PBMOD45	R/W	8/16	0x00
0xF2B7		PBMOD5		R/W	8	0x00
0xF2B8	Port B mode register 67	PBMOD6	PBMOD67	R/W	8/16	0x00
0xF2B9		PBMOD7		R/W	8	0x00
0xF2BA to 0xF2EF	Reserved register	-	-	-	-	-
0xF2F0	PORTXT data input register	PXTDI	—	R	8	0x03
0xF2F1	Reserved register	-	-	-	-	-
0xF2F2	PORTXT mode register 01	PXTMOD0	PXTMOD01	R/W	8/16	0x00
0xF2F3		PXTMOD1		R/W	8	0x00
0xF2F4 to 0xF2FF	Reserved register	-	-	-	-	-

Table 17-2 List of Registers / Bits

Port Name	Pin Name	Control register / bit						Available				
		Port n data register (PnD)		Port n mode register m (PnMODm)	Port n pulse mode register (PnPMD)		Port n pulse selection register (PnPSL)	48pin product	52pin product	64pin product	80pin product	100pin product
Port XT	PI00	-	PXT0DI	PXTMOD0	-	-	-	●	●	●	●	●
	PI01	-	PXT1DI	PXTMOD1	-	-	-	●	●	●	●	●
Port 0	P01	-	P01DI	P0MOD1	-	-	-	●	●	●	●	●
	P02	P02DO	P02DI	P0MOD2	-	-	-	●	●	●	●	●
	P03	P03DO	P03DI	P0MOD3	P03PLVL	P03PEN	P03PSL	●	●	●	●	●
	P04	P04DO	P04DI	P0MOD4	-	-	-	●	●	●	●	●
	P05	P05DO	P05DI	P0MOD5	-	-	-	●	●	●	●	●
	P06	P06DO	P06DI	P0MOD6	-	-	-	●	●	●	●	●
	P07	P07DO	P07DI	P0MOD7	-	-	-	●	●	●	●	●
Port 1	P10	P10DO	P10DI	P1MOD0	-	-	-	●	●	●	●	●
	P11	P11DO	P11DI	P1MOD1	P11PLVL	P11PEN	P11PSL	●	●	●	●	●
	P12	P12DO	P12DI	P1MOD2	-	-	-	●	●	●	●	●
	P13	P13DO	P13DI	P1MOD3	P13PLVL	P13PEN	P13PSL	●	●	●	●	●
	P14	P14DO	P14DI	P1MOD4	-	-	-	●	●	●	●	●
	P15	P15DO	P15DI	P1MOD5	-	-	-	●	●	●	●	●
	P16	P16DO	P16DI	P1MOD6	-	-	-	●	●	●	●	●
	P17	P17DO	P17DI	P1MOD7	-	-	-	●	●	●	●	●
Port 2	P20	P20DO	P20DI	P2MOD0	P20PLVL	P20PEN	P20PSL	●	●	●	●	●
	P21	P21DO	P21DI	P2MOD1	-	-	-	●	●	●	●	●
	P22	P22DO	P22DI	P2MOD2	P22PLVL	P22PEN	P22PSL	●	●	●	●	●
	P23	P23DO	P23DI	P2MOD3	-	-	-	●	●	●	●	●
	P24	P24DO	P24DI	P2MOD4	-	-	-	●	●	●	●	●
	P25	P25DO	P25DI	P2MOD5	P25PLVL	P25PEN	P25PSL	●	●	●	●	●
	P26	P26DO	P26DI	P2MOD6	-	-	-	●	●	●	●	●
	P27	P27DO	P27DI	P2MOD7	P27PLVL	P27PEN	P27PSL	●	●	●	●	●
Port 3	P30	P30DO	P30DI	P3MOD0	-	-	-	●	●	●	●	●
	P31	P31DO	P31DI	P3MOD1	-	-	-	●	●	●	●	●
	P32	P32DO	P32DI	P3MOD2	-	-	-	●	●	●	●	●
	P33	P33DO	P33DI	P3MOD3	P33PLVL	P33PEN	P33PSL	●	●	●	●	●
Port 4	P40	P40DO	P40DI	P4MOD0	-	-	-	-	-	●	●	●
	P41	P41DO	P41DI	P4MOD1	-	-	-	-	●	●	●	●
	P42	P42DO	P42DI	P4MOD2	-	-	-	-	-	●	●	●
	P43	P43DO	P43DI	P4MOD3	-	-	-	●	●	●	●	●
	P44	P44DO	P44DI	P4MOD4	-	-	-	-	-	●	●	●
	P45	P45DO	P45DI	P4MOD5	-	-	-	-	-	●	●	●
	P46	P46DO	P46DI	P4MOD6	-	-	-	-	-	●	●	●
	P47	P47DO	P47DI	P4MOD7	-	-	-	-	●	●	●	●

Port Name	Pin Name	Control register / bit						Available				
		Port n data register (PnD)		Port n mode register m (PnMODm)	Port n pulse mode register (PnPMD)		Port n pulse selection register (PnPSL)	48pin product	52pin product	64pin product	80pin product	100pin product
Port 5	P50	P50DO	P50DI	P5MOD0	-	-	-	●	●	●	●	●
	P51	P51DO	P51DI	P5MOD1	-	-	-	-	●	●	●	●
	P52	P52DO	P52DI	P5MOD2	-	-	-	-	-	●	●	●
	P53	P53DO	P53DI	P5MOD3	-	-	-	-	-	●	●	●
	P54	P54DO	P54DI	P5MOD4	-	-	-	-	-	●	●	●
	P55	P55DO	P55DI	P5MOD5	-	-	-	-	-	●	●	●
	P56	P56DO	P56DI	P5MOD6	-	-	-	-	●	●	●	●
	P57	P57DO	P57DI	P5MOD7	-	-	-	-	-	●	●	●
Port 7	P70	P70DO	P70DI	P7MOD0	-	-	-	-	-	●	●	●
	P76	P76DO	P76DI	P7MOD6	-	-	-	-	-	-	●	●
	P77	P77DO	P77DI	P7MOD7	-	-	-	-	-	-	●	●
Port 8	P80	P80DO	P80DI	P8MOD0	-	-	-	-	-	-	●	●
	P81	P81DO	P81DI	P8MOD1	-	-	-	-	-	-	●	●
	P82	P82DO	P82DI	P8MOD2	-	-	-	-	-	-	●	●
	P83	P83DO	P83DI	P8MOD3	-	-	-	-	-	-	-	●
	P84	P84DO	P84DI	P8MOD4	-	-	-	-	-	-	-	●
	P85	P85DO	P85DI	P8MOD5	-	-	-	-	-	-	-	●
	P86	P86DO	P86DI	P8MOD6	-	-	-	-	-	-	-	●
	P87	P87DO	P87DI	P8MOD7	-	-	-	-	-	-	-	●
Port 9	P90	P90DO	P90DI	P9MOD0	-	-	-	-	-	-	-	●
	P91	P91DO	P91DI	P9MOD1	-	-	-	-	-	-	-	●
	P92	P92DO	P92DI	P9MOD2	-	-	-	-	-	-	-	●
	P93	P93DO	P93DI	P9MOD3	-	-	-	-	-	-	●	●
	P94	P94DO	P94DI	P9MOD4	-	-	-	-	-	-	●	●
	P95	P95DO	P95DI	P9MOD5	-	-	-	-	-	-	●	●
	P96	P96DO	P96DI	P9MOD6	-	-	-	-	-	-	●	●
	P97	P97DO	P97DI	P9MOD7	-	-	-	-	-	-	-	●
Port A	PA0	PA0DO	PA0DI	PAMOD0	-	-	-	-	-	-	-	●
	PA1	PA1DO	PA1DI	PAMOD1	-	-	-	-	-	-	-	●
	PA2	PA2DO	PA2DI	PAMOD2	-	-	-	-	-	-	-	●
	PA3	PA3DO	PA3DI	PAMOD3	-	-	-	-	-	-	●	●
	PA4	PA4DO	PA4DI	PAMOD4	-	-	-	-	-	-	●	●
	PA5	PA5DO	PA5DI	PAMOD5	-	-	-	-	-	-	-	●
	PA6	PA6DO	PA6DI	PAMOD6	-	-	-	-	-	-	-	●
	PA7	PA7DO	PA7DI	PAMOD7	-	-	-	-	-	-	-	●
Port B	PB0	PB0DO	PB0DI	PBMOD0	-	-	-	-	-	-	-	●
	PB1	PB1DO	PB1DI	PBMOD1	-	-	-	-	-	-	-	●
	PB2	PB2DO	PB2DI	PBMOD2	-	-	-	-	-	-	●	●
	PB3	PB3DO	PB3DI	PBMOD3	-	-	-	-	-	-	●	●
	PB4	PB4DO	PB4DI	PBMOD4	-	-	-	-	-	-	●	●
	PB5	PB5DO	PB5DI	PBMOD5	-	-	-	-	-	-	●	●
	PB6	PB6DO	PB6DI	PBMOD6	-	-	-	-	-	-	-	●
	PB7	PB7DO	PB7DI	PBMOD7	-	-	-	-	-	-	-	●

*1 P34,P35,P36,P37 pins have GPI/O function only. So Writing to bit 4-7 of their PnPMODm is not available.

17.2.2 Port 0 Data Register (P0D)

P0D is a SFR to read the level of the port n pin and write output data.
When the input is enabled, the input level of the port 0 pin is read from P0DI.
When the output is enabled, the value written to P0DO is output to the port 0 pin.
The data written to P0DO is readable. This bit can be set even when the output is disabled.
Enable or disable the input or output by using the port 0 mode register m.
See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of P0DO that have no corresponding pin.

Address: 0xF200(P0DI/P0D), 0xF201(P0DO)
Access: R/W
Access size: 8/16 bit
Initial value: 0x00FF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	P0D															
Byte	P0DO								P0DI							
Bit	P07DO	P06DO	P05DO	P04DO	P03DO	P02DO	-	-	P07DI	P06DI	P05DI	P04DI	P03DI	P02DI	Pn1DI	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15 to 10	P07DO to P02DO	Set the output level of port 0 pin. 0: Output "L" (Initial value) 1: Output "H"
9 to 8	-	Reserved bits
7 to1	P07DI to P00DI	Set the input level of port n pin. 0: The input level is "L" 1: The input level is "H" (Initial value)
0	-	Reserved bit

17.2.3 Port n Data Register (PnD:n＝1 to 9, A, B)

PnD is a SFR to read the level of the port n pin and write output data.
The input level of the port n pins can be read by reading PnDI in the input mode. Data written to PnDO in the output mode are output to the port n pins. The data written to PnDO is readable. The bit can be set when output is enabled or disabled. Enable or disable the input or output by using the port n mode register. See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of PnDO that have no corresponding pin.

Address: 0xF210(P1DI/P1D), 0xF211(P1DO), 0xF220(P2DI/P2D), 0xF221(P2DO),
0xF230(P3DI/P3D), 0xF231(P3DO), 0xF240(P4DI/P4D), 0xF241(P4DO),
0xF250(P5DI/P5D), 0xF251(P5DO), 0xF260(P6DI/P6D), 0xF261(P6DO),
0xF270(P7DI/P7D), 0xF271(P7DO), 0xF280(P8DI/P8D), 0xF281(P8DO)),
0xF290(P9DI/P9D), 0xF291(P9DO), 0xF2A0(PADI/PAD), 0xF2A1(PADO),
0xF2B0(PBDI/PBD), 0xF2B1(PBDO)
Access: R/W
Access size: 8/16 bit
Initial value: 0x00FF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PnD															
Byte	PnDO								PnDI							
Bit	Pn7DO	Pn6DO	Pn5DO	Pn4DO	Pn3DO	Pn2DO	Pn1DO	Pn0DO	Pn7DI	Pn6DI	Pn5DI	Pn4DI	Pn3DI	Pn2DI	Pn1DI	Pn0DI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15 to 8	Pn7DO to Pn0DO	Set the output level of port n pin. 0: Output "L" (Initial value) 1: Output "H"
7 to 0	Pn7DI to Pn0DI	Set the input level of port n pin. 0: The input level is "L" 1: The input level is "H" (Initial value)

17.2.4 Port 0 Mode Register 1 (P0MOD1)

P0MOD1 is SFR to set P01 pin.

Address: 0xF203(P0MOD1)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0005

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	P0MOD1								-							
Bit	-	-	-	-	-	P01PU	P01OE	P01IE	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 11	-	Reserved bits
10	P01PU	Enable the internal pull-up resistor of P01 pin. 0: disable (Without a pull-up resistor) 1: enable (With a pull-up resistor) (Initial value)
9	P01OE	Enable the output of P01 pin 0: Disable the output (Initial value) 1: Enable the output
8	P01IE	Enable the input of P01 pin 0: Disable the input 1: Enable the input (Initial value)
7 to 0	-	Reserved bits

[Note]

- **Because P01/TEST0 pin is initially configured as input with pull-up resistor, enter the "L" level in the default setting to the pin causes the input overcurrent flow.**

17.2.5 Port n Mode Register 01 (PnMOD01:n＝1 to 9, A, B)

PnMOD01 is a SFR to select the input/output mode, input/output status, and shared function of Pn0 pin and Pn1 pin. See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of PnMOD01 register that have no corresponding pins.

Address: 0xF212(P1MOD0/P1MOD01), 0xF213(P1MOD1),
0xF222(P2MOD0/P2MOD01), 0xF223(P2MOD1),
0xF232(P3MOD0/P3MOD01), 0xF233(P3MOD1),
0xF242(P4MOD0/P4MOD01), 0xF243(P4MOD1),
0xF252(P5MOD0/P5MOD01), 0xF253(P5MOD1),
0xF262(P6MOD0/P6MOD01), 0xF263(P6MOD1),
0xF272(P7MOD0),
0xF282(P8MOD0/P8MOD01), 0xF283(P8MOD1),
0xF292(P9MOD0/P9MOD01), 0xF293(P9MOD1),
0xF2A2(PAMOD0/PAMOD01), 0xF2A3（PAMOD1),
0xF2B2(PBMOD0/PBMOD01), 0xF2B3(PBMOD1)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PnMOD01															
Byte	PnMOD1								PnMOD0							
Bit	Pn1MD3	Pn1MD2	Pn1MD1	Pn1MD0	Pn1OD	Pn1PU	Pn1OE	Pn1IE	Pn0MD3	Pn0MD2	Pn0MD1	Pn0MD0	Pn0OD	Pn0PU	Pn0OE	Pn0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 12	Pn1MD3 to Pn1MD0	Select the shared function of Pn1 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: either 0 or 1
11	Pn1OD	Select the output type of Pn1 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly. See theML62Q2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
10	Pn1PU	Enable the internal pull-up resistor of Pn1 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
9	Pn1OE	Enable the output of Pn1 pin. 0: Disable the output (Initial value) 1: Enable the output
8	Pn1IE	Enable the input of Pn1 pin. 0: Disable the input (Initial value) 1: Enable the input

Bit No.	Bit symbol name	Description
7 to 4	Pn0MD3 to Pn0MD0	Select the shared function of Pn0 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: either 0 or 1
3	Pn0OD	Select the output type of Pn0 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly. See the ML62Q2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
2	Pn0PU	Enable the internal pull-up resistor of Pn0 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
1	Pn0OE	Enable the output of Pn0 pin. 0: Disable the output (Initial value) 1: Enable the output
0	Pn0IE	Enable the input of Pn0 pin. 0: Disable the input (Initial value) 1: Enable the input

[Note]

- **When using an external interrupt, set the PnMODm register (m=0 to 7) certainly before setting the EICON0, EIMOD0 register, and IE1 register. Setting the PnMODm register with enabling interrupt may causes an unintended interrupt.**
- **In order to prevent unintended output, set peripheral circuits and shared functions before enabling output is recommended.**

17.2.6 Port n Mode Register 23 (PnMOD23:n＝0 to 6, 8, 9, A, B)

PnMOD23 is a SFR to select the input/output mode, input/output status, and shared function of Pn2 pin and Pn3 pin. See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of PnMOD23 register that have no corresponding pins.

Address: 0xF204(P0MOD2/P0MOD23), 0xF205(P0MOD3),
0xF214(P1MOD2/P1MOD23), 0xF215(P1MOD3),
0xF224(P2MOD2/P2MOD23), 0xF225(P2MOD3),
0xF234(P3MOD2/P3MOD23), 0xF235(P3MOD3),
0xF244(P4MOD2/P4MOD23), 0xF245(P4MOD3),
0xF254(P5MOD2/P5MOD23), 0xF255(P5MOD3),
0xF264(P6MOD2/P6MOD23), 0xF265(P6MOD3),
0xF284(P8MOD2/P8MOD23), 0xF285(P8MOD3),
0xF294(P9MOD2/P9MOD23)), 0xF295(P9MOD3),
0xF2A4(PAMOD2/PAMOD23), 0xF2A5(PAMOD3),
0xF2B4(PBMOD2/PBMOD23), 0xF2B5(PBMOD3)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PnMOD23															
Byte	PnMOD3								PnMOD2							
Bit	Pn3MD3	Pn3MD2	Pn3MD1	Pn3MD0	Pn3OD	Pn3PU	Pn3OE	Pn3IE	Pn2MD3	Pn2MD2	Pn2MD1	Pn2MD0	Pn2OD	Pn2PU	Pn2OE	Pn2IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 12	Pn3MD3 to Pn3MD0	Select the shared function of Pn3 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: either 0 or 1
11	Pn3OD	Select the output type of Pn3 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly. See the 2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
10	Pn3PU	Enable the internal pull-up resistor of Pn3 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
9	Pn3OE	Enable the output of Pn3 pin. 0: Disable the output (Initial value) 1: Enable the output
8	Pn3IE	Enable the input of Pn3 pin. 0: Disable the input (Initial value) 1: Enable the input

Bit No.	Bit symbol name	Description
7 to 4	Pn2MD3 to Pn2MD0	Select the shared function of Pn2 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: 0 or 1 (don't care)
3	Pn2OD	Select the output type of Pn2 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly. See the 2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
2	Pn2PU	Select the internal pull-up resistor of Pn2 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
1	Pn2OE	Select the output of Pn2 pin. 0: Disable the output (Initial value) 1: Enable the output
0	Pn2IE	Select the input of Pn2 pin. 0: Disable the input (Initial value) 1: Enable the input

[Note]

- **When using an external interrupt, set the PnMOD23 register certainly before setting the EICON0, EIMOD0 register, and IE1 register. Setting the PnMOD23 register with enabling interrupt may causes an unintended interrupt.**
- **In order to prevent unintended output, set peripheral circuits and shared functions before enabling output is recommended.**

17.2.7 Port n Mode Register 45 (PnMOD45:n＝0 to 6, 8, 9, A, B)

PnMOD45 is a SFR to select the input/output mode, input/output status, and shared function of Pn4 pin and Pn5 pin. See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of PnMOD45 register that have no corresponding pins.

Address: 0xF206(P0MOD4/P0MOD45), 0xF207(P0MOD5),
0xF216(P1MOD4/P1MOD45), 0xF217(P1MOD5),
0xF226(P2MOD4/P2MOD45), 0xF227(P2MOD5),
0xF246(P4MOD4/P4MOD45), 0xF247(P4MOD5),
0xF256(P5MOD4/P5MOD45), 0xF257(P5MOD5),
0xF266(P6MOD4/P6MOD45), 0xF267(P6MOD5),
0xF286(P8MOD4/P8MOD45), 0xF287(P8MOD5),
0xF296(P9MOD4/P9MOD45), 0xF297(P9MOD5),
0xF2A6(PAMOD4/PAMOD45), 0xF2A7(PAMOD5),
0xF2B6(PBMOD4/PBMOD45), 0xF2B7(PBMOD5)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PnMOD45															
Byte	PnMOD5								PnMOD4							
Bit	Pn5MD3	Pn5MD2	Pn5MD1	Pn5MD0	Pn5OD	Pn5PU	Pn5OE	Pn5IE	Pn4MD3	Pn4MD2	Pn4MD1	Pn4MD0	Pn4OD	Pn4PU	Pn4OE	Pn4IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 12	Pn5MD3 to Pn5MD0	Select the shared function of Pn5 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: ether 0 or 1 * P35 pin does not have shared function. P35MD3-0 are not writable. The reading value is "0".
11	Pn5OD	Select the output type of Pn5 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly. See the 2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
10	Pn5PU	Enable the internal pull-up resistor of Pn5 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
9	Pn5OE	Enable the output of Pn5 pin. 0: Disable the output (Initial value) 1: Enable the output
8	Pn5IE	Enable the input of Pn5 pin. 0: Disable the input (Initial value) 1: Enable the input

Bit No.	Bit symbol name	Description
7 to 4	Pn4MD3 to Pn4MD0	Select the shared function of Pn4 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: ether 0 or 1 * P34 pin does not have shared function. P35MD3 to 0 are not writable. The reading value is "0".
3	Pn4OD	Select the output type of Pn4 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly See the 2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
2	Pn4PU	Enable the internal pull-up resistor of Pn4 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
1	Pn4OE	Enable the output of Pn4 pin. 0: Disable the output (Initial value) 1: Enable the output
0	Pn4IE	Enable the input of Pn4 pin. 0: Disable the input (Initial value) 1: Enable the input

[Note]

- **When using an external interrupt, set the PnMOD45 register certainly before setting the EICON0, EIMOD0 register, and IE1 register. Setting the PnMOD45 register with enabling interrupt may causes an unintended interrupt.**
- **In order to prevent unintended output, set peripheral circuits and shared functions before enabling output is recommended.**

17.2.8 Port n Mode Register 67 (PnMOD67:n＝0 to 9, A, B)

PnMOD67 is a SFR to select the input/output mode, input/output status, and shared function of Pn6 pin and Pn7 pin. See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of PnMOD67 register that have no corresponding pins.

Address: 0xF208(P0MOD6/P0MOD67), 0xF209(P0MOD7),
0xF218(P1MOD6/P1MOD67), 0xF219(P1MOD7),
0xF228(P2MOD6/P2MOD67), 0xF229(P2MOD7),
0xF248(P4MOD6/P4MOD67), 0xF249(P4MOD7),
0xF258(P5MOD6/P5MOD67), 0xF259(P5MOD7),
0xF268(P6MOD6/P6MOD67), 0xF269(P6MOD7),
0xF278(P7MOD6/P7MOD67), 0xF279(P7MOD7),
0xF288(P8MOD6/P8MOD67), 0xF289(P8MOD7),
0xF298(P9MOD6/P9MOD67), 0xF299(P9MOD7),
0xF2A8(PAMOD6/PAMOD67), 0xF2A9(PAMOD7),
0xF2B8(PBMOD6/PBMOD67), 0xF2B9(PBMOD7)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PnMOD67															
Byte	PnMOD7								PnMOD6							
Bit	Pn7MD3	Pn7MD2	Pn7MD1	Pn7MD0	Pn7OD	Pn7PU	Pn7OE	Pn7IE	Pn6MD3	Pn6MD2	Pn6MD1	Pn6MD0	Pn6OD	Pn6PU	Pn6OE	Pn6IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 12	Pn7MD3 to Pn7MD0	Select the shared function of Pn7 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: either 0 or 1 * P37 pin does not have shared function. P37MD3-0 are not writable. The reading value is "0".
11	Pn7OD	Select the output type of Pn7 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly See the 2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
10	Pn7PU	Enable the internal pull-up resistor of Pn7 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
9	Pn7OE	Enable the output of Pn7 pin. 0: Disable the output (Initial value) 1: Enable the output
8	Pn7IE	Enable the input of Pn7 pin. 0: Disable the input (Initial value) 1: Enable the input

Bit No.	Bit symbol name	Description
7 to 4	Pn6MD3 to Pn6MD0	Select the shared function of Pn6 pin. For the details of the shared function, see Table 1-3 "ML62Q2700 Group Pin List" 0000: Primary function (Initial value) 0001: 2nd function 0010: 3rd function 0011: 4th function 0100: 5th function 0101: 6th function 0110: 7th function 0111: 8th function 1XXX: Do not use (Primary function) X: either 0 or 1 * P36 pin does not have shared function. P36MD3-0 are not writable. The reading value is "0".
3	Pn6OD	These bits are used choose the output type of Pn6 pin. By selecting N-channel open-drain output improves output current capability and allows the LED to be driven directly See the 2700 data sheet for details about the current drive ability. 0: CMOS output (Initial value) 1: N-channel open drain output
2	Pn6PU	Enable the internal pull-up resistor of Pn6 pin. 0: Without a pull-up resistor (Initial value) 1: With a pull-up resistor
1	Pn6OE	Enable the output of Pn6 pin. 0: Disable the output (Initial value) 1: Enable the output
0	Pn6IE	Enable the input of Pn6 pin. 0: Disable the input (Initial value) 1: Enable the input

[Note]

- **When using an external interrupt, set the PnMOD67 register certainly before setting the EICON0, EIMOD0 register, and IE1 register. Setting the PnMOD67 register with enabling interrupt may causes an unintended interrupt.**
- **In order to prevent unintended output, set peripheral circuits and shared functions before enabling output is recommended.**
-

17.2.9 Port n Pulse Mode Register (PnPMD:n＝0 to 3)

PnPMD is a SFR to use when outputting a carrier frequency (pulse output) to the port n.
See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of PnPMD register that have no corresponding pin.

Address: 0xF20A(P0PMDL/P0PMD), 0xF20B(P0PMDH), 0xF21A(P1PMDL/P1PMD), 0xF21B(P1PMDH), 0xF22A(P2PMDL/P2PMD), 0xF22B(P2PMDH), 0xF23A(P3PMDL/P3PMD), 0xF23B(P3PMDH)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PnPMD															
Byte	PnPMDH								PnPMDL							
Bit	Pn7PLVL	Pn6PLVL	Pn5PLVL	Pn4PLVL	Pn3PLVL	Pn2PLVL	Pn1PLVL	Pn0PLVL	Pn7PEN	Pn6PEN	Pn5PEN	Pn4PEN	Pn3PEN	Pn2PEN	Pn1PEN	Pn0PEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 8	Pn7PLVL to Pn0PLVL	Selects whether to output the carrier frequency to the "H" level output from the Pn7~Pn0 pins or to the "L" level output from the Pn7~Pn0 pins. 0: Output the carrier frequency to the pins when the output level is "H" (initial value) 1: Output the carrier frequency to the pins when the output level is "L"
7 to 0	Pn7PEN to Pn0PEN	Enable or disable the pulse output of Pn7 to Pn0. These bits are valid when Pn7 to Pn0 pins are configured as output is enabled (Pn7OE to Pn0OE are "0"). 0: Disable pulse output (initial value) 1: Enable pulse output

17.2.10 Port n Pulse Selection Register (PnPSL:n＝0 to 3)

PnPSL is a SFR to select the timer for generating the carrier frequency to the port n.
See Table 17-2 "List of Registers / Bits" to check available pins and bits. Write "0" to the bits of PnPSL register that have no corresponding pin.

Address: 0xF20C（P0PSLL/P0PSL）, 0xF20D（P0PSLH）, 0xF21C（P1PSLL/P1PSL）, 0xF21D（P1PSLH）, 0xF22C（P2PSLL/P2PSL）, 0xF22D（P2PSLH）, 0xF23C（P3PSLL/P3PSL）, 0xF23D（P3PSLH）
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PnPSL															
Byte	PnPSLH								PnPSLL							
Bit	-	-	-	-	-	-	-	-	Pn7PSL	Pn6PSL	Pn5PSL	Pn4PSL	Pn3PSL	Pn2PSL	Pn1PSL	Pn0PSL
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 8	-	Reserved bits
7 to 0	PnmPSL	Select the timer for generating the carrier frequency to the Pnm. These bits setting are valid only when the Pnm pin is set to output enabled (PnmOE is set to "0"). n : Port numbers 0 to 9, A, B m: Bit number 0 to 7 0: 16-bit timer 0 output (TMO0) (Initial value) 1: Functional timer 0 output (FTO0)

17.2.11 PORTXT Data Input Register (PXTDI)

PXTDI is a SFR to use for reading the level of XT0/XT1 pin.
The level of XT0/PI0 and XT1/PI1 is readable in the input mode. Set PXT0IE bit and PXT1IE bit of PXTMOD01 register for switching the port to the input mode. The port is unavailable to use when connecting the crystal resonator.

Address: 0xF2F0(PXTDI)
Access: R
Access size: 8 bit
Initial value: 0x03

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								PXTDI							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PXT1DI	PXT0DI
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit No.	Bit symbol name	Description
7 to 2	-	Reserved bits
1	PXT1DI	Reading the level of XT1/PI1. 0: The input level of XT1/PI1 pin is "L" 1: The input level of XT1/PI1 pin is "H"
0	PXT0DI	Reading the level of XT0/PI0. 0: The input level of XT0/PI0 pin is "L" 1: The input level of XT0/PI0 pin is "H"

[Note]

- **PI0 and PI1 are unavailable to use as input ports when using the crystal resonator for the oscillation clock. Also, PI1 is unavailable to use as an input port when using the XT1 for the external clock input. See Chapter 6 "Clock Generation Circuit" for more details on how to use the crystal oscillation or external clock input.**

17.2.12 PORTXT Mode Register 01 (PXTMOD01)

PXTMOD01 is a SFR to select the input mode of the XT0/PI0 pin and XT1/PI1 pin.
The port is unavailable to use when connecting the crystal resonator.

Address: 0xF2F2(PXTMOD0/PXTMOD01), 0xF2F3(PXTMOD1)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PXTMOD01															
Byte	PXTMOD1								PXTMOD0							
Bit	-	-	-	-	-	-	-	PXT1IE	-	-	-	-	-	-	-	PXT0IE
R/W	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 9	-	Reserved bits
8	PXT1IE	Select the input mode of the XT1/PI1 pin. 0: High impedance (Initial value) 1: Input mode
7 to 1	-	Reserved bits
0	PXT0IE	Select the input mode of the XT0/PI0 pin. 0: High impedance (Initial value) 1: Input mode

17.3 Description of Operation

The following describes of port functions, where "n" is port number 0 to 9, A, B, and "m" is bit number 0 to 7.

17.3.1 Input

Each pin of port n except for the P01 sets the PnmIE bit of the PnMODm register to enter the state where input is enabled.
In the state with input enabled, the pin level can be read using the PnDI. In addition, pull-up can be enabled by setting the PnmPU bit of the PnMODm register.
At a system reset, input disabled and no pull-up are selected as the initial status of pins except for the P01. As one of the P01 port, Input enable and pull-up are selected.

17.3.2 Output

Each pin of port n set to output enable state by setting PnmOD bit of PnMODm register to select either CMOS output or N-channel open drain output as an output type and sets PnmOE bit of PnMODm register.
In the state with output enabled, "L" or "H" level is output to each pin of the general-purpose port according to the value set in the PnDO.
At system reset, output disabled and CMOS output are selected as the initial status.
n: Port number 0 to 9, A, B
m: Bit number 0 to 7

17.3.3 Primary Functions Other than Input/Output Function

External input (EXI0 to EXI11), analog input for SA-ADC or crystal/external clock input can be used as the primary function other than the input/output function.
When using EXI0 to EXI7 as external interrupt input and the clock inputs of the 16-bit timer or trigger/clock input of the functional timer, set the PnMODm register of the applicable port to input enabled (PnmIE bit="1").
When using as analog input for SA-ADC; AIN0 to AIN15 and VREF, set the PnMODm register of the applicable port to input disabled (PnmIE bit="0" and PnmOE bit="0").
When using as crystal/external clock input, set by the FLMOD register; refer to Chapter 6. After the setting, PORTEXT mode register setting is invalid
See Chapter 18 "External Interrupt Control" for external interrupts, Chapter 8 "16-Bit Timer" for clock input of the 16-bit timer, and Chapter 9 "Functional Timer" for external trigger/clock input of the functional timer.

17.3.4 Shared Function

Each pin of port n is usable 2^{nd} to 8^{th} functions as the shared function.
Set PnmMD3 to PnmMD0 bits of the PnMODm register to select each of the 2^{nd} to 8^{th} functions.

17.3.5 Carrier Frequency Output

17.3.5.1 Carrier Frequency Output Operation

A carrier frequency signal can be output from port n by setting PnPMD Register. See Table 17-2 "List of Registers/Bits" for pins supporting the carrier frequency output function. For the carrier frequency output, either of 16-bit timer 0 output (TMO0) or functional timer 0 output (FTO0) can be used through setting the PnPSL register.
See Chapter 8 "16-Bit Timer" for details of 16-bit timer 0, and Chapter 9 "Functional Timer" for functional timer 0.
Figures 17-3 and 17-4 show an example of use of the carrier frequency output function.

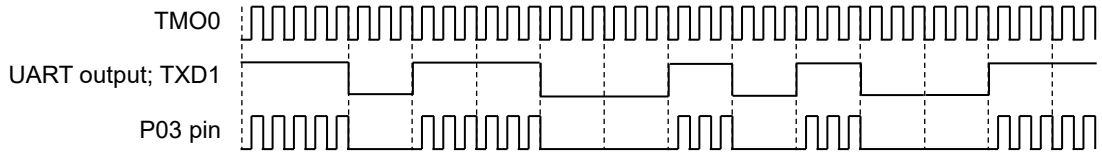


Figure 17-3 Example of Carrier Frequency Output When P03 Pin is Assigned to UART Output Pin
(P03PEN bit ="1", P03PLVL bit= "0" of P0PMD register)

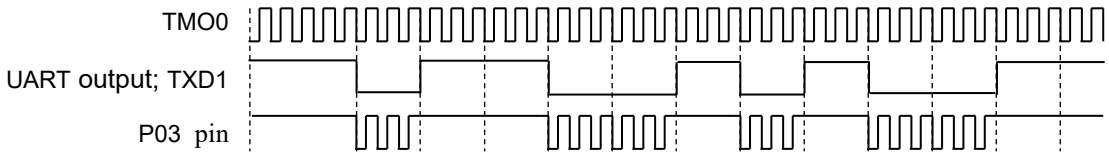


Figure 17-4 Example of Carrier Frequency Output When P03 Pin is Assigned to UART Output Pin
(P03PEN bit ="1", P03PLVL bit= "1" of P0PMD register)

17.3.5.2 Carrier Frequency Output Function Setting Procedure

Figure 17-5 shows an example of the carrier frequency output function setting procedure (with P03 pin used, TXD1 shared function, functional timer 0 output (FTO0) used as a timer, carrier frequency output at "L" level).

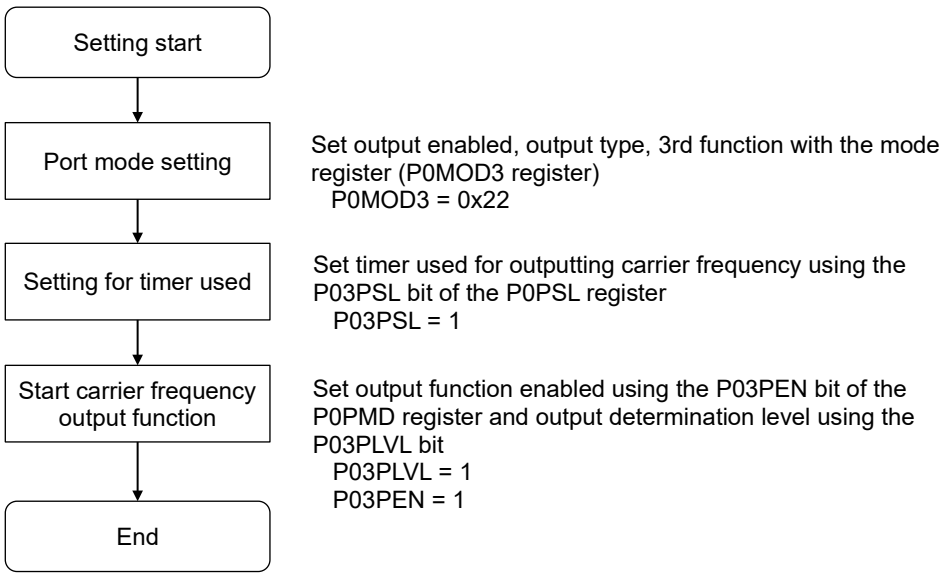


Figure 17-5 Example of Carrier Frequency Output Function Setting Procedure

17.3.6 Port Output Level Test

The level specified in the PnDO is readable from the PnDI by setting the PnmOE bit of the PnMODm register to "1" and the PnmIE bit to "1". Use of this function allows confirmation that the level set in the PnDO is being normally output to the port.

17.3.7 Port Setting Example

Figure 17-6 shows an example for setting port registers to output 0x55 to a port 2. It is also available to set output level before outputting.

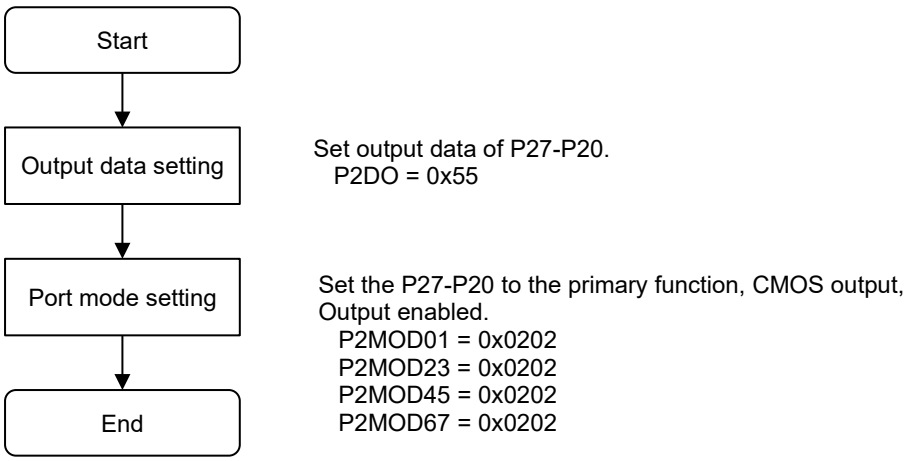


Figure 17-6 Setting example to output data to port 2

17.3.8 Notes for using the P00/TEST0 pin

P01/TEST0 pin is used for the general port, the on-chip debug function or ISP function.
When using the on-chip debug function or ISP function, P00/TEST0 is unavailable to use as the general purpose port.
When using the general port, P00/TEST0 is unavailable to use for the on-chip debug function or ISP function.

Chapter 18 External Interrupt Function

18. External Interrupt Function

18.1 General Description

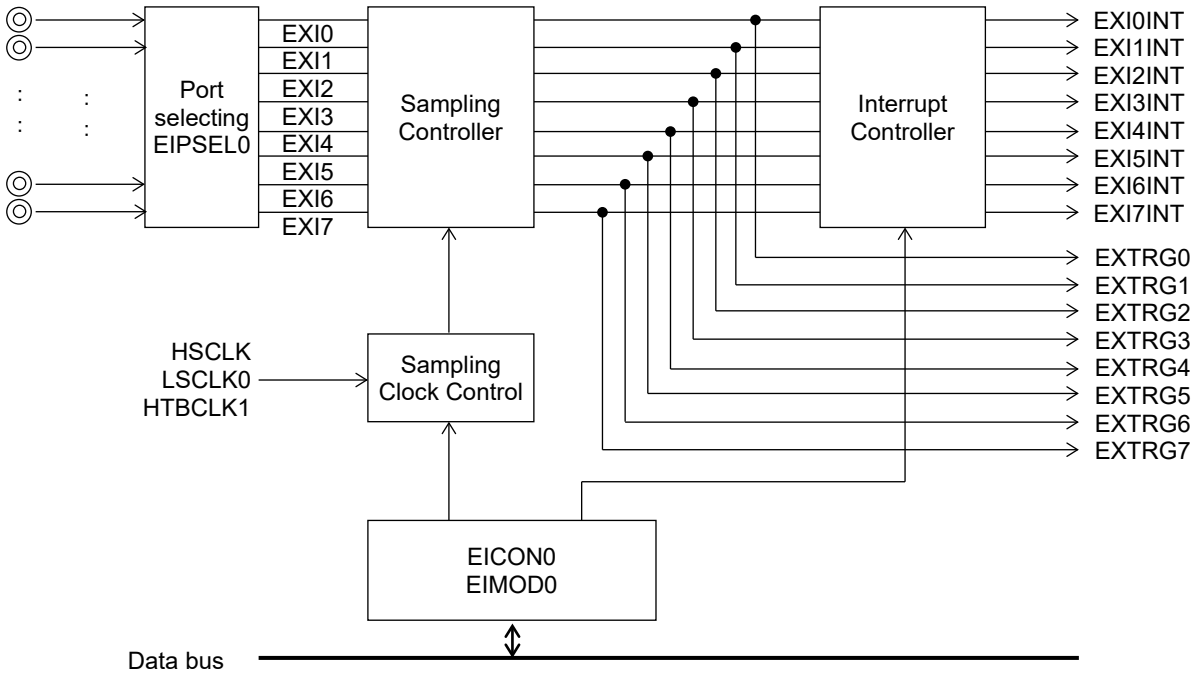
An external interrupt can occur at the timing of the signal entering the general-purpose port changes.
The interrupt channel has each dedicated interrupt vector. See Chapter 5 "Interrupt" for details of the interrupt vector.

18.1.1 Features

- Maskable 8 interrupts (1 of 8 interrupts shared with 4 external interrupts: extended external interrupts)
- Selectable interrupt modes: interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode or both-edge interrupt mode
- Selectable "with sampling" or "without sampling" for the input signal
- Selectable sampling clock: LSCLK0, HSCLK or HTBCLK1

18.1.2 Configuration

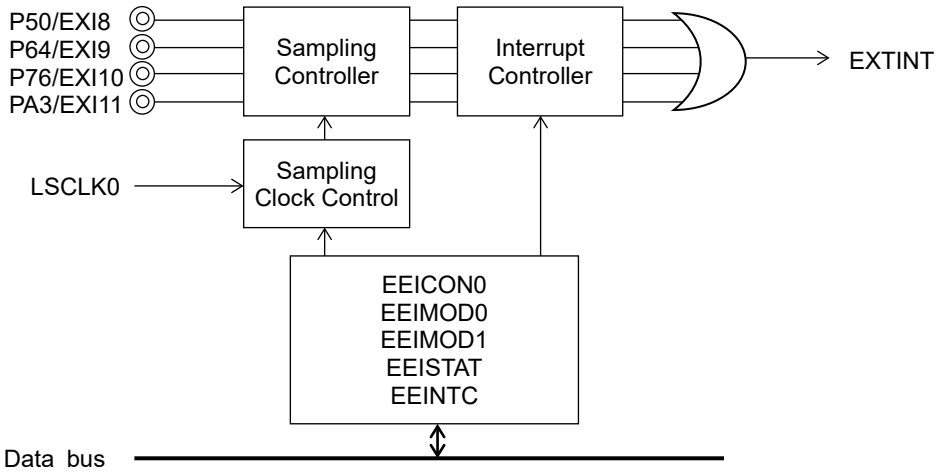
Figure 18-1 shows the configuration of the external interrupt function (EXI0 to EXI7)



EICON0 : External interrupt control register 0
EIMOD0: External interrupt mode register 0
EIPSEL0: External interrupt port select register 0

Figure 18-1 Configuration of External Interrupt Function

Figure 18-2 shows the configuration of the external interrupt function (EXI8 to EXI11)



EEICON0 : Extended External interrupt control register 0
EEIMOD0 : Extended External interrupt mode register 0
EEISTAT : Extended External interrupt status register

Figure 18-2 Configuration of Extended External Interrupt Function

18.1.3 List of Pins

The external interrupt is assigned to the primary function of the general port.

Pin name	I/O	Function
EXI0	I	External Interrupt Input 0
EXI1	I	External Interrupt Input 1
EXI2	I	External Interrupt Input 2
EXI3	I	External Interrupt Input 3
EXI4	I	External Interrupt Input 4
EXI5	I	External Interrupt Input 5
EXI6	I	External Interrupt Input 6
EXI7	I	External Interrupt Input 7
EXI8	I	External Interrupt Input 8 (Extended external interrupt)
EXI9	I	External Interrupt Input 9 (Extended external interrupt)
EXI10	I	External Interrupt Input 10 (Extended external interrupt)
EXI11	I	External Interrupt Input 11 (Extended external interrupt)

Table 18-1 shows the list of the general ports used for the external interrupt and the register settings of the ports.

Table 18-1 Ports used for the external interrupt and the register settings

Pin name	Shared port		Setting register	Setting value	ML62Q2700group				
					48pin product	52pin product	64pin product	80pin product	100pin product
EXI0	P02	Primary function	P0MOD2	0000_0X01*1	●	●	●	●	●
	P41		P4MOD1	0000_0X01*1	-	●	●	●	●
	P54		P5MOD4	0000_0X01*1	-	-	●	●	●
	P70		P7MOD0	0000_0X01*1	-	-	●	●	●
EXI1	P03		P0MOD3	0000_0X01*1	●	●	●	●	●
	P31		P3MOD1	0000_0001*1	●	●	●	●	●
	P55		P5MOD5	0000_0X01*1	-	-	●	●	●
	P11		P1MOD1	0000_0X01*1	●	●	●	●	●
EXI2	P04		P0MOD4	0000_0X01*1	●	●	●	●	●
	P33		P3MOD3	0000_0X01*1	●	●	●	●	●
	P14		P1MOD4	0000_0X01*1	●	●	●	●	●
	P44		P4MOD4	0000_0X01*1	-	-	●	●	●
EXI3	P17		P1MOD7	0000_0X01*1	●	●	●	●	●
	P61		P6MOD1	0000_0X01*1	●	●	●	●	●
	P51		P5MOD1	0000_0X01*1	-	●	●	●	●
	P45		P4MOD5	0000_0X01*1	-	-	●	●	●
EXI4	P21		P2MOD1	0000_0X01*1	●	●	●	●	●
	P63		P6MOD3	0000_0X01*1	●	●	●	●	●
	P52		P5MOD2	0000_0X01*1	-	-	●	●	●
	P46		P4MOD6	0000_0X01*1	-	-	●	●	●
EXI5	P23		P2MOD3	0000_0X01*1	●	●	●	●	●
	P65		P6MOD5	0000_0X01*1	●	●	●	●	●
	P53		P5MOD3	0000_0X01*1	-	-	●	●	●
	P47		P4MOD7	0000_0X01*1	-	●	●	●	●

Pin name	Shared port		Setting register	Setting value	ML62Q2700group				
					48pin product	52pin product	64pin product	80pin product	100pin product
EXI6	P26	Primary function	P2MOD6	0000_0X01*1	●	●	●	●	●
	P67		P6MOD7	0000_0X01*1	-	-	●	●	●
	P12		P1MOD2	0000_0X01*1	●	●	●	●	●
	P80		P8MOD0	0000_0X01*1	-	-	-	●	●
EXI7	P27		P2MOD7	0000_0X01*1	●	●	●	●	●
	P43		P4MOD3	0000_0X01*1	●	●	●	●	●
	P13		P1MOD3	0000_0X01*1	●	●	●	●	●
	P81		P8MOD1	0000_0X01*1	-	-	-	●	●
EXI8	P50		P5MOD0	0000_0X01*1	●	●	●	●	●
EXI9	P64		P6MOD4	0000_0X01*1	●	●	●	●	●
EXI10	P76		P7MOD6	0000_0X01*1	-	-	-	●	●
EXI11	PA3		PAMOD3	0000_0X01*1	-	-	-	●	●

●: available, -:not available
*1 : "X" determines the condition of the port input

X	Condition of the port input
0	Input (without an internal pull-up resistor)
1	Input (with an internal pull-up resistor)

18.2 Description of Registers

18.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF044	External interrupt control registers 0	EICON0L	EICON0	R/W	8/16	0x00
0xF045		EICON0H		R/W	8	0x00
0xF046	Reserved registers	-	-	-	-	-
0xF047						
0xF048	External interrupt mode registers 0	EIMOD0L	EIMOD0	R/W	8/16	0x00
0xF049		EIMOD0H		R/W	8	0x00
0xF04A	Reserved registers	-	-	-	-	-
0xF04B						
0xF04C	External interrupt port selection registers 0	EIPSEL0L	EIPSEL0	R/W	8/16	0x00
0xF04D		EIPSEL0H		R/W	8	0x00
0xF0E4	Extended External interrupt control registers 0	EEICON0L	EEICON0	R/W	8/16	0x00
0xF0E5		EEICON0H		R/W	8	0x00
0xF0E6	Reserved registers	-	-	-	-	-
0xF0E7						
0xF0E8	Extended External interrupt mode registers 0	EEIMOD0L	EEIMOD0	R/W	8/16	0x00
0xF0E9		EEIMOD0H		R	8	0x00
0xF0EA	Extended External interrupt mode registers 1	EEIMOD1L	EEIMOD1	R/W	8/16	0x00
0xF0EB		EEIMOD1H		R	8	0x00
0xF0EC	Extended External interrupt status registers	EEISTATL	EEISTAT	R	8/16	0x00
0xF0ED		EEISTATH		R	8	0x00
0xF0EE	Extended External interrupt clear registers	EEINTCL	EEINTC	W	8/16	0x00
0xF0EF		EEINTCH		W	8	0x00

18.2.2 External Interrupt Control Register 0 (EICON0)

EICON0 is a SFR to select the detection edge of the external interrupt input (EXI0 to EXI7).
After the edge detection, an external interrupt (EXI0INT to EXI7INT) occurs .

Address : 0xF044(EICON0L/EICON0), 0xF045(EICON0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EICON0															
Byte	EICON0H								EICON0L							
Bit	PI7E1	PI6E1	PI5E1	PI4E1	PI3E1	PI2E1	PI1E1	PI0E1	PI7E0	PI6E0	PI5E0	PI4E0	PI3E0	PI2E0	PI1E0	PI0E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 8	PI7E1 to PI0E1	Select the detection edge of the external interrupt (EXI0 to EXI7). The detection edge is set by a combination of PInE1 and PInE0 bits (n=0 to 7). 00 : Interrupt disabled (Initial value) 01 : Falling-edge interrupt 10 : Rising-edge interrupt 11 : Both-edge interrupt The relation of the bit number and the target external interrupt: Bit 15, 7 (PI7E1, PI7E0) : EXI7INT Interrupt Bit 14, 6 (PI6E1, PI6E0) : EXI6INT Interrupt Bit 13, 5 (PI5E1, PI5E0) : EXI5INT Interrupt Bit 12, 4 (PI4E1, PI4E0) : EXI4INT Interrupt Bit 11, 3 (PI3E1, PI3E0) : EXI3INT Interrupt Bit 10, 2 (PI2E1, PI2E0) : EXI2INT Interrupt Bit 9, 1 (PI1E1, PI1E0) : EXI1INT Interrupt Bit 8, 0 (PI0E1, PI0E0) : EXI0INT Interrupt
7 to 0	PI7E0 to PI0E0	

18.2.3 External Interrupt Mode Register 0 (EIMOD0)

EIMOD0 is a SFR to select the sampling clock and with/without sampling for the external interrupt (EXI0 to EXI7). The sampling clock selected in EIMOD0 register is shared by EXI0 to EXI7.

Address : 0xF048(EIMOD0L/EIMOD0), 0xF049(EIMOD0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EIMOD0															
Byte	EIMOD0H								EIMOD0L							
Bit	-	-	PG0DIV1	PG0DIV0	PG0CS1	PG0CS0	-	-	PI7SM	PI6SM	PI5SM	PI4SM	PI3SM	PI2SM	PI1SM	PI0SM
R/W	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 14	-	Reserved bits
13 to 12	PG0DIV1 to PG0DIV0	Select frequency dividing ratio for the sampling clock in the EXI0 to EXI7. 00: No dividing (Initial value) 01: Divide by 2 of the sampling clock source 10: Divide by 4 of the sampling clock source 11: Divide by 8 of the sampling clock source
11 to 10	PG0CS1 to PG0CS0	Select the sampling clock source of EXI0 to EXI7. 00: LSCLK0 (Initial value) 01: HSCLK 10: HTBCLK1 11: rsvd
9, 8	-	Reserved bits
7 to 0	PI7SM to PI0SM	Select whether the input signals of EXI0 to EXI7 are detected with the sampling clock. 0: Detected without the sampling clock (Initial value) 1: Detected with the sampling clock except in STOP/STOP-D mode The relation of the bit number and the target external interrupt: Bit 7 (PI7SM) : EXI7INT Interrupt Bit 6 (PI6SM) : EXI6INT Interrupt Bit 5 (PI5SM) : EXI5INT Interrupt Bit 4 (PI4SM) : EXI4INT Interrupt Bit 3 (PI3SM) : EXI3INT Interrupt Bit 2 (PI2SM) : EXI2INT Interrupt Bit 1 (PI1SM) : EXI1INT Interrupt Bit 0 (PI0SM) : EXI0INT Interrupt

[Note]

- **When a high-speed clock is selected as the sampling clock, no sampling is required except for the HSCLK supply state (ENOSC=1 and oscillation stabilization is completed). Set it to "LSCLK0" if necessary.**
- **During STOP/STOP-D mode, it works without sampling.**

18.2.4 External Interrupt Port Selection Register 0 (EIPSEL0)

EIPSEL0 is a SFR used to select a port assigned to EXI0 to EXI7.

Address : 0xF04C(EIPSEL0L/EIPSEL0), 0xF04D(EIPSEL0H),
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EIPSEL0															
Byte	EIPSEL0H								EIPSEL0L							
Bit	EI7PS1	EI7PS0	EI6PS1	EI6PS0	EI5PS1	EI5PS0	EI4PS1	EI4PS0	EI3PS1	EI3PS0	EI2PS1	EI2PS0	EI1PS1	EI1PS0	EI0PS1	EI0PS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15-0	EInPS1, EInPS0	Select a port assigned to EXIn. See Table 18-2 for detail. 00: Selection 0 (Initial value) 01: Selection 1 10: Selection 2 11: Selection 3

Table 18-2 assignment port to each EXI

EInPS1, EInPS0	EXI7	EXI6	EXI5	EXI4	EXI3	EXI2	EXI1	EXI0
00	P27	P26	P23	P21	P17	P04	P03	P02
01	P43	P67	P65	P63	P61	P33	P31	P41
10	P13	P12	P53	P52	P51	P14	P55	P54
11	P81*1	P80*1	P47	P46	P45	P44	P11	P70

*1: 100/80 pin product only. Unimplemented products are the same as setting 0.

18.2.5 Extended External Interrupt Control Register 0 (EEICON0)

EEICON0 is a SFR to select the detection edge of the external interrupt input (EXI8 to EXI11).

Address : 0xF0E4(EEICON0L/EEICON0), 0xF0E5(EEICON0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EICON0															
Byte	EICON0H								EICON0L							
Bit	-	-	-	-	EPI3E1	EPI2E1	EPI1E1	EPI0E1	-	-	-	-	EPI3E0	EPI2E0	EPI1E0	EPI0E0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 12 7 to 4	-	Reserved bits
11 to 8	EPI3E1 to EPI0E1	Select the detection edge of the external interrupt (EX8 to EX11). The detection edge is set by a combination of EPInE1 and EPInE0 bits (n=0 to 3). 00 : Interrupt disabled (Initial value) 01 : Falling-edge interrupt 10 : Rising-edge interrupt 11 : Both-edge interrupt The relation of the bit number and the target external interrupt: Bit 11, 3 (PI3E1, PI3E0) : EXI11INT Interrupt Bit 10, 2 (PI2E1, PI2E0) : EXI10INT Interrupt Bit 9, 1 (PI1E1, PI1E0) : EXI9INT Interrupt Bit 8, 0 (PI0E1, PI0E0) : EXI8INT Interrupt
3 to 0	EPI3E0 to EPI0E0	

[Note]

- **When writing to IRQ01/IRQ23/IRQ45/IRQ67 from the CPU while extended external interrupt is enabled, write "1" to EEIR bit of EEINTC register and request the interrupt again.**

18.2.6 Extended External Interrupt Mode Register 0 (EEIMOD0)

EEIMOD0 is a SFR to select the sampling clock and with/without sampling for the external interrupt EXI8 to EXI11.

Address : 0xF0E8(EEIMOD0L/EEIMOD0), 0xF0E9(EEIMOD0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EEIMOD0															
Byte	EEIMOD0H								EEIMOD0L							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	PI3SM	PI2SM	PI1SM	PI0SM
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 4	-	Reserved bits
3 to 0	EPI3SM to EPI0SM	Select whether the input signals of EXI8 to EXI11 are detected with the sampling clock. Selecting without sampling is prohibited. Always set "1". 0: Detected without the sampling clock (Initial value) 1: Detected with the sampling clock The relation of the bit number and the target external interrupt(occur after edge detection): Bit 3 (EPI3SM) : EXI11INT Interrupt Bit 2 (EPI2SM) : EXI10INT Interrupt Bit 1 (EPI1SM) : EXI9INT Interrupt Bit 0 (EPI0SM) : EXI8INT Interrupt

[Note]

- **In STOP and STOP-D modes, the sampling clock stops, so no sampling is performed regardless of the value of the EPI3SM to EPI0SM bits in the EEIMOD0 register. There is a section [*1] where the interrupt is disabled.**

  [*1] : When switching to the corresponding mode: maximum 30µs
  When returning from the corresponding mode: Period until the sampling clock (low-speed clock) supply starts.
  Since the period until the clock starts supplying varies depending on the setting, refer to "Table 4-5 Startup time from stan-by mode" in "Chapter 4 Power Management".

18.2.7 Extended External Interrupt Mode Register 1 (EEIMOD1)

EEIMOD1 is a SFR to select the sampling clock for EXI8 to EXI11.
The sampling clock selected in the EEIMOD1 register is shared by EXI8 to EXI11.

Address : 0xF0EA(EEIMOD1L/EEIMOD1), 0xF0EB(EEIMOD1H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EEIMOD1															
Byte	EEIMOD1H								EEIMOD1L							
Bit	-	-	-	-	-	-	-	-	-	EPG0DIV2	EPG0DIV1	EPG0DIV0	-	rsvd	-	-
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 7	-	Reserved bits
6 to 4	EPG0DIV2 to EPG0DIV0	Selects the sampling clock divider ratio of EXI8 to EXI11. 000: No divide (default) 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 101: Divide by 32 110: Divide by 64 111: No divider
3	-	Reserved bits
2	rsvd	Reserved bits. Write 0.
1, 0	-	Reserved bits

18.2.8 Extended External Interrupt Status Register (EESTAT)

EESTAT is a SFR to indicates the interrupt status of an extended external interrupt.
EEISTAT register is a read-only register.
EEI3S to EEI0S bits are initialized to "0" by writing "1" to the same bit of EEINTC register in addition to the reset function.

Address : 0xF0EC(EEISTATL/EEISTAT), 0xF0ED(EEISTATH)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EEISTAT															
Byte	EEISTATH								EEISTATL							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	EEI3S	EEI2S	EEI1S	EEI0S
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 4	-	Reserved bits
3 to 0	EEI3S to EEI0S	Indicates the interrupt status of the extended external interrupt. 0: No interrupt occurs (initial value) 1: Interrupt occurs The relation of the bit number and the target external interrupt (occur after edge detection): Bit 3 (EEI3S): EXI11INT interrupt Bit 2 (EEI2S): EXI10INT interrupt Bit 1 (EEI1S): EXI9INT interrupt Bit 0 (EEI0S): EXI8INT interrupt

[Note]

When using the on-chip debug function, do not uncheck "External Interrupt" in "Peripheral circuits to continue operation during break". If this check is cleared, this status may be cleared.

18.2.9 Extended External Interrupt Clear Register (EEINTC)

EESINTC is a SFR to clears the extended external interrupt status.
Writing "1" to EEI3C to EEI0C bits clears the interrupt status of the same bit in EEISTAT register.
Reads always 0x0000.

Address : 0xF0EE(EEINTCL/EEINTC), 0xF0EF(EEINTCH)
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	EEINTC															
Byte	EEINTCH								EEINTCL							
Bit	EEIR	-	-	-	-	-	-	-	-	-	-	-	EEI3C	EEI2C	EEI1C	EEI0C
R/W	W	R	R	R	R	R	R	R	R	R	R	R	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	EEIR	Request external interrupts Write "1" before the interrupt routine completes and after writing to the IRQ01/IRQ23/IRQ45/IRQ67 registers. Write 0 : invalid Write 1 : If there is a unprocessed interrupt factor, issue the interrupt request again
14 to 4	-	Reserved bits
3 to 0	EEI3C to EEI0C	Clear the status of the extended external interrupt. Write 0 : invalid Write 1 : Clear interrupt status The relation of the bit number and the target external interrupt (occur after edge detection): Bit 3 (EEI3C): EXI11INT interrupt Bit 2 (EEI2C): EXI10INT interrupt Bit 1 (EEI1C): EXI9INT interrupt Bit 0 (EEI0C): EXI8INT interrupt

[Note]

- **Do not set the EEIR bit at the same time as the EEI3C~EEI0C bit.**
- **When an extended external interrupt occurs and the CPU writes to the interrupt request register (IRQ01, IRQ23, IRQ45, IRQ67), the extended external interrupt status register (EEISTAT) is set, but the extended external interrupt interrupt request bit (QEXTX=Bit 8) of the IRQ23 register may not be set and the CPU may not be notified of an interrupt.**
- **If an extended external interrupt is enabled (when the extended external interrupt control register 0 (EEICON0) is set to something other than "Interrupt Prohibition"), set the EEIR of EEINTC to 1 and rerequest the interrupt.**

18.3 Description of Operation

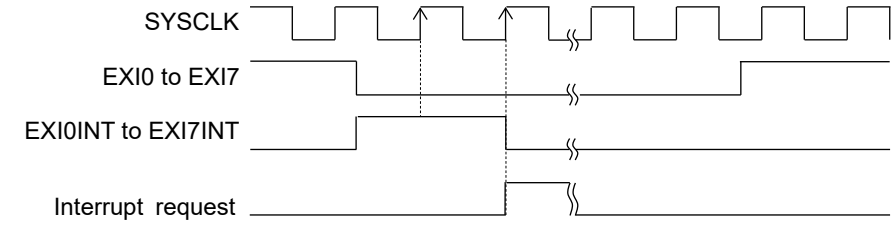
18.3.1 Interrupt Request Timing

Figure 18-3 shows the interrupt generation timing without sampling (when the rising-edge/falling-edge/both-edge interrupt mode is chosen). Figure 18-4 shows the interrupt generation timing with sampling (when the rising-edge interrupt mode is selected).
Table 18-3 shows the difference between the external interrupt generation timings with or without sampling after detection of the edge.

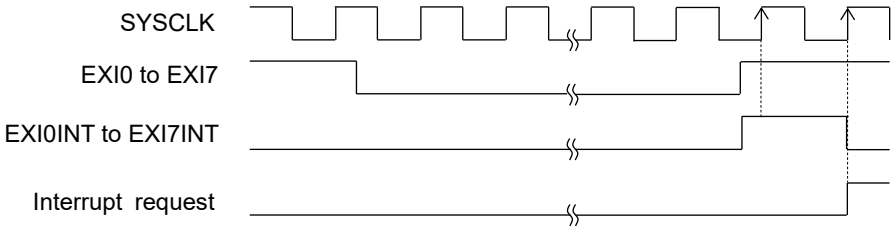
Table 18-3 EXI0T to EXI7INT occurrence After Detection of Edge of EXI0 to EXI7

Sampling	Generation timing
No	Occurs synchronously to the system clock
Yes	After three times matches*2 with the sampling clock, it occurs synchronously to the system clock

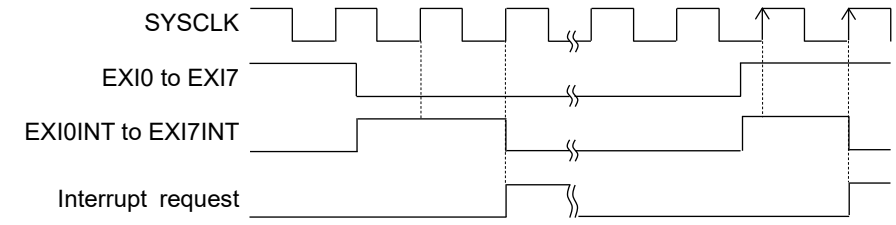
*1 : The edge to be detected is selected by EICON0 register.
*2 : When there is no change in EXI0 to EXI7 for 3 clocks after edge detection, EXI0INT to EXI7INT is occurred synchronously to the system clock.



(a) When falling-edge interrupt mode is chosen



(b) When rising-edge interrupt mode is chosen



(c) When both-edge interrupt mode is chosen

Figure 18-3 External Interrupt Generation Timing (without Sampling)

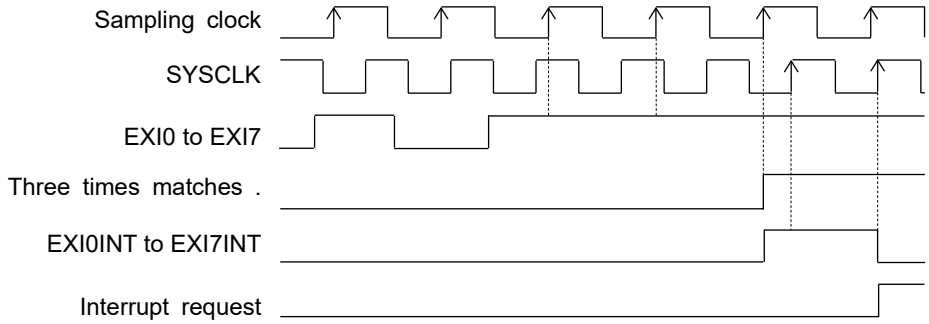
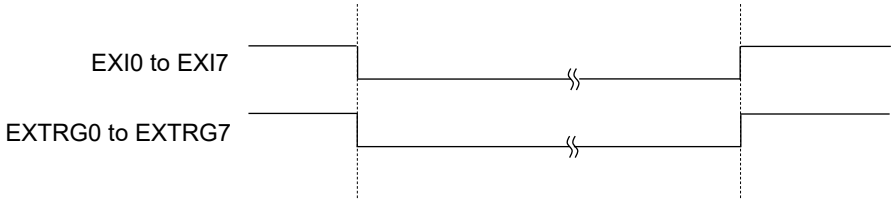


Figure 18-4 External Interrupt Generation Timing (with Sampling, with Rising-edge Interrupt Mode Chosen)

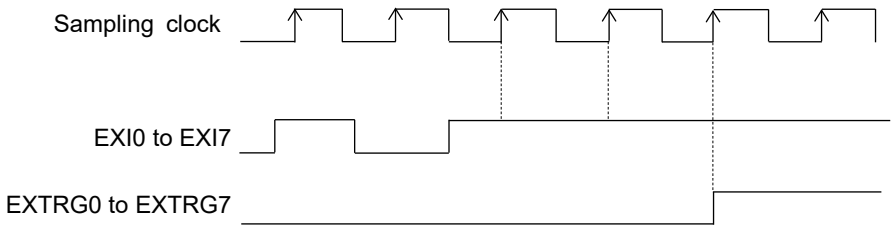
18.3.2 External Trigger Signal

Pins assigned with external interrupt is available as external trigger signals (EXTRG0 to EXTRG7) for the 16-bit timer and function timer.
In addition, the sampling function contained in the external interrupt function is available.

Figure 18-5 shows the external trigger signal timing.



(a) Without sampling



(b) With sampling

Figure 18-5 Functional Timer Trigger Signal

18.3.3 External Interrupt Setting Flow

Figure 18-6 shows the external interrupt setting flow.

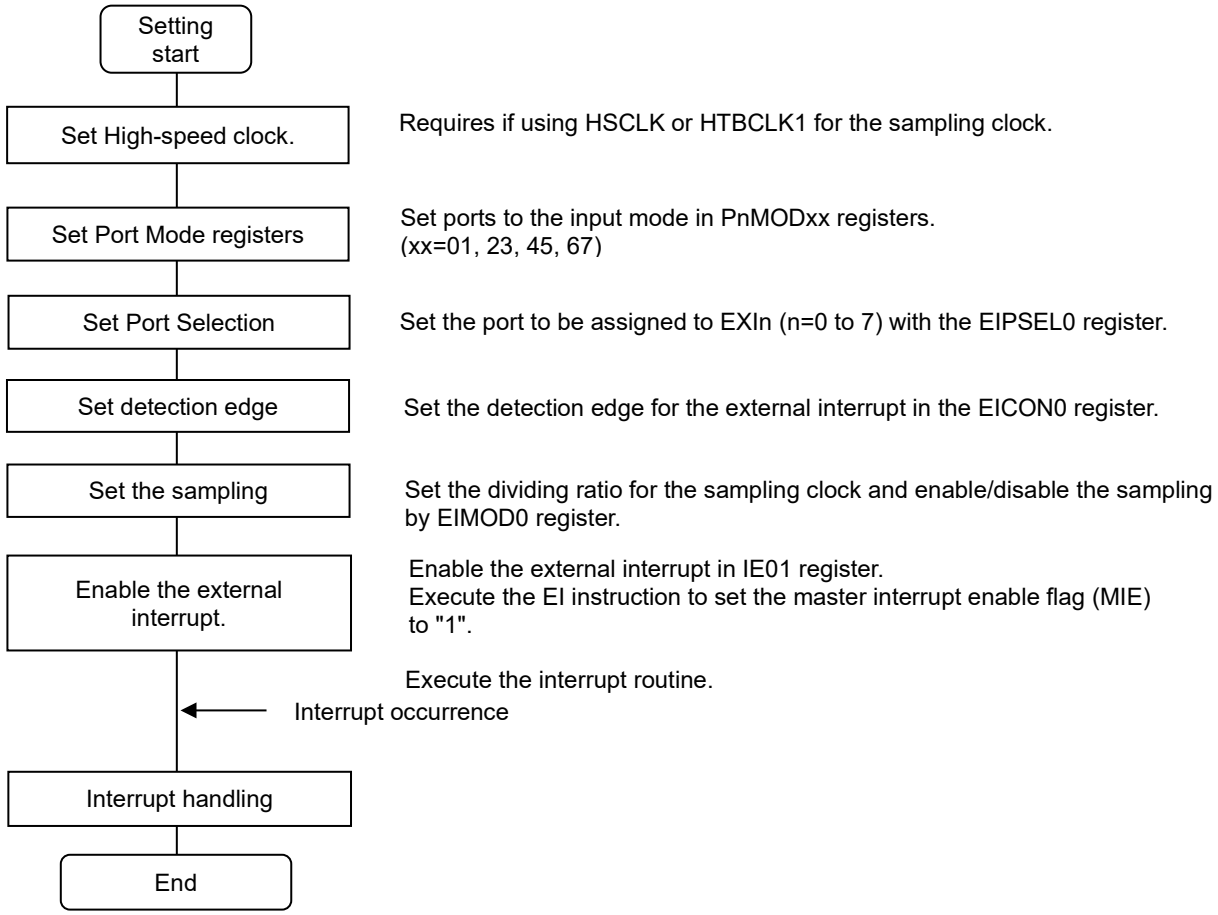
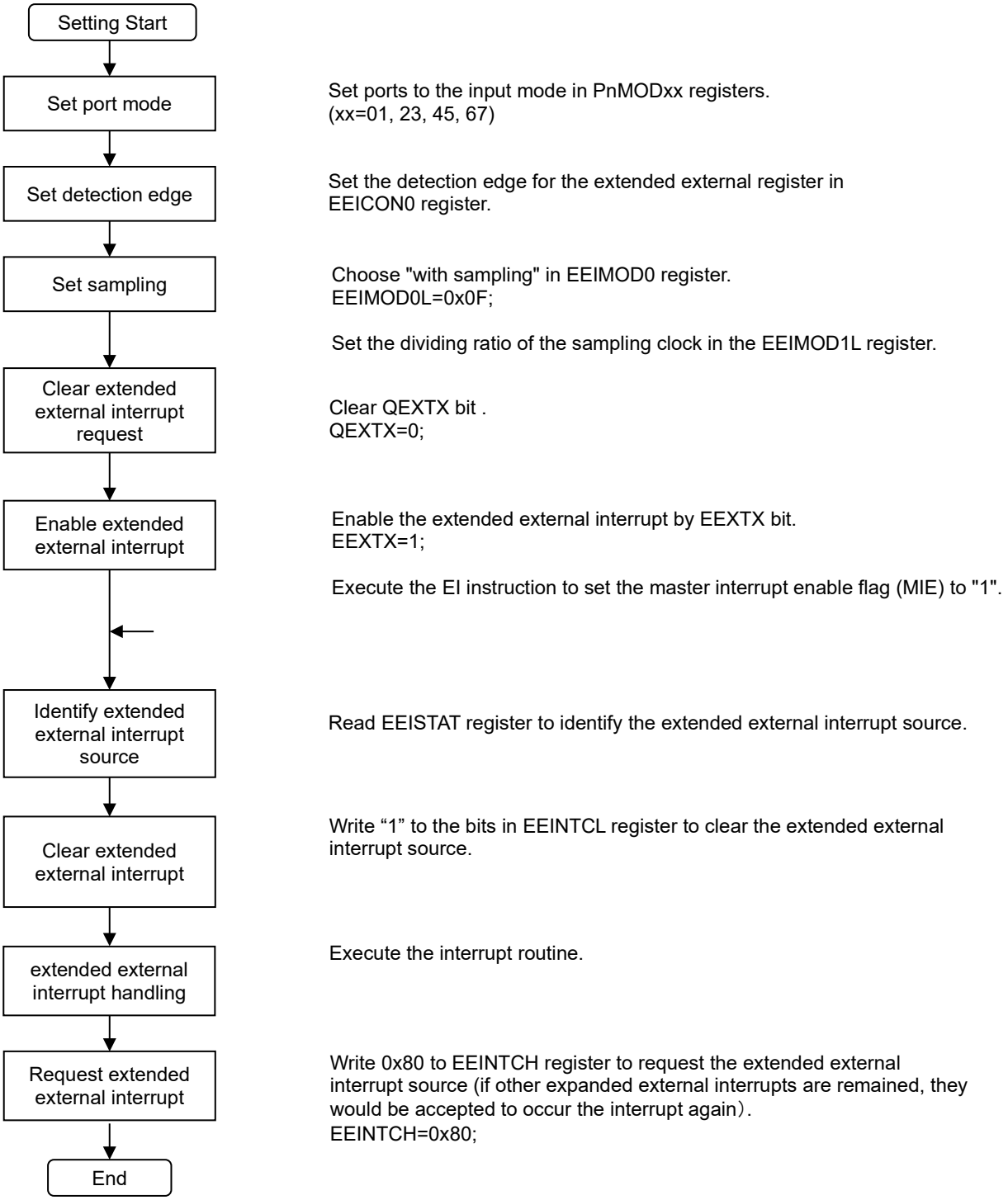


Figure 18-6 External Interrupt Setting Flow

18.3.4 Expanded External Interrupt Setting Flow

Figure 18-7 shows the expanded external interrupt setting flow.



*1:Re-request interrupt by writing "1" to EEIR bit of EEITNTC register when interrupt request registers (IRQ01, IRQ23, IRQ45, IRQ67) are written by CPU while expanded external interrupt is enabled.

Figure 18-7 Expanded External Interrupt Setting Flow

Chapter 19 CRC Calculator

19. CRC Calculator

19.1 General Description

ML62Q2700 groups have the CRC (Cyclic Redundancy Check) calculator that performs CRC calculation and generates the CRC data used for error detection in serial communications.
Also, It has automatic CRC calculation mode to check data in program memory, available in HALT mode or HALT-H mode.

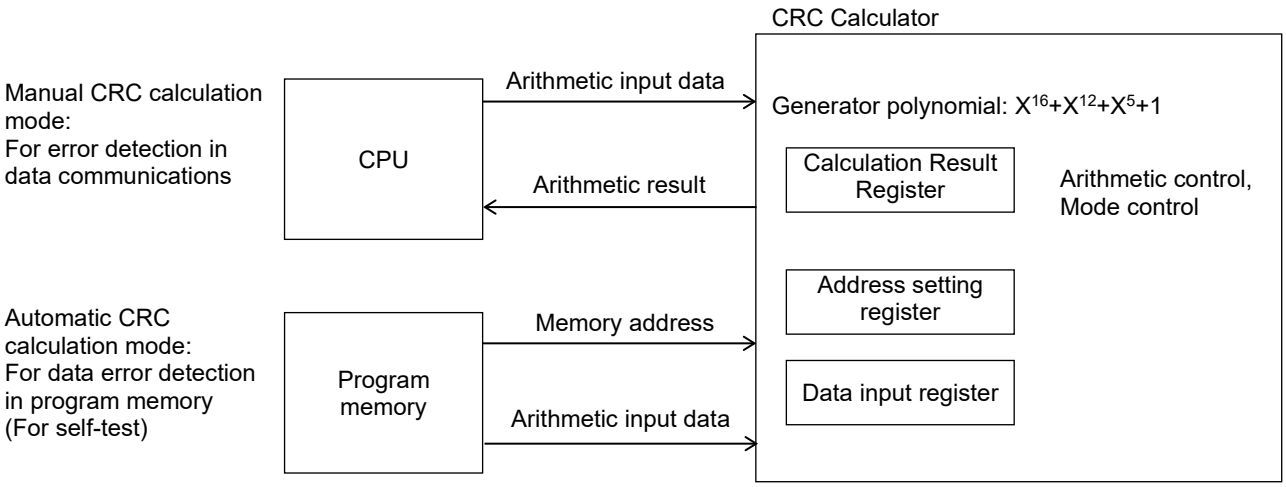


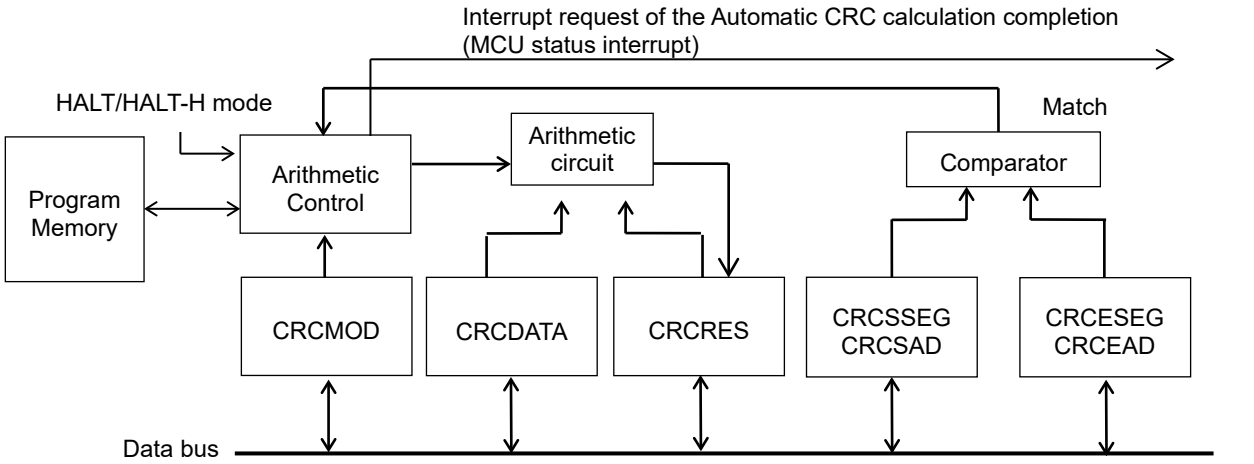
Figure 19-1 CRC calculator overview

19.1.1 Features

- Manual CRC calculation mode
  Generates CRC data from data set in CRC calculation register by the software
  Calculation unit is 8bit
- Automatic CRC calculation mode
  Automatic CRC calculation by the hardware to check data in program memory in HALT or HALT-H mode and generates CRC data
  Calculation unit is 32bit. The interrupt occurs when the arithmetic operation is completed
- Generator polynomial: $X^{16}+X^{12}+X^5+1$
- MSB first or LSB first is selectable

19.1.2 Configuration

Figure 19-2 shows the configuration of the CRC calculator.



CRCMOD : CRC Calculation Mode Register
CRCDATA : CRC Calculation Data Register
CRCRES : CRC Calculation Result Register
CRCSSEG : Automatic CRC Calculation Start Segment Setting Register
CRCESEG : Automatic CRC Calculation End Segment Setting Register
CRCSAD : Automatic CRC Calculation Start Address Setting Register
CRCEAD : Automatic CRC Calculation End Address Setting Register

Figure 19-2 Configuration of CRC Generator

19.2 Description of Registers

19.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF0D0	Automatic CRC Calculation Start Address Setting Register	CRCSADL	CRCSAD	R/W	8/16	0x00
0xF0D1		CRCSADH		R/W	8	0x00
0xF0D2	Automatic CRC Calculation End Address Setting Register	CRCEADL	CRCEAD	R/W	8/16	0xFC
0xF0D3		CRCEADH		R/W	8	0xFF
0xF0D4	Automatic CRC Calculation Start Segment Setting Register	CRCSSEG	-	R/W	8	0x00
0xF0D5	Reserved register	-	-	-	-	-
0xF0D6	Automatic CRC Calculation End Segment Setting Register	CRCESEG	-	R/W	8	0x0F
0xF0D7	Reserved register	-	-	-	-	-
0xF0D8	CRC Calculation Data Register	CRCDATA	-	R/W	8	0x00
0xF0D9	Reserved register	-	-	-	-	-
0xF0DA	CRC Calculation Result Register	CRCRESL	CRCRES	R/W	8/16	0xFF
0xF0DB		CRCRESH		R/W	8	0xFF
0xF0DC	CRC Calculation Mode Register	CRCMOD	-	R/W	8	0x00
0xF0DD	Reserved register	-	-	-	-	-

19.2.2 Automatic CRC Calculation Start Address Setting Register (CRCSAD)

CRCSAD is a SFR to set the start address of automatic CRC calculation.
This register is incremented during the automatic CRC calculation mode. This register is writable if the CRCAEN bit of the CRCMOD register is "0".

Address: 0xF0D0 (CRCSADL/CRCSADL), 0xF0D1 (CRCSADH)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CRCSAD															
Byte	CRCSADH								CRCSADL							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

19.2.3 Automatic CRC Calculation End Address Setting Register (CRCEAD)

CRCEAD is a SFR to set the end address of automatic CRC calculation.
To write this register is available if the CRCAEN bit of the CRCMOD register is "0" only.

Address: 0xF0D2 (CRCEADL/CRCEAD), 0xF0D3 (CRCEADH)
Access: R/W
Access size: 8/16 bit
Initial value: 0xFFFC

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CRCEAD															
Byte	CRCEADH								CRCEADL							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

[Note]

- **Automatic CRC calculation is four-byte length. Generate an expected value by four bytes. Writing to the bits 1 and bit0 are ignored; they are fixed to "1" internally during the calculation.**
- **If an address set to CRCEAD and CRCESEG is smaller than one of CRCSAD and CRCSSEG, the calculation does not execute. Do not specify segment or address out of program code area. See Section 2.5 "Program Memory Space" for details of the program code area.**

19.2.4 Automatic CRC Calculation Start Segment Setting Register (CRCSSEG)

CRCSSEG is a SFR to set the start segment of automatic CRC calculation.
This register is incremented during the automatic CRC calculation mode. This register is writable if the CRCAEN bit of the CRCMOD register is "0".

Address: 0xF0D4 (CRCSSEG)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								CRCSSEG							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

19.2.5 Automatic CRC Calculation End Segment Setting Register (CRCESEG)

CRCESEG is a SFR to set the end segment of automatic CRC calculation.
To write this register is available if the CRCAEN bit of the CRCMOD register is "0" only.

Address: 0xF0D6 (CRCESEG)
Access: R/W
Access size: 8 bit
Initial value: 0xFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								CRCESEG							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

[Note]

- **If an address set to CRCEAD and CRCESEG is smaller than one of CRCSAD and CRCSSEG, the calculation does not execute. Do not specify segment or address out of program code area. See Section 2.5 "Program Memory Space" for details of the program code area.**

19.2.6 CRC Calculation Data Register (CRCDATA)

CRCDATA is a SFR to set the CRC calculation data. Set it by eight bits.
One clock after writing data to the CRCDATA, the calculation result is stored in the CRC Calculation Result Register (CRCRES). This register is writable if the CRCAEN bit of the CRCMOD register is "0".

Address: 0xF0D8 (CRCDATA)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								CRCDATA							
Bit	-	-	-	-	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

19.2.7 CRC Calculation Result Register (CRCRES)

CRCRES is a SFR. The CRC calculation result is stored by the hardware.
Set data to the CRCRES as an initial data for the CRC calculation. To write this register is available if the CRCAEN bit of the CRCMOD register is "0" only.

Address: 0xF0DA (CRCRESL/CRCRES), 0xF0DB (CRCRESH)
Access: R/W
Access size: 8/16 bit
Initial value: 0xFFFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CRCRES															
Byte	CRCRESH								CRCRESL							
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

19.2.8 CRC Calculation Mode Register (CRCMOD)

CRCMOD is SFR to control the CRC calculation mode.

Address: 0xF0DC (CRCMOD)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								CRCMOD							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRCDIR	CRCAEN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 2	-	Reserved bit
1	CRCDIR	Select the shift direction of the CRC calculation. 0: LSB first (Initial value) 1: MSB first
0	CRCAEN	Enable the automatic CRC calculation mode. If entering the HALT/HALT-H mode when the CRCAEN bit is "1", the CRC calculation starts for the program code area in the range specified by the CRCSSEG and CRCESEG register and CRCSAD and CRCEAD register. When CRC calculation is completed, the CRCAEN is reset to "0.", also the CRC calculation completion interrupt is generated. See Chapter 29 "Safety Function" for details of the automatic CRC calculation completion interrupt. 0: Disable the automatic CRC calculation mode (Initial value) 1: Enable the automatic CRC calculation mode

19.3 Description of Operation

Two modes are available for the CRC calculator: manual CRC calculation mode and automatic CRC calculation mode.

- Manual CRC Calculation Mode
  CRC calculation is executed by hardware as needed through writing data to the CRC calculation register by software.
  Calculation unit: 8-bit.
- Automatic CRC Calculation Mode
  In the HALT/HALT-H mode, data in the program memory area is automatically CRC-calculated by hardware.
  Calculation unit: 32-bits with the interrupt generated when the automatic CRC calculation is completed.

19.3.1 Manual CRC Calculation Mode

In the manual CRC calculation mode, the calculation result is outputted to the CRC calculation result register (CRCRES) by writing the initial value to the 16-bit CRC calculation result register (CRCRES) then writing data to 8-bit CRC calculation data register (CRCDATA). For data error detection in serial communication, etc., presence of errors can be detected by transferring data with the calculation result attached when transmission and performing the same CRC calculation in the reception side.

19.3.1.1 Use case of Manual CRC Calculation Mode

The following chart shows the process flow of serial transmission with the CRC calculation result attached to data.
In this example, 11-byte data with 0x21 in the beginning is used as transmit data, and calculation result is obtained.
Transmission and CRC calculation data: 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x29, 0x81, 0x7F

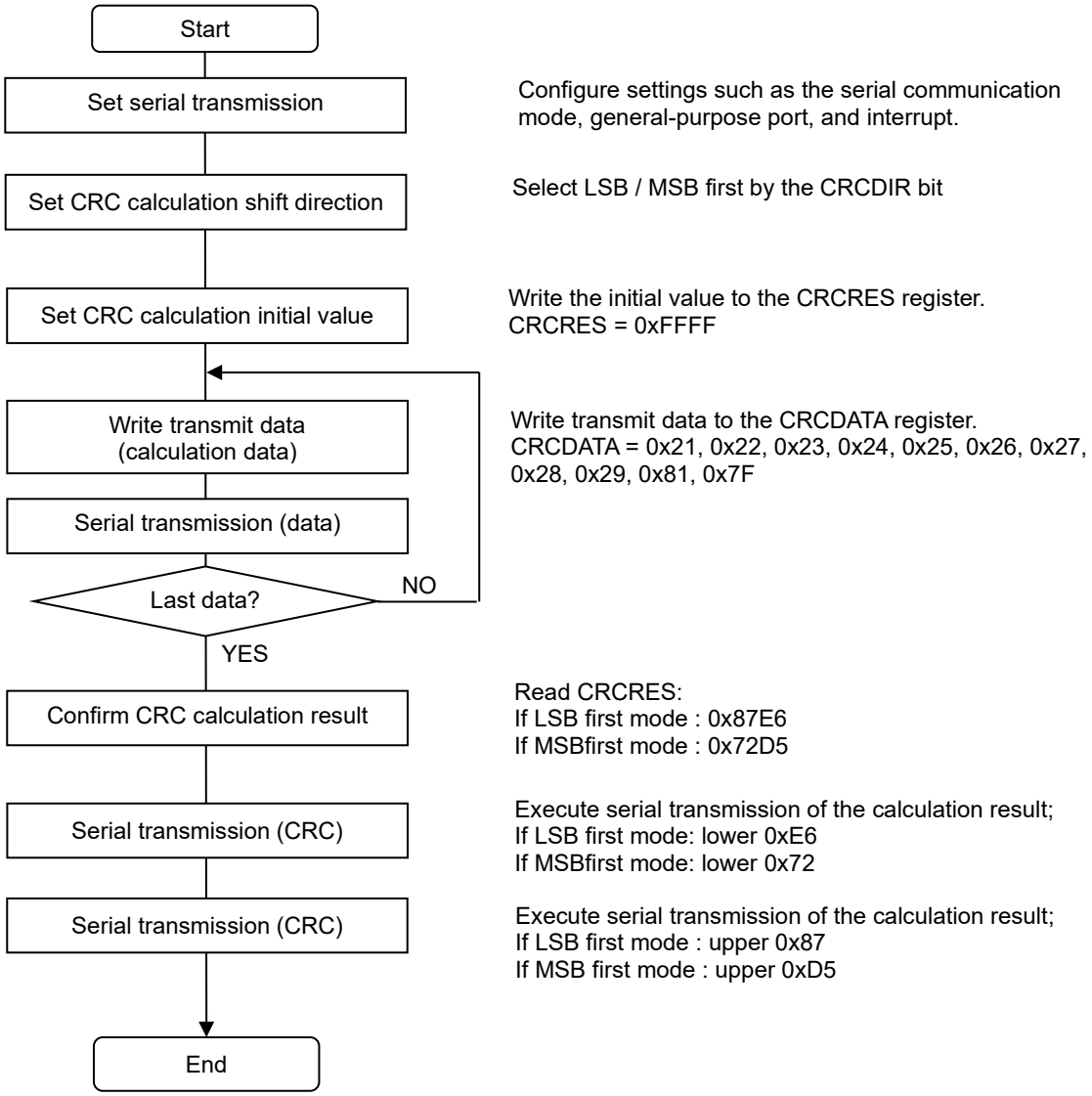


Figure 19-3 CRC Calculation Processing Flow 1 (Serial Transmission)

The following chart shows the CRC calculation process flow with the CRC calculation result attached to the serial receive data.
In this example, 13-byte received data with 0x21 in the beginning is used as calculation data. The first 11 bytes of the CRC calculation result is added to the last two bytes.

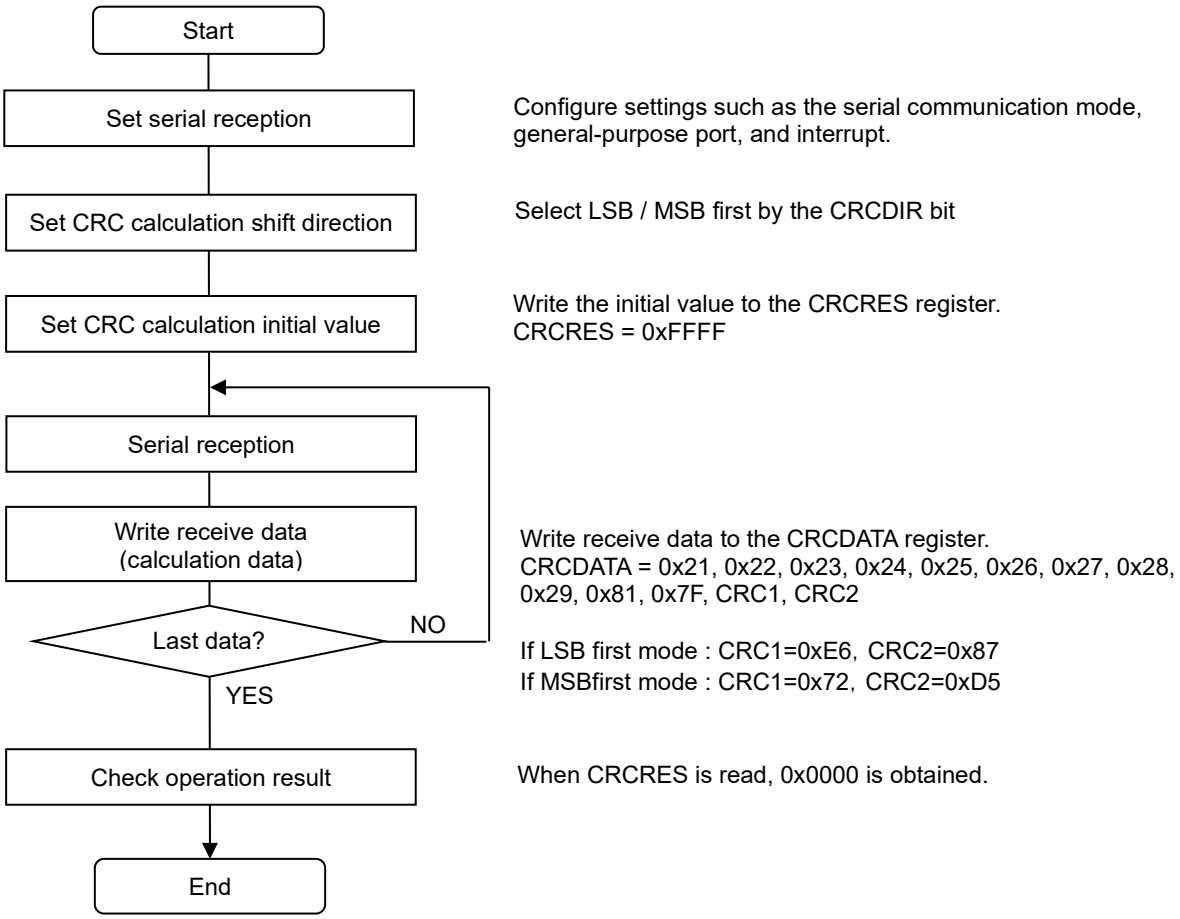


Figure 19-4 CRC Calculation Processing Flow 2 (Serial Reception/LSB First)

19.3.1.2 Operation Timing Chart in Manual CRC Calculation Mode

Set the initial value of CRC calculation in the CRCRES register. When 8-bit data is written to the CRCDATA register, the calculation result is stored in the CRCRES register on the next clock rising-edge. The CRC calculation result can be checked anytime by reading the CRCRES register.
Figure 19-5 shows the operation timing chart of CRC calculation.

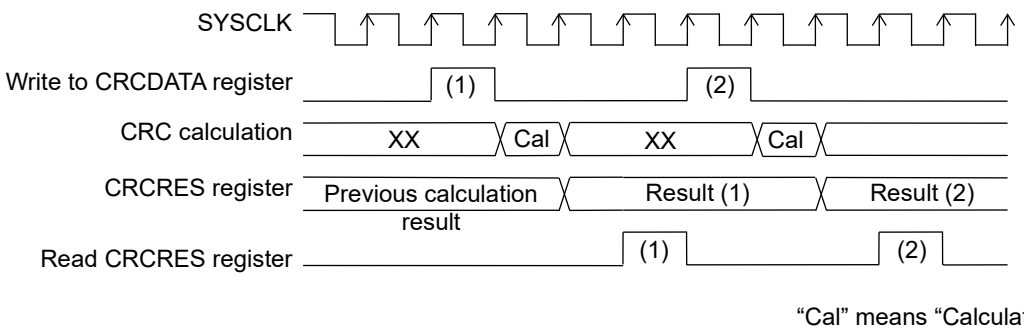


Figure 19-5 Timing Chart of CRC Calculation

19.3.2 Automatic CRC Calculation Mode

In the automatic CRC calculation mode, an arbitrary program memory area is automatically CRC-calculated in the HALT/HALT-H mode and the result is output to the CRC calculation result register (CRCRES). The calculation is four-byte length. Generate an expected value by four bytes.
For data error detection in program memory (for self-test), using software, the result of the automatic calculation can be compared with the expected value written to Flash memory in advance.
The expected value is created in the generation tool of the ROM code data from LAPIS.

19.3.2.1 Example of Use of Automatic CRC Calculation Mode

The following chart shows the automatic CRC calculation process flow.

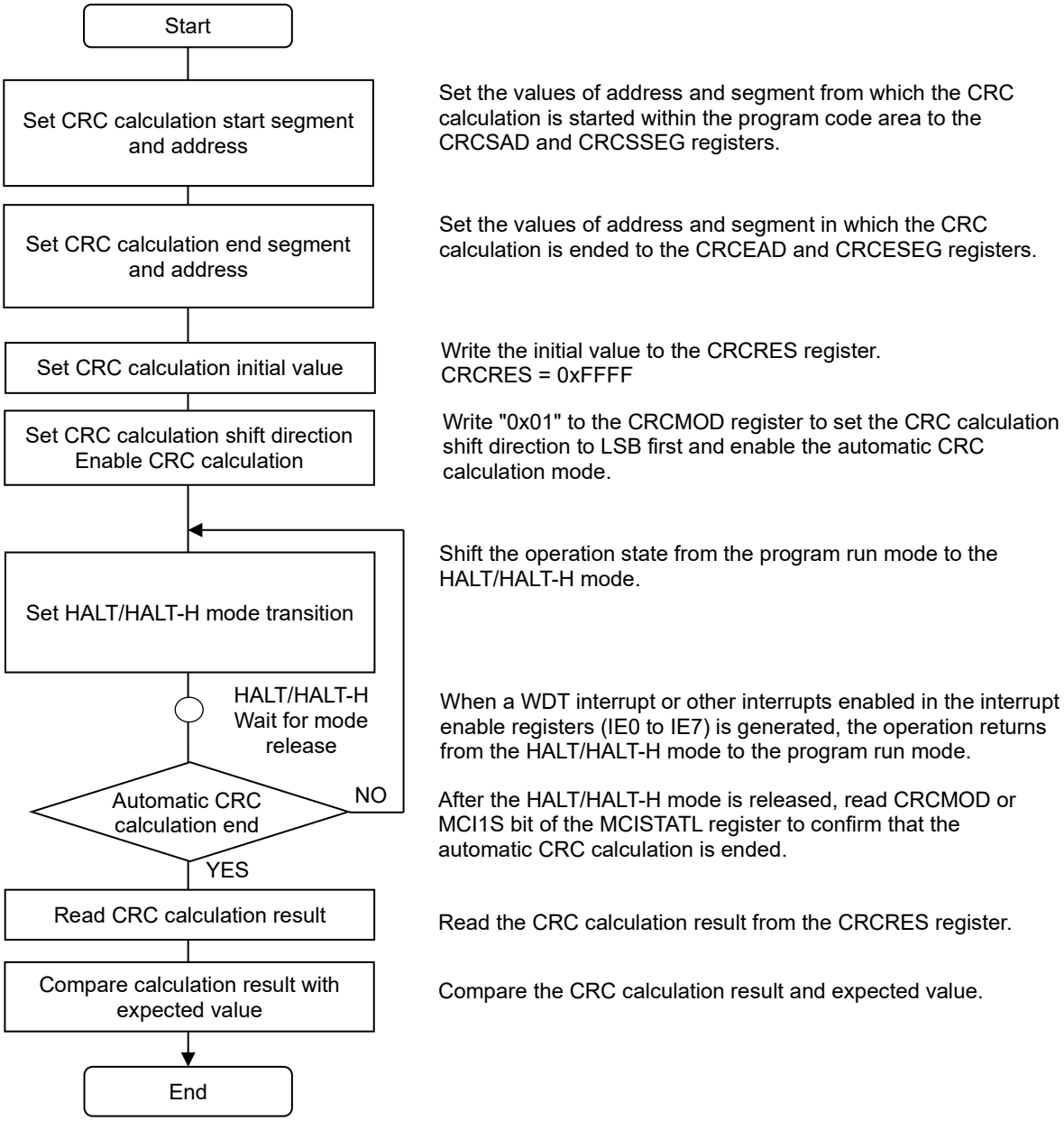


Figure 19-6 Automatic CRC Calculation Process Flow

The CRC calculation of data in the program code area configured in the CRCSSEG, CRCSAD, CRCESEG, and CRCEAD registers is started when entering to the HALT/HALT-H mode, if the CRCAEN bit of CRCMOD register is "1".

When the HALT/HALT-H mode released while the calculation is in progress, the calculation is aborted. If shifting to the HALT/HALT-H mode again, the calculation resumes at the address it was aborted. The CRCSSEG and CRCAD registers are incremented each time data is read from the program code area.

If the calculation starts segment and address (values of CRCSSEG and CRCSAD registers) match the calculation end segment and address (values of CRCESEG and CRCEAD registers), the CRC calculation is ended, the CRCAEN bit becomes "0", and the automatic CRC calculation completion interrupt request is generated. If the automatic CRC calculation completion interrupt is enabled, then the HALT/HALT-H mode is released and the MCU status interrupt is generated.

To enable/disable the automatic CRC calculation completion interrupt is set by the MCU status interrupt enable register (MCINTEL). See Chapter 29 "Safety Function" for details of the MCINTEL register.

See "ML62Q2000 Series Self-test Sample Software AP Notes" and a manual of the generation tool of the ROM code data for details of self-test program using the automatic CRC calculation mode or how to generate expected values.

[Note]

- **To perform CRC calculation in the manual mode when automatic CRC calculation is not completed, save the value in the CRCRES register before calculation. Once the CRC calculation in the manual mode is completed, move the saved value back to the CRCRES register and set the CRCAEN bit to "1". If entering the HALT/HALT-H mode, then the automatic CRC calculation can be restarted.**
- **The final addresses at the end of the previous operation are stored in the CRCSAD and CRCSSEG registers. If values in the CRCSAD and CRCSSEG registers are overwritten with the CRCAEN bit set to "0", the calculation works incorrectly.**

Chapter 22 Voltage Level Supervisor

22. Voltage Level Supervisor

22.1 General Description

ML62Q2700 group has the Voltage Level Supervisor (VLS: Voltage Level Supervisor) that detects whether the voltage level of V_{DD} is lower or higher than the specified threshold voltage.

22.1.1 Features

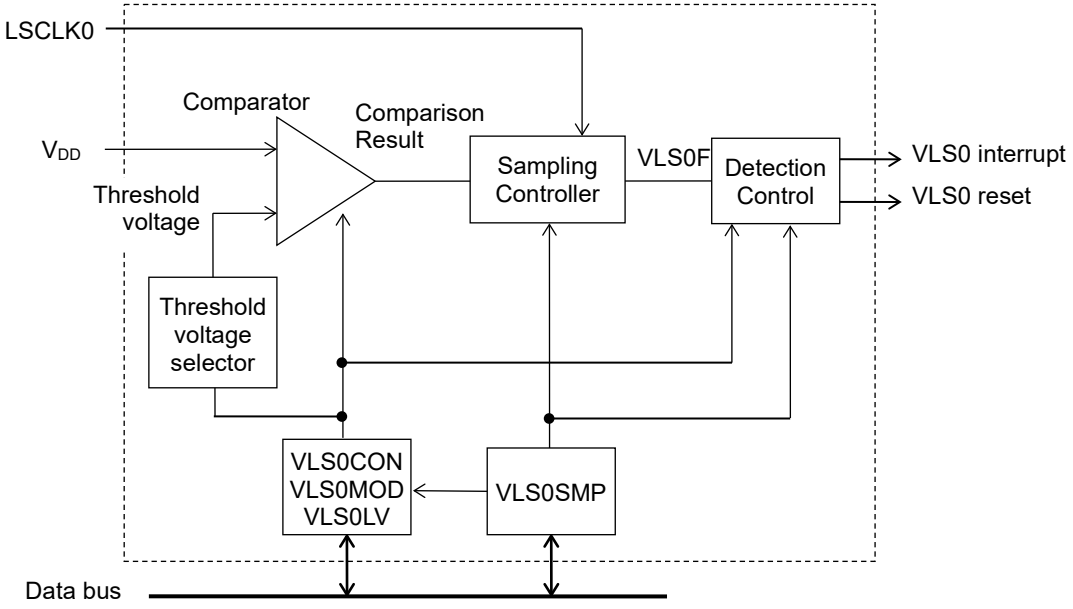
- Accuracy: ±4 %
- Threshold voltage: Selectable from 15 values (1.85 to 4.00V)
- Operation mode: Supervisor mode (continuous detection) or single mode (single detection)

Mode	Description
Single mode 1	Detect the voltage level of V_{DD} only once. The interrupt occurs after detecting the voltage of V_{DD}, indicates the detection has been completed.
Single mode 2	Detect the voltage level of V_{DD} only once. The interrupt occurs after detecting the voltage of V_{DD} is lower than the threshold voltage, indicates the MCU is in the low voltage condition.
Supervisor mode	Detect continuously the voltage level of V_{DD}, suitable for always detecting the low voltage level of V_{DD} and generating the interrupt or reset. The interrupt or reset occurs according to the setting in the VLS0MOD register. The VLS0 reset function is available by choosing the supervisor mode.

- Voltage level supervisor reset (VLS0 reset)
- Voltage level supervisor interrupt (VLS0 interrupt)
- Initialized by the power-on reset (POR) or pin reset

22.1.2 Configuration

Figure 22-1 shows the configuration of the VLS.



VLS0CON : Voltage level supervisor 0 control register
VLS0MOD : Voltage level supervisor 0 mode register
VLS0LV : Voltage level supervisor 0 level register
VLS0SMP : Voltage level supervisor 0 sampling register

Figure 22-1 Configuration of Voltage Level Supervisor

22.2 Description of Registers

22.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF890	Voltage level supervisor 0 control register	VLS0CON	-	R/W	8	0x00
0xF891	Reserved register	-	-	-	-	-
0xF892	Voltage level supervisor 0 mode register	VLS0MOD	-	R/W	8	0x00
0xF893	Reserved register	-	-	-	-	-
0xF894	Voltage level supervisor 0 level register	VLS0LV	-	R/W	8	0x0E
0xF895	Reserved register	-	-	-	-	-
0xF896	Voltage level supervisor 0 sampling register	VLS0SMP	-	R/W	8	0x00
0xF897	Reserved register	-	-	-	-	-

22.2.2 Voltage Level Supervisor 0 Control Register (VLS0CON)

VLS0CON is a SFR to control the VLS.
This register is initialized only with power on reset and pin reset.

Address: 0xF890 (VLS0CON)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VLS0CON							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	VLS0RF	VLS0F	VLS0EN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 3	-	Reserved bit
2	VLS0RF	Indicate whether the voltage level detection result is valid or not. This bit is valid only in the supervisor mode. It is fixed to "0" in the single mode. 0: VLS is stopped or VLS is being stabilized (initial value) 1: VLS detection result is valid (readable state)
1	VLS0F	Monitor the voltage level. This bit retains the last detection result. This bit is cleared to "0" by writing "1", but not cleared to “0” by writing "0". Also, this bit is cleared to "0" when the VLS starts operating. 0: Voltage (V_{DD}) is higher than the threshold voltage (initial value) 1: Voltage (V_{DD}) is lower than the threshold voltage
0	VLS0EN	Control the VLS operation. In the single mode, this bit is automatically reset to "0" after detecting the voltage level and the VLS stops operating. 0: Disable VLS operating (Initial value) 1: Enable VLS operating

[Note]

- **There is a limitation in each mode for entering the STOP/STOP-D mode while the VLS is running.**

Operation	Description
Running in Supervisor mode	Only when the VLS0RF bit is "1", able to enter the STOP/STOP-D mode.
Running in Single mode	Unable to enter the STOP/STOP-D mode. After stopping single mode operation (VLS0EN bit = "0"), enter to the STOP/STOP-D mode.

- **If a reset other than power-on reset and pin reset occurs during VLS operation, the VLS retains its operating state.**

22.2.3 Voltage Level Supervisor 0 Mode Register (VLS0MOD)

VLS0MOD is a SFR to control the operation mode of the VLS.
Set this register only when the VLS is stopped (VLS0EN bit of VLS0CON register is "0").
Also, this register is initialized only with power on reset and pin reset.

Address: 0xF892 (VLS0MOD)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VLS0MOD							
Bit	-	-	-	-	-	-	-	-	-	-	VLS0AMD1	VLS0AMD0	-	-	VLS0SEL1	VLS0SEL0
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7, 6	-	Reserved bits
5, 4	VLS0AMD1, VLS0AMD0	Select the VLS operating mode 00: Single mode 1 (Initial value) It detects the voltage level of V_{DD} only once. When VLS0SEL1 and VLS0SEL0 bits are "0x2", the interrupt occurs when detecting the voltage level of V_{DD}. The result can be checked by reading VLS0F bit of VLS0CON register. 01: Single mode 2 It detects the voltage level of V_{DD} only once. When VLS0SEL1 and VLS0SEL0 bits are "0x2", the interrupt occurs when detecting the voltage level of V_{DD} is lower than the threshold voltage (when the VLS0F of VLS0CON is "1"). 1X: Supervisor mode It always detects the voltage level of V_{DD}. The interrupt or reset occurs depending on the conditions of VLS0SEL1 and VLS0SEL0 bits.
3, 2	-	Reserved bits
1, 0	VLS0SEL1, VLS0SEL0	Control enable/disable of the VLS0 reset / VLS0 interrupt request. See section 22.3 “Description of Operation” for details of the occurrence condition of VLS0 reset / VLS0 interrupt request. 00: disable Reset function, disable Interrupt function (Initial value) 01: enable Reset function, disable Interrupt function 10: disable Reset function, enable Interrupt function 11: enable Reset function, disable Interrupt function

[Note]

- **There is a limitation in each mode for entering the STOP/STOP-D mode while the VLS is running.**

Operation	Description
Running in Supervisor mode	Only when the VLS0RF bit is "1", able to enter the STOP/STOP-D mode.
Running in Single mode	Unable to enter the STOP/STOP-D mode. After stopping single mode operation (VLS0EN bit = "0"), enter to the STOP/STOP-D mode.

22.2.4 Voltage Level Supervisor 0 Level Register (VLS0LV)

VLS0LV is a SFR to set the threshold voltage for VLS detection.
Set this register only when the VLS0 is stopped (VLS0EN bit of VLS0CON register is "0").
Also, this register is initialized only with power on reset and pin reset.

Address: 0xF894 (VLS0LV)
Access: R/W
Access size: 8 bit
Initial value: 0x0E

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VLS0LV							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	VLS0LV3	VLS0LV2	VLS0LV1	VLS0LV0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit No.	Bit symbol name	Description
7 to 4	-	Reserved bits
3 to 0	VLS0LV3 to VLS0LV0	Select the threshold voltage (V_{VLSF} / V_{VLSR}) of VLS detected while the V_{DD} is falling or rising. VLS has hysteresis characteristics. For the characteristics of threshold voltage detected while the power is falling or rising, see the ML62Q2700 data sheet. 0000: 3.99V ± 4% 0001: 3.68V ± 4% 0010: 3.05V ± 4% 0011: 2.96V ± 4% 0100: 2.84V ± 4% 0101: 2.76V ± 4% 0110: 2.66V ± 4% 0111: 2.54V ± 4% 1000: 2.45V ± 4% 1001: 2.35V ± 4% 1010: 2.24V ± 4% 1011: 2.16V ± 4% 1100: 2.05V ± 4% 1101: 1.95V ± 4% 1110: 1.85V ± 4% (Initial value) 1111: Do not use (1.85V±4%)

22.2.5 Voltage Level Supervisor 0 Sampling Register (VLS0SMP)

VLS0SMP is a SFR to control sampling the voltage level detection.
Set this register only when the VLS0 is stopped (VLS0EN bit of VLS0CON register is "0").
This register is resettable by Power On Reset (POR) and RESET_N pin reset only.

Address: 0xF896 (VLS0SMP)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VLS0SMP							
Bit	-	-	-	-	-	-	-	-	-	rsvd	VLS0DIV1	VLS0DIV0	VLS0SM1	rsvd	-	-
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7	-	Reserved bit
6	rsvd	Reserved bit
5 to 4	VLS0DIV1 to VLS0DIV0	Select frequency dividing ratio for the sampling clock. 00: No dividing (Initial value) 01: divided by 2 10: divided by 4 11: divided by 8
3	VLS0SM1	Select the sampling clock source for detecting the voltage level. 0: No sampling (Initial value) 1: LSCLK0
2	rsvd	Reserved bit. Always set "0".
1, 0	-	Reserved bits

[Note]
- **In the STOP/STOP-D mode, the VLS works without sampling regardless the setting in VLS0SM1 bit.**

22.3 Description of Operation

VLS determines whether V_{DD} is higher or lower than the specified threshold voltage and reads it out. It also generates a VLS interrupt or VLS reset.
VLS has hysteresis characteristics. See the data sheet of each product for characteristics of the threshold voltage at power voltage fall / rise.
The following two operation modes are available for VLS:

- Supervisor mode:

Operation	Write "1" to VLS0EN to enable VLS to operate and determines the voltage, and notify the VLS0RF flag when the detection result is valid. VLS continue to determines after that.	
Function	Interrupt of detecting voltage variations	Interrupt occurs when V_{DD} falls below the threshold voltage or V_{DD} varies from lower than the threshold voltage to higher than the threshold voltage.
	Reset of detecting low voltage	Reset occurs when V_{DD} drops below the threshold voltage.

- Single mode:

Operation	Write "1" to VLS0EN to enable VLS to operate and detect the voltage, and when the detection result is valid, "0" is automatically written to VLS0EN to complete the detection.	
Function	Single mode 1: Voltage decision interrupt	The interrupt is occurred at the time of completion of the voltage decision.
	Single mode 2: Low voltage detection interrupt	The interrupt is occurred when the power voltage becomes lower than the threshold voltage.

22.3.1 Supervisor Mode

In the supervisor mode, the voltage level of V_{DD} can be constantly detected. This mode is suitable for using the reset when the low voltage is detected, or the interrupt when the voltage variations is detected.
The supervisor mode always determines the voltage level of V_{DD} and outputs an interrupt when voltage variation is detected and a reset when a low voltage is detected.
Figure 22-2 shows the flow chart for starting the VLS in the supervisor mode.

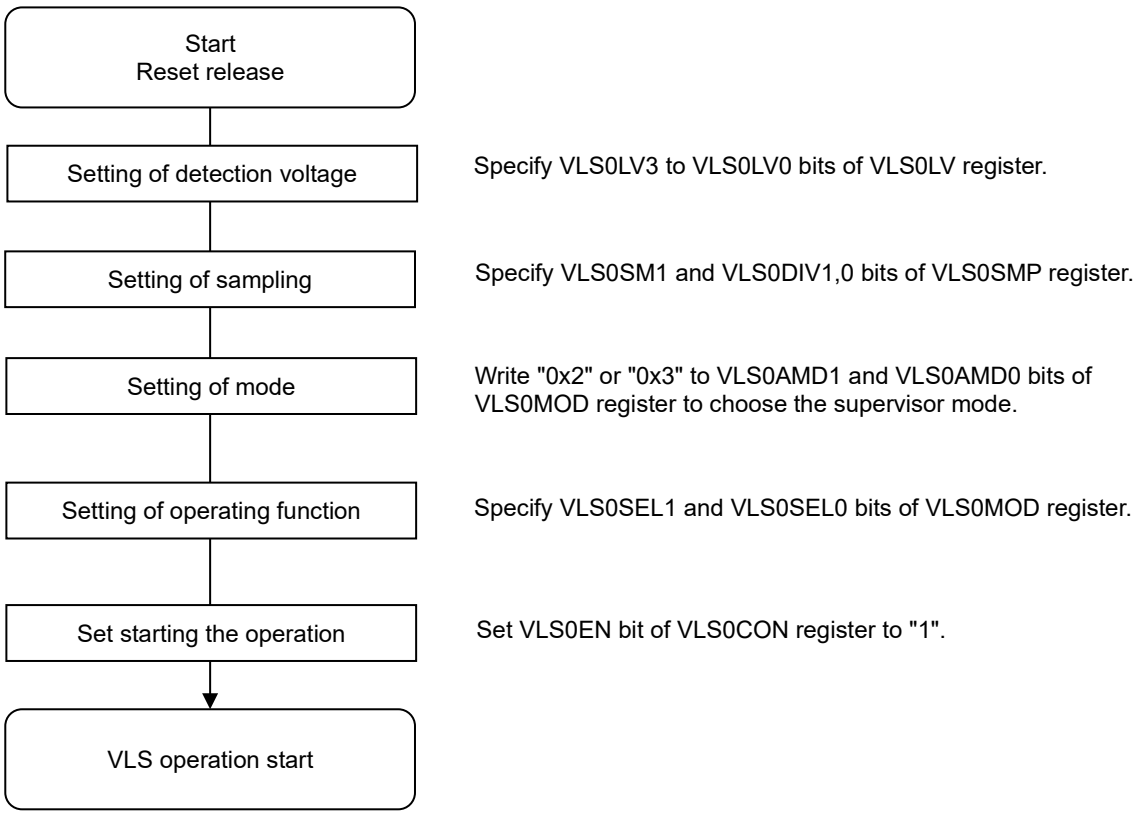


Figure 22-2 Flow chart for starting the VLS in the supervisor mode

22.3.1.1 Reset Output

Figure 22-3 shows the operation timing chart when the VLS0 reset output without sampling is specified.

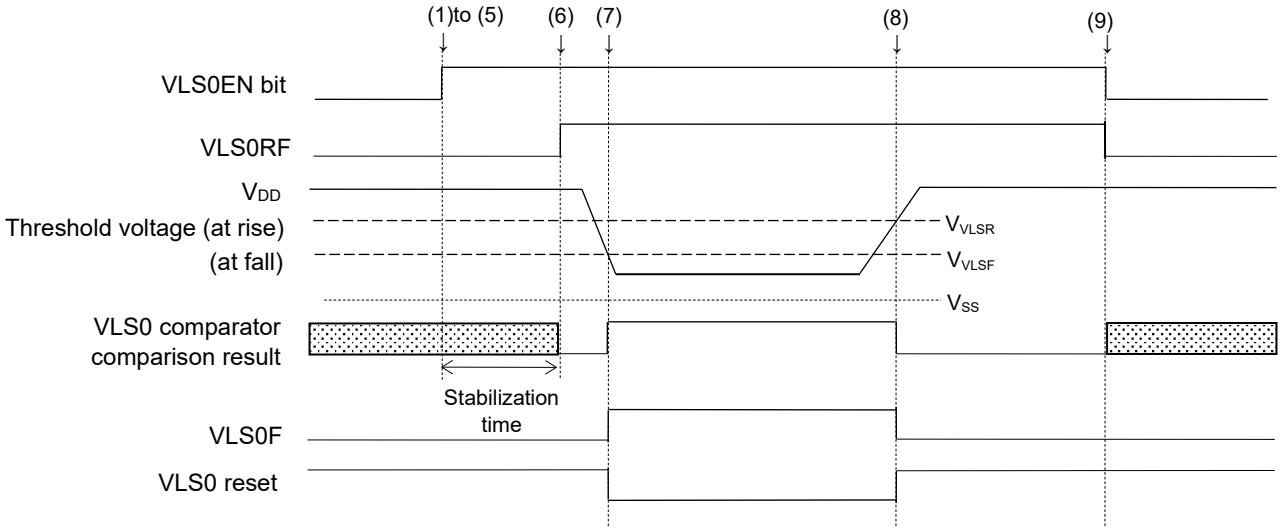


Figure 22-3 Operation Timing Chart When the VLS0 Reset Output without Sampling is specified

The operation shown in Figure 22-3 is described below:

(1) Select the detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "No sampling" by the VLS0SM1bit of the VLS0SMP register.
(3) Write "0x2" or "0x3" to VLS0AMD1 and VLS0AMD0 bits of VLS0MOD register to set to the supervisor mode.
(4) Write “0x1” to VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register to select the VLS0 reset enable.
(5) Set the VLS0EN bit of the VLS0CON register to "1" (VLS0 starts operation in the supervisor mode).
(6) After approximately 300 µs passed, the detection result of VLS0 is stabilized and the VLS0RF bit of the VLSCON register is set to "1" (value of the voltage level supervisor bit (VLS0F) is read in software) (*[1]).
(7) When the power voltage (V_{DD}) becomes below the threshold voltage V_{VLSF}, the VLS0F bit is set to "1" to generate the VLS0 reset.
(8) If V_{DD} varies equal to or above the threshold voltage (V_{VLSR}), the VLS0F bit is cleared to "0" to release the VLS0 reset.
(9) Write "0" to the VLS0EN bit to disable VLS0 operation.

*[1]: VLS0F bit/interrupt/reset is masked until the VLS0RF bit becomes "1".

Figure 22-4 shows the operation timing chart when the VLS0 reset output with sampling is specified.

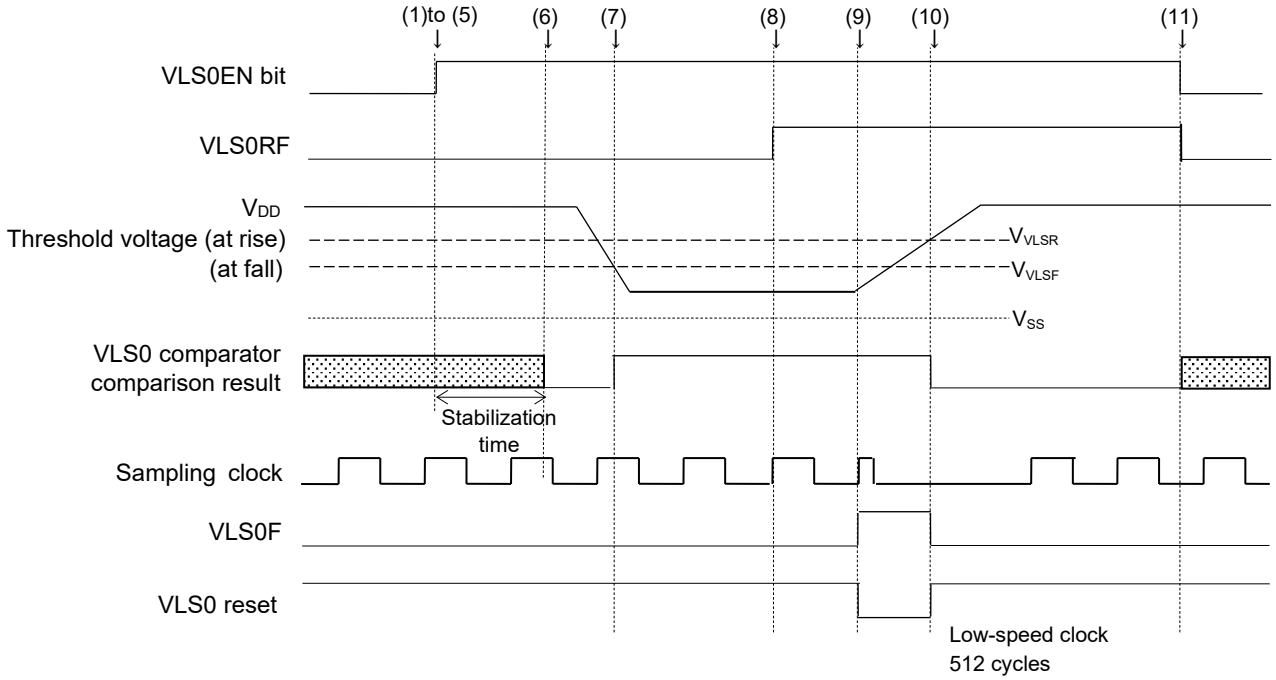


Figure 22-4 Operation Timing Chart When the VLS0 Reset Output with Sampling is specified

The operation shown in Figure 22-4 is described below:

(1) Select a detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "Sampling with LSCLK0" by the VLS0SM1 bit of the VLS0SMP register. And specify sampling clock dividing ratio by the VLS0DIV1 to VLS0DIV0 bits of the VLS0SMP register.
(3) Write "0x2" or "0x3" to VLS0AMD1 and VLS0AMD0 bits of the VLS0MOD register to set to the supervisor mode.
(4) Enable the VLS0 reset by VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register .
(5) Write "1" to the VLS0EN bit to enable VLS operation.
(6) Wait until the comparison result of the VLS comparator is stabilized (approx. 300 μs).
(7) V_{DD} becomes below the threshold voltage (V_{VLSF}).
(8) Once the comparison result of the VLS comparator is stabilized, the VLS0RF bit is set to "1" after three cycles of the sampling clock.
(9) If the comparison result of the VLS comparator is below the threshold voltage (V_{VLSF}) and this condition continues for the duration of three cycles or more of the sampling clock, the VLS0F bit is set to "1" and the VLS0 reset is generated.
(10) If the comparison result of the VLS comparator becomes equal to or above the threshold voltage (V_{VLSR}), the VLS0F bit is cleared to "0" to release the VLS0 reset.
(11) Write "0" to the VLS0EN bit to disable VLS operation.

[Note]

- **Entering the STOP/STOP-D mode is not allowed during the VLS stabilization time. If entering the STOP/STOP-D mode after the supervisor mode is enabled, make sure that the VLS0RF bit is set to "1", and then enter the STOP/STOP-D mode.**
- **The initial value of the VLS detection voltage is 1.85V, so the MCU becomes in reset mode when the V_{DD} is 1.85V or lower and VLS0 is specified as supervisor mode with the reset function. Therefore, set the detection voltage before enabling the VLS0 operation.**
- **When using the reset function of VLS like a reset IC, set the threshold voltage appropriate for the system in the low-speed clock state after starting the power supply, and start VLS.**

22.3.1.2 Interrupt Output

Figure 22-5 shows an example of the operation timing chart when the VLS0 interrupt output without sampling is specified.

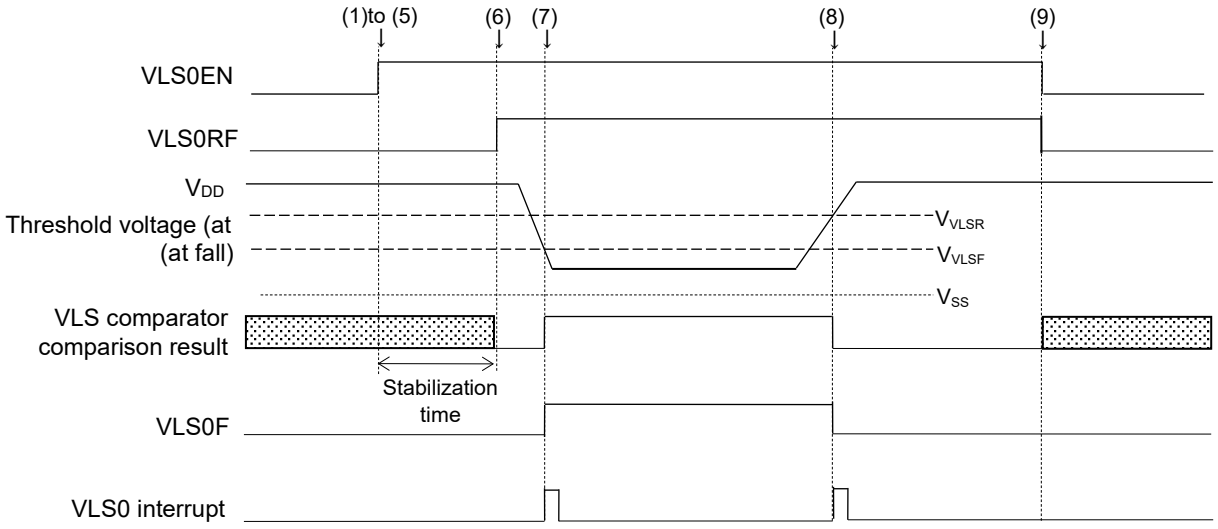


Figure 22-5 Operation Timing Chart When the VLS0 Interrupt Output without Sampling is specified

The operation shown in Figure 22-5 is described below:

(1) Select a detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "No sampling" by the VLS0SM1 bit of the VLS0SMP register.
(3) Write "0x2" or "0x3" to VLS0AMD1 and VLS0AMD0 bits of VLS0MOD register in order to select the supervisor mode.
(4) Enable the VLS0 interrupt by VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register.
(5) Write "1" to the VLS0EN bit to enable VLS operation.
(6) When the comparison result of the VLS comparator is stabilized, the VLS0RF bit is set to "1".
(7) When V_{DD} becomes below the threshold voltage (V_{VLSF}), the VLS0F bit is set to "1" to generate the VLS0 interrupt.
(8) If V_{DD} becomes equal to or above the threshold voltage (V_{VLSR}), the VLS0F bit is cleared to "0" to generate the VLS0 interrupt.
(9) Write "0" to the VLS0EN bit to disable VLS operation.

Figure 22-6 shows an example of the operation timing chart when the VLS0 interrupt output with sampling is specified.

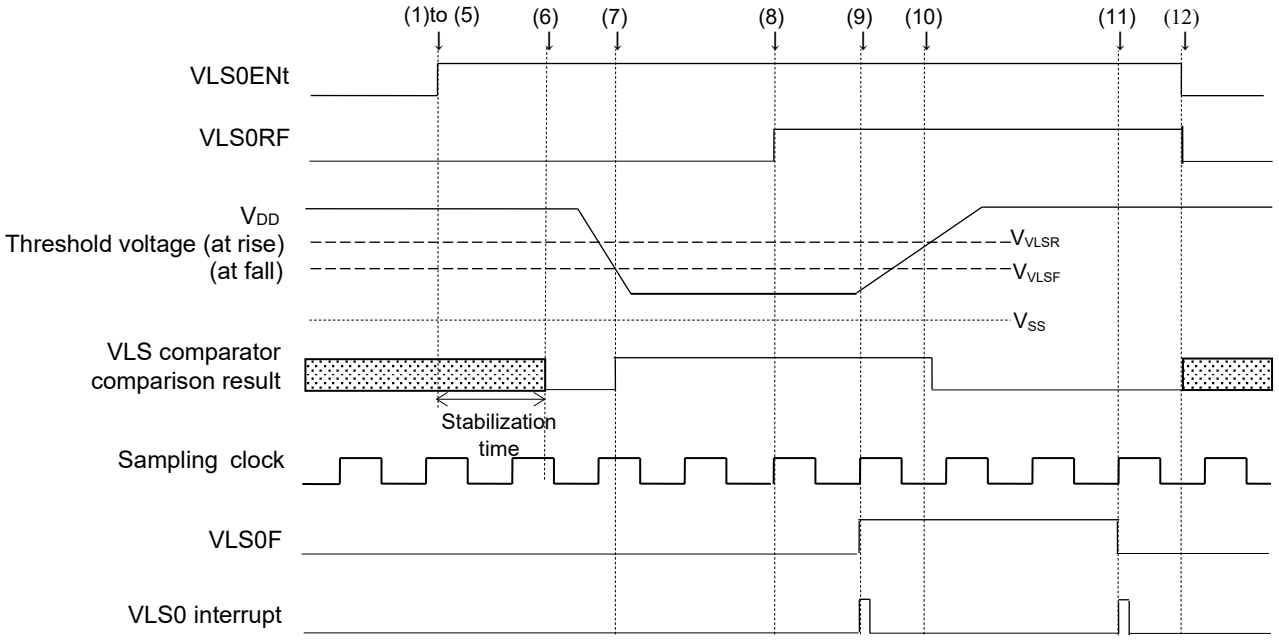


Figure 22-6 Operation Timing Chart When the VLS0 Interrupt Output with Sampling is specified

The operation shown in Figure 22-6 is described below:

(1) Select a detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "Sampling with LSCLK0" by the VLS0SM1 bit of the VLS0SMP register. And specify sampling clock dividing ratio by the VLS0DIV1 to VLS0DIV0 bits of the VLS0SMP register.
(3) Write "0x2" or "0x3" to VLS0AMD1 and VLS0AMD0 bits of VLS0MOD register in order to select the supervisor mode.
(4) Enable VLS0 interrupt by VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register in order to.
(5) Write "1" to the VLS0EN bit to enable VLS operation.
(6) Wait until the comparison result of the VLS comparator is stabilized (approx. 300 μs).
(7) V_{DD} becomes below the threshold voltage (V_{VLSF}).
(8) Once the comparison result of the VLS comparator is stabilized, the VLS0RF bit is set to "1" after three cycles of the sampling clock.
(9) If the comparison result of the VLS comparator is below the threshold voltage (V_{VLSF}) and this condition continues for the duration of three cycles or more of the sampling clock, the VLS0F bit is set to "1" and the VLS0 interrupt is generated.
(10) The comparison result of the VLS comparator becomes equal to or above the threshold voltage (V_{VLSR}).
(11) If the comparison result of the VLS comparator is equal to or above the threshold voltage (V_{VLSR}) and this condition continues for the duration of three cycles or more of the sampling clock, the VLS0F bit is cleared to "0" and the VLS0 interrupt is generated.
(12) Write "0" to the VLS0EN bit to disable VLS operation.

[Note]

- **Entering the STOP/STOP-D mode is not allowed during the VLS stabilization time. If entering the STOP/STOP-D mode after the supervisor mode is enabled, make sure that the VLS0RF bit is set to "1", and then enter the STOP/STOP-D mode.**
- **When VLS0 is stopped (VLS0EN bit="0") while the V_{DD} is lower than the specified threshold voltage (VLS0F bit="1"), the VLS interrupt is generated.**

22.3.2 Single Mode

In the single mode, the software waits for the VLS0 interrupt to detect the voltage. It is suitable for intermittently checking V_{DD}.

Figure 22-7 shows the flow chart for starting the VLS in the single mode.

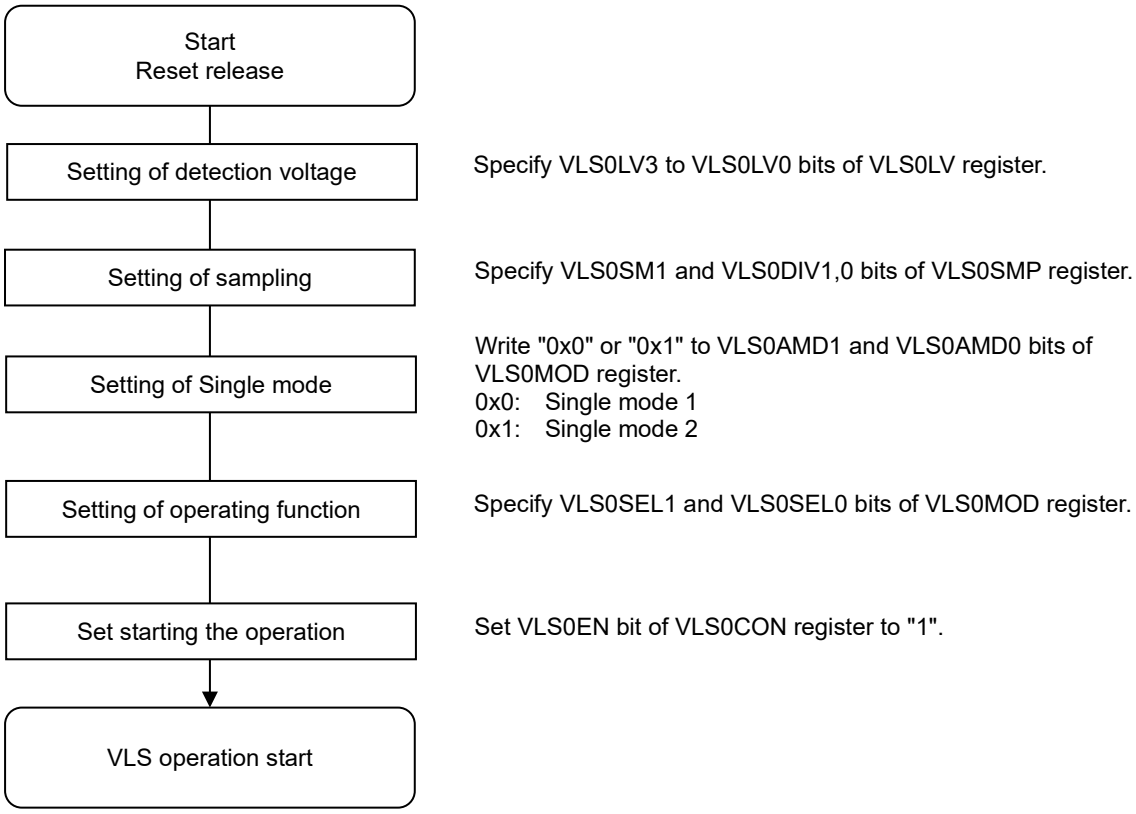


Figure 22-7 Flow chart for starting the VLS in the single mode

22.3.2.1 Single mode 1

The single mode 1 always generates the interrupt at completing the detection.
Figure 22-8 shows an example of the operation timing chart without sampling in single mode 1.

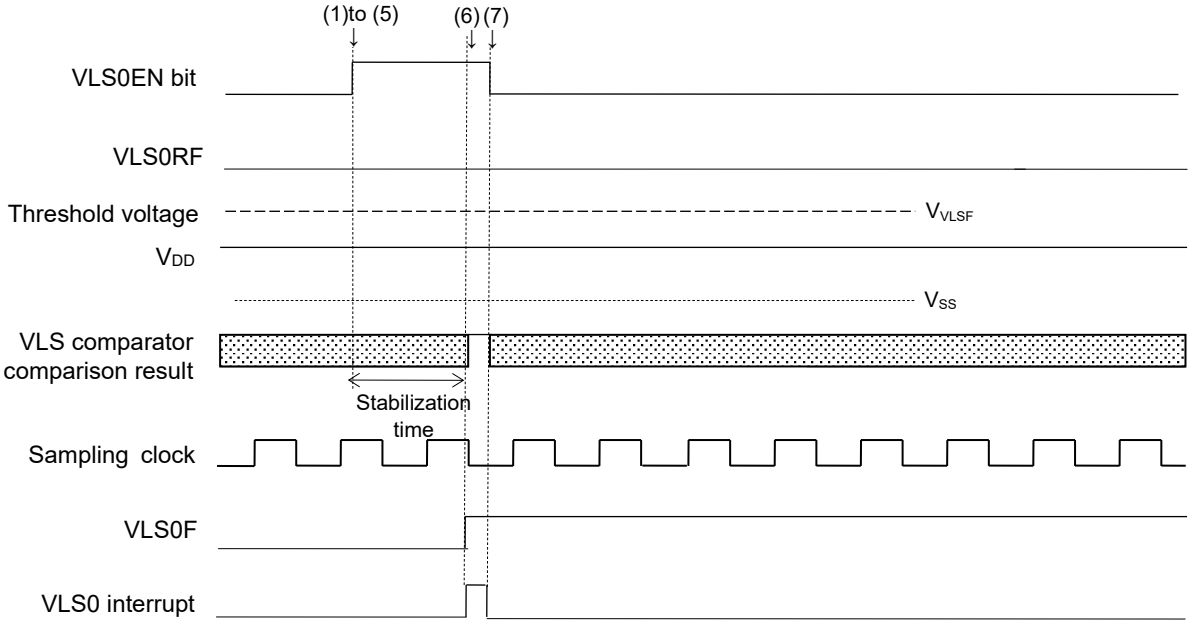


Figure 22-8 Operation Timing Chart without Sampling (Single Mode 1)

The operation shown in Figure 22-8 is described below:

(1) Select a detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "No sampling" by the VLS0SM1 bit of the VLS0SMP register.
(3) Write "0x0" to VLS0AMD1 and VLS0AMD0 bits of VLS0MOD register in order to select the single mode 1.
(4) Enable the VLS interrupt by VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register.
(5) Write "1" to the VLS0EN bit to enable VLS operation.
(6) If V_{DD} is below the threshold voltage (V_{VLSF}) when the comparison result of the VLS comparator is stabilized (*1), the VLS0F bit is set to "1" and the VLS0 interrupt (detection complete) is generated. The VLS0 interrupt (detection complete) is generated regardless of the detection result of V_{DD}.
(7) After the interrupt is generated, the VLS0EN bit is cleared to "0" and VLS operation is disabled.
(8) Read the VLS0F bit to confirm the detection result.

*1: Stabilization time: Approximately 300 μs (approx. 300 μs + sampling clock cycle x 3 when sampling is enabled)

Figure 22-9 shows an example of the operation timing chart with sampling in single mode 1.

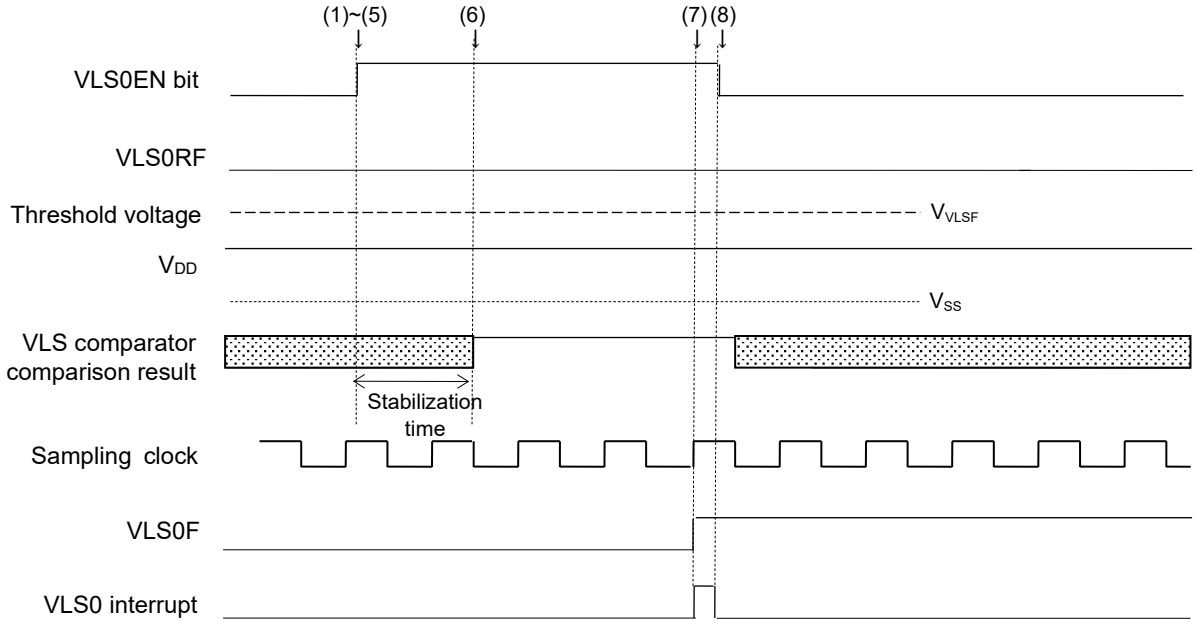


Figure 22-9 Operation Timing Chart with Sampling (Single Mode 1)

The operation shown in Figure 22-9 is described below:

(1) Select a detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "Sampling with LSCLK0" by the VLS0SM1 bit of the VLS0SMP register. And specify sampling clock dividing ratio by the VLS0DIV1 to VLS0DIV0 bits of the VLS0SMP register.
(3) Write "0x0" to VLS0AMD1 and VLS0AMD0 bits of VLS0MOD register in order to select the single mode 1.
(4) Enable the VLS interrupt by VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register.
(5) Write "1" to the VLS0EN bit to enable VLS operation.
(6) Wait until the comparison result of the VLS comparator is stabilized (approx. 300 μs).
(7) If V_{DD} is below the threshold voltage (V_{VLSF}) after three cycles of the sampling clock, the VLS0F bit is set to "1" and the VLS0 interrupt (detection complete) is generated. The VLS0 interrupt (detection complete) is generated regardless of the detection result of V_{DD}.
(8) After the interrupt is generated, the VLS0EN bit is cleared to "0" and VLS operation is disabled.
(9) Read the VLS0F bit to confirm the detection result.

[Note]

- **Entering the STOP/STOP-D mode is not allowed while the single mode operation is in progress. Enter the STOP/STOP-D mode after the single mode operation is completed (VLS0EN bit="0").**

22.3.2.2 Single mode 2

The single mode 2 generates the interrupt when the V_{DD} is lower than the threshold voltage.
Figure 22-10 shows an example of the operation timing chart without sampling in single mode 2.

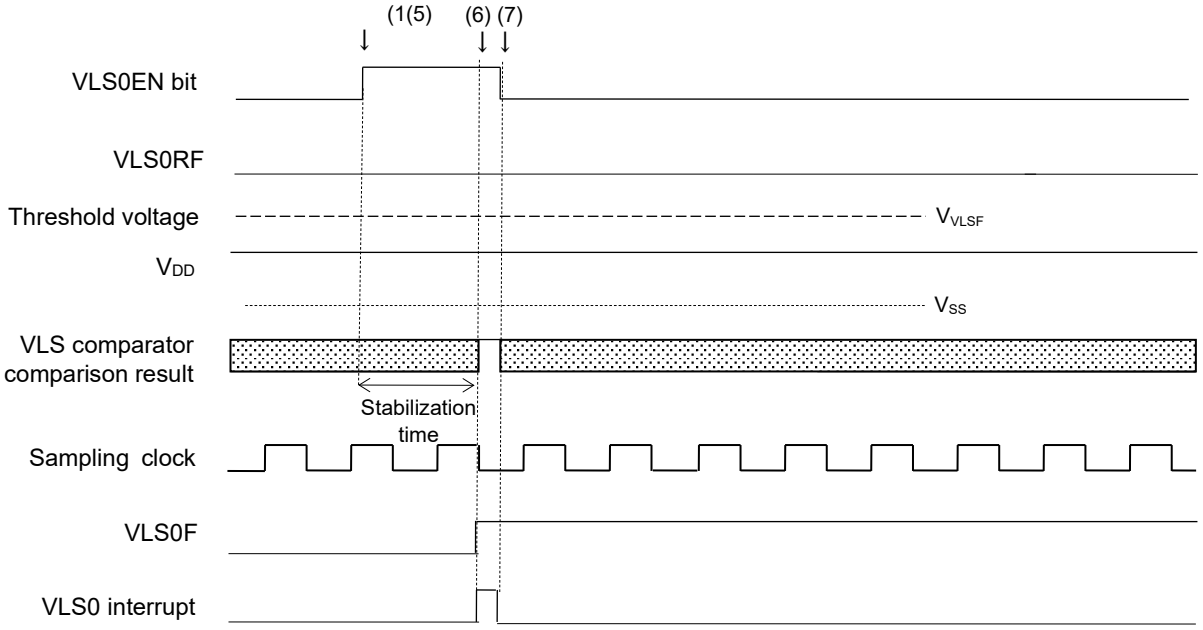


Figure 22-10 Operation Timing Chart without Sampling (Single Mode 2)

The operation shown in Figure 22-10 is described below:

(1) Select a detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "No sampling" by the VLS0SM1 bit of the VLS0SMP register.
(3) Write "0x1" to VLS0AMD1 and VLS0AMD0 bits of VLS0MOD register in order to select the single mode 2.
(4) Enable the VLS0 interrupt by VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register.
(5) Write "1" to the VLS0EN bit to enable VLS.
(6) If V_{DD} is below the specified threshold voltage (V_{VLSF}) when the comparison result of the VLS comparator is stabilized, voltage level supervisor flag (VLS0F) is set to "1" and the VLS0 interrupt (low voltage) is generated. If V_{DD} is higher than the specified threshold voltage (V_{VLSF}), the VLS0F bit is cleared to "0" and the VLS0 interrupt (low voltage) is not generated.
(7) The VLS0EN bit is set to "0" and VLS is disabled regardless of whether the VLS0 interrupt occurs or not.

Figure 22-11 shows an example of the operation timing chart with sampling in single mode 2.

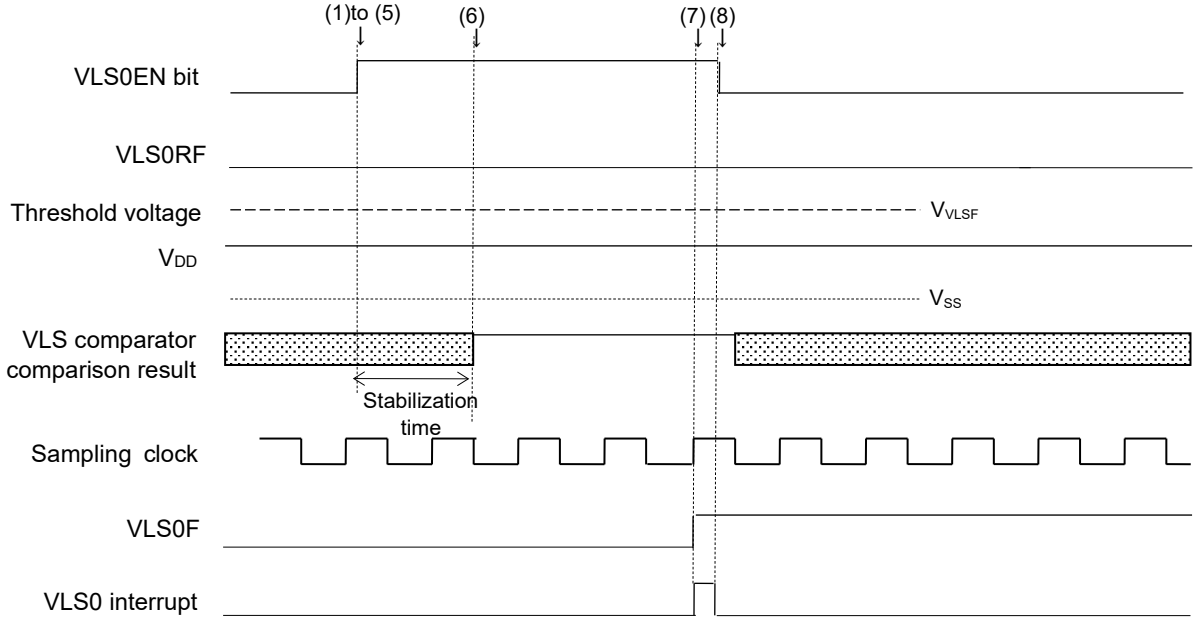


Figure 22-11 Operation Timing Chart with Sampling (Single Mode 2)

The operation shown in Figure 22-11 is described below:

(1) Select a detection voltage by the VLS0LV3 to VLS0LV0 bits of the VLS0LV register.
(2) Select "Sampling with LSCLK" by the VLS0SM1 bit of the VLS0SMP register. And specify sampling clock dividing ratio by the VLS0DIV1 to VLS0DIV0 bits of the VLS0SMP register.
(3) Write "0x1" to VLS0AMD1 and VLS0AMD0 bits of VLS0MOD register in order to select the single mode 2.
(4) Enable the VLS0 interrupt by VLS0SEL1 and VLS0SEL0 bits of the VLS0MOD register in order to.
(5) Write "1" to the VLS0EN bit to enable VLS operation.
(6) Wait until the comparison result of the VLS comparator is stabilized (approx. 300 μs).
(7) If V_{DD} is below the threshold voltage (V_{VLSF}) after three cycles of the sampling clock, the VLS0F bit is set to "1" and the VLS0 interrupt (low voltage) is generated. If V_{DD} is equal to or above the threshold voltage (V_{VLSF}), the VLS0F bit is cleared to "0" and the VLS0 interrupt (low voltage) is not generated.
(8) The VLS0EN bit is set to "0" and VLS is disabled regardless of whether the VLS0 interrupt occurs or not.

[Note]

- **Entering the STOP/STOP-D mode is not allowed while the single mode operation is in progress. Enter the STOP/STOP-D mode after the single mode operation is completed (VLS0EN bit="0").**
- **If V_{DD} is higher than the specified threshold voltage, the VLS0 interrupt is not generated.**

Chapter 23 Successive Approximation Type A/D Converter

23. Successive Approximation Type A/D Converter

23.1 General Description

ML62Q2700 group has the Successive Approximation type A/D Converter (SA-ADC), converts an analog input level to a digital value.
The number of A/D Converter channels is dependent of the product specification.
Table 23-1 shows the number of channels.

Table 23-1 Number of A/D Converter channels

Channel no.(n)	ML62Q2700 group				
	48pin product	52pin product	64pin product	80pin product	100pin product
0	●	●	●	●	●
1	●	●	●	●	●
2	●	●	●	●	●
3	●	●	●	●	●
4	●	●	●	●	●
5	●	●	●	●	●
6	●	●	●	●	●
7	●	●	●	●	●
8	●	●	●	●	●
9	●	●	●	●	●
10	●	●	●	●	●
11	●	●	●	●	●
12	-	-	-	●	●
13	-	-	-	●	●
14	-	-	-	●	●
15	-	-	-	●	●

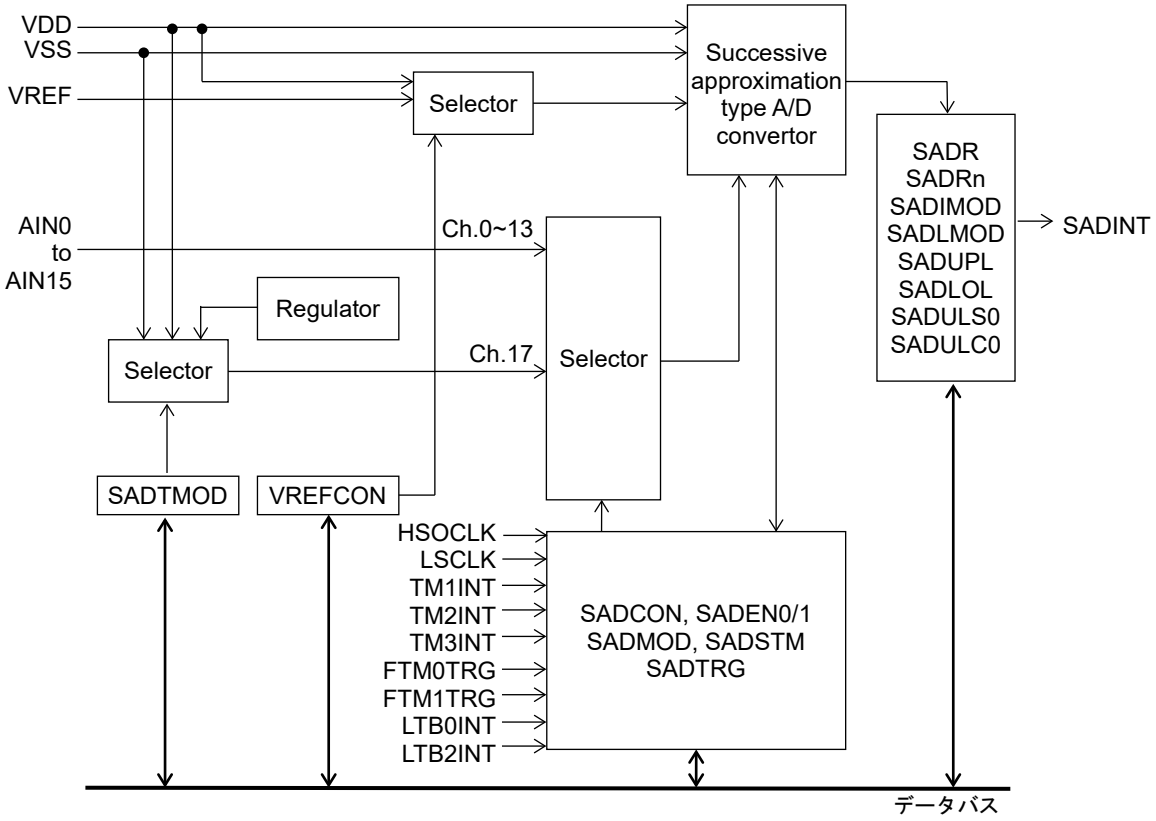
●: available -: Not available

23.1.1 Features

- Resolution : 12bit
- Conversion time : Min. 1.375μs/channel (at conversion clock is 16MHz)
- Number of input channel : Max. 16 channel
- Selectable Reference voltage: Input voltage from the VDD pin or External reference voltage (VREF pin)
- Configurable sample time
- Consecutive scan conversion function for specified channels
- Consecutive scan conversion with a specific interval time
- Configurable interval time between after consecutive scan conversion and the start of the next consecutive scan conversion
- Dedicated register for each channel to store the conversion result
- Interrupt request based on upper and lower limits of conversion results
- A/D converter self test function (full scale, zero scale, A/D conversion of internal reference voltage)
- Following triggers is selectable to start the A/D conversion
  - 16-bit Timer interrupt request (TM1INT, TM2INT, TM3INT)
  - Functional Timer trigger (FTM0TRG, FTM1TRG)
  - Low-speed Time Base Counter interrupt (LTB0INT, LTB2INT)

23.1.2 Configuration

Figure 23-1 shows the configuration of SA-ADC.



SADCON	: SA-ADC control register
SADEN0/1	: SA-ADC enable register 0, 1
SADMOD	: SA-ADC mode register
SADSTM	: SA-ADC conversion interval register
SADR	: SA-ADC result register
SADRn	: SA-ADC result register n (n=0 to 13)
SADIMOD	: SA-ADC interrupt mode register
SADLMOD	: SA-ADC upper/lower limit mode register
SADUPL	: SA-ADC upper limit setting register
SADLOL	: SA-ADC lower limit setting register
SADULS0	: SA-ADC upper/lower limit status register 0
SADULC0	: SA-ADC upper/lower limit status clear register 0
VREFCON	: Reference voltage control register
SADTRG	: SA-ADC trigger register
SADTMOD	: SA-ADC test mode register
SADINT	: SA-ADC interrupt request
TM1INT,TM2INT,TM3INT	: 16-bit timer 1,2,3 interrupt
FTM0TRG,FTM1TRG	: Functional timer 0, 1 trigger
LTB0INT	: Low speed time base counter 0 interrupt
LTB2INT	: Low speed time base counter 2 interrupt

Figure 23-1 Configuration of successive approximation type A/D Converter

23.1.3 List of Pins

The I/O pins of the Successive Approximation type A/D converter are assigned to the shared function of the general ports.

Pin name	I/O	Description
VDD	-	Positive power supply for SA-ADC
VSS	-	Negative power supply for SA-ADC
VREF	-	Reference power supply for SA-ADC
AIN0	I	SA-ADC channel 0 analog input
AIN1	I	SA-ADC channel 1 analog input
AIN2	I	SA-ADC channel 2 analog input
AIN3	I	SA-ADC channel 3 analog input
AIN4	I	SA-ADC channel 4 analog input
AIN5	I	SA-ADC channel 5 analog input
AIN6	I	SA-ADC channel 6 analog input
AIN7	I	SA-ADC channel 7 analog input
AIN8	I	SA-ADC channel 8 analog input
AIN9	I	SA-ADC channel 9 analog input
AIN10	I	SA-ADC channel 10 analog input
AIN11	I	SA-ADC channel 11 analog input
AIN12	I	SA-ADC channel 12 analog input
AIN13	I	SA-ADC channel 13 analog input
AIN14	I	SA-ADC channel 14 analog input
AIN15	I	SA-ADC channel 15 analog input

Table 23-2 shows the list of the general ports used for the A/D Converter and the register settings of the ports.

Table 23-2 Ports used in the A/D Converter and the register settings

Channel no.	Pin name	Shared port		Setting Register	Setting value	ML62Q2700 group
0	AIN0	P17	Primary Func.	P1MOD7	0000_0000	●
1	AIN1	P20	Primary Func.	P2MOD0	0000_0000	●
2	AIN2	P21	Primary Func.	P2MOD1	0000_0000	●
3	AIN3	P22	Primary Func.	P2MOD2	0000_0000	●
4	AIN4	P24	Primary Func.	P2MOD4	0000_0000	●
5	AIN5	P25	Primary Func.	P2MOD5	0000_0000	●
6	AIN6	P26	Primary Func.	P2MOD6	0000_0000	●
7	AIN7	P27	Primary Func.	P2MOD7	0000_0000	●
8	AIN8	P65	Primary Func.	P6MOD5	0000_0000	●
9	AIN9	P66	Primary Func.	P6MOD6	0000_0000	●
10	AIN10	P43	Primary Func.	P4MOD3	0000_0000	●
11	AIN11	P03	Primary Func.	P0MOD3	0000_0000	●
12	AIN12	P56	Primary Func.	P5MOD6	0000_0000	●
13	AIN13	P57	Primary Func.	P5MOD7	0000_0000	●
14	AIN14	PA3	Primary Func.	PAMOD3	0000_0000	●
15	AIN15	PA4	Primary Func.	PAMOD4	0000_0000	●
16	VREF	P23	Primary Func.	P2MOD3	0000_0000	●

[Note]

- **When using the SA-ADC, set PnmIE bit and PnmOE bit of port n mode register 01/23/45/67 (n: port number 1, 2, 3, 7, n: bit number 0 to 7) to "0" as "Disable input" and "Disable output", otherwise a shoot-through current may flow.**
- **Noise influence to the conversion accuracy can be reduced by following ways.**
  - **Not switch other pins that are not used for conversion during A/D conversion**
  - **Execute A/D conversion while HALT mode.**

23.2 Description of Registers

23.2.1 List of Registers

Registers for unequipped channels are not available to use. They return 0x0000 for reading.

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF800	SA-ADC mode register	SADMODL	SADMOD	R/W	8/16	0x00
0xF801		SADMODH		R/W	8	0x00
0xF802	SA-ADC control register	SADCONL	SADCON	R/W	8/16	0x00
0xF803		SADCONH		R/W	8	0x00
0xF804	SA-ADC conversion interval register	SADSTML	SADSTM	R/W	8/16	0x00
0xF805		SADSTMH		R/W	8	0x00
0xF806	Reference voltage control register	VREFCON	-	R/W	8	0x00
0xF807	Reserved register	-	-	-	-	-
0xF808	SA-ADC interrupt mode register	SADIMOD	-	R/W	8	0x00
0xF809	Reserved register	-	-	-	-	-
0xF80A	SA-ADC trigger register	SADTRG	-	R/W	8	0x00
0xF80B	Reserved register	-	-	-	-	-
0xF80C	SA-ADC enable register 0	SADEN0L	SADEN0	R/W	8/16	0x00
0xF80D		SADEN0H		R/W	8	0x00
0xF80E	SA-ADC enable register 1	SADEN1L	SADEN1	R/W	8/16	0x00
0xF80F		SADEN1H		R/W	8	0x00
0xF810 to 0xF81F	Reserved registers	-	-	-	-	-
0xF820	SA-ADC upper/lower limit mode register	SADLMODL	SADLMOD	R/W	8/16	0x00
0xF821		SADLMODH		R/W	8	0x00
0xF822	SA-ADC upper limit setting register	SADUPLL	SADUPL	R/W	8/16	0xF0
0xF823		SADUPLH		R/W	8	0xFF
0xF824	SA-ADC lower limit setting register	SADLOLL	SADLOL	R/W	8/16	0x00
0xF825		SADLOLH		R/W	8	0x00
0xF826	SA-ADC upper/lower limit status register 0	SADULS0L	SADULS0	R	8/16	0x00
0xF827		SADULS0H		R	8	0x00
0xF828	Reserved registers	-	-	-	-	-
0xF829						
0xF82A	SA-ADC upper/lower limit status clear register 0	SADULC0L	SADULC0	W	8/16	0x00
0xF82B		SADULC0H		W	8	0x00
0xF82C to 0xF82F	Reserved registers	-	-	-	-	-
0xF830	SA-ADC test mode register	SADTMOD	-	R/W	8	0x00
0xF831 to 0xF83D	Reserved registers	-	-	-	-	-
0xF83E	SA-ADC result register	SADRL	SADR	R	8/16	0x00
0xF83F		SADRH		R	8	0x00
0xF840	SA-ADC result register 0	SADR0L	SADR0	R	8/16	0x00
0xF841		SADR0H		R	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF842	SA-ADC result register 1	SADR1L	SADR1	R	8/16	0x00
0xF843		SADR1H		R	8	0x00
0xF844	SA-ADC result register 2	SADR2L	SADR2	R	8/16	0x00
0xF845		SADR2H		R	8	0x00
0xF846	SA-ADC result register 3	SADR3L	SADR3	R	8/16	0x00
0xF847		SADR3H		R	8	0x00
0xF848	SA-ADC result register 4	SADR4L	SADR4	R	8/16	0x00
0xF849		SADR4H		R	8	0x00
0xF84A	SA-ADC result register 5	SADR5L	SADR5	R	8/16	0x00
0xF84B		SADR5H		R	8	0x00
0xF84C	SA-ADC result register 6	SADR6L	SADR6	R	8/16	0x00
0xF84D		SADR6H		R	8	0x00
0xF84E	SA-ADC result register 7	SADR7L	SADR7	R	8/16	0x00
0xF84F		SADR7H		R	8	0x00
0xF850	SA-ADC result register 8	SADR8L	SADR8	R	8/16	0x00
0xF851		SADR8H		R	8	0x00
0xF852	SA-ADC result register 9	SADR9L	SADR9	R	8/16	0x00
0xF853		SADR9H		R	8	0x00
0xF854	SA-ADC result register 10	SADR10L	SADR10	R	8/16	0x00
0xF855		SADR10H		R	8	0x00
0xF856	SA-ADC result register 11	SADR11L	SADR11	R	8/16	0x00
0xF857		SADR11H		R	8	0x00
0xF858	SA-ADC result register 12	SADR12L	SADR12	R	8/16	0x00
0xF859		SADR12H		R	8	0x00
0xF85A	SA-ADC result register 13	SADR13L	SADR13	R	8/16	0x00
0xF85B		SADR13H		R	8	0x00
0xF85C	SA-ADC result register 14	SADR14L	SADR14	R	8/16	0x00
0xF85D		SADR14H		R	8	0x00
0xF85E	SA-ADC result register 15	SADR15L	SADR15	R	8/16	0x00
0xF85F		SADR15H		R	8	0x00

23.2.2 SA-ADC Mode Register (SADMOD)

SADMOD is a SFR to set the operation mode and operating clock frequency for SA-ADC.

Address : 0xF800 (SADMODL/SADMOD), 0xF801 (SADMODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADMOD															
Byte	SADMODH								SADMODL							
Bit	SAINITT3	SAINITT2	SAINITT1	SAINITT0	SAINIT	-	-	SASHT4	SASHT3	SASHT2	SASHT1	SASHT0	SACK2	SACK1	SACK0	SALP
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 12	SAINITT3 to SAINITT0	Configure the SA-ADC amplifier stability time at A/D conversion starting. Wait time for stability [s] = setting value / SAD_CLK frequency Set the time to equal or more than 0.5[µs] When SAINIT="1", it is included discharge time for sample hold capacitor. In this case, set the time to equal or more than 0.65[µs]. Configure the appropriate clock count considering the external circuit impedance connecting to the analog input pin. Table 23-3 shows example for typical setting.
11	SAINIT	Select whether to start A/D conversion after discharging the charge of the previous A/D conversion charged to the sample hold capacitance, or to start the A/D conversion without discharging. 0: Without discharging (Initial value) 1: With discharging
10 to 9	-	Reserved bits
8 to 4	SASHT4 to SASHT0	Set the sampling time. sampling time [s] = (setting value + 1) / SAD_CLK frequency Set the time to equal or more than 3. Set the setting value to equal or more than 0.5[µs] at V_{REF}≥2.7V, 24[µs] at V_{REF}≥1.8V Configure the appropriate clock count considering the external circuit impedance connecting to the analog input pin. Table 23-4 shows example for typical setting.
3 to 1	SACK2 to SACK0	Select the frequency of the A/D conversion operating clock (SAD_CLK). The SAD_CLK frequency should be equal or lower 16 MHz. 000: 1/1 x HSOCLK (Initial value) 001: 1/2 x HSOCLK 010: 1/4 x HSOCLK 011: 1/8 x HSOCLK 100: 1/16 x HSOCLK 101: Do not use 110: Do not use 111: 1/1 x LSCLK0 A/D conversion time excluding discharge/amp stability time is calculated by the following formula. A/D conversion time [s] = (SASHT4 to SASHT0 value + 15) / SAD_CLK frequency
0	SALP	Select whether the A/D conversion of each channel is Single A/D conversion or Consecutive scan A/D conversion. The conversion interval time in the consecutive scan A/D conversion mode is specified in the SADSTM register. 0: Single A/D conversion (Initial value) 1: Consecutive scan A/D conversion

Table 23-3 Example for SAINITT3 to 0 setting

SAD_CLK	SAINITT3 to 0 SAINIT=1 (Discharge time/Amp. stability) > 0.65µs	SAINITT3 to 0 SAINIT=0 (Amp. stability) > 0.5µs
16 MHz	1010	1000
12 MHz	1000	0110
8 MHz	0101	0100
6 MHz	0100	0011
4 MHz	0011	0010
< 4 MHz	0010	0010

Table 23-4 Example for SASHT4 to 0 setting

SAD_CLK	SASHT4 to 0 (Sampling time)		
	V_{REF} ≥ 1.8V	V_{REF} ≥ 2.4V	V_{REF} ≥ 2.7V
~ 16 MHz	-	-	00111
~ 8 MHz	-	00011	00011
1 MHz	10011	00011	00011
32.768 kHz	00011	00011	00011

23.2.3 SA-ADC Control Register (SADCON)

SADCON is a SFR to control the operation of the A/D converter.

Address : 0xF802 (SADCONL/SADCON), 0xF803 (SADCONH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADCON															
Byte	SADCONH								SADCONL							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SATGEN	SARUN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 2	-	Reserved bits
1	SATGEN	Enable starting the A/D conversion by the trigger events. 0: Disable the trigger operation (Initial value) 1: Enable the trigger operation
0	SARUN	Start or stop the A/D conversion. Write "1" to this bit to start the A/D conversion, and "0" to stop it. When "0" is written to SALP bit and the A/D conversion on the largest number of channel is ended, this SARUN bit is automatically reset to "0". When "1" is written to SALP, the A/D conversion repeats until the SARUN bit is reset to "0" by the software. 0: Stop the A/D conversion (Initial value) 1: Start the A/D conversion

[Note]

- **Start the A/D conversion with one or more channels selected by the SA-ADC enable registers (SADEN0 and SADEN1). If no channel is selected, the operation does not start.**
- **When switching to STOP/STOP-D mode, wait until SARUN bit becomes "0". When SARUN bit is "1", the transition to STOP/STOP-D mode cannot be entered.**
- **When SACK2 to 0 bits are set to 0x7, it takes up to 3 clocks of the low-speed clock (LSCLK0) from writing to SARUN to the start or stop operation.**

23.2.4 SA-ADC Conversion Interval Register (SADSTM)

SADSTM is a SFR to set the interval time in the consecutive scan A/D conversion mode.
The interval time is determined by the following formula.

A/D conversion interval time = SAD_CLK cycle X SADSTM setting value

In case A/D conversion of channel 2 and channel 5, the conversion interval is the time after consecutive A/D conversion of channels 2 and 5 until the next A/D conversion of channel 2 is started.
The next A/D conversion starts at the timing that the value set in this register has been counted with SAD_CLK.

Address : 0xF804 (SADSTML/SADSTM), 0xF805 (SADSTMH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADSTM															
Byte	SADSTMH								SADSTML							
Bit	SADSTM15	SADSTM14	SADSTM13	SADSTM12	SADSTM11	SADSTM10	SADSTM9	SADSTM8	SADSTM7	SADSTM6	SADSTM5	SADSTM4	SADSTM3	SADSTM2	SADSTM1	SADSTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23.2.5 Reference Voltage Control Register (VREFCON)

VREFCON is a SFR to select reference voltage for the SA-ADC.

Address : 0xF806 (VREFCON)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VREFCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	VREFP0	-	-	-	rsvd
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 5	-	Reserved bits
4	VREFP0	Select the reference voltage source for the A/D conversion. 0: VDD pin (Initial value) 1: VREF pin
3 to 1	-	Reserved bits
0	rsvd	Reserved bit. Always set “0”

23.2.6 SA-ADC Interrupt Mode Register (SADIMOD)

SADIMOD is a SFR to select the interrupt mode of the SA-ADC.

Address : 0xF808 (SADIMOD)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SADIMOD							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SADIMD1	SADIMD0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 2	-	Reserved bits
1	SADIMD1	Select the timing of the A/D converter interrupt request occurrence when the upper and lower limit determination function is used. 0: Request interrupt at a timing corresponding to SADIMD0 setting when the upper limit and lower limit determination function are used and the detection result coincides (initial value). 1: Request interrupt according to the SADIMD0 setting regardless of the detection result even when using the upper limit and lower limit determination function.
0	SADIMD0	Select the occurrence timing of SA-ADC interrupt request. 0: Request interrupt after all A/D conversions for the selected channel are complete (Initial value) 1: Request an interrupt at the end of the A/D conversion for each channel

23.2.7 SA-ADC Trigger Register (SADTRG)

SADTRG is a SFR used to control the trigger event for the SA-ADC.

Address : 0xF80A (SADTRG)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SADTRG							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	SASTS3	SASTS2	SASTS1	SASTS0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 4	-	Reserved bits
3 to 0	SASTS3 to SASTS0	Select the source of the trigger event to start SA-ADC. 0000: 16-bit Timer 1 interrupt (TM1INT) (Initial value) 0001: 16-bit Timer 2 interrupt (TM2INT) 0010: 16-bit Timer 3 interrupt (TM3INT) 0011: Do not use (Reserved) 0100: Functional Timer 0 trigger (FTM0TRG) 0101: Functional Timer 1 trigger (FTM1TRG) 0110: Do not use (Reserved) 0111: Do not use (Reserved) 1000: Time Base Counter 0 interrupt (LTB0INT) 1001: Time Base Counter 2 interrupt (LTB2INT) 1110 to 1111: Do not use (Reserved)

23.2.8 SA-ADC Enable Register 0 (SADEN0)

SADEN0 is a SFR to select channels to be converted of the A/D converter.

Address : 0xF80C (SADEN0L/SADEN0), 0xF80D (SADEN0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADEN0															
Byte	SADEN0H								SADEN0L							
Bit	SACH 15	SACH 14	SACH 13	SACH 12	SACH 11	SACH 10	SACH 09	SACH 08	SACH 07	SACH 06	SACH 05	SACH 04	SACH 03	SACH 02	SACH 01	SACH 00
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
This bit is used to control enable/disable the conversion on a target channel.
0: Disabled (Initial value)
1: Enabled

When multiple bits of SACHn (n=00 to 17) are set to "1", the A/D conversion starts in the order of smaller channel number.

Bit No.	Bit symbol name	Description (target channel)
15	SACH15	Channel 15
14	SACH14	Channel 14
13	SACH13	Channel 13
12	SACH12	Channel 12
11	SACH11	Channel 11
10	SACH10	Channel 10
9	SACH09	Channel 9
8	SACH08	Channel 8
7	SACH07	Channel 7
6	SACH06	Channel 6
5	SACH05	Channel 5
4	SACH04	Channel 4
3	SACH03	Channel 3
2	SACH02	Channel 2
1	SACH01	Channel 1
0	SACH00	Channel 0

[Note]
- **Do not start the A/D conversion when the all bits of SACHn (n=00 to 17) set to "0". When A/D conversion is started in this state, the SARUN bit of the SADCON register does not become "1".**

23.2.9 SA-ADC Enable Register 1 (SADEN1)

SADEN1 is a SFR to select channels to be converted of the A/D converter .

Address : 0xF80E (SADEN1L/SADEN1), 0xF80F (SADEN1H)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADEN1															
Byte	SADEN1H								SADEN1L							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SACH 17	-
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description (target channel)
15 to 2	-	Reserved bits
1	SACH17	Control enable/disable the conversion on channel 17; A/D converter test. 0: Disable the conversion on channel 17 (initial value) 1: Enable the conversion on channel 17
0	-	Reserved bit

[Note]

- **Do not start the A/D conversion when the all bits of SACHn (n=00 to 17) are "0". When A/D conversion is started in this state, the SARUN bit of the SADCON register does not become "1".**

23.2.10 SA-ADC Upper/Lower Limit Mode Register (SADLMOD)

SADLMOD is a SFR to set modes in the A/D conversion result upper/lower limit detection function.

Address : 0xF820 (SADLMODL/SADLMOD), 0xF821 (SADLMODH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADLMOD															
Byte	SADLMODH								SADLMODL							
Bit	-	-	-	-	-	-	SALMD1	SALMD0	-	-	-	-	-	-	-	SALEN
R/W	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 10	-	Reserved bits
9, 8	SALMD1, SALMD0	Set a condition of the A/D conversion result upper/lower limit detection. If the A/D conversion result matches the conditions, the corresponding channel in the SA-ADC upper limit lower limit status register 0 (SADULS0) is set to "1", and an interrupt request is occurred according to the setting of the SA-ADC interrupt mode register (SADIMOD). 00: SADLOL value ≤ A/D conversion value ≤ SADUPL value (Initial value) 01: A/D conversion value > SADUPL value 10: A/D conversion value < SADLOL value 11: A/D conversion value > SADUPL or A/D conversion value < SADLOL value
7 to 1	-	Reserved bits
0	SALEN	Selects whether to use the upper and lower limit determination functions of A/D conversion. When SALEN is "0", the SA-ADC upper limit lower limit status register 0 (SADULS0) is not updated. 0: No use the upper and lower limit determination functions of A/D conversion (initial value) 1: Use the upper and lower limit determination functions

23.2.11 SA-ADC Upper Limit Setting Register (SADUPL)

SADUPL is a SFR to set the upper limit value among the conditions for the upper and lower limit determination functions of A/D conversion.

Address : 0xF822 (SADUPLL/SADUPL), 0xF823 (SADUPLH)
Access : R/W
Access size : 8/16 bit
Initial value : 0xFFF0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADUPL															
Byte	SADUPLH								SADUPLL							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0

23.2.12 SA-ADC Lower Limit Setting Register (SADLOL)

SADLOL is a SFR to set the lower limit value among the conditions for the upper and lower limit determination functions of A/D conversion.

Address : 0xF824 (SADLOLL/SADLOL), 0xF825 (SADLOLH)
Access : R/W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADLOL															
Byte	SADLOLH								SADLOLL							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23.2.13 SA-ADC Upper/Lower Limit Status Register 0 (SADULS0)

SADULS0 is a read-only SFR to indicate whether the A/D conversion result matches to the condition of upper/lower limit.

Address : 0xF826 (SADULS0L/SADULS0), 0xF827 (SADULS0H)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADULS0															
Byte	SADULS0H								SADULS0L							
Bit	SAULS15	SAULS14	SAULS13	SAULS12	SAULS11	SAULS10	SAULS09	SAULS08	SAULS07	SAULS06	SAULS05	SAULS04	SAULS03	SAULS02	SAULS01	SAULS00
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
Indicate the upper and lower limit judgment results of A/D conversion for the corresponding channel.
0: Unmatched to the condition of upper/lower limit (SALMD1 to 0). (Initial value)
1: Matched to the condition of upper/lower limit (SALMD1 to 0).
The corresponding bit remains "1" until the corresponding bit is cleared in the SADULC0 register or the LSI is reset.
When all channels that enable conversion are completed with SALEN=1, an interrupt request is occurred according to the setting of the SA-ADC interrupt mode register (SADIMOD) when any bit of the register SADULS0 is "1" when the conversion of all channels that are enabled to be converted is completed.
Refer to Figure 23-9 to 23-11 for the timing of the interrupt and updates of detection result.

Bit No.	Bit symbol name	Description (target channel)
15	SAULS15	Channel 15 (AIN15)
14	SAULS14	Channel 14 (AIN14)
13	SAULS13	Channel 13 (AIN13)
12	SAULS12	Channel 12 (AIN12)
11	SAULS11	Channel 11 (AIN11)
10	SAULS10	Channel 10 (AIN10)
9	SAULS09	Channel 9 (AIN9)
8	SAULS08	Channel 8 (AIN8)
7	SAULS07	Channel 7 (AIN7)
6	SAULS06	Channel 6 (AIN6)
5	SAULS05	Channel 5 (AIN5)
4	SAULS04	Channel 4 (AIN4)
3	SAULS03	Channel 3 (AIN3)
2	SAULS02	Channel 2 (AIN2)
1	SAULS01	Channel 1 (AIN1)
0	SAULS00	Channel 0 (AIN0)

[Note]
- **When the upper and lower limit determination functions of A/D conversion are used (SALEN=1), the interrupt can be cleared by clearing the corresponding bits of SAULC15 to SAULC00 or resetting the LSI.**
- **When executing A/D conversion (SALP=0) only once, confirm that the corresponding bit of SAULS15 to SAULS00 is "0" before setting SARUN to "1".**
- **When executing continuous A/D conversion (SALP=1), confirm that the corresponding bit of SAULS15 to SAULS00 is "0" before the next A/D conversion ends.**

23.2.14 SA-ADC Upper/Lower Limit Status Clear Register 0 (SADULC0)

SADULC0 is a write-only SFR to clear the A/D conversion result matches to the condition of upper/lower limit.

Address : 0xF82A (SADULC0L/SADULC0), 0xF82B (SADULC0H)
Access : W
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADULC0															
Byte	SADULC0H								SADULC0L							
Bit	SAULC15	SAULC14	SAULC13	SAULC12	SAULC11	SAULC10	SAULC09	SAULC08	SAULC07	SAULC06	SAULC05	SAULC04	SAULC03	SAULC02	SAULC01	SAULC00
R/W	R	R	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
It is used to clear a target result of upper/lower limit detection.
Writing “0”: Invalid
Writing “1”: clear a target result

Bit No.	Bit symbol name	Description (target channel)
15	SAULC15	Channel 15 (AIN15)
14	SAULC14	Channel 14 (AIN14)
13	SAULC13	Channel 13 (AIN13)
12	SAULC12	Channel 12 (AIN12)
11	SAULC11	Channel 11 (AIN11)
10	SAULC10	Channel 10 (AIN10)
9	SAULC09	Channel 9 (AIN9)
8	SAULC08	Channel 8 (AIN8)
7	SAULC07	Channel 7 (AIN7)
6	SAULC06	Channel 6 (AIN6)
5	SAULC05	Channel 5 (AIN5)
4	SAULC04	Channel 4 (AIN4)
3	SAULC03	Channel 3 (AIN3)
2	SAULC02	Channel 2 (AIN2)
1	SAULC01	Channel 1 (AIN1)
0	SAULC00	Channel 0 (AIN0)

23.2.15 SA-ADC Result Register (SADR)

SADR is a read-only SFR to store the A/D conversion results on channels 0 to 15 and 17 (A/D converter test function). The A/D conversion result is overwritten in the SADR register for each channel A/D conversion.
In addition, the A/D conversion result of the A/D converter test function of channel 17 is stored only in the SADR register.

Symbol name	Channel
SADR	Latest conversion result of channels 0 to 15 and 17

Address : 0xF83E (SADRL/SADR), 0xF83F (SADRH)
Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADR															
Byte	SADRH								SADRL							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	-	-	-	-
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23.2.16 SA-ADC Result Register n (SADRn : n=0 to 15)

SADRn is a SFR to store the SA-ADC conversion results on channels 0 to 15.

Address : 0xF840 (SADR0L/SADR0), 0xF841 (SADR0H),
0xF842 (SADR1L/SADR1), 0xF843 (SADR1H),
0xF844 (SADR2L/SADR2), 0xF845 (SADR2H),
0xF846 (SADR3L/SADR3), 0xF847 (SADR3H),
0xF848 (SADR4L/SADR4), 0xF849 (SADR4H),
0xF84A (SADR5L/SADR5), 0xF84B (SADR5H),
0xF84C (SADR6L/SADR6), 0xF84D (SADR6H),
0xF84E (SADR7L/SADR7), 0xF84F (SADR7H),
0xF850 (SADR8L/SADR8), 0xF851 (SADR8H),
0xF852 (SADR9L/SADR9), 0xF853 (SADR9H),
0xF854 (SADR10L/SADR10), 0xF855 (SADR10H),
0xF856 (SADR11L/SADR11), 0xF857 (SADR11H),
0xF858 (SADR12L/SADR12), 0xF859 (SADR12H),
0xF85A (SADR13L/SADR13), 0xF85B (SADR13H),
0xF85C (SADR14L/SADR14), 0xF85B (SADR14H),
0xF85E (SADR15L/SADR15), 0xF85B (SADR15H),

Access : R
Access size : 8/16 bit
Initial value : 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SADRn															
Byte	SADRnH								SADRnL							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The A/D conversion result of each channel can be read from SADRn.

Symbol name	Channel
SADR0	Channel 0 (AIN0)
SADR1	Channel 1 (AIN1)
SADR2	Channel 2 (AIN2)
SADR3	Channel 3 (AIN3)
SADR4	Channel 4 (AIN4)
SADR5	Channel 5 (AIN5)
SADR6	Channel 6 (AIN6)
SADR7	Channel 7 (AIN7)
SADR8	Channel 8 (AIN8)
SADR9	Channel 9 (AIN9)
SADR10	Channel 10 (AIN10)
SADR11	Channel 11 (AIN11)
SADR12	Channel 12 (AIN12)
SADR13	Channel 13 (AIN13)
SADR14	Channel 14 (AIN14)
SADR15	Channel 15 (AIN15)

23.2.17 SA-ADC Test Mode Register (SADTMOD)

SADTMOD is a SFR to control the SA-ADC test function.

Address : 0xF830 (SADTMOD)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SADTMOD							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SADTM1	SADTM0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This function enables to check if SA-A/D converter and the analog switch is working properly by executing the A/D conversion for the full scale, zero scale and the internal reference voltage (approx. 1.0 V).
The A/D conversion result is stored in the SA-ADC result register (SADR).

Also, the AIN input level is measured by using a measurement value of internal reference voltage.
For example:
1: Convert at $V_{REF} = V_{DD}$, SACH17=1, SADTM1-0=3, where the result is “a”.
2: Convert at $V_{REF} = V_{DD}$, SACHn=1, where the result is “b”.
An input level from AINn is b/a [V] .

It is also feasible to set SACHn and SACH17 of AINn to 1 and measure continuously.
The results is readable from SADRn and SADR respectively.

Bit No.	Bit symbol name	Description
7 to 2	-	Reserved bits
1 to 0	SADTM1, SADTM0	Set the SA-A/D converter test function. It is select the input to channel 17. 00: No use the A/D converter test function (Initial value) 01: Full scale A/D conversion 10: Zero scale A/D conversion 11: Internal reference voltage (approx.1.0V) A/D conversion

23.3 Description of Operation

23.3.1 Operation of Successive Approximation Type A/D Converter

Figure 23-2 shows a setting example when one-time A/D conversion is performed using channel 1 and 0.

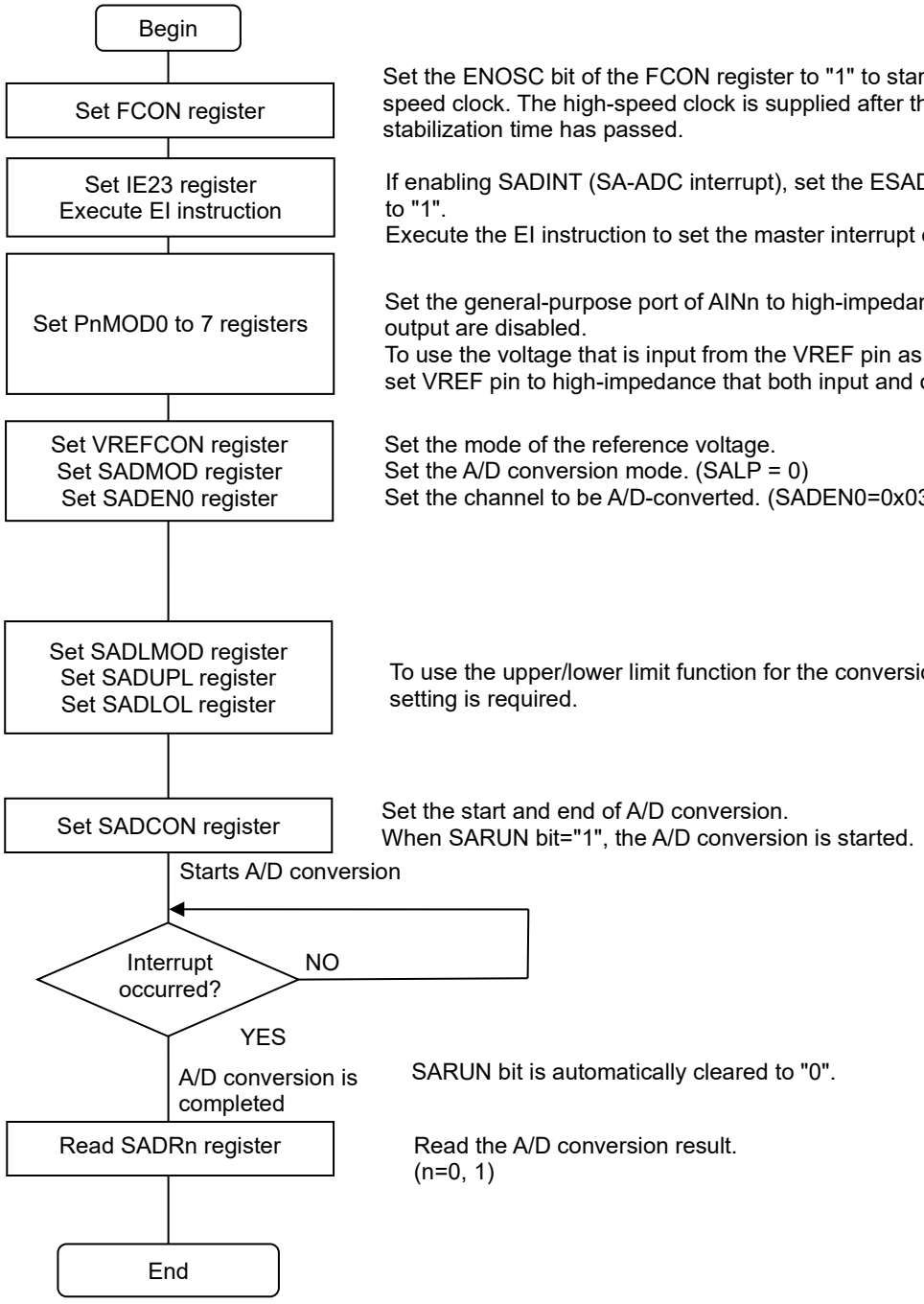


Figure 23-2 Example of A/D Conversion Setting

Figure 23-3 shows a setting example when one-time A/D conversion is performed in HALT mode using channel 1 and 0.

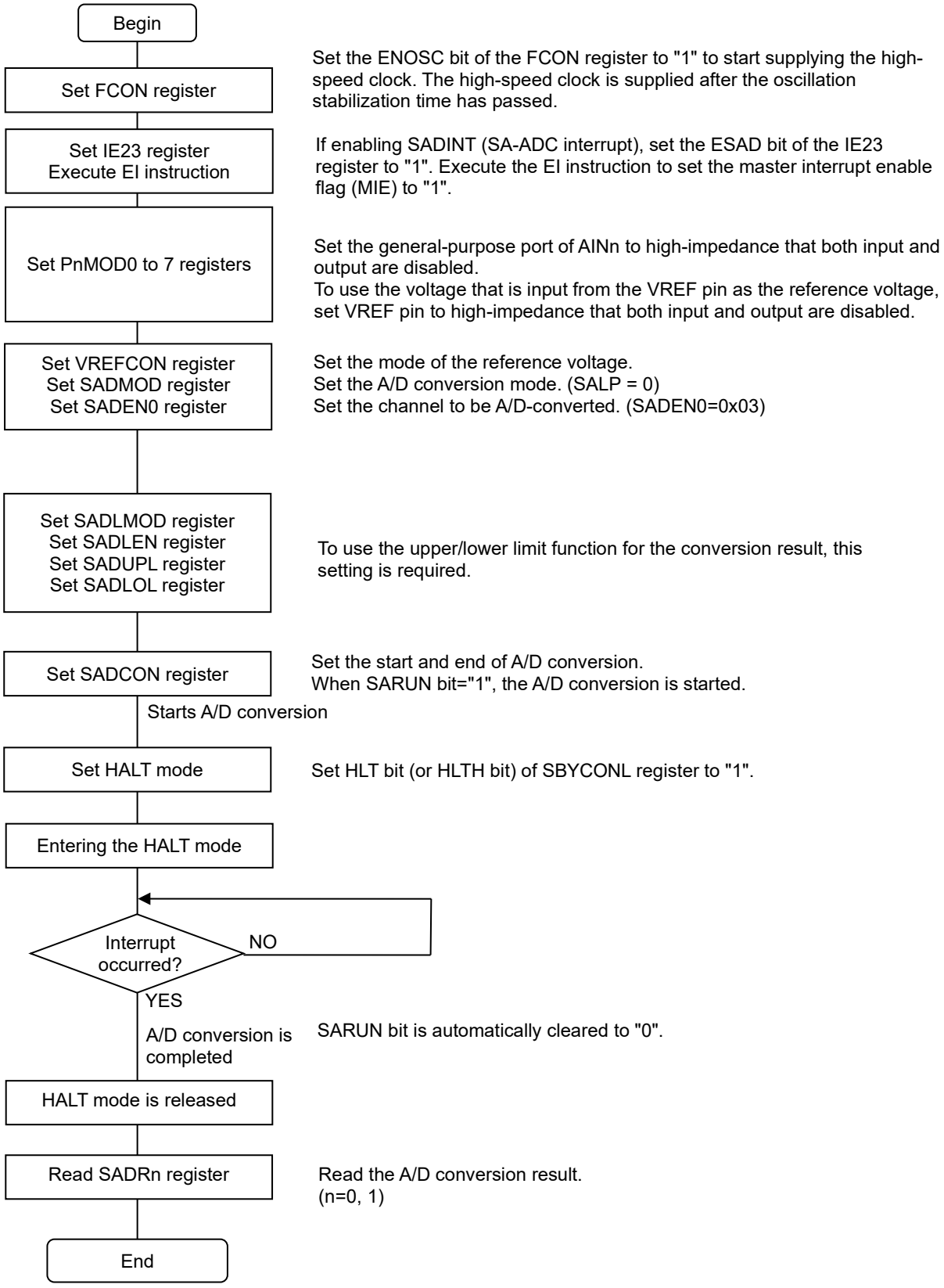


Figure 23-3 Example of A/D Conversion Setting (Converting in HALT mode)

Figure 23-4 shows a setting example when one-time A/D conversion is performed using channel 1 and 0 starting by a trigger event.

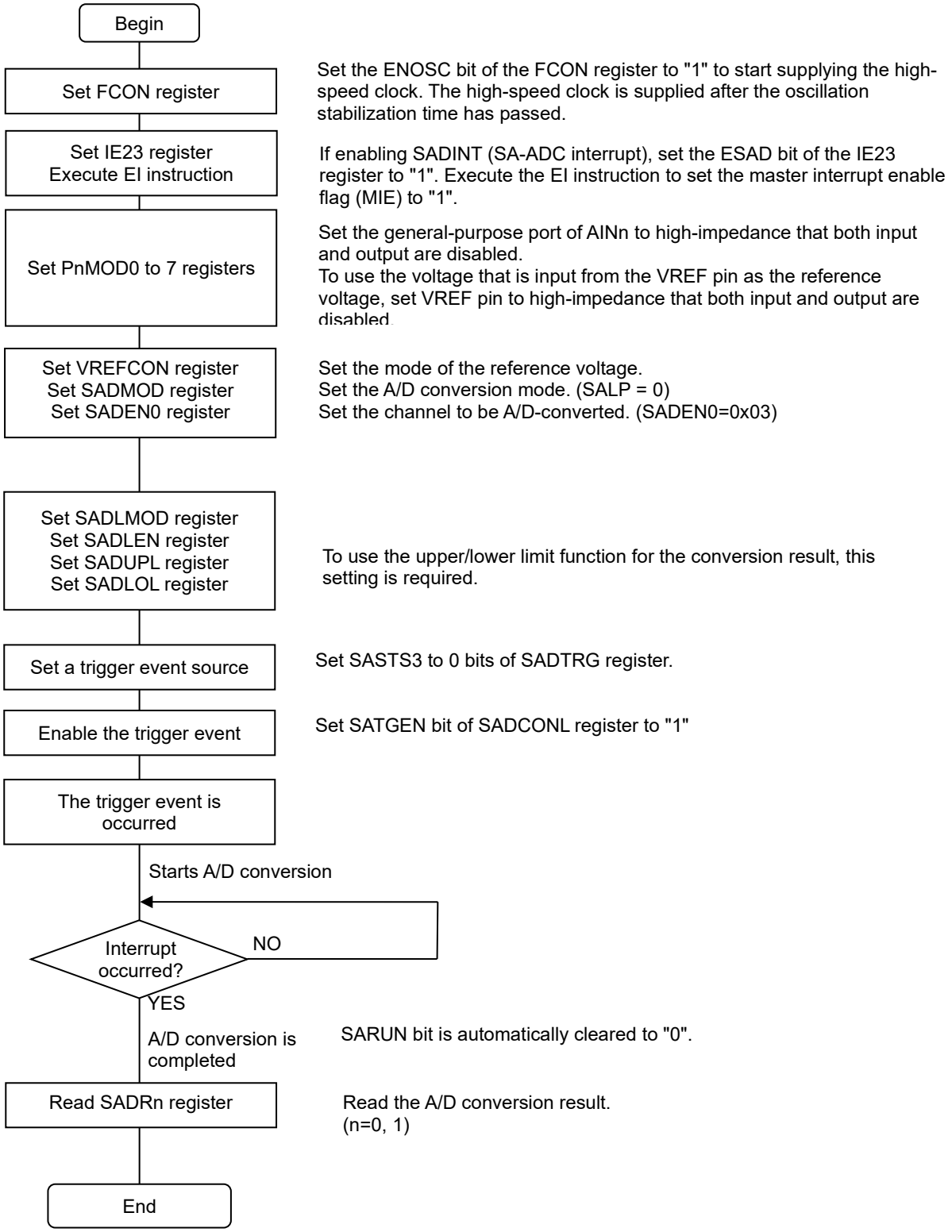
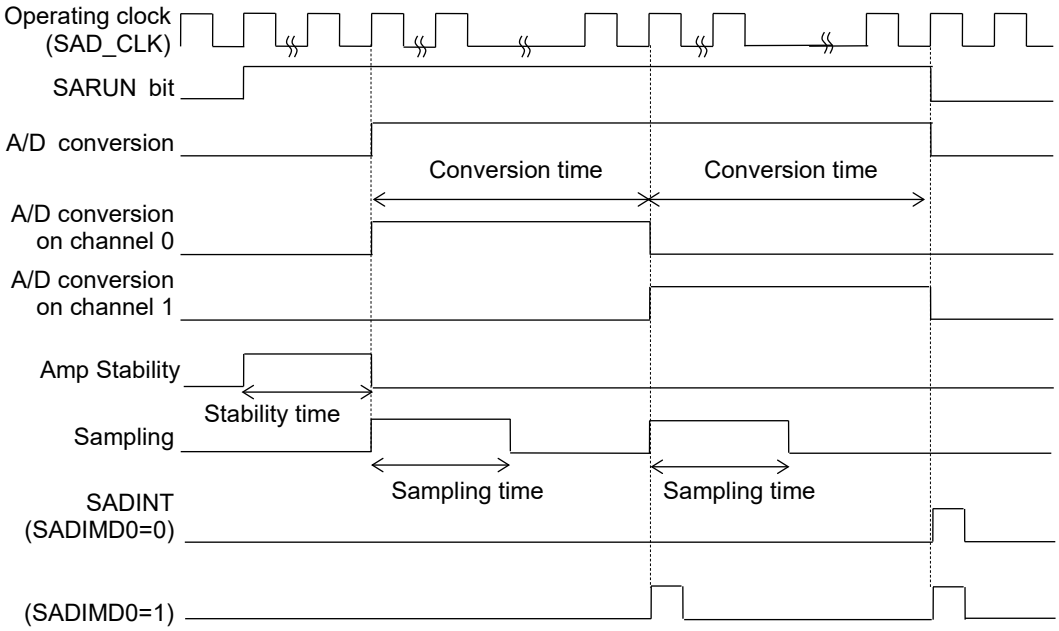


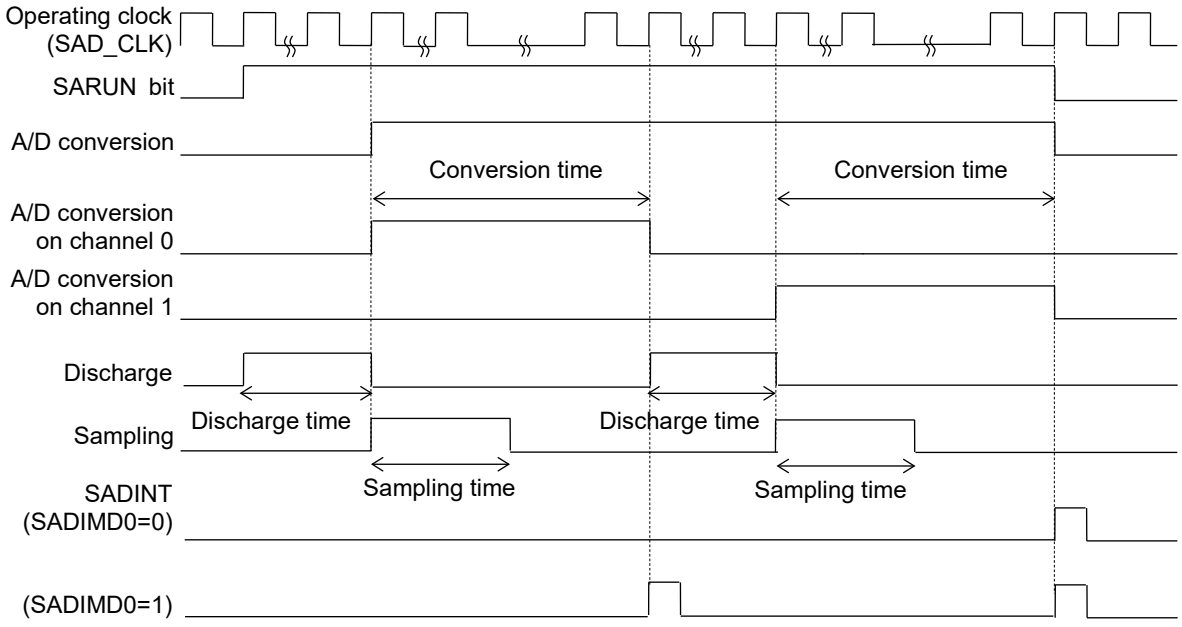
Figure 23-4 Example of A/D Conversion Setting (Start converting by a trigger event)

Figure 23-5 and 23-6 show operation waveforms when one-time A/D conversion is performed using channel 1 and 0.



Operating clock (SAD_CLK) is configured by SACK2-0 bits of SADMOD register.
Amp stability time is configured by SAINITT3-0 bits of SADMOD register.
Sampling time is configured by SASHT4-0 bits of SADMOD register.
Interrupt mode is configured by SADIMOD register.

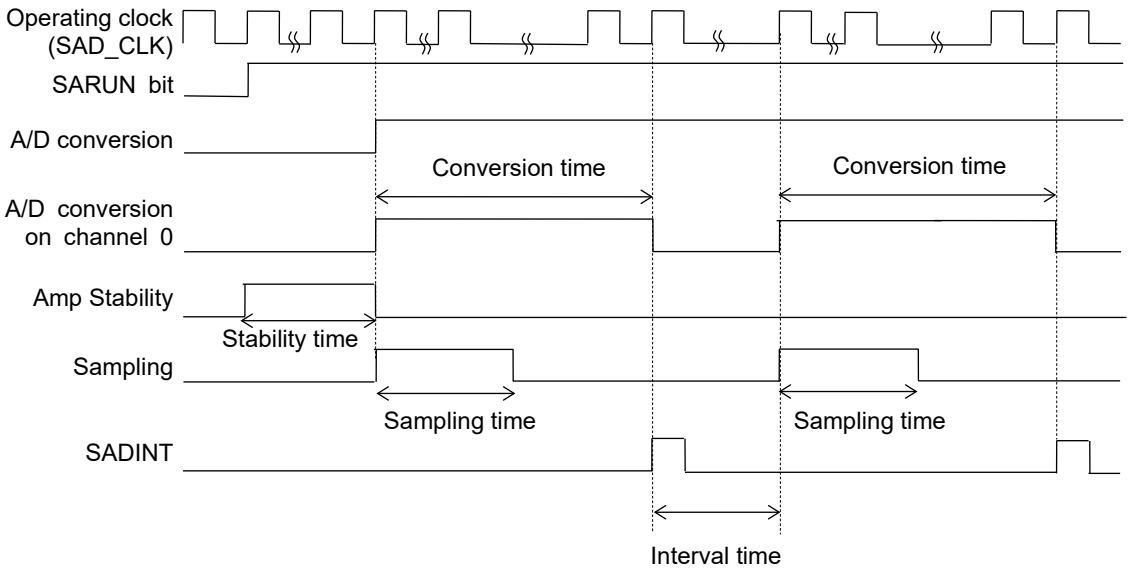
Figure 23-5 Operation Waveforms of A/D Conversion (One-time Conversion, Without Discharge)



Operating clock (SAD_CLK) is configured by SACK2-0 bits of SADMOD register.
Discharge enabling and time are configured by SAINIT bit and SAINITT3-0 bits of SADMOD register.
Sampling time is configured by SASHT4-0 bits of SADMOD register.
Interrupt mode is configured by SADIMOD register.

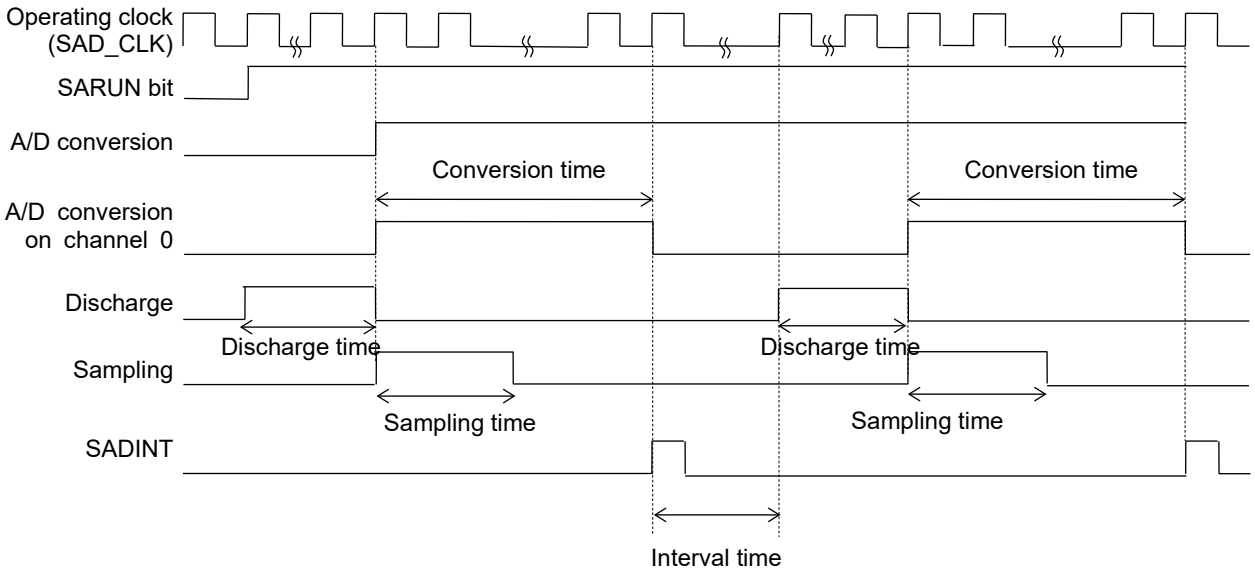
Figure 23-6 Operation Waveforms of A/D Conversion (One-time Conversion, With Discharge)

Figure 23-7 and 23-8 show the operation waveforms when the continuous A/D conversion is performed using channel 0.



Operating clock (SAD_CLK) is configured by SACK2-0 bits of SADMOD register.
Amp stability time is configured by SAINITT3-0 bits of SADMOD register.
Sampling time is configured by SASHT4-0 bits of SADMOD register.
Interrupt mode is configured by SADIMOD register.

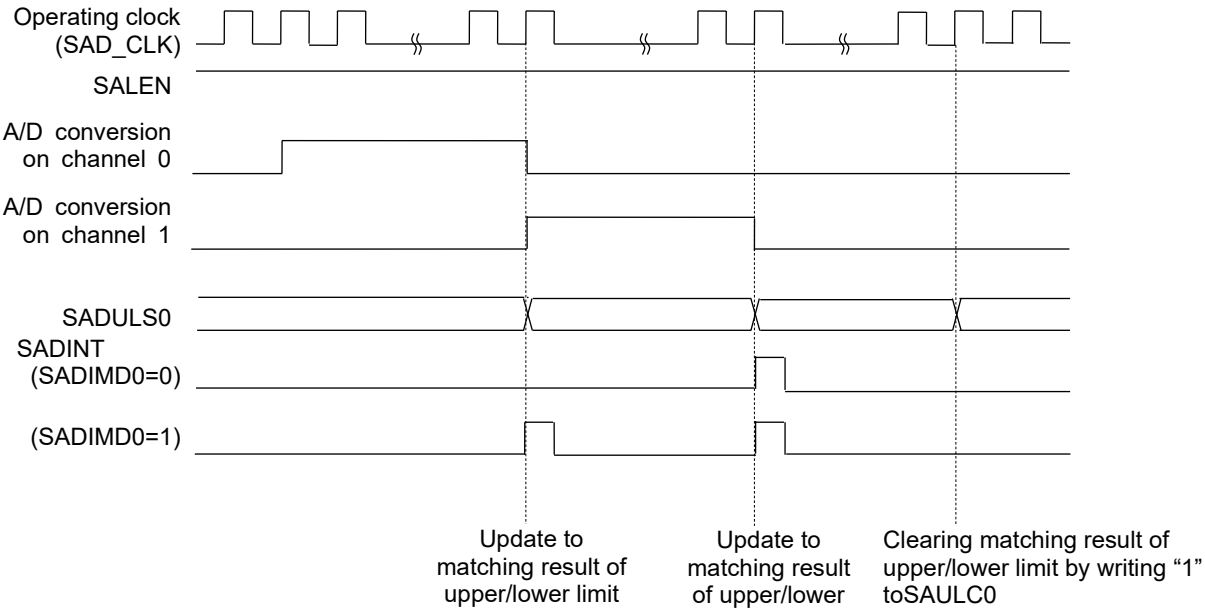
Figure 23-7 Operation Waveforms of A/D Conversion (Continuous Conversion, Without Discharge)



Operating clock (SAD_CLK) is configured by SACK2-0 bits of SADMOD register.
Discharge enabling and time are configured by SAINIT bit and SAINITT3-0 bits of SADMOD register.
Sampling time is configured by SASHT4-0 bits of SADMOD register.
Interrupt mode is configured by SADIMOD register.

Figure 23-8 Operation Waveforms of A/D Conversion (Continuous Conversion, With Discharge)

Figure 23-9 to 23-11 show the operation waveforms when an A/D conversion is performed with upper/lower limit function using channel 1 and 0.



A reflection of writing “1” to SAULC0 bit to clear matching result of upper/lower limit, is delayed maximum 1clock of the SAD_CLK.

Figure 23-9 Operation Waveforms of A/D Conversion with Upper/Lower Limit
(when set SADIMD1 bit to 0, in the case of matched to the limit ranges (SALMD1 to 0))

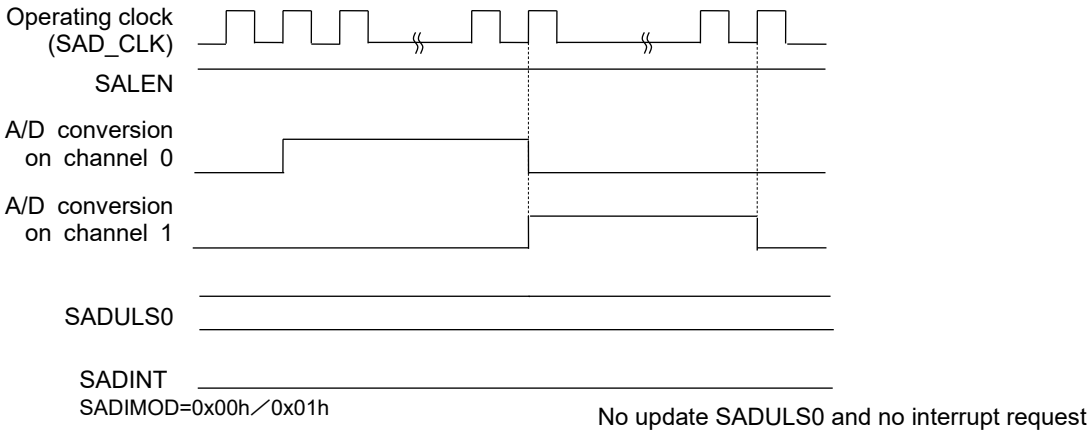
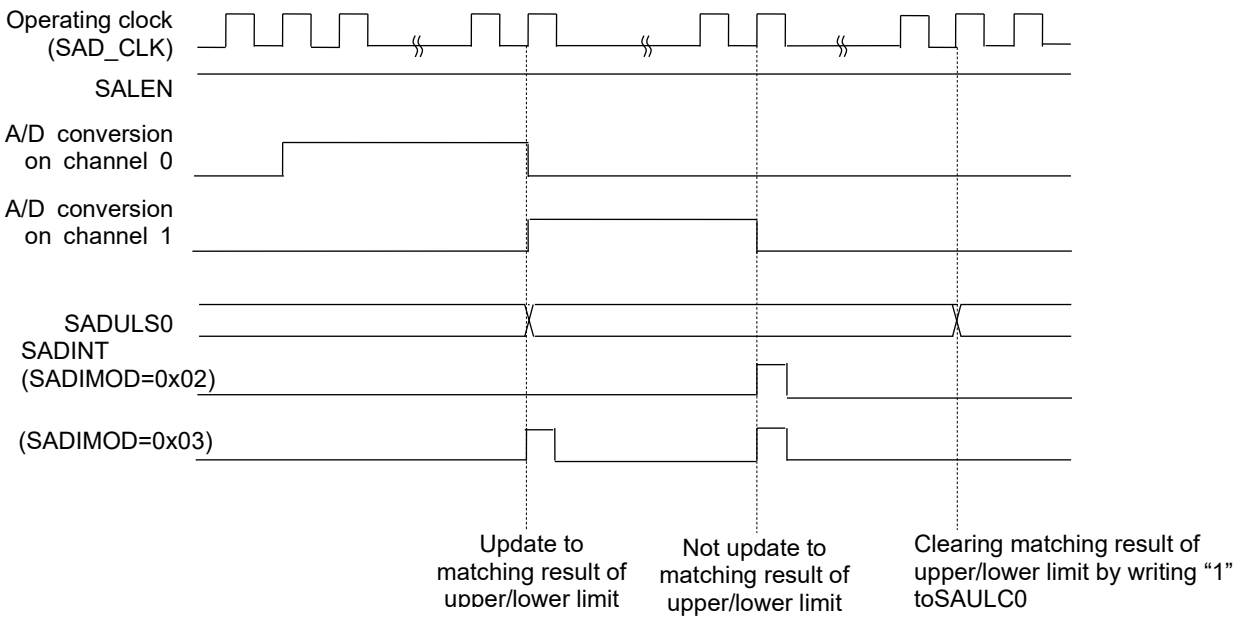


Figure 23-10 Operation Waveforms of A/D Conversion with Upper/Lower Limit
(when set SADIMD1 bit to 0, in the case of not matched to the limit ranges (SALMD1 to 0))



The interrupt occurs regardless of matching result of upper/lower limit.

Figure 23-11 Operation Waveforms of A/D Conversion with Upper/Lower Limit (SADIMD1 = 1)

23.3.2 How to test the Successive Approximation Type A/D Converter

The self test is available by A/D-converting the full scale, zero scale and internal reference voltage.
Follow this procedure to check if the successive approximation type A/D converter works correctly. (n=0 to 15)

(1) A/D convert AINn pin. (conversion result 1)
(2) A/D convert AIN=full scale by setting the SADTMOD register (SADTMOD=0x01).
(3) A/D convert the AINn pin. (conversion result 2)
(4) A/D convert AIN=zero scale by setting the SADTMOD register (SADTMOD=0x02).
(5) A/D convert the AINn pin. (conversion result 3)
(6) A/D convert AIN=internal reference voltage(approx.1.0V) by setting the SADTMOD register (SADTMOD=0x03).
(7) A/D convert the AINn pin. (conversion result 4)
(8) Confirm conversion result 1 = conversion result 2 = conversion result 3 = conversion result 4.
Use the same AINn pin for the A/D conversion in (1), (3), (5) and (7).
(9) Confirm the conversion result in (2), (4) and (6) is different each other and also different from the result in (1), (3), (5) and (7).

23.4 Notes on SA-ADC

23.4.1 Sampling Time Setting

Sampling time of the SA-ADC should satisfy the following formula:

$$\text{Sampling time} > 9(C_{SAMPLE} + C_{PARA})(R_1 + R_2)$$

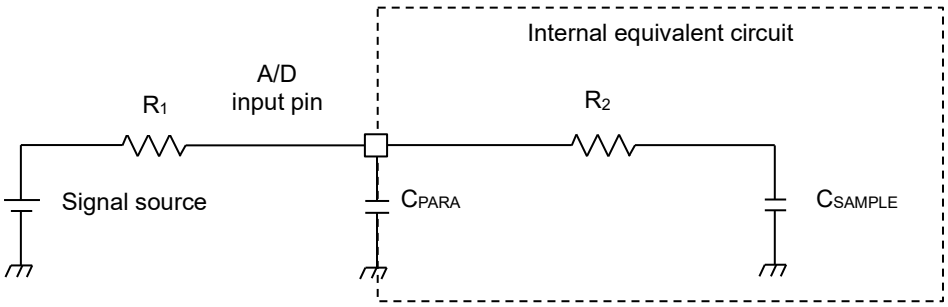
To calculate sampling time more precisely, use the following formula:

$$\text{Sampling time} = \left\{log_e(2^n) + log_e\left(\frac{C_{SAMPLE}}{C_{SAMPLE} + C_{PARA}}\right)\right\}(C_{SAMPLE} + C_{PARA})(R_1 + R_2)$$

C_{PARA} varies depending on board-layout and connected parts. Please check the accuracy of SA-ADC with the actual board.

R_1 : Input impedance of external resistor
R_2 : Internal resistor value which is the sum of the internal resistor and the ON register of the switch
C_{SAMPLE} : Sample hold capacitor
C_{PARA} : Parasitic capacitance of the A/D input line (Measure the capacitance between the A/D input line and V_{SS}.)
n : Resolution of SA-ADC

The following diagram shows the equivalent circuit in this case:



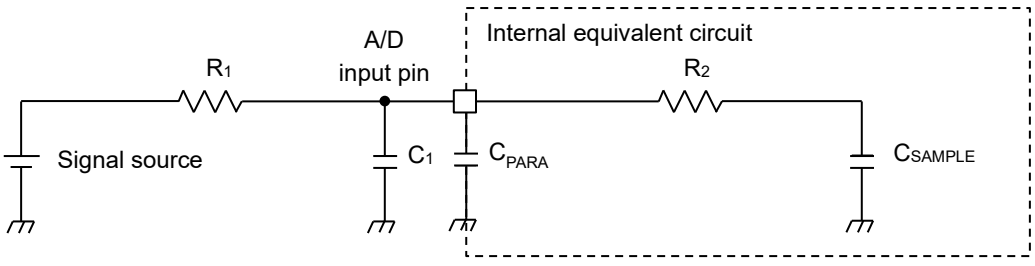
V_{REF}	R_2[kΩ]	C_{SAMPLE} [pF]
1.8V≤V_{REF}≤2.4V	170k	5pF
2.4V≤V_{REF}≤2.7V	20k	5pF
2.7V≤V_{REF}≤5.5V	10k	5pF

The values above are reference values.
Set the sampling time for V_{REF} condition that includes the lowest voltage of the usage range of V_{REF}.
If the sampling time above is unsatisfied, connect the external capacitor C_1 near by A/D input pin to satisfy the following formula.

$$(C_1 + C_{PARA}) > 2^n C_{SAMPLE}$$
$$\text{Sampling time} > 9C_{SAMPLE}R_2$$

C_1 : External capacitor

The equivalent circuit when the external capacitor C_1 is connected is as follows:



Note that the voltage at the A/D input pin transitionally changes due to the external capacitor C_1 and the external resistor R_1. Therefore, when sampling data, wait until the voltage is stabilized. If the stabilization timing is unknown, perform A/D conversion once, then wait for time constant τ ($=R_1C_1$) to 4τ or so and perform A/D conversion again. Confirm that the difference between values is small, and then sample data.

23.4.2 Noise Suppression

In order to prevent deterioration in accuracy of A/D conversion, operate the A/D converter in the environment with low noise.
The following processes are recommended for noise reduction:

- A/D conversion in the HALT mode.
- Do not have clock input/output from a pin located in the vicinity of the pin in which A/D conversion is in progress.
- Do not have clock input/output from the pin in which A/D conversion is in progress and other A/D conversion pins.

In addition, the capacitor for noise suppression should be connected between VREF and VSS, as well as between VDD and VSS. When connecting, place the capacitor in the immediate vicinity of LSI using short wiring.

Chapter 25 Audio Playback Function

25.Audio Playback Function

25.1 Summary

The ML62Q2700 group has a built-in audio playback function.

25.1.1 Feature

Audio PWM is output from P61 and P62 which are setting sixth function. Audio playback by connecting an external speaker amplifier to P61/P62.

Audio playback time:(in the case of the 16Kbytes Control program size)

Part number	Flash Memory Size (bit)	Maximum playback Time (second) (At sampling frequency is 7.81kHz)	
		4bit ADPCM2	16bit PCM
ML62Q2727/Q2737/Q2747	1919.5K (built-in)	62.8	15.7
ML62Q2726/Q2736/Q2746	1407.5K (built-in)	46.0	11.4
ML62Q2725/Q2735/Q2745	1151.5K (built-in)	37.6	9.3
ML62Q2703/Q2713/Q2723	639.5K (built-in)	20.8	5.2
ML62Q2702/Q2712/Q2722	383.5K (built-in)	12.5	3.1
All Products	128 M (external)	4296.2	1074.0

- Sampling frequency: Selectable from among
  - 7.81/15.63/31.25 kHz; 10.42/20.83 kHz; 6.25/12.5/25.0 kHz in each phrase
- Allows audio operations using the following voice synthesis algorithms:
  - 4-bit ADPCM2, 8-bit non-linear PCM, 8-bit straight PCM, and 16-bit straight PCM.
- Volume adjustment function: Adjustable 32 levels volume (including off-state).
- Edit ROM function: multiple phrases continuous playback
  - Efficient use of memory capacity for voice code data. Refer to the section 25.3.9, Edit ROM Function for detail.
- Integrated Serial Flash Memory Interface Supports External Memory. (7th function of P14 toP16 and P50 to P53)
  - No mixture of Audio code data arrangement in integrated Flash Memory and External Serial Flash memory is allowed
- "High" level fixed detection function of audio PWM output
  - This function prevents overcurrent from continuing to flow through the external speaker amplifier in case PWM fixed to "High" level due to internal PWM malfunction. When the LSI detects that the internal PWM is fixed at the "high" level, the LSI sets the audio PWM output pin to Hi-z.

25.1.2 Configuration

25.1.2.1 Block Configuration

Figure 25-1 shows the block configuration of the audio playback function.

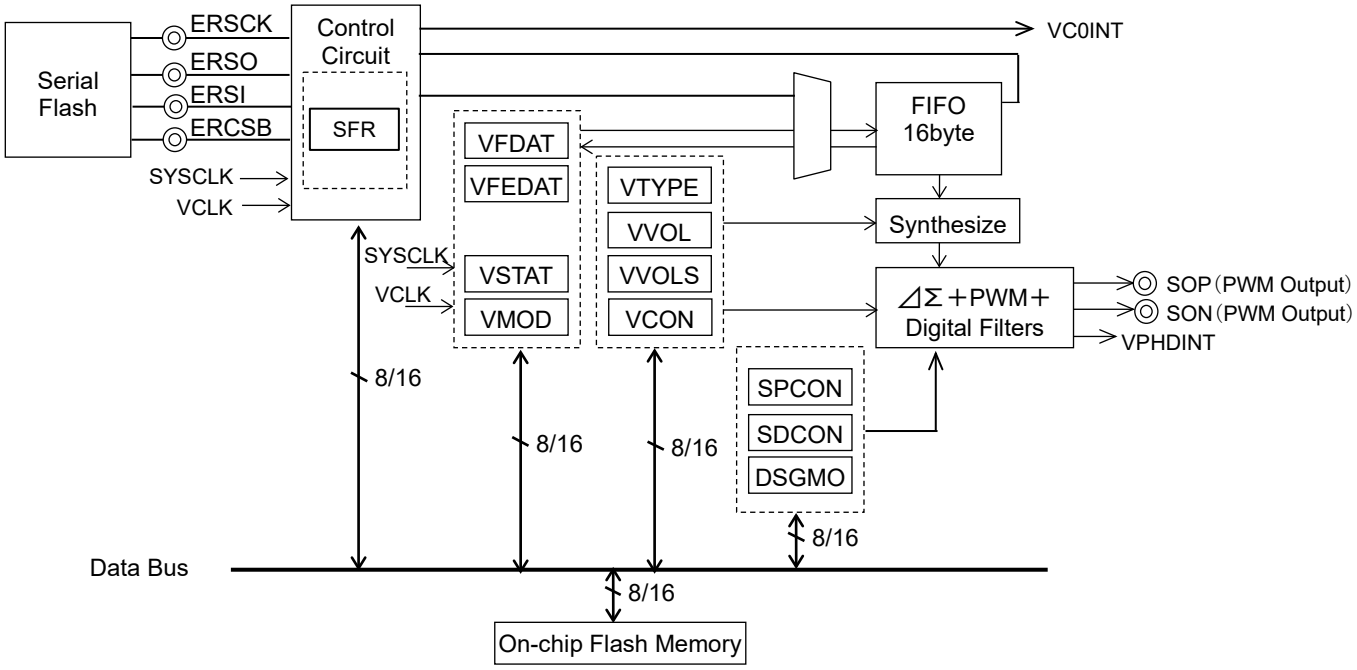


Figure 25-1 Block Configuration of Audio Playback Function

The operating principle of sound reproduction is as follows.

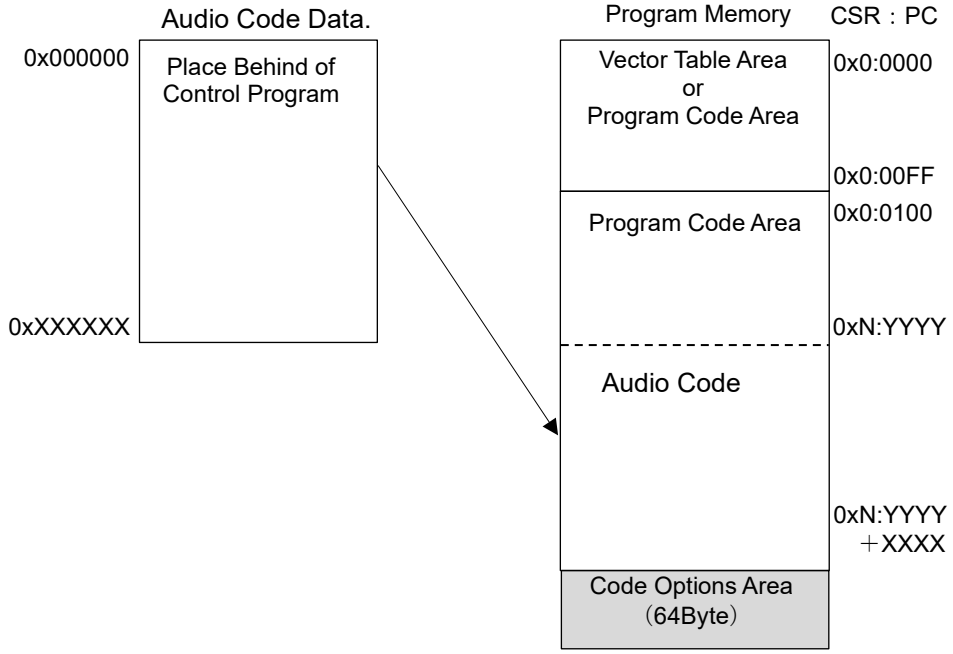
1. Original sound data (WAV file) is converted into audio code data (binary data, Motorola S format) by Speech LSI Utility tools (audio phrase creation, voice synthesis method, sampling frequency, etc.). The data is placed in the flash memory as audio code data.
2. Audio data placed in the flash memory is transferred to the voice synthesis circuit via the CPU
3. Voice synthesizes is carried out while storing audio data in a FIFO, and reproduces the sound close to the original sound with digital filters.
4. PWM signal is output from a digital filter and amplified by an external speaker amplifier for audio reproduction.

【Note】

- **When using the audio playback function, select the Low speed crystal oscillation clock (XT32K) as the clock source for the Low speed clock 0 (LSCLK0).**
- **When using the audio playback function, enable High speed clock oscillation by frequency control register（FCONW）.**
- **Selects PLL oscillation mode from 24 MHz mode or 16 MHz mode and set the high-speed clock mode register (FHCKMOD) so that the system clock set 24 MHz in 24 MHz mode and 16 MHz in 16 MHz mode.**

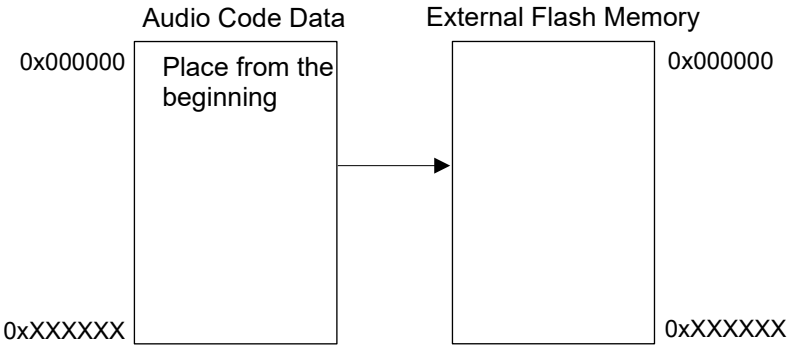
25.1.2.2 Arrangement of Audio Code Data

When the audio code data is placed in the internal flash memory, it is placed after the control program. When placing in external flash memory, place it from the beginning.
Figure 25-2 shows the arrangement of audio code data.



0xXXXXXX : The last Address of the Audio Code Data
0xN:YYYY : The last Address of the Control Program (N:0 to 3)

Figure 25-2 Arrangement of Audio Code Data (when placed in the internal flash memory)



0xXXXXXX : The last Address of the Audio Code Data

Figure 25-2 Arrangement of Audio Code Data (when placed in the external flash memory)

25.1.3 Terminal List

The input and output terminals of the audio playback function are assigned to functions that can also be used as general-purpose ports.

Terminal Name	I/O	Description
SOP	O	P-side output of audio PWM
SON	O	N-side output of audio PWM
ERSCK	I/O	Serial clock input and output of external serial flash memory for audio
ERSO	O	Serial data output of external serial flash memory for audio
ERSI	I	Serial data input for external serial flash memory for audio
ERCSB	I/O	Chip select input/output of external serial flash memory for audio

Table 25-1 lists the generic port and register settings used for audio playback functions.

Table 25-1 Audio Playback Port and Register Settings

Terminal Name	Port		Setting Register	Setting Value
SOP	P61	6th function	P6MOD1	0101_0010
SON	P62	6th function	P6MOD2	0101_0010
ERSCK	P50	7th function	P5MOD0	0110_0011
ERSO	P16	7th function	P1MOD6	0110_0010
	P51	7th function	P5MOD1	0110_0010
ERSI	P14	7th function	P1MOD4	0110_0001
	P52	7th function	P5MOD2	0110_0001
ERCSB	P15	7th function	P1MOD5	0110_0011
	P53	7th function	P5MOD3	0110_0011

25.1.4 Terminal combinations

Table 25-2 lists the terminal combination of each package. Other combination is invalid.

Table 25-2 Terminal combination of each package

Port name	48pin product	52pin product	64pin product	80pin product	100pin product
SOP	P61	P61	P61	P61	P61
SON	P62	P62	P62	P62	P62
ERSCK	P50	P50	P50	P50	P50
ERSO	P16	P51	P51	P51	P51
ERSI	P14	P14	P52	P52	P52
ERCSB	P15	P15	P53	P53	P53

25.2 Register Description

25.2.1 Register List

Address	Name	Symbol Name		R/W	Size	Initial Value
		Byte	Word			
0xFA00	Audio Data Start Address Register L	STAADRL0	STAADRML0	R/W	8/16	0x00
0xFA01	Audio Data Start Address Register M	STAADRM0		R/W	8	0x00
0xFA02	Audio Data Start Address Register H	STAADRH0	STAADRHH0	R/W	8/16	0x00
0xFA03	Reserved Register	-	-	R	8	0x00
0xFA04	Audio Data Stop Address Register L	STPADRL0	STPADRML0	R/W	8/16	0XFF
0xFA05	Audio Data Stop Address Register M	STPADRM0		R/W	8	0XFF
0xFA06	Audio Data Stop Address Register H	STPADRH0	STPADRHH0	R/W	8/16	0XFF
0xFA07	Reserved Register	-	-	R	8	0x00
0xFA08	Event Management Start Address Register L	STAADRL1	STAADRML1	R/W	8/16	0x00
0xFA09	Event Management Start Address Register M	STAADRM1		R/W	8	0x00
0xFA0A	Event Management Start Address Register H	STAADRH1	STAADRHH1	R/W	8/16	0x00
0xFA0B	Reserved Register	-	-	R	8	0x00
0xFA0C	Event Management Stop Address Register L	STPADRL1	STPADRML1	R/W	8/16	0XFF
0xFA0D	Event Management Stop Address Register M	STPADRM1		R/W	8	0XFF
0xFA0E	Event Management Stop Address Register H	STPADRH1	STPADRHH1	R/W	8/16	0XFF
0xFA0F	Reserved Register	-	-	R	8	0x00
0xFA10	Editing Data Start Address Register L	STAADRL2	STAADRML2	R/W	8/16	0x00
0xFA11	Editing Data Start Address Register M	STAADRM2		R/W	8	0x00
0xFA12	Editing Data Start Address Register H	STAADRH2	STAADRHH2	R/W	8/16	0x00
0xFA13	Reserved Register	-	-	R	8	0x00
0xFA14	Editing Data Stop Address Register L	STPADRL2	STPADRML2	R/W	8/16	0XFF
0xFA15	Editing Data Stop Address Register M	STPADRM2		R/W	8	0XFF
0xFA16	Editing Data Stop Address Register H	STPADRH2	STPADRHH2	R/W	8/16	0XFF
0xFA17	Reserved Register	-	-	R	8	0x00
0xFA18	Audio Playback Mode Register	VEXMOD	-	R/W	8	0x00
0xFA19	Reserved Register	-	-	-	-	-
0xFA1A	Audio Readout Request Register	VEXCNT	VEXCONT	R/W	8/16	0x00
0xFA1B	Audio Readout Stop Register	VEXSTP		W	8	0x00
0xFA1C	Audio Data Readout Interrupt Threshold Setting Register	VEXAE	-	R/W	8	0x00
0xFA1D	Reserved Register	-	-	-	-	-
0xFA1E	Audio Interrupt Permission Register	VEXIE	-	R/W	8	0x10
0xFA1F	Reserved Register	-	-	-	-	-
0xFA20	Audio Interrupt Request Status Register	VEXSTAT	-	R	8	0x00
0xFA21	Reserved Register	-	-	-	-	-
0xFA22	Audio Interrupt Request Clear Register L	VEXSTATCLL	VEXSTATCL	W	8/16	0x00
0xFA23	Audio Interrupt Request Clear Register H	VEXSTATCLH		W	8	0x00
0xFA24	Audio Data Readout Address Counter L	ADRCNTL0	ADRCNTML0	R	8/16	0x00
0xFA25	Audio Data Readout Address Counter M	ADRCNTM0		R	8	0x00
0xFA26	Audio Data Readout Address Counter H	ADRCNTH0	ADRCNTHH0	R	8/16	0x00
0xFA27	Reserved Register	-	-	R	8	0x00
0xFA28	Audio Data Playback Stop Address Register L	CSTPADRL0	ADRCNTML0	R	8/16	0x00
0xFA29	Audio Data Playback Stop Address Register M	CSTPADRM0	CSTPADRML0	R	8	0x00
0xFA2A	Audio Data Playback Stop Address Register H	CSTPADRH0	CSTPADRHH0	R	8/16	0x00
0xFA2B	Reserved Register	-	-	R	8	0x00
0xFA2C to 0xFA2F	Reserved Register	-	-	-	-	-

Address	Name	Symbol Name		R/W	Size	Initial Value
		Byte	Word			
0xFA30	Audio Data Readout Store Register0	CH0BUF0	CH0BUF10	R	8/16	0x00
0xFA31	Audio Data Readout Store Register1	CH0BUF1		R	8	0x00
0xFA32	Audio Data Readout Store Register2	CH0BUF2	CH0BUF32	R	8/16	0x00
0xFA33	Audio Data Readout Store Register3	CH0BUF3		R	8	0x00
0xFA34	Audio Data Readout Store Register4	CH0BUF4	CH0BUF54	R	8/16	0x00
0xFA35	Audio Data Readout Store Register5	CH0BUF5		R	8	0x00
0xFA36	Audio Data Readout Store Register6	CH0BUF6	CH0BUF76	R	8/16	0x00
0xFA37	Audio Data Readout Store Register7	CH0BUF7		R	8	0x00
0xFA38	Event Management Readout StoreRegister0	CH1BUF0	CH1BUF10	R	8/16	0x00
0xFA39	Event Management Readout Store Register1	CH1BUF1		R	8	0x00
0xFA3A	Event Management Readout Store Register2	CH1BUF2	CH1BUF32	R	8/16	0x00
0xFA3B	Event Management Readout Store Register3	CH1BUF3		R	8	0x00
0xFA3C	Event Management Readout Store Register4	CH1BUF4	CH1BUF54	R	8/16	0x00
0xFA3D	Event Management Readout Store Register5	CH1BUF5		R	8	0x00
0xFA3E	Event Management Readout Store Register6	CH1BUF6	CH1BUF76	R	8/16	0x00
0xFA3F	Event Management Readout Store Register7	CH1BUF7		R	8	0x00
0xFA40	Editing Data Readout Store Register0	CH2BUF0	CH2BUF10	R	8/16	0x00
0xFA41	Editing Data Readout Store Register1	CH2BUF1		R	8	0x00
0xFA42	Editing Data Readout Store Register2	CH2BUF2	CH2BUF32	R	8/16	0x00
0xFA43	Editing Data Readout Store Register3	CH2BUF3		R	8	0x00
0xFA44	Editing Data Readout Store Register4	CH2BUF4	CH2BUF54	R	8/16	0x00
0xFA45	Editing Data Readout Store Register5	CH2BUF5		R	8	0x00
0xFA46	Editing Data Readout Store Register6	CH2BUF6	CH2BUF76	R	8/16	0x00
0xFA47	Editing Data Readout Store Register7	CH2BUF7		R	8	0x00
0xFA48 to 0xFAAF	Reserved Register	-	-	-	-	-
0xFAB0	Audio FIFO Data Register	VFDAT	-	W	8	0x00
0xFAB1	Reserved Register	-	-	-	-	-
0xFAB2	Audio FIFO Phrase End Data Register	VFEDAT	-	W	8	0x00
0xFAB3	Reserved Register	-	-	-	-	-
0xFAB4	Reserved Register	-	-	-	-	-
0xFAB5	Reserved Register	-	-	-	-	-
0xFAB6	Audio Status Register	VSTAT	-	R	8	0x11
0xFAB7	Reserved Register	-	-	-	-	-
0xFAB8	Audio Mode Register	VMOD	-	R/W	8	0x00
0xFAB9	Reserved Register	-	-	-	-	-
0xFABA	Audio Data Type Register	VTYPE	-	R/W	8	0x41
0xFABB	Reserved Register	-	-	-	-	-
0xFABC	Volume Setting Register	VVOL	-	R/W	8	0x09
0xFABD	Reserved Register	-	-	-	-	-
0xFABE	Audio Playback Control Register	VCON	-	R/W	8	0x00
0xFABF	Reserved Register	-	-	-	-	-
0xFAC0 to 0xFAC7	Reserved Register	-	-	-	-	-
0xFAC8	Audio PWM Control Register	SPCON	-	R/W	8	0x00
0xFAC9	Reserved Register	-	-	-	-	-
0xFACA to 0xFACF	Reserved Register	-	-	-	-	-

Address	Name	Symbol Name		R/W	Size	Initial Value
		Byte	Word			
0xFAD0	Volume Status Register	VVOLS	-	R	8	0x09
0xFAD1 to 0xFADF	Reserved Register	-	-	-	-	-
0xFAE0	Audio PWM Fixed Detection Control Register	SDCON	-	R/W	8	0x00
0xFAE1	Reserved Register	-	-	-	-	-
0xFAE2 to 0xFAE3	Reserved Register	-	-	-	-	-
0xFAE4	PWM Output Waveform Mode Register for Audio	DSGMOD	-	R/W	8	0x02
0xFAE5	Reserved Register	-	-	-	-	-
0xFAE6 to 0xFAFF	Reserved Register	-	-	-	-	-

25.2.2 Audio Data Start Address Register M/L(STAADRML0)

STAADRML0 is a SFR to set the middle and lower addresses of the read start address of the audio data stored in the external flash memory.
This is used when the audio code data is placed in the external flash memory
When VEXCNT0 bit of the audio read request register (VEXCONT) is set to "1", the audio data is read from the address set in this register synchronously with the sampling frequency.
Write to the audio FIFO in the order of the read audio data

Address: 0xFA00(STAADRL0/STAADRML0), 0xFA01(STAADRM0)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STAADRML0															
Byte	STAADRM0								STAADRL0							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.3 Audio Data Start Address Register H (STAADRHH0)

STAADRHH0 is a SFR to set the upper order address of the read start address of the audio data stored in the external flash memory.
This is used when the audio code data is placed in external flash memory.
When VEXCNT0 bit of the audio read request register (VEXCONT) is set to "1", audio data is read from the address set in this register synchronously to the sampling frequency.
Write to the audio FIFO in the order of the read audio data.

Address: 0xFA02(STAADRH0/STAADRHH0)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STAADRHH0															
Byte	-								STAADRH0							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.4 Audio Data Stop Address Register M/L (STPADRML0)

STPADRML0 is a SFR to set the middle and bottom addresses of the read end address of the audio data stored in the external flash memory.
This is used when the audio code data is placed in external flash memory.
When VEXCNT0 bit of the audio read request register (VEXCONT) is set to "1", the audio data is read to the address set in this register synchronously with the sampling frequency.

Address: 0xFA04(STPADRL0/STPADRML0), 0xFA05(STPADRM0)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0xFFFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STPADRML0															
Byte	STPADRM0								STPADRL0							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

25.2.5 Audio Data Stop Address Register H (STPADRHH0)

STPADRHH0 is a SFR to set the upper order address of the read end address of audio data stored in the external flash memory.
This is used when the audio code data is placed in external flash memory.
When VEXCNT0 bit of the audio read request register (VEXCONT) is set to "1", audio data up to the address set in this register is read synchronously to the sampling frequency.

Address: 0xFA06(STPADRH0/STPADRHH0)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x00FF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STPADRHH0															
Byte	-								STPADRH0							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

25.2.6 Event Management Start Address Register M/L (STAADRML1)

STAADRML1 is a SFR to set the middle and lower addresses of the start address of reading event management data stored in the external flash memory.
This is used when the audio code data is placed in the external flash memory.
Setting VEXCNT1 bit of the audio read request register (VEXCONT) to "1" synchronizes with the sampling frequency and starts reading event management data from the address set in this register.

Address: 0xFA08(STAADRL1/STAADRML1), 0xFA09(STAADRM1)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STAADRML1															
Byte	STAADRM1								STAADRL1							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.7 Event Management Start Address Register H (STAADRHH1)

STAADRHH1 is a SFR to set the upper address of the read start address of the event management data stored in the external flash memory.
It is used when the audio code data is placed in the external flash memory.
Setting VEXCNT1 bit of the audio read request register (VEXCONT) to "1" synchronizes with the sampling frequency and starts reading event management data up to the address set in this register.

Address: 0xFA0A(STAADRH1/STAADRHH1)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STAADRHH1															
Byte	-								STAADRH1							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.8 Event Management Stop Address Register M/L (STPADRML1)

STPADRML1 is a SFR to set the middle and lower addresses of the read end address of the event management data stored in the external flash memory.
It is used when audio code data is placed in the external flash memory.
When VEXCNT1 bit of the audio read request register (VEXCONT) is set to "1", event management data up to the address set in this register is read synchronously to the sampling frequency.

Address: 0xFA0C(STPADRL1/STPADRML1), 0xFA0D(STPADRM1)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STPADRML1															
Byte	STPADRM1								STPADRL1							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

【Note】

- **To set the value of the event management stop address register H/M/L, add +7 to the value set in the event management start address register H/M/L.**

25.2.9 Event Management Stop Address Register H (STPADRHH1)

STPADRHH1 is a SFR to set the upper address of the read end address of the event management data stored in the external flash memory.
It is used when the audio code data is placed in the external flash memory.
When VEXCNT1 bit of the audio read request register (VEXCONT) is set to "1", event management data up to the address set in this register is read synchronously to the sampling frequency.

Address: 0xFA0E(STPADRH1/STPADRHH1)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STPADRHH1															
Byte	-								STPADRH1							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

【Note】

- **To set the value of the event management stop address register H/M/L, add +7 to the value set in the event management start address register H/M/L.**

25.2.10 Editing Data Start Address Register M/L (STAADRML2)

STAADRML2 is a SFR to set the middle and lower addresses of the start address of the editing data read stored in the external flash memory.
It is used when the audio code data is placed in the external flash memory.
When VEXCNT2 bit of the audio read request register (VEXCONT) is set to "1", editing data is read from the address set in this register synchronously to the sampling frequency.

Address: 0xFA10(STAADRL2/STAADRML2), 0xFA11(STAADRM2)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STAADRML2															
Byte	STAADRM2								STAADRL2							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.11 Editing Data Start Address Register H (STAADRHH2)

STAADRHH2 is a SFR to set the upper order address of the read start address of the editing data stored in the external flash memory.
It is used when the audio code data is placed in the external flash memory.
When VEXCNT2 bit of the audio read request register (VEXCONT) is set to "1", editing data is read from the address set in this register synchronously to the sampling frequency.

Address: 0xFA12(STAADRH2/STAADRHH2)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STAADRHH2															
Byte	-								STAADRH2							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.12 Editing Data Stop Address Register M/L (STPADRML2)

STPADRML2 is a SFR to set the middle and lower address of the read end address of the editing data stored in the external flash memory.
It is used whenthe audio code data is placed in the external flash memory.
When VEXCNT2 bit of the audio read request register (VEXCONT) is set to "1", editing data up to the address set in this register is read synchronously to the sampling period.

Address: 0xFA14(STPADRL2/STPADRML2), 0xFA15(STPADRM2)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STPADRML2															
Byte	STPADRM2								STPADRL2							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

【Note】

- **To set the value of the Editing data stop address register H/M/L, add +7 to the value set in the Editing data start address register H/M/L.**

25.2.13 Editing Data Stop Address Register H (STPADRHH2)

STPADRHH2 is a SFR to set the upper order address of the read end address of the editing data stored in the external flash memory.
Used when the audio code data is placed in the external flash memory.
When VEXCNT2 bit of the audio read request register (VEXCONT) is set to "1", editing data up to the address set in this register is read synchronously to the sampling period.

Address: 0xFA16(STPADRH2/STPADRHH2)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	STPADRHH2															
Byte	-								STPADRH2							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

【Note】

- **To set the value of the Editing data stop address register H/M/L, add +7 to the value set in the Editing data start address register H/M/L.**

25.2.14 Audio Playback Mode Register (VEXMOD)

VEXMOD is a SFR to set the playback mode during playback of audio data stored in the external flash memory.

Address: 0xFA18(VEXMOD)
Access: R/W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VEXMOD							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	VEXMODL	VEXMODM
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	description
7 to 2	-	Reserved bits
1	VEXMODL	instruct continuous playback. If "1" is set, one phrase is played followed by the next phrase. 0: Not play repeatedly (initial value) 1: Play repeatedly
0	VEXMODM	instruct silent playback. While "1" is set, it will be played silently. 0: Not play silently (initial value) 1: Silent playback

25.2.15 Audio Readout Request Register (VEXCONT)

VEXCONT is a SFR to indicates the request to read and stop the audio data stored in the external flash memory.

Address: 0xFA1A(VEXCNT/VEXCONT), 0xFA1B(VEXSTP)
Access: R/W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	VEXCONT															
Byte	VEXSTP								VEXCNT							
Bit	-	-	-	-	-	VEXSTP2	VEXSTP1	VEXSTP0	-	-	-	-	-	VEXCNT2	VEXCNT1	VEXCNT0
R/W	R	R	R	R	R	W	W	W	R	R	R	R	R	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	description
15 to 11	-	Reserved bits
10	VEXSTP2	Request to stop reading the editing data stored in the external flash memory. Note that write "1" to VEXSTP2 bit five times in a row. If the bit is set to "1" before starting readout, the readout is canceled. If the bit is set to "1" during readout, the readout is stopped in synchronizing with the sampling frequency and VEXCNT2 bit is set to "0". 0: No request to stop readout the editing data stored in the external flash memory (initial value) 1: Request to stop readout the editing data stored in the external flash memory
9	VEXSTP1	Request to stop reading the event management data stored in the external flash memory. If the bit is set to "1" before starting readout, the readout is canceled. If the bit is set to "1" during readout, the readout is stopped in synchronizing with the sampling frequency and VEXCNT1 bit is set to "0". 0: No request to stop readout the event management data stored in the external flash memory (initial value) 1: Request to stop reading the event management data stored in external flash memory
8	VEXSTP0	Request to stop reading the audio data stored in the external flash memory. If the bit is set to "1" before starting readout, the readout is canceled. If the bit is set to "1" during readout, the readout is stopped in synchronizing with the sampling frequency and VEXCNT0 bit is set to "0". 0: No request to stop readout the audio data stored in the external flash memory (initial value) 1: Request to stop reading the audio data stored in external flash memory
7 to 3	-	Reserved bits
2	VEXCNT2	Indicate to start reading the editing data stored in the external flash memory. If the bit is set to "1", the sampling frequency is synchronized, and the Editing data is read from the address set in the Editing data start address register. Read 8 bytes of data within one period of the sampling frequency. When reading to the address set in the Editing data stop address register is completed, it is reset to "0". Only "1" writes are enabled, "0" writes are ignored. If you want to set it to "0", write "1" in the VEXSTP2 bit. 0: No reading the editing data stored in external flash memory (initial value) 1: Reading the editing data stored in external flash memory
1	VEXCNT1	Indicate to start reading event management data stored in the external flash memory. If "1" is set, the sampling frequency is synchronized, and the event management data is read from the address set in the event management data start address register. Read 8 bytes of data within one period of the sampling frequency. When reading to the address set in the event management data stop address register is completed, it is reset to "0". Only "1" writes are enabled, "0" writes are ignored. If you want to set it to "0", write "1" in the VEXSTP1 bit. 0: No reading the event management data stored in external flash memory (initial value) 1: Reading the event management data stored in external flash memory

Bit Number	Bit Symbol Name	description
0	VEXCNT0	Indicate to start reading the audio data stored in the external flash memory. If the bit is set to "1", the sampling frequency is synchronized, and the audio data is read from the address set in the audio data start address register. Read 8 bytes of data within one period of the sampling frequency. When the reading of a phrase that has been canceled from repeated playback is completed, it is reset to "0". Only "1" writes are enabled, "0" writes are ignored. Writing "1" to the VEXSTP0 bit enables "0" writing. 0: No reading the audio data stored in external flash memory (initial value) 1: Reading the audio data stored in external flash memory

25.2.16 Audio Data Readout Interrupt Threshold Setting Register (VEXAE)

VEXAE is a SFR to set the threshold for interrupt requests that occur before the read is complete when reading audio data stored in external flash memory.

Address: 0xFA1C (VEXAE)
Access: R/W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VEXAE							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	VEXAE1	VEXAE0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	description
7 to 2	-	Reserved bits
1, 0	VEXAE1, VEXAE0	Sets the threshold for interrupt requests that occur before the readout is complete. 00: Raises an interrupt request when the audio data readout is complete. (initial value) 01: Raises an interrupt request when the audio data readout is equal or less than 8 bytes remaining before the readout is complete 10: Raises an interrupt request when the audio data readout is equal or less than 16 bytes remaining before the readout is complete 11: Raises an interrupt request when the audio data readout is equal or less than 32 bytes remaining before the readout is complete

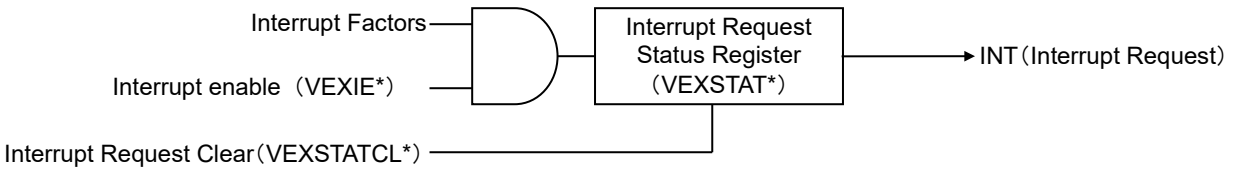
25.2.17 Audio Interrupt Enable Register (VEXIE)

VEXIE is a SFR to disable or enable interrupt of audio code data read interrupt and audio playback function interrupt stored in the external flash memory. Writing a "1" to each bit enables interrupts and notifies the interrupt controller.

Address: 0xFA1E (VEXIE)
Access: R/W
Access Size: 8bit
Initial Value: 0x10

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VEXIE							
Bit	-	-	-	-	-	-	-	-	-	-	-	VEXIE VOI	VEXIE AE	VEXIE CH2	VEXIE CH1	VEXIE CH0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit Number	Bit Symbol Name	description
7 to 5	-	Reserved bits
4	VEXIEVOI	0: Interrupt disabled according to the audio status register (VSTAT) 1: Interrupt enabled according to the audio status register (VSTAT) (initial value)
3	VEXIEAE	0: Interrupt disabled according to the voice data read interrupt threshold value setting (initial value) 1: Interrupt enabled according to the voice data read interrupt threshold value setting
2	VEXIECH2	0: Disable interrupts for reading Editing data stored in the external flash memory (initial value) 1: Enable interrupts for reading Editing data stored in the external flash memory
1	VEXIECH1	0: Disable interrupts for reading event management data stored in the external flash memory (initial value) 1: Enable interrupts for reading event management data stored in the external flash memory
0	VEXIECH0	0: Disable interrupts for reading audio data stored in the external flash memory (initial value) 1: Enable interrupts for reading audio data stored in the external flash memory



*: Bits of Interest for each Register

25.2.18 Audio Interrupt Request Status Register (VEXSTAT)

VEXSTAT is a SFR to indicate the interrupt status of the audio code data read interrupt and the audio playback function interrupt stored in the external flash memory.

Address: 0xFA20(VEXSTAT)
Access: R
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VEXSTAT							
Bit	-	-	-	-	-	-	-	-	-	-	-	VEXSTATVO	VEXSTATAE	VEXSTAT2	VEXSTAT1	VEXSTAT0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	description
7 to 5	-	Reserved bits
4	VEXSTATVO	0: No interrupt occurrence according to the audio status register (VSTAT) (initial value) 1: An interrupt occurrence according to the audio status register (VSTAT)
3	VEXSTATAE	0: No interrupt occurrence according to the audio data readout interrupt threshold setting (VSTAT) (initial value) 1: An interrupt occurrence according to the audio data readout interrupt threshold setting (VSTAT)
2	VEXSTAT2	0: No interrupt occurrence to complete reading of Editing data stored in the external flash memory (initial value) 1: An interrupt occurrence to complete reading of Editing data stored in the external flash memory
1	VEXSTAT1	0: No interrupt occurrence to complete reading of event management data stored in the external flash memory (initial value) 1: An interrupt occurrence to complete reading of event management data stored in the external flash memory
0	VEXSTAT0	0: No interrupt occurrence to complete reading of audio data stored in the external flash memory (initial value) 1: An interrupt occurrence to complete reading of audio data stored in the external flash memory

25.2.19 Audio Interrupt Request Clear Register (VEXSTATCLL, VEXSTATCLH)

VEXSTATCLL and VEXSTATCLH are SFR to clears the interrupt status of the audio code data read interrupt and the audio playback function interrupt stored in the external flash memory.

Address: 0xFA22(VEXSTATCLL/VEXSTATCL), 0xFA23(VEXSTATCLH)
Access: W
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	VEXSTATCL															
Byte	VEXSTATCLH								VEXSTATCLL							
Bit	VEXIR	-	-	-	-	-	-	-	-	-	-	VEXSTATCL4	VEXSTATCL3	VEXSTATCL2	VEXSTATCL1	VEXSTATCL0
R/W	W	R	R	R	R	R	R	R	R	R	R	W	W	W	W	W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	description
15	VEXIR	Interrupt request bit 0: Write disabled 1: If there is an unprocessed interrupt factor, the interrupt request is issued again
14 to 5	-	Reserved bits
4	VEXSTATCL4	0: Write disabled 1: Clearing interrupt occurrence status according to the audio status register
3	VEXSTATCL3	0: Write disabled 1: Clearing interrupt occurrence status according to the audio data readout interrupt threshold setting
2	VEXSTATCL2	0: Write disabled 1: Clears the interrupt status of read completion of Editing data stored in external flash memory
1	VEXSTATCL1	0: Write disabled 1: Clears the interrupt status of read completion of event management data stored in external flash memory
0	VEXSTATCL0	0: Write disabled 1: Clears the interrupt status of read completion of audio data stored in external flash memory

25.2.20 Audio Data Readout Address Counter M/L (ADRCNTML0)

ADRCNTML0 is a SFR to indicates the read address of the audio data stored in the external flash memory.
It is updated in synchronized with the sampling frequency.
By reading this register, the progress of readout the audio data can be confirmed.

Address: 0xFA24(ADRCNTL0/ADRCNTML0), 0xFA25(ADRCNTM0)
Access: R
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ADRCNTML0															
Byte	ADRCNTM0								ADRCNTL0							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.21 Audio Data Readout Address Counter H (ADRCNTHH0)

ADRCNTHH0 is a SFR to indicates the read address of the audio data stored in the external flash memory.
It is updated in synchronized with the sampling frequency.
By reading this register, the progress of readout the audio data can be confirmed.

Address: 0xFA26(ADRCNTH0/ADRCNTHH0)
Access: R
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	ADRCNTHH0															
Byte	-								ADRCNTH0							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.22 Audio Data Playback Stop Address Register M/L (CSTPADRML0)

CSTPADRML0 is a SFR to indicates the stop address of the audio data currently being played when audio data stored in the external flash memory is being played.
When reading this register, the address is preserved when reading CSTPADRL0 / CSTPADRML0, so be sure to Read CSTPADRL0/CSTPADRML0 first.

Address: 0xFA28(CSTPADRL0/CSTPADRML0), 0xFA29(CSTPADRM0)
Access: R
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CSTPADRML0															
Byte	CSTPADRM0								CSTPADRL0							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.23 Audio Data playback Stop Address Register H (CSTPADRHH0)

CSTPADRHH0 is a SFR to indicates the stop address of the currently playing the audio data when playing the audio data stored in the external flash memory.
When reading this register, the address is preserved when reading CSTPADRL0 / CSTPADRML0, so be sure to read CSTPADRL0/CSTPADRML0 first.

Address: 0xFA2A(ADRCNTH0/ADRCNTHH0)
Access: R
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CSTPADRHH0															
Byte	-								CSTPADRH0							
Bit	-	-	-	-	-	-	-	-	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.24 Audio Data Readout Store Register n (CH0BUFn: n=0 to 7)

CH0BUFn is a SFR to stores the read data when reading the audio data stored in the external flash memory.
The read audio data can be confirmed.

Address: 0xFA30(CH0BUF0/CH0BUF10), 0xFA31(CH0BUF1)
0xFA32(CH0BUF2/CH0BUF32), 0xFA33(CH0BUF3)
0xFA34(CH0BUF4/CH0BUF54), 0xFA35(CH0BUF5)
0xFA36(CH0BUF6/CH0BUF76), 0xFA37(CH0BUF7)
Access: R
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CH0BUF(n+1,n)															
Byte	CH0BUFn+1								CH0BUFn							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.25 Event Management Readout Store Register n (CH1BUFn: n=0 to 7)

CH1BUFn is a SFR to stores the read data when reading event management data stored in the external flash memory.

Address: 0xFA38(CH1BUF0/CH1BUF10), 0xFA39(CH1BUF1)
0xFA3A(CH1BUF2/CH1BUF32), 0xFA3B(CH1BUF3)
0xFA3C(CH1BUF4/CH1BUF54), 0xFA3D(CH1BUF5)
0xFA3E(CH1BUF6/CH1BUF76), 0xFA3F(CH1BUF7)
Access: R
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CH1BUF(n+1,n)															
Byte	CH1BUFn+1								CH1BUFn							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The data stored is shown in the table below. You can check the read event management data.

Register Name	MSB							LSB
CH1BUF0	H0	P2	P1	P0	S3	S2	S1	S0
CH1BUF1	A23	A22	A21	A20	A19	A18	A17	A16
CH1BUF2	A15	A14	A13	A12	A11	A10	A9	A8
CH1BUF3	A7	A6	A5	A4	A3	A2	A1	A0
CH1BUF4	0	0	0	VOL4	VOL3	VOL2	VOL1	VOL0
CH1BUF5	T23	T22	T21	T20	T19	T18	T17	T16
CH1BUF6	T15	T14	T13	T12	T11	T10	T9	T8
CH1BUF7	T7	T6	T5	T4	T3	T2	T1	T0

H0: Edited/Unedited audio phrase (1: Edit phrase used 0: Edit phrase not used)
P2-P0: Audio synthesis method
S3-S0: Sampling frequency
A23-A0: Audio start address (edit management start address if H0=1)
T23-T0: Audio stop address (edit management stop address if H0=1)
VOL4-VOL0: VOL settings

25.2.26 Editing Data Readout Store Register n (CH2BUFn: n=0 to 7)

CH2BUFn is a SFR to stores the read data when reading Editing data stored in the external flash memory.

Address: 0xFA40(CH2BUF0/CH2BUF10), 0xFA41(CH2BUF1)
0xFA42(CH2BUF2/CH2BUF32), 0xFA43(CH2BUF3)
0xFA44(CH2BUF4/CH2BUF54), 0xFA45(CH2BUF5)
0xFA46(CH2BUF6/CH2BUF76), 0xFA47(CH2BUF7)
Access: R
Access Size: 8bit/16bit
Initial Value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CH2BUF(n+1,n)															
Byte	CH2BUFn+1								CH2BUFn							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The data stored is shown in the table below. You can check the read Editing data.

<M0 bit = "0">

Register Name	MSB							LSB
CH2BUF0	M0	P2	P1	P0	S3	S2	S1	S0
CH2BUF1	A23	A22	A21	A20	A19	A18	A17	A16
CH2BUF2	A15	A14	A13	A12	A11	A10	A9	A8
CH2BUF3	A7	A6	A5	A4	A3	A2	A1	A0
CH2BUF4	0	0	0	VOL4	VOL3	VOL2	VOL1	VOL0
CH2BUF5	T23	T22	T21	T20	T19	T18	T17	T16
CH2BUF6	T15	T14	T13	T12	T11	T10	T9	T8
CH2BUF7	T7	T6	T5	T4	T3	T2	T1	T0

M0: Silence bit (1: Silence insertion 0: Phrase playback)
P2-P0: Audio synthesis method
S3-S0: Sampling frequency
A23-A0: Audio start address
T23-T0: Audio stop address
VOL4-VOL0: VOL settings

<M0 bit = "1">

Register Name	MSB							LSB
CH2BUF0	M0	1	1	1	0	0	0	0
CH2BUF1	F7	F6	F5	F4	F3	F2	F1	F0
CH2BUF2	*	*	*	*	*	*	*	*
CH2BUF3	*	*	*	*	*	*	*	*
CH2BUF4	*	*	*	*	*	*	*	*
CH2BUF5	*	*	*	*	*	*	*	*
CH2BUF6	*	*	*	*	*	*	*	*
CH2BUF7	*	*	*	*	*	*	*	*

M0: Silence bit (1: Silence insertion 0: Phrase playback)
F7-F0: Silence time (4ms~1024ms, 4ms increments)
*: Don't care

The setting formula for silence time is as follows.

$$\text{Silence time} = (2^7 \times (F7) + 2^6 \times (F6) + 2^5 \times (F5) + 2^4 \times (F4) + 2^3 \times (F3) + 2^2 \times (F2) + 2^1 \times (F1) + 2^0 \times (F0) + 1) \times 4\text{ms}$$

25.2.27 Audio FIFO Data Register (VFDAT)

VFDAT is a SFR to stores the audio data.
It is used when the audio code data is placed in the internal flash memory.
The audio data area stores the audio data of each audio synthesis method.

Address: 0xFAB0(VFDAT)
Access: W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VFDAT							
Bit	-	-	-	-	-	-	-	-	VFDAT 7	VFDAT 6	VFDAT 5	VFDAT 4	VFDAT 3	VFDAT 2	VFDAT 1	VFDAT 0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The audio data arrangement format for each audio synthesis method is shown below.

[1] 4-bit ADPCM2
Every 4 bits of data are placed from the MSB side.

Audio Data	MSB	LSB
1st byte	Data1	Data2
2nd byte	Data3	Data4
3rd byte	Data5	Data6
……		

[2] 8-bit straight PCM
The 8-bit data is placed as is.

Audio Data	MSB LSB
1st byte	Data1
2nd byte	Data2
3rd byte	Data3
……	

[3] 16-bit straight PCM
The lower 8 bits of data are followed by the upper 8 bits of data, arranged in 16-bit increments.

Audio Data	MSB LSB
1st byte	Data1(Lower 8 bit)
2nd byte	Data1(Top 8 bit)
3rd byte	Data2(Lower 8 bit)
4th byte	Data2(Top 8 bit)
……	

25.2.28 Audio Phrase End Data Register (VFEDAT)

VFEDAT is a SFR to stores the final data of a phrase.
It is used when the audio code data is placed in the internal flash memory.
Store the data of the last phrase in the register because the data of the last phrase is recognized, and the audio arithmetic circuit is initialized.

Address: 0xFAB2(VFEDAT)
Access: W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VFEDAT							
Bit	-	-	-	-	-	-	-	-	VFEDAT7	VFEDAT6	VFEDAT5	VFEDAT4	VFEDAT3	VEFDAT2	VEFDAT1	VEFDAT0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.29 Audio Status Register (VSTAT)

VSTAT is a SFR to shows the status of each audio playback function.

Address: 0xFAB6(VSTAT)
Access: R
Access Size: 8bit
Initial Value: 0x11

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VSTAT							
Bit	-	-	-	-	-	-	-	-	VERR	-	-	VAEND	VDEND	VFUL	VMID	VEMP
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bit Number	Bit Symbol Name	description
15 to 8	-	Reserved bits
7	VERR	Indicates readout error of audio data. The audio arithmetic circuit reads the audio data written to the FIFO according to the audio synthesis method every sampling period, but if there is readout error of audio data, the VERR bit read "1". Error determination of audio data readout is executed only when the following conditions are satisfied. 16-bit straight PCM :When the audio arithmetic circuit reads out the FIFO audio data in a state of 1 byte 0: No readout error (initial value) 1: Readout error
6, 5	-	Reserved bits
4	VAEND	Indicates that the audio PWM circuit is powering down. When the VCEN bit of the audio playback control register (VCON) is set from "0" to "1", the audio PWM circuit starts operation and then VAEND will be "0". Also, when the VCEN bit is set from "1" to "0", the audio PWM circuit is powered down and then VAEND will be "1. 0: Audio PWM circuit is in operation 1: Audio PWM circuit is in power down (initial value)
3	VDEND	Indicates that the final data is being output from a digital filter. The final data of the audio phrase written to the audio phrase end data register (VFEDAT) is captured into the digital filter and EMPTY When output from a digital filter in its state, the VDEND bit becomes "1".If there is a write operation in the FIFO data register (when it is no longer EMPTY) or when VCEN bit = "0", VDEND is "0". 0: The final data is not being output from the digital filter (initial value) 1: The final data is being output from a digital filter.
2	VFUL	Indicates that the all audio data (32 byte) is filled out (FULL) in the FIFO which stores the audio data. 0: Status of the FIFO ≠ FULL (initial value) 1: Status of the FIFO = FULL
1	VMID	Indicates the status of remaining state (MIDDLE) of the audio data of the FIFO which stores the audio data. The remaining state of the audio data remains in the FIFO as the FIFO interrupt request level set by the FIFO interrupt control register (VMOD). You can set the size of the audio data. 0: Status of the FIFO < MIDDLE 1: Status of the FIFO ≥ MIDDLE
0	VEMP	Indicates that there is no audio data (EMPTY) in the FIFO which stores the audio data. 0: Status of the FIFO ≠EMPTY 1: Status of the FIFO =EMPTY

Interrupts of audio data requests are occurred by the following factors, so readout VSTAT to check the factors of the interrupt request.

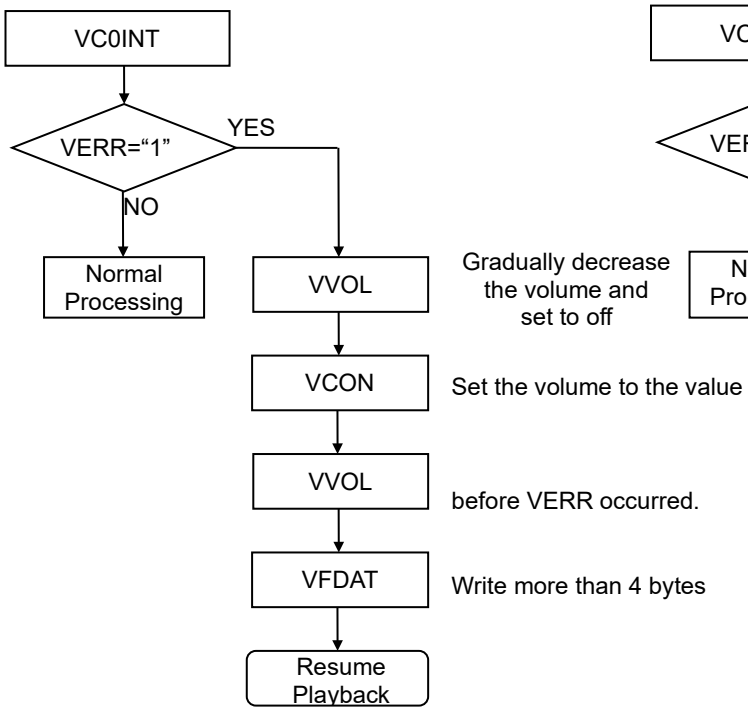
- When the VMID bit change from "1" to "0" (when the audio data in the FIFO is less than the number of bytes specified in VMOD)
- When the VDEND bit change to "1" (when the final data of the audio is output to the digital filter)
- When the VAEND bit change to "1" (audio PWM circuit is in powered down)
- When the VERR bit change to "1" (if there is an audio data readout error)

Write "1" to VEXIEVOI (bit 4) of the audio interrupt enable register (VEXIE), the interrupts is enabled and the interrupt controller is notified. Reset the audio interrupt request status register (VEXSTAT) to "0" at the end of the interrupt process.

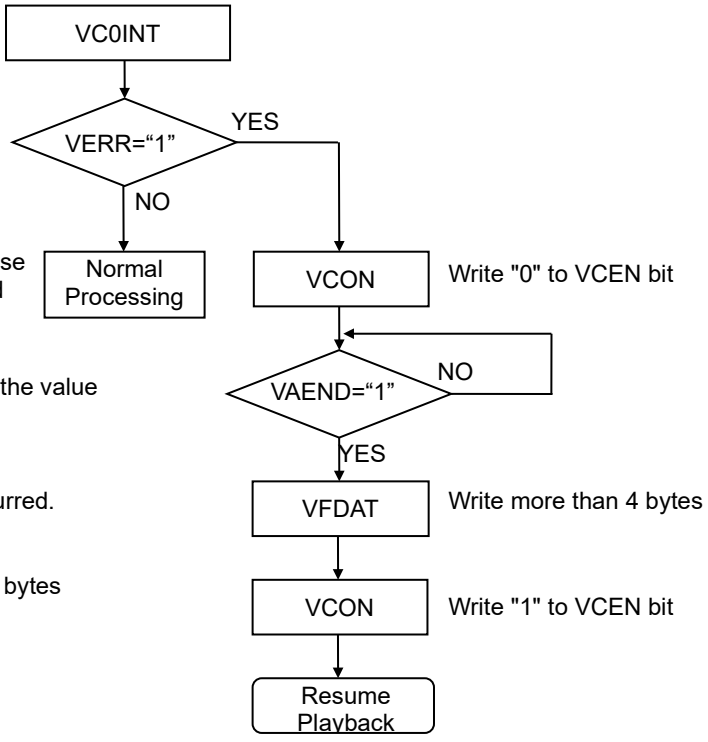
【Note】

- **From writing of VFDAT to VSTAT flag update takes 2 clocks of the audio playback function clock, so execute read confirmation of flag update after placing 4 or more NOP instructions after VFDAT write.**
- **From setting the VCEN from "1" to "0" to SEND becomes 1 takes 2 clocks of the audio playback function clock, so execute read confirmation of flag update after placing 4 or more NOP instructions after VCEN write.**
- **If the VERR becomes "1", execute the following process (1) or (2).**

(1) Processing by VSTP Bit in VCON
Initialize the FIFO and arithmetic circuitry with audio PWM circuitry powered up



(2) Processing by VCEN Bit in VCON
Resume from audio power-up processing with audio PWM circuitry powered down



25.2.30 Audio Mode Register (VMOD)

VMOD is a SFR to set Audio Mode.

Address: 0xFAB8(VMOD)
Access: R/W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VMOD							
Bit	-	-	-	-	-	-	-	-	VVOLPS	-	-	-	-	-	VFMD1	VFMD0
R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	description
15 to 8	-	Reserved bit
7	VVOLPS	Selects the timing when the settings of the volume setting register (VVOL) are reflected. When "0" is set, the VVOL setting value is reflected in the playback sound immediately. When "1" is set, the VVOL setting value is reflected synchronously with the timing of the start of phrase playback Even if VVOL setting is changed during audio playback, it will not be reflected in the playback sound. During continuous playback, it is used to change the volume synchronously with subsequent playback of the next phrase data(the next data of the data written to VFEDAT). 0: reflect the set value of the volume setting register (VVOL) immediately (initial value) 1: reflect the setting value of the volume setting register (VVOL) synchronously to the start of phrase playback.
6 to 2	-	Reserved bits
1, 0	VFMD1, VFMD0	Selects the number of bytes remaining as the number of bytes remaining in the FIFO to store the audio data is set to the interrupt request level. When the audio data in the FIFO is less than the remaining number of bytes specified in VFMD1 and VFMD0, the VMID bit in the Audio Status Register (VSTAT) becomes "0". 00: 1byte(initial value) 01: 10byte 10: 4byte 11: 8byte

25.2.31 Audio Data Type Register (VTYPE)

VTYPE is a SFR to set the audio synthesis method and sampling frequency.

Address: 0xFABA(VTYPE)
Access: R/W
Access Size: 8bit
Initial Value: 0x41H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VTYPE							
Bit	-	-	-	-	-	-	-	-	-	VSYN2	VSYN1	VSYN0	VSMP3	VSMP2	VSMP1	VSMP0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bit Number	Bit Symbol Name	description
15 to 7	-	Reserved bits
6 to 4	VSYN2 to VSYN0	Select the audio synthesis method (4-bit ADPCM2,8-bit non-linear PCM,8-bit straight PCM, and 16-bit straight PCM).

setting	audio synthesis method
000	Unavailable
001	4bit ADPCM2
010	8bit Non-linear PCM
011	8bit straight PCM
100	16bit straight PCM (initial value)
101	Unavailable
110	Unavailable
111	Unavailable

Bit Number	Bit Symbol Name	description
3 to 0	VSMP3 to VSMP0	Select the sampling frequency.

setting	sampling frequency
0000	Unavailable
0001	7.81kHz (initial value)
0010	15.63kHz
0011	31.25kHz
0100	Unavailable
0101	10.42kHz
0110	20.83kHz
0111	Unavailable
1000	6.25kHz
1001	12.50kHz
1010	25.00kHz
1011	Unavailable
11XX	Unavailable

X: 0/1 Either one

25.2.32 Volume Settings Register (VVOL)

VVOL is a SFR to set the volume value.

Address: 0xFABC (VVOL)
Access: R/W
Access Size: 8bit
Initial Value: 0x09

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VVOL							
Bit	-	-	-	-	-	-	-	-	-	-	-	VVOL4	VVOL3	VVOL2	VVOL1	VVOL0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit Number	Bit Symbol Name	description
7 to 5	-	Reserved bits
4 to 0	VVOL4 to VVOL0	Select volume.

Setting	Volume [dB]	Setting	Volume [dB]
00000	+2.98	10000	-3.34
00001	+2.70	10001	-3.94
00010	+2.40	10010	-4.58
00011	+2.10	10011	-5.28
00100	+1.78	10100	-6.04
00101	+1.45	10101	-6.87
00110	+1.11	10110	-7.79
00111	+0.76	10111	-8.82
01000	+0.39	11000	-9.99
01001	+0.00 (initial value)	11001	-11.34
01010	-0.41	11010	-12.94
01011	-0.83	11011	-14.90
01100	-1.28	11100	-17.44
01101	-1.75	11101	-21.04
01110	-2.25	11110	-27.31
01111	-2.77	11111	Off

25.2.33 Audio Playback Control Register (VCON)

VCON is a SFR to controls audio playback.

Address: 0xFABE (VCON)
Access: R/W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	VSTP	-	-	-	VCEN
R/W	R	R	R	R	R	R	R	R	R	R	R	W	R	R	R	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	description
7 to 5	-	Reserved bits
4	VSTP	Control playback stop during audio playback. When "1" is written to VSTP, audio playback stop and the audio calculation result is fixed at 0000H. And also the FIFO is cleared. Note that write "1" to VSTP five times in a row. When audio code data is placed in the internal flash memory and playback is resumed and in use., store at least 4 bytes of audio data in the FIFO data register (VFDAT). When placing audio code data in the internal flash memory and resuming playback, store at least 4 bytes of audio data in the FIFO data register (VFDAT). When using audio code data by placing it in an external flash memory, write "1" to the VEXSTP0 bit of the audio read request register (VEXCONT) five times in a row, stop reading the audio data, and then set VSTP. Check that the reading of the audio data has stopped by reading the VEXCNT0 bit. To resume, reset the audio playback function with bit 12 of the block reset control register 2 (BRECON2), set the next playback setting, and resume. In case not to reset the audio playback function, configure the application to write "1" in the VEXCNT0 bit with VCEN=1 and make a read request after the sampling frequency*1 cycle or more has elapsed.
3 to 1	-	Reserved bits
0	VCEN	Controls stop/start of the audio playback function. 0: Stop operation of the audio playback function (initial value) 1: Start operation of the audio playback function

25.2.34 Volume Status Register (VVOLS)

VVOLS is a SFR to indicates the status of the VVOL reflected during audio playback.

Address: 0xFAD0(VVOLS)
Access: R
Access Size: 8bit
Initial Value: 0x09

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								VVOLS							
Bit	-	-	-	-	-	-	-	-	-	-	-	VVOLS 4	VVOLS 3	VVOLS 2	VVOLS 1	VVOLS 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Depending on VVOLPS setting of the audio mode register (VMOD), the value that can be read by VVOLS changes. If VOLPS is set to "0", the same value as the volume setting register (VVOL) can be read. When VVOLPS is set to "1", the following states can be seen when comparing VVOLS and VVOLS readout values.

VVOLPS	description
0	The same value of VVOL can be read from VVOLS (initial value)
1	In case VVOL value matches to the VVOLS readout: VVOL settings is reflected to the audio playback. In case VVOL value does not match to VVOLS readout: VVOL settings is not yet refracted to the audio playback. The next audio playback has not yet begun.

25.2.35 Audio PWM Control Register (SPCON)

SPCON is a SFR to controls audio PWM.

Address: 0xFAC8(SPCON)
Access: R/W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SPCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SPGAIN	SPEN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	Explanation
7 to 2	-	Reserved bits
1	SPGAIN	Selects the input gain value of a delta-sigma D/A converter. When SPGAIN is set to "1", the modulation efficiency of the delta-sigma D/A converter is increased to 100%, but the sound quality is slightly deteriorated. 0: Gain x1(initial value) 1: Gain x1.11
0	SPEN	Controls the audio PWM output. When outputting audio PWM output from the P61/P62 pins, set this bit to "1" and set the P61/P62 pins to the sixth function. 0: Audio PWM: No output (initial value) 1: Audio PWM: Output

25.2.36 PWM Fixed Sense Control Register for Audio (SDCON)

SDCON is a SFR to controls the "H" level fixed detection circuit of PWM.

Address: 30xFAE0(SDCON)
Access: R/W
Access Size: 8bit
Initial Value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								SDCON							
Bit	-	-	-	-	-	-	-	-	SDF	-	-	-	SDD2	SDD1	SDD0	SDEN
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol Name	Explanation
7	SDF	Judgment result flag of the PWM "H" level fixed detection circuit. It is "1" when PWM "H" level fixed is detected, and "0" when PWM "H" level fixed is not detected. When SDF="1", an audio PWM fixed detection interrupt occurs, and the audio output pin (P61/P62 pin) is set to Hi-Z. 0: PWM "H" level fixed is not detected (initial value) 1: PWM "H" level fixed is detected
6 to 4	-	Reserved bits
3 to 1	SDD2 to SDD0	Set the fixed detection time of the PWM "H" level. 000: 62.5µs (initial value) 001: 125µs 010: 250µs 011: 500µs 100: 1ms 101: 2ms 110: 4ms 111: "H" level fixed detection off
0	SDEN	Controls on/off of the PWM "H" level fixed detection circuit. When SDEN is set to "1", the PWM "H" level fixed detection circuit is turned on, and when it is set to "0", it is turned off. 0: PWM "H" level fixed detection circuit is off (initial value) 1: PWM "H" level fixed detection circuit is on

【Note】

- **Fixed detection circuitry works during audio playback. The register settings for audio playback are shown below. When SPEN="1" and VCEN="1", the PWM "H" level fixed detection circuit is enabled.**

Register Name	SPCON Register(Address:0xFAC8)							
Bit	7	6	5	4	3	2	1	0
Bit Name	-	-	-	-	-	-	SPGAIN	SPEN
Setting Value	*	*	*	*	*	*	*	1

Register Name	VCON Register(Address:0xFABE)							
Bit	7	6	5	4	3	2	1	0
Bit Name	-	-	-	VSTP	-	-	-	VCEN
Setting Value	*	*	*	*	*	*	*	1

25.2.37 PWM Output Waveform Mode Register for Audio (DSGMOD)

DSGMOD is a SFR to controls PWM output waveforms for audio.

Address: 0xFAE4（DSGMOD）
Access: R/W
Access Size: 8bit
Initial Value: 0x02

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								DSGMOD							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	DSGMD1	DSGMD0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit Number	Bit Symbol Name	description
7 to 2	-	Reserved bits
1	DSGMD1	Select the output mode of the delta-sigma D/A converter. Select according to the speaker amplifier and the filter to be connected to the outside. 0: Delta-sigma D/A converter 5-value output mode 1: Delta-sigma D/A converter 17-value output mode (initial value)
0	DSGMD0	Selects the output mode of the audio PWM. 0: PWM3 value output mode: Output from 1/2VDD to SOP on the + side, output on the - side to SON (initial value) 1: PWM2 value output mode: outputs the inverting output of SOP to SON

25.3 Description of Operation

25.3.1 Audio playback behavior when audio code data is placed in the internal flash memory

When the VCEN bit of the audio playback control register (VCON) register is set to "1", the delta-sigma D/A converter enters the operating state and starts audio synthesis arithmetic processing and audio data request interrupt operations. When there are 4 or more bytes of audio data to be calculated in the FIFO data register (VFDAT) with VCEN bit = "1", the calculation starts according to the audio synthesis method and volume selected in the audio data type register (VTYPE) and volume setting register (VVOL).
An audio data request interrupt (VC0INT) occurs when there is fewer audio data than the interrupt request level set by the voice mode register (VMOD). In addition, after storing the final data of the phrase in the FIFO phrase end data register (VFEDAT), the FIFO becomes EMPTY when the final data is imported into the audio arithmetic circuit. When the final data is output from the digital filter in the EMPTY state, an audio data request interrupt occurs, and the VDEND bit of the audio status register (VSTAT) becomes "1".

Also, store the final data of the audio phrase in VFEDAT to recognize it. When the audio arithmetic circuit is initialized after the final data calculation, and at the same time there are 4 bytes or more of audio data to be calculated in the VFDAT, the speech synthesis method and sampling frequency stored in the audio data type register (VTYPE) are updated and playback is resumed. At this time, if you want to reflect the VVOL setting value synchronously with the start of playback of the next phrase, set the VVOLPS of the VMOD register to "1".If it is "0", the VVOLS setting value is reflected immediately.

Figure 25-3 shows audio playback flowchart, Figure 25-4 shows continuous playback flowchart, Figure 25-5~6 shows the operation timing of audio playback, and Figure 25-7~8 shows the audio power-up/power-down timing.

【Note】

- **When operating at sysclk=24MHz, do not write to VFDAT/VFEDAT consecutively and place two or more NOP instructions to avoid erroneous writing to the Audio FIFO.**

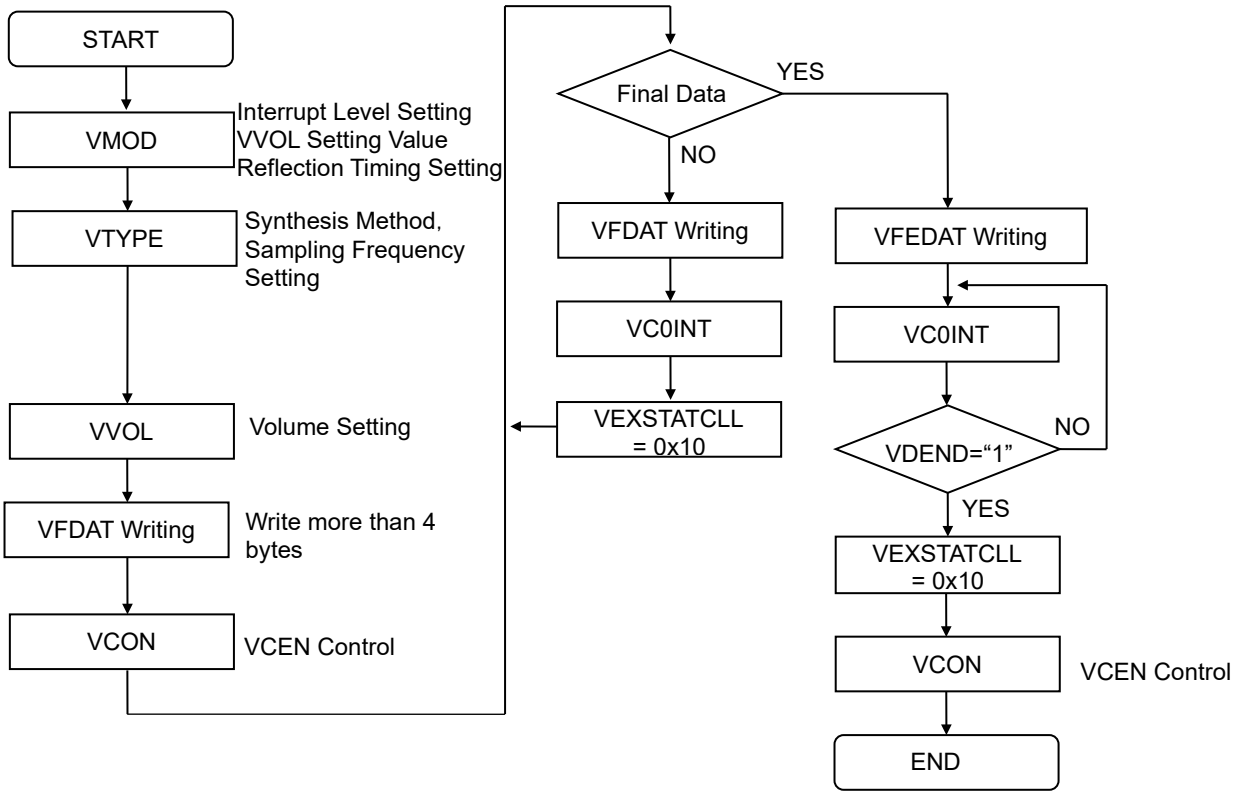
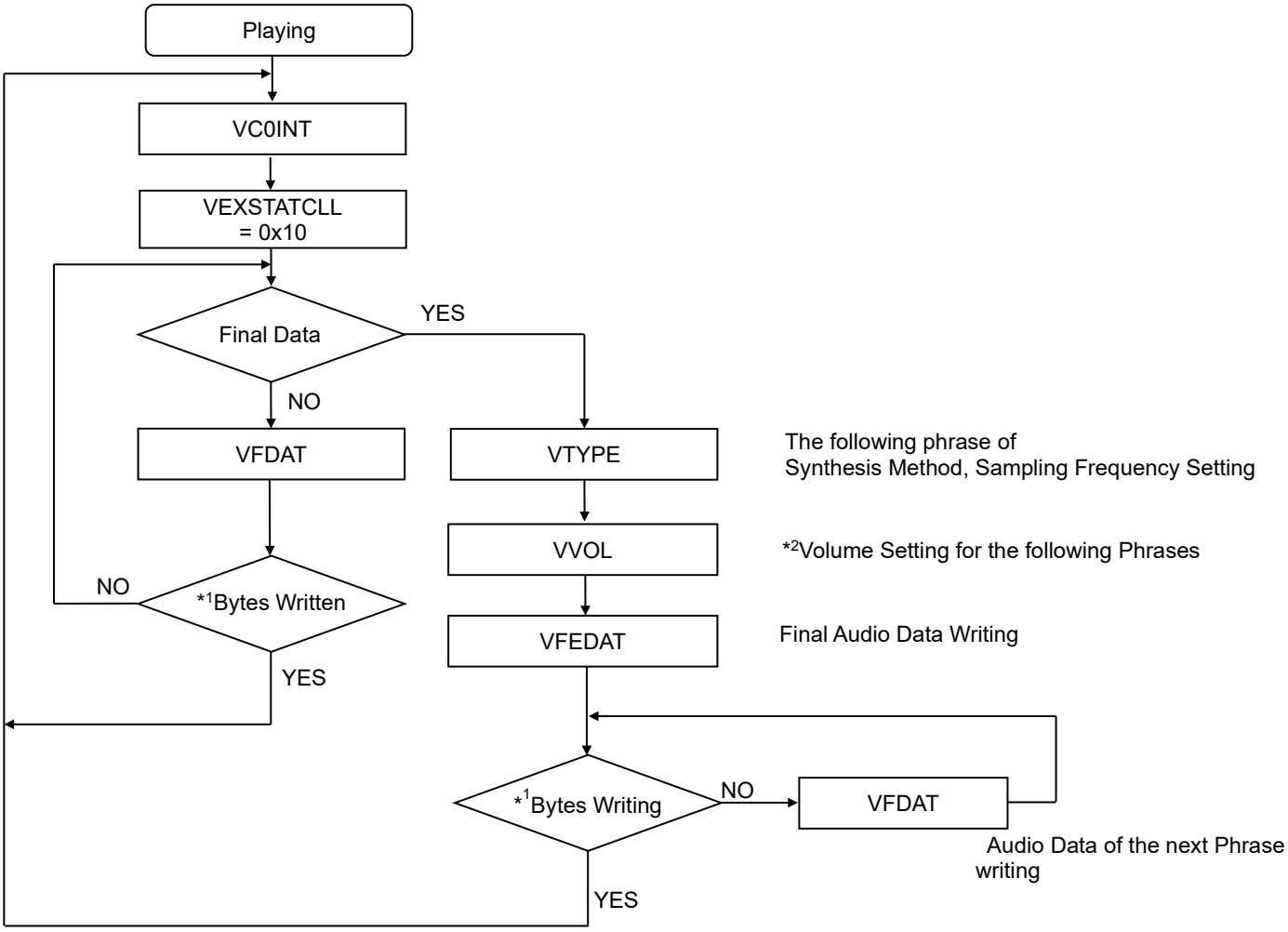


Figure 25-3 Flowchart of Audio Playback



*1 Select the number of bytes to be written according to the capacity of the FIFO and the FIFO interrupt request level set by VFMD1 and VFMD0 in the VMOD register.
*2 If VVOL setting value to be reflected in sync with the start of playback of the next phrase, set the VVOLPS of the VMOD register to "1". If it is "0", the VVOL setting value is reflected immediately.

Figure 25-4 Flowchart of Continuous Playback

25.3.2 Audio Playback Operation Timing

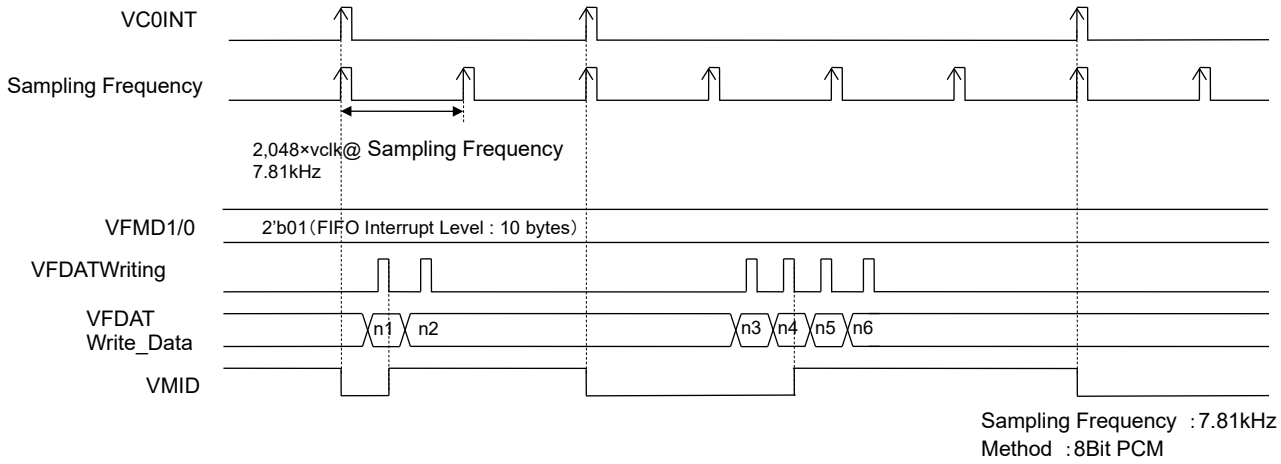


Figure 25-5 Basic Operation Timing of Audio Playback

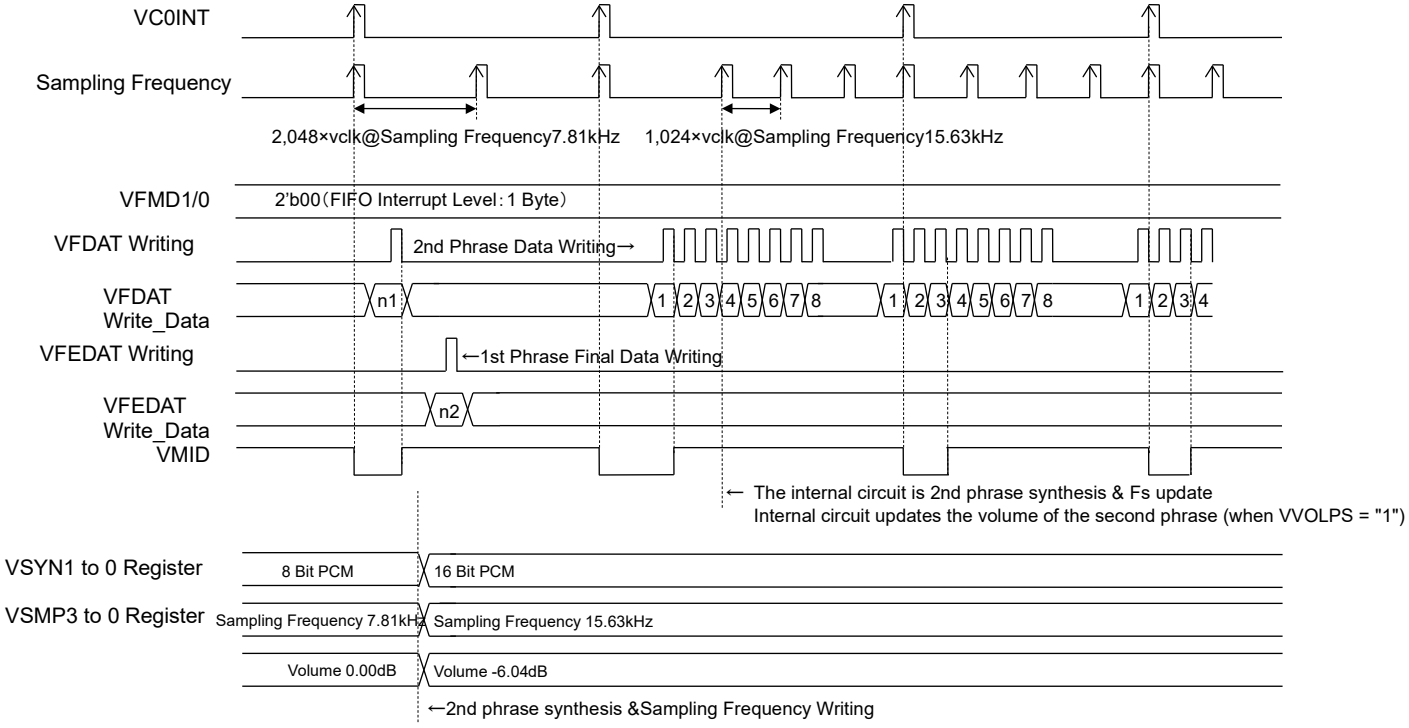


Figure 25-6 Operation Timing of Continuous Playback

【Note】

- **Store the final data of the 1st phrase in the FIFO phrase end data register (VFEDAT).**

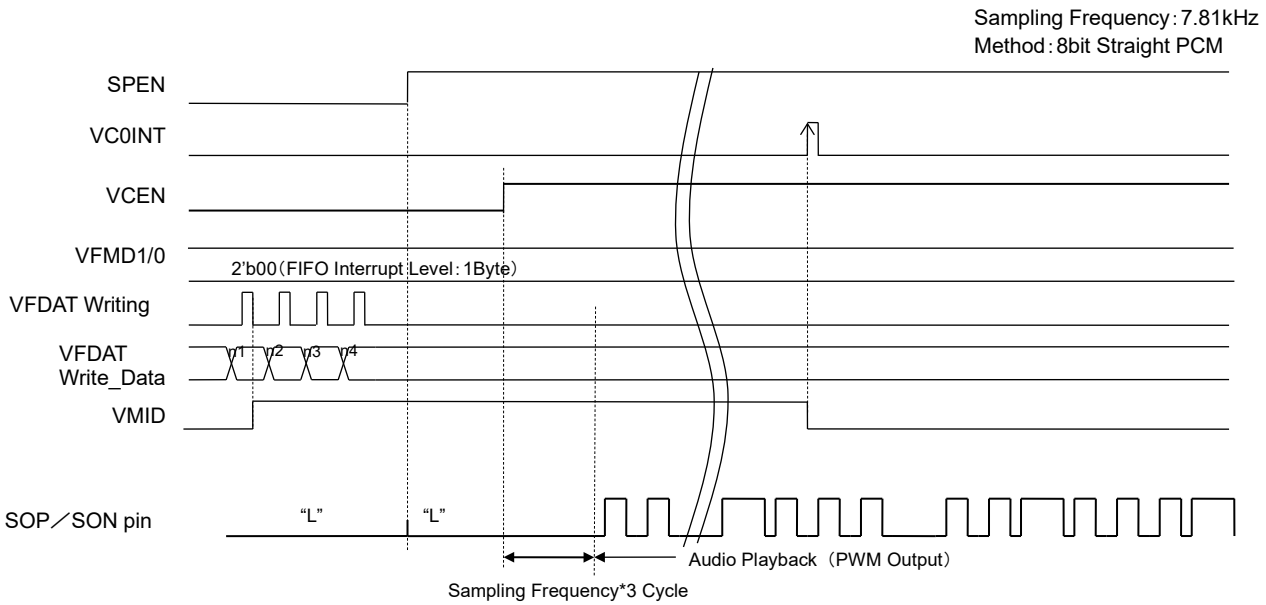


Figure 25-7 Audio PWM Circuit Operation Start Timing

When the SPEN bit of the audio PWM control register (SPCON) is set to "1" and VCEN bit of the audio playback control register (VCON) is set to "1", and there are 4 or more bytes of audio data to be calculated in the FIFO audio data register (VFDAT) after the sampling frequency 3 cycles have elapsed, the audio data type register (VTYPE) is displayed. Start the calculation according to the speech synthesis method selected in (start the calculation sequentially from n1 in the Figure 25-7).

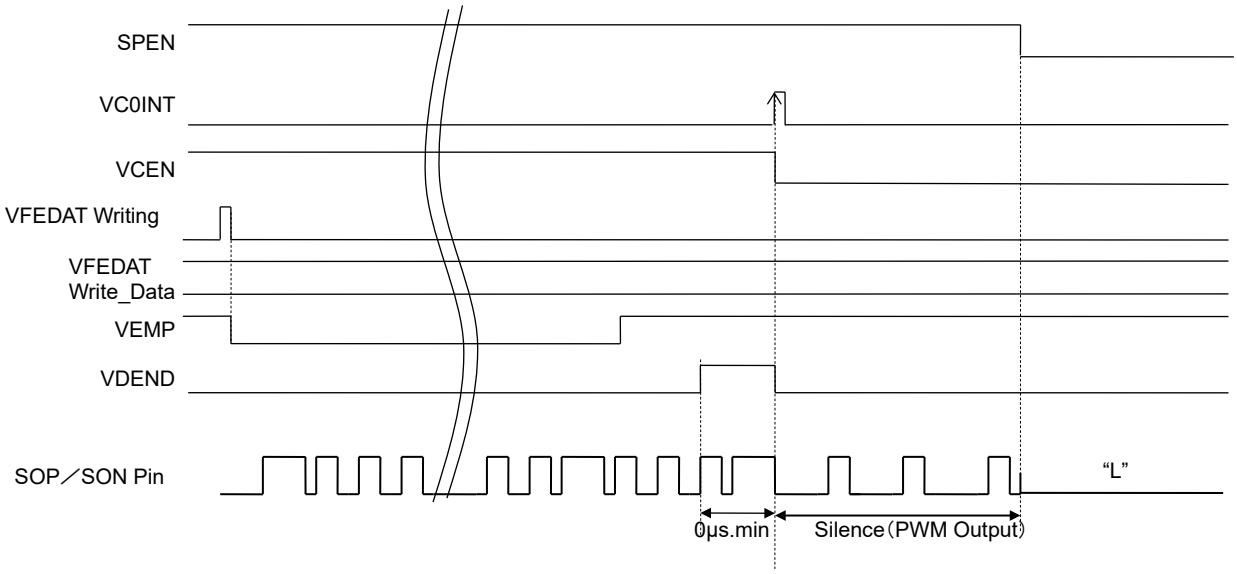


Figure 25-8 Audio PWM Circuit Shutdown Timing

Write the final data to the FIFO phrase end data register (VFEDAT), set VDEND bit of the FIFO status register (VSTAT) to "1", and then set VCEN bit of the audio playback control register (VCON) to "0".

25.3.3 Audio Playback Behavior when Audio Code Data is placed in External Flash Memory

Figure 25-9 shows a flowchart of audio playback when audio code data is placed in an external flash memory, and Figure 25-10 shows a flowchart of continuous playback.
The audio data in the specified address range is read from the external flash memory and automatically transferred to the audio FIFO, which is different from the case where the audio code data is placed in the internal flash memory.
Other audio arithmetic processing is same.
Set the P14 to P16 pins and P50 to P53 pins of the general-purpose port to the 7th function to enable the interface with the external flash memory.
In addition, P61 pin and P62 pin of the general-purpose port are set to the 6th function and enable audio PWM output.
Set VCEN bit of the audio playback control register (VCON) to "1".
Set the event management start address register (STAADRH1/M1/L1) and the event management stop address register (STPADRH1/M1/L1) to read the audio information to be played from the event management area (audio management area).
After that, when VEXCNT1 bit of the audio read request register (VEXCONT) is set to "1", the data reading of the external flash memory starts from the address set in the event management start address register (STAADRH1/M1/L1) in synchronization with the sampling frequency.
The read data is stored in the event management read store register (CH1BUFn:n=0 to 7) every single byte.
When the read data reaches the address set in the event management stop address register (STPADRH1/M1/L1), VEXCNT1 bit of the voice read request register (VEXCONT) becomes "0", and a read completion interrupt of the event management data occurs.
Since bit 7 of CH1BUF0 register stores information on whether or not to use editing data, if it is "1", set the editing data start address register (STAADRH2/M /L2) and the editing data stop address register (STPADRH2 / M2 / L2), and set VECCNT2 bit of the voice reading request register (VEXCONT) to "1", start reading data from the Editing data area (Edit ROM area).
When the address set in the Editing data stop address register ((STPADRH2/M2/L2) is reached, bit 2 of the voice read request register becomes "0", and an Editing data read completion interrupt occurs.
At this time, the read data is stored in the Editing data read store register (CH2BUFn: n=0 to 7).

Read each information of the audio data from the event management read store register (CH1BUFn: n=0 to 7) or the Editing data read store register (CH2BUFn: n=0 to 7), and set the corresponding register as follows.

- Read the start address information of the audio data and set it to the audio data start address register (STAADRH0/M0/L0).
- Read the stop address information of the audio data and set it to the audio data stop address register (STPADRH0/M0/L0).
- Read the audio synthesis method and sampling frequency information and set them to the audio data type register (VTYPE).
- Read the VOL setting information and set it in the volume setting register (VVOL).

After each setting is completed, set VEXCNT0 bit of the audio read request register (VEXCONT) to "1". Synchronous with the sampling frequency, starts reading data from the external flash memory from the address set in the audio data start address register (STAADRH0/M0/L0), and playback audio while writing to the audio FIFO.
When the readout reaches the address set in the audio data stop address register (STPADRH0 / M0 / L0) and VEXMODL bit of the audio playback mode register (VEXMOD) is "0", VEXCNT0 bit of the audio read request register (VEXCONT) becomes "0" and the read ends, an audio data read completion interrupt occurs.
In case VEXMODL bit of the audio playback mode register (VEXMOD) is "1", VEXCNT0 bit of the audio readout request register (VEXCONT) stay "1" and the readout continues. An audio data read completion interrupt occurs in the sense that the readout of one phrase is completed.
If the audio data start address register is updated, data reading from that address continues.
If the audio data start address register has not been updated, data reading from the same address continues.
An interrupt can be occurred before the audio data read is completed by setting the audio data read interrupt threshold register (VEXAE).
By using each interrupt to read the audio information from the event management area (audio management area) and the editing data area (edit ROM area), update the audio data, and continue audio playback.

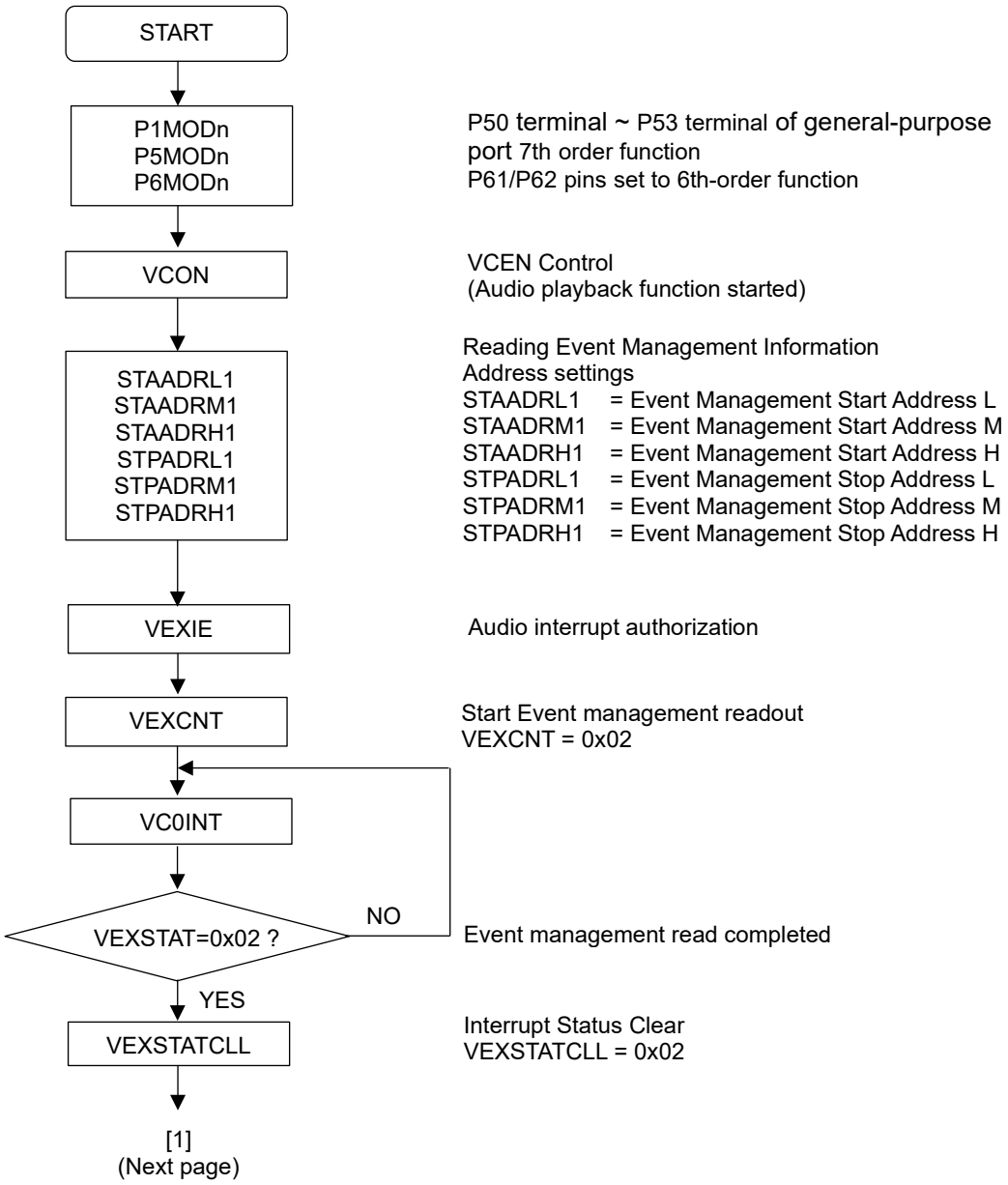


Figure 25-9 Audio Playback Flowchart (In case audio code data is placed in external flash memory)

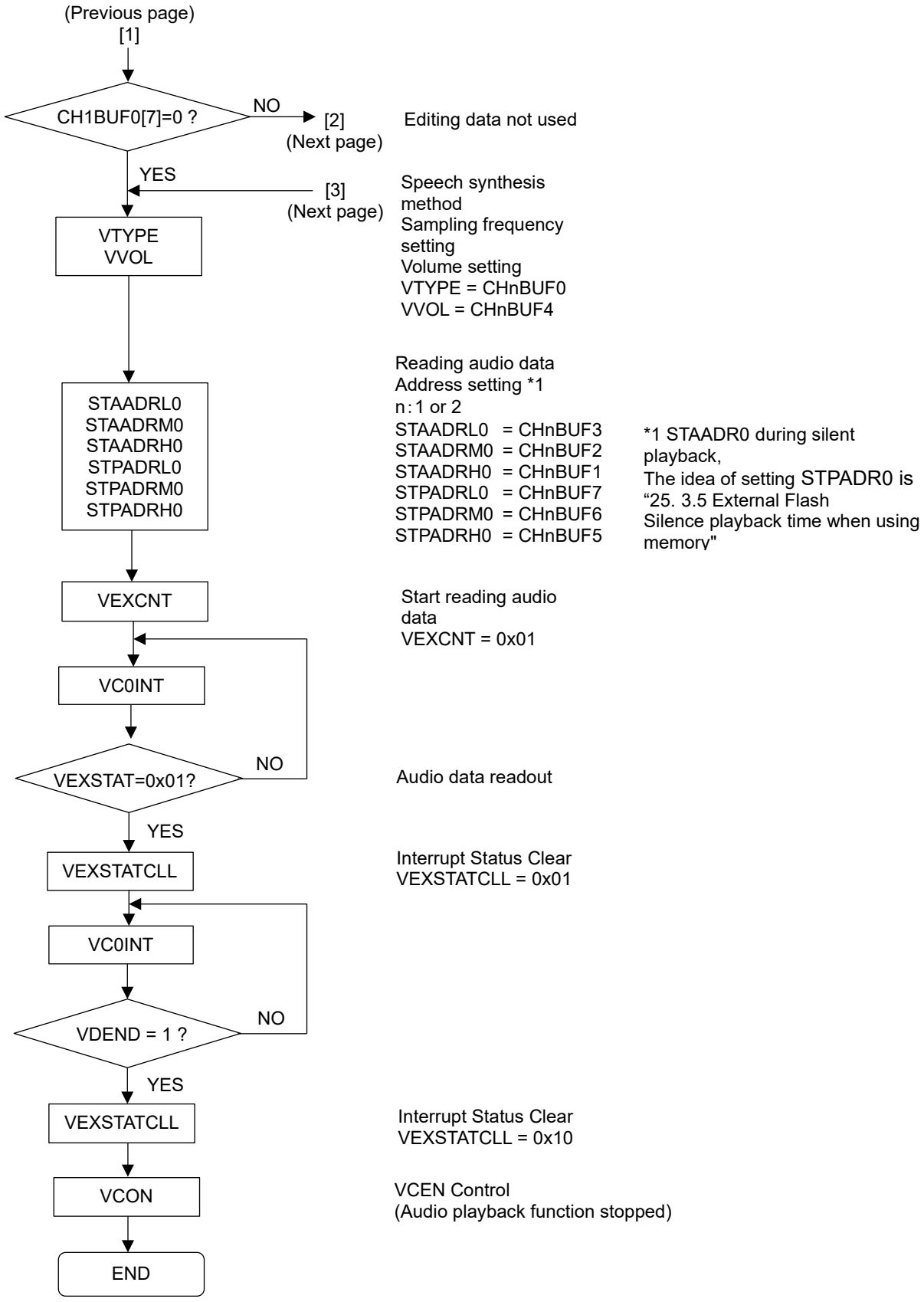


Figure 25-9 Flowchart of Audio Playback (In case audio code data is placed in external flash memory)

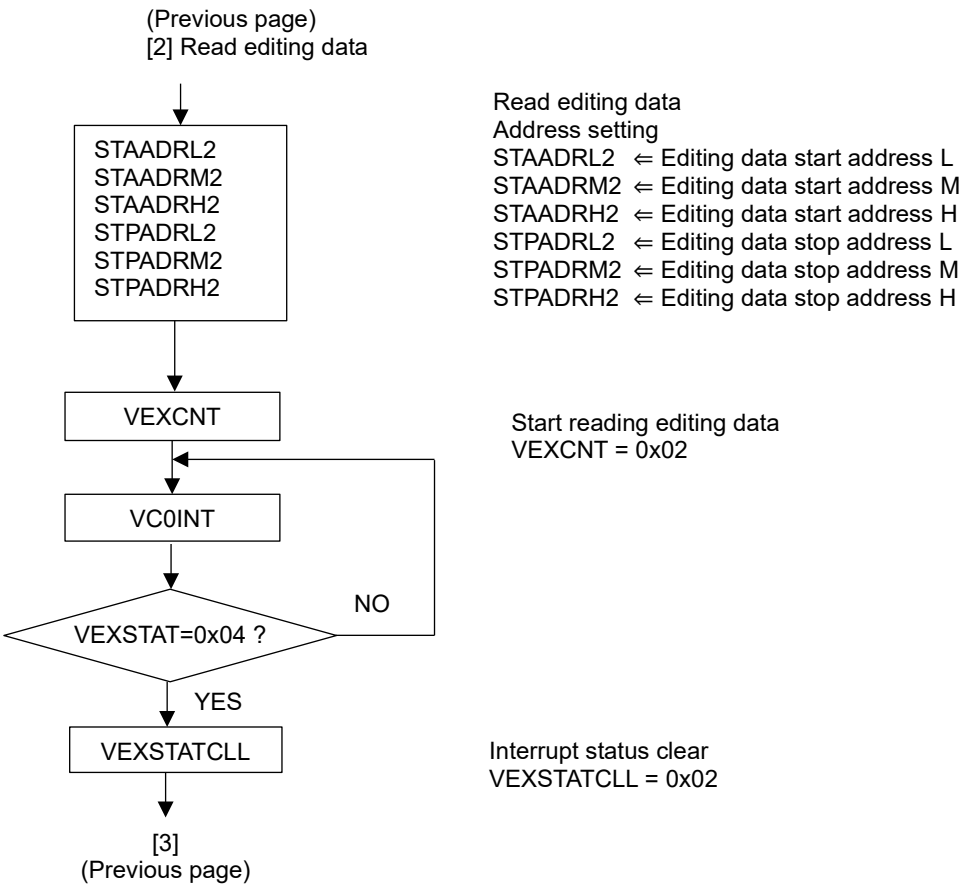
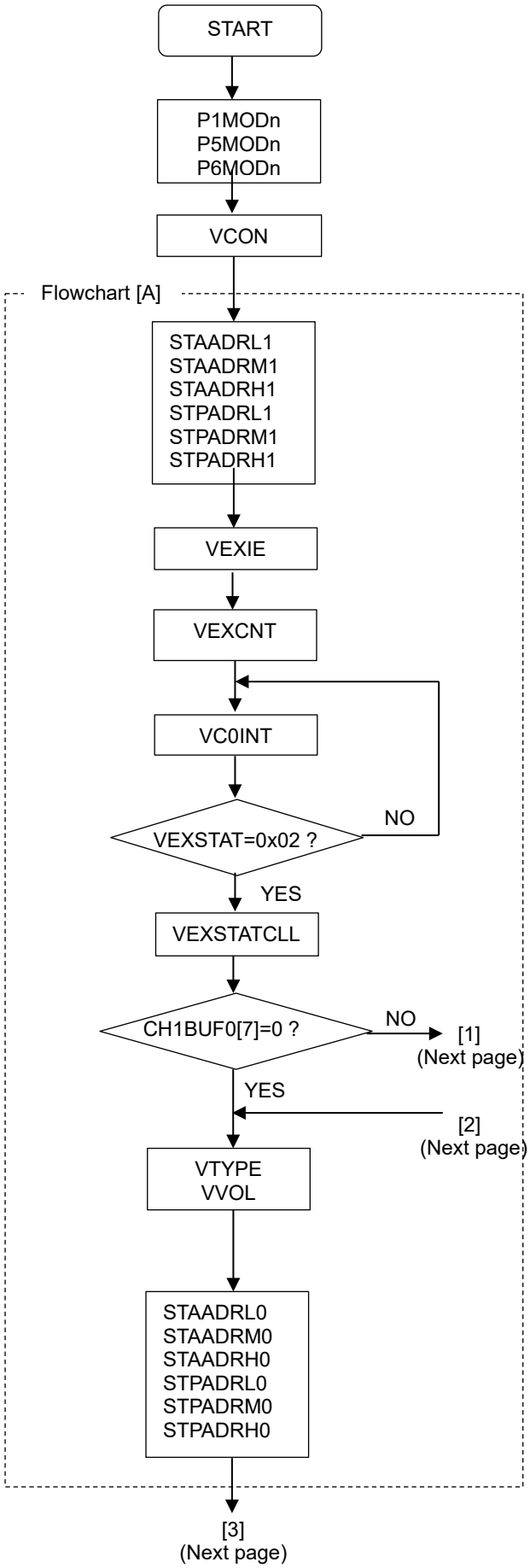


Figure 25-9 Flowchart of Audio Playback (In case audio code data is placed in external flash memory)



Relevant pins for P14 ~ P16 or P50 ~ P53 set to 7th order function
P61/P62 pins set to sixth-order function

VCEN Control
(Audio playback function started)

Retrieving Event management information address setting
STAADRL1 = Event management start address L
STAADRM1 = Event management start address M
STAADRH1 = Event management start address H
STPADRL1 = Event management stop address L
STPADRM1 = Event management stop address M
STPADRH1 = Event management stop address H

Audio interrupt authorization

Event management readout started
VEXCNT = 0x02

Event management readout complete

Interrupt status clear
VEXSTATCLL = 0x02

Editing data not used

Speech synthesis method,
Sampling frequency setting
Volume settings
VTYPE = CHnBUF0
VVOL = CHnBUF4

Reading audio data
Address setting *1
n : 1 or 2
STAADRL0 = CHnBUF3
STAADRM0 = CHnBUF2
STAADRH0 = CHnBUF1
STPADRL0 = CHnBUF7
STPADRM0 = CHnBUF6
STPADRH0 = CHnBUF5

*1 STAADR0 during silent playback,
The idea of setting STPADR0 is 25.3.5 External Flash Silence playback time when using memory" See

Figure 25-10 Flowchart of continuous playback

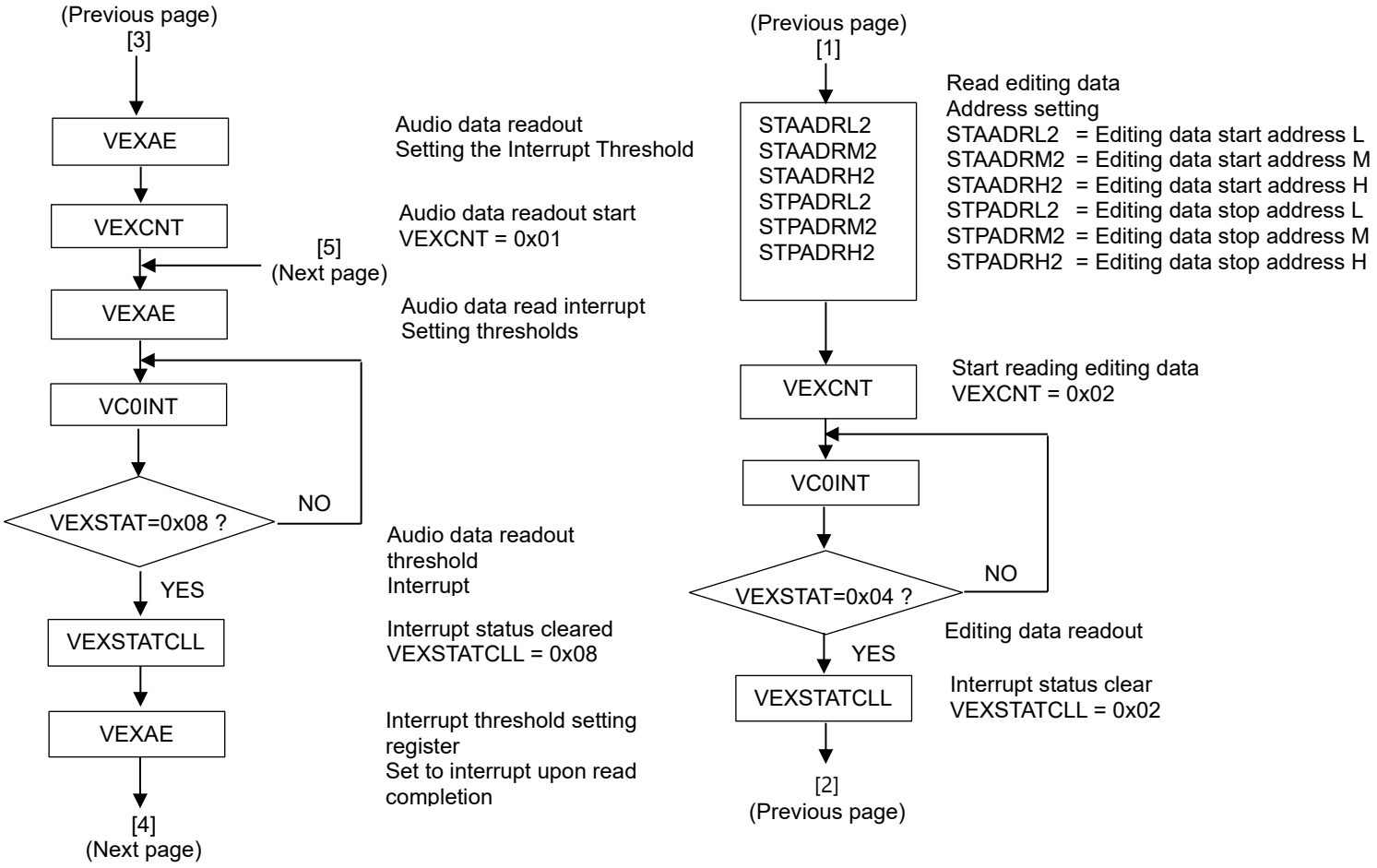


Figure 25-10 Flowchart of continuous playback

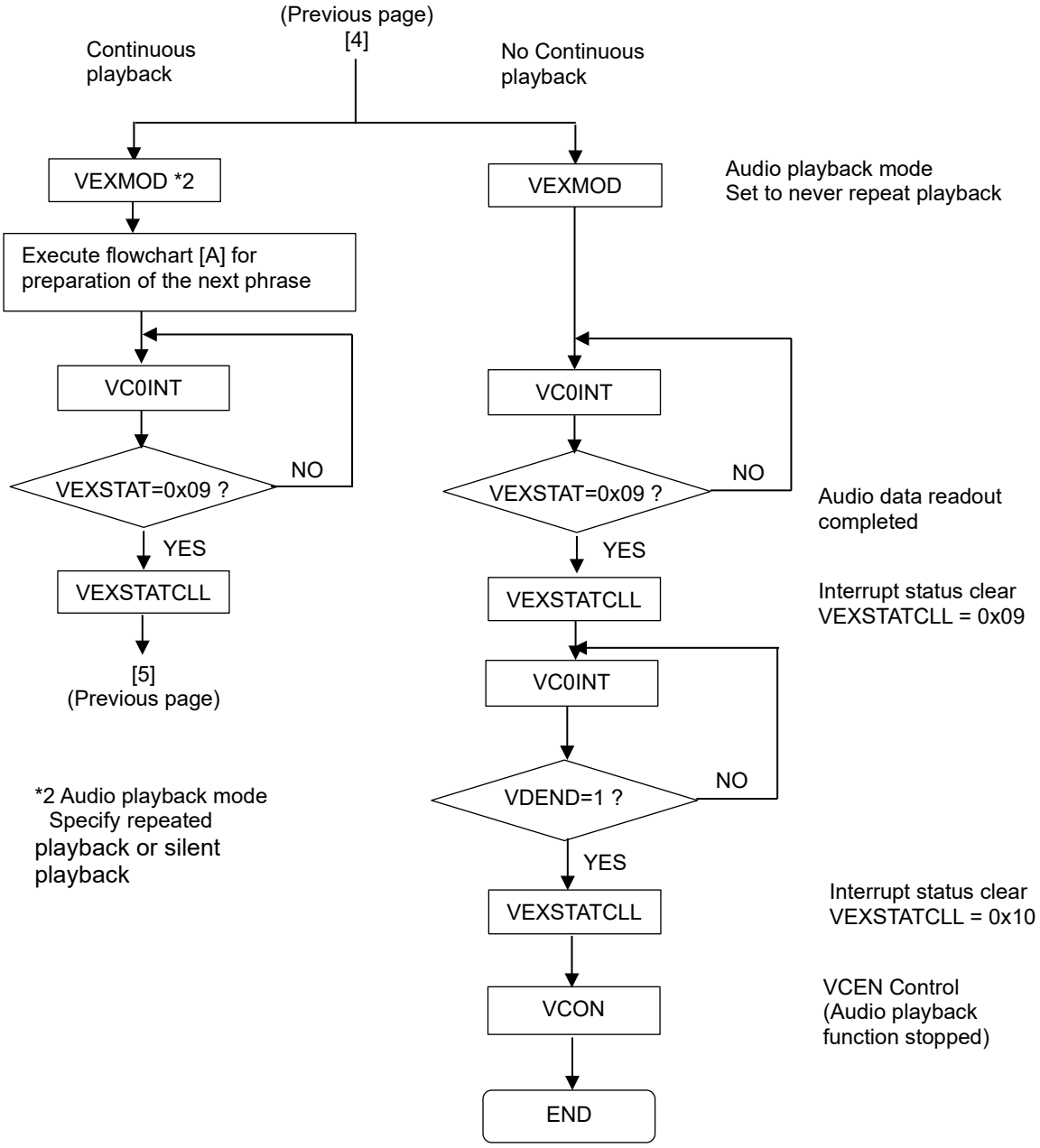
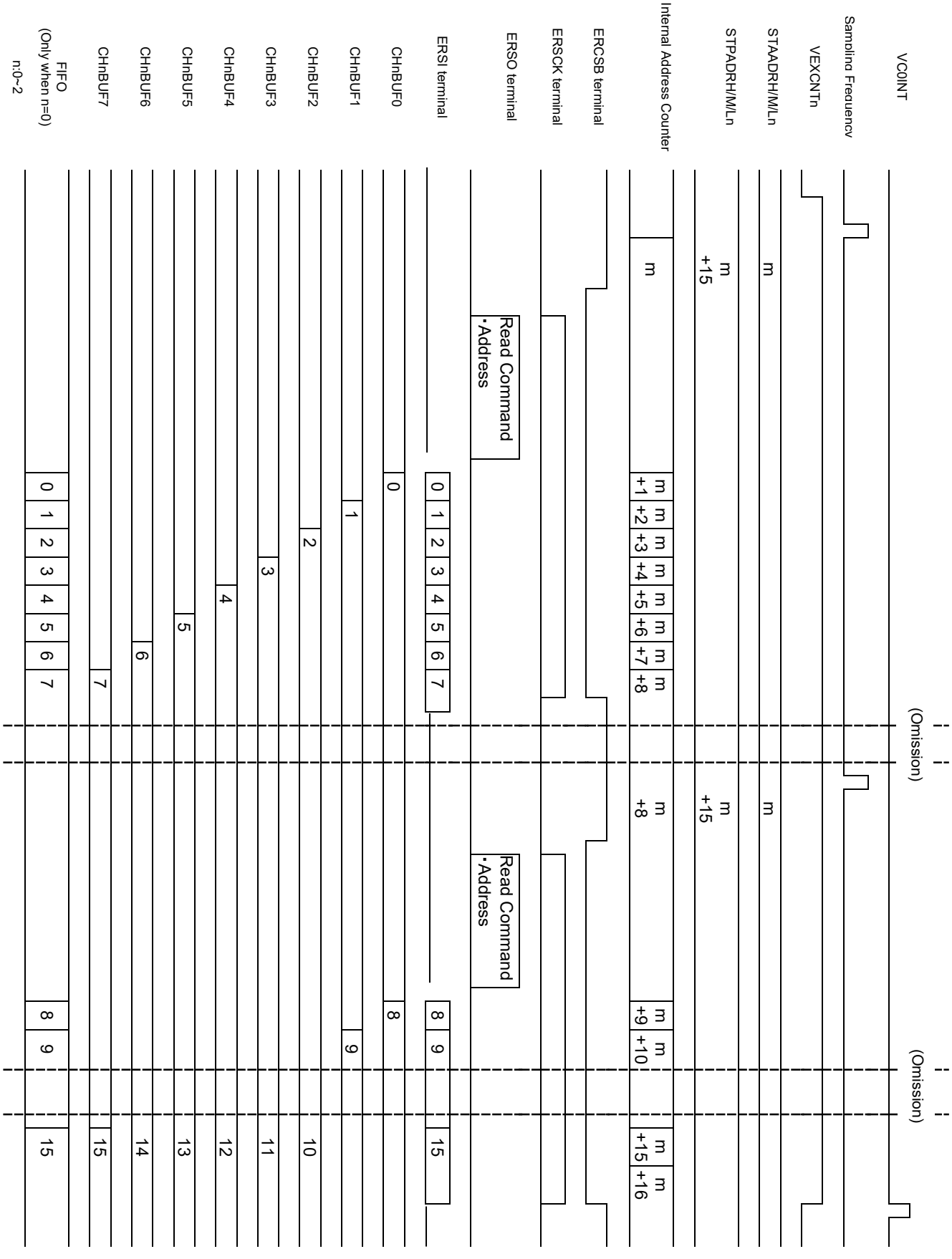


Figure 25-10 Flowchart of continuous playback

25.3.4 Basic operation of automatic transfer when using external flash memory



25.3.5 Silence playback time when using external flash memory

Set the silence playback time in the audio data start address register (STAADRH0/M0/L0) and the audio data stop address register (STPADRH0/M0/L0).
In case VEXMODM bit of the audio playback mode register (VEXMOD) is set to "1", readout the data specified by the audio data start address register (STAADRH0/M0/L0) and the audio data stop address register (STPADRH0/M0/L0), and silent playback is executed during audio is playing.

The following describes the concept of setting with a sampling frequency of 7.81kHz and an 8bit PCM.
In case 4ms silence time is set, the period of the sampling frequency of 7.81kHz will be 128μs, so it is correspond to 4ms÷128μs=31.25sampling frequencies. In the case of 8bit PCM, audio data is processed one byte at a time, so set the setting to read 32 bytes of audio data.
Therefore, if readout audio data by setting audio data start address register = 0x0000 and setting audio data stop address register =0x001F, the silent playback period is 4ms.
In addition, the following describes how to set with a sampling frequency of 7.81kHz and 8bit PCM the silence time specified in the editing area in the audio code data.

```
    MOV     Rk,         #00H
    MOV     Rl,         #01H
    MOV     Rm,         #20H
    MOV     Rm+1,       #00H
    MOV     Rn+1,       #00H
    MOV     Rn,         CH2BUF1     ;Silence time settings read from the editing area are stored in general-purpose
registers.
    SLLC    Rn+1,       #05H        ;Shifts the setting value stored in the general-purpose register 5 bits to the left.
    SLL     Rn,         #05H        ;Shifts the setting value stored in the general-purpose register 5 bits to the left.
    ADD     ERn,        ERm         ;ERn←ERn+32
    ST      ERn,        STPADRML0   ;Set to audio data stop address register (middle and lower)
    ST      Rk,         STPADRH0    ;Set to audio data stop address register (higher)
    ST      Rl,         STAADRL0    ;Set and adjust the audio data start address register
```

Note:m,n : even number

25.3.6 Audio PWM Output Control

SPEN bit of the audio PWM control register (SPCON) is authorization control bit of the PWM output. when the bit is set to "1", enter the PWM output state. When outputting audio PWM output from the P61/P62 pin, set SPEN to "1" and set the P61/P62 pin to the 6th order.
Figure 25-11 shows an example of an operation time chart.

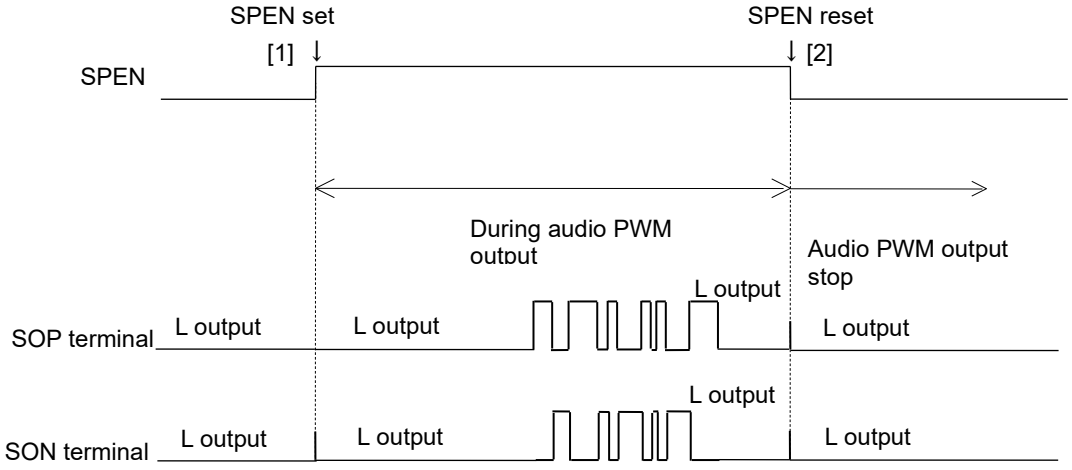


Figure 25-11 Example of operation time chart

Figure 25-11 works as follows:

[1] When SPEN is set to "1", the PWM output from the audio circuit is started.
[2] When SPEN is set to "0", the PWM output from the audio circuit is stopped.

25.3.6.1 PWM "H" level fixed detection circuit operation

ML62Q2700 group has a built-in PWM "H" level fixed detection circuit to prevent overcurrent from flowing through the external speaker amplifier when the PWM is fixed at the "high" level due to an internal PWM abnormality. When the fixed "H" level of PWM is detected, the audio output pin is set to Hi-z.
The PWM "H" level fixed detection circuit controls the on/off by the SDEN bit of the audio PWM fixed detection control register (SDCON), and holds the PWM "H" level fixed detection result in the SDF bit of SDCON
SDEN is the enable control bit of the PWM "H" level fixed detection circuit. If SDEN is set to "1", it will be turned on. If SDEN is set to "0", it will be turned off.
SDF is the determination flag. When SDF is "1", it indicates that PWM "H" level is fixed.
The detection time of PWM "H" level fixed detection can be set with SDD2 to 0 bits.

Figure 25-12 shows an example of an operating time chart.

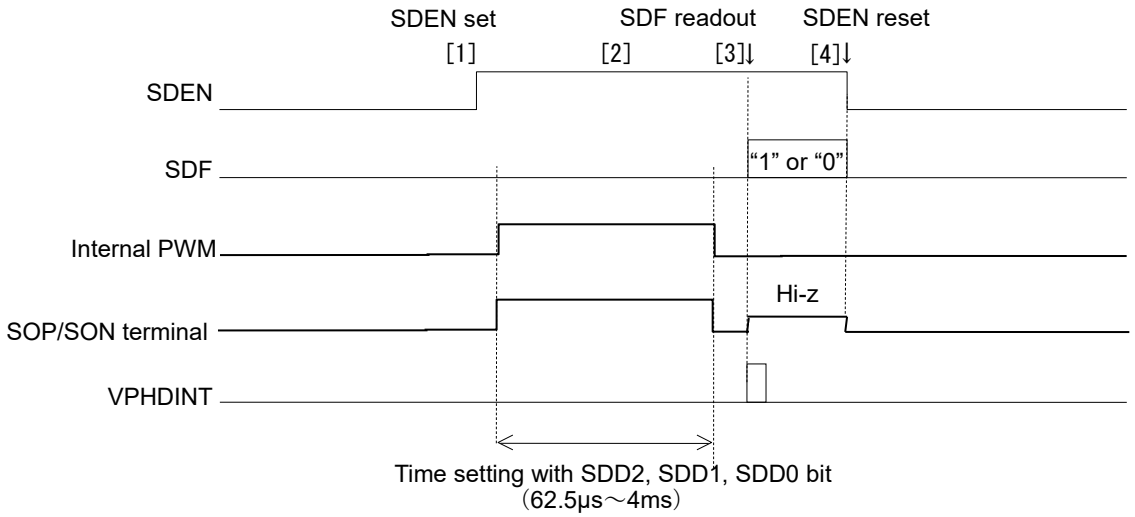


Figure 25-12 Example of operation time chart

Figure 25-12 behaves as follows:

[1] Set SDEN to "1" and turn on the PWM "H" level fixed detection circuit.
[2] PWM detects a fixed "H" level, and when the time set in SDD2, SDD1, and SDD0 bits elapses, SDF is displayed to "H" At the same time, a "H" pulse is output from VPHDINT. Also, the audio output terminal becomes Hi-z.
[3] Read the judgment result flag (SDF).
[4] Set SDEN to "0" and turn off the PWM "high" level fixed detection circuit.

25.3.7 Audio code data configuration and audio data generating method

Audio code data consists of audio management area, audio area, and edit ROM area.
The audio management area is an area that manages phrase information in code data, and stores data that controls the start address, stop address, use or non-use of the edit ROM function, etc. of the voice data for the specified phrase (phrase address).
The audio area contains the actual waveform data.
The Edit ROM area stores data for effective use of audio data. For details, refer to the "19.3.10 Edit ROM function" section. If the edit ROM is not used, the edit ROM area does not exist. composition

To generate audio code data, use our Speech LSI Utility tool. For details, refer to the Speech LSI Utility User's Manual.

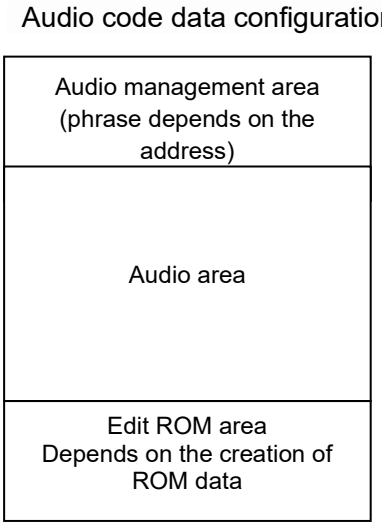


Figure 25-13 Audio code data configuration diagram

25.3.8 Playback time and memory capacity

The playback time depends on the memory capacity, sampling frequency, and playback method. The equation is shown below.
However, this is the playback time when the edit ROM function is not used. Depends on the phrase address.

$$\text{Playback Time} = \frac{1.024 \times (\text{Audio memory capacity} - \text{Audio management area} - \text{Edit ROM area})\,(\text{k bit})}{\text{Sampling frequency}\,(\text{kHz}) \times \text{Bit length}}\ (\text{s})$$

(The bit lengths of 4-bit ADPCM2, 8-bit PCM, and 16-bit PCM are 4, 8, and 16, respectively.)

256 Kbytes of internal flash memory, 16 Kbytes of control program, 7.81kHz sampling frequency, 4-bit ADPCM2 system, 32 phrases, about 6 without the edit ROM function 2. The playback time will be 8 seconds. (Disabled code option area 0.0625 Kbytes = 64 bytes)

Audio memory capacity = 256(Kbytes) - 16(Kbytes) - 0.0625(Kbytes) = 239.9375 (Kbytes) = 1919.5 (Kbits)

Speech control area = 32 (phrases) × 8 (bytes) = 256 (bytes) = 2 (Kbits)

$$\text{Playback Time} = \frac{1.024 \times (1919.5 - 2)\,(\text{k bit})}{7.81\,(\text{kHz}) \times 4(\text{bit})} = 62.8\,(\text{s})$$

The playback time of one phrase must be 20ms or longer.

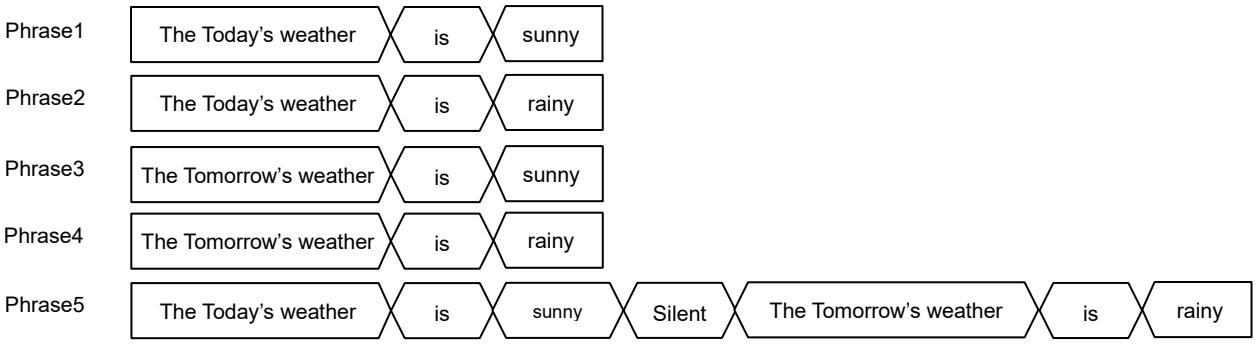
25.3.9 Edit ROM Function

The edit ROM function is a function that allows you to play multiple phrases consecutively. The following functions can be set using the edit ROM function.

- Continuous playback (The number of times specified for continuous playback is unlimited. Depends on the amount of flash memory.)
- Silence insertion function (4ms to 1,024ms)

By using the edit ROM function, the capacity of flash memory can be used efficiently.
Figure 25-14 shows an example of the configuration of voice code data when the edit ROM function is used.

Example 1: Phrase construction when using the edit ROM function



Example 2: Data structure when Example 1 is converted to audio code data

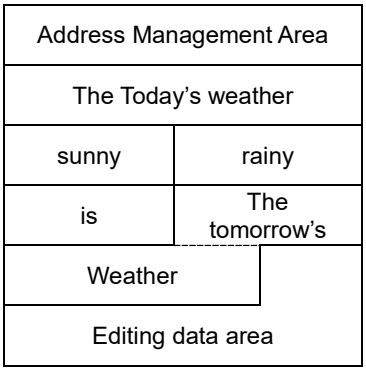
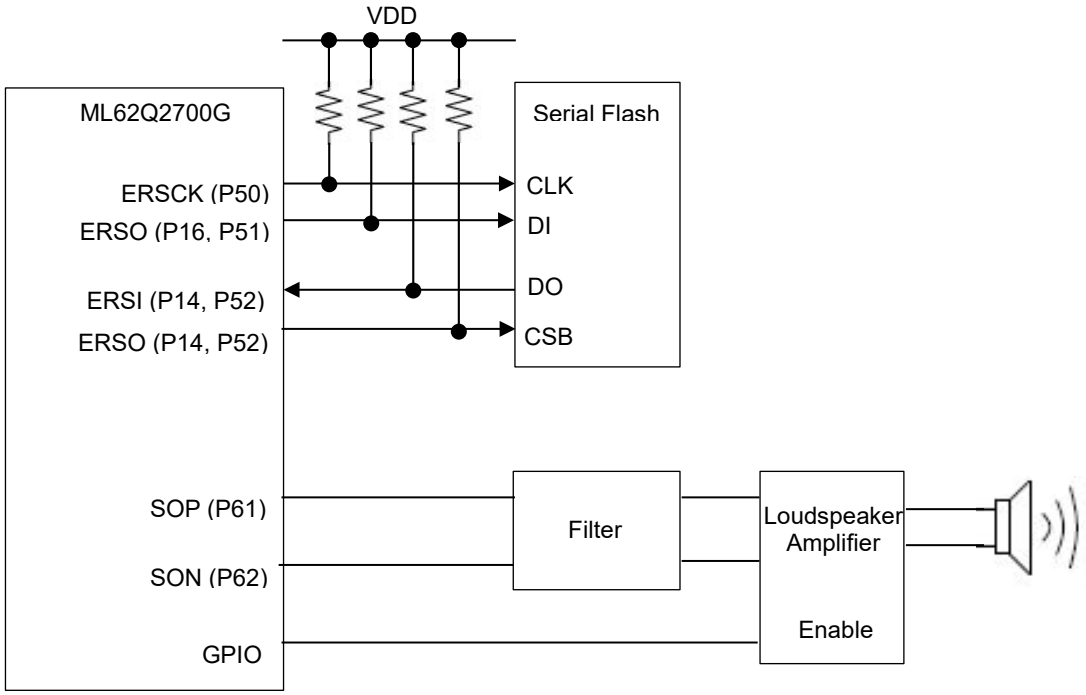


Figure 25-14 Configuration diagram of edit ROM data

25.4 Example of connecting external flash memory and external speaker amplifier



- The pin for connecting the external serial flash memory enters the Hi-z state after the power is turned on. It is recommended to connect a pull-up resistor depending on the serial flash memory specifications to be connected.
- If popping noise is a concern, start with silent playback and set the external amplifier to the allowed state during silent playback.
- Refer to the specifications of the speaker amplifier to be used to determine the filter.

Chapter 26 Flash Memory

26. Flash Memory

26.1 General Description

ML62Q2700 group has the flash memory in the program memory space and data flash area. For details of the program memory space and data flash area, see Chapter 2 "CPU and Memory Space".
The flash memory is programmable by following three ways.

- The ways of programming the flash memory

Programming method	Tool/Register/Communication	Reference Chapter
Programming by the on-chip debug function	On-chip debug emulator or other flash programmers	Chapter 28 "On chip Debug function"
Self-Programming by using the special function register (SFR)	Special Function Registers (SFRs) for programming the flash memory	Section 26.3 "Self-programming"
Programming by the ISP (In-System Programming) function	UART communication with an external device 3rd Party Flash programmers (*1)	Section 26.4 "ISP function"

*1: For 3rd party flash writers, please contact each flash writer manufacturer.

The following is the overview of the differences and functions of each product in the program memory space and data flash area.

- Program memory space and Data flash area Overview (Size and Address)

Product name	Program memory space		Data flash area	
	Size	Address	Size	Address
ML62Q2727/2737/2747	256KByte	0x0:0000 to 0x3:FFFF	4KByte (128Byte x 32sector)	0x1F:0000 to 0x1F:0FFF
ML62Q2726/2736/2746	192KByte	0x0:0000 to 0x2:FFFF		
ML62Q2725/2735/2745	160KByte	0x0:0000 to 0x2:7FFF		
ML62Q2703/2713/2723	96KByte	0x0:0000 to 0x1:7FFF		
ML62Q2702/2712/2722	64KByte	0x0:0000 to 0x0:FFFF		

- Program memory space and Data flash area Overview (Functions and Characteristics)

Item		Program memory space	Data flash area
Erasing and programming unit	Chip erasing (ISP only)	All area	All area
	Block erasing	16K byte	all area
	Sector erasing	1K byte	128 byte
	Programming	4 byte (32bit)	1 byte (8bit)
Erasing and programming time	Chip erasing (ISP only)	Max. about 50ms	Max. about 50ms
	Block erasing		
	Sector erasing		
	Programming	Max. about 80µs	Max. about 40µs
Programming cycle		100 times	10,000 times
Erasing and programming temperature		0°C to +40°C	-40°C to +85°C
Background operation(BGO) function		-	Yes
Erasing and programming completion Interrupt		No	Yes

26.1.1 List of Pins

Programming by the ISP function uses the following pins.

Pin name	I/O	Function
TEST1_N	I	clock input for ISP mode
TEST0	I/O	data input/output for ISP mode

26.2 Register Description

26.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF090	Flash address register	FLASHAL	FLASHA	R/W	8/16	0xFF
0xF091		FLASHAH		R/W	8	0xFF
0xF092	Flash data register 0	FLASHD0L	FLASHD0	R/W	8/16	0xFF
0xF093		FLASHD0H		R/W	8	0xFF
0xF094	Flash data register 1	FLASHD1L	FLASHD1	R/W	8/16	0xFF
0xF095		FLASHD1H		R/W	8	0xFF
0xF096	Flash control register	FLASHCON	-	W	8	0x00
0xF097	Reserved register	-	-	-	-	-
0xF098	Flash acceptor	FLASHACP	-	W	8	0x00
0xF099	Reserved register	-	-	-	-	-
0xF09A	Flash segment register	FLASHSEG	-	R/W	8	0x10
0xF09B	Reserved register	-	-	-	-	-
0xF09C	Flash self register	FLASHSLF	-	R/W	8	0x00
0xF09D	Reserved register	-	-	-	-	-
0xF09E	Flash status register	FLASHSTA	-	R	8	0x00
0xF09F	Reserved register	-	-	-	-	-

26.2.2 Flash Address Register (FLASHA)

FLASHA is a SFR to set the erasing and programming address.

Address : 0xF090 (FLASHAL/FLASHA), 0xF091 (FLASHAH)
Access : R/W
Access size : 8/16 bit
Initial value : 0xFFFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FLASHA															
Byte	FLASHAH								FLASHAL							
Bit	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15 to 0	FA15 to FA0	Set the erasing or programming address.

[Note]

- **Note that programming for the program memory space is performed by the unit of 4 bytes. Because of this, the setting values in the FA1 bit and FA0 bit are ignored.**

26.2.3 Flash Segment Register (FLASHSEG)

FLASHSEG is a SFR to set the segment for erasing and programming the flash memory.

Address : 0xF09A (FLASHSEG)
Access : R/W
Access size : 8 bit
Initial value : 0x10

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FLASHSEG							
Bit	-	-	-	-	-	-	-	-	-	-	-	FSEG4	FSEG3	FSEG2	FSEG1	FSEG0
R/W	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 5	-	Reserved bits
4 to 0	FSEG4 to FSEG0	Specifies the segment address of the flash memory to be erase/write to data.

Table 26-1 shows the address setting value for block erasing and Table 26-2 shows the address setting value for sector erasing.

Table 26-1 Address Setting Values for Block Erasing

Segment	Block	Address	Size	FLASHSEG register	FLASHA register
Segment 0	Block 0	0x0000 to 0x3FFF	16KByte	0x00	0x0000
	Block 1	0x4000 to 0x7FFF	16KByte		0x4000
	Block 2	0x8000 to 0xBFFF	16KByte		0x8000
	Block 3	0xC000 to 0xFFFF	16KByte		0xC000
Segment 1	Block 4	0x0000 to 0x3FFF	16KByte	0x01	0x0000
	Block 5	0x4000 to 0x7FFF	16KByte		0x4000
	Block 6	0x8000 to 0xBFFF	16KByte		0x8000
	Block 7	0xC000 to 0xFFFF	16KByte		0xC000
Segment 2	Block 8	0x0000 to 0x3FFF	16KByte	0x02	0x0000
	Block 9	0x4000 to 0x7FFF	16KByte		0x4000
	Block 10	0x8000 to 0xBFFF	16KByte		0x8000
	Block 11	0xC000 to 0xFFFF	16KByte		0xC000
Segment 3	Block 12	0x0000 to 0x3FFF	16KByte	0x03	0x0000
	Block 13	0x4000 to 0x7FFF	16KByte		0x4000
	Block 14	0x8000 to 0xBFFF	16KByte		0x8000
	Block 15	0xC000 to 0xFFFF	16KByte		0xC000
Segment 4	Block 16	0x0000 to 0x3FFF	16KByte	0x04	0x0000
	Block 17	0x4000 to 0x7FFF	16KByte		0x4000
	Block 18	0x8000 to 0xBFFF	16KByte		0x8000
	Block 19	0xC000 to 0xFFFF	16KByte		0xC000
Segment 5	Block 20	0x0000 to 0x3FFF	16KByte	0x05	0x0000
	Block 21	0x4000 to 0x7FFF	16KByte		0x4000
	Block 22	0x8000 to 0xBFFF	16KByte		0x8000
	Block 23	0xC000 to 0xFFFF	16KByte		0xC000
Segment 6	Block 24	0x0000 to 0x3FFF	16KByte	0x06	0x0000
	Block 25	0x4000 to 0x7FFF	16KByte		0x4000
	Block 26	0x8000 to 0xBFFF	16KByte		0x8000
	Block 27	0xC000 to 0xFFFF	16KByte		0xC000
Segment 7	Block 28	0x0000 to 0x3FFF	16KByte	0x07	0x0000
	Block 29	0x4000 to 0x7FFF	16KByte		0x4000
	Block 30	0x8000 to 0xBFFF	16KByte		0x8000
	Block 31	0xC000 to 0xFFFF	16KByte		0xC000
Segment 31	Block 0	0x0000 to 0x0FFF	4KByte	0x1F	0x0000

Table 26-2-1 Address Setting Values for Sector Erasing

Segment	Block	Address	Size	FLASHSEG register	FLASHA register
Segment 0	Sector 0	0x0000 to 0x03FF	1KByte	0x00	0x0000
	Sector 1	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 62	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 63	0xFC00 to 0xFFFF	1KByte		0xFC00
Segment 1	Sector 64	0x0000 to 0x03FF	1KByte	0x01	0x0000
	Sector 65	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 126	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 127	0xFC00 to 0xFFFF	1KByte		0xFC00
Segment 2	Sector 128	0x0000 to 0x03FF	1KByte	0x02	0x0000
	Sector 129	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 190	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 191	0xFC00 to 0xFFFF	1KByte		0xFC00
Segment 3	Sector 192	0x0000 to 0x03FF	1KByte	0x03	0x0000
	Sector 193	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 254	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 255	0xFC00 to 0xFFFF	1KByte		0xFC00
Segment 4	Sector 256	0x0000 to 0x03FF	1KByte	0x04	0x0000
	Sector 257	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 318	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 319	0xFC00 to 0xFFFF	1KByte		0xFC00
Segment 5	Sector 320	0x0000 to 0x03FF	1KByte	0x05	0x0000
	Sector 321	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 382	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 383	0xFC00 to 0xFFFF	1KByte		0xFC00
Segment 6	Sector 384	0x0000 to 0x03FF	1KByte	0x06	0x0000
	Sector 385	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 446	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 447	0xFC00 to 0xFFFF	1KByte		0xFC00
Segment 7	Sector 448	0x0000 to 0x03FF	1KByte	0x07	0x0000
	Sector 449	0x0400 to 0x07FF	1KByte		0x0400
	:	:	:		:
	Sector 510	0xF800 to 0xFBFF	1KByte		0xF800
	Sector 511	0xFC00 to 0xFFFF	1KByte		0xFC00

Table 26-2-2 Address Setting Values for Sector Erasing

Segment	Block	Address	Size	FLASHSEG register	FLASHA register
Segment 31	Sector 0	0x0000 to 0x007F	128Byte	0x1F	0x0000
	Sector 1	0x0080 to 0x00FF	128Byte		0x0080
	Sector 2	0x0100 to 0x017F	128Byte		0x0100
	Sector 3	0x0180 to 0x01FF	128Byte		0x0180
	:	:	:		:
	Sector 12	0x0600 to 0x067F	128Byte		0x0600
	Sector 13	0x0680 to 0x06FF	128Byte		0x0680
	Sector 14	0x0700 to 0x077F	128Byte		0x0700
	Sector 15	0x0780 to 0x07FF	128Byte		0x0780
	:	:	:		:
	Sector 28	0x0E00 to 0x0E7F	128Byte		0x0E00
	Sector 29	0x0E80 to 0x0EFF	128Byte		0x0E80
	Sector 30	0x0F00 to 0x0F7F	128Byte		0x0F00
	Sector 31	0x0F80 to 0x0FFF	128Byte		0x0F80

26.2.4 Flash Data Register 0 (FLASHD0)

FLASHD0 is a SFR to set programming data.

Address : 0xF092 (FLASHD0L/FLASHD0), 0xF093 (FLASHD0H)
Access : R/W
Access size : 8/16 bit
Initial value : 0xFFFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FLASHD0															
Byte	FLASHD0H								FLASHD0L							
Bit	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15 to 8	FD15 to FD8	Set the 2nd byte data.
7 to 0	FD7 to FD0	Set the 1st byte data.

26.2.5 Flash Data Register 1 (FLASHD1)

FLASHD1 is a SFR to set programming data.

Address : 0xF094 (FLASHD1L/FLASHD1), 0xF095 (FLASHD1H)
Access : R/W
Access size : 8/16 bit
Initial value : 0xFFFF

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	FLASHD1															
Byte	FLASHD1H								FLASHD1L							
Bit	FD31	FD30	FD29	FD28	FD27	FD26	FD25	FD24	FD23	FD22	FD21	FD20	FD19	FD18	FD17	FD16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15 to 8	FD31 to FD24	Set the 4th byte data.
7 to 0	FD23 to FD16	Set the 3rd byte data.

There are some differences for programming the program memory space and the data flash area.

Programming target	Register	How to start programming to flash	Description
Program memory space	FLASHD0 register and Four bytes specified in FLASHD1 register	Writing data into FLASHD1/FLASHD1H	Write data into FLASHD0 register at first and FLASHD1 register the second, in LSB first.
Data flash area	FLASHD0L register only (one byte) in FLASHD0 register.	Writing data into FLASHD0/FLASHD0L	Data written into FLASHD0H of FLASHHD0 register and FLASHD1 register are invalid.

[Note]

- **Since writing to the program memory space or writing to the data flash is determined by the value set in the flash segment register (FLASHSEG), set the register first.**
- **During programming data-flash, a CPU program processing continues using the back ground operation function (BGO). To confirm of writing completion, readout FDPRSTA bit of FLASHSTA register.**
- **Erase data in the addresses to be written in advance. Overwrite the data without erasing, the data is not guaranteed.**
- **Do not read/write to unused areas to prevent the CPU malfunction.**

26.2.6 Flash Control Register (FLASHCON)

FLASHCON is a write-only SFR to control the block erasing and sector erasing for the flash memory. This register always returns 0x00 for reading.

Address : 0xF096 (FLASHCON)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FLASHCON							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FSERS	FERS
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 2	-	Reserved bits
1, 0	FSERS, FERS	Start the sector erasing or block erasing. When FSERS bit is set to "0" and FERS bit is set to "1", the blocks specified in the FLASHSEG and FLASHAH registers are erased. When FSERS bit is set to "1" and FERS bit is set to "0", the sectors specified in the FLASHSEG and FLASHAH registers are erased. 00: No use (No function) 01: Start block erasing 10: Start sector erasing 11:No use (No function)

26.2.7 Flash Acceptor (FLASHACP)

FLASHACP is a write-only SFR to accept for erasing/programming the flash memory.

Address : 0xF098 (FLASHACP)
Access : W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FLASHACP							
Bit	-	-	-	-	-	-	-	-	fac7	fac6	fac5	fac4	fac3	fac2	fac1	fac0
R/W	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register restricts erase/write operations to prevent erroneous erase operation and erroneous write operation.
When "0xFA" and "0xF5" are written to FLASHACP in this order, the erasing or programming function is enabled only once. For subsequent continuous erasing or programming, "0xFA" and "0xF5" must be written to FLASHACP each time.

Even if other instructions are comes in between the instruction that writes "0xFA" and "0xF5" to FLASHACP, the erasing or programming function is still valid.
If data other than "0xF5" is written to FLASHACP after "0xFA" is written, "0xFA" becomes invalid. In this case, it needs to write "0xFA" again.

[Note]

- **If writes to FLASHSTA register when other than 0x0, the data in the flash memory being processed is not guaranteed.**

26.2.8 Flash Self Register (FLASHSLF)

FLASHSLF is a SFR to enable erasing and programming the flash memory. When system clock is the low-speed clock, it is not writable.

Address : 0xF09C (FLASHSLF)
Access : R/W
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FLASHSLF							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FSELF
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 1	-	Reserved bits
0	FSELF	Enable erasing and programming the flash memory. This setting is kept after completed erasing/programming. 0: Disabled (Initial value) 1: Enabled

[Note]

- **If writes to FLASHSTA register when other than 0x0, the data in the flash memory being processed is not guaranteed.**

26.2.9 Flash Status Register (FLASHSTA)

FLASHSTA is a read-only SFR to check status of the flash memory.

Address : 0xF09E (FLASHSTA)
Access : R
Access size : 8 bit
Initial value : 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								FLASHSTA							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	FDPRSTA	FDERSTA
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 2	-	Reserved bits
1	FDPRSTA	Indicate whether the data flash area is in the state of programming. 0: Not in the state of programming (Initial value) 1: In the state of programming
0	FDERSTA	Indicate whether the data flash area is in the state of erasing. 0: Not in the state of erasing (Initial value) 1: In the state of erasing

This register is used when erasing or programming the data flash memory.

Erasing/Programming target	Availability to read this register while erasing/programming	Description
Program memory space	Unavailable	No use the FLASHSTA register.
Data flash area	Available	Start erasing/programming the flash after checking the each bit of FLASHSTA is set to "0".

FLASHSTA register is not used when erasing/writing the program memory space. This is because the CPU stops program operation while the program memory space is being erased/written, FLASHSTA register cannot be read.

As the Back Ground Operation (BGO) function allows the CPU continue running the program codes, make a process for the next erasing and programming by checking the FDERSTA bit or FDPRSTA bit to see if the erasing or programming is completed.

While erasing/writing the data flash area, the CPU program processing continues using the background operation function (BGO), to confirm that the erase/write has completion before writing to the next erase/write.

[Note]
- **Execute the erasing or programming after checking the FDERSTA bit or FDPRSTA bit are "0".**
- **Do not execute the erasing or programming when either the FDERSTA bit or the FDPRSTA bit is "1".**

26.3 Self-programming

The self-programming is the function to program (erase and program) the program memory space and data flash area using SFRs.
Table 26-3 shows the self-programming specifications for each of the program memory space and data flash area.

Table 26-3 Self-programming of Program Memory Space and Data Flash Area

		Program memory space (Segment 0 to 7)	Data flash area (segment 31)
Programming unit	Erasing block	16 Kbyte	all area
	Erasing sector	1 Kbyte	128 byte
	Programming	4 byte	1 byte
CPU operation during block/sector erase or program		Stop program processing (after completion of erasing/programming, resume program processing)	Continue program processing through the background operation (BGO) function
Confirmation of end of block/sector erasing or programming		Confirmation not required (as program run is stopped during erasing/programming)	Confirmation can be made through FLASHSTA register
Target area where block/sector erasing has been applied		Every bit becomes "1" (the bit written with "0" by writing becomes "0" from "1")	
Note on data programming		Erase the area to be reprogrammed (data programmed without erasing is not guaranteed)	
Function to prevent unintended erasing/programming		Flash self-register (FLASHSLF) and flash acceptor (FLASHACP) incorporated (*1)	
Flash memory erasing/programming		Supported only when system clock is the high-speed clock (*2)	
Note on user program programming		Before programming the user program, prepare a program for self-programming in the program code area which is not erased/reprogrammed	-
Remapping function		User program update, etc. can be performed by simultaneously using remapping function	-

*1: After the programming is enabled by the FLASHSLF register, if "0xFA" and "0xF5" are written to the flash acceptor (FLASHACP), block/sector erase or reprogram is enabled only once.
*2: See Chapter 6 "Clock Generation Circuit" for enabling oscillation of the high-speed oscillation circuit and switching the system clock.

26.3.1 Notes on Debugging Self-programming Code

When debugging the area within the scope of program for self-programming (from setting the flash acceptor to writing the flash data register 0, 1) using U16 development environment (debugger), use the debugger according to the precautions described in Table 26-4.

Table 26-4 Notes on Debugging Self-programming

Limited function	Notes
Breakpoint setting	Do not perform the real time execution with break points set in the scope of program for self-programming (from setting the flash acceptor to setting the flash data register0, 1). Otherwise, the flash memory may not be reprogrammed if break points occur within the scope of program for self-programming.
Step execution	Do not perform the step execution within the scope of program for self-programming. Otherwise, the flash memory may not be reprogrammed if the step execution is performed within the scope of program for self-programming.

26.3.2 Programming Program Memory Space

In the program memory space (flash memory), block erase in units of 16 Kbytes, sector erase in units of 1 Kbyte, and reprogram in units of 4 bytes can be executed.
Figure 26-1 shows the flow diagram for erasing the program memory space.

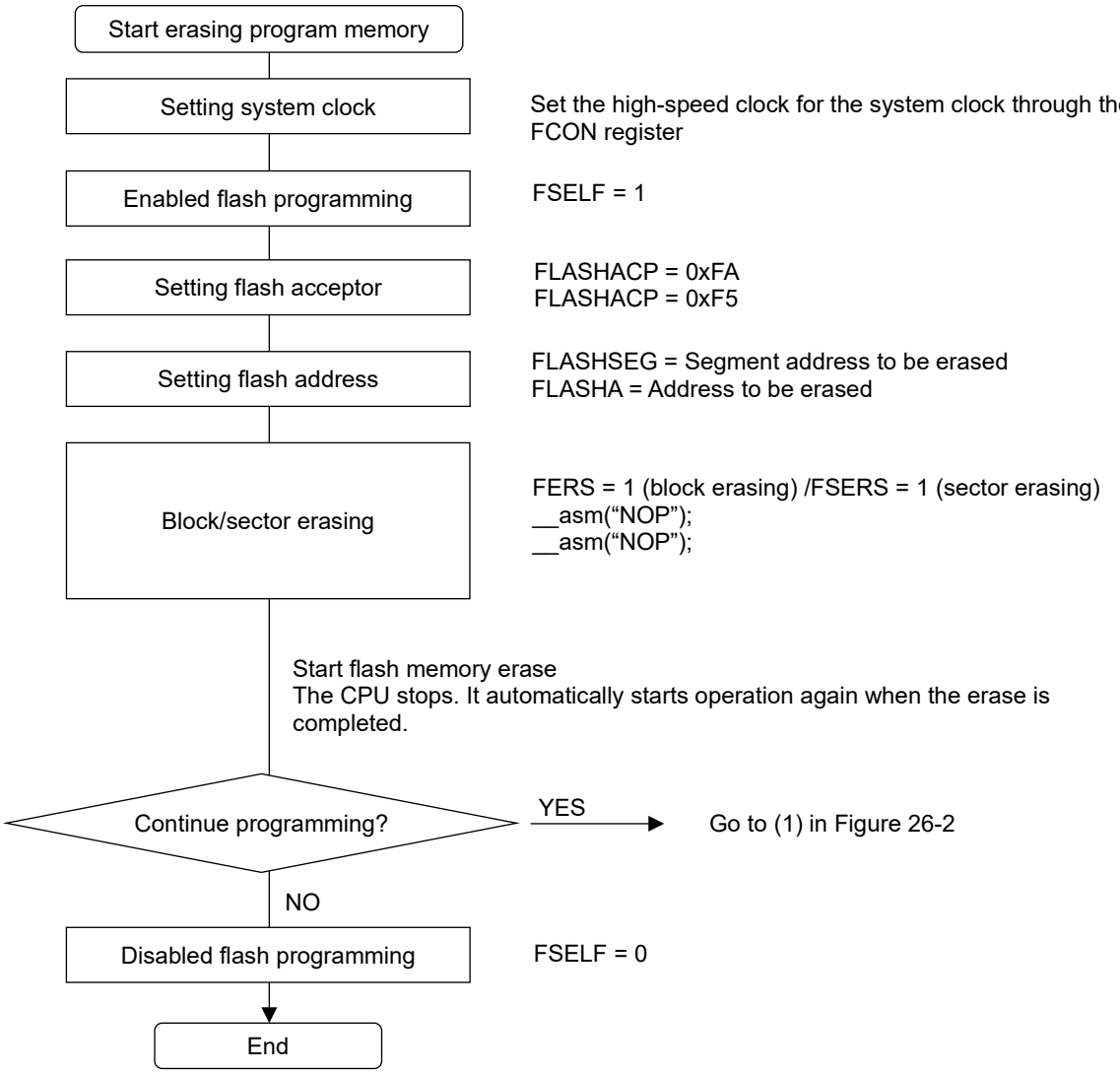


Figure 26-1 Flow Diagram for Erasing Program Memory Space

[Note]

- **Only erase areas irrelevant to program processing. If erasing the area where program processing is in progress, the LSI works incorrectly.**
- **During block/sector erasing, the CPU stops the operation for maximum 50 ms whereas peripheral circuits continue operation. Therefore, clear the WDT counter accordingly.**
- **For block/sector erasing, place two NOP instructions following the instruction used to set FERS/FSERS bits of the FLASHCON register to "1".**

Figure 26-2 shows the flow diagram for programming the program memory space.

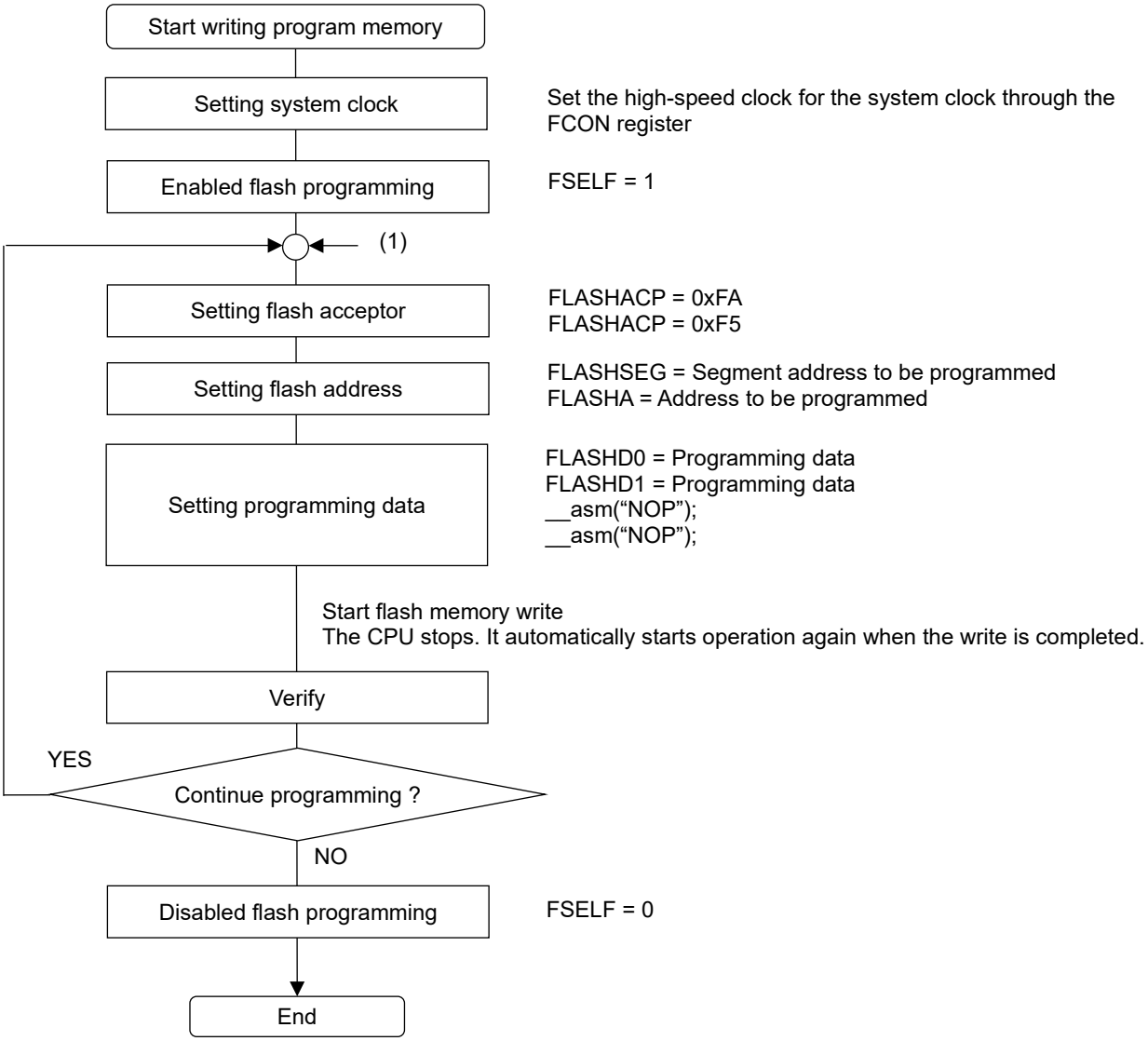


Figure 26-2 Flow Diagram for Programming Program Memory Space

[Note]

- **Only erase areas irrelevant to program processing. If erasing the area where program processing is in progress, the LSI malfunctions.**
- **During the programming, the CPU stops the operation for maximum 80 µs whereas peripheral circuits continue operation. Therefore, clear the WDT counter accordingly.**
- **For data programming setting, place two NOP instructions following the instruction used to set the programming data in the FLASHD1 register.**

26.3.3 Programming Data Flash Area

In the data flash area (flash memory), block erase in all area, sector erase in units of 128 bytes, and programming in units of 1 byte can be executed. During block/sector erase or program in the data flash area, the CPU continues program processing using the background operation (BGO) function.
Figure 26-3 shows the flow diagram for erasing the data flash area.

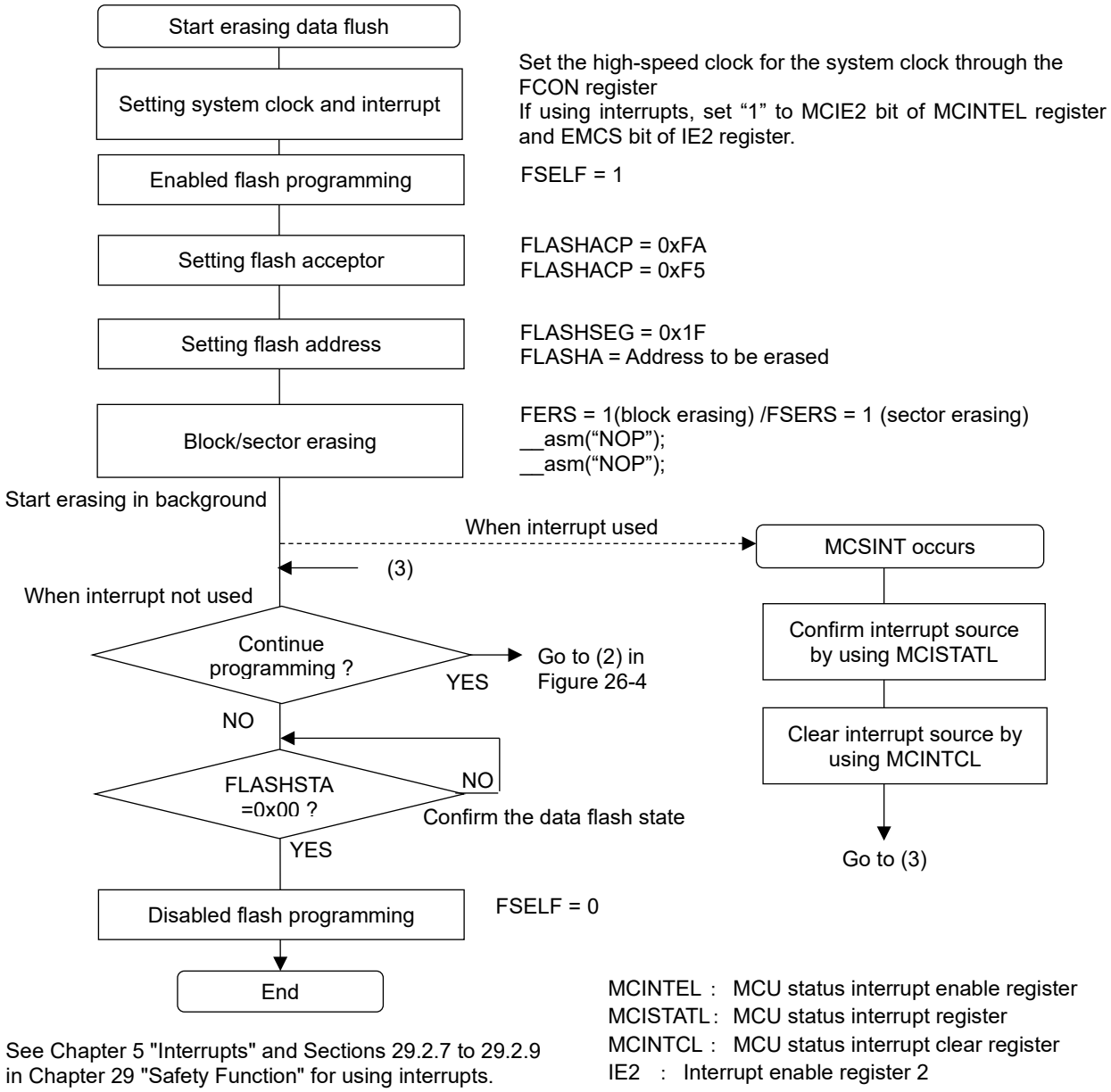


Figure 26-3 Flow Diagram for Erasing Data Flash Area

[Note]

- **The CPU continues program processing even while data flash erasing is in progress. An entering to the STOP/STOP-D/HALT-D/HALT-H mode is not available during the erasing. In addition, set the FSELF bit of the FLASHSLF register to "0" after the erasing is completed.**
- **The data flash area is unreadable during erasing.**
- **For block/sector erasing, place two NOP instructions following the instruction used to set FERS/FSERS bits of the FLASHCON register to "1".**

Figure 26-4 shows the flow diagram for programming the data flash area.

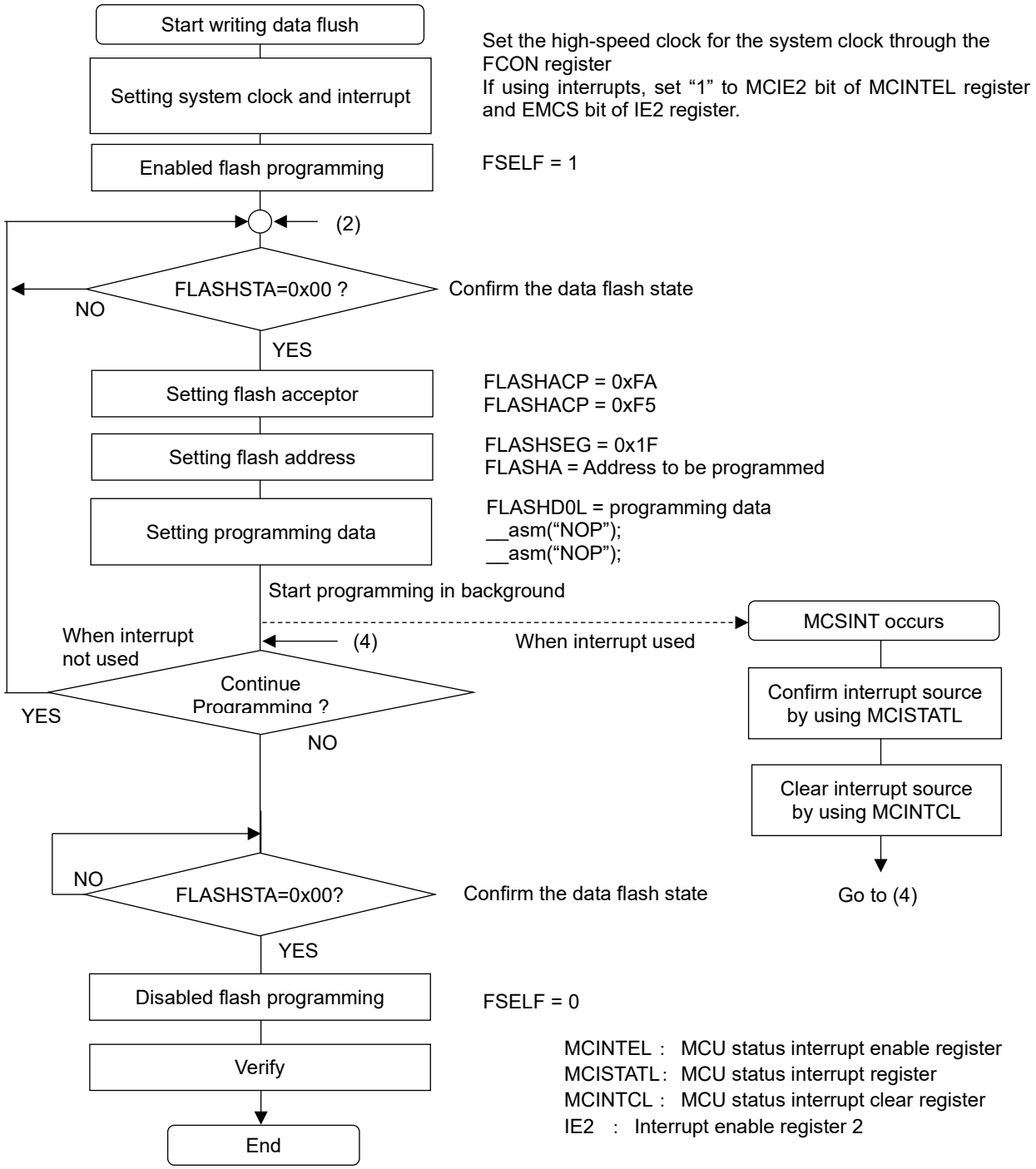


Figure 26-4 Flow Diagram for Programming Data Flash Area

[Note]

- **The CPU continues program processing even while data flash programming is in progress. An entering to the STOP/STOP-D/HALT-D/HALT-H mode is not available during the programming. In addition, set the FSELF bit of the FLASHSLF register to "0" (erase/program disabled) after the programming ended.**
- **The data flash area is unreadable during programming.**
- **For data programming setting, place two NOP instructions following the instruction used to set the programming data in the FLASHD0L register.**

26.3.4 Notes on use of self-programming

Table 26-5 shows the notes on the use of self-programming (block erasing/sector erasing/programming).

Table 26-5 Notes on Use of Self-programming

Item	Notes
System clock during use of self-programming	Set to high-speed clock. See Chapter "6 Clock Generation Circuit" for enabling the high-speed clock oscillation and switching the system clock.
If power outage or forced termination due to a reset occurs	Data in flash memory is not guaranteed. Perform block/sector erase again then program data.
If LSI does not start up due to occurrence of power outage or forced termination during programming (*1)	Program the program again using on-chip debug emulator or ISP function.
Access to SFRs related flash control.	Do not perform to write to the FLASHACP/FLASHSLF register during self-programming; when FLASHSTA is not 0x0.

*1: While programming the block or sector including address 0:0000 of the program area is in progress.

26.4 In-System Programming Function

The In-System Programming (ISP) function is used to program a program memory space or data flash area through 2-wired synchronous serial port communication with an external device.

26.4.1 Programming Procedure

Figure 26-5 shows the flow diagram for programming the flash memory using the ISP function.

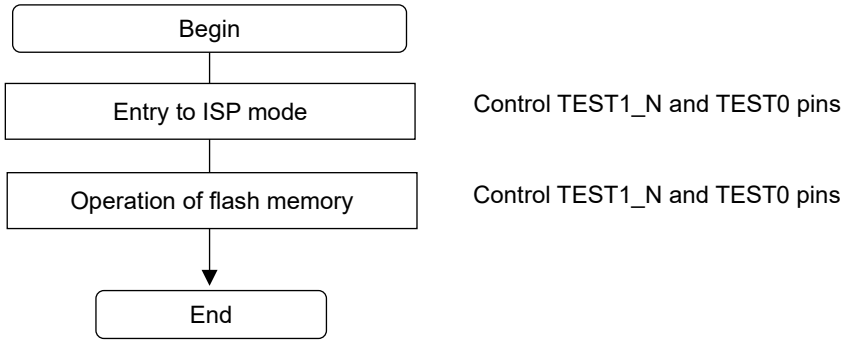


Figure 26-5 Flow Diagram for Programming Flash Memory Using ISP Function

26.4.2 Communication Method

Table 26-6 describes the communication method of the ISP function.

Table 26-6 ISP Function Communication Method

Item	Description
Communication Method	2-wired synchronous serial port
Data format	8-bit length, MSB first
Baud rate	1.5 to 2.5MHz

26.4.3 Control Command

3-byte commands are used to make the communication in the ISP function.
Table 26-7 shows the ISP mode commands.

Table 26-7 ISP Mode Command List

Command		1st byte	2nd byte	3rd byte
Entry	Mode entry command (1)	0xAB	0x63	0x59
	Mode entry command (2)	0xA4	0x55	0x0D
	Entry confirmation command *1	0x01	(Read) 0x06	(Read) 8'b111x_xxxx
Initial setting	Initial setting command (1)	0x1A	0x00	0x08
	Initial setting command (2)	0x1A	0x00	0x00
	Initial setting command (3)	0xC0	0x00	0x01
	Initial setting command (4)	0xC0	0x00	0x05
	Initial setting command (5)	0xC0	0x00	0x03
	Initial setting command (6)	0xCE	0x00	0x01
	Initial setting command (7)	0xCE	0x00	0x00
	Initial setting command (8)	0x96	0xFF	0xFF
	Initial setting command (9)	0x98	0xFF	0xFF
	Initial setting command (10)	0x9A	0xFF	0xFF
	Initial setting command (11)	0x9C	0xFF	0xFF
	Initial setting command (12)	0x9E	0xFF	0xFF
	Initial confirmation command (1) *1	0x01	(Read) 0x06	(Read) 0xC0
	Initial confirmation command (2) *1	0x91	(Read) 0x00	(Read) 0x00
Common setting	Segment setting command	0xC6	0x00	(segment value) 0x00-0x1F
	Address setting command	0xC8	Higher 8 bits	Lower 8 bits
	BUSY confirmation command *1	0xC5	(Read) 0x00: IDLE other :not IDLE	(Read) 0x1F
Block erasing	Block erasing command	0xC2	0x00	0x05
Chip erasing	Chip erasing command	0xC2	0x00	0x06
For programing data	Data setting command H ; in program code area (higher 2bytes)	0xD2	Higher Byte	Lower Byte
	Data setting command L ; in program code area (lower 2bytes)	0xCA	Higher Byte	Lower Byte
	Data setting command D ; in data flash area	0xCA	0xFF	1Byte data
	Programming command	0xC2	0x00	0x04
For verify	Expected data setting command H ; in program code area (higher 2bytes)	0xE4	Higher Byte	Lower Byte
	Expected data setting command L ; in program code area (lower 2bytes)	0xE2	Higher Byte	Lower Byte
	Expected data setting command D ; in data flash area	0xE4	0xFF	1Byte data
	Verify command	0xC2	0x00	0x02
	Verify confirmation command *1 ; collation result of expected data	0xE7	(Read) 0x00	(Read) 0x03 : OK 0x01 : OK at current cycle, but has been NG in the past cycles. 0x00 or 0x02: NG
	Stack clear command 1	0xD2	0x00	0x00
	Stack clear command 2	0xCA	0x00	0x00
	Stack clear command 3	0xE6	0x00	0x03

[Note]
- **Accessing to the program code area is performed in 4byte units. Set 4byte boundaries (0H/4H/8H/CH) for lower 4bits of the address. Accessing to the data flash area is performed in units of 1byte.**
- **All commands except some confirmation commands (*1) are reflected when a next command is sent.**

26.4.3.1 Command Timing

See the ML62Q2700 data sheet for AC specifications.
Transmit one command within 80µs. Retry communication after 200µs or more as an interval time if communication cannot be made.
However, ISP mode has a function to determine that a timeout is set out after a certain period and exit the mode.
After switching to ISP mode, issue one of the following commands at intervals within 800ms.

- Initial setting command (1) + any commands
- Expected data setting command H + any commands
- Expected data setting command D + any commands
- BUSY confirmation command

The completion of issuing each entry command or command other than each confirm command (mode entry command (1) (2), entry confirmation command, initial confirmation command (1) (2), BUSY confirmation command, verify confirmation command) is the rising edge of the first TEST1_N of the next command.

26.4.4 How to Entry ISP Mode

Figure 26-6 shows flow diagram and timing diagram to entry ISP mode.

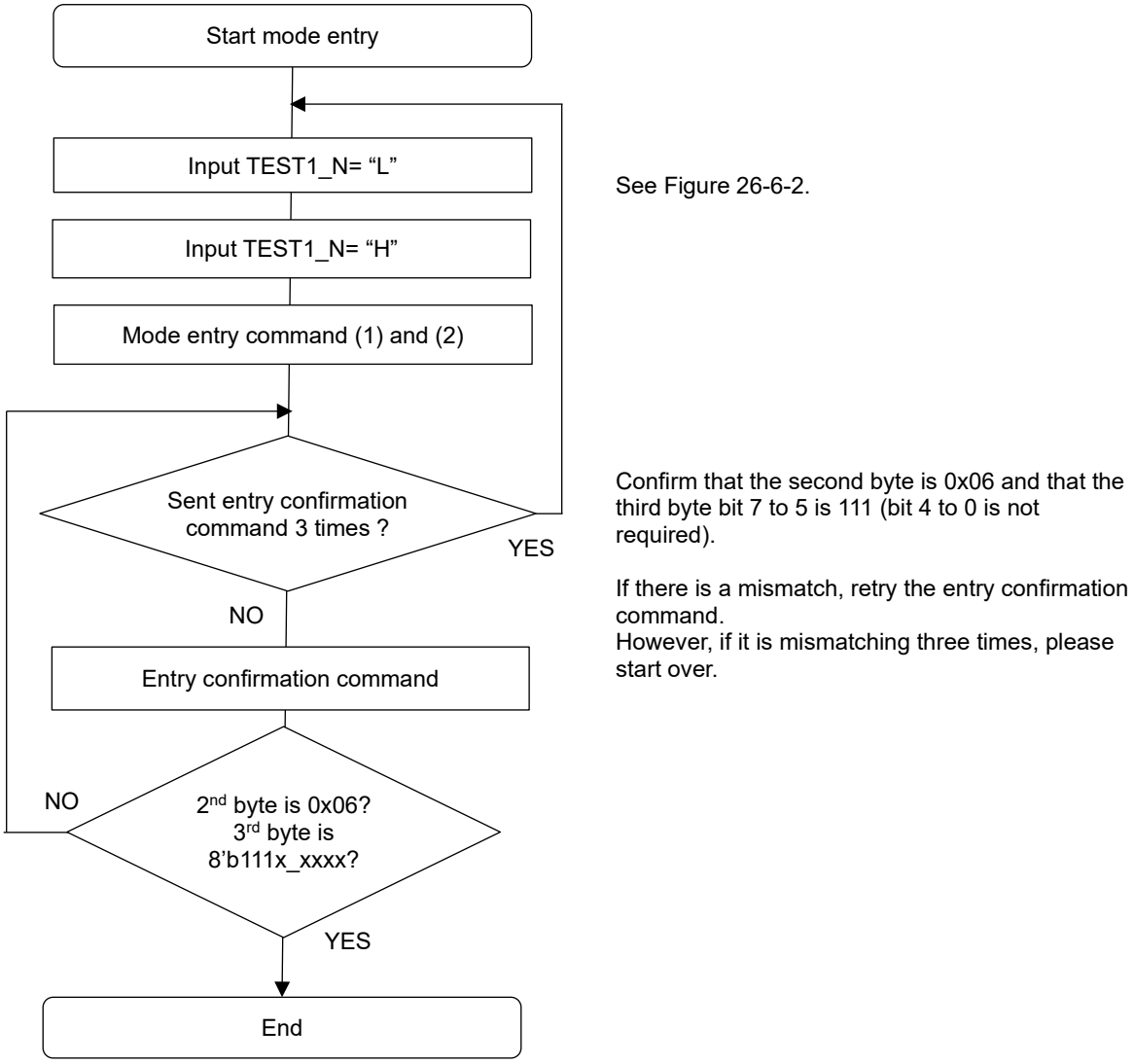


Figure 26-6-1 Flow diagram to entry ISP mode

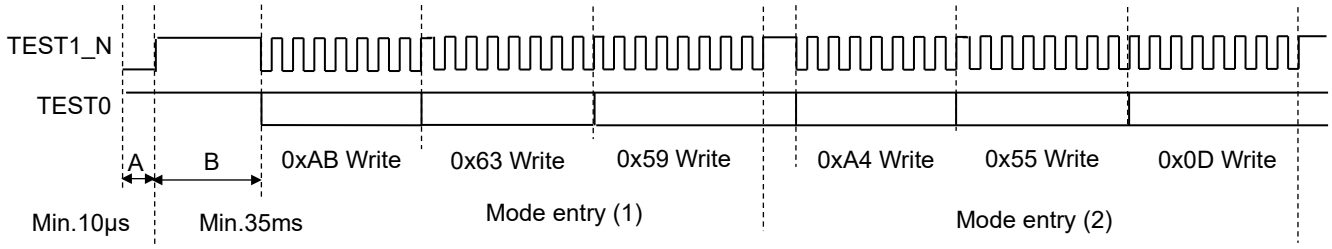


Figure 26-6-2 Timing diagram to entry ISP mode

26.4.5 Handling the Flash Memory

Figure 26-7 shows the flow diagram for erasing/programming the flash memory after transition to the ISP mode.

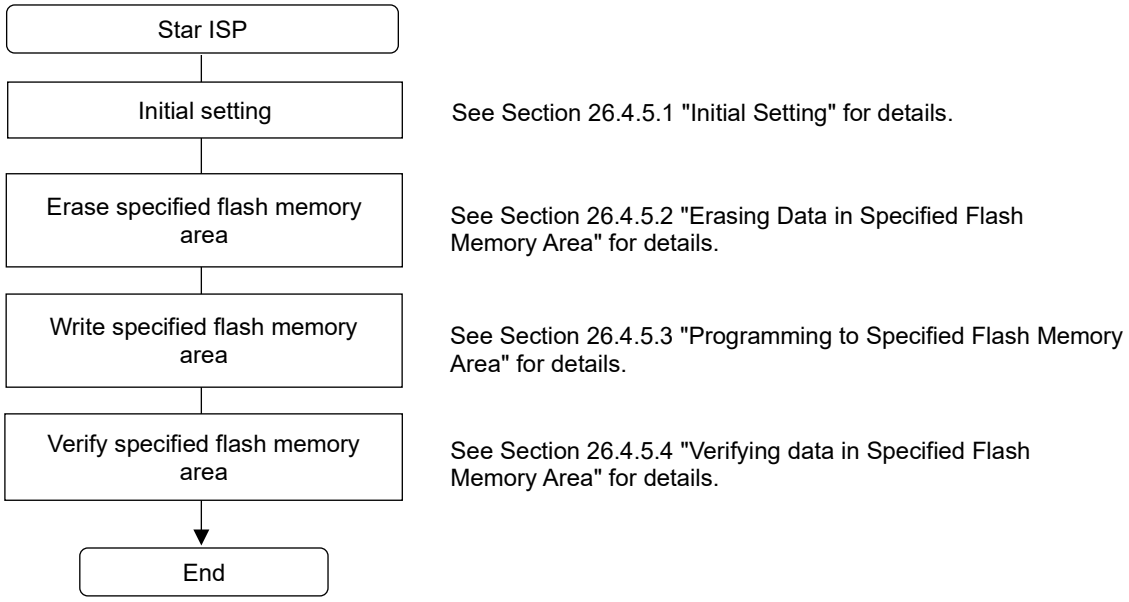


Figure 26-7 Flow Diagram for Erasing/Programming Flash Memory (Overview)

26.4.5.1 Initial Setting

Figure 26-8 shows the initial setting flow.

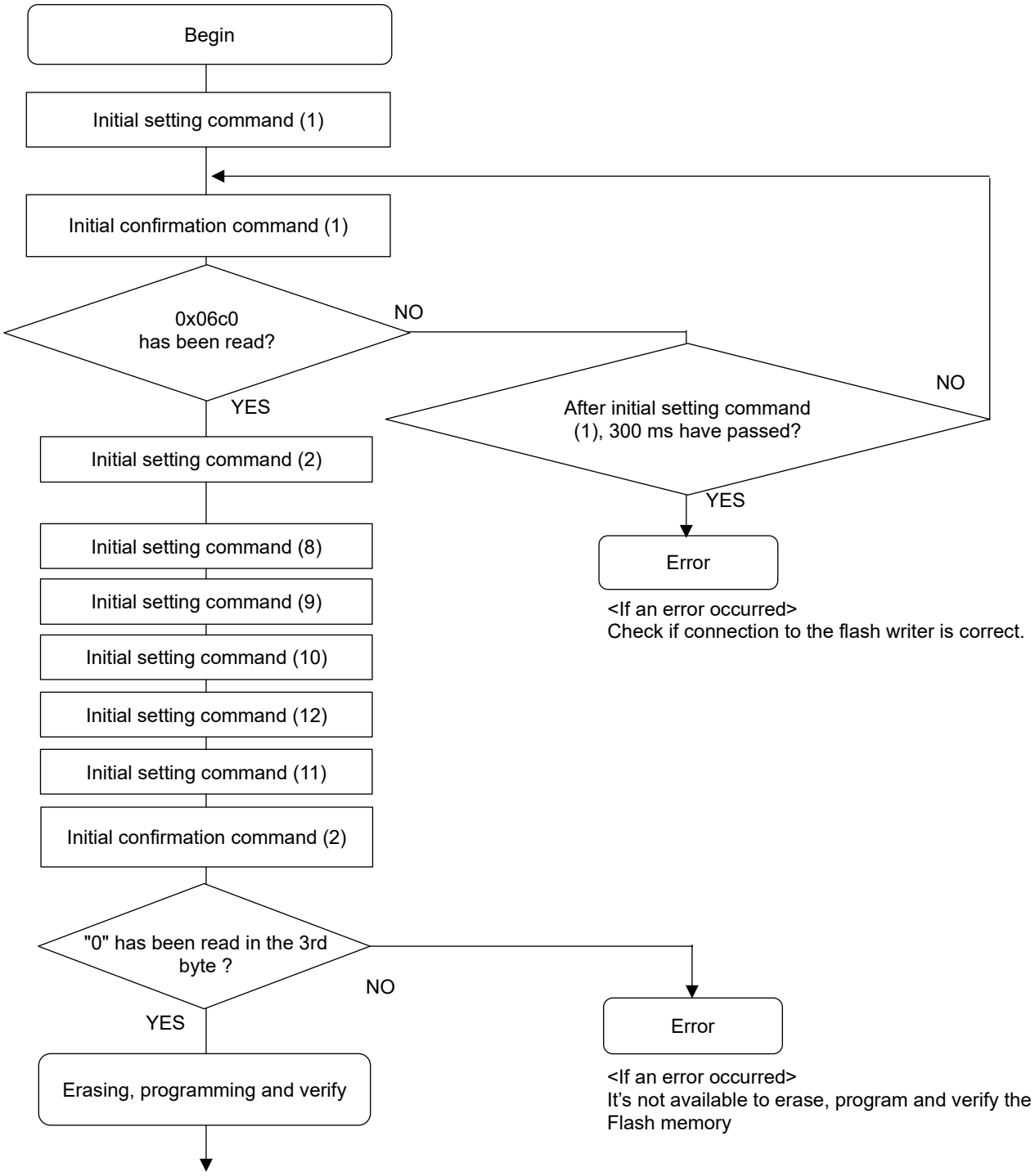


Figure 26-8 Initial Setting Flow Diagram

[Note]

- **Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing".**

26.4.5.2 Erasing Data in Specified Flash Memory Area

Figure 26-9 shows the flow diagram for erasing data in specified flash memory area.

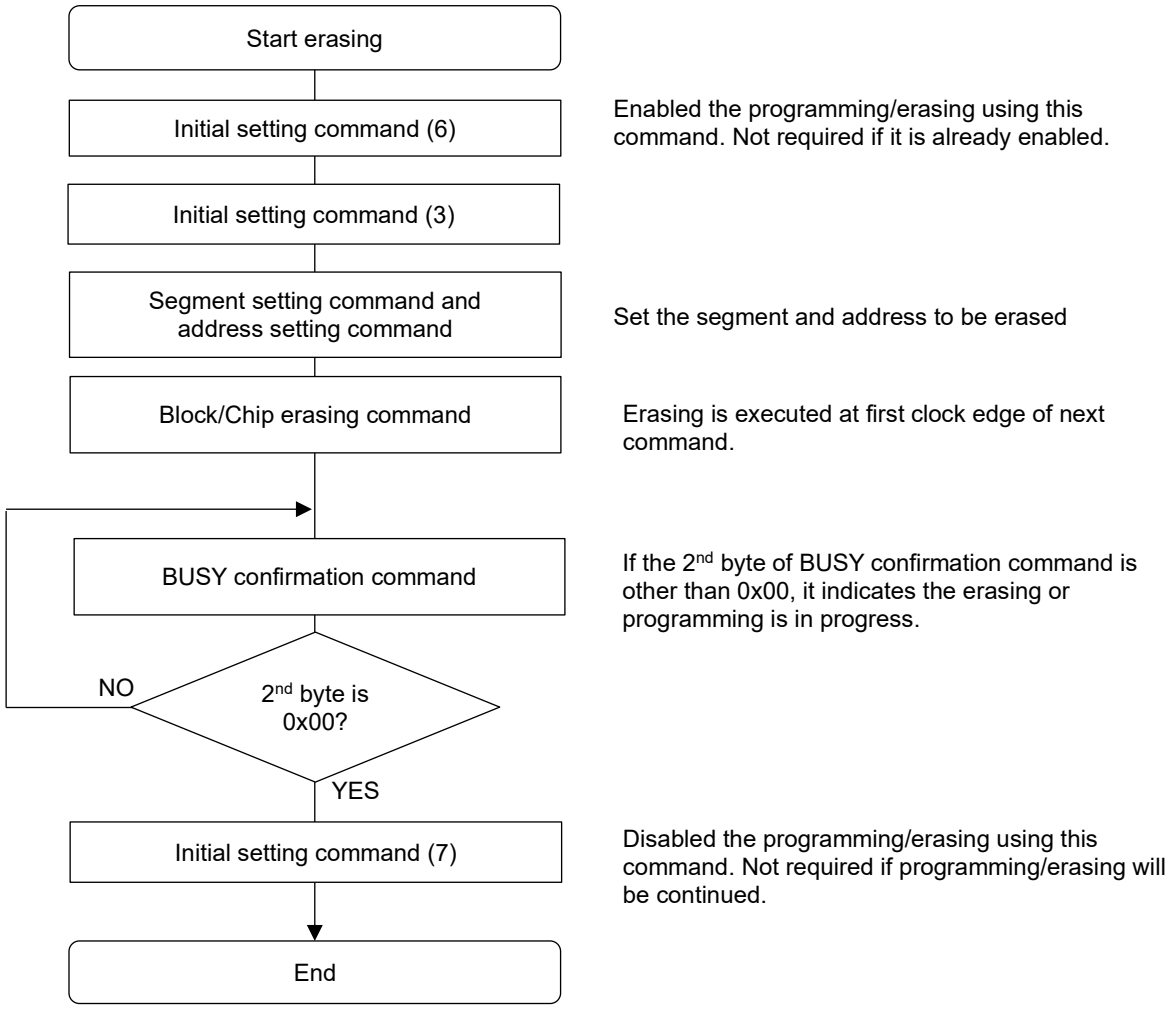


Figure 26-9 Flow Diagram for Erasing in Specified Flash Memory Area

[Note]

- **Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing".**
- **Transmit any command after 'initial setting command (7)' if other command will not be transmit.**

26.4.5.3 Programming to Specified Flash Memory Area

Figure 26-10 shows the flow diagram for programming to the specified flash memory area.

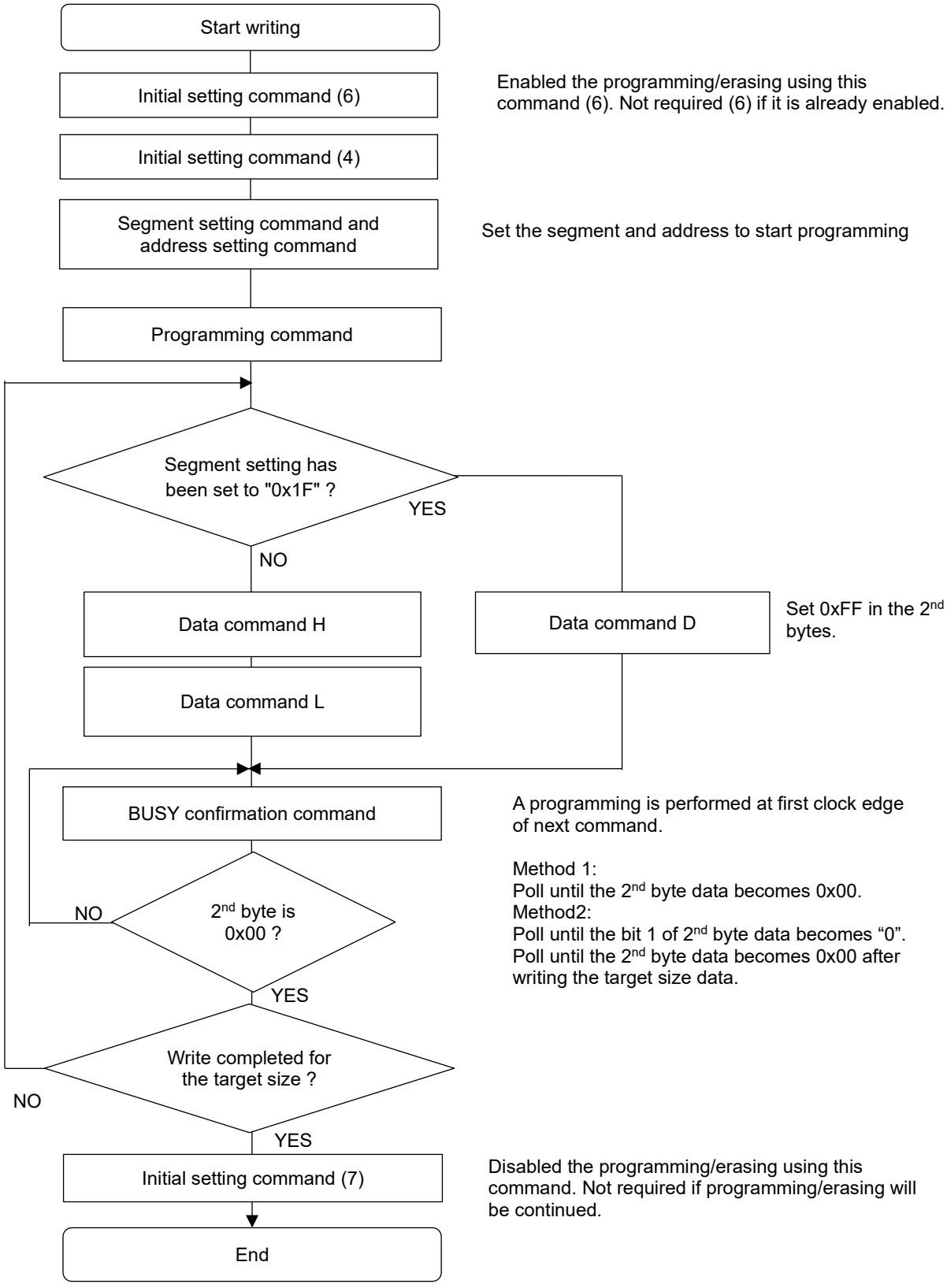


Figure 26-10 Flow Diagram for Programming to Specified Flash Memory Area

[Note]

- **Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing".**
- **Transmit any command after ‘initial setting command (7)’ if other command will not be transmit.**

26.4.5.4 Verifying data in Specified Flash Memory Area

Figure 26-11 shows the flow diagram for verifying data in the specified flash memory area.

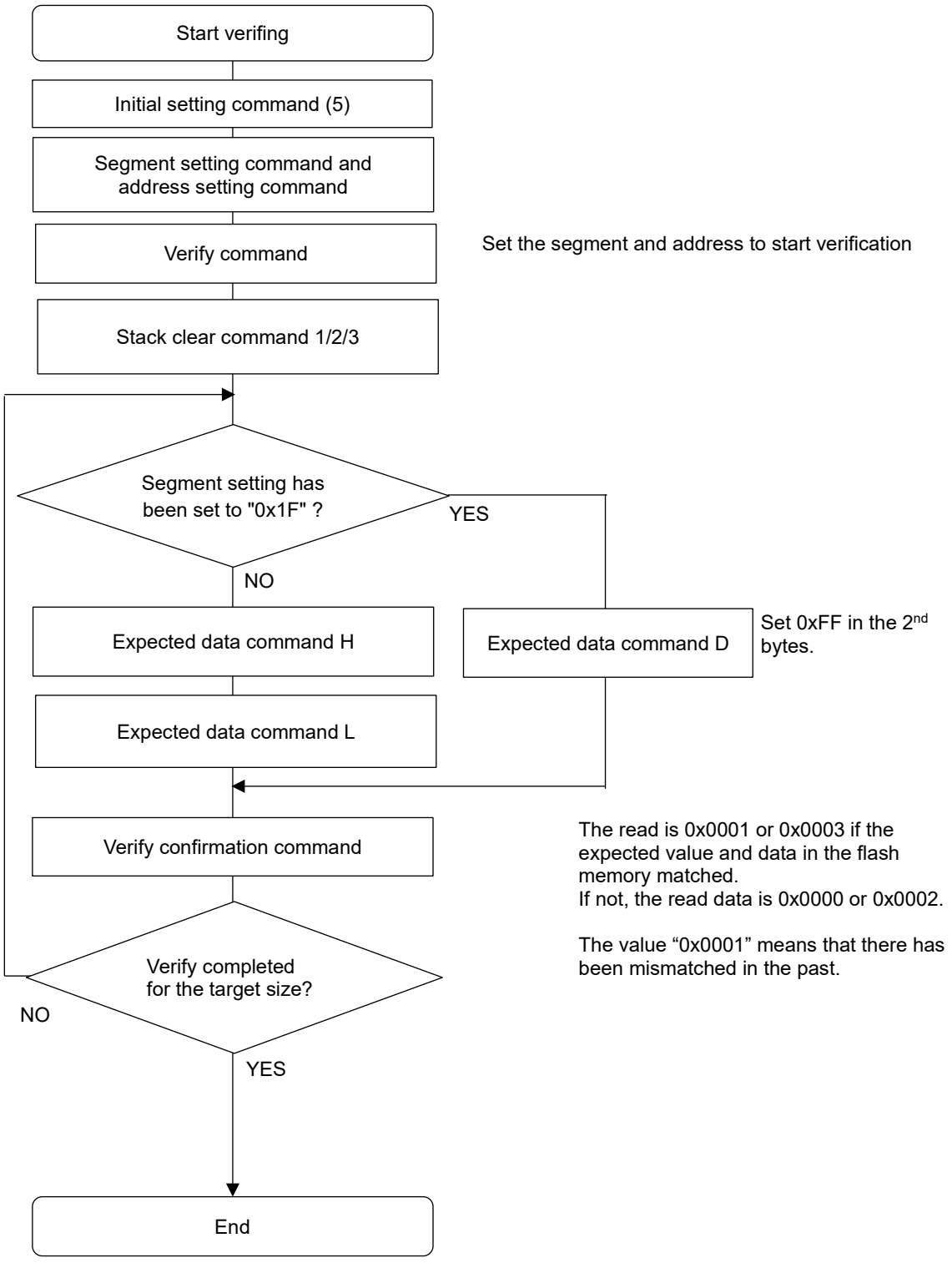


Figure 26-11 Flow Diagram for Verifying Specified Flash Memory Area

[Note]

- **Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing".**

26.4.6 Advanced Control of Flash Memory Erasing/Programming

This section describes how to implement shorter Flash memory erasing/programing/verify time.

The programming flow shown in section 26.4.5.3 is to confirm the busy signal after transmitting the erase command or the programming data before transmitting a next command or data. The processing time is reducible by transmitting the commands during the time the BUSY signal is released (t_{busy}).

The mismatch results are stacked, so the confirming each sending expect data is not needed. The stacked result is cleared by clear command.

26.4.6.1 Timing to transmit command of Advanced Control

The LSI executes erasing/programming instructions to the Flash memory when it receives commands for the erasing/programming. It requires the Busy time (t_{busy}) as an interval time to accept the next communication command. Therefore, transmit the communication commands for erasing/programming the Flash memory with an interval of longer than t_{busy}.

The timing of command transmit is calculated as follows.
Command transfer time : t_{cmd} = (24[bit] / transfer rate[bps])
Wait time : t_{wait} = Busy time : t_{busy} – (t_{cmd} × number of commands)

Figure 26-12 shows an example of command transmit for programming with using BUSY confirmation command.
When the transfer rate is 2Mbps and programming data in program code area:
Send the commands so that the interval between the first clocks of the two “BUSY confirmation command” is t_{busy} or more.

t_{cmd} = 24 bit / 2Mbps = 12 [µs]
t_{wait} = t_{busy} – (t_{cmd} × 2) = 80 – 12 × 2 = 56 [µs]

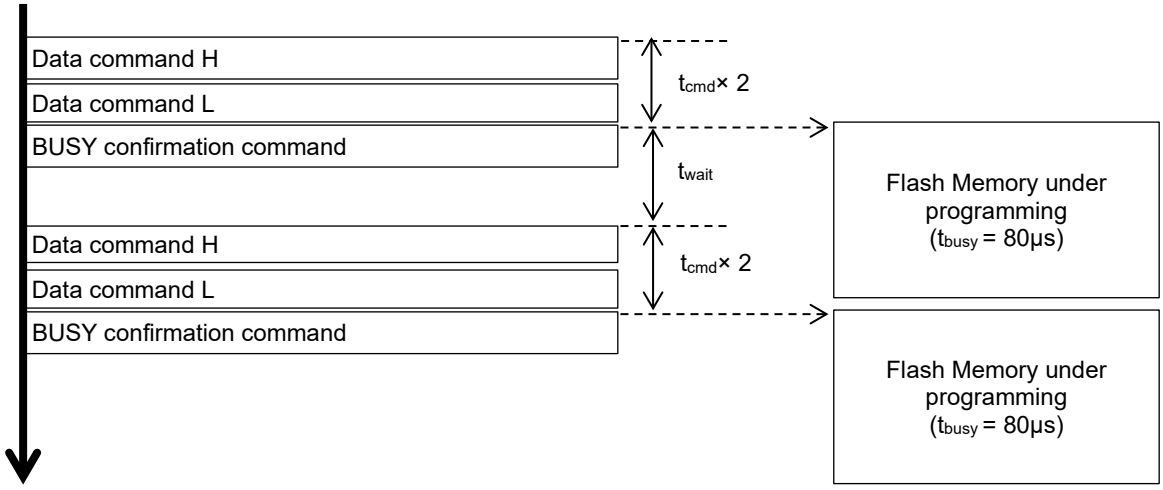


Figure 26-12 Advanced control #1 of programming the program code area

Figure 26-13 shows an example of using “data command H” instead of “BUSY confirmation command”.

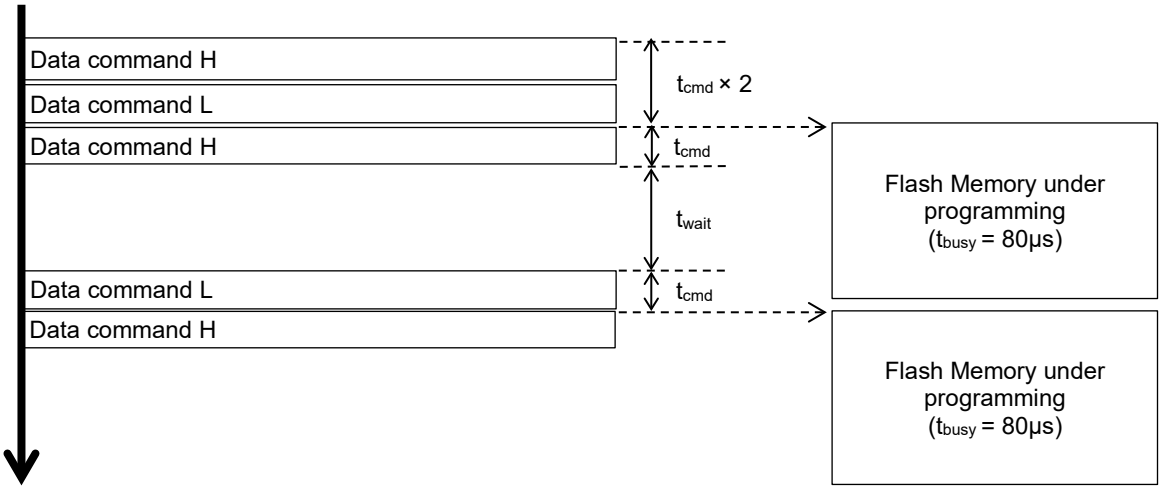


Figure 26-13 Advanced control #2 of programming the program code area

Figure 26-14 shows an example for programming to data flash area.
When the transfer rate is 2Mbps and programming data in data flash area:
Send the command “Data command D” so that the command acceptance interval is t_{busy} or more.

t_{cmd} = 24 bit / 2Mbps = 12 [μs]
t_{wait} = t_{busy} – (t_{cmd} × 1) = 40 – 12 × 1 = 28 [μs]

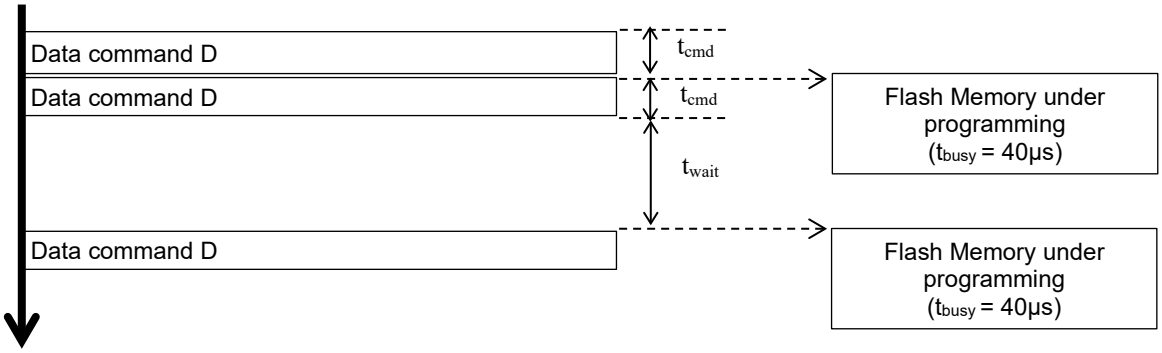


Figure 26-14 Advanced control of programming to the data flash

26.4.6.2 Erasing Data in Specified Flash Memory Area (Advanced control)

Figure 26-15 shows the flow diagram for erasing the specified flash memory area by the advanced control.

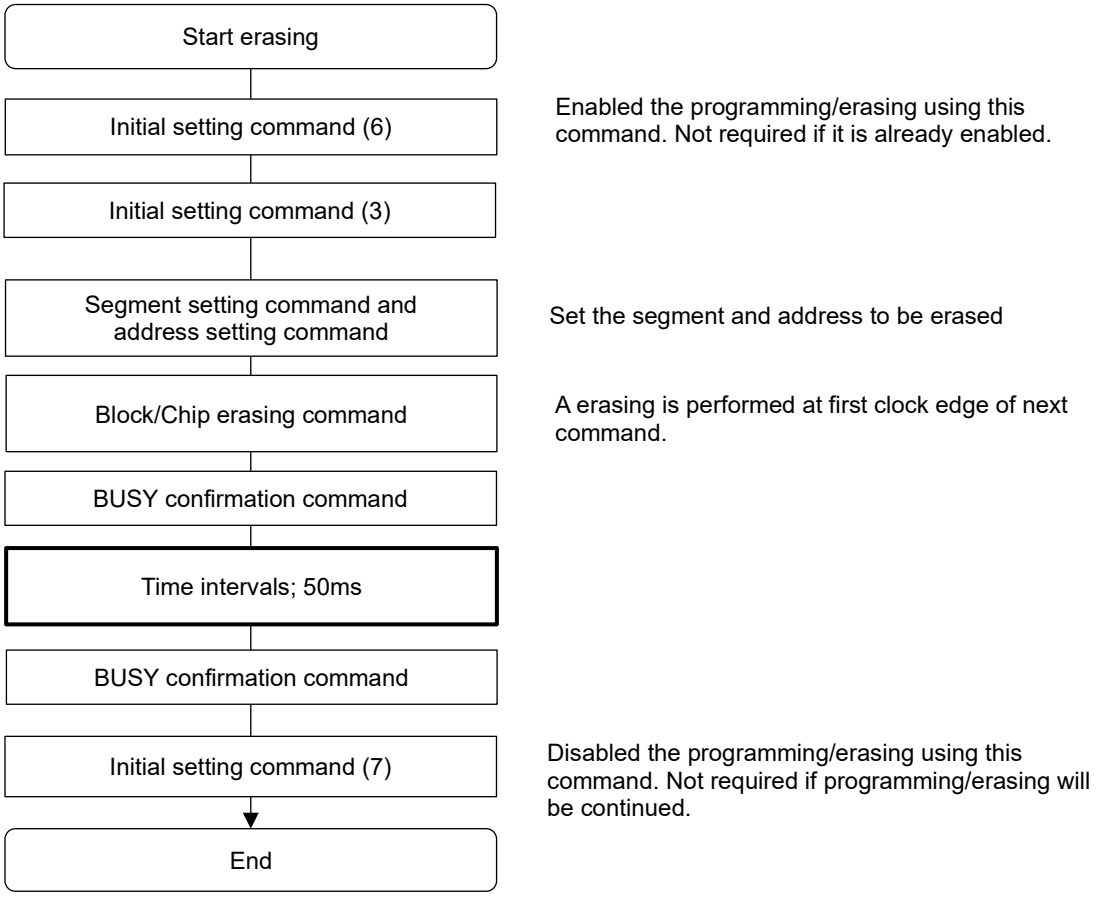


Figure 26-15 Flow Diagram for Erasing Specified Flash Memory Area (Advanced Control)

[Note]
- **Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing".**
- **Transmit any command after 'initial setting command (7)' if other command will not be transmitted.**

26.4.6.3 Programming to Specified Flash Memory Area (Advanced control)

Figure 26-16 shows the flow diagram for programming to the specified flash memory area by the advanced control.

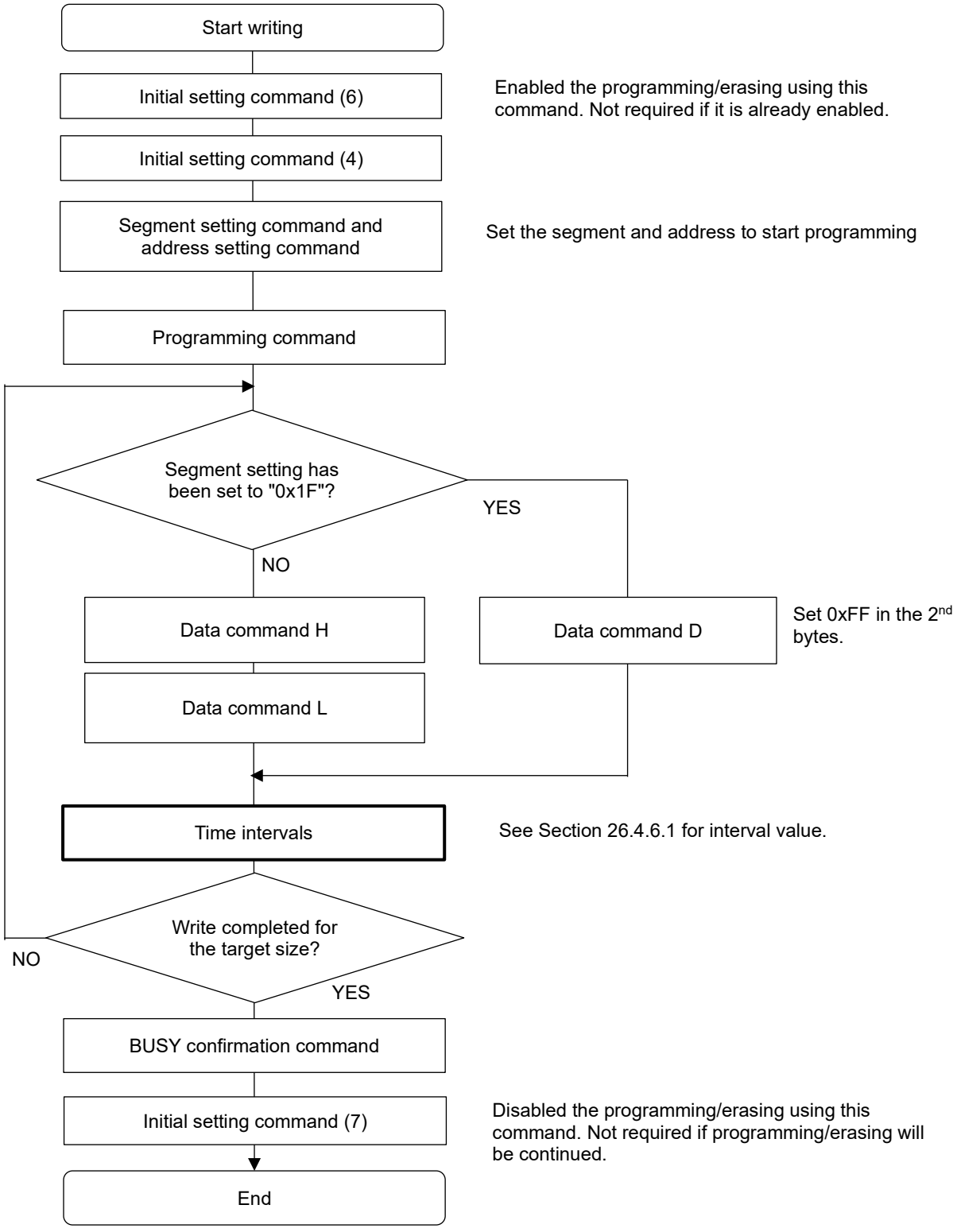


Figure 26-16 Flow Diagram for Programming Specified Flash Memory Area (Advanced Control)

[Note]

- **Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing.**
- **Transmit any command after 'initial setting command (7)' if other command will not be transmitted.**

26.4.6.4 Verifying Data in Specified Flash Memory Area (Advanced control)

Figure 26-17 shows the flow diagram for verifying data in the specified flash memory area by the advanced control.

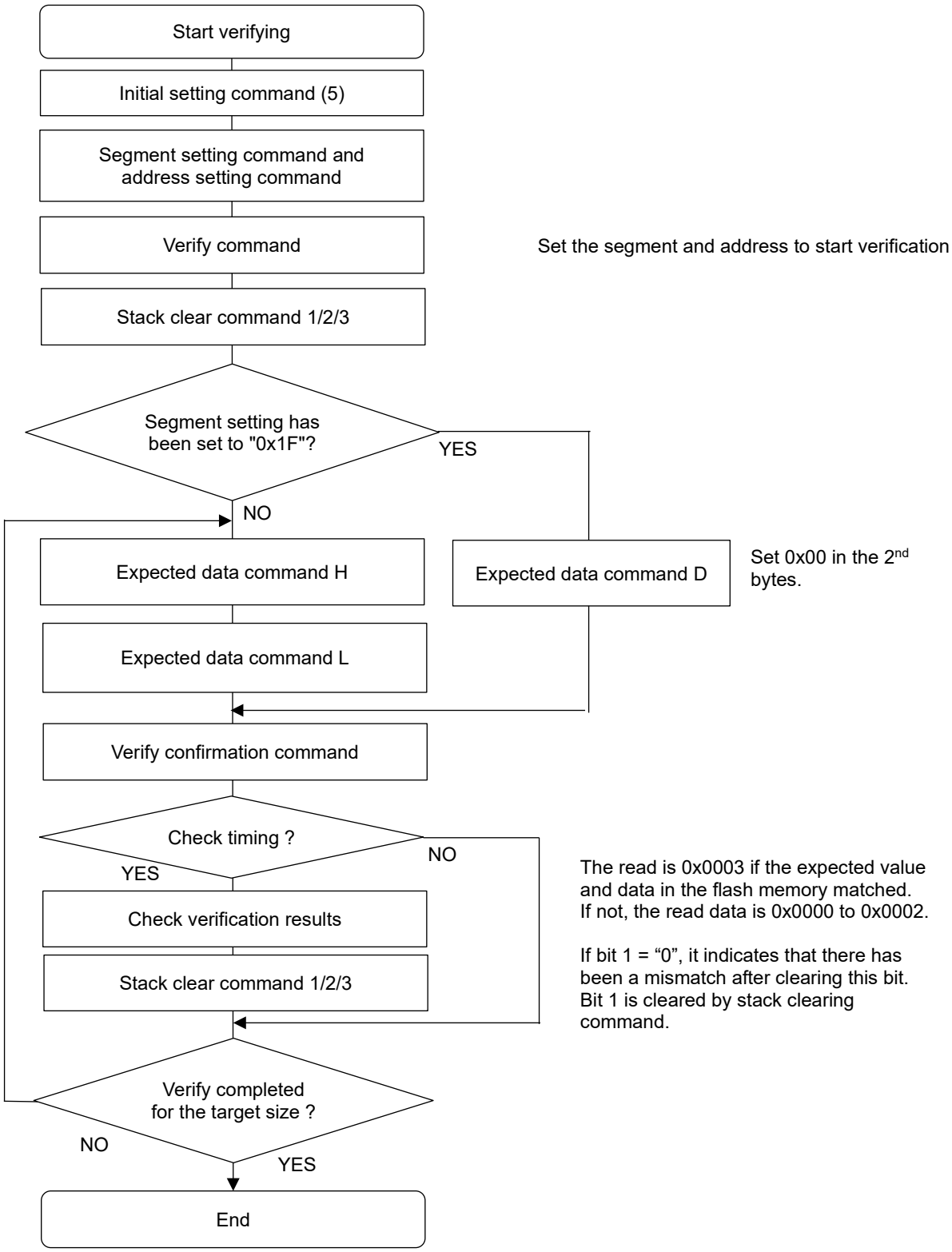


Figure 26-17 Flow Diagram for Verifying Specified Flash Memory Area (advanced control)

[Note]
- **Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing".**
- **Transmit any command after ‘stack clear command 3’ if other command will not be transmitted.**

Chapter 27 LCD Driver

27. LCD driver

27.1 General Description

The ML62Q2700 gropup has the LCD driver that displays the contents of display register 00 to 64 onto a LCD panel.

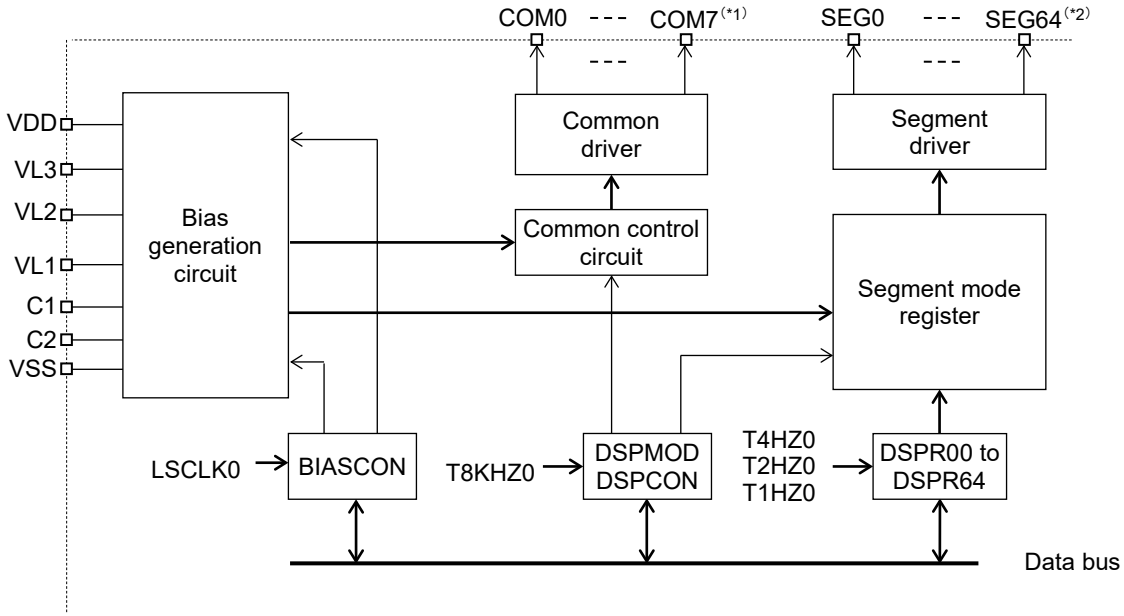
27.1.1 Features

- Max.480 dots
  ML62Q2745/ML62Q2746/ML62Q2747 : 60seg×8com(com Max.), 65seg×3com(seg Max.)
  ML62Q2735/ML62Q2736/ML62Q2737 : 45seg×8com(com Max.), 50seg×3com(seg Max.)
  ML62Q2725/ML62Q2726/ML62Q2727 : 35seg×8com(com Max.), 40seg×3com(seg Max.)
  ML62Q2722/ML62Q2723 : 35seg×8com(com Max.), 40seg×3com(seg Max.)
  ML62Q2712/ML62Q2713 : 27seg×8com(com Max.), 32seg×3com(seg Max.)
  ML62Q2702/ML62Q2703 : 24seg×8com(com Max.), 29seg×3com(seg Max.)

- Unused segment/common output pins are available as general-purpose input/output pins.
- 1/1 duty to 1/8 duty
- 1/3 bias (bias generation circuit embedded)
- LCD drive waveform selectable (waveform A or B)
- Frame frequency selectable (approx. 32Hz, 38 Hz, 64 Hz, 75 Hz, 128 Hz or 150 Hz)
- LCD drive voltage generation mode selectable (internal boosting/external supply capacitive dividing/internal application dividing/external supply)
- LCD stop, LCD display, all on and all off modes selectable
- LCD tone reversal available
- LED display control available (external MOS transistors are required for driving)
- Contrast adjustment: Adjusted in 16 levels (only in the internal boosting mode)
- LCD blinking available (the upper 4 bit or lower 4 bit of display register switch automatically or by software in 1/1 to 1/4 duty mode only)

27.1.2 Configuration of LCD Display Function

Figure 27-1 shows the configuration of the LCD display function circuit.



*1: COM0 pin to COM2 pin are shared with general-purpose input/output pins.
COM3 pin to COM7 pin are shared with segment output pins or general-purpose input/output pins.

*2: SEG0 pin to SEG4 pin are shared with common output pins or general-purpose input/output pins.
SEG5 pin to SEG64 pin are shared with general-purpose input/output pins.

BIASCON	: Bias control register
DSPMOD	: Display mode register
DSPCON	: Display control register
DSPR0 0to DSPR64	: Display register 00 to 64

Figure 27-1 Configuration of LCD Driver

27.1.3 Configuration of Bias Generation Circuit

The bias generation circuit operation is selectable from the following four methods.

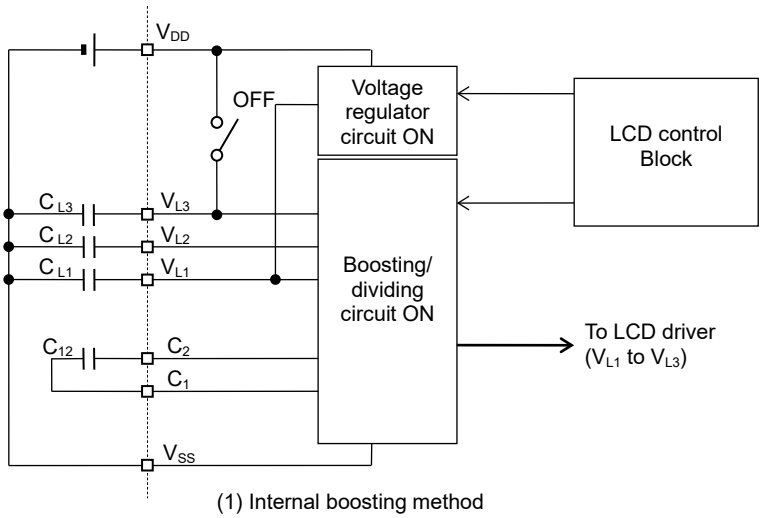
(1) Internal boosting method:
Boost the voltage (V_{L1}) generated from the internal voltage regulator circuit using the capacitor (C_{12}) to output the LCD driving voltages (V_{L1} to V_{L3}).
The display contrast can be adjusted in 16 levels using LCN4 to LCN0 bits in bias control register (BIASCON).

(2) Internal capacitive dividing method:
Connect V_{L3} to V_{DD} internally and generate V_{L2} and V_{L1} by the means of capacitance voltage division using the capacitor (C_{12}).

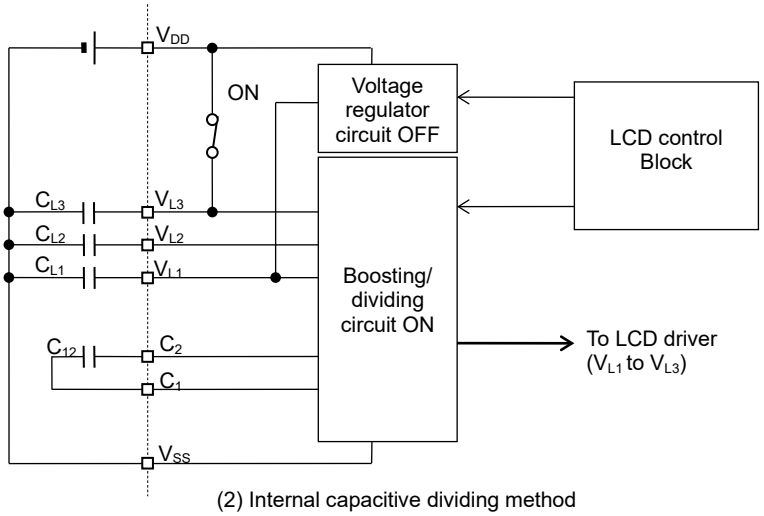
(3) External supply capacitive dividing method:
Supply a voltage to V_{L3} externally and generate V_{L2} and V_{L1} by the means of capacitance voltage division using the capacitor (C_{12}).

(4) External supply method:
Supply voltages to V_{L1} to V_{L3} externally.

Setting BSON bit of bias control register (BIASCON) to "1" starts the bias generation circuit operation. For the internal boosting method, the display contrast can be adjusted in 32 levels using LCN4 to LCN0 bits.
Figure 27-2 shows an external configuration example for each method of the bias generation circuit.

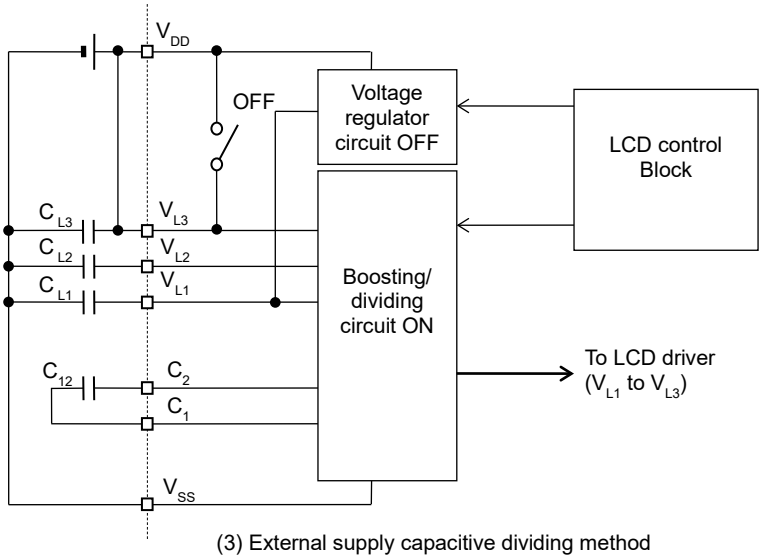


(1) Internal boosting method

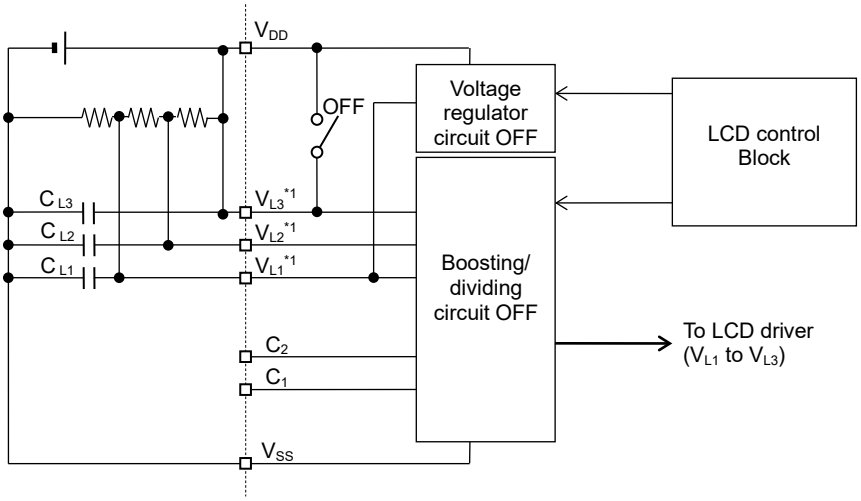


(2) Internal capacitive dividing method

Figure 27-2 External Configuration Example of Bias Generation Circuit (1)



(3) External supply capacitive dividing method



(*1) See “27.3.7 Configuration Example to drive LED” if using the LED drive mode.

(4) External supply method

Figure 27-2 External Configuration Example of Bias Generation Circuit (2)

27.1.4 List of Pins

●: Available -: Unavailable

Pin name	48pin product ML62Q2703 ML62Q2702	52pin product ML62Q2713 ML62Q2712	64pin product ML62Q2727 ML62Q2726 ML62Q2725 ML62Q2723 ML62Q2722	80pin product ML62Q2737 ML62Q2736 ML62Q2735	100pin product ML62Q2747 ML62Q2746 ML62Q2745	Function
C1	●	●	●	●	●	Capacitor connection 1 for LCD bias power generation
C2	●	●	●	●	●	Capacitor connection 2 for LCD bias power generation
VL1	●	●	●	●	●	LCD bias power supply 1
VL2	●	●	●	●	●	LCD bias power supply 2
VL3	●	●	●	●	●	LCD bias power supply 3
P04/COM0	●	●	●	●	●	General-purpose input/output/ Common output
P05/COM1	●	●	●	●	●	General-purpose input/output / Common output
P06/COM2	●	●	●	●	●	General-purpose input/output/ Common output
P07/ COM3/SEG0	●	●	●	●	●	General-purpose input/output / Common output / Segment output
P10/ COM4/SEG1	●	●	●	●	●	General-purpose input/output / Common output / Segment output
P11/ COM5/SEG2	●	●	●	●	●	General-purpose input/output / Common output / Segment output
P12/ COM6/SEG3	●	●	●	●	●	General-purpose input/output/ Common output / Segment output
P13/ COM7/SEG4	●	●	●	●	●	General-purpose input/output / Common output / Segment output
P50/SEG5	●	●	●	●	●	General-purpose input/output/ Segment output
P51/SEG6	-	●	●	●	●	General-purpose input/output / Segment output
P52/SEG7	-	-	●	●	●	General-purpose input/output / Segment output
P53/SEG8	-	-	●	●	●	General-purpose input/output/ Segment output
P90/SEG9	-	-	-	-	●	General-purpose input/output / Segment output
P91/SEG10	-	-	-	-	●	General-purpose input/output / Segment output
P92/SEG11	-	-	-	-	●	General-purpose input/output/ Segment output
P93/SEG12	-	-	-	●	●	General-purpose input/output/ Segment output
P94/SEG13	-	-	-	●	●	General-purpose input/output/ Segment output
P95/SEG14	-	-	-	●	●	General-purpose input/output/ Segment output
P96/SEG15	-	-	-	●	●	General-purpose input/output/ Segment output
P97/SEG16	-	-	-	-	●	General-purpose input/output/ Segment output
PA0/SEG17	-	-	-	-	●	General-purpose input/output/ Segment output
PA1/SEG18	-	-	-	-	●	General-purpose input/output/ Segment output
PA2/SEG19	-	-	-	-	●	General-purpose input/output/ Segment output
P54/SEG20	-	-	●	●	●	General-purpose input/output/ Segment output
P55/SEG21	-	-	●	●	●	General-purpose input/output/ Segment output

Pin name	48pin product	52pin product	64pin product	80pin product	100pin product	Function
	ML62Q2703 ML62Q2702	ML62Q2713 ML62Q2712	ML62Q2727 ML62Q2726 ML62Q2725 ML62Q2723 ML62Q2722	ML62Q2737 ML62Q2736 ML62Q2735	ML62Q2747 ML62Q2746 ML62Q2745	
P14/SEG22	●	●	●	●	●	General-purpose input/output/ Segment output
P15/SEG23	●	●	●	●	●	General-purpose input/output/ Segment output
P16/SEG24	●	●	●	●	●	General-purpose input/output/ Segment output
P17/SEG25	●	●	●	●	●	General-purpose input/output/ Segment output
P20/SEG26	●	●	●	●	●	General-purpose input/output/ Segment output
P21/SEG27	●	●	●	●	●	General-purpose input/output/ Segment output pin
P22/SEG28	●	●	●	●	●	General-purpose input/output/ Segment output
P23/SEG29	●	●	●	●	●	General-purpose input/output/ Segment output
P24/SEG30	●	●	●	●	●	General-purpose input/output/ Segment output
P25/SEG31	●	●	●	●	●	General-purpose input/output/ Segment output
P26/SEG32	●	●	●	●	●	General-purpose input/output/ Segment output
P27/SEG33	●	●	●	●	●	General-purpose input/output/ Segment output
P56/SEG34	-	●	●	●	●	General-purpose input/output/ Segment output
P57/SEG35	-	-	●	●	●	General-purpose input/output/ Segment output
PA3/SEG36	-	-	-	●	●	General-purpose input/output/ Segment output
PA4/SEG37	-	-	-	●	●	General-purpose input/output/ Segment output
PA5/SEG38	-	-	-	-	●	General-purpose input/output/ Segment output
PA6/SEG39	-	-	-	-	●	General-purpose input/output/ Segment output
PA7/SEG40	-	-	-	-	●	General-purpose input/output/ Segment output
PB0/SEG41	-	-	-	-	●	General-purpose input/output/ Segment output
PB1/SEG42	-	-	-	-	●	General-purpose input/output/ Segment output
PB2/SEG43	-	-	-	●	●	General-purpose input/output/ Segment output
PB3/SEG44	-	-	-	●	●	General-purpose input/output/ Segment output
PB4/SEG45	-	-	-	●	●	General-purpose input/output/ Segment output
PB5/SEG46	-	-	-	●	●	General-purpose input/output/ Segment output
P40/SEG47	-	-	●	●	●	General-purpose input/output/ Segment output pin
P41/SEG48	-	●	●	●	●	General-purpose input/output/ Segment output
P30/SEG49	●	●	●	●	●	General-purpose input/output/ Segment output
P31/SEG50	●	●	●	●	●	General-purpose input/output/ Segment output
P32/SEG51	●	●	●	●	●	General-purpose input/output/ Segment output

Pin name	48pin product	52pin product	64pin product	80pin product	100pin product	Function
	ML62Q2703 ML62Q2702	ML62Q2713 ML62Q2712	ML62Q2727 ML62Q2726 ML62Q2725 ML62Q2723 ML62Q2722	ML62Q2737 ML62Q2736 ML62Q2735	ML62Q2747 ML62Q2746 ML62Q2745	
P33/SEG52	●	●	●	●	●	General-purpose input/output/ Segment output
P60/SEG53	●	●	●	●	●	General-purpose input/output/ Segment output
P61/SEG54	●	●	●	●	●	General-purpose input/output/ Segment output
P62/SEG55	●	●	●	●	●	General-purpose input/output/ Segment output
P63/SEG56	●	●	●	●	●	General-purpose input/output/ Segment output
P64/SEG57	●	●	●	●	●	General-purpose input/output/ Segment output
P65/SEG58	●	●	●	●	●	General-purpose input/output/ Segment output
P66/SEG59	●	●	●	●	●	General-purpose input/output/ Segment output
P67/SEG60	-	-	●	●	●	General-purpose input/output/ Segment output
P42/SEG61	-	-	●	●	●	General-purpose input/output/ Segment output
PB6/SEG62	-	-	-	-	●	General-purpose input/output/ Segment output
PB7/SEG63	-	-	-	-	●	General-purpose input/output/ Segment output
P77/SEG64	-	-	-	-	●	General-purpose input/output/ Segment output

27.2 Description of Registers

27.2.1 List of Registers

Address	Name	Symbol(Byte)	Symbol(Word)	R/W	Size	Initial Value
0xF0F0	Bias control register	BIASCONL	BIASCON	R/W	8/16	0x08
0xF0F1		BIASCONH		R/W	8	0x00
0xF0F2	Display mode register	DSPMODL	DSPMOD	R/W	8/16	0x40
0xF0F3		DSPMODH		R/W	8	0x00
0xF0F4	Display control register	DSPCONL	DSPCON	R/W	8/16	0x00
0xF0F5		DSPCONH		R/W	8	0x00
0xF0F6	Segment mode register 0	SEGMOD0L	SEGMOD0	R/W	8/16	0x00
0xF0F7		SEGMOD0H		R/W	8	0x00
0xF0F8	Segment mode register 1	SEGMOD1L	SEGMOD1	R/W	8/16	0x00
0xF0F9		SEGMOD1H		R/W	8	0x00
0xF0FA	Segment mode register 2	SEGMOD2L	SEGMOD2	R/W	8/16	0x00
0xF0FB		SEGMOD2H		R/W	8	0x00
0xF0FC	Segment mode register 3	SEGMOD3L	SEGMOD3	R/W	8/16	0x00
0xF0FD		SEGMOD3H		R/W	8	0x00
0xF0FE	Segment mode register 4	SEGMOD4L	SEGMOD4	R/W	8/16	0x00
0xF0FF		-		R	8	0x00
0xF100 to 0xF140	Display register 00 to Display register 64	DSPR00 to DSPR64	DSPRWn (n:an even number in decimalization)	R/W	8/16	Undefined
				R/W	8	Undefined

27.2.2 Bias Control Register(BIASCON)

BIASCON is a SFR to control the bias generation circuit.
Write BIASCONL when the display turns off (when the LMD1 bit and LMD0 bit of DSPCON register are "0").
Writing to BIASCONL is disabled in other modes.

Address: 0xF0F0(BIASCONL/BIASCON), 0xF0F1(BIASCONH)
Access: R/W
Access size: 8/16bits
Initial value: 0x0008

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	BIASCON															
Byte	BIASCONH								BIASCONL							
Bit	-	-	-	LCN4	LCN3	LCN2	LCN1	LCN0	BTSEL1	BTSEL0	DSMD1	DSMD0	BSN2	BSN1	BSN0	BSON
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit No.	Bit symbol name	Description
15 to 13	-	Reserved bits
12 to 8	LCN4 to LCN0	Adjust the display contrast in 16 voltage levels. The display contrast is adjustable by controlling the V_{L1} voltage. The display contrast depends on the set value. A lower setting value turns thinner shade the contrast, and a higher setting value turns thicker shade the contrast. See the electrical characteristics in the data sheet for more details about the voltage level. Contrast (voltage) 0x00: 0.950V(initial value) 0x10: 1.350V 0x02: 1.000V 0x12: 1.400V 0x04: 1.050V 0x14: 1.450V 0x06: 1.100V 0x16: 1.500V 0x08: 1.150V 0x18: 1.550V 0x0A: 1.200V 0x1A: 1.600V 0x0C: 1.250V 0x1C: 1.650V 0x0E: 1.300V 0x1E: 1.700V
7, 6	BTSEL1, BTSEL0	Select the means of bias generation circuit operation. When driving the LED, select the external supply method. 00: External supply method (Initial value) 01: Internal boosting method 10: External supply capacitive dividing method 11: Internal capacitive dividing method
5	DSMD1	Select the display device. 0: LCD (Initial value) 1: LED
4	DSMD0	Select the black and white inversion display mode. 0: Normal display (Initial value) 1: black and white inversion display

Bit No.	Bit symbol name	Description
3 to 1	BSN2 to BSN0	Select the clock for boosting the voltage in the bias generation circuit. 000: LSCLK(32.768kHz) 001: 1/2 LSCLK(16.384kHz) 010: 1/4 LSCLK(8.192kHz) 011: 1/8 LSCLK(4.096kHz) 100: 1/16 LSCLK(2.048kHz) (Initial value) 101: 1/32 LSCLK(1.024kHz) 110: 1/64 LSCLK(512Hz) 111: 1/128 LSCLK(256Hz)
0	BSON	Control the bias generation circuit operation. Setting the BSON bit to "1" generates the LCD driving voltages (V_{L1} to V_{L3}). 0: Bias generation circuit turns off (Initial value) 1: Bias generation circuit turns on

27.2.3 Display Mode Register (DSPMOD)

DSPMODH is a SFR to control the LCD driver waveform type, frame frequency and duty .
Write DSPMODL when the display turns off (when the LMD1 bit and LMD0 bit of DPSCON register are "0").
Writing to DSPMODL is disabled in other modes.

Address: 0xF0F2(DSPMODL/DSPMOD), 0xF0F3(DSPMODH)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0040

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	DSPMOD															
Byte	DSPMODH								DSPMODL							
Bit	-	-	-	WTYPE	-	-	-	-	FRM2	FRM1	FRM0	-	DUTY3	DUTY2	DUTY1	DUTY0
R/W	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 13	-	Reserved bits
12	WTYPE	Select the LCD drive waveform. Select the waveform A when driving the LED. 0: Waveform A:reversed line (Initial value) 1: Waveform B:reversed frame
11 to 8	-	Reserved bits
7 to 5	FRM2 to FRM0	Select the frame frequency of the LCD driver. 000: Frame frequency 32 Hz 001: Frame frequency 38 Hz 010: Frame frequency 64 Hz (Initial value) 011: Frame frequency 75 Hz 100: Frame frequency 128 Hz 101: Frame frequency 150 Hz 110: Setting prohibited 111: Setting prohibited
4	-	Reserved bits
3 to 0	DUTY3 to DUTY0	These bits are used to set the display duty and common pin. For COM7 to COM3 pin functions, the settings of these bits are given priority over the segment mode register. 0000: COM pin not used (Initial value). 0001: 1/1 duty. COM0 pin used. 0010: 1/2 duty. COM0 to COM1 pins used. 0011: 1/3 duty. COM0 to COM2 pins used. 0100: 1/4 duty. COM0 to COM3 pins used. 0101: 1/5 duty. COM0 to COM4 pins used. 0110: 1/6 duty. COM0 to COM5 pins used. 0111: 1/7 duty. COM0 to COM6 pins used. 1000: 1/8 duty. COM0 to COM7 pins used. Others: Setting prohibited (COM pin not used).

27.2.4 Display Control Register (DSPCON)

DSPCON is a SFR to control the display mode.

Address: 0xF0F4(DSPCONL/DSPCON), 0xF0F5(DSPCONH)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	DSPCON															
Byte	DSPCONH								DSPCONL							
Bit	-	-	-	-	-	MMOD2	MMOD1	MMOD0	-	-	-	-	-	-	LMD1	LMD0
R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 11	-	Reserved bits
10 to 8	MMOD2 to MMOD0	Configure the data display method when 1/1 duty to 1/4 duty are set. When the duty of 1/5 to 1/8 are selected, this function is disabled. 000: Display 1: Display the lower 4-bit data of the display register00 to 64 (DSPR00 to 64) (Initial value). 001: Display 2: Display the higher 4-bit data of the display register00 to 64 (DSPR00 to 64). 010: Switching display 1: Display the data area in the display 1 and display 2 alternately every one second; nega edge of T1HZR. 011: Switching display 2: Display the data area in the display 1 and display 2 alternately every 1/2 second; nega edge of T2HZR. 100: Switching display 4: Display the data area in the display 1 and display 2 alternately every 1/4 second; nega edge of T4HZR.[*1] Others: Setting prohibited (Switching display 4) [*1]: Available only when using crystal oscillation
7 to 2	-	Reserved bits
1, 0	LMD1, LMD0	Control the LCD display. Display status — Common/segment pin status 00: Display stop (Initial). — V_{SS} level 01: All off — Normal display mode[*1] : Off waveform; Reverse display mode[*1]: On waveform 10: Display — Normal display mode[*1]: Data “1“ of display register 00 to 64 drives On waveform; Reverse display mode[*1]: Data “0“ of display register00 to 64 drives Off waveform 11: All on — Normal display mode[*1]: On waveform; Reverse display mode[*1]: Off waveform [*1]: Bias control register (BIASCON) DSMD0 bit setting

27.2.5 Segment Mode Register 0 (SEGMOD0)

SEGMOD0 is a SFR to select SEG15 to SEG0 functions.

Address: 0xF0F6(SEGMOD0L/SEGMOD0), 0xF0F7(SEGMOD0H)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SEGMOD0															
Byte	SEGMOD0H								SEGMOD0L							
Bit	S15MD	S14MD	S13MD	S12MD	S11MD	S10MD	S9MD	S8MD	S7MD	S6MD	S5MD	S4MD	S3MD	S2MD	S1MD	S0MD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	S15MD	Select the general-purpose input/output and segment output functions. 0: P96 (Initial value) 1: SEG15
14	S14MD	Select the general-purpose input/output and segment output functions. 0: P95 (Initial value) 1: SEG14
13	S13MD	Select the general-purpose input/output and segment output functions. 0: P94 (Initial value) 1: SEG13
12	S12MD	Select the general-purpose input/output and segment output functions. 0: P93 (Initial value) 1: SEG12
11	S11MD	Select the general-purpose input/output and segment output functions. 0: P92 (Initial value) 1: SEG11
10	S10MD	Select the general-purpose input/output and segment output functions. 0: P91 (Initial value) 1: SEG10
9	S9MD	Select the general-purpose input/output and segment output functions. 0: P90 (Initial value) 1: SEG9
8	S8MD	Select the general-purpose input/output and segment output functions. 0: P53 (Initial value) 1: SEG8
7	S7MD	Select the general-purpose input/output and segment output functions. 0: P52 (Initial value) 1: SEG7
6	S6MD	Select the general-purpose input/output and segment output functions. 0: P51. (Initial value) 1: SEG6.
5	S5MD	Select the general-purpose input/output and segment output functions. 0: P50 (Initial value) 1: SEG5

Bit No.	Bit symbol name	Description
4	S4MD	Select the general-purpose input/output and segment output functions. 0: P13 (Initial value) 1: SEG4
3	S3MD	Select the general-purpose input/output and segment output functions. 0: P12 (Initial value) 1: SEG3
2	S2MD	Select the general-purpose input/output and segment output functions. 0: P11 (Initial value) 1: SEG2
1	S1MD	Select the general-purpose input/output and segment output functions. 0: P10 (Initial value) 1: SEG1
0	S0MD	Select the general-purpose input/output and segment output functions. 0: P07 (Initial value) 1: SEG0

[Note]

- **If the SEGMOD0 register is set in the display state, there is a risk of erroneous display or panel damage, so set it in the display stop state (LMD1, LMD0=00 in the DSPCON register).**

27.2.6 Segment Mode Register 1(SEGMOD1)

SEGMOD1 is a SFR to select the SEG31 to SEG16 functions.

Address: 0xF0F8(SEGMOD1L/SEGMOD1), 0xF0F9(SEGMOD1H)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SEGMOD1															
Byte	SEGMOD1H								SEGMOD1L							
Bit	S31MD	S30MD	S29MD	S28MD	S27MD	S26MD	S25MD	S24MD	S23MD	S22MD	S21MD	S20MD	S19MD	S18MD	S17MD	S16MD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	S31MD	Select the general-purpose input/output and segment output functions. 0: P25 (Initial value) 1: SEG31
14	S30MD	Select the general-purpose input/output and segment output functions. 0: P24 (Initial value) 1: SEG30
13	S29MD	Select the general-purpose input/output and segment output functions. 0: P23 (Initial value) 1: SEG29
12	S28MD	Select the general-purpose input/output and segment output functions. 0: P22 (Initial value) 1: SEG28
11	S27MD	Select the general-purpose input/output and segment output functions. 0: P21 (Initial value) 1: SEG27
10	S26MD	Select the general-purpose input/output and segment output functions. 0: P20 (Initial value) 1: SEG26
9	S25MD	Select the general-purpose input/output and segment output functions. 0: P17 (Initial value) 1: SEG25
8	S24MD	Select the general-purpose input/output and segment output functions. 0: P16 (Initial value) 1: SEG24
7	S23MD	Select the general-purpose input/output and segment output functions. 0: P15 (Initial value) 1: SEG23
6	S22MD	Select the general-purpose input/output and segment output functions. 0: P14 (Initial value) 1: SEG22
5	S21MD	Select the general-purpose input/output and segment output functions. 0: P55 (Initial value) 1: SEG21

Bit No.	Bit symbol name	Description
4	S20MD	Select the general-purpose input/output and segment output functions. 0: P54 (Initial value) 1: SEG20
3	S19MD	Select the general-purpose input/output and segment output functions. 0: PA2 (Initial value) 1: SEG19
2	S18MD	Select the general-purpose input/output and segment output functions. 0: PA1 (Initial value) 1: SEG18
1	S17MD	Select the general-purpose input/output and segment output functions. 0: PA0 (Initial value) 1: SEG17
0	S16MD	Select the general-purpose input/output and segment output functions. 0: P97 (Initial value) 1: SEG16

[Note]

- **If the SEGMOD1 register is set in the display state, there is a risk of erroneous display or panel damage, so set it in the display stop state (LMD1, LMD0=00 in the DSPCON register).**
-

27.2.7 Segment Mode Register 2(SEGMOD2)

SEGMOD2 is a SFR to select the SEG47 to SEG32 functions.

Address: 0xF0FA(SEGMOD2L/SEGMOD2), 0xF0FB(SEGMOD2H)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SEGMOD2															
Byte	SEGMOD2H								SEGMOD2L							
Bit	S47MD	S46MD	S45MD	S44MD	S43MD	S42MD	S41MD	S40MD	S39MD	S38MD	S37MD	S36MD	S35MD	S34MD	S33MD	S32MD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	S47MD	Select the general-purpose input/output and segment output functions. 0: P40 (Initial value) 1: SEG47
14	S46MD	Select the general-purpose input/output and segment output functions. 0: PB5 (Initial value) 1: SEG46
13	S45MD	Select the general-purpose input/output and segment output functions. 0: PB4 (Initial value) 1: SEG45
12	S44MD	Select the general-purpose input/output and segment output functions. 0: PB3 (Initial value) 1: SEG44
11	S43MD	Select the general-purpose input/output and segment output functions. 0: PB2 (Initial value) 1: SEG43
10	S42MD	Select the general-purpose input/output and segment output functions. 0: PB1 (Initial value) 1: SEG42
9	S41MD	Select the general-purpose input/output and segment output functions. 0: PB0 (Initial value) 1: SEG41
8	S40MD	Select the general-purpose input/output and segment output functions. 0: PA7 (Initial value) 1: SEG40
7	S39MD	Select the general-purpose input/output and segment output functions. 0: PA6 (Initial value) 1: SEG39
6	S38MD	Select the general-purpose input/output and segment output functions. 0: PA5 (Initial value) 1: SEG38
5	S37MD	Select the general-purpose input/output and segment output functions. 0: PA4 (Initial value) 1: SEG37

Bit No.	Bit symbol name	Description
4	S36MD	Select the general-purpose input/output and segment output functions. 0: PA3 (Initial value) 1: SEG36
3	S35MD	Select the general-purpose input/output and segment output functions. 0: P57 (Initial value) 1: SEG35
2	S34MD	Select the general-purpose input/output and segment output functions. 0: P56 (Initial value) 1: SEG34
1	S33MD	Select the general-purpose input/output and segment output functions. 0: P27 (Initial value) 1: SEG33
0	S32MD	Select the general-purpose input/output and segment output functions. 0: P26 (Initial value) 1: SEG32

[Note]

- **If the SEGMOD2 register is set in the display state, there is a risk of erroneous display or panel damage, so set it in the display stop state (LMD1, LMD0=00 in the DSPCON register).**

27.2.8 Segment Mode Register 3(SEGMOD3)

SEGMOD3 is SFR to select the SEG63 to SEG48 functions.

Address: 0xF0FC(SEGMOD3L/SEGMOD3), 0xF0FD(SEGMOD3H)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SEGMOD3															
Byte	SEGMOD3H								SEGMOD3L							
Bit	S63MD	S62MD	S61MD	S60MD	S59MD	S58MD	S57MD	S56MD	S55MD	S54MD	S53MD	S52MD	S51MD	S50MD	S49MD	S48MD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15	S63MD	Select the general-purpose input/output and segment output functions. 0: PB7 (Initial value) 1: SEG63
14	S62MD	Select the general-purpose input/output and segment output functions. 0: PB6 (Initial value) 1: SEG62
13	S61MD	Select the general-purpose input/output and segment output functions. 0: P42 (Initial value) 1: SEG61
12	S60MD	Select the general-purpose input/output and segment output functions. 0: P67 (Initial value) 1: SEG60
11	S59MD	Select the general-purpose input/output and segment output functions. 0: P66 (Initial value) 1: SEG59
10	S58MD	Select the general-purpose input/output and segment output functions. 0: P65 (Initial value) 1: SEG58
9	S57MD	Select the general-purpose input/output and segment output functions. 0: P64 (Initial value) 1: SEG57
8	S56MD	Select the general-purpose input/output and segment output functions. 0: P63 (Initial value) 1: SEG56
7	S55MD	Select the general-purpose input/output and segment output functions. 0: P62 (Initial value) 1: SEG55
6	S54MD	Select the general-purpose input/output and segment output functions. 0: P61 (Initial value) 1: SEG54
5	S53MD	Select the general-purpose input/output and segment output functions. 0: P60 (Initial value) 1: SEG53

Bit No.	Bit symbol name	Description
4	S52MD	Select the general-purpose input/output and segment output functions. 0: P33 (Initial value) 1: SEG52
3	S51MD	Select the general-purpose input/output and segment output functions. 0: P32 (Initial value) 1: SEG51
2	S50MD	Select the general-purpose input/output and segment output functions. 0: P31 (Initial value) 1: SEG50
1	S49MD	Select the general-purpose input/output and segment output functions. 0: P30 (Initial value) 1: SEG49
0	S48MD	Select the general-purpose input/output and segment output functions. 0: P41 (Initial value) 1: SEG48

[Note]

- **If the SEGMOD3 register is set in the display state, there is a risk of erroneous display or panel damage, so set it in the display stop state (LMD1, LMD0=00 in the DSPCON register).**

27.2.9 Segment Mode Register 4 (SEGMOD4)

SEGMOD4 is SFR to select the SEG64 functions.

Address: 0xF0FE(SEGMOD4L)
Access: R/W
Access size: 8/16 bits
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SEGMOD4															
Byte	-								SEGMOD4L							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	S64MD
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 1	-	Reserved bits
0	S64MD	Select the general-purpose input/output and segment output functions. 0: P77 (Initial value) 1: SEG64

[Note]

- **If the SEGMOD4 register is set in the display state, there is a risk of erroneous display or panel damage, so set it in the display stop state (LMD1, LMD0=00 in the DSPCON register).**

27.2.10 Display Register00 to 64 (DSPR00 to DSPR64)

DSPR00 to DSPR64 are SFR to store the display data.
As the initial value of these registers are undefined, set data tbefore display.

Address: 0xF100(DSPRW00/DSPR00), 0xF101(DSPR01), 0xF102(DSPRW02/DSPR02), 0xF103(DSPR03), 0xF104(DSPRW04/DSPR04), 0xF105(DSPR05), 0xF106(DSPRW06/DSPR06), 0xF107(DSPR07), 0xF108(DSPRW08/DSPR08), 0xF109(DSPR09), 0xF10A(DSPRW10/DSPR10), 0xF10B(DSPR11), 0xF10C(DSPRW12/DSPR12), 0xF10D(DSPR13), 0xF10E(DSPRW14/DSPR14), 0xF10F(DSPR15), 0xF110(DSPRW16/DSPR16), 0xF111(DSPR17), 0xF112(DSPRW18/DSPR18), 0xF113(DSPR19), 0xF114(DSPRW20/DSPR20), 0xF115(DSPR21), 0xF116(DSPRW22/DSPR22), 0xF117(DSPR23), 0xF118(DSPRW24/DSPR24), 0xF119(DSPR25), 0xF11A(DSPRW26/DSPR26), 0xF11B(DSPR27), 0xF11C(DSPRW28/DSPR28), 0xF11D(DSPR29), 0xF11E(DSPRW30/DSPR30), 0xF11F(DSPR31), 0xF120(DSPRW32/DSPR32), 0xF121(DSPR33), 0xF122(DSPRW34/DSPR34), 0xF123(DSPR35), 0xF124(DSPRW36/DSPR36), 0xF125(DSPR37), 0xF126(DSPRW38/DSPR38), 0xF127(DSPR39), 0xF128(DSPRW40/DSPR40), 0xF129(DSPR41), 0xF12A(DSPRW42/DSPR42), 0xF12B(DSPR43), 0xF12C(DSPRW44/DSPR44), 0xF12D(DSPR45), 0xF12E(DSPRW46/DSPR46), 0xF12F(DSPR47), 0xF130(DSPRW48/DSPR48), 0xF131(DSPR49), 0xF132(DSPRW50/DSPR50), 0xF133(DSPR51), 0xF134(DSPRW52/DSPR52), 0xF135(DSPR53), 0xF136(DSPRW54/DSPR54), 0xF137(DSPR55), 0xF138(DSPRW56/DSPR56), 0xF139(DSPR57), 0xF13A(DSPRW58/DSPR58), 0xF13B(DSPR59), 0xF13C(DSPRW60/DSPR60), 0xF13D(DSPR61), 0xF13E(DSPRW62/DSPR62), 0xF13F(DSPR63), 0xF140(DSPRW64/DSPR64),
Initial value: R/W
Access size: 8/16 bits
Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	DSPRWn															
Byte	DSPRm								DSPRn							
Bit	C7	C6	C5	C4	C3	C2	C1	C0	C7	C6	C5	C4	C3	C2	C1	C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

m: odd number (ex. 01, 03, 05, ・・・63)
n: even number (ex. 00, 02, 04, ・・・64)

Bit No.	Bit symbol name	Description
15 to 8	C7 to C0	Select drive off waveform or drive on waveform。 0: Drive Off waveform 1: Drive On waveform
7 to 0	C7 to C0	Select drive off waveform or drive on waveform。 0: Drive Off waveform 1: Drive On waveform

Table 27-1 shows a list of registers available for each product.
"-" means the register does not exist and writing to register is invalid and "0" is read.

Table 27-1 List of Display Registers

●: Available -: Unavailable

Register name	Address	Corresponding segment	48pin product	52pin product	64pin product	80pin product	100pin product
			ML62Q2703 ML62Q2702	ML62Q2713 ML62Q2712	ML62Q2727 ML62Q2726 ML62Q2725 ML62Q2723 ML62Q2722	ML62Q2737 ML62Q2736 ML62Q2735	ML62Q2747 ML62Q2746 ML62Q2745
DSPR00	0xF100	SEG0	●	●	●	●	●
DSPR01	0xF101	SEG1	●	●	●	●	●
DSPR02	0xF102	SEG2	●	●	●	●	●
DSPR03	0xF103	SEG3	●	●	●	●	●
DSPR04	0xF104	SEG4	●	●	●	●	●
DSPR05	0xF105	SEG5	●	●	●	●	●
DSPR06	0xF106	SEG6	-	●	●	●	●
DSPR07	0xF107	SEG7	-	-	●	●	●
DSPR08	0xF108	SEG8	-	-	●	●	●
DSPR09	0xF109	SEG9	-	-	-	-	●
DSPR10	0xF10A	SEG10	-	-	-	-	●
DSPR11	0xF10B	SEG11	-	-	-	-	●
DSPR12	0xF10C	SEG12	-	-	-	●	●
DSPR13	0xF10D	SEG13	-	-	-	●	●
DSPR14	0xF10E	SEG14	-	-	-	●	●
DSPR15	0xF10F	SEG15	-	-	-	●	●
DSPR16	0xF110	SEG16	-	-	-	-	●
DSPR17	0xF111	SEG17	-	-	-	-	●
DSPR18	0xF112	SEG18	-	-	-	-	●
DSPR19	0xF113	SEG19	-	-	-	-	●
DSPR20	0xF114	SEG20	-	-	●	●	●
DSPR21	0xF115	SEG21	-	-	●	●	●
DSPR22	0xF116	SEG22	●	●	●	●	●
DSPR23	0xF117	SEG23	●	●	●	●	●
DSPR24	0xF118	SEG24	●	●	●	●	●
DSPR25	0xF119	SEG25	●	●	●	●	●
DSPR26	0xF11A	SEG26	●	●	●	●	●
DSPR27	0xF11B	SEG27	●	●	●	●	●
DSPR28	0xF11C	SEG28	●	●	●	●	●
DSPR29	0xF11D	SEG29	●	●	●	●	●
DSPR30	0xF11E	SEG30	●	●	●	●	●
DSPR31	0xF11F	SEG31	●	●	●	●	●
DSPR32	0xF120	SEG32	●	●	●	●	●
DSPR33	0xF121	SEG33	●	●	●	●	●
DSPR34	0xF122	SEG34	-	●	●	●	●
DSPR35	0xF123	SEG35	-	-	●	●	●
DSPR36	0xF124	SEG36	-	-	-	●	●
DSPR37	0xF125	SEG37	-	-	-	●	●
DSPR38	0xF126	SEG38	-	-	-	-	●
DSPR39	0xF127	SEG39	-	-	-	-	●
DSPR40	0xF128	SEG40	-	-	-	-	●
DSPR41	0xF129	SEG41	-	-	-	-	●

Register name	Address	Corresponding segment	48pin product	52pin product	64pin product	80pin product	100pin product
			ML62Q2703 ML62Q2702	ML62Q2713 ML62Q2712	ML62Q2727 ML62Q2726 ML62Q2725 ML62Q2723 ML62Q2722	ML62Q2737 ML62Q2736 ML62Q2735	ML62Q2747 ML62Q2746 ML62Q2745
DSPR42	0xF12A	SEG42	-	-	-	-	●
DSPR43	0xF12B	SEG43	-	-	-	●	●
DSPR44	0xF12C	SEG44	-	-	-	●	●
DSPR45	0xF12D	SEG45	-	-	-	●	●
DSPR46	0xF12E	SEG46	-	-	-	●	●
DSPR47	0xF12F	SEG47	-	-	●	●	●
DSPR48	0xF130	SEG48	-	●	●	●	●
DSPR49	0xF131	SEG49	●	●	●	●	●
DSPR50	0xF132	SEG50	●	●	●	●	●
DSPR51	0xF133	SEG51	●	●	●	●	●
DSPR52	0xF134	SEG52	●	●	●	●	●
DSPR53	0xF135	SEG53	●	●	●	●	●
DSPR54	0xF136	SEG54	●	●	●	●	●
DSPR55	0xF137	SEG55	●	●	●	●	●
DSPR56	0xF138	SEG56	●	●	●	●	●
DSPR57	0xF139	SEG57	●	●	●	●	●
DSPR58	0xF13A	SEG58	●	●	●	●	●
DSPR59	0xF13B	SEG59	●	●	●	●	●
DSPR60	0xF13C	SEG60	-	-	●	●	●
DSPR61	0xF13D	SEG61	-	-	●	●	●
DSPR62	0xF13E	SEG62	-	-	-	-	●
DSPR63	0xF13F	SEG63	-	-	-	-	●
DSPR64	0xF140	SEG64	-	-	-	-	●

27.3 Description of Operation

27.3.1 Operation of LCD Driver Circuit

Figure 27-3 shows the LCD driver circuit operation.

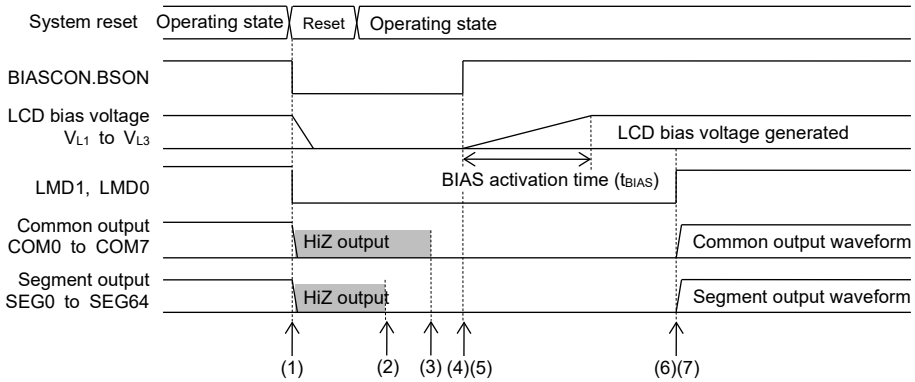


Figure 27-3 LCD Driver Circuit Operation

(1) A system reset stops the operation of bias generation circuit and LCD driver, and the common output and segment output pins enter high impedance state.
(2) Select the segment to be used by setting the segment mode register0 to 4. The selected segment pin outputs Vss level.
(3) Set the frame frequency and the duty by the display mode register (DSPMOD).
V_{SS} level is output from the common output pin corresponding to the setting duty.
(4) Set the bias generation circuit operation mode by setting the bias control register (BIASCON).
(5) When using a display mode other than the external supply mode, turn on the bias generation circuit (BSON="1") with the bias control register (BIACON).
(6) Set display data in the display registers00 to 64 (DSPR00 to DSPR64).
(7) After waiting for more than the bias generation circuit start up time (t_{BIAS}), set the display mode by configuring the LMD1 and LMD0 bits of the display control register (DSPCON). (The display waveform is output from common output and segment output pins.)
For the bias generation circuit start up time (t_{BIAS}), refer to the electrical characteristics in the data sheet.

27.3.2 Display Register Segment Map

Figure 27-4 shows the segment map configuration of the display registers00 to 64 (DSPR00 to DSPR64).

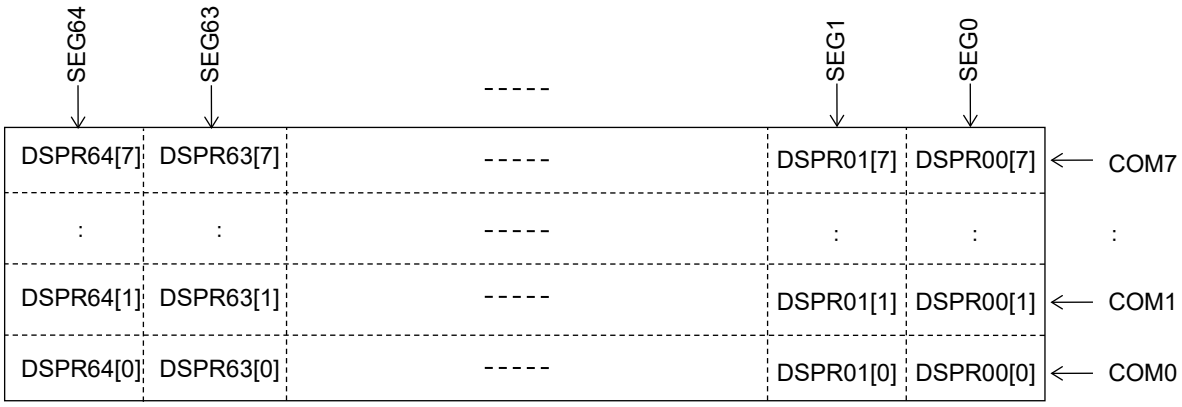


Figure 27-4 Display Register Segment Map Configuration

27.3.3 Common Output Waveform

Figure 27-5 shows the waveform A, the output from the common pins in 1/3 duty mode.

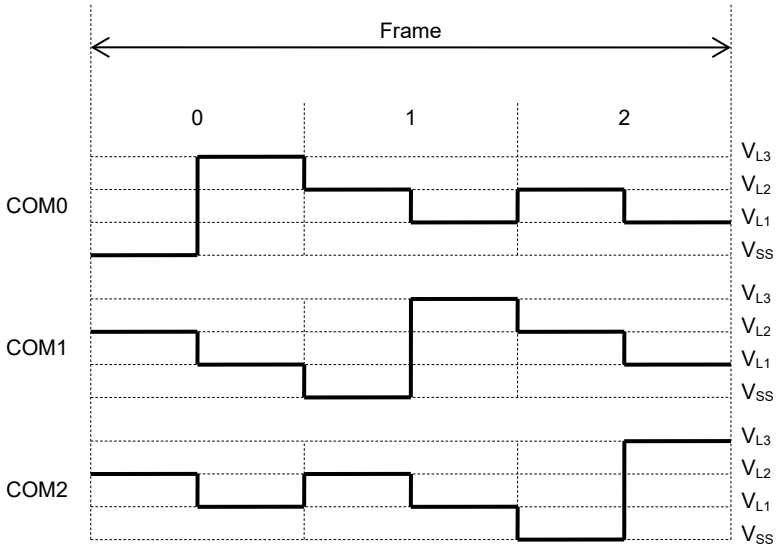


Figure 27-5 Waveform A, the output from Common Pins in 1/3 Duty

Figure 27-6 shows the waveform A, the output from the common pins in 1/4 duty mode.

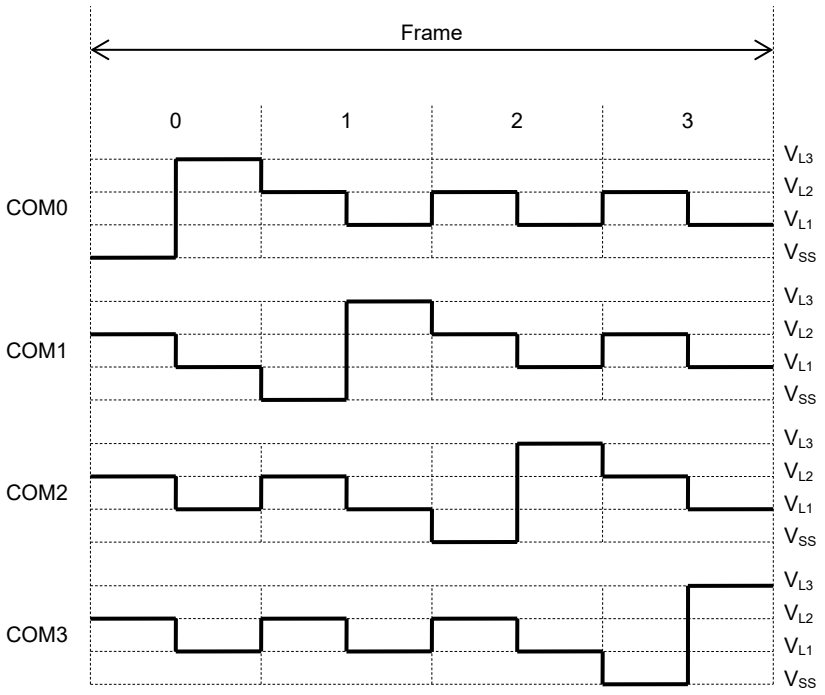


Figure 27-6 Waveform A, the output from Common Pins in 1/4 Duty

Figure 27-7 shows the waveform B, the output from the common pins in 1/3 duty mode.

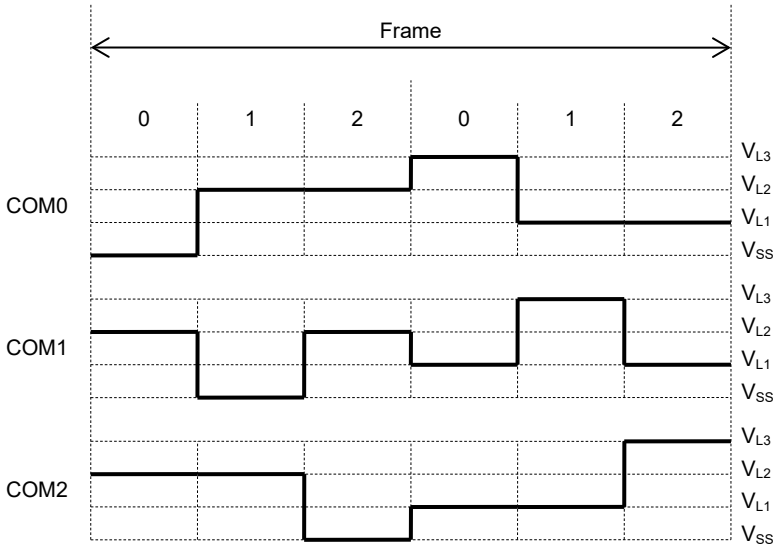


Figure 27-7 Waveform B, the output from Common Pins in 1/3 Duty

Figure 27-8 shows the waveform B, the output from the common pins in 1/4 duty mode.

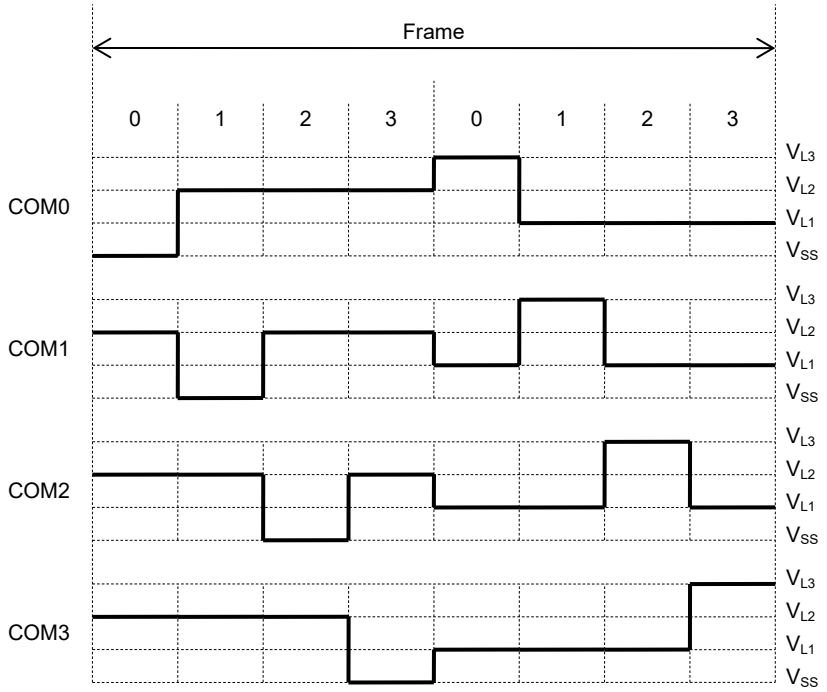


Figure 27-8 Waveform B, the output from Common Pins in 1/4 Duty

27.3.4 Segment Output Waveform

Figure 27-9 shows the waveform A, the output from the segment pins in 1/3 duty mode.

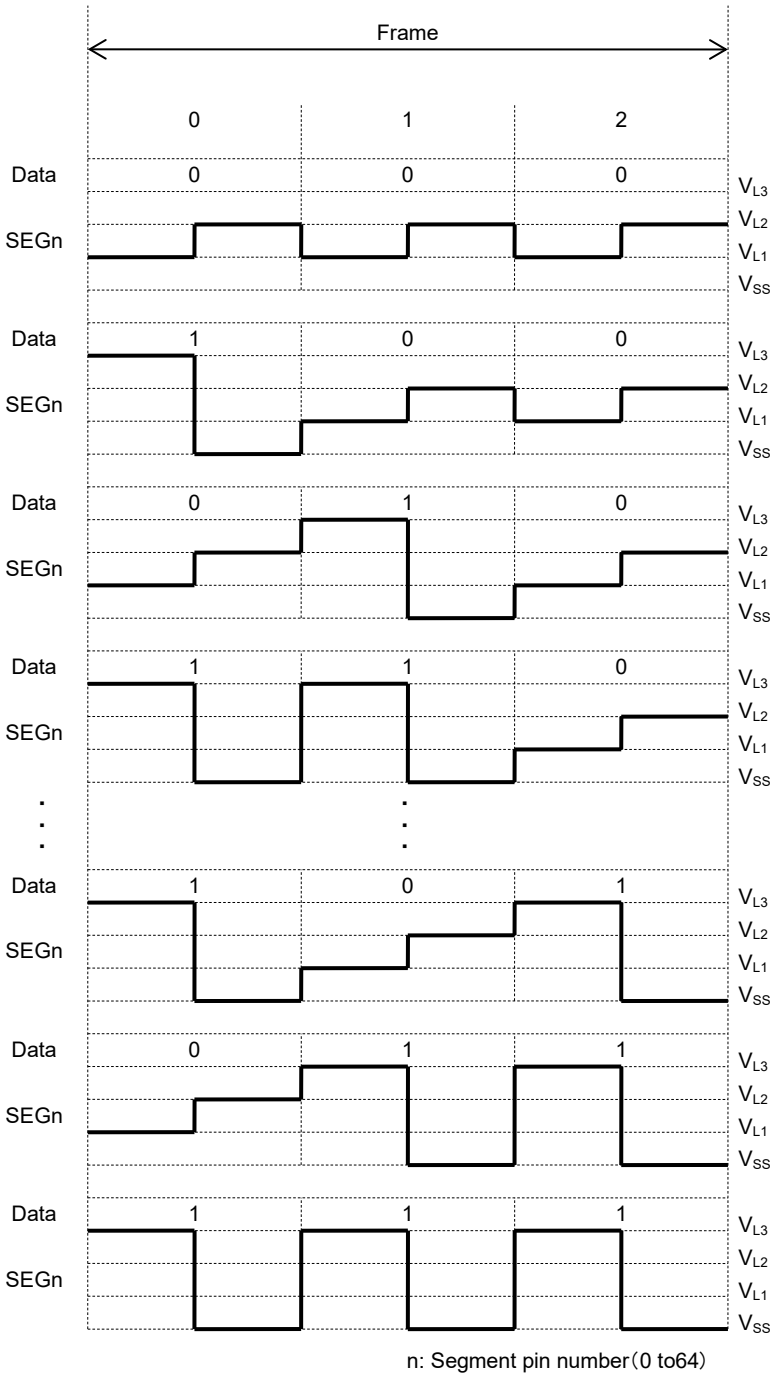


Figure 27-9 Waveform A, output from Segment Pins in 1/3 Duty

Figure 27-10 shows the waveform A, the output from the segment pins in 1/4 duty mode.

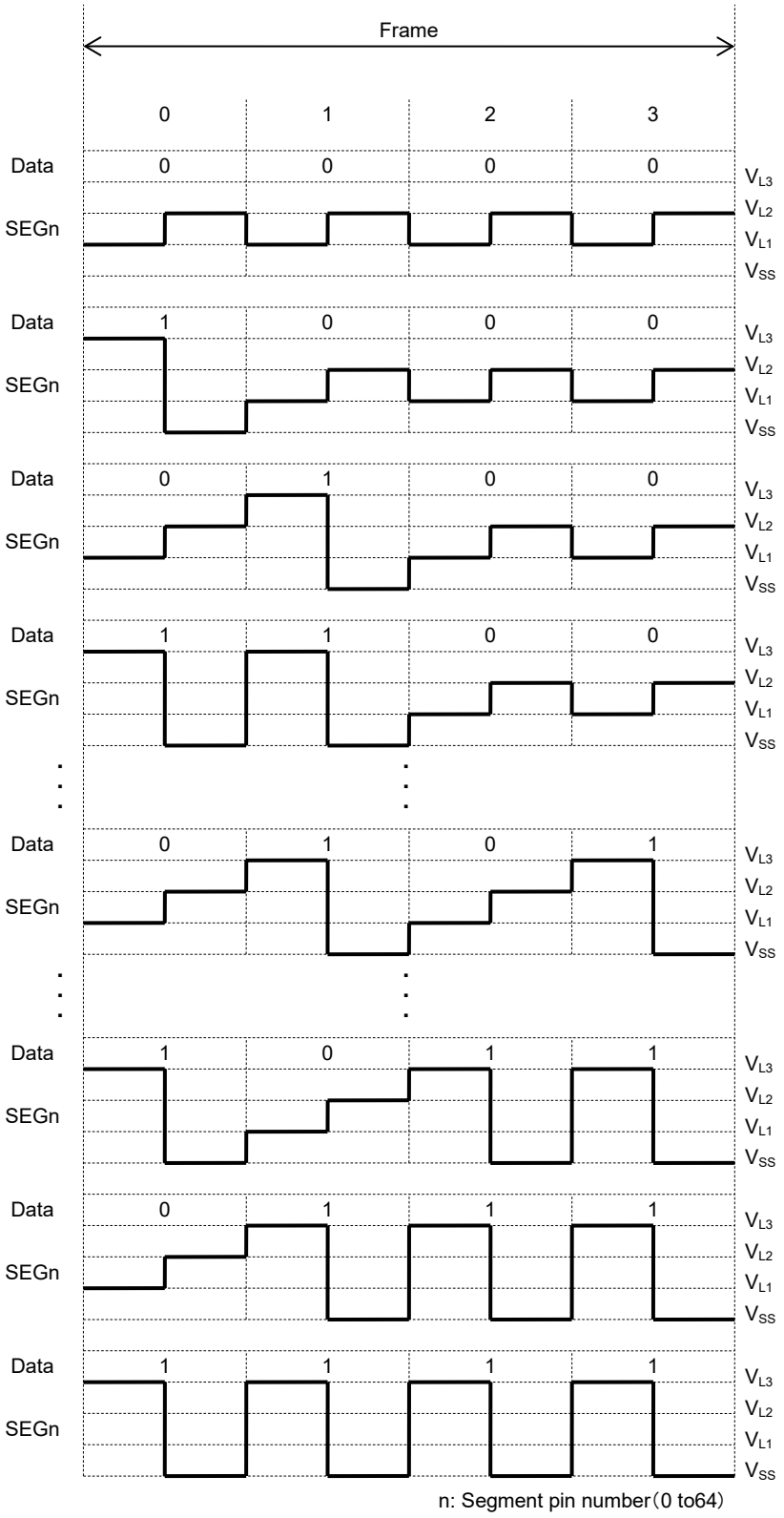


Figure 27-10 Waveform A, the output from Segment Pins in 1/4 Duty

Figure 27-11 shows the waveform B, the output from the segment pins in 1/3 duty mode.

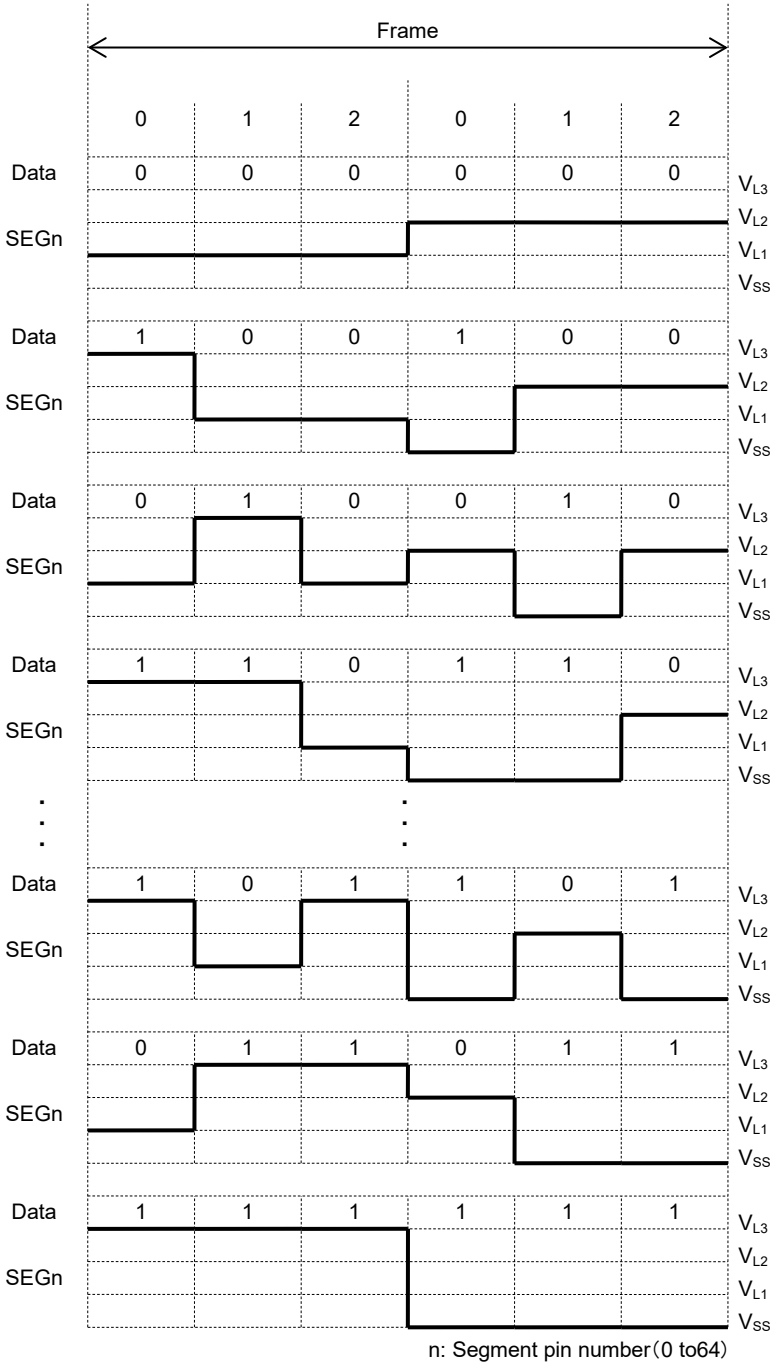


Figure 27-11 Waveform B, the output from Segment Pins in 1/3 Duty

Figure 27-12 shows the waveform B, the output from the segment pins in 1/4 duty mode.

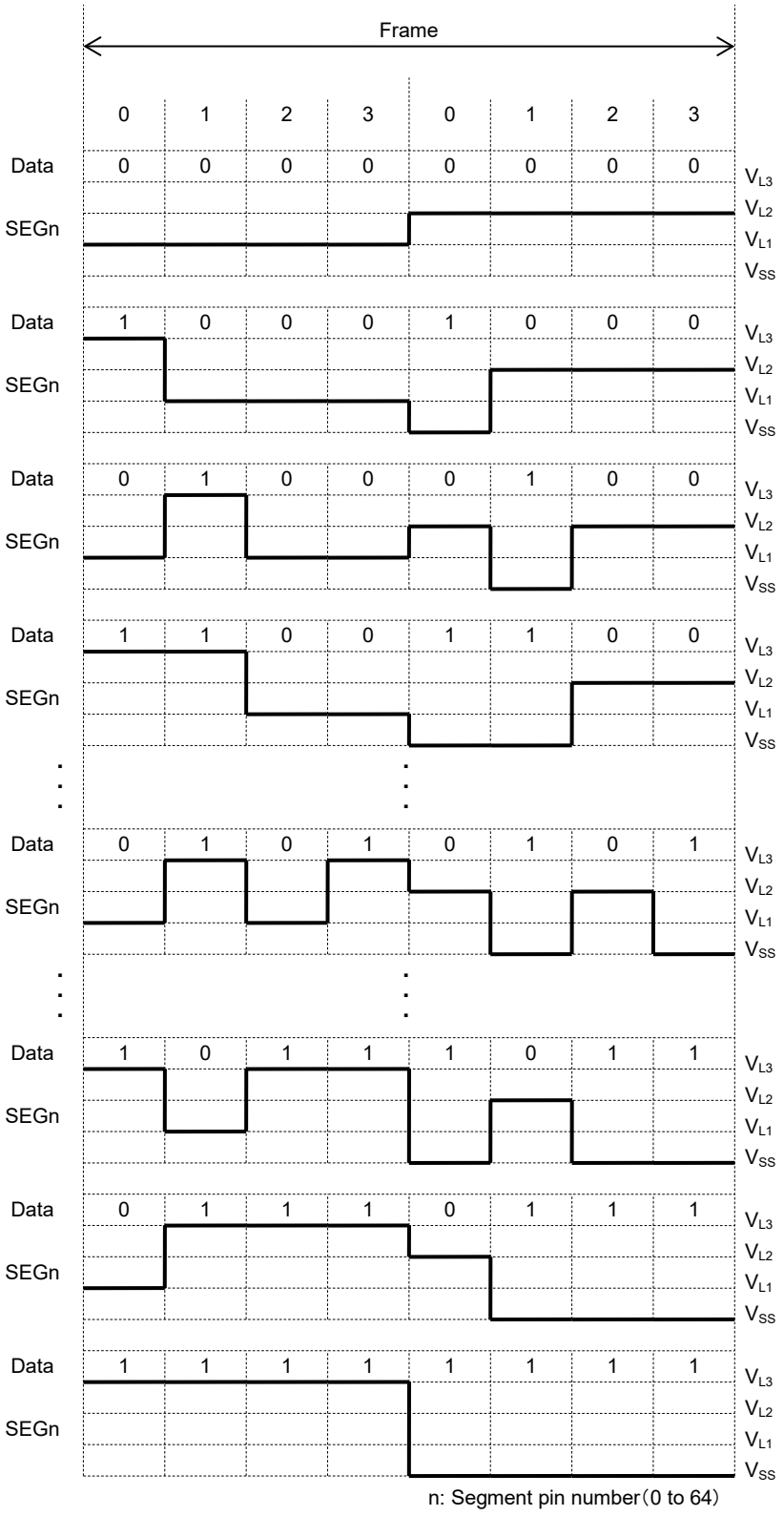


Figure 27-12 Waveform B, the output from Segment Pins in 1/4 Duty

27.3.5 Common Output Waveform for LED drive

Figure 27-13 shows the waveform A, the output from the common pins in 1/3 duty and LED drive mode.

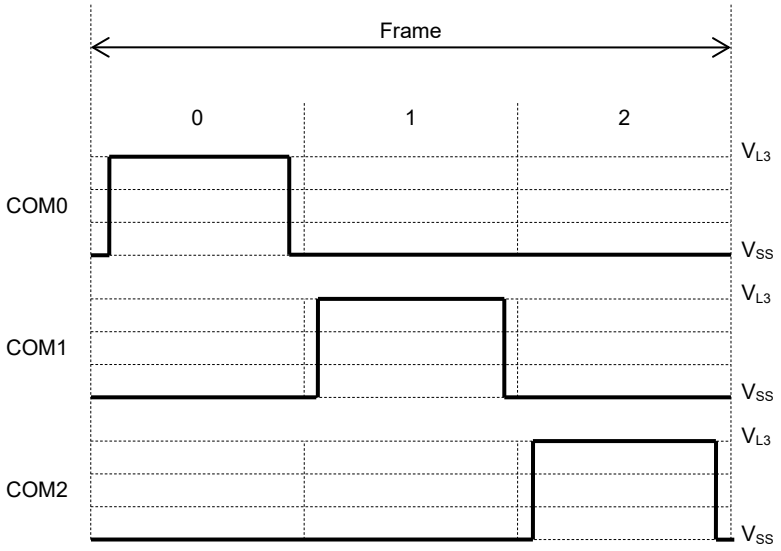


Figure 27-13 Waveform A, output from Common Pins in 1/3 Duty and LED drive mode

Figure 27-14 shows the waveform A, the output from the common pins in 1/4 duty and LED drive mode.

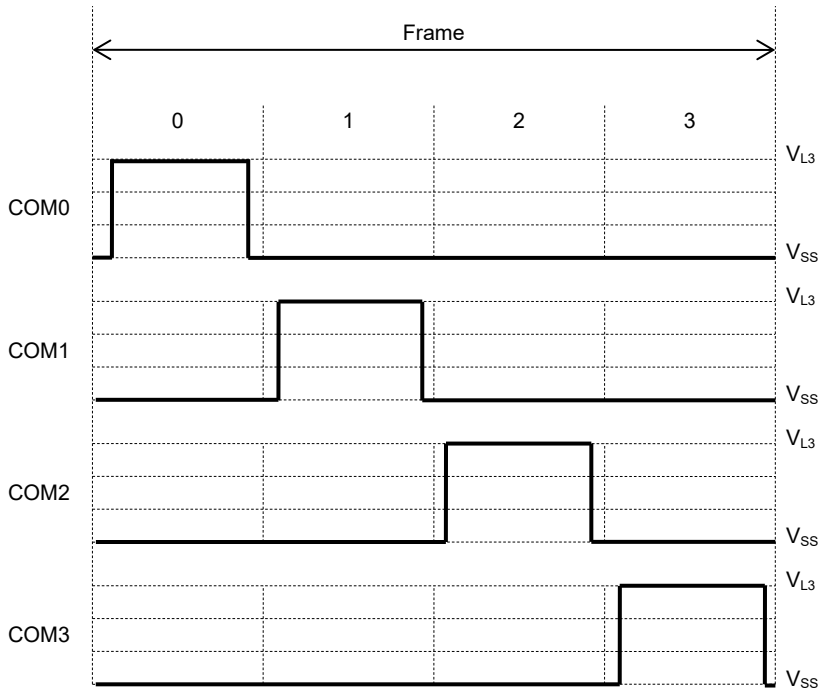


Figure 27-14 Waveform A, the output from Common Pins in 1/4 Duty and LED drive mode

27.3.6 Segment Output Waveform for LED drive

Figure 27-15 shows the waveform A, the output from the segment pins in 1/3 duty and LED drive mode.

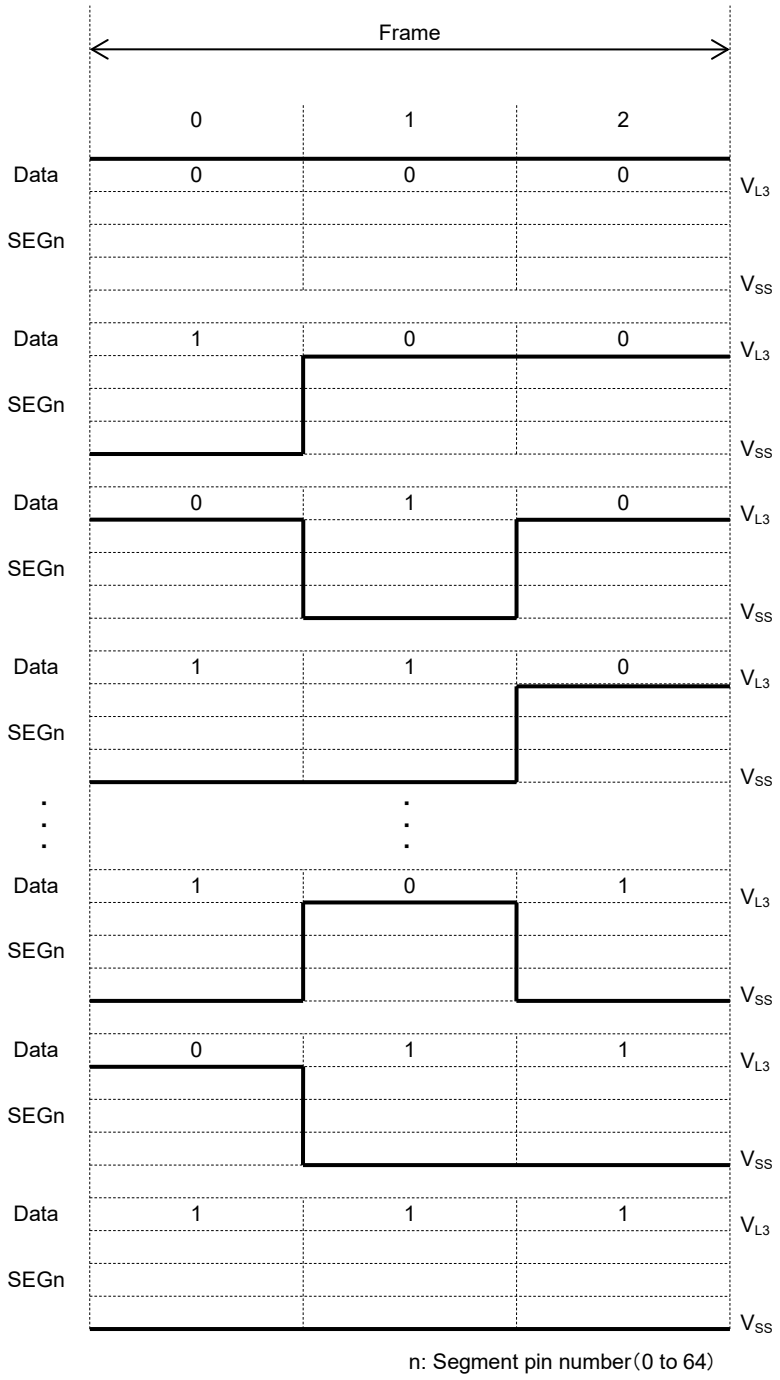


Figure 27-15 Waveform A, the output from Segment Pins in 1/3 Duty and LED drive mode

Figure 27-16 shows the waveform A, the output from the segment pins in 1/4 duty and LED drive mode.

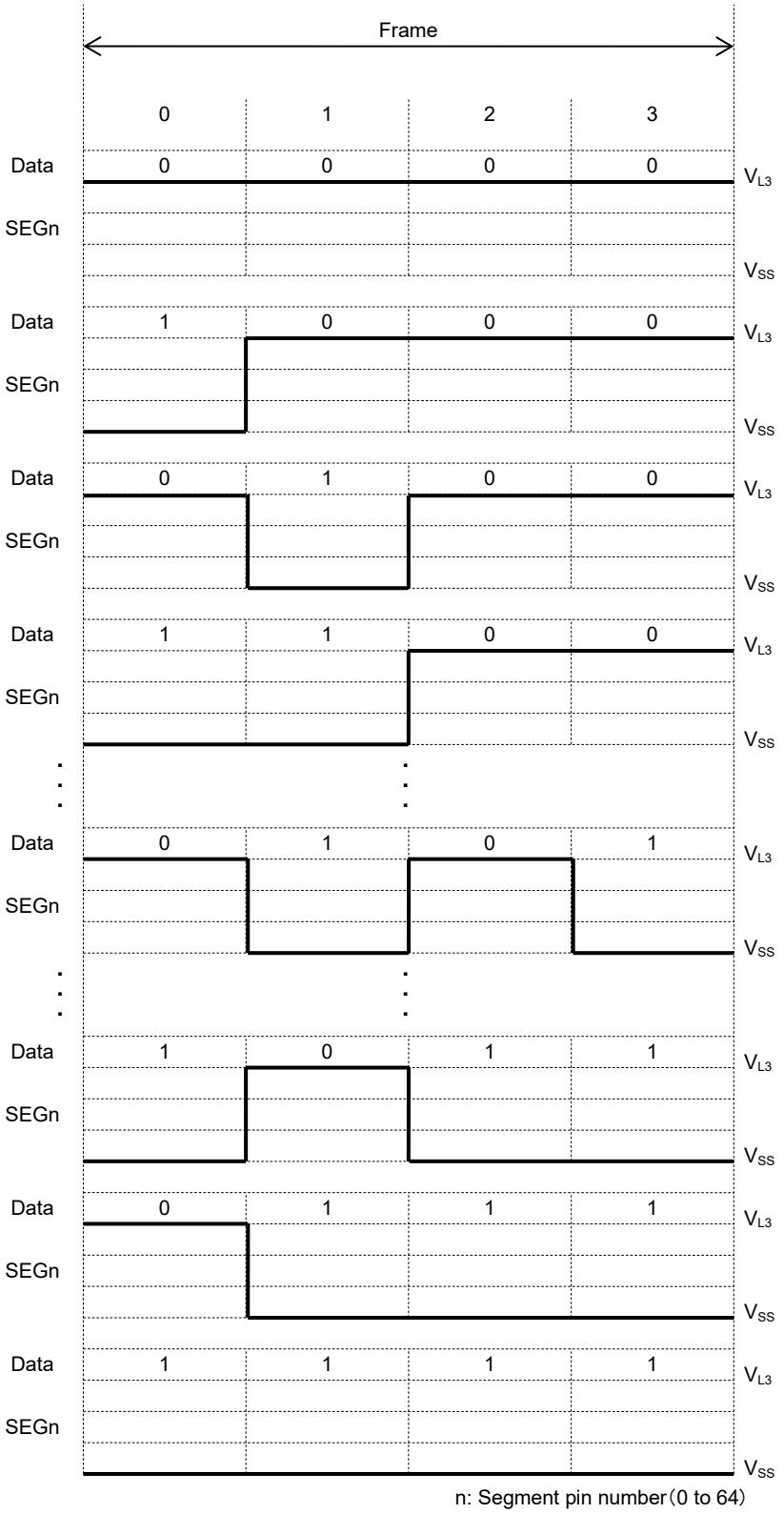


Figure 27-16 Waveform A, output from Segment Pins in 1/4 Duty and LED drive mode

27.3.7 Configuration Example to drive LEDs

In case of controlling the LED display, an external MOS transistor for LED drive is required.
Figure 27-17 shows the configuration example in LED drive mode .

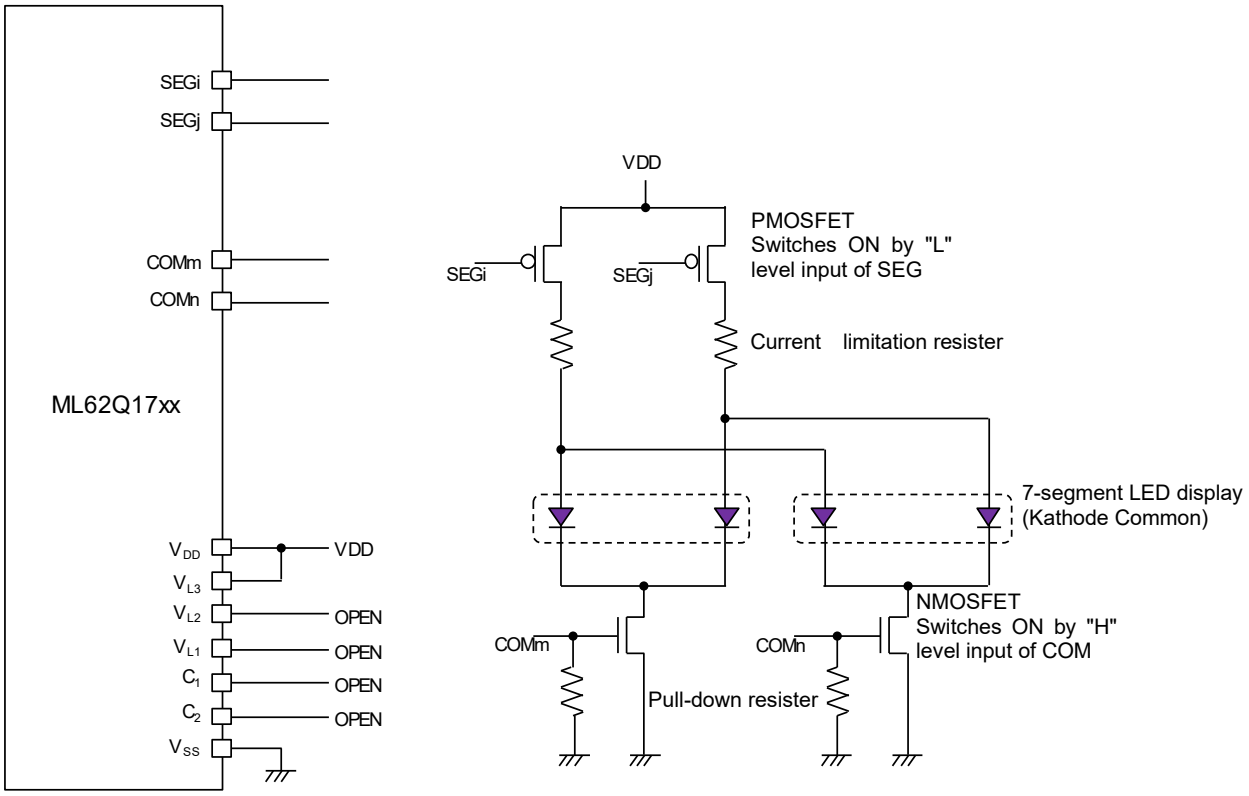


Figure 27-17 Configuration example in LED drive mode

Chapter 28 On-Chip Debug Function

28. On-Chip Debug Function

28.1 General Description

This function is used by connecting the host PC and the LSI through the on-chip debug emulator (hereafter referred to as "On-chip emulator").
On-board debugging or programming is available by using the program development environment software (debugger) installed on the host PC.

28.1.1 Features

- The following debug functions are provided using the debugger by connecting the LSI and the On-chip emulator
  - Emulation
    - Real time emulation
    - Single step emulation
  - Break
    - Hardware break point break (4points)
    - RAM data matching break
    - Sequential break
    - Stack overflow break/underflow break
    - Unused ROM area access break
    - RAM parity error break
  - Trace
    - Branch tracing
  - Real time watch
  - CPU resource display/change
    - Program memory reference/disassembly
    - RAM and SFR display/change
    - Register display/change in the CPU
  - Program download
    - Program download/read/erase to/from flash memory
    - Data write/read/erase to/from data flash
  - Peripheral circuit operation continue/stop control during break
    Target peripheral circuits: External interrupt, Low-speed time base counter, 16-bit timer, Functional timer, UART, Analog module (Successive approximation type A/D converter, VLS)

- The following program download function is provided using the flash multi-writer by connecting LSI and On-chip emulator.
  - Program download
    - Erasing/Programming the program memory space
    - Erasing/Programming the data flash memory area

28.1.2 Configuration

When using the on-chip debug function, two methods are available for power supply to LSI as described below:

- Use the 3.3 V_{OUT} power supply (+3.3 V/100 mA) of On-chip emulator
- Use the power supply of the target system (V_{DD}=1.8 V to 5.5 V)

28.1.2.1 Using 3.3 V_{OUT} Power Supply (+3.3 V/100 mA) of On-chip Emulator

Figure 28-1 shows a connection example when using the 3.3 VOUT power supply (+3.3 V/100 mA) of On-chip emulator.

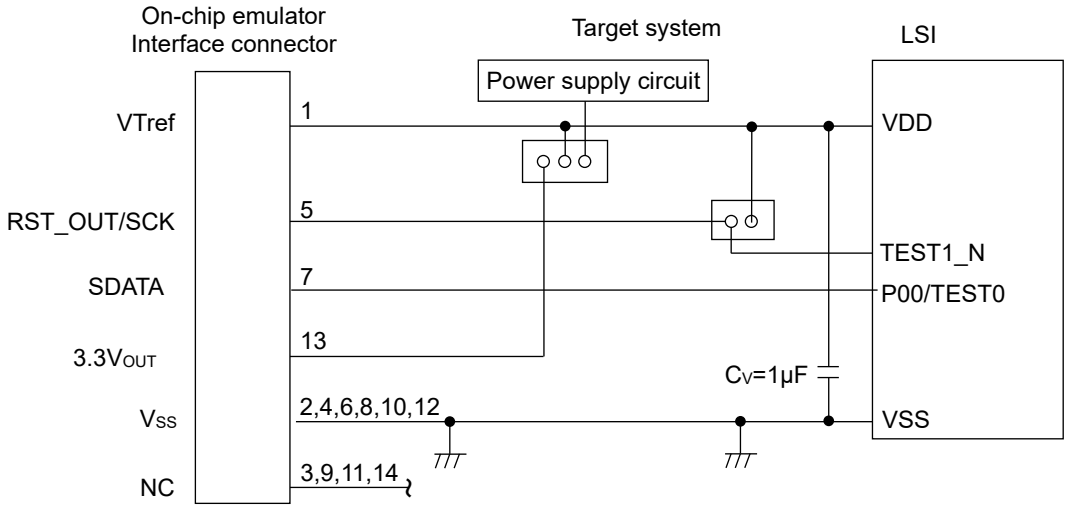


Figure 28-1 Connection Example When Using On-chip Emulator 3.3 VOUT Power Supply

28.1.2.2 Using Power Supply of Target System (V_{DD}=1.8 V to 5.5 V)

Figure 28-2 shows a connection example when using the power supply (V_{DD}=1.8 V to 5.5 V) of the target system.

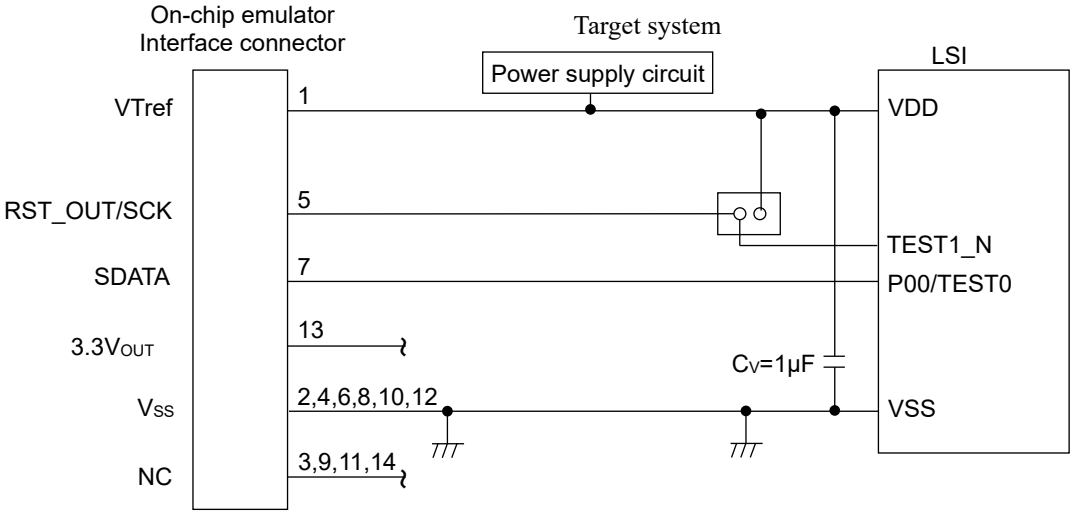


Figure 28-2 Connection Example When Using Target System Power Supply

28.1.3 List of Pins

The following pins are used for the on-chip debug function.

Signal name	I/O	Function
TEST1_N	I	On-chip debug function signal input
P00/TEST0	I/O	On-chip debug function signal input/output

28.2 How to Use On-chip Debug Function

See manual of the debugger for how to use the on-chip debug function using On-chip emulator and the debugger.
See manual of the flash multi-writer for how to download a program using On-chip emulator and flash multi-writer.

28.3 Precautions

[Note] on usage of the on-chip debug function.

- Make TEST1_N pin able to be connected to VDD with a jumper or something when not using the on-chip debug function.
- Validate the ROM code on user production board without the On-chip emulator.
- Disconnect On-chip emulator when measuring the current consumption of the target system. If On-chip emulator remains connected, the current consumption increases as the on-chip debug circuit inside the LSI works for the communication.
- When using the 3.3 VOUT power supply of On-chip emulator, do not apply power of the target system to the VDD pin of LSI. If both power supplies are connected, On-chip emulator may be damaged, or an electric shock or fire may occur.
- LSI used to debug a program is not covered by the product warranty. Do not use the LSI for mass-production.
- A reset due to unused ROM area access does not occur in the on-chip debug mode regardless of code option settings.
- A RAM parity error reset does not occur in the on-chip debug mode and the break operation occurs instead.
- If the contents of the data memory are displayed in the debugger in a state where a RAM parity error may occur (including when the RAM is not initialized), a RAM parity error may occur even if the RAM area is not displayed.
- The all interrupts and watchdog timer operation always stop while the debugger is in the break state.
- On-chip emulator might be affected by the external environments such as the host PC, USB cable, On-chip emulator interface cable and the target system. Please confirm proper environments before using on-chip emulator.
- If adding an external capacitor to the TEST1_N pin, prepare a jumper function on the board so that the capacitor gets dis-connectable when using the debugger or Flash multi-writer.

28.4 Operation of Peripheral Circuits during breaks in the on-chip debug mode

The debugger allows users to choose whether to continue or stop operating the peripheral circuits during the break state on the debugger.
Table 28-1 shows the optional items, the target peripherals and how the operation is controlled.
Each optional item is displayed with a check box on the debugger. See manual of the debugger for more details on how to use the function.

Table 28-1 Peripheral controls during the break on the debugger

Optional item	Peripheral Circuit	Description
External Interrupt	External Interrupt	If the item is checked on, the target LSI accepts the external input during the break. If the item checked off, the target LSI does not accept the external input during the break.
LTBR1	LTBR1 of Low-speed Time Base	If the item is checked on, operation of the peripheral operation continues during the break. If the item checked off, operation of the peripheral stops during the break.
LTBR0	LTBR0 of Low-speed Time Base	If the item is checked on, operation of the peripheral operation continues during the break. If the item checked off, operation of the peripheral stops during the break.
General Timer	16-bit Timer	If the item is checked on, operation of the peripheral operation continues during the break. If the item checked off, operation of the peripheral stops during the break.
Functional Timer	Functional Timer	If the item is checked on, operation of the peripheral operation continues during the break. If the item checked off, operation of the peripheral stops during the break.
UART	UART	If the item is checked on, operation of the peripheral operation continues during the break. If the item checked off, operation of the peripheral stops during the break.
Analog Module （ADC/VLS）	SA-ADC and VLS	If the item is checked on, operation of the peripheral operation continues during the break. If the item checked off, operation of the peripheral stops during the break.

28.5 Reset in the On-Chip Debug Tool

By executing reset from the debug tool, RSTAT register POR bit is set to "1". However, low-speed crystal oscillation and VLS functions are not reset. If it is necessary to start them from initial state, set these pertinent SFRs to initial value. Then execute reset from debug tools.

Chapter 29 Safety Function

29. Safety Function

29.1 General Description

ML62Q2700 group has the safety functions to make a safe stop in case a failure is detected by executing the self-diagnosis software, available to support IEC60730/60335 Class B.

29.1.1 Features

- Safety Functions on the LSI

Function Name	Description	Control by SFR
RAM guard	Protect from the miss-writing to the specified RAM area	Available
SFR guard	Protect from the miss-writing to the specified SFR	Available
Successive approximation type A/D converter test	Successive approximation type AD converter self test function	Available
RAM parity error detection	Check for the occurrence of a parity error in RAM and to reset the LSI when a parity error occurs (SFR can allow/prevent reset, with reset status flag, with parity error flag)	Available
ROM unused area access reset	Monitors the program counter (PC) of the CPU and generate a reset when a program in an invalid area is executed (enable/disable reset by the code option, with reset status flag)	-
Clock mutual monitoring	Monitor whether the oscillation of the high-speed and low-speed clocks are normal	Available
CRC calculation	Detect data error in the flash memory or data error in communications	Available
UART self-test function	UART self-test	Available
SSIO self-test function	SSIO self-test	Available
I^2C self-test function	I^2C self-test function	Available
WDT counter read	WDT counter read	Available
Port output level self-test function	General port self-test	Available
Clock backup function and the self-test	Switch automatically to the low-speed RC oscillation in case the low-speed crystal oscillation stopped, and the self test	Available
MCU status interrupt	Control interrupts generated by RAM parity error, automatic CRC calculation completion, and data flash erase/program completion.	Available

29.2 Description of Registers

29.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial Value
		Byte	Word			
0xF0B0	RAM Guard Setting Register 0	RAMGD	-	R/W	8	0x00
0xF0B1 to 0xF0B3	Reserved register	-	-	-	-	-
0xF0B4	SFR Guard Setting Register 0	SFRGD0L	SFRGD0	R/W	8/16	0x00
0xF0B5		SFRGD0H		R/W	8	0x00
0xF0B6	SFR Guard Setting Register 1	SFRGD1L	SFRGD1	R/W	8/16	0x00
0xF0B7		SFRGD1H		R/W	8	0x00
0xF0B8 to 0xFBB	Reserved register	-	-	-	-	-
0xF0BC	RAM Parity Setting Register	RASFMOD	-	R/W	8	0x00
0xF0BD	Reserved register	-	-	-	-	-
0xF0BE	Communication Test Setting Register 0	COMFT0L	COMFT0	R/W	8/16	0x00
0xF0BF		COMFT0H		R/W	8	0x00
0xF050	MCU Status Interrupt Enable Register	MCINTEL	-	R/W	8	0x00
0xF051	Reserved register	-	-	-	-	-
0xF052	MCU Status Interrupt Register	MCISTATL	-	R	8	0x00
0xF053	Reserved register	-	-	-	-	-
0xF054	MCU Status Interrupt Clear Register (L/H)	MCINTCLL	-	W	8	0x00
0xF055		MCINTCLH		W	8	0x00

29.2.2 RAM Guard Setting Register (RAMGD)

RAMGD is a SFR to disable writing the RAM.
Data in the specified RAM area is protectable.

Address: 0xF0B0 (RAMGD)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								RAMGD							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	RGD2	RGD1	RGD0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7 to 3	-	Reserved bits
2 to 0	RGD2 to RGD0	Select a protect area for writing on the RAM. 000: All RAM area writable and readable (Initial value) 001: 0x0:0EFC0 to 0x0:0EFFF (64 byte) is unwritable and readable 010: 0x0:0EF80 to 0x0:0EFFF (128 byte) is unwritable and readable 011: 0x0:0EF00 to 0x0:0EFFF (256 byte) is unwritable and readable 100: 0x0:0EE00 to 0x0:0EFFF (512 byte) is unwritable and readable 101: Do not use (0x0:0EE00 to 0x0:0EFFF (512 byte) is unwritable and readable) 110: Do not use (0x0:0EE00 to 0x0:0EFFF (512 byte) is unwritable and readable) 111: Do not use (0x0:0EE00 to 0x0:0EFFF (512 byte) is unwritable and readable)

29.2.3 SFR Guard Setting Register 0 (SFRGD0)

SFRGD0 is a SFR to disables certain SFRs writing from CPU.
Data in the specified SFR area is protectable by setting.

Address: 0xF0B4 (SFRGD0L/SFRGD0), 0xF0B5(SFRGD0H)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SFRGD0															
Byte	SFRGD0H								SFRGD0L							
Bit	-	-	-	-	-	-	-	-	-	-	SGD05	SGD04	SGD03	SGD02	SGD01	SGD00
R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
It is configured writable/unwritable target SFRs
0: Target SFRs are writable and readable (Initial value)
1: Target SFRs are unwritable and readable

Bit No.	Bit symbol name	Description (target SFRs)
15 to 6	-	Reserved bits
5	SGD05	WDTMOD register; see Chapter “10 Watchdog timer”
4	SGD04	BCKCONn and BRECONn registers (n=0 to 3); see Chapter “4 Power management”
3	SGD03	RASFMOD register; see this chapter.
2	SGD02	SFRs described in chapter 22. VLS.
1	SGD01	SFRs described in chapter 6. Clock Generation Circuit.
0	SGD00	SFRs described in chapter 5 Interrupt

29.2.4 SFR Guard Setting Register 1 (SFRGD1)

SFRGD1 is a SFR to disables certain SFRs writing from CPU.
Data in the specified SFR area is protectable by setting.

Address: 0xF0B6(SFRGD1L/SFRGD1), 0xF0B7(SFRGD1H)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	SFRGD1															
Byte	SFRGD1H								SFRGD1L							
Bit	SGD1F	-	-	-	-	-	-	-	SGD17	SGD16	SGD15	-	SGD13	SGD12	SGD11	SGD10
R/W	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
It is configured writable/unwritable target SFRs in chapter 17. GPIO.
0: Target SFRs are writable and readable (Initial value)
1: Target SFRs are unwritable and readable

Bit No.	Bit symbol name	Description (target SFRs)
15	SGD1F	SFRs related to the port XT
14 to 12	-	Reserved bits
11	SGD1B	SFRs related to the port B
10	SGD1A	SFRs related to the port A
9	SGD19	SFRs related to the port 9
8	SGD18	SFRs related to the port 8
7	SGD17	SFRs related to the port 7
6	SGD16	SFRs related to the port 6
5	SGD15	SFRs related to the port 5
4	SGD14	SFRs related to the port 4
3	SGD13	SFRs related to the port 3
2	SGD12	SFRs related to the port 2
1	SGD11	SFRs related to the port 1
0	SGD10	SFRs related to the port 0

29.2.5 RAM Parity Setting Register (RASFMOD)

RASFMOD is a SFR to control the RAM parity error reset function.
The RAM parity error is detectable and the RAM parity error reset is generatable.
The reset flag by a RAM parity error can be checked by the reset status register (SRSTAT).
See Chapter 3 "Reset Function" for details about the reset flag.

Address: 0xF0BC(RASFMOD)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								RASFMOD							
Bit	-	-	-	-	-	-	-	-	PERF	-	-	-	-	-	-	PEREN
R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit No.	Bit symbol name	Description
7	PERF	Indicate the RAM parity error occurs. Writing "1" clear this bit, writing “0” does not clear this bit. When PEREN is written to "1" to enable the parity error reset function, the reset status register (SRSTAT) can be used to check. 0: RAM parity error not occur (Initial value) 1: RAM parity error occurs
6 to 1	-	Reserved bits
0	PEREN	Enable/disable the RAM parity error reset function. 0: Disabled (Initial value) 1: Enabled

29.2.6 Communication Test Setting Register (COMFT0)

COMFT0 is a SFR to control the communication test function, which enables the loop back test with transmit data in the serial communication units. See Section 29.3.1 "Communication Function Self Test" for more details.
As the I^2C bus unit and the I^2C master are equipped with the function to read the transmit data, the function can be used for testing. For details, see Chapter 13 "I^2C Bus".

Address: 0xF0BE(COMFT0/COMFT0L), 0xF0BF(COMFT0H)
Access: R/W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ワード	COMFT0															
バイト	COMFT0H								COMFT0L							
ビット	CMFT15	CMFT14	CMFT13	CMFT12	-	CMFT10	CMFT09	CMFT08	-	-	CMFT05	CMFT04	CMFT03	CMFT02	CMFT01	CMFT00
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
初期値	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
It is configured enable/disable the self-test for target communication function.
0: Target function is disabled. (Initial value)
1: Target function is enabled.

Bit No.	Bit symbol name	Description (target)
15	CMFT15	ESSIO2
14	CMFT14	ESSIO1
13	CMFT13	ESSIO0
12	CMFT12	SSIOF0
11	-	Reserved bits
10	CMFT10	SSIO2
9	CMFT09	SSIO1
8	CMFT08	SSIO0
7 to 6	-	Reserved bits
5	CMFT05	EUART2
4	CMFT04	EUART1
3	CMFT03	EUART0
2	CMFT02	UART2
1	CMFT01	UART1
0	CMFT00	UART0

29.2.7 MCU Status Interrupt Enable Register (MCINTEL)

MCINTEL is a SFR control enabling/disabling three types of interrupt status on the microcontroller.

Address: 0xF050 (MCINTEL)
Access: R/W
Access size: 8 bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								MCINTEL							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	MCI2E	MCI1E	MCI0E
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
It is configured enable/disable target interrupt.
0: Target interrupt is disabled. (Initial value)
1: Target interrupt is enabled.

Bit No.	Bit symbol name	Description (target interrupt)
7 to 3	-	Reserved bits
2	MCI2E	The interrupt at the completion of data flash erasing/programming.
1	MCI1E	The interrupt at the completion of automatic CRC calculation.
0	MCI0E	The interrupt at the occurrence of RAM parity error.

29.2.8 MCU Status Interrupt Register (MCISTATL)

MCISTATL is a read-only SFR to indicate status of the three types of interrupts.
MCI2S to MCI0S bit are initialized, in addition to reset function, by writing "1" to the same number of bit in the MCINTCL register.

Address: 0xF052 (MCISTATL)
Access: R
Access size: 8bit
Initial value: 0x00

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	-								MCISTATL							
Bit	-	-	-	-	-	-	-	-	-	-	-	-	-	MCI2S	MCI1S	MCI0S
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits:
It is to indicate status of target interrupt.
0: Target interrupt has not been generated. (Initial value)
1: Target interrupt has been generated.

Bit No.	Bit symbol name	Description (target interrupt)
7 to 3	-	Reserved bits
2	MCI2S	The interrupt at the completion of data flash erasing/programming.
1	MCI1S	The interrupt at the completion of automatic CRC calculation.
0	MCI0S	The interrupt at the occurrence of RAM parity error.

[Note]
- **If the MCISTATL register is not zero, a request to interrupt controller is not given when a new interrupt occurs. Clear the MCISTATL register with the MCINTCL register before that time.**

29.2.9 MCU Status Interrupt Clear Register L/H (MCINTCLL, MCINTCLH)

MCINTCL is a write-only SFR to clear the MCU status interrupts.
If MCI2C to MCI0C bit are set to "1", the interrupt request by the same number of bit in the MCISTATL register gets cleared.
This register always returns "0x0000" for reading.

Address: 0xF054(MCINTCLL), 0xF055(MCINTCLH)
Access: W
Access size: 8/16 bit
Initial value: 0x0000

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	-															
Byte	MCINTCLH								MCINTCLL							
Bit	MCIR	-	-	-	-	-	-	-	-	-	-	-	-	MCI2C	MCI1C	MCI0C
R/W	W	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W
Initial value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Common description of each bits; bit 2 to 0 :
It is to indicate status of target interrupt.
Writing “0” : Invalid
Writing “1” : Target interrupt status gets cleared.

Bit No.	Bit symbol name	Description
15	MCIR	Request bit for the MCU status interrupt. Write "1" to this bit before returning from the interrupt routine. Writing "0":Invalid Writing "1":If an unhandled interrupt exists, it generates the interrupt request again.
14 to 3	-	Reserved bits
2	MCI2C	The interrupt at the completion of data flash erasing/programming.
1	MCI1C	The interrupt at the completion of automatic CRC calculation.
0	MCI0C	The interrupt at the occurrence of RAM parity error.

29.3 Description of Operation

29.3.1 Communication Function Self-Test

This self test is enabled by COMFT0 register setting.
The communication function can be tested through the self test by internally connecting transmit and receive data of UART and SSIO (synchronous serial port) of the serial communication unit.
Before testing the communication, write "1" to the corresponding bit of COMFT0 register.
Transmit side data output can be enabled/disabled by setting the mode (secondary to octonary function) of the general-purpose port.
For receive side data, it is not required to set the mode (2^{nd} to 8^{th} function) of the general-purpose port.
Figure 29-1 shows a concept diagram of the communication test. Figure 29-2 shows a flow chart of the communication test.

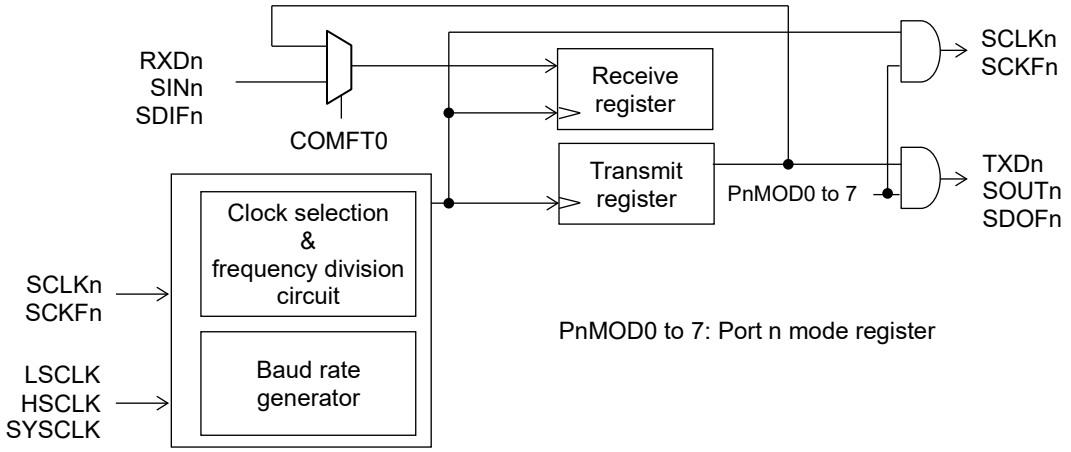


Figure 29-1 Communication Test Concept Diagram

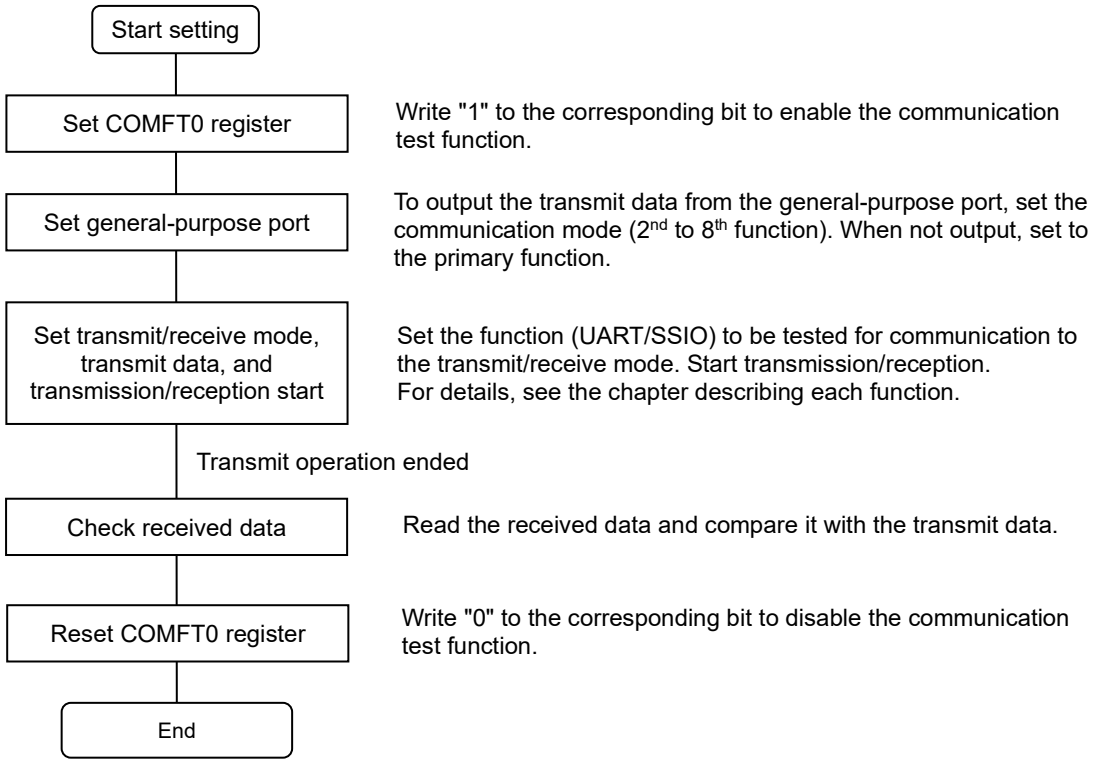


Figure 29-2 Communication Test Flow Chart

29.3.2 Unused ROM Area Access Reset Function

This function constantly monitors the program counter (PC) of the CPU. It generates the LSI reset when it detects that the program counter (PC) executes a program located outside of the area. This function can be enabled/disabled by the code option. The reset flag due to unused ROM area access can be confirmed with the SRSTAT register.
See Chapter 3 "Reset Function" for details of the reset flag.

<ROM unused area>

Program memory size : CSR:PC
256KB : 0x3:0FFC0 to 0x7:0FFFF
192KB : 0x2:0FFC0 to 0x7:0FFFF
160KB : 0x2:07FC0 to 0x7:0FFFF
96KB : 0x1:07FC0 to 0x7:0FFFF
64KB : 0x0:0FFC0 to 0x7:0FFFF

[Note]
- **CSR[3] is unused on the ML62Q2700 group. The data of CSR "0x8 to 0xF" are handled as "0x0 to 0x7".**

29.3.3 Clock Mutual Monitoring Function

This function monitors whether the low-speed clock (low-speed RC oscillator circuit) and the high-speed clock (PLL oscillator circuit) oscillate normally.
The 16-bit timer and functional timer are available to implement the function.

In addition, it is possible to monitor LSCLK0 by counting LSCLK0 using RC1K as a trigger.
This function enables mutual monitoring of the clocks of the two oscillator circuits.
See the application note for more details.

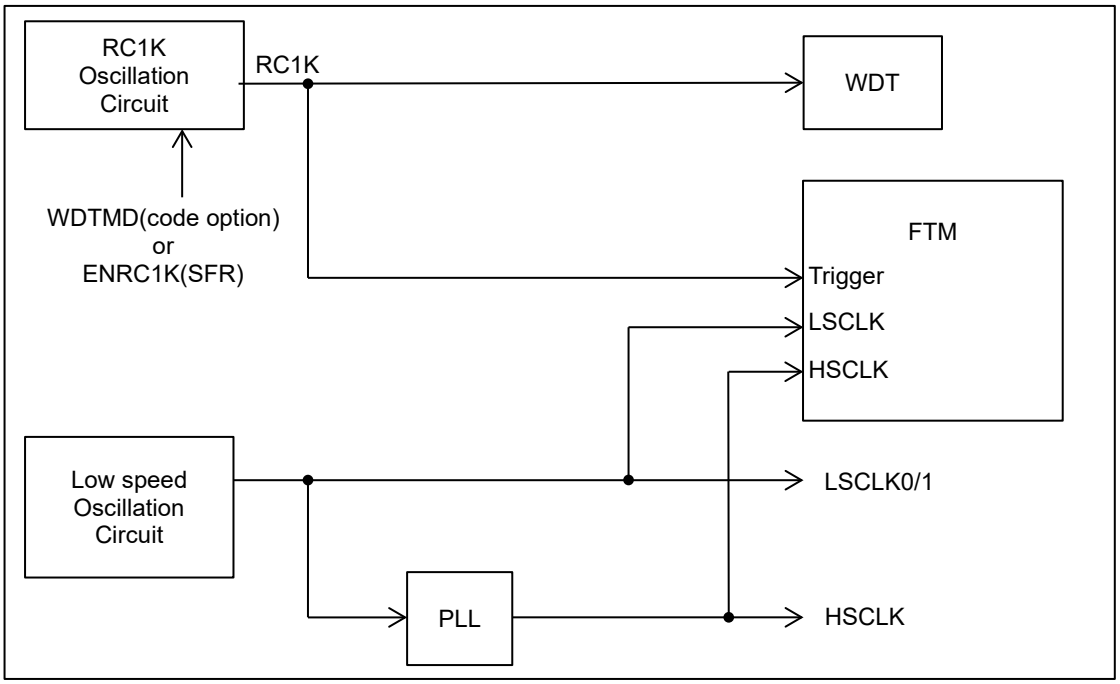
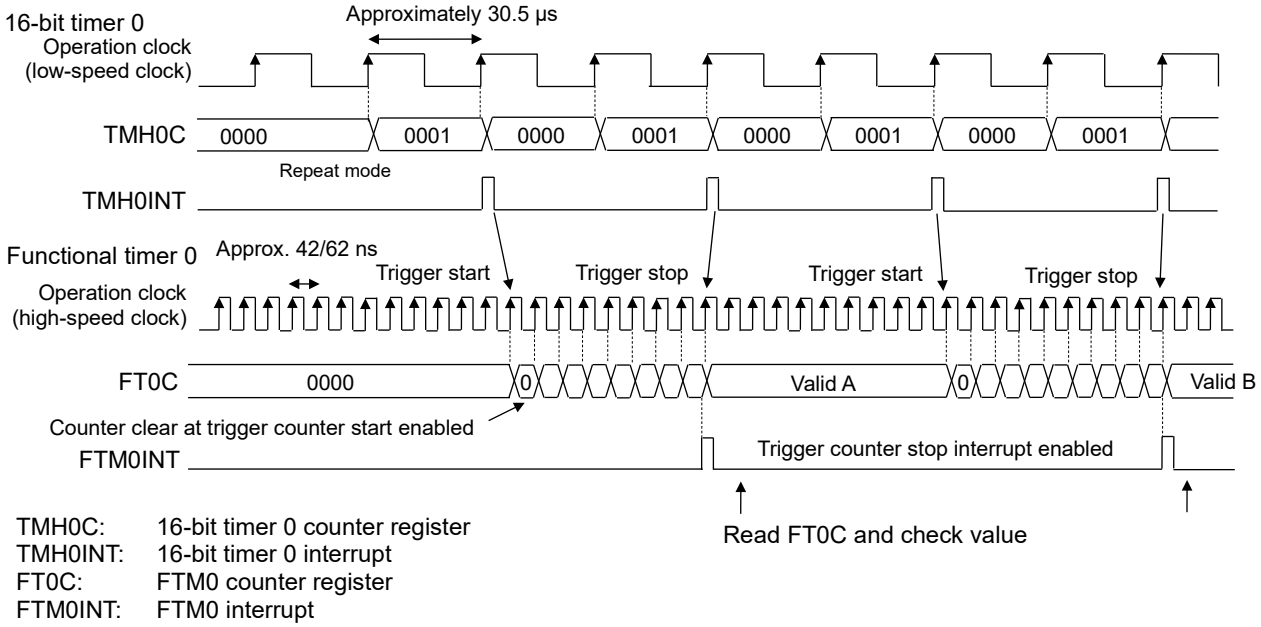


Figure 29-3 Clock Mutual Monitoring Function Block Diagram

Figure 29-4 shows an example of the monitoring operation, using 16-bit timer 0 and Functional timer 0, for the high-speed clock (PLL oscillation circuit) oscillation.



TMH0C: 16-bit timer 0 counter register
TMH0INT: 16-bit timer 0 interrupt
FT0C: FTM0 counter register
FTM0INT: FTM0 interrupt

Figure 29-4 High-Speed Clock (PLL Oscillation Circuit) Oscillation Monitoring Example

Figure 29-5 describes the setting for the monitoring example shown in Figure 29-4.

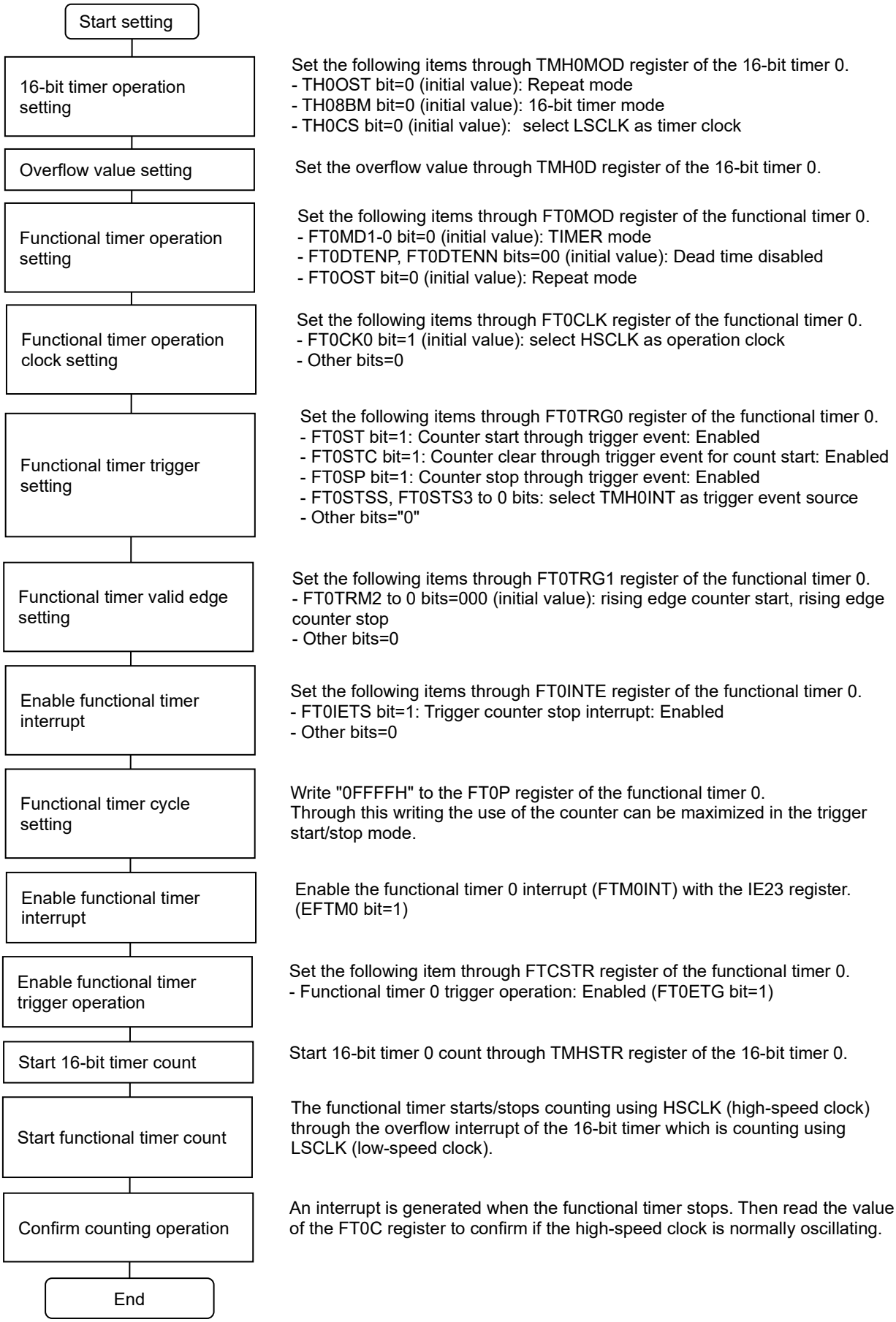


Figure 29-5 Setting of High-Speed Clock (PLL Oscillation Circuit) Oscillation Monitoring Example

[Note]

- **For "Overflow value setting" in Figure 29-5, set the value so that the overflow period of the 16-bit timer n is to be shorter than that of the functional timer n. If the functional timer n overflows, it disables the accurate check.**

29.3.4 CRC Calculation

The CRC (Cyclic Redundancy Check) calculation detects data errors including arbitrary data errors. Two CRC modes are available as described below. Select either one depending on the intended use.
See Chapter 19 "CRC Calculator" for details of its operation.

Table 29-1 CRC Calculation Mode

CRC calculation	Description
Automatic CRC calculation mode	Automatically execute calculation of the program code area in units of 32 bits in the HALT/HALT-H mode.
Manual CRC calculation mode	Execute calculation of arbitrary data written from the CPU in units of 8 bits.

29.3.5 WDT Counter Read

The count value can be read from the watchdog timer counter register (WDTMC). Periodic checks of the count value allow confirmation that the watchdog timer is normally counting.
See Chapter 10 "Watchdog Timer" for its operation.

29.3.6 Port Output Level Test

When the general-purpose port is used as an output pin, the output data can be read by setting the input/output mode.
See Chapter 17 "General-purpose Port" for its operation.

29.3.7 Successive Approximation Type A/D Converter Test

The self test can be executed by A/D-converting the full scale, zero scale and internal reference voltage.
See “23.3.2 Test function of Successive Approximation Type A/D Converter” for details.

29.3.8 Clock Backup Function and Its Test

The built-in test function automatically switches the low-speed crystal oscillation to the low-speed RC oscillation, when the oscillation is stopped.
See Chapter 6 "Clock Generation Circuit" for details.

Chapter 30 Code Option

30. Code Option

30.1 General Description

The code option is used to select CPU operating mode, PLL reference frequency, watchdog timer operation, and so on. depending on values written in the code option area of the program memory area.

The hardware automatically refers to data in the code option area when the microcontroller starts up due to one of system resets described below to set each function.
The code option area can be erased or programmed through the on-chip debug function, self-rewrite function of flash memory, or ISP function.

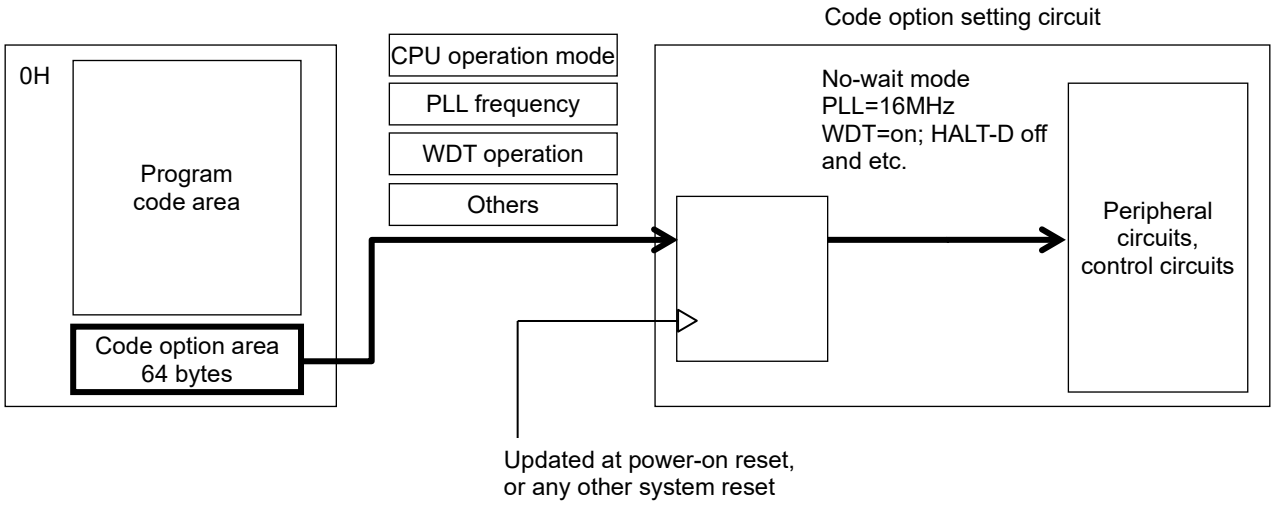


Figure 30-1 Code Option Overview

30.1.1 Function List

- The configured code options are referenceable from SFRs space
- Enabling or disabling the unused ROM area access reset
- Enabling or disabling the remapping function
- The software remap or hardware remap is selectable for the remap function
- Enabling or disabling the watchdog timer operation at HALT/HALT-H, HALT-D
- Enabling or disabling the watchdog timer operation
- Select PLL reference frequency (1MHz / 16MHz / 24MHz)
- CPU operation mode (wait mode or no-wait mode)
- Enabling or disabling a clock back-up function of LSCLK1

30.2 Description of Code Option

30.2.1 Reading from SFRs

The address of code option area is dependent of the size of the program memory space (flash memory).
The address of SFRs for reading is fixed.

SFR address	Name	Symbol name		R/W	Size
		Byte	Word		
0xF920	Code Option 0	CODEOP0L	CODEOP0	R	8/16
0xF921		CODEOP0H		R	8
0xF922	Code Option 1	CODEOP1L	CODEOP1	R	8/16
0xF923		CODEOP1H		R	8
0xF924	Code Option 2	CODEOP2L	CODEOP2	R	8/16
0xF925		CODEOP2H		R	8

[Note]
- **The value of a code option that can be referenced from the SFR area is readable only when the INITE flag in the reset status register (RSTAT) is "0".**

30.2.2 Code Option 0 (CODEOP0)

Address: (See Table 30-1)
SFR address for reading: 0xF920 (CODEOP0L/CODEOP0), 0xF921(CODEOP0H)
Access to SFR : R
Access size to SFR: 8/16 bit
Initial value: 0xFFFF (Erased or factory default setting for products with blank flash memory)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CODEOP0															
Byte	CODEOP0H								CODEOP0L							
Bit	-	-	-	PCERMD	-	-	-	REMAPMD	LS1BU	-	-	-	WDTPWMD1	WDTPWMD0	-	WDTMD
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15 to 13	-	Reserved bits. Set "1" to all bits.
12	PCERMD	Select to enable/disable the unused ROM area access reset. See Section 29.3.2 "Unused ROM Area Access Reset Function" for the unused ROM area access reset. 0: Disabled 1: Enabled (Initial value)
11 to 9	-	Reserved bits. Set "1" to all bits.
8	REMAPMD	Select to enable/disable the remapping function (software remap or hardware remap) operation. See Section 2.8 "Remapping Function" for details of the remapping function. 0: Enabled 1: Disabled (Initial value)
7	LS1BU	Enable /disable a back-up function of LSCLK1. 0: Disabled 1: Enabled (Initial value)
6 to 4	-	Reserved bits. Set "1" to all bits.
3	WDTPWMD1	Select to enable/disable the watchdog timer (WDT) operation in HALT-D mode, if WDTMD = “1”. 0: Disabled 1: Enabled (Initial value)
2	WDTPWMD0	Select to enable/disable the watchdog timer (WDT) operation in HALT/HALT-H mode, if WDTMD = “1”. 0: Disabled 1: Enabled (Initial value)
1	-	Reserved bit. Set "1" to this bit.
0	WDTMD	Select to enable/disable the watchdog timer (WDT) operation. 0: Disabled 1: Enabled (Initial value)

30.2.3 Code Option 1 (CODEOP1)

Address: (See Table 30-1)
SFR address for reading: 0xF922 (CODEOP1L/CODEOP1), 0xF923(CODEOP1H)
Access to SFR : R
Access size to SFR: 8/16 bit
Initial value: 0xFFFF (Erased or factory default setting for products with blank flash memory)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CODEOP1															
Byte	CODEOP1H								CODEOP1L							
Bit	-	-	-	-	-	-	-	-	-	VLMD	-	-	PLLMD1	PLLMD0	CPUMD1	CPUMD0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15 to 7	-	Reserved bits. Set "1" to all bits.
6	VLMD	If V_{DDL} voltage is not lowered except in STOP-D/HALT-D mode, set it to 0. If setting “1”, wake-up time from the HALT-H for PLL16/24M may be delayed comparing with setting “0”.
5, 4	-	Reserved bits. Set "1" to all bits.
3, 2	PLLMD1, PLLMD0	Select the PLL reference frequency. 00: 1MHz 01: Do not use 10: 24 MHz 11: 16 MHz (Initial value) The following table shows the relation between the PLL reference frequency and the maximum operating frequency of CPU and the peripheral circuits.

PLL frequency	Maximum operating frequency		
	Peripheral circuit	CPU (wait mode)	CPU (no-wait mode)
24MHz	24MHz	24MHz	6MHz
16MHz	16MHz	16MHz	8MHz
1MHz	1MHz	1MHz	1MHz

		See Chapter 2 "CPU and Memory Space" and Appendix C "Instruction Execution Cycle" for the CPU operation modes (wait mode and no-wait mode).
1, 0	CPUMD1, CPUMD0	Select the CPU operation mode. 00: Prohibited to use (wait mode) 01: Wait mode 10: Prohibited to use (no-wait mode) 11: No-wait mode (Initial value)

30.2.4 Code Option 2 (CODEOP2)

Address: (See Table 30-1)
SFR address for reading: 0xF924 (CODEOP2L/CODEOP2), 0xF925 (CODEOP2H)
Access to SFR : R
Access size to SFR: 8/16 bit
Initial value: 0xFFFF (Erased or factory default setting for products with blank flash memory)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CODEOP2															
Byte	CODEOP2H								CODEOP2L							
Bit	CREMAPMD	CRES2	CRES1	CRES0	CREA15	CREA14	CREA13	CREA12	-	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit No.	Bit symbol name	Description
15	CREMAPMD	Control the initial value of Flash Remap Address Register (REMAPADD) after system reset. 0: The initial value of the REMAPADD consists of CREA15 to 12 bits and CRES1 to 0 bits 1: The initial value of the REMAPADD is 0x00 If setting this bit to "0", The initial value of the REMAPADD consists of CREA15 to 12 bits and CRES2 to 0 bits. For details on REMAPADD, see Section 2.7.3 "Flash Remap Address Register (REMAPADD)". The remap function is enabled by setting REMAPMD bit of the Code Options 0. The MCU remaps to the address specified with the CREA15 to 12 bits and the CRES1 to 0 bits every time at the system reset. See also Section 2.8.3 "Code Option Remap".
14 to 12	CRES2 to CRES0	Set the initial values of RES2 to RES0 bits of the Flash Remap Address Register (REMAPADD). RES2 and RES1 are reserved bits.
11 to 8	CREA15 to CREA12	Set the initial values of REA15 to REA12 bits of the Flash Remap Address Register (REMAPADD).
7 to 0	-	Reserved bits. Set "1" to all bits.

CPU instruction execution start address after releasing the reset

Reset	REMAPMD	CREMAPMD	Remap function	CPU instruction execution start address
CPU reset (BRK instruction)	1	1	Disabled	0x0000
	1	0		
	0	1	Enabled Software remap	Address set in the REMAPADD register
	0	0		
System reset	1	1	Disabled	0x0000
	1	0		
	0	1	Enabled Code option remap	Initial data of the REMAPADD register (data set by the Code Options 2)
	0	0		

See Section 2.7.3 "Flash Remap Address Register (REMAPADD)" and Section 2.8.3 "Code Option Remap".

30.3 Code Option Data Setting

The address of code option area is dependent of the size of the program memory space (flash memory).
Table 30-1 shows addresses of code option areas for each product.

Table 30-1 List of Addresses of Code Option Areas for Each Product

Product name	Program memory space size	Code Option area	Address		
			CODEOP2	CODEOP1	CODEOP0
ML62Q2727/2737/2747	256K byte	0x3:FFC0 to 0x3:FFFF	0x3:FFD4	0x3:FFD2	0x3:FFD0
ML62Q2726/2736/2746	192K byte	0x2:FFC0 to 0x2:FFFF	0x2:FFD4	0x2:FFD2	0x2:FFD0
ML62Q2725/2735/2745	160K byte	0x2:7FC0 to 0x2:7FFF	0x2:7FD4	0x2:7FD2	0x2:7FD0
ML62Q2703/2713/2723	96K byte	0x1:7FC0 to 0x1:7FFF	0x1:7FD4	0x1:7FD2	0x1:7FD0
ML62Q2702/2712/2722	64K byte	0x0:FFC0 to 0x0:FFFF	0x0:FFD4	0x0:FFD2	0x0:FFD0

Figure 30-2 shows an example of a code option setting program (for products with the program memory space=160 Kbytes). The setting is described in the start-up file (ML622xxx.ASM) of each product.
Set every unused bit of the code option data area to "1".
For products with blank flash memory, every bit has been set to "1" as the factory default setting.

```
;--------------------------------------------------------------------
;            Filling the Test area at code memory
;--------------------------------------------------------------------
    cseg #2 at      07fc0h      ; address
        dw          0ffffh      ; 07fc0h
        dw          0ffffh      ; 07fc2h
        dw          0ffffh      ; 07fc4h
        dw          0ffffh      ; 07fc6h
        dw          0ffffh      ; 07fc8h
        dw          0ffffh      ; 07fcah
        dw          0ffffh      ; 07fcch
        dw          0ffffh      ; 07fceh
        dw          0eef8h      ; 07fd0h（CODEOP0）
    ; Unused ROM area access reset disabled, remapping operation enabled, WDT operation disabled
        dw          0fff9h      ; 07fd2h（CODEOP1）
    ; PLL frequency 24 MHz, CPU wait mode
        dw          04dffh      ; 07fd4h（CODEOP2）
    ; Remapping address(0:d000h)
        dw          0ffffh      ; 07fd6h
        dw          0ffffh      ; 07fd8h
        dw          0ffffh      ; 07fdah
        dw          0ffffh      ; 07fdch
        dw          0ffffh      ; 07fdeh

    cseg #2 at      0ffe0h      ; address
        dw          0ffffh      ; 07fe0h
    ……
    ……
```

Figure 30-2 Example of Code Option Data Program (for Products with the Program Memory Space = 160Kbytes)

[Note]

- **For the code option data definition, always use the dw directive instruction to configure the data in the unit of word.**

Chapter 31 Auxiliary Function

31. Auxiliary Function

31.1 General Description

- Indication of Product ID
- Indication of unique chip ID (32bit); reading from FLASH
- Bit swap for Max. 32bit data; converting MSB/LSB.
- Byte swap for Max. 32bit data; converting Big/Little endian.

31.2 Description of Registers

31.2.1 List of Registers

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF930	Product ID register 0	PID0L	PID0	R	8/16	*1
0xF931		PID0H		R	8	*1
0xF932	Product ID register 1	PID1L	PID1	R	8/16	0x22
0xF933		PID1H		R	8	0x06
0xF940	Converting Base Data register L	CNVBD0	CNVBDL	R/W	8/16	Undefined
0xF941		CNVBD1		R/W	8	Undefined
0xF942	Converting Base Data register H	CNVBD2	CNVBDH	R/W	8/16	Undefined
0xF943		CNVBD3		R/W	8	Undefined
0xF944	Bit Swap Result register L	CNVAD0	CNVADL	R	8/16	Undefined
0xF945		CNVAD1		R	8	Undefined
0xF946	Bit Swap Result register H	CNVAD2	CNVADH	R	8/16	Undefined
0xF947		CNVAD3		R	8	Undefined
0xF948	Byte Swap Result register L	CNVED0	CNVEDL	R	8/16	Undefined
0xF949		CNVED1		R	8	Undefined
0xF94A	Byte Swap Result register H	CNVED2	CNVEDH	R	8/16	Undefined
0xF94B		CNVED3		R	8	Undefined

*1: It depends on product.

31.2.2 Product ID Register 0,1 (PID0, PID1)

This is a SFR to indicate product ID.

Address : 0xF930 (PID0L/PID0), 0xF931(PID0H), 0xF932 (PID1L/PID1), 0xF933(PID1H),
Access : R
Access size : 8/16 bit
Initial value : PID1: 0622, PID0:5xx0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PID1															
Byte	PID1H								PID1L							
Bit	-	-	-	-	d53	d52	d51	d50	d43	d42	d41	d40	d33	d32	d31	d30
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1	0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	PID0															
Byte	PID0H								PID0L							
Bit	d23	d22	d21	d20	d13	d12	d11	d10	d03	d02	d01	d00	ex3	ex2	ex1	ex0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0	1	0	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0

Bit No.	Bit symbol name	Description
15 to 4	-	Indicates 6-digit number of product name. The upper 20-bit number is fixed at “0x6227”. The lower 8-bit number depends on the product name.
3 to 0	-	Indicates 1 character from A to F as extended identifier of product. If the product name has “P” or “T”, it is ignored. If the product name has no alphabet, this indicates “0” in principle.

Ex) ML62Q2747 : “0x0622_7470”

31.2.3 Converting Base Data Register L/H (CNVBDL, CNVBDH)

This is a SFR to set a conversion source data.

Address : 0xF940 (CNVBD0/CNVBDL), 0xF941 (CNVBD1), 0xF942 (CNVBD2/CNVBDH), 0xF943 (CNVBD3)
Access : R/W
Access size : 8/16 bit
Initial value : Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CNVBDH															
Byte	CNVBD3								CNVBD2							
Bit	d31	d30	d29	d28	d27	d26	d25	d24	d23	d22	d21	d20	d19	d18	d17	d16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CNVBDL															
Byte	CNVBD1								CNVBD0							
Bit	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

31.2.4 Bit Swap Result Register L/H (CNVADL, CNVADH)

This is a SFR to read a bit-swap converted data. The bit-swap is a conversion that reverses bit by bit.

Address : 0xF944 (CNVAD0/CNVADL), 0xF945 (CNVAD1), 0xF946 (CNVAD2/CNVADH), 0xF947 (CNVAD3)
Access : R
Access size : 8/16 bit
Initial value : Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CNVADH															
Byte	CNVAD3								CNVAD2							
Bit	d0	d1	d2	d3	d4	d5	d6	d7	d8	d9	d10	d11	d12	d13	d14	d15
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CNVADL															
Byte	CNVAD1								CNVAD0							
Bit	d16	d17	d18	d19	d20	d21	d22	d23	d24	d25	d26	d27	d28	d29	d30	d31
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

31.2.5 Byte Swap Result Register L/H (CNVEDL, CNVEDH)

This is a SFR to read a byte-swap converted data. The bit-swap is a conversion that reverses byte by byte.

Address : 0xF948 (CNVED0/CNVEDL), 0xF949 (CNVED1), 0xF94A (CNVED2/CNVEDH), 0xF94B (CNVED3)
Access : R
Access size : 8/16 bit
Initial value : Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CNVEDH															
Byte	CNVED3								CNVED2							
Bit	d7	d6	d5	d4	d3	d2	d1	d0	d15	d14	d13	d12	d11	d10	d9	d8
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word	CNVEDL															
Byte	CNVED1								CNVED0							
Bit	d23	d22	d21	d20	d19	d18	d17	d16	d31	d30	d29	d28	d27	d26	d25	d24
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Initial value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

31.3 Description of Operation

31.3.1 How to Confirm Unique ID

A LSI chip of ML62Q2700 group has unique ID with 32-bit. It is to read from test area in data memory space.
The address assignment is different for each product.

Table 31-1 Address to read for each product

Product name	Program Memory size	Data Memory Space Address to read.
ML62Q27x7	256KByte	0xC:03F8~B
ML62Q27x6	192KByte	0xB:03F8~B
ML62Q27x5	160KByte	0xA:83F8~B
ML62Q27x3	96KByte	0x9:83F8~B
ML62Q27x2	64KByte	0x9:03F8~B

31.3.2 Data Swap Function

Set data to CNVBDL and CNVBDH registers, then Read a bit-swap result from CNVADL/CNVADH registers and a byte-swap result from CNVEDL/CNVEDH registers.

Ex)
In the case that CNVBDH = 0x1234, CNVBDL = 0x5678,

Result :
CNVADH = 0x1E6A, CNVADL = 0x2C48
CNVEDH = 0x7856, CNVADL = 0x3412

Appendix

Appendix A SFR List

The SFR list is show below. The functionality is not guaranteed when access to "Reserved" register. So please do not access them.
Initial value with *1 depend on code option that is set. See Chapter "30 Code option".
Initial value with *2 depend on product. See Chapter "31 Auxiliary Function".

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF000	Data segment register	DSR	-	R/W	8	0x00
0xF001	Reserved	-	-	-	-	-
0xF002	High-speed clock mode register	FHCKMODL	FHCKMOD	R/W	8/16	0x00
0xF003		FHCKMODH		R/W	8	0x43
0xF004	Low-speed clock mode register	FLMODL	FLMOD	R/W	8/16	0x00
0xF005		FLMODH		R/W	8	0x00
0xF006	Clock control register	FCON	FCONW	R/W	8/16	0x00
0xF007		FCON1		R/W	8	0x00
0xF008	High-speed clock wake up time setting register	FHWUPT	-	R/W	8	0x00
0xF009 to 0xF00B	Reserved	-	-	-	-	-
0xF00C	Backup Clock Status register	FBUSTAT	FBUSTATW	R/W	8/16	0x01
0xF00D		FBUSTATH		R	8	0x01
0xF00E	Reserved	-	-	-	-	-
0xF00F	Reserved	-	-	-	-	-
0xF010	Watchdog timer control register	WDTCON	-	R/W	8	0x00
0xF011	Reserved	-	-	-	-	-
0xF012	Watchdog timer mode register	WDTMOD	-	R/W	8	0x06
0xF013	Reserved	-	-	-	-	-
0xF014	Watchdog timer counter register	WDTMCL	WDTMC	R	8/16	0x00
0xF015		WDTMCH		R	8	0x00
0xF016	Watchdog timer status register	WDTSTA	-	R	8	0x01
0xF017	Reserved	-	-	-	-	-
0xF018	Stop code acceptor	STPACP	-	W	8	0x00
0xF019	Reserved	-	-	-	-	-
0xF01A	Standby control register	SBYCONL	SBYCON	W	8/16	0x00
0xF01B		SBYCONH		R/W	8	0x00
0xF01C	Standby prohibition flag register	SBYEFLG	-	R	8	0x00
0xF01D to 0xF01F	Reserved	-	-	-	-	-
0xF020	Interrupt enable register 01	IE0	IE01	R/W	8/16	0x00
0xF021		IE1		R/W	8	0x00
0xF022	Interrupt enable register 23	IE2	IE23	R/W	8/16	0x00
0xF023		IE3		R/W	8	0x00
0xF024	Interrupt enable register 45	IE4	IE45	R/W	8/16	0x00
0xF025		IE5		R/W	8	0x00
0xF026	Interrupt enable register 67	IE6	IE67	R/W	8/16	0x00
0xF027		IE7		R/W	8	0x00
0xF028	Interrupt request register 01	IRQ0	IRQ01	R/W	8/16	0x00
0xF029		IRQ1		R/W	8	0x00
0xF02A	Interrupt request register 23	IRQ2	IRQ23	R/W	8/16	0x00
0xF02B		IRQ3		R/W	8	0x00
0xF02C	Interrupt request register 45	IRQ4	IRQ45	R/W	8/16	0x00
0xF02D		IRQ5		R/W	8	0x00
0xF02E	Interrupt request register 67	IRQ6	IRQ67	R/W	8/16	0x00
0xF02F		IRQ7		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF030	Interrupt level control enable register	ILEN	-	R/W	8	0x00
0xF031	Reserved	-	-	-	-	-
0xF032	Current interrupt level management register	CIL	-	R/W	8	0x00
0xF033	Interrupt level mask register	MCIL	-	R/W	8	0x00
0xF034	Interrupt level control register 0	ILC00	ILC0	R/W	8/16	0x00
0xF035		ILC01		R/W	8	0x00
0xF036	Interrupt level control register 1	ILC10	ILC1	R/W	8/16	0x00
0xF037		ILC11		R/W	8	0x00
0xF038	Interrupt level control register 2	ILC20	ILC2	R/W	8/16	0x00
0xF039		ILC21		R/W	8	0x00
0xF03A	Interrupt level control register 3	ILC30	ILC3	R/W	8/16	0x00
0xF03B		ILC31		R/W	8	0x00
0xF03C	Interrupt level control register 4	ILC40	ILC4	R/W	8/16	0x00
0xF03D		ILC41		R/W	8	0x00
0xF03E	Interrupt level control register 5	ILC50	ILC5	R/W	8/16	0x00
0xF03F		ILC51		R/W	8	0x00
0xF040	Interrupt level control register 6	ILC60	ILC6	R/W	8/16	0x00
0xF041		ILC61		R/W	8	0x00
0xF042	Interrupt level control register 7	ILC70	ILC7	R/W	8/16	0x00
0xF043		ILC71		R/W	8	0x00
0xF044	External interrupt control register 0	EICON0L	EICON0	R/W	8/16	0x00
0xF045		EICON0H		R/W	8	0x00
0xF046	Reserved	-	-	-	-	-
0xF047	Reserved	-	-	-	-	-
0xF048	External interrupt mode register 0	EIMOD0L	EIMOD0	R/W	8/16	0x00
0xF049		EIMOD0H		R/W	8	0x00
0xF04A	Reserved	-	-	R	8	0x00
0xF04B	Reserved	-	-	R	8	0x00
0xF04C	External interrupt port selection register 0	EIPSEL0L	EIPSEL0	R/W	8/16	0x00
0xF04D		EIPSEL0H		R/W	8	0x00
0xF04E	Reserved	-	-	-	-	-
0xF04F	Reserved	-	-	-	-	-
0xF050	MCU Status Interrupt Enable Register	MCINTEL	-	R/W	8	0x00
0xF051	Reserved	-	-	-	-	-
0xF052	MCU Status Interrupt Register	MCISTATL	-	R	8	0x00
0xF053	Reserved	-	-	-	-	-
0xF054	MCU Status Interrupt Clear Register (L/H)	MCINTCLL	-	W	8	0x00
0xF055		MCINTCLH		W	8	0x00
0xF056	Reserved	-	-	-	-	-
0xF057	Reserved	-	-	-	-	-
0xF058	Reset status register	RSTATL	RSTAT	R/W	8/16	Undefined
0xF059		RSTATH		R/W	8	Undefined
0xF05A	Safety function reset status register	SRSTAT	-	R/W	8	Undefined
0xF05B	Reserved	-	-	-	-	-
0xF05C	Software reset acceptor	SOFTRACP	-	W	8	0x00
0xF05D	Reserved	-	-	-	-	-
0xF05E	Software reset control register	SOFTRCON	-	R/W	8	0x00
0xF05F to 0xF06F	Reserved	-	-	-	-	-
0xF070	Block clock control register 0	BCKCON0L	BCKCON0	R/W	8/16	0x7F
0xF071		BCKCON0H		R/W	8	0x01

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF072	Block clock control register 1	BCKCON1L	BCKCON1	R/W	8/16	0xFF
0xF073		BCKCON1H		R/W	8	0x13
0xF074	Block clock control register 2	BCKCON2L	BCKCON2	R/W	8/16	0x7F
0xF075		BCKCON2H		R/W	8	0x18
0xF076	Block clock control register 3	BCKCON3L	BCKCON3	R/W	8/16	0x05
0xF077		BCKCON3H		R/W	8	0x77
0xF078	Block reset control register 0	BRECON0L	BRECON0	R/W	8/16	0x7F
0xF079		BRECON0H		R/W	8	0x01
0xF07A	Block reset control register 1	BRECON1L	BRECON1	R/W	8/16	0xFF
0xF07B		BRECON1H		R/W	8	0x13
0xF07C	Block reset control register 2	BRECON2L	BRECON2	R/W	8/16	0x7F
0xF07D		BRECON2H		R/W	8	0x18
0xF07E	Block reset control register 3	BRECON3L	BRECON3	R/W	8/16	0x05
0xF07F		BRECON3H		R/W	8	0x77
0xF080 to 0xF085	Reserved	-	-	-	-	-
0xF086	High speed time base clock setting register	HTBDR	-	R/W	8	0x00
0xF087 to 0xF08F	Reserved	-	-	-	-	-
0xF090	Flash address register	FLASHAL	FLASHA	R/W	8/16	0xFF
0xF091		FLASHAH		R/W	8	0xFF
0xF092	Flash data register 0	FLASHD0L	FLASHD0	R/W	8/16	0xFF
0xF093		FLASHD0H		R/W	8	0xFF
0xF094	Flash data register 1	FLASHD1L	FLASHD1	R/W	8/16	0xFF
0xF095		FLASHD1H		R/W	8	0xFF
0xF096	Flash control register	FLASHCON	-	W	8	0x00
0xF097	Reserved	-	-	-	-	-
0xF098	Flash acceptor	FLASHACP	-	W	8	0x00
0xF099	Reserved	-	-	-	-	-
0xF09A	Flash segment register	FLASHSEG	-	R/W	8	0x10
0xF09B	Reserved	-	-	-	-	-
0xF09C	Flash self register	FLASHSLF	-	R/W	8	0x00
0xF09D	Reserved	-	-	-	-	-
0xF09E	Flash status register	FLASHSTA	-	R	8	0x00
0xF09F	Reserved	-	-	-	-	-
0xF0A0	Flash remap address register	REMAPADD	-	R/W	8	*1
0xF0A1 to 0xF0AF	Reserved	-	-	-	-	-
0xF0B0	RAM Guard Setting Register 0	RAMGD	-	R/W	8	0x00
0xF0B1 to 0xF0B3	Reserved	-	-	-	-	-
0xF0B4	SFR Guard Setting Register 0	SFRGD0L	SFRGD0	R/W	8/16	0x00
0xF0B5		SFRGD0H		R/W	8	0x00
0xF0B6	SFR Guard Setting Register 1	SFRGD1L	SFRGD1	R/W	8/16	0x00
0xF0B7		SFRGD1H		R/W	8	0x00
0xF0B8 to 0xF0BB	Reserved	-	-	-	-	-
0xF0BC	RAM Parity Setting Register	RASFMOD	-	R/W	8	0x00
0xF0BD	Reserved	-	-	-	-	-
0xF0BE	Communication Test Setting Register 0	COMFT0L	COMFT0	R/W	8/16	0x00
0xF0BF		COMFT0H		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF0C0 to 0xF0C3	Reserved	-	-	-	-	-
0xF0C4	Clock backup test mode acceptor	FBTACP	-	W	8	0x00
0xF0C5	Reserved	-	-	-	-	-
0xF0C6	Clock backup test mode register	FBTCON	-	R/W	8	0x00
0xF0C7 to 0xF0CF	Reserved	-	-	-	-	-
0xF0D0	Automatic CRC Calculation Start Address Setting Register	CRCSADL	CRCSAD	R/W	8/16	0x00
0xF0D1		CRCSADH		R/W	8	0x00
0xF0D2	Automatic CRC Calculation End Address Setting Register	CRCEADL	CRCEAD	R/W	8/16	0xFC
0xF0D3		CRCEADH		R/W	8	0xFF
0xF0D4	Automatic CRC Calculation Start Segment Setting Register	CRCSSEG	-	R/W	8	0x00
0xF0D5	Reserved	-	-	-	-	-
0xF0D6	Automatic CRC Calculation End Segment Setting Register	CRCESEG	-	R/W	8	0x0F
0xF0D7	Reserved	-	-	-	-	-
0xF0D8	CRC Calculation Data Register	CRCDATA	-	R/W	8	0x00
0xF0D9	Reserved	-	-	-	-	-
0xF0DA	CRC Calculation Result Register	CRCRESL	CRCRES	R/W	8/16	0xFF
0xF0DB		CRCRESH		R/W	8	0xFF
0xF0DC	CRC Calculation Mode Register	CRCMOD	-	R/W	8	0x00
0xF0DD to0xF0E3	Reserved	-	-	-	-	-
0xF0E4	Extended External Interrupt Control Register 0	EEICON0L	EEICON0	R/W	8/16	0x00
0xF0E5		EEICON0H		R/W	8	0x00
0xF0E6	Reserved	-	-	-	-	-
0xF0E7	Reserved	-	-	-	-	-
0xF0E8	Extended External Interrupt Mode Registe 0	EEIMOD0L	EEIMOD0	R/W	8/16	0x00
0xF0E9		EEIMOD0H		R	8	0x00
0xF0EA	Extended External Interrupt Mode Registe 1	EEIMOD1L	EEIMOD1	R/W	8/16	0x00
0xF0EB		EEIMOD1H		R	8	0x00
0xF0EC	Extended External Interrupt Status Registe	EEISTATL	EEISTAT	R	8/16	0x00
0xF0ED		EEISTATH		R	8	0x00
0xF0EE	Extended External Interrupt Clear Registe	EEINTCL	EEINTC	W	8/16	0x00
0xF0EF		EEINTCH		W	8	0x00
0xF0F0	BIAS Control Register	BIASCONL	BIASCON	R/W	8/16	0x08
0xF0F1		BIASCONH	—	R/W	8	0x00
0xF0F2	Display Mode Register	DSPMODL	DSPMOD	R/W	8/16	0x40
0xF0F3		DSPMODH		R/W	8	0x00
0xF0F4	Display Control Register	DSPCONL	DSPCON	R/W	8/16	0x00
0xF0F5		DSPCONH		R/W	8	0x00
0xF0F6	Segiment Mode Register 0	SEGMOD0L	SEGMOD0	R/W	8/16	0x00
0xF0F7		SEGMOD0H		R/W	8	0x00
0xF0F8	Segiment Mode Register 1	SEGMOD1L	SEGMOD1	R/W	8/16	0x00
0xF0F9		SEGMOD1H		R/W	8	0x00
0xF0FA	Segiment Mode Register 2	SEGMOD2L	SEGMOD2	R/W	8/16	0x00
0xF0FB		SEGMOD2H		R/W	8	0x00
0xF0FC	Segiment Mode Register 3	SEGMOD3L	SEGMOD3	R/W	8/16	0x00
0xF0FD		SEGMOD3H		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF0FE	Segiment Mode Register 4	SEGMOD4L	SEGMOD4	R/W	8/16	0x00
0xF0FF		—		R	8	0x00
0xF100	Display Register 0	DSPR00	DSPRW00	R/W	8/16	Undefined
0xF101	Display Register 1	DSPR01		R/W	8	Undefined
0xF102	Display Register 2	DSPR02	DSPRW02	R/W	8/16	Undefined
0xF103	Display Register 3	DSPR03		R/W	8	Undefined
0xF104	Display Register 4	DSPR04	DSPRW04	R/W	8/16	Undefined
0xF105	Display Register 5	DSPR05		R/W	8	Undefined
0xF106	Display Register 6	DSPR06	DSPRW06	R/W	8/16	Undefined
0xF107	Display Register 7	DSPR07		R/W	8	Undefined
0xF108	Display Register 8	DSPR08	DSPRW08	R/W	8/16	Undefined
0xF109	Display Register 9	DSPR09		R/W	8	Undefined
0xF10A	Display Register 10	DSPR10	DSPRW10	R/W	8/16	Undefined
0xF10B	Display Register 11	DSPR11		R/W	8	Undefined
0xF10C	Display Register 12	DSPR12	DSPRW12	R/W	8/16	Undefined
0xF10D	Display Register 13	DSPR13		R/W	8	Undefined
0xF10E	Display Register 14	DSPR14	DSPRW14	R/W	8/16	Undefined
0xF10F	Display Register 15	DSPR15		R/W	8	Undefined
0xF110	Display Register 16	DSPR16	DSPRW16	R/W	8/16	Undefined
0xF111	Display Register 17	DSPR17		R/W	8	Undefined
0xF112	Display Register 18	DSPR18	DSPRW18	R/W	8/16	Undefined
0xF113	Display Register 19	DSPR19		R/W	8	Undefined
0xF114	Display Register 20	DSPR20	DSPRW20	R/W	8/16	Undefined
0xF115	Display Register 21	DSPR21		R/W	8	Undefined
0xF116	Display Register 22	DSPR22	DSPRW22	R/W	8/16	Undefined
0xF117	Display Register 23	DSPR23		R/W	8	Undefined
0xF118	Display Register 24	DSPR24	DSPRW24	R/W	8/16	Undefined
0xF119	Display Register 25	DSPR25		R/W	8	Undefined
0xF11A	Display Register 26	DSPR26	DSPRW26	R/W	8/16	Undefined
0xF11B	Display Register 27	DSPR27		R/W	8	Undefined
0xF11C	Display Register 28	DSPR28	DSPRW28	R/W	8/16	Undefined
0xF11D	Display Register 29	DSPR29		R/W	8	Undefined
0xF11E	Display Register 30	DSPR30	DSPRW30	R/W	8/16	Undefined
0xF11F	Display Register 31	DSPR31		R/W	8	Undefined
0xF120	Display Register 32	DSPR32	DSPRW32	R/W	8/16	Undefined
0xF121	Display Register 33	DSPR33		R/W	8	Undefined
0xF122	Display Register 34	DSPR34	DSPRW34	R/W	8/16	Undefined
0xF123	Display Register 35	DSPR35		R/W	8	Undefined
0xF124	Display Register 36	DSPR36	DSPRW36	R/W	8/16	Undefined
0xF125	Display Register 37	DSPR37		R/W	8	Undefined
0xF126	Display Register 38	DSPR38	DSPRW38	R/W	8/16	Undefined
0xF127	Display Register 39	DSPR39		R/W	8	Undefined
0xF128	Display Register 40	DSPR40	DSPRW40	R/W	8/16	Undefined
0xF129	Display Register 41	DSPR41		R/W	8	Undefined
0xF12A	Display Register 42	DSPR42	DSPRW42	R/W	8/16	Undefined
0xF12B	Display Register 43	DSPR43		R/W	8	Undefined
0xF12C	Display Register 44	DSPR44	DSPRW44	R/W	8/16	Undefined
0xF12D	Display Register 45	DSPR45		R/W	8	Undefined
0xF12E	Display Register 46	DSPR46	DSPRW46	R/W	8/16	Undefined
0xF12F	Display Register 47	DSPR47		R/W	8	Undefined

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF130	Display Register 48	DSPR48	DSPRW48	R/W	8/16	Undefined
0xF131	Display Register 49	DSPR49		R/W	8	Undefined
0xF132	Display Register 50	DSPR50	DSPRW50	R/W	8/16	Undefined
0xF133	Display Register 51	DSPR51		R/W	8	Undefined
0xF134	Display Register 52	DSPR52	DSPRW52	R/W	8/16	Undefined
0xF135	Display Register 53	DSPR53		R/W	8	Undefined
0xF136	Display Register 54	DSPR54	DSPRW54	R/W	8/16	Undefined
0xF137	Display Register 55	DSPR55		R/W	8	Undefined
0xF138	Display Register 56	DSPR56	DSPRW56	R/W	8/16	Undefined
0xF139	Display Register 57	DSPR57		R/W	8	Undefined
0xF13A	Display Register 58	DSPR58	DSPRW58	R/W	8/16	Undefined
0xF13B	Display Register 59	DSPR59		R/W	8	Undefined
0xF13C	Display Register 60	DSPR60	DSPRW60	R/W	8/16	Undefined
0xF13D	Display Register 61	DSPR61		R/W	8	Undefined
0xF13E	Display Register 62	DSPR62	DSPRW62	R/W	8/16	Undefined
0xF13F	Display Register 63	DSPR63		R/W	8	Undefined
0xF140	Display Register 64	DSPR64	DSPRW64	R/W	8/16	Undefined
0xF141 to 0xF1FF	Reserved	—	—	—	—	—
0xF200	Port 0 data register	P0DI	P0D	R	8/16	0xFF
0xF201		P0DO		R/W	8	0x00
0xF202	Reserved	-	-	-	-	-
0xF203	Port 0 mode register 1	P0MOD1	-	R/W	8	0x05
0xF204	Port 0 mode register 23	P0MOD2	P0MOD23	R/W	8/16	0x00
0xF205		P0MOD3		R/W	8	0x00
0xF206	Port 0 mode register 45	P0MOD4	P0MOD45	R/W	8/16	0x00
0xF207		P0MOD5		R/W	8	0x00
0xF208	Port 0 mode register 67	P0MOD6	P0MOD67	R/W	8/16	0x00
0xF209		P0MOD7		R/W	8	0x00
0xF20A	Port 0 pulse mode register	P0PMDL	P0PMD	R/W	8/16	0x00
0xF20B		P0PMDH		R/W	8	0x00
0xF20C	Port 0 pulse selection register	P0PSLL	P0PSL	R/W	8/16	0x00
0xF20D		P0PSLH		R/W	8	0x00
0xF20E	Reserved	-	-	-	-	-
0xF20F	Reserved	-	-	-	-	-
0xF210	Port 1 data register	P1DI	P1D	R	8/16	0xFF
0xF211		P1DO		R/W	8	0x00
0xF212	Port 1 mode register 01	P1MOD0	P1MOD01	R/W	8/16	0x00
0xF213		P1MOD1		R/W	8	0x00
0xF214	Port 1 mode register 23	P1MOD2	P1MOD23	R/W	8/16	0x00
0xF215		P1MOD3		R/W	8	0x00
0xF216	Port 1 mode register 45	P1MOD4	P1MOD45	R/W	8/16	0x00
0xF217		P1MOD5		R/W	8	0x00
0xF218	Port 1 mode register 67	P1MOD6	P1MOD67	R/W	8/16	0x00
0xF219		P1MOD7		R/W	8	0x00
0xF21A	Port 1 pulse mode register	P1PMDL	P1PMD	R/W	8/16	0x00
0xF21B		P1PMDH		R/W	8	0x00
0xF21C	Port 1 pulse selection register	P1PSLL	P1PSL	R/W	8/16	0x00
0xF21D		P1PSLH		R/W	8	0x00
0xF21E	Reserved	-	-	-	-	-
0xF21F	Reserved	-	-	-	-	-

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF220	Port 2 data register	P2DI	P2D	R	8/16	0xFF
0xF221		P2DO		R/W	8	0x00
0xF222	Port 2 mode register 01	P2MOD0	P2MOD01	R/W	8/16	0x00
0xF223		P2MOD1		R/W	8	0x00
0xF224	Port 2 mode register 23	P2MOD2	P2MOD23	R/W	8/16	0x00
0xF225		P2MOD3		R/W	8	0x00
0xF226	Port 2 mode register 45	P2MOD4	P2MOD45	R/W	8/16	0x00
0xF227		P2MOD5		R/W	8	0x00
0xF228	Port 2 mode register 67	P2MOD6	P2MOD67	R/W	8/16	0x00
0xF229		P2MOD7		R/W	8	0x00
0xF22A	Port 2 pulse mode register	P2PMDL	P2PMD	R/W	8/16	0x00
0xF22B		P2PMDH		R/W	8	0x00
0xF22C	Port 2 pulse selection register	P2PSLL	P2PSL	R/W	8/16	0x00
0xF22D		P2PSLH		R/W	8	0x00
0xF22E	Reserved	-	-	-	-	-
0xF22F	Reserved	-	-	-	-	-
0xF230	Port 3 data register	P3DI	P3D	R	8/16	0xFF
0xF231		P3DO		R/W	8	0x00
0xF232	Port 3 mode register 01	P3MOD0	P3MOD01	R/W	8/16	0x00
0xF233		P3MOD1		R/W	8	0x00
0xF234	Port 3 mode register 23	P3MOD2	P3MOD23	R/W	8/16	0x00
0xF235		P3MOD3		R/W	8	0x00
0xF236 to 0xF239	Reserved	-	-	-	-	-
0xF23A	Port 3 Pulse Mode Register	P3PMDL	P3PMD	R/W	8/16	0x00
0xF23B		P3PMDH		R/W	8	0x00
0xF23C	Port 3 Pulse Select Register	P3PSLL	P3PSL	R/W	8/16	0x00
0xF23D		P3PSLH		R/W	8	0x00
0xF23E	Reserved	-	-	-	-	-
0xF23F	Reserved	-	-	-	-	-
0xF240	Port 4 Data Register	P4DI	P4D	R	8/16	0xFF
0xF241		P4DO		R/W	8	0x00
0xF242	Port 4 Mode Register 0	P4MOD0	P4MOD01	R/W	8/16	0x00
0xF243		P4MOD1		R/W	8	0x00
0xF244	Port 4 Mode Register 23	P4MOD2	P4MOD23	R/W	8/16	0x00
0xF245		P4MOD3		R/W	8	0x00
0xF246	Port 4 Mode Register 45	P4MOD4	P4MOD45	R/W	8/16	0x00
0xF247		P4MOD5		R/W	8	0x00
0xF248	Port 4 Mode Register 67	P4MOD6	P4MOD67	R/W	8/16	0x00
0xF249		P4MOD7		R/W	8	0x00
0xF24A to 0xF24F	Reserved	-	-	-	-	-
0xF250	Port 5 data register	P5DI	P5D	R	8/16	0xFF
0xF251		P5DO		R/W	8	0x00
0xF252	Port 5 mode register 01	P5MOD0	P5MOD01	R/W	8/16	0x00
0xF253		P5MOD1		R/W	8	0x00
0xF254	Port 5 mode register 23	P5MOD2	P5MOD23	R/W	8/16	0x00
0xF255		P5MOD3		R/W	8	0x00
0xF256	Port 5 mode register 45	P5MOD4	P5MOD45	R/W	8/16	0x00
0xF257		P5MOD5		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF258	Port 5 mode register 67	P5MOD6	P5MOD67	R/W	8/16	0x00
0xF259		P5MOD7		R/W	8	0x00
0xF25A to 0xF25F	Reserved	-	-	-	-	-
0xF260	Port 6 data register	P6DI	P6D	R	8/16	0xFF
0xF261		P6DO		R/W	8	0x00
0xF262	Port 6 mode register 01	P6MOD0	P6MOD01	R/W	8/16	0x00
0xF263		P6MOD1		R/W	8	0x00
0xF264	Port 6 mode register 23	P6MOD2	P6MOD23	R/W	8/16	0x00
0xF265		P6MOD3		R/W	8	0x00
0xF266	Port 6 mode register 45	P6MOD4	P6MOD45	R/W	8/16	0x00
0xF267		P6MOD5		R/W	8	0x00
0xF268	Port 6 mode register 67	P6MOD6	P6MOD67	R/W	8/16	0x00
0xF269		P6MOD7		R/W	8	0x00
0xF26A to 0xF26F	Reserved	-	-	-	-	-
0xF270	Port 7 data register	P7DI	P7D	R	8/16	0xFF
0xF271		P7DO		R/W	8	0x00
0xF272	Port 7 mode register 0	P7MOD0	P7MOD01	R/W	8/16	0x00
0xF273 to 0xF277	Reserved	-	-	-	-	-
0xF278	Port 7 mode register 67	P7MOD6	P7MOD67	R/W	8/16	0x00
0xF279		P7MOD7		R/W	8	0x00
0xF27A to 0xF27F	Reserved	-	-	-	-	-
0xF280	Port 8 data register	P8DI	P8D	R	8/16	0xFF
0xF281		P8DO		R/W	8	0x00
0xF282	Port 8 mode register 01	P8MOD0	P8MOD01	R/W	8/16	0x00
0xF283		P8MOD1		R/W	8	0x00
0xF284	Port 8 mode register 23	P8MOD2	P8MOD23	R/W	8/16	0x00
0xF285		P8MOD3		R/W	8	0x00
0xF286	Port 8 mode register 45	P8MOD4	P8MOD45	R/W	8/16	0x00
0xF287		P8MOD5		R/W	8	0x00
0xF288	Port 8 mode register 67	P8MOD6	P8MOD67	R/W	8/16	0x00
0xF289		P8MOD7		R/W	8	0x00
0xF28A to 0xF28F	Reserved	-	-	-	-	-
0xF290	Port 9 data register	P9DI	P9D	R	8/16	0xFF
0xF291		P9DO		R/W	8	0x00
0xF292	Port 9 mode register 01	P9MOD0	P9MOD01	R/W	8/16	0x00
0xF293		P9MOD1		R/W	8	0x00
0xF294	Port 9 mode register 23	P9MOD2	P9MOD23	R/W	8/16	0x00
0xF295		P9MOD3		R/W	8	0x00
0xF296	Port 9 mode register 45	P9MOD4	P9MOD45	R/W	8/16	0x00
0xF297		P9MOD5		R/W	8	0x00
0xF298	Port 9 mode register 67	P9MOD6	P9MOD67	R/W	8/16	0x00
0xF299		P9MOD7		R/W	8	0x00
0xF29A to 0xF29F	Reserved	-	-	-	-	-

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF2A0	Port A data register	PADI	PAD	R	8/16	0xFF
0xF2A1		PADO		R/W	8	0x00
0xF2A2	Port A mode register 01	PAMOD0	PAMOD01	R/W	8/16	0x00
0xF2A3		PAMOD1		R/W	8	0x00
0xF2A4	Port A mode register 23	PAMOD2	PAMOD23	R/W	8/16	0x00
0xF2A5		PAMOD3		R/W	8	0x00
0xF2A6	Port A mode register 45	PAMOD4	PAMOD45	R/W	8/16	0x00
0xF2A7		PAMOD5		R/W	8	0x00
0xF2A8	Port A mode register 67	PAMOD6	PAMOD67	R/W	8/16	0x00
0xF2A9		PAMOD7		R/W	8	0x00
0xF2AA to 0xF2AF	Reserved	-	-	-	-	-
0xF2B0	Port B data register	PBDI	PBD	R	8/16	0xFF
0xF2B1		PBDO		R/W	8	0x00
0xF2B2	Port B mode register 01	PBMOD0	PBMOD01	R/W	8/16	0x00
0xF2B3		PBMOD1		R/W	8	0x00
0xF2B4	Port B mode register 23	PBMOD2	PBMOD23	R/W	8/16	0x00
0xF2B5		PBMOD3		R/W	8	0x00
0xF2B6	Port B mode register 45	PBMOD4	PBMOD45	R/W	8/16	0x00
0xF2B7		PBMOD5		R/W	8	0x00
0xF2B8	Port B mode register 67	PBMOD6	PBMOD67	R/W	8/16	0x00
0xF2B9		PBMOD7		R/W	8	0x00
0xF2BA to 0xF2EF	Reserved	-	-	-	-	-
0xF2F0	PORTXT data input register	PXTDI	-	R/W	8	0x00
0xF2F1	Reserved	-	-	-	-	-
0xF2F2	PORTXT mode register 01	PXTMOD0	PXTMOD01	R/W	8/16	0x00
0xF2F3		PXTMOD1		R/W	8	0x00
0xF2F4 to 0xF2FF	Reserved	-	-	-	-	-
0xF300	16-bit timer 0 data register	TMH0DL	TMH0D	R/W	8/16	0xFF
0xF301		TMH0DH		R/W	8	0xFF
0xF302	16-bit timer 0 counter register	TMH0CL	TMH0C	R/W	8/16	0x00
0xF303		TMH0CH		R/W	8	0x00
0xF304	16-bit timer 0 mode register	TMH0MODL	TMH0MOD	R/W	8/16	0x00
0xF305		TMH0MODH		R/W	8	0x00
0xF306	Reserved	-	-	-	-	-
0xF307	Reserved	-	-	-	-	-
0xF308	16-bit timer 1 data register	TMH1DL	TMH1D	R/W	8/16	0xFF
0xF309		TMH1DH		R/W	8	0xFF
0xF30A	16-bit timer 1 counter register	TMH1CL	TMH1C	R/W	8/16	0x00
0xF30B		TMH1CH		R/W	8	0x00
0xF30C	16-bit timer 1 mode register	TMH1MODL	TMH1MOD	R/W	8/16	0x00
0xF30D		TMH1MODH		R/W	8	0x00
0xF30E	Reserved	-	-	-	-	-
0xF30F	Reserved	-	-	-	-	-
0xF310	16-bit timer 2 data register	TMH2DL	TMH2D	R/W	8/16	0xFF
0xF311		TMH2DH		R/W	8	0xFF

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF312	16-bit timer 2 counter register	TMH2CL	TMH2C	R/W	8/16	0x00
0xF313		TMH2CH		R/W	8	0x00
0xF314	16-bit timer 2 mode register	TMH2MODL	TMH2MOD	R/W	8/16	0x00
0xF315		TMH2MODH		R/W	8	0x00
0xF316	Reserved	-	-	-	-	-
0xF317	Reserved	-	-	-	-	-
0xF318	16-bit timer 3 data register	TMH3DL	TMH3D	R/W	8/16	0xFF
0xF319		TMH3DH		R/W	8	0xFF
0xF31A	16-bit timer 3 counter register	TMH3CL	TMH3C	R/W	8/16	0x00
0xF31B		TMH3CH		R/W	8	0x00
0xF31C	16-bit timer 3 mode register	TMH3MODL	TMH3MOD	R/W	8/16	0x00
0xF31D		TMH3MODH		R/W	8	0x00
0xF31E	Reserved	-	-	-	-	-
0xF31F	Reserved	-	-	-	-	-
0xF320	16-bit timer 4 data register	TMH4DL	TMH4D	R/W	8/16	0xFF
0xF321		TMH4DH		R/W	8	0xFF
0xF322	16-bit timer 4 counter register	TMH4CL	TMH4C	R/W	8/16	0x00
0xF323		TMH4CH		R/W	8	0x00
0xF324	16-bit timer 4 mode register	TMH4MODL	TMH4MOD	R/W	8/16	0x00
0xF325		TMH4MODH		R/W	8	0x00
0xF326	Reserved	-	-	-	-	-
0xF327	Reserved	-	-	-	-	-
0xF328	16-bit timer 5 data register	TMH5DL	TMH5D	R/W	8/16	0xFF
0xF329		TMH5DH		R/W	8	0xFF
0xF32A	16-bit timer 5 counter register	TMH5CL	TMH5C	R/W	8/16	0x00
0xF32B		TMH5CH		R/W	8	0x00
0xF32C	16-bit timer 5 mode register	TMH5MODL	TMH5MOD	R/W	8/16	0x00
0xF32D		TMH5MODH		R/W	8	0x00
0xF32E	Reserved	-	-	-	-	-
0xF32F	Reserved	-	-	-	-	-
0xF330	16-bit timer 6 data register	TMH6DL	TMH6D	R/W	8/16	0xFF
0xF331		TMH6DH		R/W	8	0xFF
0xF332	16-bit timer 6 counter register	TMH6CL	TMH6C	R/W	8/16	0x00
0xF333		TMH6CH		R/W	8	0x00
0xF334	16-bit timer 6 mode register	TMH6MODL	TMH6MOD	R/W	8/16	0x00
0xF335		TMH6MODH		R/W	8	0x00
0xF336 to 0xF33F	Reserved	-	-	-	-	-
0xF340	16-bit timer start register	TMHSTRL	TMHSTR	W	8/16	0x00
0xF341		TMHSTRH		W	8	0x00
0xF342	16-bit timer stop register	TMHSTPL	TMHSTP	W	8/16	0x00
0xF343		TMHSTPH		W	8	0x00
0xF344	16-bit timer status register	TMHSTATL	TMHSTAT	R	8/16	0x00
0xF345		TMHSTATH		R	8	0x00
0xF346	Reserved	-	-	-	-	-
0xF347	Reserved	-	-	-	-	-
0xF350	16-bit timer X data register	TMHXDL	TMHXD	R/W	8/16	0xFF
0xF351		TMHXDH		R/W	8	0xFF
0xF352	16-bit timer X counter register	TMHXCL	TMHXC	R/W	8/16	0x00
0xF353		TMHXCH		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF354	16-bit timer X mode register	TMHXMODL	TMHXMOD	R/W	8/16	0x00
0xF355		TMHXMODH		R/W	8	0x00
0xF356	Reserved	-	-	-	-	-
0xF357	Reserved	-	-	-	-	-
0xF358	16-bit timer X start register	TMHXSTR	-	W	8	0x00
0xF359	Reserved	-	-	-	-	-
0xF35A	16-bit timer X stop register	TMHXSTP	-	W	8	0x00
0xF35B	Reserved	-	-	-	-	-
0xF35C	16-bit timer X status register	TMHXSTAT	-	R	8	0x00
0xF35D to 0xF37F	Reserved	-	-	-	-	-
0xF380	FTM common update register	FTCUD	-	W	8	0x00
0xF381	Reserved	-	-	-	-	-
0xF382	FTM common control register	FTCCONL	FTCCON	R/W	8/16	0x00
0xF383		FTCCONH		R/W	8	0x00
0xF384	FTM common start register	FTCSTRL	FTCSTR	W	8/16	0x00
0xF385		FTCSTRH		W	8	0x00
0xF386	FTM common stop register	FTCSTPL	FTCSTP	W	8/16	0x00
0xF387		FTCSTPH		W	8	0x00
0xF388	FTM common status register	FTCSTATL	FTCSTAT	R	8/16	0x00
0xF389		FTCSTATH		R	8	0x00
0xF38A to 0xF39F	Reserved	-	-	-	-	-
0xF3A0	Low-speed Time Base Counter register	LTBR0	LTBR01	R/W	8/16	0x00
0xF3A1		LTBR1		R/W	8	0x00
0xF3A2	Low-speed Time Base Counter Control register	LTBCON0	LTBCON	R/W	8/16	0x03
0xF3A3		LTBCON1		R/W	8	0x02
0xF3A4	Reserved	-	-	-	-	-
0xF3A5	Reserved	-	-	-	-	-
0xF3A6	Low-speed Time Base Counter Frequency Adjustment register	LTBADJL	LTBADJ	R/W	8/16	0x00
0xF3A7		LTBADJH		R/W	8	0x00
0xF3A8	Low-speed Time Base Counter Interrupt selection register	LTBINTL	LTBINT	R/W	8/16	0x60
0xF3A9		LTBINTH		R/W	8	0x71
0xF3AA to 0xF3FF	Reserved	-	-	-	-	-
0xF400	FTM0 cycle register	FT0PL	FT0P	R/W	8/16	0xFF
0xF401		FT0PH		R/W	8	0xFF
0xF402	FTM0 event A register	FT0EAL	FT0EA	R/W	8/16	0x00
0xF403		FT0EAH		R/W	8	0x00
0xF404	FTM0 event B register	FT0EBL	FT0EB	R/W	8/16	0x00
0xF405		FT0EBH		R/W	8	0x00
0xF406	FTM0 dead time register	FT0DTL	FT0DT	R/W	8/16	0x00
0xF407		FT0DTH		R/W	8	0x00
0xF408	FTM0 counter register	FT0CL	FT0C	R/W	8/16	0x00
0xF409		FT0CH		R/W	8	0x00
0xF40A	FTM0 status register	FT0STAT	-	R	8	0x30
0xF40B	Reserved	-	-	-	-	-
0xF40C	FTM0 mode register	FT0MODL	FT0MOD	R/W	8/16	0x00
0xF40D		FT0MODH		R/W	8	0x40

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF40E	FTM0 clock register	FT0CLKL	FT0CLK	R/W	8/16	0x00
0xF40F		FT0CLKH		R/W	8	0x00
0xF410	FTM0 trigger register 0	FT0TRG0L	FT0TRG0	R/W	8/16	0x00
0xF411		FT0TRG0H		R/W	8	0x00
0xF412	FTM0 trigger register 1	FT0TRG1L	FT0TRG1	R/W	8/16	0x00
0xF413		FT0TRG1H		R/W	8	0x00
0xF414	FTM0 interrupt enable register	FT0INTEL	FT0INTE	R/W	8/16	0x00
0xF415		FT0INTEH		R/W	8	0x00
0xF416	FTM0 interrupt status register	FT0INTSL	FT0INTS	R	8/16	0x00
0xF417		FT0INTSH		R	8	0x00
0xF418	FTM0 interrupt clear register	FT0INTCL	-	W	8	0x00
0xF419		FT0INTCH		W	8	0x00
0xF41A to 0xF41F	Reserved	-	-	-	-	-
0xF420	FTM1 cycle register	FT1PL	FT1P	R/W	8/16	0xFF
0xF421		FT1PH		R/W	8	0xFF
0xF422	FTM1 event A register	FT1EAL	FT1EA	R/W	8/16	0x00
0xF423		FT1EAH		R/W	8	0x00
0xF424	FTM1 event B register	FT1EBL	FT1EB	R/W	8/16	0x00
0xF425		FT1EBH		R/W	8	0x00
0xF426	FTM1 dead time register	FT1DTL	FT1DT	R/W	8/16	0x00
0xF427		FT1DTH		R/W	8	0x00
0xF428	FTM1 counter register	FT1CL	FT1C	R/W	8/16	0x00
0xF429		FT1CH		R/W	8	0x00
0xF42A	FTM1 status register	FT1STAT	-	R	8	0x30
0xF42B	Reserved	-	-	-	-	-
0xF42C	FTM1 mode register	FT1MODL	FT1MOD	R/W	8/16	0x00
0xF42D		FT1MODH		R/W	8	0x40
0xF42E	FTM1 clock register	FT1CLKL	FT1CLK	R/W	8/16	0x00
0xF42F		FT1CLKH		R/W	8	0x00
0xF430	FTM1 trigger register 0	FT1TRG0L	FT1TRG0	R/W	8/16	0x00
0xF431		FT1TRG0H		R/W	8	0x00
0xF432	FTM1 trigger register 1	FT1TRG1L	FT1TRG1	R/W	8/16	0x00
0xF433		FT1TRG1H		R/W	8	0x00
0xF434	FTM1 interrupt enable register	FT1INTEL	FT1INTE	R/W	8/16	0x00
0xF435		FT1INTEH		R/W	8	0x00
0xF436	FTM1 interrupt status register	FT1INTSL	FT1INTS	R	8/16	0x00
0xF437		FT1INTSH		R	8	0x00
0xF438	FTM1 interrupt clear register	FT1INTCL	FT1INTC	W	8/16	0x00
0xF439		FT1INTCH		W	8	0x00
0xF43A to 0xF43F	Reserved	-	-	-	-	-
0xF440	FTM2 cycle register	FT2PL	FT2P	R/W	8/16	0xFF
0xF441		FT2PH		R/W	8	0xFF
0xF442	FTM2 event A register	FT2EAL	FT2EA	R/W	8/16	0x00
0xF443		FT2EAH		R/W	8	0x00
0xF444	FTM2 event B register	FT2EBL	FT2EB	R/W	8/16	0x00
0xF445		FT2EBH		R/W	8	0x00
0xF446	FTM2 dead time register	FT2DTL	FT2DT	R/W	8/16	0x00
0xF447		FT2DTH		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF448	FTM2 counter register	FT2CL	FT2C	R/W	8/16	0x00
0xF449		FT2CH		R/W	8	0x00
0xF44A	FTM2 status register	FT2STAT	-	R	8	0x30
0xF44B	Reserved	-	-	-	-	-
0xF44C	FTM2 mode register	FT2MODL	FT2MOD	R/W	8/16	0x00
0xF44D		FT2MODH		R/W	8	0x40
0xF44E	FTM2 clock register	FT2CLKL	FT2CLK	R/W	8/16	0x00
0xF44F		FT2CLKH		R/W	8	0x00
0xF450	FTM2 trigger register 0	FT2TRG0L	FT2TRG0	R/W	8/16	0x00
0xF451		FT2TRG0H		R/W	8	0x00
0xF452	FTM2 trigger register 1	FT2TRG1L	FT2TRG1	R/W	8/16	0x00
0xF453		FT2TRG1H		R/W	8	0x00
0xF454	FTM2 interrupt enable register	FT2INTEL	FT2INTE	R/W	8/16	0x00
0xF455		FT2INTEH		R/W	8	0x00
0xF456	FTM2 interrupt status register	FT2INTSL	FT2INTS	R	8/16	0x00
0xF457		FT2INTSH		R	8	0x00
0xF458	FTM2 interrupt clear register	FT2INTCL	FT2INTC	W	8/16	0x00
0xF459		FT2INTCH		W	8	0x00
0xF45A to 0xF45F	Reserved	-	-	-	-	-
0xF460	FTM3 cycle register	FT3PL	FT3P	R/W	8/16	0xFF
0xF461		FT3PH		R/W	8	0xFF
0xF462	FTM3 event A register	FT3EAL	FT3EA	R/W	8/16	0x00
0xF463		FT3EAH		R/W	8	0x00
0xF464	FTM3 event B register	FT3EBL	FT3EB	R/W	8/16	0x00
0xF465		FT3EBH		R/W	8	0x00
0xF466	FTM3 dead time register	FT3DTL	FT3DT	R/W	8/16	0x00
0xF467		FT3DTH		R/W	8	0x00
0xF468	FTM3 counter register	FT3CL	FT3C	R/W	8/16	0x00
0xF469		FT3CH		R/W	8	0x00
0xF46A	FTM3 status register	FT3STAT	-	R	8	0x30
0xF46B	Reserved	-	-	-	-	-
0xF46C	FTM3 mode register	FT3MODL	FT3MOD	R/W	8/16	0x00
0xF46D		FT3MODH		R/W	8	0x40
0xF46E	FTM3 clock register	FT3CLKL	FT3CLK	R/W	8/16	0x00
0xF46F		FT3CLKH		R/W	8	0x00
0xF470	FTM3 trigger register 0	FT3TRG0L	FT3TRG0	R/W	8/16	0x00
0xF471		FT3TRG0H		R/W	8	0x00
0xF472	FTM3 trigger register 1	FT3TRG1L	FT3TRG1	R/W	8/16	0x00
0xF473		FT3TRG1H		R/W	8	0x00
0xF474	FTM3 interrupt enable register	FT3INTEL	FT3INTE	R/W	8/16	0x00
0xF475		FT3INTEH		R/W	8	0x00
0xF476	FTM3 interrupt status register	FT3INTSL	FT3INTS	R	8/16	0x00
0xF477		FT3INTSH		R	8	0x00
0xF478	FTM3 interrupt clear register	FT3INTCL	FT3INTC	W	8/16	0x00
0xF479		FT3INTCH		W	8	0x00
0xF47A to 0xF47F	Reserved	-	-	-	-	-
0xF480	FTM4 cycle register	FT4PL	FT4P	R/W	8/16	0xFF
0xF481		FT4PH		R/W	8	0xFF

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF482	FTM4 event A register	FT4EAL	FT4EA	R/W	8/16	0x00
0xF483		FT4EAH		R/W	8	0x00
0xF484	FTM4 event B register	FT4EBL	FT4EB	R/W	8/16	0x00
0xF485		FT4EBH		R/W	8	0x00
0xF486	FTM4 dead time register	FT4DTL	FT4DT	R/W	8/16	0x00
0xF487		FT4DTH		R/W	8	0x00
0xF488	FTM4 counter register	FT4CL	FT4C	R/W	8/16	0x00
0xF489		FT4CH		R/W	8	0x00
0xF48A	FTM4 status register	FT4STAT	-	R	8	0x30
0xF48B	Reserved	-	-	-	-	-
0xF48C	FTM4 mode register	FT4MODL	FT4MOD	R/W	8/16	0x00
0xF48D		FT4MODH		R/W	8	0x40
0xF48E	FTM4 clock register	FT4CLKL	FT4CLK	R/W	8/16	0x00
0xF48F		FT4CLKH		R/W	8	0x00
0xF490	FTM44 trigger register 0	FT4TRG0L	FT4TRG0	R/W	8/16	0x00
0xF491		FT4TRG0H		R/W	8	0x00
0xF492	FTM4 trigger register 1	FT4TRG1L	FT4TRG1	R/W	8/16	0x00
0xF493		FT4TRG1H		R/W	8	0x00
0xF494	FTM4 interrupt enable register	FT4INTEL	FT4INTE	R/W	8/16	0x00
0xF495		FT4INTEH		R/W	8	0x00
0xF496	FTM4 interrupt status register	FT4INTSL	FT4INTS	R	8/16	0x00
0xF497		FT4INTSH		R	8	0x00
0xF498	FTM4 interrupt clear register	FT4INTCL	FT4INTC	W	8/16	0x00
0xF499		FT4INTCH		W	8	0x00
0xF49A to 0xF49F	Reserved	-	-	-	-	-
0xF4A0	FTM5 cycle register	FT5PL	FT5P	R/W	8/16	0xFF
0xF4A1		FT5PH		R/W	8	0xFF
0xF4A2	FTM5 event A register	FT5EAL	FT5EA	R/W	8/16	0x00
0xF4A3		FT5EAH		R/W	8	0x00
0xF4A4	FTM5 event B register	FT5EBL	FT5EB	R/W	8/16	0x00
0xF4A5		FT5EBH		R/W	8	0x00
0xF4A6	FTM5 dead time register	FT5DTL	FT5DT	R/W	8/16	0x00
0xF4A7		FT5DTH		R/W	8	0x00
0xF4A8	FTM5 counter register	FT5CL	FT5C	R/W	8/16	0x00
0xF4A9		FT5CH		R/W	8	0x00
0xF4AA	FTM5 status register	FT5STAT	-	R	8	0x30
0xF4AB	Reserved	-	-	-	-	-
0xF4AC	FTM5 mode register	FT5MODL	FT5MOD	R/W	8/16	0x00
0xF4AD		FT5MODH		R/W	8	0x40
0xF4AE	FTM5 clock register	FT5CLKL	FT5CLK	R/W	8/16	0x00
0xF4AF		FT5CLKH		R/W	8	0x00
0xF4B0	FTM5 trigger register 0	FT5TRG0L	FT5TRG0	R/W	8/16	0x00
0xF4B1		FT5TRG0H		R/W	8	0x00
0xF4B2	FTM5 trigger register 1	FT5TRG1L	FT5TRG1	R/W	8/16	0x00
0xF4B3		FT5TRG1H		R/W	8	0x00
0xF4B4	FTM5 interrupt enable register	FT5INTEL	FT5INTE	R/W	8/16	0x00
0xF4B5		FT5INTEH		R/W	8	0x00
0xF4B6	FTM5 interrupt status register	FT5INTSL	FT5INTS	R	8/16	0x00
0xF4B7		FT5INTSH		R	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF4B8	FTM5 interrupt clear register	FT5INTCL	FT5INTC	W	8/16	0x00
0xF4B9		FT5INTCH		W	8	0x00
0xF4BA to 0xF4BF	Reserved	-	-	-	-	-
0xF4C0	FTM6 cycle register	FT6PL	FT6P	R/W	8/16	0xFF
0xF4C1		FT6PH		R/W	8	0xFF
0xF4C2	FTM6 event A register	FT6EAL	FT6EA	R/W	8/16	0x00
0xF4C3		FT6EAH		R/W	8	0x00
0xF4C4	FTM6 event B register	FT6EBL	FT6EB	R/W	8/16	0x00
0xF4C5		FT6EBH		R/W	8	0x00
0xF4C6	FTM6 dead time register	FT6DTL	FT6DT	R/W	8/16	0x00
0xF4C7		FT6DTH		R/W	8	0x00
0xF4C8	FTM6 counter register	FT6CL	FT6C	R/W	8/16	0x00
0xF4C9		FT6CH		R/W	8	0x00
0xF4CA	FTM6 status register	FT6STAT	-	R	8	0x30
0xF4CB	Reserved	-	-	-	-	-
0xF4CC	FTM6 mode register	FT6MODL	FT6MOD	R/W	8/16	0x00
0xF4CD		FT6MODH		R/W	8	0x40
0xF4CE	FTM6 clock register	FT6CLKL	FT6CLK	R/W	8/16	0x00
0xF4CF		FT6CLKH		R/W	8	0x00
0xF4D0	FTM6 trigger register 0	FT6TRG0L	FT6TRG0	R/W	8/16	0x00
0xF4D1		FT6TRG0H		R/W	8	0x00
0xF4D2	FTM6 trigger register 1	FT6TRG1L	FT6TRG1	R/W	8/16	0x00
0xF4D3		FT6TRG1H		R/W	8	0x00
0xF4D4	FTM6 interrupt enable register	FT6INTEL	FT6INTE	R/W	8/16	0x00
0xF4D5		FT6INTEH		R/W	8	0x00
0xF4D6	FTM6 interrupt status register	FT6INTSL	FT6INTS	R	8/16	0x00
0xF4D7		FT6INTSH		R	8	0x00
0xF4D8	FTM6 interrupt clear register	FT6INTCL	FT6INTC	W	8/16	0x00
0xF4D9		FT6INTCH		W	8	0x00
0xF4DA to 0xF4DF	Reserved	-	-	-	-	-
0xF4E0	FTM7 cycle register	FT7PL	FT7P	R/W	8/16	0xFF
0xF4E1		FT7PH		R/W	8	0xFF
0xF4E2	FTM7 event A register	FT7EAL	FT7EA	R/W	8/16	0x00
0xF4E3		FT7EAH		R/W	8	0x00
0xF4E4	FTM7 event B register	FT7EBL	FT7EB	R/W	8/16	0x00
0xF4E5		FT7EBH		R/W	8	0x00
0xF4E6	FTM3 dead time register	FT7DTL	FT7DT	R/W	8/16	0x00
0xF4E7		FT7DTH		R/W	8	0x00
0xF4E8	FTM7 counter register	FT7CL	FT7C	R/W	8/16	0x00
0xF4E9		FT7CH		R/W	8	0x00
0xF4EA	FTM7 status register	FT7STAT	-	R	8	0x30
0xF4EB	Reserved	-	-	-	-	-
0xF4EC	FTM7 mode register	FT7MODL	FT7MOD	R/W	8/16	0x00
0xF4ED		FT7MODH		R/W	8	0x40
0xF4EE	FTM7 clock register	FT7CLKL	FT7CLK	R/W	8/16	0x00
0xF4EF		FT7CLKH		R/W	8	0x00
0xF4F0	FTM7 trigger register 0	FT7TRG0L	FT7TRG0	R/W	8/16	0x00
0xF4F1		FT7TRG0H		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF4F2	FTM7 trigger register 1	FT7TRG1L	FT7TRG1	R/W	8/16	0x00
0xF4F3		FT7TRG1H		R/W	8	0x00
0xF4F4	FTM7 interrupt enable register	FT7INTEL	FT7INTE	R/W	8/16	0x00
0xF4F5		FT7INTEH		R/W	8	0x00
0xF4F6	FTM7 interrupt status register	FT7INTSL	FT7INTS	R	8/16	0x00
0xF4F7		FT7INTSH		R	8	0x00
0xF4F8	FTM7 interrupt clear register	FT7INTCL	FT7INTC	W	8/16	0x00
0xF4F9		FT7INTCH		W	8	0x00
0xF4FA to 0xF4FF	Reserved	-	-	-	-	-
0xF500	Serial port 0 transmission/reception buffer	SIO0BUFL	SIO0BUF	R/W	8/16	0x00
0xF501		SIO0BUFH		R/W	8	0x00
0xF502	Serial port 0 status register	SIO0STATL	SIO0STAT	R	8/16	0x00
0xF503		SIO0STATH		W	8	0x00
0xF504	Serial port 0 control register	SIO0CONL	SIO0CON	R/W	8/16	0x00
0xF505		SIO0CONH		R/W	8	0x00
0xF506	Serial port 0 mode register	SIO0MODL	SIO0MOD	R/W	8/16	0x00
0xF507		SIO0MODH		R/W	8	0x00
0xF508	Serial port 0 interval setting register	SIO0DLYL	-	R/W	8	0x00
0xF509	Reserved	-	-	-	-	-
0xF50A	Serial port 0 interrupt control register	SIO0ICNL	-	R/W	8	0x00
0xF50B to 0xF50F	Reserved	-	-	-	-	-
0xF510	Serial port 1 transmission/reception buffer	SIO1BUFL	SIO1BUF	R/W	8/16	0x00
0xF511		SIO1BUFH		R/W	8	0x00
0xF512	Serial port 1 status register	SIO1STATL	SIO1STAT	R	8/16	0x00
0xF513		SIO1STATH		W	8	0x00
0xF514	Serial port 1 control register	SIO1CONL	SIO1CON	R/W	8/16	0x00
0xF515		SIO1CONH		R/W	8	0x00
0xF516	Serial port 1 mode register	SIO1MODL	SIO1MOD	R/W	8/16	0x00
0xF517		SIO1MODH		R/W	8	0x00
0xF518	Serial port 1 interval setting register	SIO1DLYL	-	R/W	8	0x00
0xF519	Reserved	-	-	-	-	-
0xF51A	Serial port 1 interrupt control register	SIO1ICNL	-	R/W	8	0x00
0xF51B to 0xF51F	Reserved	-	-	-	-	-
0xF520	Serial port 2 transmission/reception buffer	SIO2BUFL	SIO2BUF	R/W	8/16	0x00
0xF521		SIO2BUFH		R/W	8	0x00
0xF522	Serial port 2 status register	SIO2STATL	SIO2STAT	R	8/16	0x00
0xF523		SIO2STATH		W	8	0x00
0xF524	Serial port 2 control register	SIO2CONL	SIO2CON	R/W	8/16	0x00
0xF525		SIO2CONH		R/W	8	0x00
0xF526	Serial port 2 mode register	SIO2MODL	SIO2MOD	R/W	8/16	0x00
0xF527		SIO2MODH		R/W	8	0x00
0xF528	Serial port 2 interval setting register	SIO2DLYL	-	R/W	8	0x00
0xF529	Reserved	-	-	-	-	-
0xF52A	Serial port 2 interrupt control register	SIO2ICNL	-	R/W	8	0x00
0xF52B to 0xF52F	Reserved	-	-	-	-	-
0xF530	Extended serial port 0 transmission/reception buffer	ESIO0BUFL	ESIO0BUF	R/W	8/16	0x00
0xF531		ESIO0BUFH		R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF532	Extended serial port 0 status register	ESIO0STATL	ESIO0STAT	R	8/16	0x00
0xF533		ESIO0STATH		W	8	0x00
0xF534	Extended serial port 0 control register	ESIO0CONL	ESIO0CON	R/W	8/16	0x00
0xF535		ESIO0CONH		R/W	8	0x00
0xF536	Extended serial port 0 mode register	ESIO0MODL	ESIO0MOD	R/W	8/16	0x00
0xF537		ESIO0MODH		R/W	8	0x00
0xF538	Extended serial port 0 interval setting register	ESIO0DLYL	-	R/W	8	0x00
0xF539	Reserved	-	-	-	-	-
0xF53A	Extended serial port 0 interrupt control register	ESIO0ICNL	-	R/W	8	0x00
0xF53B to 0xF53F	Reserved	-	-	-	-	-
0xF540	Extended serial port 1 transmission/reception buffer	ESIO1BUFL	ESIO1BUF	R/W	8/16	0x00
0xF541		ESIO1BUFH		R/W	8	0x00
0xF542	Extended serial port 1 status register	ESIO1STATL	ESIO1STAT	R	8/16	0x00
0xF543		ESIO1STATH		W	8	0x00
0xF544	Extended serial port 1 control register	ESIO1CONL	ESIO1CON	R/W	8/16	0x00
0xF545		ESIO1CONH		R/W	8	0x00
0xF546	Extended serial port 1 mode register	ESIO1MODL	ESIO1MOD	R/W	8/16	0x00
0xF547		ESIO1MODH		R/W	8	0x00
0xF548	Extended serial port 1 interval setting register	ESIO1DLYL	-	R/W	8	0x00
0xF549	Reserved	-	-	-	-	-
0xF54A	Extended serial port 1 interrupt control register	ESIO1ICNL	-	R/W	8	0x00
0xF54B to 0xF54F	Reserved	-	-	-	-	-
0xF550	Extended serial port 2 transmission/reception buffer	ESIO2BUFL	ESIO2BUF	R/W	8/16	0x00
0xF551		ESIO2BUFH		R/W	8	0x00
0xF552	Extended serial port 2 status register	ESIO2STATL	ESIO2STAT	R	8/16	0x00
0xF553		ESIO2STATH		W	8	0x00
0xF554	Extended serial port 2 control register	ESIO2CONL	ESIO2CON	R/W	8/16	0x00
0xF555		ESIO2CONH		R/W	8	0x00
0xF556	Extended serial port 2 mode register	ESIO2MODL	ESIO2MOD	R/W	8/16	0x00
0xF557		ESIO2MODH		R/W	8	0x00
0xF558	Extended serial port 2 interval setting register	ESIO2DLYL	-	R/W	8	0x00
0xF559	Reserved	-	-	-	-	-
0xF55A	Extended serial port 2 interrupt control register	ESIO2ICNL	-	R/W	8	0x00
0xF55B to 0xF57F	Reserved	-	-	-	-	-
0xF580	SIOF0 control register	SF0CTRLL	SF0CTRL	R/W	8/16	0x00
0xF581		SF0CTRLH		R/W	8	0x00
0xF582	SIOF0 interrupt control register	SF0INTCL	SF0INTC	R/W	8/16	0x00
0xF583		SF0INTCH		R/W	8	0x00
0xF584	SIOF0 transfer interval control register	-	SF0TRAC	R/W	16	0x0002
0xF585		-				
0xF586	SIOF0 baud rate register	-	SF0BRR	R/W	16	0x5002
0xF587		-				
0xF588	SIOF0 status register	SF0SRRL	SF0SRR	R	8/16	0x00
0xF589		SF0SRRH		R	8	0x14
0xF58A	SIOF0 status clear register (L/H)	SF0SRCL	-	W	8	0x00
0xF58B		SF0SRCH	-	W	8	0x00
0xF58C	SIOF0 FIFO status register	SF0FSRL	SF0FSR	R	8/16	0x00
0xF58D		SF0FSRH		R	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF58E	SIOF0 writing data register	SF0DWRL	SF0DWR	R/W	8/16	0x00
0xF58F		SF0DWRH		R/W	8	0x00
0xF590	SIOF0 reading data register	SF0DRRL	SF0DRR	R	8/16	0x00
0xF591		SF0DRRH		R	8	0x00
0xF592 to 0xF5DF	Reserved	-	-	-	-	-
0xF5E0	Extended Serial Port interrupt status register	ESISTAT	-	R	8	0x00
0xF5E1	Reserved	-	-	-	-	-
0xF5E2	Extended Serial Port Interrupt Clear register	ESINTCL	ESINTC	W	8/16	0x00
0xF5E3		ESINTCH	-	W	8	0x00
0xF5E4 to 0xF5FF	Reserved	-	-	-	-	-
0xF600	UART0 reception buffer	UA0BUF0	-	R	8	0x00
0xF601	UART0 transmission buffer	UA0BUF1		R/W	8	0x00
0xF602	UART0 status register	UA0STAT	-	R	8	0x00
0xF603	UART0 status clear register	UA0STAC		W	8	0x00
0xF604	UART0 control register	UA0CON	-	R/W	8	0x00
0xF605	Reserved	-	-	-	-	-
0xF606	UART0 mode register	UA0MODL	UA0MOD	R/W	8/16	0x00
0xF607		UA0MODH		R/W	8	0x00
0xF608	UART0 interrupt enable register	UA0INTE	-	R/W	8	0x00
0xF609	Reserved	-	-	-	-	-
0xF60A	UART0 baud rate register	UA0BRTL	UA0BRT	R/W	8/16	0xFF
0xF60B		UA0BRTH		R/W	8	0x0F
0xF60C	UART0 baud rate adjustment register	UA0BRC	-	R/W	8	0x00
0xF60D to 0xF60F	Reserved	-	-	-	-	-
0xF610	UART1 reception buffer	UA1BUF0	-	R	8	0x00
0xF611	UART1 transmission buffer	UA1BUF1	-	R/W	8	0x00
0xF612	UART1 status register	UA1STAT	-	R	8	0x00
0xF613	UART1 status clear register	UA1STAC	-	W	8	0x00
0xF614	UART1 control register	UA1CON	-	R/W	8	0x00
0xF615	Reserved	-	-	-	-	-
0xF616	UART1 mode register	UA1MODL	UA1MOD	R/W	8/16	0x00
0xF617		UA1MODH		R/W	8	0x00
0xF618	UART1 interrupt enable register	UA1INTE	-	R/W	8	0x00
0xF619	Reserved	-	-	-	-	-
0xF61A	UART1 status register	UA1BRTL	UA1BRT	R/W	8/16	0xFF
0xF61B		UA1BRTH		R/W	8	0x0F
0xF61C	UART1 status clear register	UA1BRC	-	R/W	8	0x00
0xF61D to 0xF61F	Reserved	-	-	-	-	-
0xF620	UART2 reception buffer	UA2BUF0	-	R	8	0x00
0xF621	UART2 transmission buffer	UA2BUF1	-	R/W	8	0x00
0xF622	UART2 status register	UA2STAT	-	R	8	0x00
0xF623	UART2 status clear register	UA2STAC	-	W	8	0x00
0xF624	UART2 control register	UA2CON	-	R/W	8	0x00
0xF625	Reserved	-	-	-	-	-
0xF626	UART2 mode register	UA2MODL	UA2MOD	R/W	8/16	0x00
0xF627		UA2MODH		R/W	8	0x00
0xF628	UART2 interrupt enable register	UA2INTE	-	R/W	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF629	Reserved	-	-	-	-	-
0xF62A	UART2 baud rate register	UA2BRTL	UA2BRT	R/W	8/16	0xFF
0xF62B		UA2BRTH		R/W	8	0x0F
0xF62C	UART2 baud rate adjustment register	UA2BRC	-	R/W	8	0x00
0xF62D to 0xF62F	Reserved	-	-	-	-	-
0xF630	Extended UART0 reception buffer	EUA0BUF0	-	R	8	0x00
0xF631	Extended UART0 transmission buffer	EUA0BUF1	-	R/W	8	0x00
0xF632	Extended UART0 status register	EUA0STAT	-	R	8	0x00
0xF633	Extended UART0 status clear register	EUA0STAC	-	W	8	0x00
0xF634	Extended UART0 control register	EUA0CON	-	R/W	8	0x00
0xF635	Reserved	-	-	-	-	-
0xF636	Extended UART0 mode register	EUA0MODL	EUA0MOD	R/W	8/16	0x00
0xF637		EUA0MODH		R/W	8	0x00
0xF638	Extended UART0 interrupt enable register	EUA0INTE	-	R/W	8	0x00
0xF639	Reserved	-	-	-	-	-
0xF63A	Extended UART0 baud rate register	EUA0BRTL	EUA0BRT	R/W	8/16	0xFF
0xF63B		EUA0BRTH		R/W	8	0x0F
0xF63C	Extended UART0 baud rate adjustment register	EUA0BRC	-	R/W	8	0x00
0xF63D to 0xF63F	Reserved	-	-	-	-	-
0xF640	Extended UART1 reception buffer	EUA1BUF0	-	R	8	0x00
0xF641	Extended UART1 transmission buffer	EUA1BUF1	-	R/W	8	0x00
0xF642	Extended UART1 status register	EUA1STAT	-	R	8	0x00
0xF643	Extended UART1 status clear register	EUA1STAC	-	W	8	0x00
0xF644	Extended UART1 control register	EUA1CON	-	R/W	8	0x00
0xF645	Reserved	-	-	-	-	-
0xF646	Extended UART1 mode register	EUA1MODL	EUA1MOD	R/W	8/16	0x00
0xF647		EUA1MODH		R/W	8	0x00
0xF648	Extended UART1 interrupt enable register	EUA1INTE	-	R/W	8	0x00
0xF649	Reserved	-	-	-	-	-
0xF64A	Extended UART1 baud rate register	EUA1BRTL	EUA1BRT	R/W	8/16	0xFF
0xF64B		EUA1BRTH		R/W	8	0x0F
0xF64C	Extended UART1 baud rate adjustment register	EUA1BRC	-	R/W	8	0x00
0xF64D to 0xF64F	Reserved	-	-	-	-	-
0xF650	Extended UART2 reception buffer	EUA2BUF0	-	R	8	0x00
0xF651	Extended UART2 transmission buffer	EUA2BUF1	-	R/W	8	0x00
0xF652	Extended UART2 status register	EUA2STAT	-	R	8	0x00
0xF653	Extended UART2 status clear register	EUA2STAC	-	W	8	0x00
0xF654	Extended UART2 control register	EUA2CON	-	R/W	8	0x00
0xF655	Reserved	-	-	-	-	-
0xF656	Extended UART2 mode register	EUA2MODL	EUA2MOD	R/W	8/16	0x00
0xF657		EUA2MODH		R/W	8	0x00
0xF658	Extended UART2 interrupt enable register	EUA2INTE	-	R/W	8	0x00
0xF659	Reserved	-	-	-	-	-
0xF65A	Extended UART2 baud rate register	EUA2BRTL	EUA2BRT	R/W	8/16	0xFF
0xF65B		EUA2BRTH		R/W	8	0x0F
0xF65C	Extended UART2 baud rate adjustment register	EUA2BRC	-	R/W	8	0x00
0xF65D to 0xF67F	Reserved	-	-	-	-	-

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF680	Extended UART interrupt status register	EUISTAT	-	R	8/16	0x00
0xF681	Reserved	-	-	-	-	-
0xF682	Extended UART interrupt clear register	EUINTCL	EUINTC	W	8/16	0x00
0xF683		EUINTCH		W	8	0x00
0xF684 to 0xF79F	Reserved	-	-	-	-	-
0xF780	I²C bus unit 0 mode register	I2U0MSS	-	R/W	8	0x00
0xF781	Reserved	-	-	-	-	-
0xF782	I²C bus unit 0 receive register	I2U0RD	-	R	8	0x00
0xF783	Reserved	-	-	-	-	-
0xF784	I²C bus unit 0 slave address register	I2U0SA	-	R/W	8	0x00
0xF785	Reserved	-	-	-	-	-
0xF786	I²C bus unit 0 transmit data register	I2U0TD	-	R/W	8	0x00
0xF787	Reserved	-	-	-	-	-
0xF788	I²C bus unit 0 control register	I2U0CON	-	R/W	8	0x00
0xF789	Reserved	-	-	-	-	-
0xF78A	I²C bus unit 0 mode register	I2U0MODL	I2U0MOD	R/W	8/16	0x00
0xF78B		I2U0MODH		R/W	8	0x02
0xF78C	I²C bus unit 0 status register	I2U0STAT	I2U0STR	R	8/16	0x00
0xF78D		I2U0ISR		R	8	0x00
0xF78E	I²C bus unit 0 status clear register	I2U0SCLRL	I2U0SCLR	W	8/16	0x00
0xF78F		I2U0SCLRH		W	8	0x00
0xF790 to 0xF7C1	Reserved	-	-	-	-	-
0xF7C2	I²C bus master 0 receive register	I2M0RD	-	R	8	0x00
0xF7C3	Reserved	-	-	-	-	-
0xF7C4	I²C bus master 0 slave address register	I2M0SA	-	R/W	8	0x00
0xF7C5	Reserved	-	-	-	-	-
0xF7C6	I²C bus master 0 transmit data register	I2M0TD	-	R/W	8	0x00
0xF7C7	Reserved	-	-	-	-	-
0xF7C8	I²C bus master 0 control register	I2M0CON	-	R/W	8	0x00
0xF7C9	Reserved	-	-	-	-	-
0xF7CA	I²C bus master 0 mode register	I2M0MODL	I2M0MOD	R/W	8/16	0x00
0xF7CB		I2M0MODH		R/W	8	0x02
0xF7CC	I²C bus master 0 status register	I2M0STAT	I2M0STR	R	8/16	0x00
0xF7CD		I2M0ISR		R	8	0x00
0xF7CE	I²C bus master 0 status clear register	I2M0SCLRL	I2M0SCLR	W	8/16	0x00
0xF7CF		I2M0SCLRH		W	8	0x00
0xF7D0	Reserved	-	-	-	-	-
0xF7D1	Reserved	-	-	-	-	-
0xF7D2	I²C bus master 1 receive register	I2M1RD	-	R	8	0x00
0xF7D3	Reserved	-	-	-	-	-
0xF7D4	I²C bus master 1 slave address register	I2M1SA	-	R/W	8	0x00
0xF7D5	Reserved	-	-	-	-	-
0xF7D6	I²C bus master 1 transmit data register	I2M1TD	-	R/W	8	0x00
0xF7D7	Reserved	-	-	-	-	-
0xF7D8	I²C bus master 1 control register	I2M1CON	-	R/W	8	0x00
0xF7D9	Reserved	-	-	-	-	-
0xF7DA	I²C bus master 1 mode register	I2M1MODL	I2M1MOD	R/W	8/16	0x00
0xF7DB		I2M1MODH		R/W	8	0x02

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF7DC	I^2C bus master 1 status register	I2M1STAT	I2M1STR	R	8/16	0x00
0xF7DD		I2M1ISR		R	8	0x00
0xF7DE	I^2C bus master 1 status clear register	I2M1SCLRL	I2M1SCLR	W	8/16	0x00
0xF7DF		I2M1SCLRH		W	8	0x00
0xF7E0 to 0xF7FF	Reserved	-	-	-	-	-
0xF800	SA-ADC mode register	SADMODL	SADMOD	R/W	8/16	0x00
0xF801		SADMODH		R/W	8	0x00
0xF802	SA-ADC control register	SADCONL	SADCON	R/W	8/16	0x00
0xF803		SADCONH		R/W	8	0x00
0xF804	SA-ADC conversion interval register	SADSTML	SADSTM	R/W	8/16	0x00
0xF805		SADSTMH		R/W	8	0x00
0xF806	Reference voltage control register	VREFCON	-	R/W	8	0x00
0xF807	Reserved	-	-	-	-	-
0xF808	SA-ADC interrupt mode register	SADIMOD	-	R/W	8	0x00
0xF809	Reserved	-	-	-	-	-
0xF80A	SA-ADC trigger register	SADTRG	-	R/W	8	0x00
0xF80B	Reserved	-	-	-	-	-
0xF80C	SA-ADC enable register 0	SADEN0L	SADEN0	R/W	8/16	0x00
0xF80D		SADEN0H		R/W	8	0x00
0xF80E	SA-ADC enable register 1	SADEN1L	SADEN1	R/W	8/16	0x00
0xF80F		SADEN1H		R/W	8	0x00
0xF810 to 0xF81F	Reserved	-	-	-	-	-
0xF820	SA-ADC upper/lower limit mode register	SADLMODL	SADLMOD	R/W	8/16	0x00
0xF821		SADLMODH		R/W	8	0x00
0xF822	SA-ADC upper limit setting register	SADUPLL	SADUPL	R/W	8/16	0xF0
0xF823		SADUPLH		R/W	8	0xFF
0xF824	SA-ADC lower limit setting register	SADLOLL	SADLOL	R/W	8/16	0x00
0xF825		SADLOLH		R/W	8	0x00
0xF826	SA-ADC upper/lower limit status register 0	SADULS0L	SADULS0	R	8/16	0x00
0xF827		SADULS0H		R	8	0x00
0xF828	Reserved	-	-	-	-	-
0xF829	Reserved	-	-	-	-	-
0xF82A	SA-ADC upper/lower limit status clear register 0	SADULC0L	SADULC0	W	8/16	0x00
0xF82B		SADULC0H		W	8	0x00
0xF82C to 0xF82F	Reserved	-	-	-	-	-
0xF830	SA-ADC test mode register	SADTMOD	-	R/W	8	0x00
0xF831 to 0xF83D	Reserved	-	-	-	-	-
0xF83E	SA-ADC result register	SADRL	SADR	R	8/16	0x00
0xF83F		SADRH		R	8	0x00
0xF840	SA-ADC result register 0	SADR0L	SADR0	R	8/16	0x00
0xF841		SADR0H		R	8	0x00
0xF842	SA-ADC result register 1	SADR1L	SADR1	R	8/16	0x00
0xF843		SADR1H		R	8	0x00
0xF844	SA-ADC result register 2	SADR2L	SADR2	R	8/16	0x00
0xF845		SADR2H		R	8	0x00
0xF846	SA-ADC result register 3	SADR3L	SADR3	R	8/16	0x00
0xF847		SADR3H		R	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF848	SA-ADC result register 4	SADR4L	SADR4	R	8/16	0x00
0xF849		SADR4H		R	8	0x00
0xF84A	SA-ADC result register 5	SADR5L	SADR5	R	8/16	0x00
0xF84B		SADR5H		R	8	0x00
0xF84C	SA-ADC result register 6	SADR6L	SADR6	R	8/16	0x00
0xF84D		SADR6H		R	8	0x00
0xF84E	SA-ADC result register 7	SADR7L	SADR7	R	8/16	0x00
0xF84F		SADR7H		R	8	0x00
0xF850	SA-ADC result register 8	SADR8L	SADR8	R	8/16	0x00
0xF851		SADR8H		R	8	0x00
0xF852	SA-ADC result register 9	SADR9L	SADR9	R	8/16	0x00
0xF853		SADR9H		R	8	0x00
0xF854	SA-ADC result register 10	SADR10L	SADR10	R	8/16	0x00
0xF855		SADR10H		R	8	0x00
0xF856	SA-ADC result register 11	SADR11L	SADR11	R	8/16	0x00
0xF857		SADR11H		R	8	0x00
0xF858	SA-ADC result register 12	SADR12L	SADR12	R	8/16	0x00
0xF859		SADR12H		R	8	0x00
0xF85A	SA-ADC result register 13	SADR13L	SADR13	R	8/16	0x00
0xF85B		SADR13H		R	8	0x00
0xF85C	SA-ADC result register 14	SADR14L	SADR14	R	8/16	0x00
0xF85D		SADR14H		R	8	0x00
0xF85E	SA-ADC result register 15	SADR15L	SADR15	R	8/16	0x00
0xF85F		SADR15H		R	8	0x00
0xF860 to 0xF88F	Reserved	-	-	-	-	-
0xF890	Voltage level supervisor 0 control register	VLS0CON	-	R/W	8	0x00
0xF891	Reserved	-	-	-	-	-
0xF892	Voltage level supervisor 0 mode register	VLS0MOD	-	R/W	8	0x00
0xF893	Reserved	-	-	-	-	-
0xF894	Voltage level supervisor 0 level register	VLS0LV	-	R/W	8	0x0E
0xF895	Reserved	-	-	-	-	-
0xF896	Voltage level supervisor 0 sampling register	VLS0SMP	-	R/W	8	0x00
0xF897 to 0xF91F	Reserved	-	-	-	-	-
0xF920	Code Option 0	CODEOP0L	CODEOP0	R	8/16	*1
0xF921		CODEOP0H		R	8	*1
0xF922	Code Option 1	CODEOP1L	CODEOP1	R	8/16	*1
0xF923		CODEOP1H		R	8	*1
0xF924	Code Option 2	CODEOP2L	CODEOP2	R	8/16	*1
0xF925		CODEOP2H		R	8	*1
0xF926 ~0xF92F	Reserved	-	-	-	-	-
0xF930	Product ID register 0	PID0L	PID0	R	8/16	*2
0xF931		PID0H		R	8	*2
0xF932	Product ID register 1	PID1L	PID1	R	8/16	0x22
0xF933		PID1H		R	8	0x06
0xF934 to 0xF93F	Reserved	-	-	-	-	-
0xF940	Converting Base Data register L	CNVBD0	CNVBDL	R/W	8/16	Undefined
0xF941		CNVBD1		R/W	8	Undefined

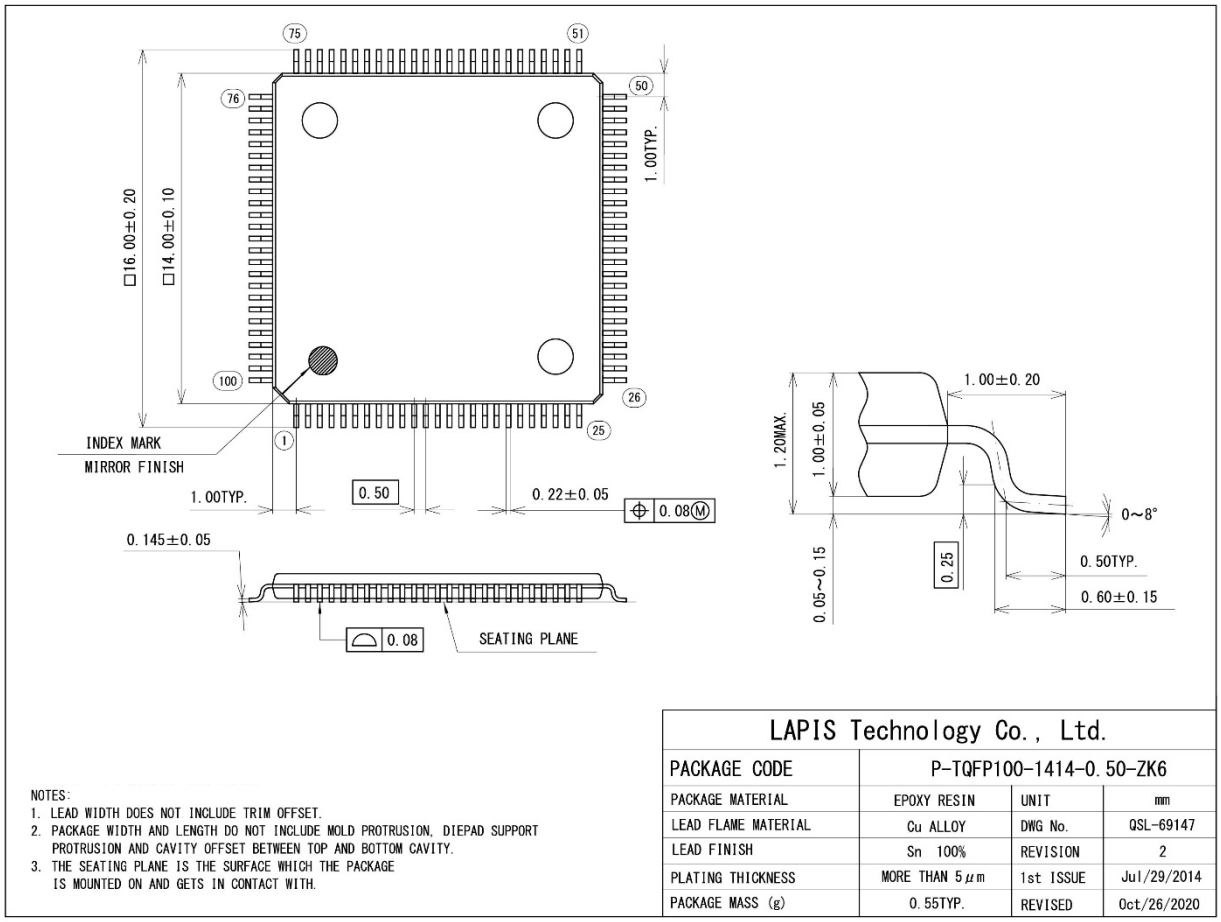
Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xF942	Converting Base Data register H	CNVBD2	CNVBDH	R/W	8/16	Undefined
0xF943		CNVBD3		R/W	8	Undefined
0xF944	Bit Swap Result register L	CNVAD0	CNVADL	R	8/16	Undefined
0xF945		CNVAD1		R	8	Undefined
0xF946	Bit Swap Result register H	CNVAD2	CNVADH	R	8/16	Undefined
0xF947		CNVAD3		R	8	Undefined
0xF948	Byte Swap Result register L	CNVED0	CNVEDL	R	8/16	Undefined
0xF949		CNVED1		R	8	Undefined
0xF94A	Byte Swap Result register H	CNVED2	CNVEDH	R	8/16	Undefined
0xF94B		CNVED3		R	8	Undefined
0xF94C to 0xF9FF	Reserved	-	-	-	-	-
0xFA00	Audio data start address register L	STAADRL0	STAADRML0	R/W	8/16	0x00
0xFA01	Audio data start address register M	STAADRM0		R/W	8	0x00
0xFA02	Audio data start address register H	STAADRH0	STAADRHH0	R/W	8/16	0x00
0xFA03	Reserved	-	-	-	-	-
0xFA04	Audio data stop address register L	STPADRL0	STPADRML0	R/W	8/16	0XFF
0xFA05	Audio data stop address register M	STPADRM0		R/W	8	0XFF
0xFA06	Audio data stop address register H	STPADRH0	STPADRHH0	R/W	8/16	0XFF
0xFA07	Reserved	-	-	-	-	-
0xFA08	Event management start address register L	STAADRL1	STAADRML1	R/W	8/16	0x00
0xFA09	Event management start address register M	STAADRM1		R/W	8	0x00
0xFA0A	Event management start address register H	STAADRH1	STAADRHH1	R/W	8/16	0x00
0xFA0B	Reserved	-	-	-	-	-
0xFA0C	Event management stop address register L	STPADRL1	STPADRML1	R/W	8/16	0XFF
0xFA0D	Event management stop address register M	STPADRM1		R/W	8	0XFF
0xFA0E	Event management stop address register H	STPADRH1	STPADRHH1	R/W	8/16	0XFF
0xFA0F	Reserved	-	-	-	-	-
0xFA10	Edit data start address register L	STAADRL2	STAADRML2	R/W	8/16	0x00
0xFA11	Edit data start address register M	STAADRM2		R/W	8	0x00
0xFA12	Edit data start address register H	STAADRH2	STAADRHH2	R/W	8/16	0x00
0xFA13	Reserved	-	-	-	-	-
0xFA14	Edit data stop address register L	STPADRL2	STPADRML2	R/W	8/16	0XFF
0xFA15	Edit data stop address register M	STPADRM2		R/W	8	0XFF
0xFA16	Edit data stop address register H	STPADRH2	STPADRHH2	R/W	8/16	0XFF
0xFA17	Reserved	-	-	-	-	-
0xFA18	Audio playback mode register	VEXMOD	-	R/W	8	0x00
0xFA19	Reserved	-	-	-	-	-
0xFA1A	Audio read request register	VEXCNT	VEXCONT	R/W	8/16	0x00
0xFA1B	Audio read stop register	VEXSTP	-	W	8	0x00
0xFA1C	Audio data read interrupt threshold setting register	VEXAE	-	R/W	8	0x00
0xFA1D	Reserved	-	-	-	-	-
0xFA1E	Audio interrupt enable register	VEXIE	-	R/W	8	0x10
0xFA1F	Reserved	-	-	-	-	-
0xFA20	Audio interrupt request status register	VEXSTAT	-	R	8	0x00
0xFA21	Reserved	-	-	-	-	-
0xFA22	Audio interrupt request clear register L	VEXSTATCLL	VEXSTATCL	W	8/16	0x00
0xFA23	Audio interrupt request clear register H	VEXSTATCLH		W	8	0x00
0xFA24	Audio data read address counter register L	ADRCNTL0	ADRCNTML0	R	8/16	0x00
0xFA25	Audio data read address counter register M	ADRCNTM0		R	8	0x00

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xFA26	Audio data read address counter register H	ADRCNTH0	ADRCNTHH0	R	8/16	0x00
0xFA27	Reserved	-	-	-	-	-
0xFA28	Audio data playback stop address register L	CSTPADRL0	ADRCNTML0	R	8/16	0x00
0xFA29	Audio data playback stop address register M	CSTPADRM0	CSTPADRML0	R	8	0x00
0xFA2A	Audio data playback stop address register H	CSTPADRH0	CSTPADRHH0	R	8/16	0x00
0xFA2B	Reserved	-	-	-	-	-
0xFA2C to 0xFA2F	Reserved	-	-	-	-	-
0xFA30	Audio data read storage register 0	CH0BUF0	CH0BUF10	R	8/16	0x00
0xFA31	Audio data read storage register 1	CH0BUF1		R	8	0x00
0xFA32	Audio data read storage register 2	CH0BUF2	CH0BUF32	R	8/16	0x00
0xFA33	Audio data read storage register 3	CH0BUF3		R	8	0x00
0xFA34	Audio data read storage register 4	CH0BUF4	CH0BUF54	R	8/16	0x00
0xFA35	Audio data read storage register 5	CH0BUF5		R	8	0x00
0xFA36	Audio data read storage register 6	CH0BUF6	CH0BUF76	R	8/16	0x00
0xFA37	Audio data read storage register 7	CH0BUF7		R	8	0x00
0xFA38	Event management read storage register 0	CH1BUF0	CH1BUF10	R	8/16	0x00
0xFA39	Event management read storage register 1	CH1BUF1		R	8	0x00
0xFA3A	Event management read storage register 2	CH1BUF2	CH1BUF32	R	8/16	0x00
0xFA3B	Event management read storage register 3	CH1BUF3		R	8	0x00
0xFA3C	Event management read storage register 4	CH1BUF4	CH1BUF54	R	8/16	0x00
0xFA3D	Event management read storage register 5	CH1BUF5		R	8	0x00
0xFA3E	Event management read storage register 6	CH1BUF6	CH1BUF76	R	8/16	0x00
0xFA3F	Event management read storage register 7	CH1BUF7		R	8	0x00
0xFA40	Edit data read storage register 0	CH2BUF0	CH2BUF10	R	8/16	0x00
0xFA41	Edit data read storage register 1	CH2BUF1		R	8	0x00
0xFA42	Edit data read storage register 2	CH2BUF2	CH2BUF32	R	8/16	0x00
0xFA43	Edit data read storage register 3	CH2BUF3		R	8	0x00
0xFA44	Edit data read storage register 4	CH2BUF4	CHBUF54	R	8/16	0x00
0xFA45	Edit data read storage register 5	CH2BUF5		R	8	0x00
0xFA46	Edit data read storage register 6	CH2BUF6	CH2BUF76	R	8/16	0x00
0xFA47	Edit data read storage register 7	CH2BUF7		R	8	0x00
0xFA48 to 0xFAAF	Reserved	-	-	-	-	-
0xFAB0	Audio FIFO data register	VFDAT	-	W	8	0x00
0xFAB1	Reserved	-	-	-	-	-
0xFAB2	Audio FIFO phrase end data register	VFEDAT	-	W	8	0x00
0xFAB3	Reserved	-	-	-	-	-
0xFAB4	Reserved	-	-	-	-	-
0xFAB5	Reserved	-	-	-	-	-
0xFAB6	Audio status register	VSTAT	-	R	8	0x11
0xFAB7	Reserved	-	-	-	-	-
0xFAB8	Audio mode register	VMOD	-	R/W	8	0x00
0xFAB9	Reserved	-	-	-	-	-
0xFABA	Audio data type register	VTYPE	-	R/W	8	0x41
0xFABB	Reserved	-	-	-	-	-
0xFABC	Volume setting register	VVOL	-	R/W	8	0x09
0xFABD	Reserved	-	-	-	-	-
0xFABE	Audio playback control register	VCON	-	R/W	8	0x00
0xFABF to 0xFAC7	Reserved	-	-	-	-	-

Address	Name	Symbol		R/W	Size	Initial value
		Byte	Word			
0xFAC8	Audio PWM control register	SPCON	-	R/W	8	0x00
0xFAC9 to 0xFACF	Reserved	-	-	-	-	-
0xFAD0	Volume status register	VVOLS	-	R	8	0x09
0xFAD1 to 0xFADF	Reserved	-	-	-	-	-
0xFAE0	Audio PWM fixed detection control register	SDCON	-	R/W	8	0x00
0xFAE1 to 0xFAE3	Reserved	-	-	-	-	-
0xFAE4	Audio PWMoutput waveform mode register	DSGMOD	-	R/W	8	0x02
0xFAE5 to 0xFFFF	Reserved	-	-	-	-	-

Appendix B Package Dimensions

100pin TQFP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

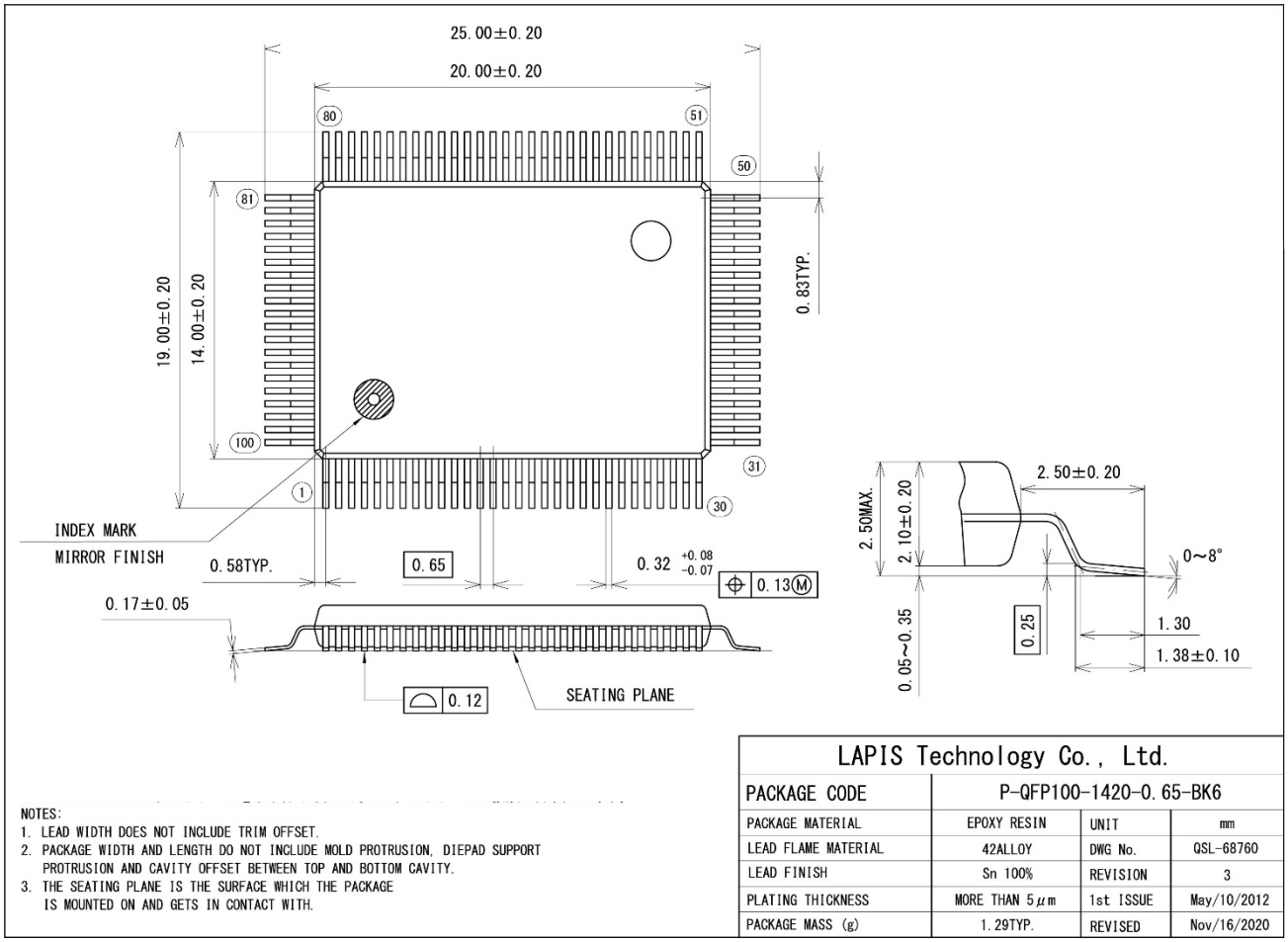
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP100-1414-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69147
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/29/2014
PACKAGE MASS (g)	0.55TYP.	REVISED	Oct/26/2020

(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

100pin QFP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

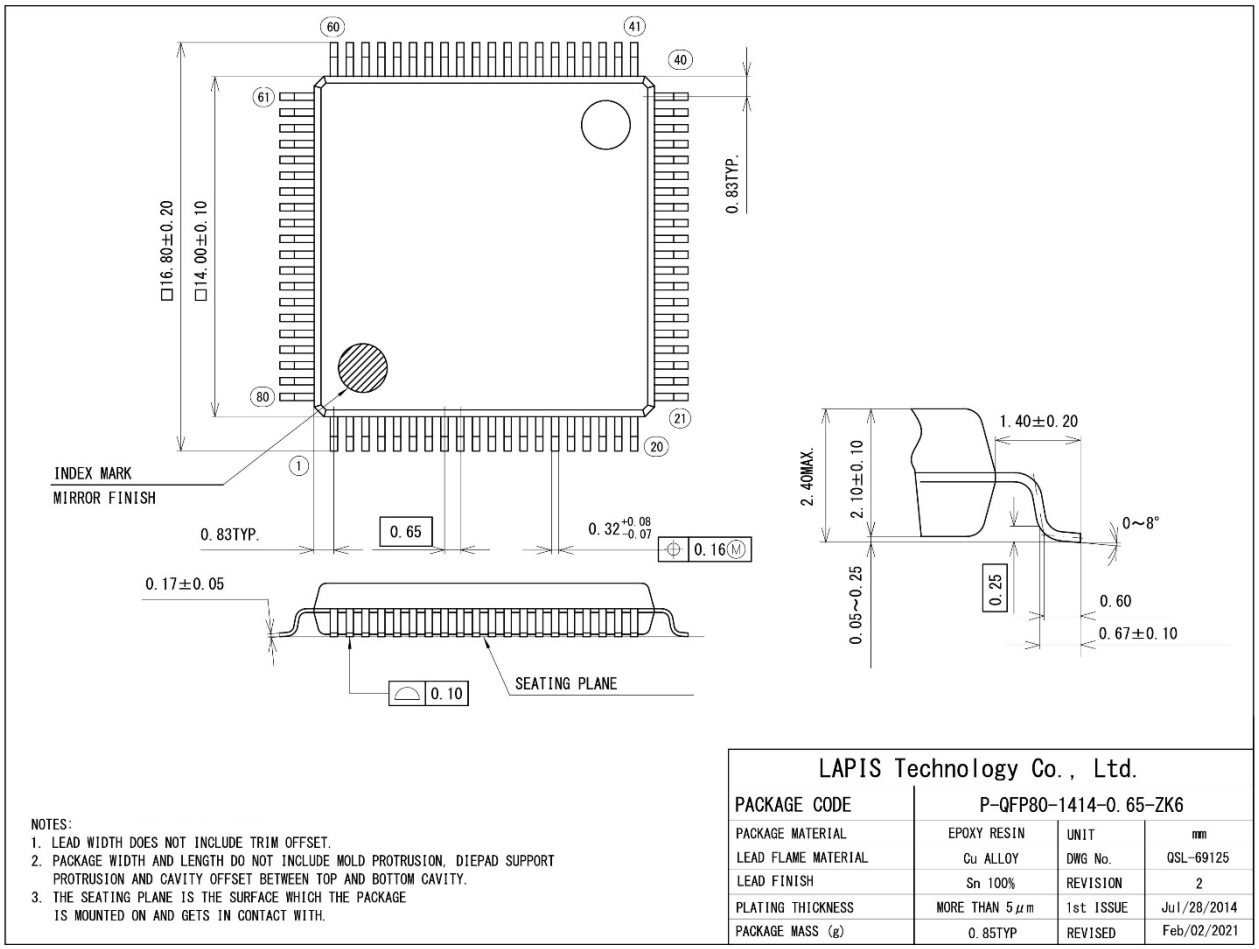
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-QFP100-1420-0.65-BK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	42ALLOY	DWG No.	QSL-68760
LEAD FINISH	Sn 100%	REVISION	3
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	May/10/2012
PACKAGE MASS (g)	1.29TYP.	REVISED	Nov/16/2020

(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

80pin QFP

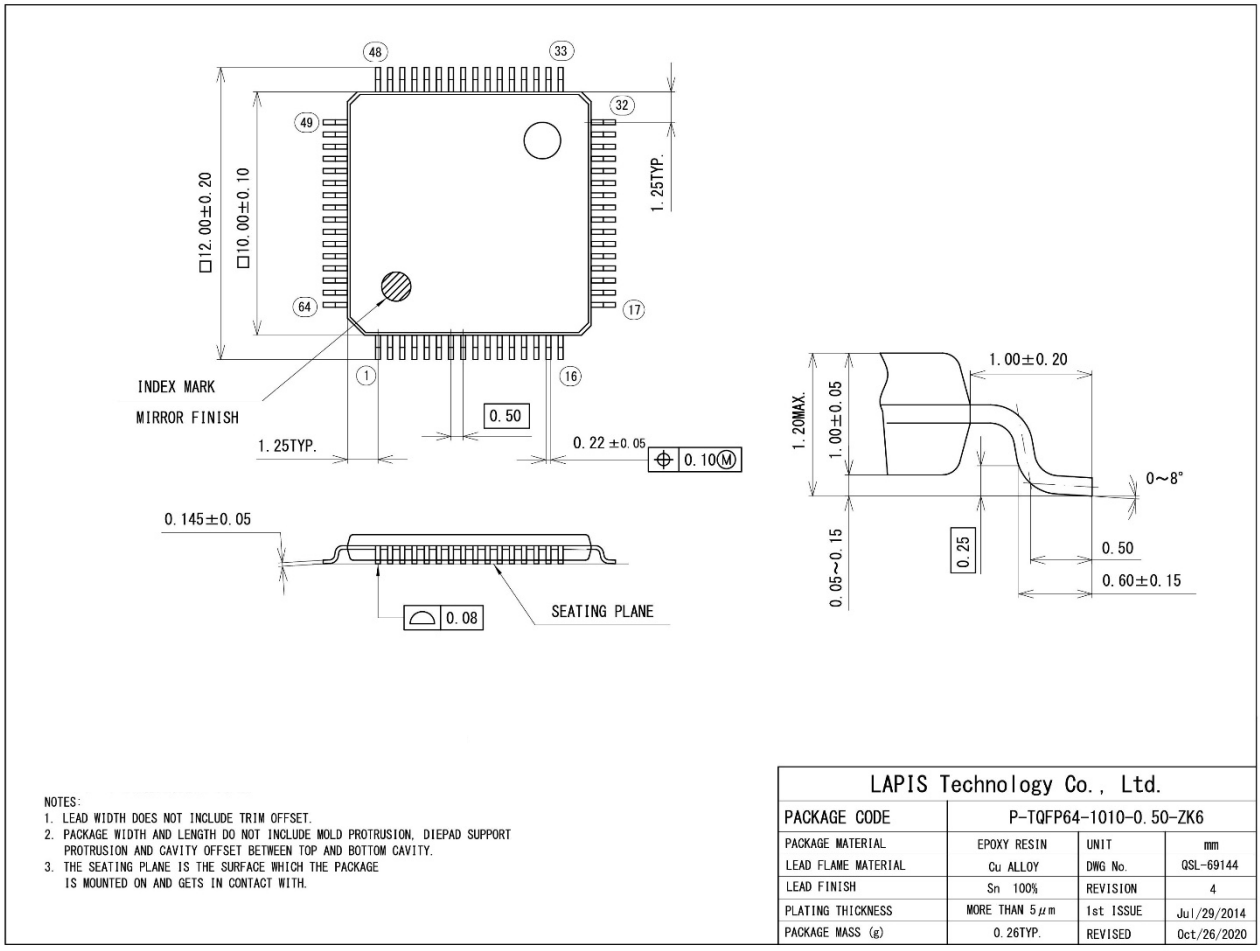


(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin TQFP

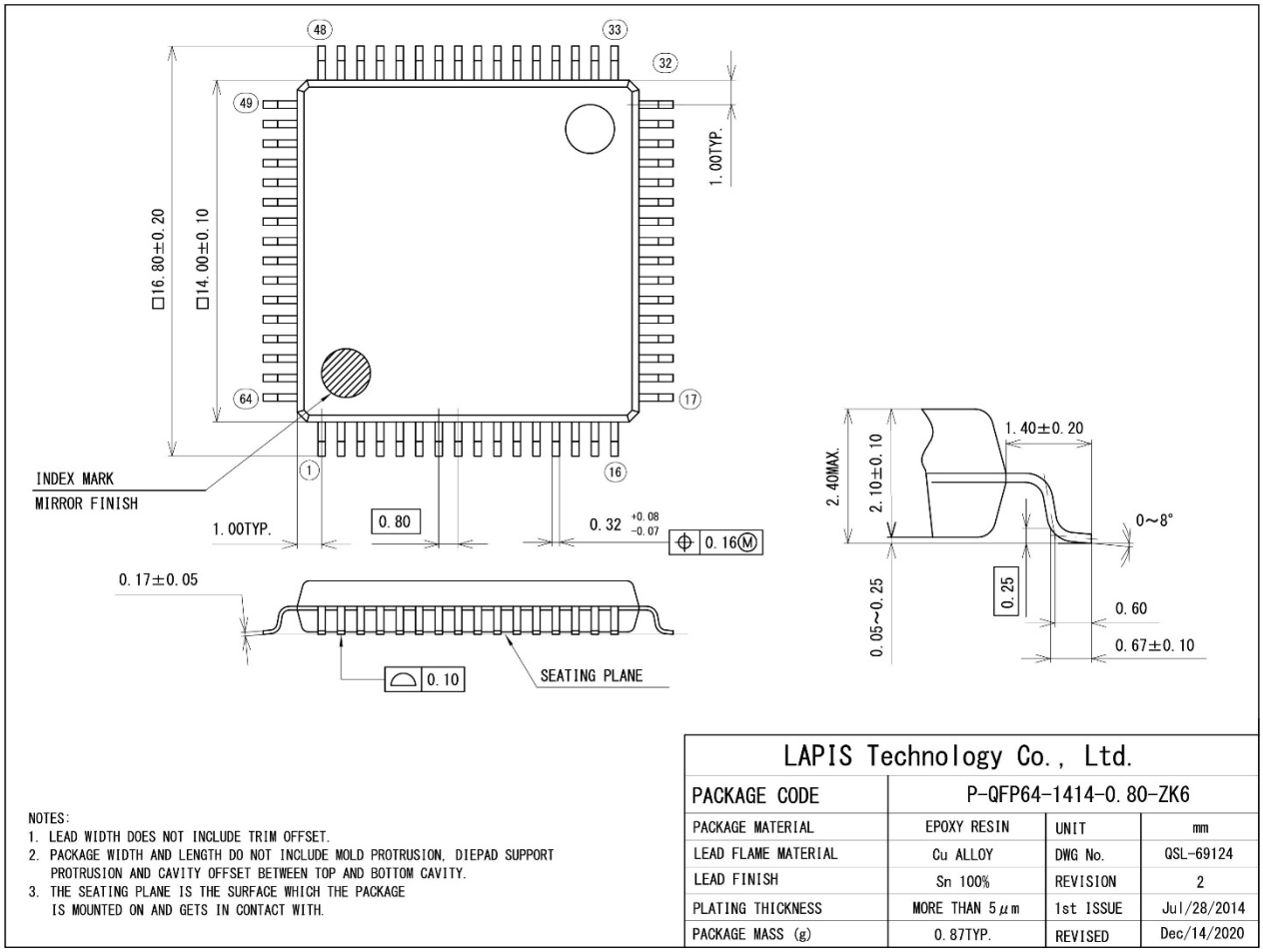


(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

64pin QFP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

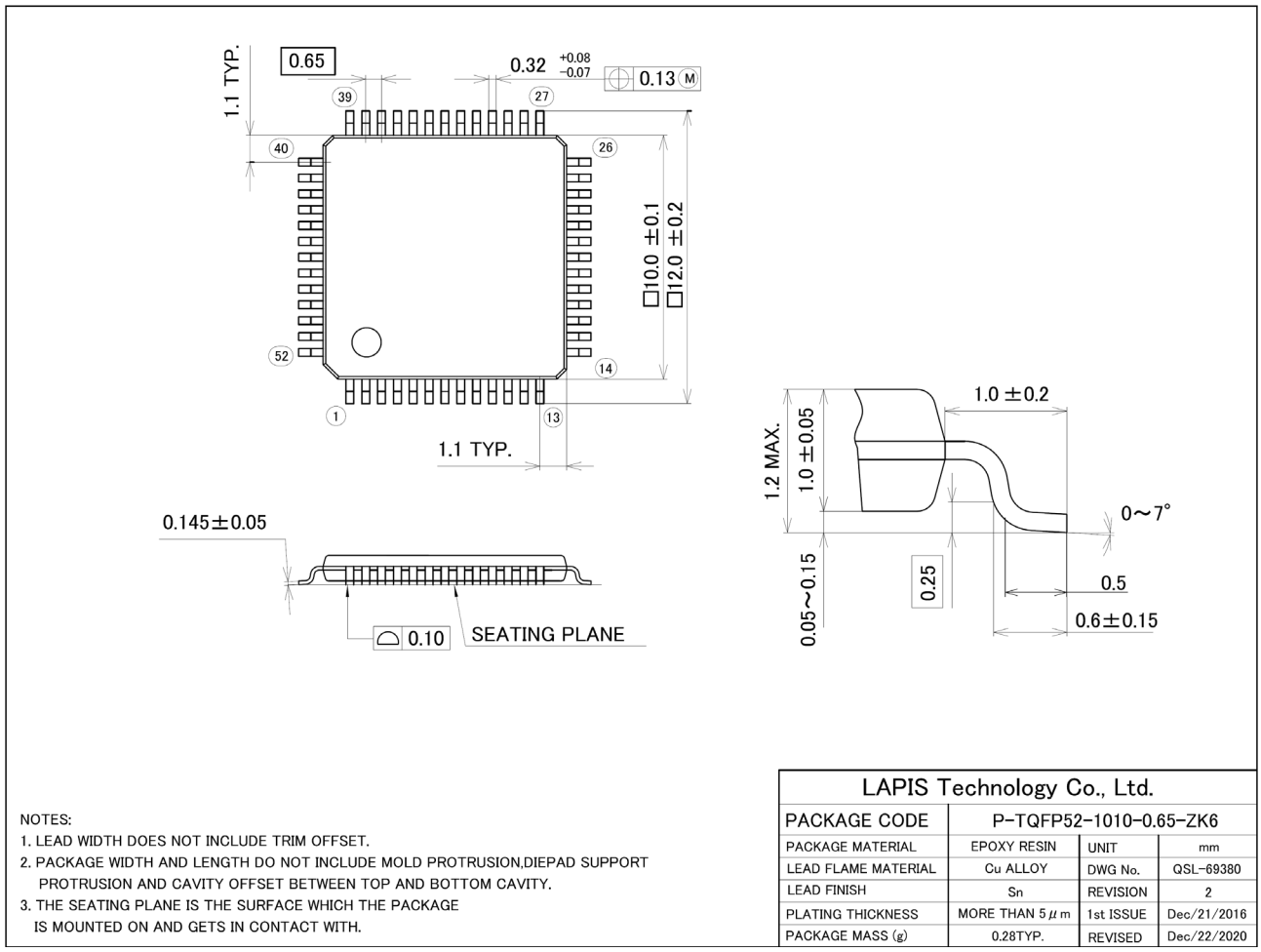
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-QFP64-1414-0.80-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69124
LEAD FINISH	Sn 100%	REVISION	2
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.87TYP.	REVISED	Dec/14/2020

(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

52pin TQFP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION,DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

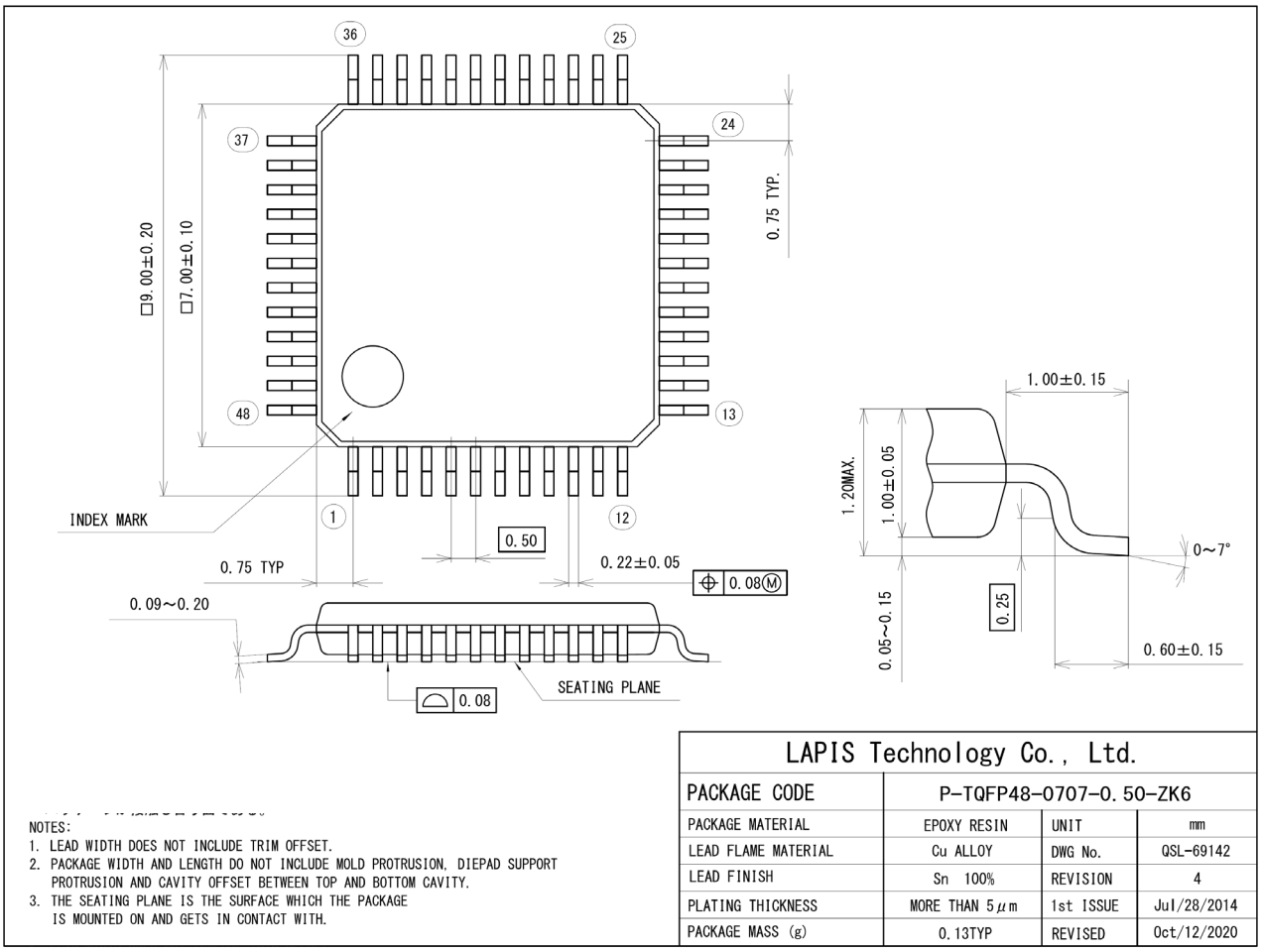
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP52-1010-0.65-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69380
LEAD FINISH	Sn	REVISION	2
PLATING THICKNESS	MORE THAN 5 μm	1st ISSUE	Dec/21/2016
PACKAGE MASS (g)	0.28TYP.	REVISED	Dec/22/2020

(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

48pin TQFP



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

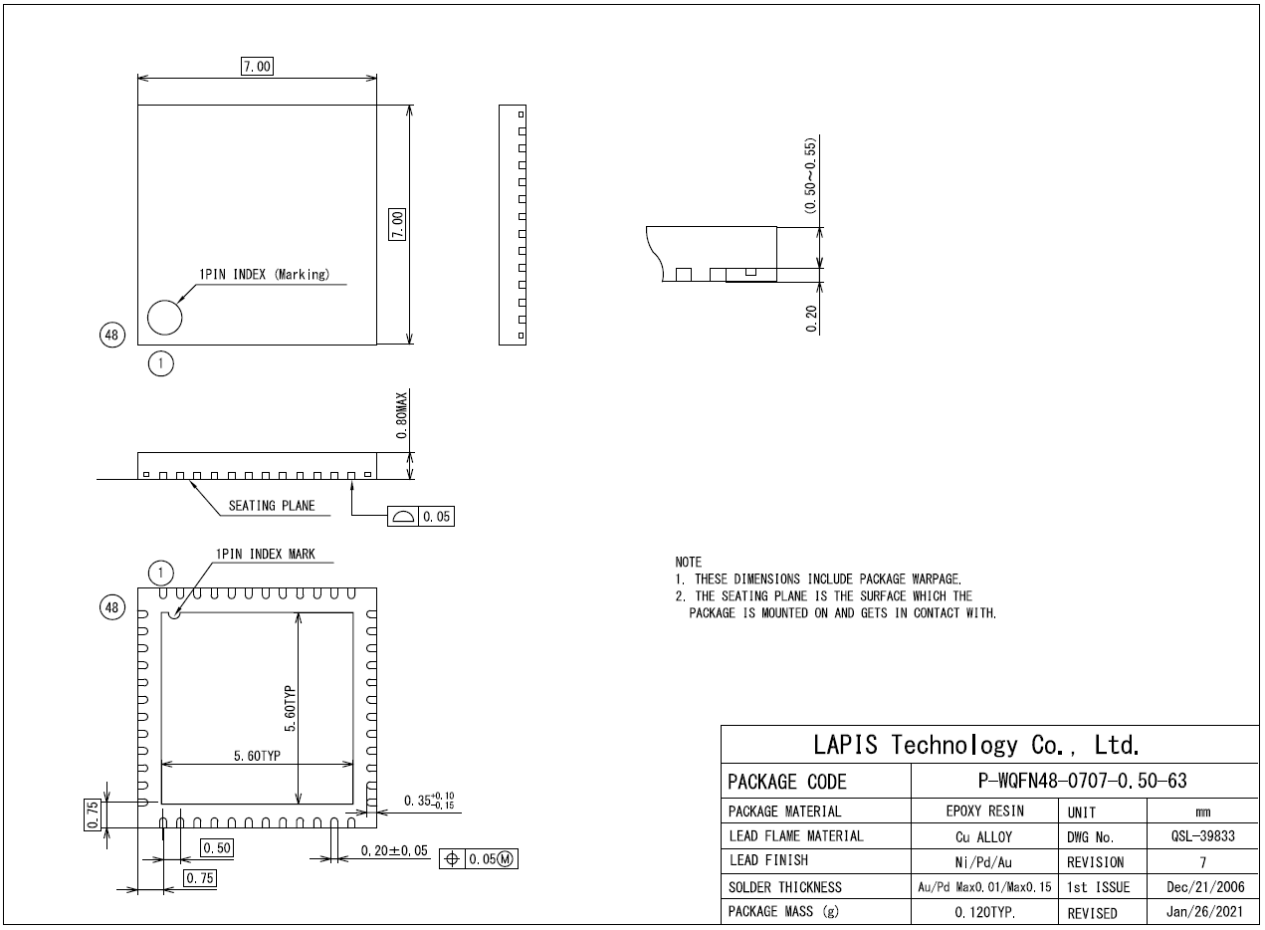
LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-ZK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69142
LEAD FINISH	Sn 100%	REVISION	4
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/28/2014
PACKAGE MASS (g)	0.13TYP	REVISED	Oct/12/2020

(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

48pin WQFN



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN48-0707-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-39833
LEAD FINISH	Ni/Pd/Au	REVISION	7
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Dec/21/2006
PACKAGE MASS (g)	0.120TYP.	REVISED	Jan/26/2021

(Unit : mm)

[Note] Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

[Note] Notes for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

Appendix C Instruction Execution Cycle

ML62Q2700 group has two CPU operating modes defined as the no wait mode and wait mode, in which there are some cases the instruction execution cycles are different each other.

CPU Operation Mode	Description
No wait mode	There is no increase of the instruction execution cycle, as there is no wait cycle for reading the program memory during the instruction execution.
Wait mode	There are some increases of the instruction execution cycle, as there are some wait cycles for reading the program memory during the instruction execution.

Tables on following pages show the all instructions of nX-U16/100 core and the execution cycles in the two CPU modes. "-" indicates that there is no memory access during the instruction execution. See "Example of Instruction execution cycle" for details on how to read the table.

Example of Instruction execution cycle

(1)			(2)-1	(2)-2	(3)-1	(3)-2	(4)	(5)
Instruction			Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
			No wait mode	Wait mode	No wait mode	Wait mode		
ADD	ERn	ERm	1	1	-	-	-	-
B	Cadr		2	6	-	-	-	1
	ERn		2	6	-	-	-	1
L	ERn	[EA]	1	1	1	5	1	-
		[EA+]	1	1	1	5	1	-

[How to read the table]

1) These are the instructions of nX-U16/100(A35 core)
2) The execution cycle of each instruction.
   The values in column (2)-1 are execution cycles in no wait mode.
   The values in column (2)-2 are execution cycles in wait mode.
3) Additional execution cycle when the instruction refers to ROM.
   The values in column (3)-1 are minimum cycles for reading when the instruction refers to ROM.
   The values in column (3)-2 are execution cycles that added waiting cycle into the values in (3)-1.
4) Additional execution cycle when the instruction reads the address allocated in segment 1 or larger.
   One cycle is added in spite of the CPU operating mode.
   For more details, see the section 1.3.4 "DSR Prefix Instructions" in the nX-U16/100 core instruction manual.
5) Additional execution effected by the instruction with the [EA+] addressing.
   One cycle is added in spite of the CPU operating mode.
   For more details, see the section 3.3 "Instruction Execution Times" in the nX-U16/100 core instruction manual.

Arithmetic Instructions

Instruction			Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
			No wait mode	Wait mode	No wait mode	Wait mode		
ADD	ERn	ERm	1	1	-	-	-	-
		#imm7	1	1	-	-	-	-
ADD	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
ADDC	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
AND	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
CMP	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
CMPC	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
MOV	ERn	ERm	1	1	-	-	-	-
		#imm7	1	1	-	-	-	-
MOV	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
OR	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
XOR	Rn	Rm	1	1	-	-	-	-
		#imm8	1	1	-	-	-	-
CMP	ERn	ERm	1	1	-	-	-	-
SUB	Rn	Rm	1	1	-	-	-	-
SUBC	Rn	Rm	1	1	-	-	-	-

Shift instructions

Instruction			Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
			No wait mode	Wait mode	No wait mode	Wait mode		
SLL	Rn	Rm	1	1	-	-	-	1
		#width	1	1	-	-	-	1
SLLC	Rn	Rm	1	1	-	-	-	1
		#width	1	1	-	-	-	1
SRA	Rn	Rm	1	1	-	-	-	1
		#width	1	1	-	-	-	1
SRL	Rn	Rm	1	1	-	-	-	1
		#width	1	1	-	-	-	1
SRLC	Rn	Rm	1	1	-	-	-	1
		#width	1	1	-	-	-	1

Load/Store instructions

Instruction			Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
			No wait mode	Wait mode	No wait mode	Wait mode		
L	ERn	[EA]	1	1	1	5	1	-
		[EA+]	1	1	1	5	1	-
		[ERm]	1	1 / 2 (*1)	1	5	1	1
		Disp16[ERm]	2	2	1	5	1	1
		Disp6[BP]	2	2	1	5	1	1
		Disp6[FP]	2	2	1	5	1	1
		Dadr	2	2	1	5	1	1
	Rn	[EA]	1	1	1	5	1	-
		[EA+]	1	1	1	5	1	-
		[ERm]	1	1 / 2 (*1)	1	5	1	1
		Disp16[ERm]	2	2	1	5	1	1
		Disp6[BP]	2	2	1	5	1	1
		Disp6[FP]	2	2	1	5	1	1
		Dadr	2	2	1	5	1	1
	XRn	[EA]	2	2	2	10	1	-
		[EA+]	2	2	2	10	1	-
	QRn	[EA]	4	4	4	15	1	-
		[EA+]	4	4	4	15	1	-
ST	ERn	[EA]	1	1	-	-	-	-
		[EA+]	1	1	-	-	-	-
		[ERm]	1	1 / 2 (*1)	-	-	-	1
		Disp16[ERm]	2	2	-	-	-	1
		Disp6[BP]	2	2	-	-	-	1
		Disp6[FP]	2	2	-	-	-	1
		Dadr	2	2	-	-	-	1
	Rn	[EA]	1	1	-	-	-	-
		[EA+]	1	1	-	-	-	-
		[ERm]	1	1 / 2 (*1)	-	-	-	1
		Disp16[ERm]	2	2	-	-	-	1
		Disp6[BP]	2	2	-	-	-	1
		Disp6[FP]	2	2	-	-	-	1
		Dadr	2	2	-	-	-	1
	XRn	[EA]	2	2	-	-	-	-
		[EA+]	2	2	-	-	-	-
	QRn	[EA]	4	4	-	-	-	-
		[EA+]	4	4	-	-	-	-

(*1) When the immediately preceding instruction is for reading the data memory or not (not the instruction for reading the data memory / the instruction for reading the data memory)

Control Register Access Instructions

Instruction			Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
			No wait mode	Wait mode	No wait mode	Wait mode		
ADD	SP	#signed8	1	1	-	-	-	-
MOV	ECSR	Rm	1	1	-	-	-	-
	ELR	ERm	1	1	-	-	-	-
	EPSW	Rm	1	1	-	-	-	-
	ERn	ELR	1	1	-	-	-	-
		SP	1	1	-	-	-	-
	PSW	Rm	1	1	-	-	-	-
		#unsigned8	1	1	-	-	-	-
	Rn	CRm	1	1	-	-	-	-
		ECSR	1	1	-	-	-	-
		EPSW	1	1	-	-	-	-
		PSW	1	1	-	-	-	-
	SP	ERm	1	1	-	-	-	-

PUSH/POP Instructions

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
PUSH	EA	1	1	-	-	-	1
	ELR	1 / 2 (*1)	1 / 2 (*1)	-	-	-	1
	EA,ELR	2 / 3 (*1)	2 / 3 (*1)	-	-	-	1
	EPSW	1	1	-	-	-	1
	EPSW,EA	2	2	-	-	-	1
	EPSW,ELR	2 / 3 (*1)	2 / 3 (*1)	-	-	-	1
	EPSW,ELR, EA	3 / 4 (*1)	3 / 4 (*1)	-	-	-	1
	LR	1 / 2 (*1)	1 / 2 (*1)	-	-	-	1
	LR,EA	2 / 3 (*1)	2 / 3 (*1)	-	-	-	1
	LR,ELR	2 / 4 (*1)	2 / 4 (*1)	-	-	-	1
	LR,EA,ELR	3 / 5 (*1)	3 / 5 (*1)	-	-	-	1
	LR,EPSW	2 / 3 (*1)	2 / 3 (*1)	-	-	-	1
	LR,EPSW,EA	3 / 4 (*1)	3 / 4 (*1)	-	-	-	1
	LR,EPSW,ELR	3 / 5 (*1)	3 / 5 (*1)	-	-	-	1
	LR,ELR,EPSW,EA	4 / 6 (*1)	4 / 6 (*1)	-	-	-	1
	ERn	1	1	-	-	-	1
	QRn	4	4	-	-	-	1
	Rn	1	1	-	-	-	1
	XRn	2	2	-	-	-	1
POP	EA	2	2	-	-	-	1
	EA,LR	3 / 4 (*1)	3 / 4 (*1)	-	-	-	1
	EA,PC	5 / 6 (*1)	10 / 11(*1)	-	-	-	1
	EA,PC,LR	6 / 8 (*1)	11 / 13 (*1)	-	-	-	1
	EA,PC,PSW	6 / 7 (*1)	11 / 13 (*1)	-	-	-	1
	EA,PC,PSW,LR	7 / 9 (*1)	12 / 14 (*1)	-	-	-	1
	EA,PSW	3	3	-	-	-	1
	EA,PSW,LR	4 / 5 (*1)	4 / 5 (*1)	-	-	-	1
	LR	1 / 2 (*1)	1 / 2 (*1)	-	-	-	1
	LR,PSW	2 / 3 (*1)	2 / 3 (*1)	-	-	-	1
	PC	3 / 4 (*1)	8 / 9 (*1)	-	-	-	1
	PC,LR	4 / 6 (*1)	9 / 11(*1)	-	-	-	1
	PC,PSW	4 / 5 (*1)	9 / 10 (*1)	-	-	-	1
	PC,PSW,LR	5 / 7 (*1)	10 / 12 (*1)	-	-	-	1
	PSW	1	1	-	-	-	1
	ERn	1	1	-	-	-	1
	QRn	4	4	-	-	-	1
	Rn	1	1	-	-	-	1
	XRn	2	2	-	-	-	1

(*1) When the memory mode is SMALL or LARGE (SMALL model/LARGE model)

Coprocessor Data Transfer Instructions

Instruction			Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
			No wait mode	Wait mode	No wait mode	Wait mode		
MOV	CRn	Rm	1	1	-	-	-	-
	CERn	[EA]	1	1	1	5	1	1
		[EA+]	1	1	1	5	1	1
	CQRn	[EA]	4	4	4	15	1	1
		[EA+]	4	4	4	15	1	1
	CRn	[EA]	1	1	1	5	1	1
		[EA+]	1	1	1	5	1	1
	CXRn	[EA]	2	2	2	10	1	1
		[EA+]	2	2	2	10	1	1
MOV	Rn	CRm	1	1	-	-	-	-
	[EA]	CERm	1	1	1	5	1	1
	[EA+]	CERm	1	1	1	5	1	1
	[EA]	CQRm	4	4	4	15	1	1
	[EA+]	CQRm	4	4	4	15	1	1
	[EA]	CRm	1	1	1	5	1	1
	[EA+]	CRm	1	1	1	5	1	1
	[EA]	CXRm	2	2	2	10	1	1
	[EA+]	CXRm	2	2	2	10	1	1

EA Register Data Transfer Instructions

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
LEA	[ERm]	1	1	-	-	-	-
	Disp16[ERm]	2	2	-	-	-	-
	Dadr	2	2	-	-	-	-

ALU Instructions

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
DAA	Rn	1	1	-	-	-	-
DAS	Rn	1	1	-	-	-	-
NEG	Rn	1	1	-	-	-	-

Bit Access Instructions

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
SB	Dbitadr	2	3	-	-	1	-
	Rn.bit_offset	1	1	-	-	-	-
RB	Dbitadr	2	3	-	-	1	-
	Rn.bit_offset	1	1	-	-	-	-
TB	Dbitadr	2	3	1	5	1	-
	Rn.bit_offset	1	1	-	-	-	-

PSW Access Instructions

Instruction	Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
	No wait mode	Wait mode	No wait mode	Wait mode		
EI	1	1	-	-	-	-
DI	3	3	-	-	-	-
SC	1	1	-	-	-	-
RC	1	1	-	-	-	-
CPLC	1	1	-	-	-	-

Sign Extension Instruction

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
EXTBW	ERn	1	1	-	-	-	-

Branch Instructions

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
B	Cadr	2	6	-	-	-	1
	ERn	2	6 / 7 (*1)	-	-	-	1
BL	Cadr	2	6	-	-	-	1
	ERn	2	6 / 7 (*1)	-	-	-	1

(*1) When the immediately preceding instruction is for reading the data memory or not (not the instruction for reading the data memory / the instruction for reading the data memory)

Conditional Relative Branch Instructions

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
BGE	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BLT	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BGT	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BLE	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BGES	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BLTS	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BGTS	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BLES	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BNE	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BEQ	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BNV	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BOV	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BPS	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BNS	Radr	1 / 2(*1)	1 / 7(*1)	-	-	-	1
BAL	Radr	2	7	-	-	-	1

(*1) When the branch condition is matched or not (Not matched / Matched)

Multiplication and Division Instructions

Instruction			Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
			No wait mode	Wait mode	No wait mode	Wait mode		
MUL	ERn	Rm	9	9	-	-	-	-
DIV	ERn	Rm	17	17	-	-	-	-

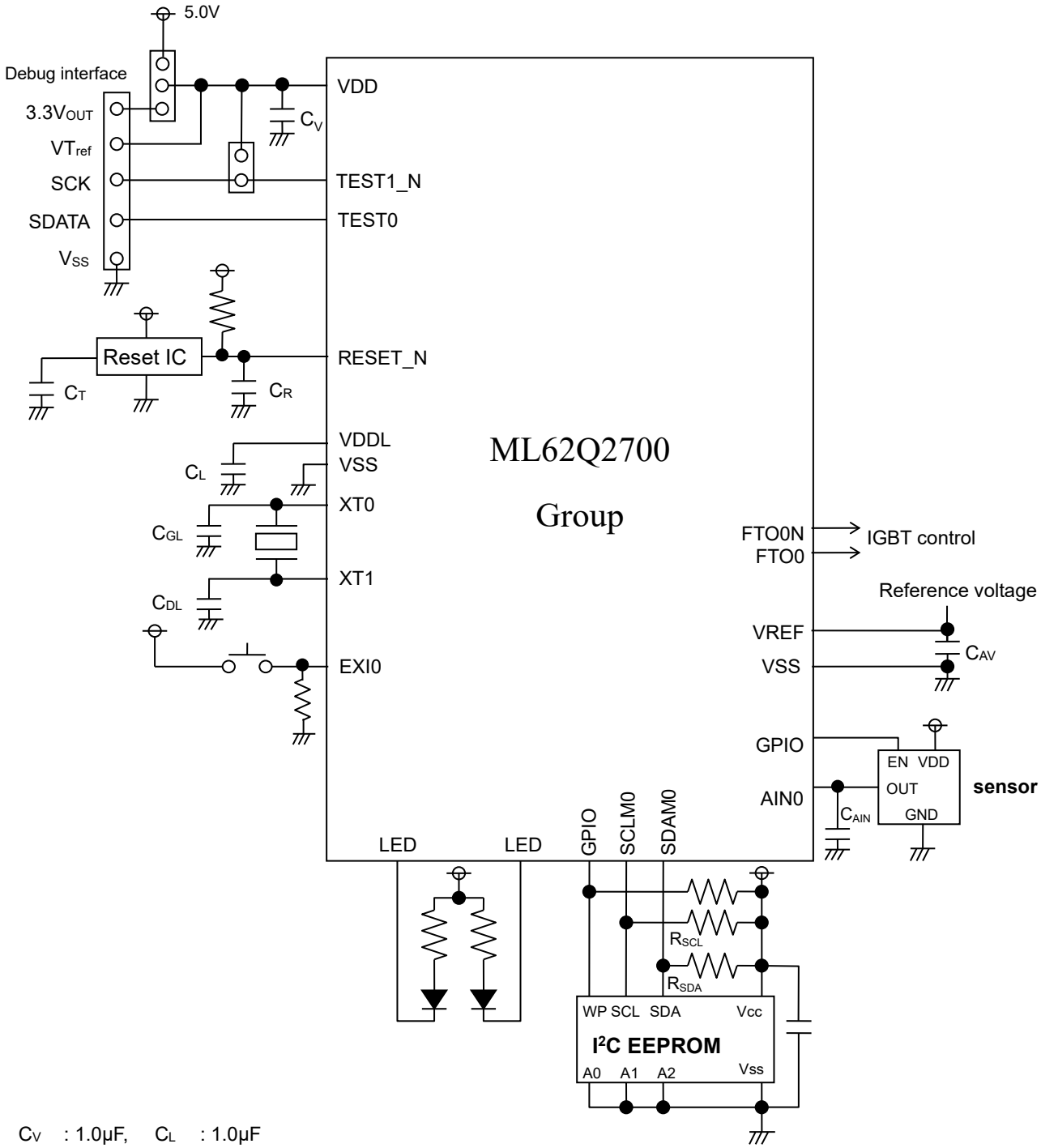
Interrupts

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
SWI	#snum	3	10	-	-	-	1
BRK		7	18	-	-	-	1
Interrupt transfer cycle		3	10	-	-	-	1

Miscellaneous

Instruction		Min. execution cycle		ROM reference cycle		Effect of DSR access	Effect of [EA+] addressing
		No wait mode	Wait mode	No wait mode	Wait mode		
NOP		1	1	-	-	-	-
DEC	[EA]	2	2	-	-	1	1
INC	[EA]	2	2	-	-	1	1
RT		2	6	-	-	1	1
RTI		2	6	-	-	1	1

Appendix D Application Circuit Example



C_V : 1.0µF, C_L : 1.0µF
C_{AV} : 1.0µF, C_{AIN} : 0.1µF
C_R : 0.1µF, C_T : 0.01µF
C_{GL}/C_{DL}: Determine after the matching evaluation.
R_{SCL}, R_{SDA} : 5kΩ or smaller

LED : P02~P07, P10~P17, P20~P27, P30~P37, P52~P57, P60~P62, P70~P73
Reset IC : BU4217 (ROHM, Nch open drain output)

[Note]

- **Place the capacitor for VDDL pin as close to the LSI power pins as possible.**

Appendix E List of Notes

This Check List has important notes to prevent commonly-made programming mistakes and frequently overlooked or misunderstood hardware specifications of the LSI. Check each note listed in chapter by chapter when coding or evaluating the program.
Number in a mark [ ] shows section number to refer.

Common to all Chapters

- □ Please see the "Notes" and the "Notes for product usage" in this document front pages.
- □ Word access is available for registers with the word symbol. Specify an even address for the word access. See "List of Registers" in each chapter.
- □ Registers for unequipped channels are not available to use. They return 0x0000 for reading. See "List of Registers" in each chapter.

1. Overview

- □ [1.3.4] Terminate unused input pins according to the table 1-5 in order to avoid unexpected through-current in the pins.

2. CPU and Memory Space

- □ [2.5] CSR[3] is unused on the ML62Q2700 group. The data of CSR "0x8 to 0xF" are handled as "0x0 to 0x7".
- □ [2.5] The Code Option area (64 bytes) is not available for the program code area. For details of Code Option settings, see Chapter 30 "Code Option" and make sure the setting data is correct.
- □ [2.5] It is recommended to fill unused areas with data "0xFFFF" (BRK instruction) in the program memory space to ensure failsafe using the generation tool of the ROM code data. See its manual for details on how to use. See "nX-U16/100 Core Instruction Manual" for details of the BRK instruction.
- □ [2.5, 2.6] Do not read or program unused areas to prevent the CPU works incorrectly.
- □ [2.6] The contents of the RAM area are undefined at power-on and system reset. Initialize this area by the software.
- □ [2.8.2] If the entire LSI is reset through a system reset, the remapping function is disabled as the REMAPADD register is restored with the initial value.

3. Reset Function

- □ [3.3.1] The BRK instruction reset only initializes the CPU if ELEVEL is 2 or higher. Peripheral circuits and other circuits are not initialized. Use the pin reset or the watchdog timer (WDT) reset to surely initialize the LSI when an abnormality is detected.
- □ [3.3.1] Command reset in on-chip debug does not reset to crystal oscillation circuit and VLS parts. Do initialization of these functions by writing SFRs on debug, if needed. See Chapter 28 for details.
- □ [3.3.2] In system reset mode, the contents of data memory (RAM) and SFRs that have an undefined initial value are not initialized. Initialize them by the software.
- □ [3.3.4] In case of instantaneous power failure and a pulse shorter than the power-on reset reaction time is asserted to VDD, MCU may not get reset and it may malfunction. In that case, please have preventive measures such as using bypass capacitor to avoid the instantaneous voltage drop or using pin reset to initialize MCU.

4. Power Management

- □ [4.1.3] In order to improve the noise resistance, place the inter-power supply bypass capacitor (C_V) and the internal logic voltage (V_{DDL}) capacitor (C_L : 1 μF) in the vicinity of LSI on the user board using the shortest possible wiring without passing through via holes.
- □ [4.1.3] The internal logic voltage (VDDL pin output) is unavailable to use for an external device voltage supply.
- □ [4.2.2] Writing to the stop code acceptor is invalid on the condition both interrupts enable bits and interrupt request bits are "1", it will not get enabled for entering to the STOP/STOP-D mode.
- □ [4.2.3] The operating state does not enter the standby mode under some conditions. See "4.3.2.6 Note of entering to the standby mode" for detail conditions.
- □ [4.2.3] When an interrupt enabled in the interrupt enable registers (IE0 to IE7) is generated on the condition of MIE flag of the program status word (PSW) is "0", it cancels the standby mode only and the CPU does not go to the interrupt routine. For more details about MIE flag, see "nX-U16/100 Core Instruction Manual".
- □ [4.2.3] Insert two NOP instructions in the next to the instruction of that sets HLT, STP, HLTH and STPD bit to "1". The operation without the two NOP instructions is not guaranteed.
- □ [4.2.6] Do not enter the standby mode when the SOFTR bit is "1". Ensure the SOFTR bit is "0" before entering the standby mode.
- □ [4.2.9, 4.2.13] Set DCKACC/RSEACC bit to "0" when the multiplication/division library "muldivu8.lib" in Development Support tools is specified. See a manual of the multiplication/division library for how to use.
- □ [4.3.2.6] Note of entering to the standby mode
- □ [4.3.2.7] Note on Return Operation from Standby Mode

- □ [4.3.2.7] Since up to two instructions are executed during the period between the release of standby mode and a transition to interrupt processing, place two NOP instructions next to the instruction set for the standby mode. When a master interrupt enable (MIE) flag of the program status word (PSW) in the nX-U16/100 CPU core is "1", following the execution of the two NOP instructions, the interrupt transition cycle will be executed and execution of the instruction for interrupt routine begins. If MIE is "0", following the execution of the two NOP instructions, the instruction execution is continued from the one that follows the NOP instruction without transition to the interrupt.
- □ [4.3.2.9] When the FHWUPT register is set to "0x01", the frequency of PLL oscillation clock gradually increases and reaches the target frequency chosen by the code option before approx. 2 ms elapse. The PLL oscillation clock during this time period can be used for the SYSCLK, however, accuracy of the frequency is not guaranteed.
- □ [4.3.3] If only the clock supply is stopped without resetting each peripheral circuit using the block control function, the output level of the pins is fixed, and excessive current may flow. In addition, unexpected current may keep flowing while SA-ADC operation is stopped.

5. Interrupts

- □ [5.2.6 ~ 5.2.9] There is a risk of clearing other request flags of This IRQ register, if writing to the specific bit of this register. Use the bit symbol to write to the specific bit. See Section [5.3.8 Writing to IRQ01/IRQ23/IRQ45/IRQ67] for more detail.
- □ [5.2.10] When disable the interrupt level control function, set the ILE bit to "0" after set the Interrupt level control register (ILC0 to ILC7) to "0x0000" and also after confirm the current interrupt request level register (CIL) is "0x00" in interrupt disabled state (IE01 to IE67 registers are "0x00").
- □ [5.2.10] When enabling the interrupt level control function, set the ILE bit to "1" when the permission flag for the interrupt in the interrupt permit register (IE01~IE67) is "0" or the master interrupt enable flag (MIE) is "0".
  If an interrupt is written when the permission flag of the interrupt in IE0~IE7 is "1" and the MIE is "1", an interrupt may occur at an unintended interrupt level.
- □ [5.2.13 ~ 5.2.20] Write to the register in the interrupt prohibited state (IE01~IE67 register="0000H" or the master interrupt enable flag (MIE) is "0"). If written in the interrupt authorization state (any bit of the IE01~IE67 register is "1" and the MIE is "1"), an interrupt may occur at an unintended interrupt level.
- □ [5.3] The WDT interrupt (WDTINT) is a non-maskable interrupt. If the non-maskable interrupt occurs while an interrupt processing is in progress, abort the interrupt processing and proceed with processing the non-maskable interrupt preferentially regardless of multiple interrupts enabled/disabled.
- □ [5.3] For failsafe, define unused all interrupt vectors. If an unused interrupt occurs, it may indicate the possibility that the CPU went out of control. It is recommended to cause the WDT overflow reset to occur using the infinite loop to initialize the LSI.
- □ [5.3.4] Notes on Interrupt Routine (with Interrupt Level Control Disabled)
- □ [5.3.4] Do not enable interrupts in a subroutine called from an interrupt routine for which multiple interrupts are disabled. Otherwise, the program may runaway when multiple interrupts occur.
- □ [5.3.5] For processing of non-maskable interrupt, follow the flow chart "In case of multiple interrupts are enabled". Registers that should be saved in the stack are ELR2 and EPSW2.
- □ [5.3.5] When programming in C, it is not required to write program codes for saving/restoring registers because they are generated in the C compiler. However, program codes for enabling/disabling interrupts through EI and DI instructions and for writing to the current interrupt level management register (CIL) must be written. See Section 5.3.6 "How To Write Interrupt Processing When Interrupt Level Control Enabled" for the specific program description.
- □ [5.3.6.1] Do not enable interrupts in a function called from a function for which multiple interrupts are disabled. Otherwise, the program may run out of control when the multiple interrupts occur.

6. Clock Generation Circuit

- □ [6.1.2] After the power-on or the system reset, LSCLK0 (32.768 kHz) is initially selected as SYSCLK.
- □ [6.1.3] Assign HCKO function to one LSI pin only.
- □ [6.3.1] The LCKO output operation is not guaranteed in the HALT-D mode.
- □ [6.3.1.2] Place the crystal resonator as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal and its wiring.
- □ [6.3.1.2] Note that oscillation may stop due to condensation.
- □ [6.3.1.2] When switching to the low speed crystal oscillation clock, ensure to use the interrupt referring to the Section 6.3.1.3 "Low-Speed Clock Control".
- □ [6.3.2.2] When the XT32K is used for LSCLK0, the high-speed clock may become an unintended frequency due to external factors such as noise, and the MCU may operates abnormally. Please evaluate enough the apparatus/system which implemented this product.
- □ [6.3.4] While the CPU is running with the low-speed clock, if running the peripheral circuits with the high-speed clock which can frequently generate interrupts, the operation may fail to function properly due to the CPU becoming incapable of processing interrupts in time. If interrupts frequently occur for reasons such as short interrupt cycles of peripheral circuits, take into account the operating frequency of the CPU so that it can process interrupts in time.

7. Low Speed Time Base Counter

- □ [7.2.2] A time base counter interrupt may occur depending on the timing to write to the LTBR01. See the program example for initializing described in Section 7.3.1 "Low Speed Time Base Counter Operation".
- □ [7.2.2] Read the LTBR01 register twice to verify the data to prevent reading uncertain data while counting-up.
- □ [7.2.3] Stop counter LTBR0 (i.e. set 0 to TB0RUN bit), before TB0CK bit is configured.
- □ [7.2.5] A time base counter interrupt may occur depending on a write timing to the LTBINT. See the program example for initializing described in 7.3.1 "Low Speed Time Base Counter Operation".
- □ [7.3.1] After writing to the LTBR01 register, the time by which the first low-speed time base counter interrupt request is generated is not guaranteed. If measuring the time using the low-speed time base counter interrupt, do so with reference to the interrupt generation interval.
- □ [7.3.2] The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the low-speed oscillation (32.768 kHz) due to temperature variations.

8. 16-bit Timer

- □ [8.2.2] Set TMHnD when the 16-bit timer n is stopped (THnSTATL bits of TMHSTAT register are "0"). If the register is changed during operation, the operation is not guaranteed.
- □ [8.2.2] When "0x0000" is written in TMHnD in the 16-bit timer mode, "0x0001" is set in TMHnD.
- □ [8.2.2] Set TMHnD so that the timer output frequency is 1MHz or less, when timer output is used.
- □ [8.2.3] Read the TMHnC register twice to verify the valid data to prevent reading uncertain data while counting-up, if a source of timer clock is as different as one of system clock.
- □ [8.2.4] Set TMHnMOD when the timer n is stopped (THnSTAT bits of TMHSTAT/TMHXSTAT register are "0"). If it is changed while it is operating, the operation is not guaranteed.
- □ [8.3.2] After the THnRUN bit is set to "1", the first interrupt has a time error equivalent to maximum of one clock of the timer clock because the counting operation starts in synchronization with the timer clock. The 2nd timer interrupt or later interrupts have constant cycles.
- □ [8.3.2] After the THnSTP bit is set to "1", a 16-bit timer n interrupt (TMnINT) may be generated depending on the stop timing because the counting operation stops in synchronization with the timer clock.

9. Functional Timer

- □ [9.2.2] When 0x0000 is written in this register, 0x0001 is set and the read value is also becomes 0x0001.
- □ [9.2.2] Set FTnP so that the functional timer output frequency is 3MHz or less, when its output is used.
- □ [9.2.3, 9.2.4] In timer mode , a data set in the FTnEA/FTnEB register must be less than that set in the FTnP register.
- □ [9.2.3] In PWM1/2 mode, a data set in the FTnEA register must be 0xFFFF or less than that set in the FTnP register.
- □ [9.2.4] In PWM1 mode, a data set in the FTnEB register must be 0xFFFF or less than that set in the FTnP register.
- □ [9.2.5] In the PWM2 mode, the data set in the FTnDT register must be less than that set in the FTnEA register.
- □ [9.2.5] In the PWM2 mode, the sum of setting data in the FTnDT register and the FTnEA register must be less than that set in the FTnP register.
- □ [9.2.6] Read FTnC register twice to verify the data to prevent reading uncertain data while counting-up according to need.
- □ [9.2.8] Set the FTnMOD register when the FTMn is stopped.
- □ [9.2.8] When switching modes after operating once, initialize this peripheral circuit by block reset.
- □ [9.2.10] The input pulse width must have two timer clocks or longer if FTnSTSS=0.
- □ [9.2.10] The counter forcibly stops and does not run when the emergency stop trigger source is the same as the trigger event source with the FTnETG = 1 and FTnEMGEN = 1.
- □ [9.2.11] If a level setting is chosen for the condition of the counter start and condition is matched, the count operation continues (restart the count-up from 0) even if a stop condition is satisfied in the one-shot mode.
- □ [9.2.11] The trigger may occur immediately after setting the FTnTRG1 register in the trigger event enabled.

10. Watchdog Timer

- □ [10.1.1] There is a limit to the abnormal operation that the watchdog timer can detect. Even if the CPU goes out of control, the watchdog timer is undetectable to the abnormality in the operation state in which the WDT counter is cleared.
- □ [10.1.1] As fail safe, WDT counter clear at one place in the main loop of the program is recommended.
- □ [10.2.2] In the WDT interrupt routine (when the interrupt level (ELEVEL) of the CPU program status word (PSW) is "2"), the WDT counter is unable to get cleared.
- □ [10.2.3] See ML62Q2700 data sheet for accuracy of WDTCLK .
- □ [10.3.1] In the STOP/STOP-D mode, the WDT timer is stopped.
- □ [10.3.3] When using the window function enabled mode, always define a WDT interrupt function even though no WDT interrupt occurs. For providing the fail-safe, it is recommended to generate the WDT invalid clear reset by forcibly clearing the WDT in the WDT interrupt function.
- □ [10.3.3] In the watchdog timer (WDT) interrupt function, as the interrupt level (ELEVEL) of the CPU program status word (PSW) becomes "2", the WDT counter is unable to get cleared. Clear the WDT when the ELEVEL is "0" or "1". It is recommended that the WDT counter is cleared at one place in the main loop of the program as a fail-safe.

11. Synchronous Serial Port

- □ [11.2.5] Set the SIOnMOD register while communication is stopped (SnEN=0). If it is rewritten during communication, data may not be transmitted or received normally.
- □ [11.2.11] Set ESIOnMOD register while communication is stopped (ESnEN=0). If it is rewritten during communication, data may not be transmitted or received normally.
- □ [11.2.15] Do not set ESIR bit with the ESI2C to ESI0C bit simultaneously.
- □ [11.2.15] When the CPU writes to the interrupt request register (IRQ01, IRQ23, IRQ45, IRQ67) at the timing of the extended external interrupt occurs, the extended serial port interrupt status register (ESISTAT) is set, but the interrupt request bit of the extended serial port interrupt (bit 2 of the QESIO = IRQ67 register) is not set and the CPU may not be notified of the interrupt..
- □ [11.2.15] When writing to IRQ01, IRQ23, IRQ45, and IRQ67, set the ESIR bit of ESINTC to 1 after writing and re-request the interrupt.
- □ [11.2.15] Refer to the Fig 11-12 for Extended serial port interrupt setting flow..
- □ [11.3.3] To prevent an overrun error after the first reception, read the SIOnBUF register before setting the SnEN bit to "1".

12. Synchronous Serial Port with FIFO

- □ [12.2.5] The maximum transfer frequency of SIOF is 4MHz, so set it so that it does not exceed 4MHz..
- □ [12.2.7] Write "1" to SF0IRQ bit while there is any unprocessed interrupt source and processing all the interrupt sources before exiting the interrupt vector will cause re-entry to the interrupt vector with no interrupt source after exiting the interrupt vector. Ensure to write "1" before exiting the interrupt vector.

13. I^2C Bus

- □ [13.1.4] Connect appropriate External pull-up resistors to SDAU0 pin, SCLU0, SDAMn, and SCLMn1 pins according to the I2C bus specification. The internal pull-up resistors does not meet the I2C bus specification. See the data sheet for the value of internal pull-up resistors..
- □ [13.1.4, 13.2.2] If power off this LSI during slave mode is in use, it disables communications of other devices on the I2C bus. Keep this LSI powered on while it works as a slave mode until the master device is powered off..
- □ [13.1.4, 13.2.2] Do not connect multiple master devices on the I2C bus when using the master function.
- □ [13.2.2] All SFRs are shared in master mode and slave mode. If switching master/slave mode, stop the operation by setting "0" to I2U0EN bit of I2UMOD register, then change the mode and reconfigure each SFRs.
- □ [13.2.2] When using the master function, do not connect multiple master devices on the I2C bus.
- □ [13.2.2] If power of this LSI is cut off during slave mode is in use, it disables communications of other devices on the I2C bus. Keep this LSI powered on while it works as a slave mode until the master device is powered off.
- □ [13.3.4] Update I2U0ACT/I2MnACT without bit access instructions in the control register setting wait state.
- □ [13.3.4] When the I2U0ST/I2M0ST bit is "1", write other bits of I2U0CON/I2M0CON register in the control register setting wait state.
- □ [13.4.4] If system clock is extremely slower than the communication speed, the data transmission/reception may not be succeeded.
- □ [13.4.4] Before releasing the communication wait state, set the system clock speed to appropriate speed for the communication.
- □ [13.4.5] In case if disabling the waking up from STOP mode/STOP-D mode/HALT-D mode by slave address matching, stop operation by setting I2U0EN to "0" before switching to STOP mode/STOP-D mode/HALT-D mode.
- □ [13.5.4] When the slave device uses the clock stretch function which holds the SCLU0 pin at "L" level, the time t_{CYC} and time t_{LOW} are extended.
- □ [13.6.2] If entering to the STOP/STOP-D mode while the slave mode is enabled, first make sure that communication is not in progress (from coincidence of address to reception of stop condition).
- □ [13.6.4] The master device should Wait for the SYSCLK to be supplied in order to transmit the start condition after wakeup from the STOP-D/HALT-D mode by slave address matching.
- □ [13.6.4] It is supported the Standard/Fast mode (to max. 400 kbps) in the STOP-D／HALT-D mode.

14.UART

- □ [14.2.1] When the DCKUAn of Block control register 2 (BCKCON2) is "1", the SFR readout value of the corresponding channel is "0x00/0x0000". However, the settings themselves are retained. When DCKUAn is set back to "0", the SFR readout value is the set value. For information about block control registers, see Chapter 4 Power Management .
- □ [14.2.6] Set the mode/baud rate of the pin and UART before setting the UnEN bit to "1".
- □ [14.2.7] Set UAnMOD register while communication is stopped, and do not rewrite it while communicating.
- □ [14.2.9, 14.2.10] Set UAnBRC register while communication is stopped, and do not rewrite it while communicating.
- □ [14.2.15] Set the mode/baud rate of the pins and extended UARTn before setting the EUnEN bit to "1".
- □ [14.2.16] Set EUAnMOD register while communication is stopped, and do not rewrite it while communicating.
- □ [14.2.18] Set EUAnBRC register while communication is stopped, and do not rewrite it while communicating.
- □ [14.2.19] Set EUAnBRT register while communication is stopped, and do not rewrite it while communicating.

- □ [14.2.21] Do not set EUIR bit and EUI21C to EUI00C bits simultaneously.
- □ [14.2.21] When the CPU writes to the interrupt request register (IRQ01, IRQ23, IRQ45, IRQ67) when an extended external interrupt occurs, the extended UART interrupt status register (EUISTAT) is set, but the interrupt request bit of the extended UART interrupt (QEUA = bit 3 of the IRQ67 register) is not set and the CPU may not be notified of an interrupt.
- □ [14.2.21] When writing to IRQ01, IRQ23, IRQ45, or IRQ67, set the EUIR bit of EUINTC register to 1 after the writing and rerequest the interrupt.
- □ [14.2.21] Refer to figure 14-12 for extended UART interrupt setting flow.
- □ [14.3.4] When UnFUL bit of UARTn status register (UAnSTAT) is set to "1" and UnEN bit of UARTn control register (UAnCON) is written to "1", transmission starts immediately. If the transmission data is not ready in UARTn transmit buffer (UAnBUF1), or if reception is allowed first, write "1" to the UnFUL bit of UAnSTAC, reset UnFUL bit, and then write "1" to UnEN bit of UAnCON to allow transmission and reception.
- □ [14.3.5.3] When designing the system, consider the difference of the baud rate between the transmission side and reception side, a delay of the start bit detection, signal degradation and noise influence, then adjust the baud rate and reception timing to ensure sufficient receiving margin.

17. GPIO

- □ [17.2.4] Because P01/TEST0 pin is initially configured as input with pull-up resistor, enter the "L" level in the default setting to the pin causes the input overcurrent flow.
- □ [17.2.5 to 17.2.8] When using an external interrupt, set the PnMODm register (m=0 to 7) certainly before setting the EICON0, EIMOD0 register, and IE1 register. Setting the PnMODm register with enabling interrupt may causes an unintended interrupt.
- □ [17.2.5 to 17.2.8] In order to prevent unintended output, set peripheral circuits and shared functions before enabling output is recommended.
- □ [17.2.11] PI0 and PI1 are unavailable to use as input ports when using the crystal resonator for the oscillation clock. Also, PI1 is unavailable to use as an input port when using the XT1 for the external clock input.
  See Chapter 6 "Clock Generation Circuit" for more details on how to use the crystal oscillation or external clock input.
- □ [17.3.8] Notes for using the P00/TEST0 pin

18. External Interrupt Function

- □ [18.2.3] When a high-speed clock is selected as the sampling clock, no sampling is required except for the HSCLK supply state (ENOSC=1 and oscillation stabilization is completed). Set it to "LSCLK0" if necessary.
- □ [18.2.3] During STOP/STOP-D mode, it works without sampling.
- □ [18.2.5] When writing to IRQ01/IRQ23/IRQ45/IRQ67 from the CPU while extended external interrupt is enabled, write "1" to EEIR bit of EEINTC register and request the interrupt again.
- □ [18.2.6] In STOP and STOP-D modes, the sampling clock stops, so no sampling is performed regardless of the value of the EPI3SM to EPI0SM bits in the EEIMOD0 register. There is a section *1 where the interrupt is disabled.
  *1 : When switching to the corresponding mode: maximum 30µs
  When returning from the corresponding mode: Period until the sampling clock (low-speed clock) supply starts.
  Since the period until the clock starts supplying varies depending on the setting, refer to "Table 4-5 Startup time from stan-by mode" in "Chapter 4 Power Management".
- □ [18.2.8] When using the on-chip debug function, do not uncheck "External Interrupt" in "Peripheral circuits to continue operation during break". If this check is cleared, this status may be cleared.
- □ [18.2.9] Do not set the EEIR bit at the same time as the EEI3C~EEI0C bit.
- □ [18.2.9] When an extended external interrupt occurs and the CPU writes to the interrupt request register (IRQ01, IRQ23, IRQ45, IRQ67), the extended external interrupt status register (EEISTAT) is set, but the extended external interrupt interrupt request bit (QEXTX=Bit 8) of the IRQ23 register may not be set and the CPU may not be notified of an interrupt.
- □ [18.2.9] If an extended external interrupt is enabled (when the extended external interrupt control register 0 (EEICON0) is set to something other than "Interrupt Prohibition"), set the EEIR of EEINTC to 1 and rerequest the interrupt.

19. CRC Calculator

- □ [19.2.2 ~ 19.2.5] Automatic CRC calculation is four-byte length. Generate an expected value by four bytes. Writing to the bits 1 and bit0 are ignored; they are fixed to "1" internally during the calculation.
- □ [19.2.3, 19.2.5] If an address set to CRCEAD and CRCESEG is smaller than one of CRCSAD and CRCSSEG, the calculation does not execute. Do not specify segment or address out of program code area. See section 2.5 "Program Memory Space" for details of the program code area.
- □ [19.3.2] To perform CRC calculation in the manual mode when automatic CRC calculation is not completed, save the value in the CRCRES register before calculation. Once the CRC calculation in the manual mode is completed, move the saved value back to the CRCRES register and set the CRCAEN bit to "1". If entering the HALT/HALT-H mode, then the automatic CRC calculation can be restarted.

□ [19.3.2] The final addresses at the end of the previous operation are stored in the CRCSAD and CRCSSEG registers. If values in the CRCSAD and CRCSSEG registers are overwritten with the CRCAEN bit set to "0", the calculation works incorrectly.

22. Voltage Level Supervisor

□ [22.2.2] If a reset other than power-on reset and pin reset occurs during VLS operation, the VLS retains its operating state.
□ [22.2.3] There is a limitation in each mode for entering the STOP/STOP-D mode while the VLS is running.
□ [22.2.5] In the STOP/STOP-D mode, the VLS works without sampling regardless the setting in VLS0SM1 bit.
□ [22.3.1.1, 22.3.1.2] Entering the STOP/STOP-D mode is not allowed during the VLS stabilization time. If entering the STOP/STOP-D mode after the supervisor mode is enabled, make sure that the VLS0RF bit is set to "1", and then enter the STOP/STOP-D mode.
□ [22.3.1.1] The initial value of the VLS detection voltage is 1.85V, so the MCU becomes in reset mode when the VDD is 1.85V or lower and VLS0 is specified as supervisor mode with the reset function. Therefore, set the detection voltage before enabling the VLS0 operation.
□ [22.3.1.1] When using the reset function of VLS like a reset IC, set the threshold voltage appropriate for the system in the low-speed clock state after starting the power supply, and start VLS.
□ [22.3.1.2] Entering the STOP/STOP-D mode is not allowed during the VLS stabilization time. If entering the STOP/STOP-D mode after the supervisor mode is enabled, make sure that the VLS0RF bit is set to "1", and then enter the STOP/STOP-D mode.
□ [22.3.1.2] When VLS0 is stopped (VLS0EN bit="0") while the VDD is lower than the specified threshold voltage (VLS0F bit="1"), the VLS0 interrupt is generated.
□ [22.3.2.1, 22.3.2.2] Entering the STOP/STOP-D mode is not allowed while the single mode operation is in progress. Enter the STOP/STOP-D mode after the single mode operation is completed (VLS0EN bit="0").
□ Entering the STOP/STOP-D mode is not allowed while the single mode operation is in progress. Enter the STOP/STOP-D mode after the single mode operation is completed (VLS0EN bit="0").
□ [22.3.2.2] If V_{DD} is higher than the specified threshold voltage, the VLS0 interrupt is not generated.

23. Successive Approximation Type A/D Converter

□ [23.1.3] When using the SA-ADC, set PnmIE bit and PnmOE bit of port n mode register 01/23/45/67 (n: port number 1, 2, 3, 7, m: bit number 0 to 7) to "0" as "Disable input" and "Disable output", otherwise a shoot-through current may flow.
□ [23.1.3] Noise influence to the conversion accuracy can be reduced by following ways.
Not switch other pins that are not used for conversion during A/D conversion
Execute A/D conversion while HALT mode.
□ [23.2.3] Start the A/D conversion with one or more channels selected by the SA-ADC enable registers (SADEN0 and SADEN1). If no channel is selected, the operation does not start.
□ [23.2.3] When switching to STOP/STOP-D mode, wait until SARUN bit becomes "0". When SARUN bit is "1", the transition to STOP/STOP-D mode cannot be entered.
□ [23.2.3] When SACK2 to 0 bits are set to 0x7, it takes up to 3 clocks of the low-speed clock (LSCLK0) from writing to SARUN to the start or stop operation.
□ [23.2.8, 23.2.9] Do not start the A/D conversion when the all bits of SACHn (n=00 to 17) set to "0". When A/D conversion is started in this state, the SARUN bit of the SADCON register does not become "1".
□ [23.2.13] When the upper and lower limit determination functions of A/D conversion are used (SALEN=1), the interrupt can be cleared by clearing the corresponding bits of SAULC15 to SAULC00 or resetting the LSI.
□ [23.2.13] When executing A/D conversion (SALP=0) only once, confirm that the corresponding bit of SAULS15 to SAULS00 is "0" before setting SARUN to "1".
□ [23.2.13] When performing the consecutive scan A/D conversion (SALP bit =1), confirm the bit of SAULS13 to SAULS00 is "0", before the next A/D conversion ends.
□ [23.4] Notes on SA-ADC

25. Audio Playback Function

□ [25.1.2.1] When using the audio playback function, select the Low speed crystal oscillation clock (XT32K) as the clock source for the Low speed clock 0 (LSCLK0).
□ [25.1.2.1] When using the audio playback function, enable High speed clock oscillation by frequency control register (FCONW).
□ [25.1.2.1] Selects PLL oscillation mode from 24 MHz mode or 16 MHz mode and set the high-speed clock mode register (FHCKMOD) so that the system clock set 24 MHz in 24 MHz mode and 16 MHz in 16 MHz mode.
□ [25.2.8,25.2.9] To set the value of the event management stop address register H/M/L, add +7 to the value set in the event management start address register H/M/L.
□ [25.2.12, 25.2.13] To set the value of the Editing data stop address register H/M/L, add +7 to the value set in the Editing data start address register H/M/L..

- □ [25.2.29] From writing of VFDAT to VSTAT flag update takes 2 clocks of the audio playback function clock, so execute read confirmation of flag update after placing 4 or more NOP instructions after VFDAT write.
- □ [25.2.29] From setting the VCEN from "1" to "0" to SEND becomes 1 takes 2 clocks of the audio playback function clock, so execute read confirmation of flag update after placing 4 or more NOP instructions after VCEN write.
- □ [25.2.29] If the VERR becomes "1", execute the following process (1) or (2).
- □ [25.2.36] Fixed detection circuitry works during audio playback. The register settings for audio playback are shown below. When SPEN="1" and VCEN="1", the PWM "H" level fixed detection circuit is enabled.
- □ [25.3.1] When operating at sysclk=24MHz, do not write to VFDAT/VFEDAT consecutively and place two or more NOP instructions to avoid erroneous writing to the Audio FIFO.
- □ [25.3.2] Store the final data of the 1st phrase in the FIFO phrase end data register (VFEDAT)..

26. Flash Memory

- □ [26.2.2] Note that programming for the program memory space is performed by the unit of 4 bytes. Because of this, the setting values in the FA1 bit and FA0 bit are ignored.
- □ [26.2.4, 26.2.5] Since writing to the program memory space or writing to the data flash is determined by the value set in the flash segment register (FLASHSEG), set the register first..
- □ [26.2.4, 26.2.5] During programming data-flash, a CPU can execute instruction by the back ground operation function; BGO. Confirm FDPRSTA bit of FLASHSTA register for complition of programming.
- □ [26.2.4, 26.2.5] Erase data in the addresses to be written in advance. Overwrite the data without erasing, the data is not guaranteed.
  [26.2.4, 26.2.5] Do not read/write to unused areas to prevent the CPU malfunction..
- □ [26.2.7, 26.2.8] If writes to FLASHSTA register when other than 0x0, the data in the flash memory being processed is not guaranteed.
- □ [26.2.9] Execute the erasing or programming after checking the FDERSTA bit or FDPRSTA bit are "0".
- □ [26.2.9] Do not execute the erasing or programming when either the FDERSTA bit or the FDPRSTA bit is "1".
- □ [26.3.1] Notes on Debugging Self-programming Code
- □ [26.3.2] Only erase areas irrelevant to program processing. If erasing the area where program processing is in progress, the LSI works incorrectly.
- □ [26.3.2] During block/sector erasing, the CPU stops the operation for maximum 50 ms whereas peripheral circuits continue operation. Therefore, clear the WDT counter accordingly.
- □ [26.3.2, 26.3.3] For block/sector erasing, place two NOP instructions following the instruction used to set FERS/FSERS bits of the FLASHCON register to "1".
- □ [26.3.3] The CPU continues program processing even while data flash programming is in progress. An entering to the STOP/STOP-D/HALT-D/HALT-H mode is not available during the programming. In addition, set the FSELF bit of the FLASHSLF register to "0" (erase/program disabled) after the programming ended.
- □ [26.3.3] The data flash area is unreadable during programming.
- □ [26.3.3] For data programming setting, place two NOP instructions following the instruction used to set the programming data in the FLASHD0L register.
- □ [26.3.4] Notes on use of self-programming
- □ [26.4.3] Accessing to the program code area is performed in 4byte units. Set 4byte boundaries (0H/4H/8H/CH) for lower 4bits of the address. Accessing to the data flash area is performed in units of 1byte.
- □ [26.4.3] All commands except some confirmation commands (*1) are reflected when a next command is sent.
- □ [26.4.5.1 to 26.4.5.4, 26.4.6.2 to 26.4.6.4] Transmit command to avoid a timeout. See Section 26.4.3.1 "Command Timing".
- □ [26.4.5.2 to 26.4.5.4, 26.4.6.2 to 26.4.6.4] Transmit any command after 'initial setting command (7)' if other command will not be transmit.

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27.LCD driver

- □ [27.2.5 to 27.2.9] If the SEGMOD0~4 register is set in the display state, there is a risk of erroneous display or panel damage, so set it in the display stop state (LMD1, LMD0=00 in the DSPCON register).

28. On-Chip Debug Function

- □ [28.3] Make TEST1_N pin able to be connected to VDD with a jumper or something when not using the on-chip debug function.
- □ [28.3] Validate the ROM code on user production board without the On-chip emulator.
- □ [28.3] Disconnect On-chip emulator when measuring the current consumption of the target system. If On-chip emulator remains connected, the current consumption increases as the on-chip debug circuit inside the LSI works for the communication.
- □ [28.3] When using the 3.3 VOUT power supply of On-chip emulator, do not apply power of the target system to the VDD pin of LSI. If both power supplies are connected, On-chip emulator may be damaged, or an electric shock or fire may occur

□ [28.3] LSI used to debug a program is not covered by the product warranty. Do not use the LSI for mass-production.
□ [28.3] A reset due to unused ROM area access does not occur in the on-chip debug mode regardless of code option settings.
□ [28.3] A RAM parity error reset does not occur in the on-chip debug mode and the break operation occurs instead.
□ [28.3] If the contents of the data memory are displayed in the debugger in a state where a RAM parity error may occur (including when the RAM is not initialized), a RAM parity error may occur even if the RAM area is not displayed.
□ [28.3] The all interrupts and watchdog timer operation always stop while the debugger is in the break state.
□ [28.3] On-chip emulator might be affected by the external environments such as the host PC, USB cable, On-chip emulator interface cable and the target system. Please confirm proper environments before using on-chip emulator.
□ [28.3] If adding an external capacitor to the TEST1_N pin, prepare a jumper function on the board so that the capacitor gets dis-connectable when using the debugger or Flash multi-writer.

29. Safety Function

□ [29.2.8] If the MCISTATL register is not zero, a request to interrupt controller is not given when a new interrupt occurs. Clear the MCISTATL register with the MCINTCL register before that time.
□ [29.3.2] CSR[3] is unused on the ML62Q2700 group. The data of CSR "0x8 to 0xF" are handled as "0x0 to 0x7".
□ [29.3.3] For "Overflow value setting" in Figure 29-5, set the value so that the overflow period of the 16-bit timer n is to be shorter than that of the functional timer n. If the functional timer n overflows, it disables the accurate check.

30. Code Option

□ [30.2.1] The value of a code option that can be referenced from the SFR area is readable only when the INITE flag in the reset status register (RSTAT) is "0".
□ [30.3] For the code option data definition, always use the dw directive instruction to configure the data in the unit of word.

31. Auxiliary Function

A. SFR List

□ The functionality is not guaranteed when access to “Reserved” register. So please do not access them.

B. Package Dimensions

□ The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).
□ The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

C. Instruction Execution Cycle

D. Application Circuit Example

□ Place the capacitor for VDDL pin as close to the LSI power pins as possible.

Revision History

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL62Q2700-01	2023.09.14	—	—	1st edition.
FEUL62Q2700-02	2024.03.26	*-*	*-*	Corrected typo, unified wording, revised descriptions
		-	*-*	Corrected and added information as for ML62Q2723/2723/ 2704/2722/ 2712/2702
		1	1	Revised note
		1-1	1-1	[1-1] Updated product status.
		1-1	1-1	[1.1] Added use application
		1-4, 1-5	1-4, 1-5	[1.1][1.1.1] Updated description for product name
		1-5, 1-6	1-5, 1-6	[1.1.1][1.1.2] Separated section
		1-1	1-1	[1.1] Added use application
		4-21, 4-23	4-21, 4-23	[4.3.2.2][4.3.2.6] Corrected description as for HALT-H
		4-29	4-29	[4.3.4] Corrected Table 4-8
		6-4	6-4	[6.1.2] Corrected Table 6-4.
		6-29	6-29	[6.3.2.2] Corrected sequence (6).
		8-3	8-3	[8.1.3] Corrected Table 8-2.
		9-12	9-12	[9.2.4] Added description in the CAPTURE mode.
		9-14	9-14	[9.2.6] Updated note as for the counter reading
		9-15	9-15	[9.2.7] Added description in the CAPTURE mode.
		9-23	9-23	[9.2.13] Added note as for clearing interrupt status
		-	9-43	[9.3.4.2] Added new section
		9-45	9-46	[9.3.6.1] Corrected setting flow of the event trigger.
		10-16	10-16	[10.3.3] Corrected note.
		11-17, 11-18	11-17, 11-18	[11.3.3] Corrected Figure 11-7 and 11-8
		-	14-31	[14.3.6] Added description as for extended UART interrupt.
		-	18-16	[18.3.4] Added section for extended external interrupt
		23-4	23-4	[23.1.3] Corrected Table 23-2.
		23-7, 23-8	23-7, 23-8	[23.2.2] Corrected description of the SASHT bit and Table23-4.
		23-8	23-8	[23.2.2] Added a condition of 4MHz in the Fig 23-3
		23-31	23-31	[23.4.1] Corrected V_{DD} to V_{REF} and corrected V_{REF} condition
		25-15	25-15	[25.2.15] Corrected description of VEXSTP2 bit.
		25-33	25-33	[25.2.33] Corrected description of VSTP bit.
		28-1	28-1	[28.1.1] Deleted trace function
		28-3	28-3	[28.3] Corrected the note
		29-9	29-9	[29.2.8] Added note as for clearing interrupt status
		31-5	31-5	[31.3.1] Corrected address in the Table31-1.
		E-*	E-*	Updated the description all according to revised pages in each chapter.
		*	*	Correction of errors in address and bit numbers, figures, and table numbers
		-	2-19	[2.6] Added Figure 2-3-5
		19-10	19-10	[19.3.2] Corrected the reference series
		3-4	3-4	[3.2.3] Corrected register description
		3-5	3-5	[3.3.1] Corrected Table 3-2