Accelerometer Series

Kionix™ Technology
Accelerometer IC for Automotive

KX310CR-MZ

General Description

KX310CR-MZ is a MEMS capacitive 3-axis accelerometer using Kionix™ Technology.*(Note 1)* Acceleration ranges of ±2 g, ±4 g and ±8 g are supported. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element which further utilize common mode cancellation to decrease errors from process variation, temperature, and environmental stress.

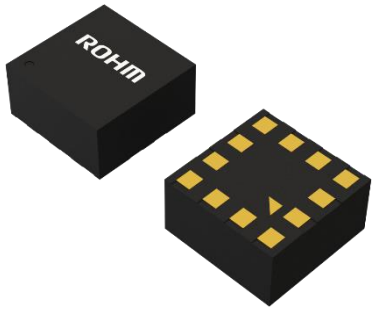
(Note 1) Kionix™ Technology is defined by the proprietary plasma micromachining process and the technology to hermetically seal at a wafer level by bonding the silicon lid wafer to the device wafer.

Key Specifications

- Acceleration Range: ±2 g, ±4 g or ±8 g
- Wake-up and Back-to-sleep Engine Threshold Resolution: 3.9 mg/counts
- Output Data Rate: 0.781 Hz to 1600 Hz
- Operating Temperature Range: -40 °C to +85 °C

Package VLGA012AV02A

W (Typ) x D (Typ) x H (Max) 2.0 mm x 2.0 mm x 1.0 mm



Features

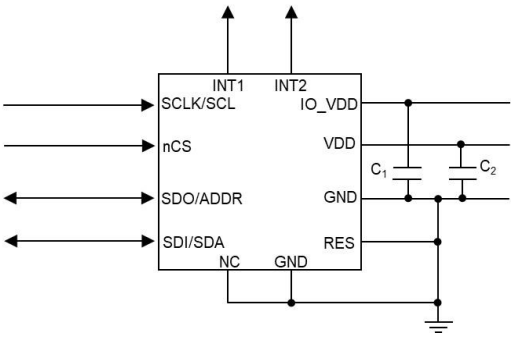
- Kionix™ Technology*(Note 1)*
- AEC-Q100 Qualified*(Note 2)*
- Selectable Acceleration Range
- Selectable Output Data Rate
- Selectable Low Power or High Resolution Mode
- Digital High-pass Filter Outputs
- Low Power Mode with Optimization
- Configurable Wake-up / Back-to-sleep Function
- Digital I²C up to 400 kHz
- Digital SPI up to 10 MHz
- Lead-free Solderability
- Excellent Temperature Performance
- High Shock Survivability
- Factory Programmed Offset and Sensitivity
- Self-test Function

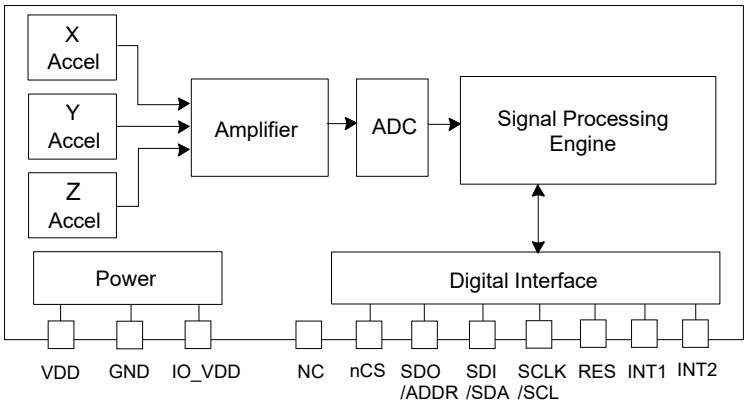
(Note 2) Grade 3

Applications

- Keyfob
- Car Navigation
- Drive Recorder
- Asset Tracking
- Telematics Insurance
- Rear Seat Reminder System

Typical Application Circuit and Block Diagram



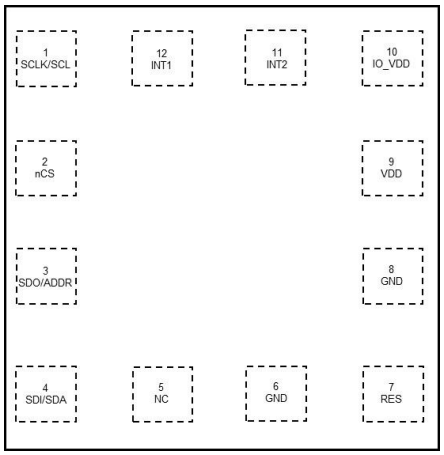


○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configuration

Top View



Pin Description

Pin No.	Pin Name	Function
1	SCLK/SCL	SPI and I^2C Serial Clock Input pin*(Note 1)*. Do not leave floating.
2	nCS*(Note 2)*	Chip Select (active Low) for SPI communication. Connect to IO_VDD for I^2C communication. Do not leave floating.
3	SDO/ADDR*(Note 3)*	Serial Data Out pin during 4-wire SPI communication and the LSB (Least Significant Bit) setting pin of the Target Address during I^2C communication.
4	SDI/SDA	Serial Data Input/Output pin during SPI communication and I^2C Serial Data pin*(Note 1)*. Do not leave floating.
5	NC	Not internally connected. Can be connected to VDD, IO_VDD or GND.
6	GND	Ground
7	RES	Reserved pin, connect to GND
8	GND	Ground
9	VDD	Power voltage pin*(Note 4)*
10	IO_VDD	Power voltage pin*(Note 4)*
11	INT2	Physical Interrupt. The pin is in High-impedance state during Power-on sequence and is driven following Power-on sequence. Leave floating if not used.
12	INT1	Physical Interrupt. The pin is in High-impedance state during Power-on sequence and is driven following Power-on sequence. Leave floating if not used.

(Note 1) When there is other device which is connected to SDA, SCL, INT1 and INT2 pins and its signal falls sharply, that might generate undershoot and the pin voltage might go below ground. When such undershoot occurs, a measure like disposing a capacitor near the pins of the device must be taken.
(Note 2) Internally pulled-up to IO_VDD (default) , and it can be disconnected by the NCS_PU_OFF register bit.
(Note 3) Internally pulled-up to IO_VDD.
(Note 4) Place a bypass capacitor (0.1 µF) as close as possible to the IC.

Absolute Maximum Rating (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage (VDD, IO_VDD)	V_{MAX}	4.5	V
Input/Output Voltage *(Note 1)*	V_{INOUT}	-0.3 to +4.5	V
Storage Temperature Range	Tstg	-40 to +125	°C
Maximum Junction Temperature	Tjmax	150	°C
Mechanical Shock (Powered and Unpowered)	S_{OVR}	5000 g for 0.5 ms 10000 g for 0.2 ms	g

(Note 1) Except VDD, IO_VDD and GND pins

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 4)*	2s2p *(Note 5)*	
VLGA012AV02A				
Junction to Ambient	θ_{JA}	195.7	131.0	°C/W
Junction to Top Characterization Parameter *(Note 3)*	Ψ_{JT}	8	6	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (VDD)	V_{VDD}	1.7	3.0	3.6	V
I/O Pads Supply Voltage (IO_VDD)	V_{IO_VDD}	1.7	3.0	V_{VDD}	V
Input Voltage	V_{IN}	0.0	-	V_{IO_VDD}	V
I^2C Communication Rate	f_{SCL_I2C}	-	-	0.4	MHz
SPI Communication Rate	f_{SCLK_SPI}	-	-	10	MHz
I^2C Target Address *(Note 6)*	-	1Eh or 1Fh			-
WHO_AM_I Register Value	-	E0h			-
Output Data Rate *(Note 7)*	-	0.781	50	1600	Hz
Output Signal Bandwidth	-	ODR/9 or ODR/2			-
Operating Temperature	Topr	-40	+25	+85	°C

(Note 6) Determined by ADDR pin assignment: GND for 1Eh, IO_VDD for 1Fh.
(Note 7) Typical values. ODR is selectable via I^2C or SPI. See ODCNTL register for details.

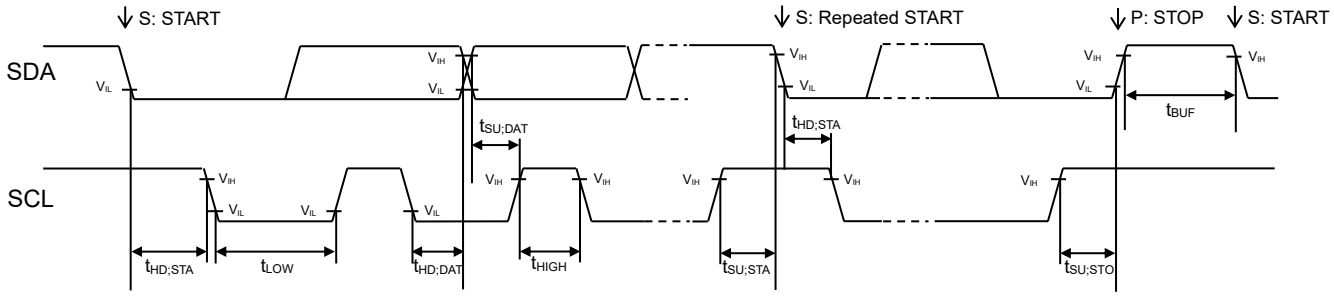
Electrical Characteristic

(Unless otherwise specified V_{VDD} = 3.0 V, V_{IO_VDD} = 3.0 V, Ta = 25 °C and Acceleration Range = ±2 g)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Current Consumption						
High Resolution Mode	I_{dd_HR}	-	250	-	µA	
Low Power Mode	I_{dd_LP1}	-	1.5	2.9	µA	ODR = 12.5 Hz *(Note 1)*
	I_{dd_LP2}	-	1.0	2.2	µA	ODR = 6.25 Hz *(Note 2)*
Standby Mode	I_{ss}	-	0.2	-	µA	
Logic						
L Input Voltage	V_{IL}	-	-	0.2 x V_{IO_VDD}	V	
H Input Voltage	V_{IH}	0.8 x V_{IO_VDD}	-	-	V	
L Output Voltage *(Note 3)*	V_{OL1}	-	-	0.2 x V_{IO_VDD}	V	V_{IO_VDD} < 2 V
	V_{OL2}	-	-	0.4	V	V_{IO_VDD} ≥ 2 V
H Output Voltage	V_{OH}	0.8 x V_{IO_VDD}	-	-	V	
nCS and SDO/ADDR pins Pull-up Resistance	R_{pu1}	-	50	-	kΩ	V_{IO_VDD} = 3.0 V
	R_{pu2}	-	130	-	kΩ	V_{IO_VDD} = 1.7 V
Boot Characteristics						
Start Up Time *(Note 4)*	T_{SU_HR}	-	0.9 + 1000 / ODR	-	ms	High Resolution Mode
	T_{SU_LP}	-	1.9	-	ms	Low Power Mode
Power Up Time *(Note 5)*	T_{PU}	-	2	20	ms	
Accelerometer Characteristics						
Zero-g Offset	-	-	±25	±90	mg	
Zero-g Offset Variation from RT over Temperature	-	-	±0.2	-	mg/°C	
Sensitivity	-	15401	16384	17367	counts/g	GSEL [1:0] = 0 (±2 g)
	-	7700	8192	8684	counts/g	GSEL [1:0] = 1 (±4 g)
	-	3850	4096	4342	counts/g	GSEL [1:0] = 2 (±8 g)
Sensitivity Variation from RT over Temperature	-	-	±0.01	-	%/°C	X,Y-axis
	-	-	±0.03	-	%/°C	Z-axis
Self-test Output Change on Activation	-	0.07	0.5	1.5	g	
Non-Linearity	-	-	±0.6	-	% of FS	
Cross Axis Sensitivity	-	-	2	-	%	
RMS Noise *(Note 6)*	-	-	5.5	-	mg	

(Note 1) Measured with OSA [3:0] = 4, AVC [2:0] = 1.
(Note 2) Measured with OSA [3:0] = 3, AVC [2:0] = 1.
(Note 3) For I^2C communication, this assumes a minimum 1.5 kΩ pull-up resistor between SCL/SDA pins and IO_VDD pin.
(Note 4) Start up time is from PC1 = 1 to valid outputs. Time varies with ODR and Power Mode bit setting.
(Note 5) Power up time is from VDD valid to device boot completion.
(Note 6) Noise varies with settings. Measured with HR = 0, OSA [3:0] = 6, AVC [2:0] = 2, IIR_BYPASS = 0, LPRO = 1 settings.

I²C Bus Timing Chart

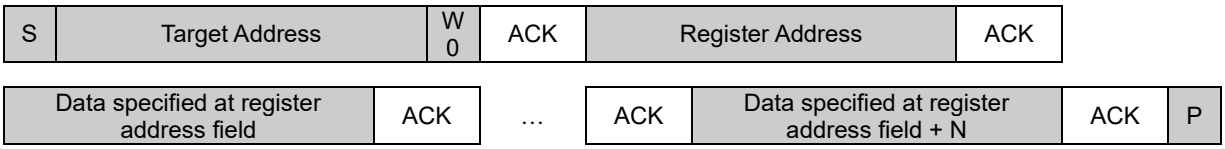


(Unless otherwise specified V_{VDD} = 3.0 V, V_{IO_VDD} = 3.0 V and Ta = 25 °C)

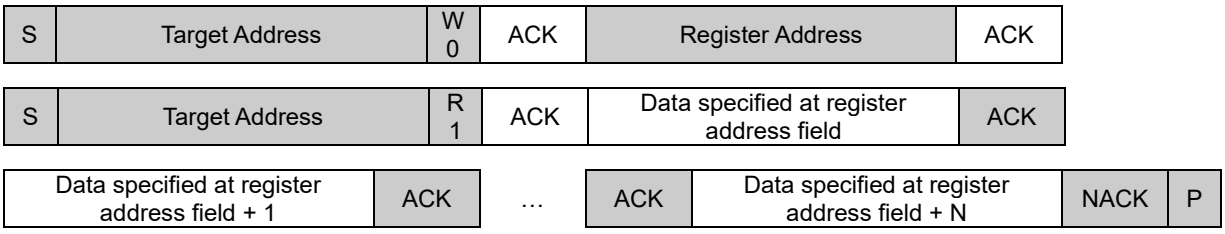
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCL Clock frequency	f_{SCL}	0	-	400	kHz	
'L' Period of SCL Clock	t_{LOW}	1.3	-	-	µs	
'H' Period of SCL Clock	t_{HIGH}	0.6	-	-	µs	
Setup Time for Repeated START	$t_{SU;STA}$	0.6	-	-	µs	
Hold Time for START	$t_{HD;STA}$	0.6	-	-	µs	
Data Setup Time	$t_{SU;DAT}$	100	-	-	ns	
Data Hold Time	$t_{HD;DAT}$	0	-	-	µs	
Setup Time for STOP	$t_{SU;STO}$	0.6	-	-	µs	
Bus Free Time between STOP and START	t_{BUF}	1.3	-	-	µs	

1. Write Format
   (1) Indicate register address

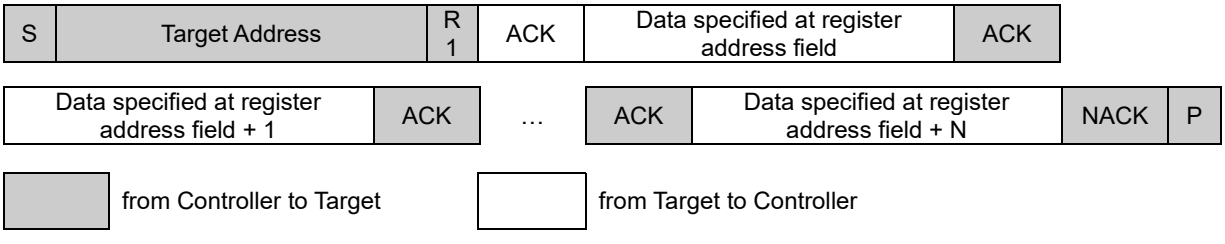
   (2) Write data after indicating register address



2. Read Format
   (1) Read data after indicating register address

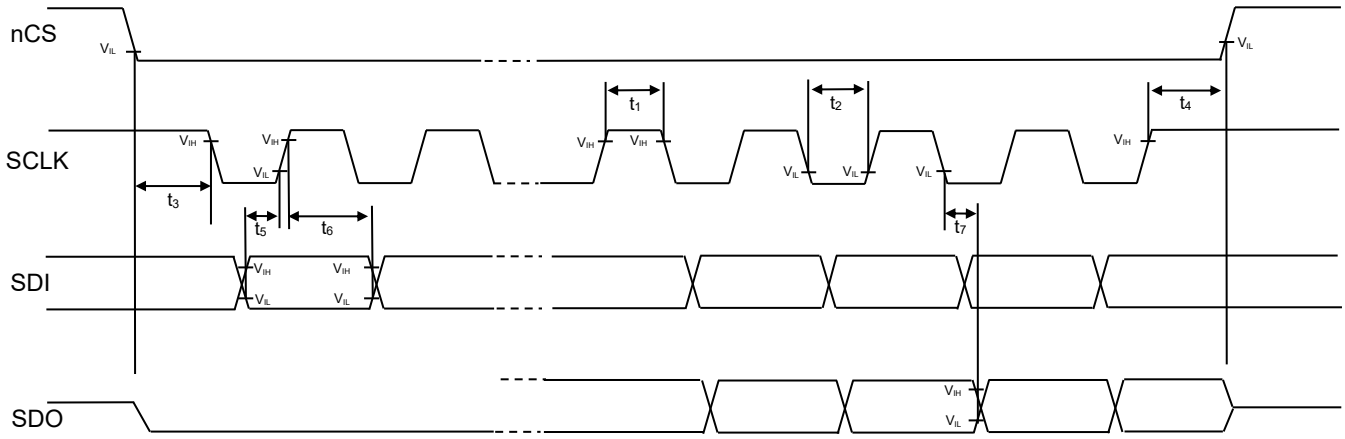


   (2) Read data from the specified register



4-Wire SPI Bus Timing Chart

Timings are with maximum 20 pF load capacitor on SDO. SCLK keeps HIGH when nCS is HIGH (no transmission). The MSB (Most Significant Bit) of the register address byte will indicate '0' when writing to the register and '1' when reading from the register. All commands are sent MSB first. The host must return nCS HIGH for at least one clock cycle ($1/f_{SCLK}$) before the next data request.

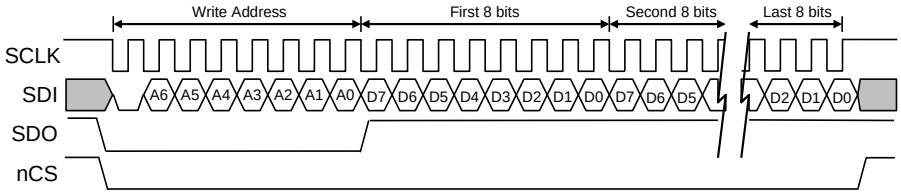


(Unless otherwise specified V_{VDD} = 3.0 V, V_{IO_VDD} = 3.0 V and Ta = 25 °C)

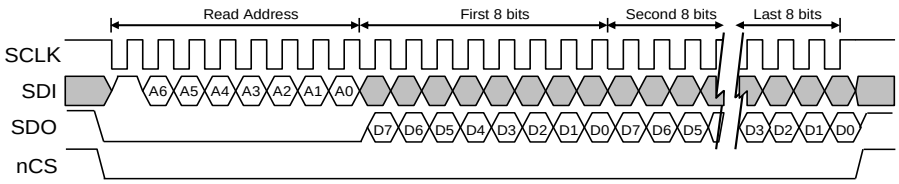
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCLK Clock frequency	f_{SCLK}	-	-	10	MHz	
'H' Period of SCLK Clock	t_1	45	-	-	ns	
'L' Period of SCLK Clock	t_2	45	-	-	ns	
nCS LOW to first SCLK falling edge	t_3	6	-	-	ns	
nCS LOW after the final SCLK rising edge to nCS rising edge	t_4	8	-	-	ns	
SDI input valid to SCLK rising edge	t_5	10	-	-	ns	
SCLK rising edge to SDI input invalid	t_6	10	-	-	ns	
SCLK falling edge to SDO output becomes valid *(Note 1)*	t_7	-	35	50	ns	

(Note 1) Only present during reads.

1. Write Fromat

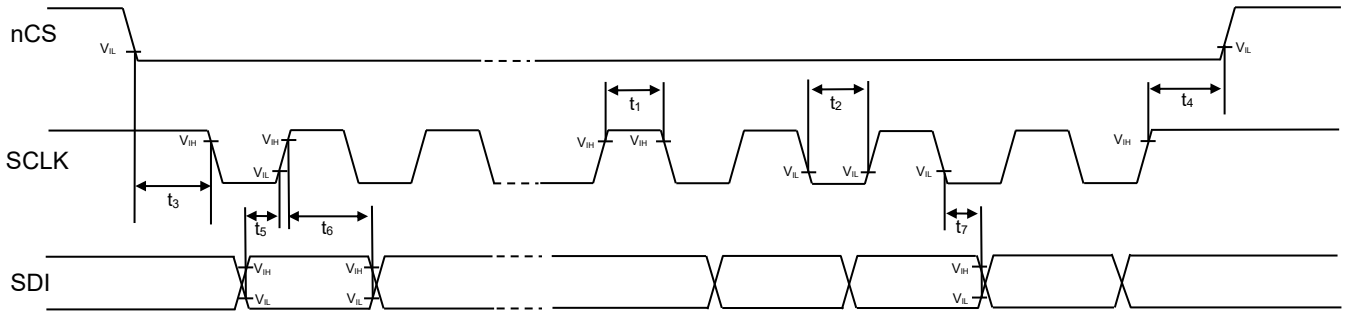


2. Read Format



3-Wire SPI Bus Timing Chart

Timings are with 1 kΩ pull-up resistor and maximum 20 pF load capacitor on SDI. SCLK keeps HIGH when nCS is HIGH (no transmission). The MSB (Most Significant Bit) of the register address byte will indicate '0' when writing to the register and '1' when reading from the register. All commands are sent MSB first. The host must return nCS HIGH for at least one clock cycle ($1/f_{SCLK}$) before the next data request.

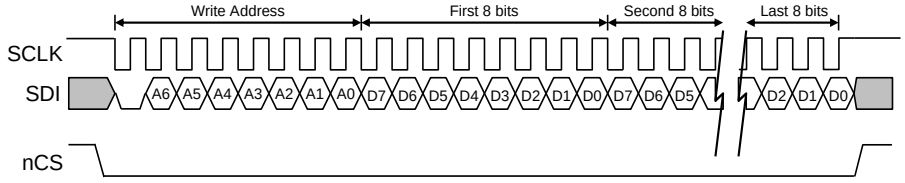


(Unless otherwise specified V_{VDD} = 3.0 V, V_{IO_VDD} = 3.0 V and Ta = 25 °C)

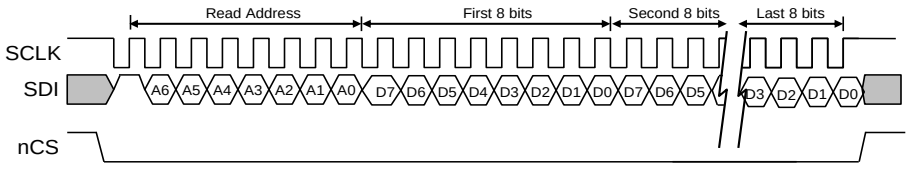
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCLK Clock frequency	f_{SCLK}	-	-	10	MHz	
'H' Period of SCLK Clock	t_1	45	-	-	ns	
'L' Period of SCLK Clock	t_2	45	-	-	ns	
nCS LOW to first SCLK falling edge	t_3	6	-	-	ns	
nCS LOW after the final SCLK rising edge to nCS rising edge	t_4	8	-	-	ns	
SDI input valid to SCLK rising edge	t_5	10	-	-	ns	
SCLK rising edge to SDI input invalid	t_6	10	-	-	ns	
SCLK falling edge to SDI output becomes valid*(Note 1)*	t_7	-	35	50	ns	

(Note 1) Only present during reads.

1. Write Fromat



2. Read Format



Register Map(Note 1)

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	XHPL	R	XHP [7:0]							
01h	XHPH	R	XHP [15:8]							
02h	YHPL	R	YHP [7:0]							
03h	YHPH	R	YHP [15:8]							
04h	ZHPL	R	ZHP [7:0]							
05h	ZHPH	R	ZHP [15:8]							
06h	XOUTL	R	XOUT [7:0]							
07h	XOUTH	R	XOUT [15:8]							
08h	YOUTL	R	YOUT [7:0]							
09h	YOUTH	R	YOUT [15:8]							
0Ah	ZOUTL	R	ZOUT [7:0]							
0Bh	ZOUTH	R	ZOUT [15:8]							
0Ch	COTR	R	COTR [7:0]							
0Eh	INS1	R	WUFS2	BTS2	XNWU2	XPWU2	YNWU2	YPWU2	ZNWU2	ZPWU2
0Fh	WHO_AM_I	R/W	WAI [7:0]							
13h	INS2	R	BTS	Reserved		DRDY	Reserved		WUFS	Reserved
14h	INS3	R	Reserved		XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU
15h	STATUS_REG	R	PC1_STAT	PARITY_F	CRC_F	INT	POR_STAT	STAT_REG	Reserved	WAKE
17h	INT_REL	R	INT_REL							
18h	CNTL1	R/W	PC1	HR	DRDYE	GSEL [1:0]		Reserved	WUFE	Reserved
19h	CNTL2	R/W	SRST	COTC	INT1_OR	INT2_OR	Reserved			
1Ah	CNTL3	R/W	Reserved					OWUF [2:0]		

(Note 1) Do not write any commands to other addresses except above.

Register Map(Note 1) **– continued**

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Bh	ODCNTL	R/W	IIR_BYPASS	LPRO	Reserved		OSA [3:0]			
1Ch	INC1	R/W	PW [1:0]		IEN1	IEA1	IEL1	PPOD	STPOL	SPI3E
1Dh	INC2	R/W	Reserved	AOI	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE
1Fh	INC4	R/W	Reserved			DRDYI1	BTSI1	Reserved	WUFI1	Reserved
20h	INC5	R/W	Reserved	NCS_PU_OFF	IEN2	IEA2	IEL2	ACLR2	ACLR1	Reserved
21h	INC6	R/W	Reserved			DRDYI2	BTSI2	Reserved	WUFI2	Reserved
23h	WUFC	R/W	WUFC [7:0]							
2Ch	MAN_WAKE	W	Reserved		MAN_WAKE2	MAN_SLEEP2	Reserved		MAN_WAKE	MAN_SLEEP
2Dh	BTS_CNTL	R/W	BTSE	0	BTS_RES [2:0]		OBTS [2:0]			
2Eh	BTSC	R/W	BTSC [7:0]							
2Fh	BTS_TH	R/W	BTSTH [7:0]							
30h	WUF_TH	R/W	WUFTH [7:0]							
31h	BTS_WUF_TH	R/W	Reserved	BTSTH [10:8]			Reserved	WUFTH [10:8]		
35h	LP_CNTL	R/W	1	AVC [2:0]			0	0	1	1
40h	WUF_TH2	R/W	WUFTH2 [7:0]							
41h	BTS_WUF_TH2	R/W	Reserved	BTSTH2 [10:8]			Reserved	WUFTH2 [10:8]		
42h	BTS_TH2	R/W	BTSTH2 [7:0]							
43h	WUFC2	R/W	WUFC2 [7:0]							
44h	BTSC2	R/W	BTSC2 [7:0]							
45h	BTS_WUF_CNTL1	R/W	WUFE2	BTSE2	OWUF2 [2:0]			OBTS2 [2:0]		
46h	BTS_WUF_CNTL2	R/W	0	TH_MODE	C_MODE_BTS	C_MODE_WUF	BTS_RES2 [2:0]			1
60h	SELFTEST	W	SELFTEST [7:0] (activation key = CAh)							

(Note 1) Do not write any commands to other addresses except above. Do not write '1' to the fields in which value is '0' in above table. Do not write '0' to the fields in which value is '1' in above table.

Register Map – continued

(00h-05h) XHPL, XHPH, YHPL, YHPH, ZHPL, ZHPH

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	XHPL	R	XHP [7:0]							
01h	XHPH	R	XHP [15:8]							
02h	YHPL	R	YHP [7:0]							
03h	YHPH	R	YHP [15:8]							
04h	ZHPL	R	ZHP [7:0]							
05h	ZHPH	R	ZHP [15:8]							

Fields	Function
XHP [15:0] YHP [15:0] ZHP [15:0]	High-pass filter accelerometer output. Data is updated at the ODR frequency determined by either OWUF in CNTL3 or OBTS in BTS_CNTL.

(06h-0Bh) XOUTL, XOUTH, YOUTL, YOUTH, ZOUTL, ZOUTH

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
06h	XOUTL	R	XOUT [7:0]							
07h	XOUTH	R	XOUT [15:8]							
08h	YOUTL	R	YOUT [7:0]							
09h	YOUTH	R	YOUT [15:8]							
0Ah	ZOUTL	R	ZOUT [7:0]							
0Bh	ZOUTH	R	ZOUT [15:8]							

Fields	Function
XOUT [15:0] YOUT [15:0] ZOUT [15:0]	When accelerometer is enabled (PC1 bit is set to 1 in CNTL1 register), the 16-bits of valid acceleration data for each axis is routed to registers. The output data is available in 2's complement data format.

Register Map – continued

Data Format:

16-bits Register Data (2's complement)	Equivalent Counts in decimal	Acceleration Range: ±2 g	Acceleration Range: ±4 g	Acceleration Range: ±8 g
0111 1111 1111 1111	+32767	+1.99994 g	+3.99988 g	+7.99976 g
0111 1111 1111 1110	+32766	+1.99988 g	+3.99976 g	+7.99952 g
…	…	…	…	…
0000 0000 0000 0001	+1	+0.00006 g	+0.00012 g	+0.00024 g
0000 0000 0000 0000	0	0.00000 g	0.00000 g	0.00000 g
1111 1111 1111 1111	-1	-0.00006 g	-0.00012 g	-0.00024 g
…	…	…	…	…
1000 0000 0000 0001	-32767	-1.99994 g	-3.99988 g	-7.99976 g
1000 0000 0000 0000	-32768	-2.00000 g	-4.00000 g	-8.00000 g

(0Ch) COTR

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	COTR	R	COTR [7:0]							

default value 55h

Fields	Function
COTR [7:0]	The COTR is used for command test response which verifies proper integrated circuit functionality. The value of this register will change from a default value of 55h to AAh when COTC bit in CNTL2 register is set. After reading AAh from this register, the value returns to the default value of 55h and COTC bit in CNTL2 register is self-cleared.

(0Eh) INS1

Motion Engine Interrupt Status register reports the axis and direction of detected motion that triggered the Wake-up2 and Back-to-sleep2 interrupt.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Eh	INS1	R	WUFS2	BTS2	XNWU2	XPWU2	YNWU2	YPWU2	ZNWU2	ZPWU2

Fields	Function
WUFS2	Reports the Wake-up2 interrupt status. This bit is cleared when the interrupt latch release register INT_REL is read. WUFS2 = 0 - No Wake-up2 event is detected. WUFS2 = 1 - Wake-up2 event is detected.
BTS2	Reports the Back-to-sleep2 interrupt status. This bit is cleared when the interrupt latch release register INT_REL is read. BTS2 = 0 - No Back-to-sleep2 event is detected. BTS2 = 1 - Back-to-sleep2 event is detected.
XNWU2	X Negative (X-) Reported
XPWU2	X Positive (X+) Reported
YNWU2	Y Negative (Y-) Reported
YPWU2	Y Positive (Y+) Reported
ZNWU2	Z Negative (Z-) Reported
ZPWU2	Z Positive (Z+) Reported

Register Map – continue

(0Fh) WHO_AM_I

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	WHO_AM_I	R/W	WAI [7:0]							

default value E0h

Fields	Function
WAI [7:0]	This register can be used for product recognition, as it can be factory written to a known byte value. The default value is E0h.

(13h) INS2

This register tells which function caused an interrupt.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
13h	INS2	R	BTS	Reserved		DRDY	Reserved		WUFS	Reserved

Fields	Function
BTS	Reports the Back-to-sleep interrupt status. This bit is cleared when the interrupt latch release register INT_REL is read. BTS = 0 - No Back-to-sleep event is detected. BTS = 1 - Back-to-sleep event is detected.
DRDY	Reports that new acceleration data is available. This bit is cleared when acceleration data is read or the interrupt latch release register INT_REL is read. DRDY = 0 - New acceleration data is not available. DRDY = 1 - New acceleration data is available.
WUFS	Reports the Wake-up interrupt status. This bit is cleared when the interrupt latch release register INT_REL is read. WUFS = 0 - No Wake-up event is detected. WUFS = 1 - Wake-up event is detected.

(14h) INS3

Motion Engine Interrupt Status register reports the axis and direction of detected motion that triggered the Wake-up and Back-to-sleep interrupt.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
14h	INS3	R	Reserved		XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU

Fields	Function
XNWU	X Negative (X-) Reported
XPWU	X Positive (X+) Reported
YNWU	Y Negative (Y-) Reported
YPWU	Y Positive (Y+) Reported
ZNWU	Z Negative (Z-) Reported
ZPWU	Z Positive (Z+) Reported

Register Map – continued

(15h) STATUS_REG

This register reports the status of the device.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
15h	STATUS_REG	R	PC1_STAT	PARITY_F	CRC_F	INT	POR_STAT	STAT_REG	Reserved	WAKE

Fields	Function
PC1_STAT	Reports if the PC1 bit in CNTL1 register is set or not. PC1_STAT = 0 - PC1 bit in CNTL1 register is not set. PC1_STAT = 1 - PC1 bit in CNTL1 register is set.
PARITY_F	Reports the Parity check failure. PARITY_F = 0 - No failure has detected. PARITY_F = 1 - Register failure has detected, perform Software Reset or Power Cycle the device.
CRC_F	Reports One Time Programmable (OTP) memory load failure. CRC_F = 0 - No failure has detected. CRC_F = 1 - OTP loading has failed. Perform Software Reset or Power Cycle the device.
INT	Reports the combined (OR) interrupt information according to interrupt setting. INT = 0 - No interrupt event is detected. INT = 1 - One or more interrupt events are detected.
POR_STAT	Reports the Power Cycle status of KX310CR-MZ. POR_STAT = 0 - No Power Cycle or Software Reset events. POR_STAT = 1 - Power Cycle or Software Reset events occurred. This bit is self-cleared when the STATUS_REG register is read.
STAT_REG	Reports whether KX310CR-MZ is running and sensing motion OK. STAT_REG = 0 - The accelerometer is either in Standby mode or has detected that supplied VDD is below the minimum required, in which case the output data may not be valid. STAT_REG = 1 - The accelerometer is running and sensing motion.
WAKE	Reports the motion detection status of Wake-up/Back-to-sleep function. WAKE = 0 - KX310CR-MZ is in the Sleep state. WAKE = 1 - KX310CR-MZ is in the Wake state. Note that the WAKE bit just indicates the motion detection status, no KX310CR-MZ power mode changes. The Sleep state is the default after power-up.

(17h) INT_REL

Latched interrupt source information is cleared, and physical interrupt latched pin is changed to its inactive state when this register is read. Read value is dummy.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
17h	INT_REL	R	INT_REL							

Register Map – continued

(18h) CNTL1

Read/write control register that provides more feature set control. Note that to properly change the value of this register (except PC1 bit) , the PC1 bit must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
18h	CNTL1	R/W	PC1	HR	DRDYE	GSEL [1:0]		Reserved	WUFE	Reserved

default value 00h

Fields	Function
PC1	Controls the operating mode of the KX310CR-MZ. When in HR = 0, allow 1.2/ODR delay time when transitioning from standby PC1 = 0 to operating mode. PC1 = 0 - KX310CR-MZ is in the Standby Mode. PC1 = 1 - KX310CR-MZ is in the either Low Power or High Resolution Mode.
HR	Determines the power mode of KX310CR-MZ. The noise varies with ODR, HR and different AVC settings possibly reducing the effective resolution. HR = 0 - KX310CR-MZ is in the Low Power Mode in case the PC1 bit is set to 1. HR = 1 - KX310CR-MZ is in the High Resolution Mode in case the PC1 bit is set to 1.
DRDYE	Enables the reporting of the availability of new acceleration data as an interrupt. DRDYE = 0 - Availability of new acceleration data is not reflected as an interrupt. DRDYE = 1 - Availability of new acceleration data is reflected as an interrupt.
GSEL [1:0]	Selects the Acceleration range of KX310CR-MZ outputs. GSEL [1:0] = 0 - Acceleration range is ±2 g. GSEL [1:0] = 1 - Acceleration range is ±4 g. GSEL [1:0] = 2 - Acceleration range is ±8 g. GSEL [1:0] = 3 - Do no set
WUFE	Enables the Wake-up function. WUFE = 0 - Wake-up function is disabled. WUFE = 1 - Wake-up function is enabled.

PC1	HR	Power Mode
0	Do not care	Standby
1	0	Low Power
1	1	High Resolution

Register Map – continued

(19h) CNTL2

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
19h	CNTL2	R/W	SRST	COTC	INT1_OR	INT2_OR	Reserved			

default value 00h

Fields	Function
SRST	Initiates Software Reset, which performs the OTP reboot routine. This bit will remain '1' until the OTP reboot routine is finished with SPI reading. The KX310CR-MZ returns NACK with I^2C reading during the reboot routine. SRST = 0 - No action SRST = 1 - The KX310CR-MZ starts the OTP reboot routine.
COTC	Command test response control bit. COTC = 0 - No action COTC = 1 - COTR register is set to AAh. COTC bit is self-cleared after the COTR reading. (COTR is also returns to 55h)
INT1_OR	Status output (The value of STAT_REG bit) overrides INT1 pin. This function is prioritized over interrupt, and any interrupt setting is ignored if this bit is set to '1'. INT1_OR = 0 - No override INT1_OR = 1 - Status output overrides to INT1 pin
INT2_OR	Status output (The value of STAT_REG bit) overrides INT2 pin. This function is prioritized over interrupt, and any interrupt setting is ignored if this bit is set to '1'. INT2_OR = 0 - No override INT2_OR = 1 - Status output overrides to INT2 pin

(1Ah) CNTL3

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Ah	CNTL3	R/W	Reserved					OWUF [2:0]		

default value 00h

Fields	Function
OWUF [2:0]	Sets the output data rate for the Wake-up and the High-pass filter outputs. The default ODR is 0.781 Hz.

OWUF [2:0]	Output Data Rate
0	0.781 Hz
1	1.563 Hz
2	3.125 Hz
3	6.25 Hz
4	12.5 Hz
5	25 Hz
6	50 Hz
7	100 Hz

Register Map – continued

(1Bh) ODCNTL

This register is responsible for configuring ODR (Output Data Rate) and filter settings. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Bh	ODCNTL	R/W	IIR_BYPASS	LPRO	Reserved		OSA [3:0]			

default value 06h

Fields	Function
IIR_BYPASS	The Low-pass filter bypass mode control IIR_BYPASS = 0 - The Low-pass filter is applied to the accelerometer data path. IIR_BYPASS = 1 - The Low-pass filter is bypassed.
LPRO	The Low-pass filter roll off frequency control LPRO = 0 - The corner frequency of the Low-pass filter is set to ODR/9. LPRO = 1 - The corner frequency of the Low-pass filter is set to ODR/2.
OSA [3:0]	Acceleration output data rate (ODR). The default ODR is 50 Hz for both High Resolution and Low Power Mode. Note that Acceleration ODR setting must be equal to or higher than ODR of enabled engines.

OSA [3:0]	High Resolution Mode Output Data Rate	Low Power Mode Output Data Rate
0	0.781 Hz	0.781 Hz
1	1.563 Hz	1.563 Hz
2	3.125 Hz	3.125 Hz
3	6.25 Hz	6.25 Hz
4	12.5 Hz	12.5 Hz
5	25 Hz	25 Hz
6	50 Hz	50 Hz
7	100 Hz	100 Hz
8	200 Hz	200 Hz
9	400 Hz	400 Hz
10	800 Hz	Do not set
11	1600 Hz	Do not set
12 - 15	Do not set	Do not set

Register Map – continued

(1Ch) INC1

This register controls the settings for the physical interrupt pin and the Self-test polarity and SPI interface mode. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Ch	INC1	R/W	PW [1:0]		IEN1	IEA1	IEL1	PPOD	STPOL	SPI3E

default value 10h

Fields	Function
PW [1:0]	Pulse interrupt width configuration of the physical interrupt pin INT1 and INT2. PW = 0 - 50 µs PW = 1 - OSA period PW = 2 - 2 x OSA period PW = 3 - Reserved
IEN1	Sets the enables/disables of the physical interrupt pin INT1. IEN1 = 0 - The physical interrupt pin INT1 is disabled. IEN1 = 1 - The physical interrupt pin INT1 is enabled.
IEA1	Sets the polarity of the physical interrupt pin INT1. IEA1 = 0 - The polarity of the physical interrupt pin is set to active Low. IEA1 = 1 - The polarity of the physical interrupt pin is set to active High.
IEL1	Sets the response of the physical interrupt pin INT1. IEL1 = 0 - The physical interrupt pin latches until it is cleared by reading INT_REL. IEL1 = 1 - The physical interrupt pin will transmit one pulse with a period of PW.
PPOD	Push-pull/open-drain configuration of the physical interrupt pin INT1 and INT2. PPOD = 0 - INT1 and INT2 are configured to push-pull. PPOD = 1 - INT1 and INT2 are configured to open-drain.
STPOL	Sets the polarity of Self-test. STPOL = 0 - The Self-test polarity is nominal. STPOL = 1 - The Self-test polarity is inverted.
SPI3E	Sets the 3-wire SPI interface. SPI3E = 0 - KX310CR-MZ is set to 4-wire SPI mode. SPI3E = 1 - KX310CR-MZ is set to 3-wire SPI mode.

Register Map – continued

(1Dh) INC2

This register controls which axis and direction of detected motion can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Dh	INC2	R/W	Reserved	AOI	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE

default value 3Fh

Fields	Function
AOI	AND-OR configuration on Wake-up and Wake-up2 detection AOI = 0 - OR combination between selected axes AOI = 1 - AND combination between selected axes Ex. In case all directions are enabled, Active state in OR configuration = (XN || XP || YN || YP || ZN || ZP) Active state in AND configuration = (XN || XP) & (YN || YP) & (ZN || ZP)
XNWUE	Enable/Disable direction of Wake-up and Wake-up2 function. XNWUE = 0 - X negative (XN) is disabled. XNWUE = 1 - X negative (XN) is enabled.
XPWUE	Enable/Disable direction of Wake-up and Wake-up2 function. XPWUE = 0 - X positive (XP) is disabled. XPWUE = 1 - X positive (XP) is enabled.
YNWUE	Enable/Disable direction of Wake-up and Wake-up2 function. YNWUE = 0 - Y negative (YN) is disabled. YNWUE = 1 - Y negative (YN) is enabled.
YPWUE	Enable/Disable direction of Wake-up and Wake-up2 function. YPWUE = 0 - Y positive (YP) is disabled. YPWUE = 1 - Y positive (YP) is enabled.
ZNWUE	Enable/Disable direction of Wake-up and Wake-up2 function. ZNWUE = 0 - Z negative (ZN) is disabled. ZNWUE = 1 - Z negative (ZN) is enabled.
ZPWUE	Enable/Disable direction of Wake-up and Wake-up2 function. ZPWUE = 0 - Z positive (ZP) is disabled. ZPWUE = 1 - Z positive (ZP) is enabled.

(1Fh) INC4

This register controls the settings for the physical interrupt pin INT1. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Fh	INC4	R/W	Reserved			DRDYI1	BTSI1	Reserved	WUFI1	Reserved

default value 00h

Fields	Function
DRDYI1	DRDYI1 = 0 - Data ready interrupt is not reported on physical interrupt pin INT1. DRDYI1 = 1 - Data ready interrupt is reported on physical interrupt pin INT1.
BTSI1	BTSI1 = 0 - Back-to-sleep interrupt is not reported on physical interrupt pin INT1. BTSI1 = 1 - Back-to-sleep interrupt is reported on physical interrupt pin INT1.
WUFI1	WUFI1 = 0 - Wake-up interrupt is not reported on physical interrupt pin INT1. WUFI1 = 1 - Wake-up interrupt is reported on physical interrupt pin INT1.

Register Map – continued

(20h) INC5

This register controls the settings for the physical interrupt pin and nCS pin pull-up. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
20h	INC5	R/W	Reserved	NCS_PU_OFF	IEN2	IEA2	IEL2	ACLR2	ACLR1	Reserved

default value 10h

Fields	Function
NCS_PU_OFF	Disconnect pull-up of nCS pin. nCS pin is internally pulled-up in default status. NCS_PU_OFF = 0 - nCS pin is internally pulled-up. NCS_PU_OFF = 1 - nCS pin is not internally pulled-up.
IEN2	Enables/disables the physical interrupt pin INT2. IEN2 = 0 - The physical interrupt pin INT2 is disabled. IEN2 = 1 - The physical interrupt pin INT2 is enabled.
IEA2	Sets the polarity of the physical interrupt pin INT2. IEA2 = 0 - The polarity of the physical interrupt pin is set to active Low. IEA2 = 1 - The polarity of the physical interrupt pin is set to active High.
IEL2	Sets the response of the physical interrupt pin INT2. IEL2 = 0 - The physical interrupt pin latches until it is cleared by reading INT_REL. IEL2 = 1 - The physical interrupt pin will transmit one pulse with a period of PW.
ACLR2	Enables/disables INT2 auto interrupt status clear for motion detect function. ACLR2 = 0 - Latched interrupt is not automatically cleared, and pulse interrupt is not generated if it has already asserted. Read INT_REL register to clear the status. ACLR2 = 1 - Latched interrupt is automatically cleared, and pulse interrupt is generated for each event.
ACLR1	Enables/disables INT1 auto interrupt status clear for motion detect function. ACLR1 = 0 - Latched interrupt is not automatically cleared, and pulse interrupt is not generated if it has already asserted. Read INT_REL register to clear the status. ACLR1 = 1 - Latched interrupt is automatically cleared, and pulse interrupt is generated for each event.

(21h) INC6

This register controls the settings for the physical interrupt pin. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
21h	INC6	R/W	Reserved			DRDYI2	BTSI2	Reserved	WUFI2	Reserved

default value 00h

Fields	Function
DRDYI2	DRDYI2 = 0 - Data ready interrupt is not reported on physical interrupt pin INT2. DRDYI2 = 1 - Data ready interrupt is reported on physical interrupt pin INT2.
BTSI2	BTSI2 = 0 - Back-to-sleep interrupt is not reported on physical interrupt pin INT2. BTSI2 = 1 - Back-to-sleep interrupt is reported on physical interrupt pin INT2.
WUFI2	WUFI2 = 0 - Wake-up interrupt is not reported on physical interrupt pin INT2. WUFI2 = 1 - Wake-up interrupt is reported on physical interrupt pin INT2.

Register Map – continued

(23h) WUFC

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
23h	WUFC	R/W	WUFC [7:0]							

default value 00h

Fields	Function
WUFC [7:0]	This register is the initial count register for the Wake-up detection timer. Every count is calculated as 1/ODR delay period, where the ODR is user-defined. A new state must be valid as many measurement periods before the change is accepted.

(2Ch) MAN_WAKE

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Ch	MAN_WAKE	W	Reserved		MAN_WAKE2	MAN_SLEEP2	Reserved		MAN_WAKE	MAN_SLEEP

default value 00h

Fields	Function
MAN_WAKE2	Manual wake/sleep engine override MAN_WAKE2 = 0 - No action MAN_WAKE2 = 1 - The WUF2/BTS2 is forced to Wake state. (The MAN_WAKE2 bit is self-cleared)
MAN_SLEEP2	Manual wake/sleep engine override MAN_SLEEP2 = 0 - No action MAN_SLEEP2 = 1 - The WUF2/BTS2 is forced to Sleep state. (The MAN_SLEEP2 bit is self-cleared)
MAN_WAKE	Manual wake/sleep engine override MAN_WAKE = 0 - No action MAN_WAKE = 1 - The WUF/BTS is forced to Wake state. (The MAN_WAKE bit is self-cleared)
MAN_SLEEP	Manual wake/sleep engine override MAN_SLEEP = 0 - No action MAN_SLEEP = 1 - The WUF/BTS is forced to Sleep state. (The MAN_SLEEP bit is self-cleared)

Register Map – continued

(2Dh) BTS_CNTL

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	BTS_CNTL	R/W	BTSE	0	BTS_RES [2:0]			OBTS [2:0]		

default value 00h

Fields	Function
BTSE	Enables the Back-to-sleep function. BTSE = 0 - Back-to-sleep function is disabled. BTSE = 1 - Back-to-sleep function is enabled.
BTS_RES [2:0]	Determines the Back-to-sleep counter resolution. For detail, see the BTSC description.
OBTS [2:0]	Sets the output data rate for the Back-to-sleep and the High-pass filter outputs. The default ODR is 0.781 Hz.

OBTS [2:0]	Output Data Rate
0	0.781 Hz
1	1.563 Hz
2	3.125 Hz
3	6.25 Hz
4	12.5 Hz
5	25 Hz
6	50 Hz
7	100 Hz

Register Map – continued

(2Eh) BTSC

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Eh	BTSC	R/W	BTSC [7:0]							

default value 00h

Fields	Function
BTSC [7:0]	This register is the initial count register for the Back-to-sleep detection timer. Every count is calculated as (1/ODR)x2$^{(BTS_RES)}$ delay period, where the ODR and BTS_RES are user-defined. A new state must be valid as many measurement periods before the change is accepted.

(2Fh-31h) BTS_TH, WUF_TH, BTS_WUF_TH

Note that to properly change the value of these registers, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	BTS_TH	R/W	BTSTH [7:0]							

default value 80h

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
30h	WUF_TH	R/W	WUFTH [7:0]							

default value 80h

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
31h	BTS_WUF_TH	R/W	Reserved	BTSTH [10:8]			Reserved	WUFTH [10:8]		

default value 00h

Fields	Function
BTSTH [10:0]	This register sets the threshold for the Back-to-sleep function. KX310CR-MZ will ship from the factory with this value set to correspond to a change in acceleration of 0.5 g.

Fields	Function
WUFTH [10:0]	This register sets the threshold for the Wake-up function. KX310CR-MZ will ship from the factory with this value set to correspond to a change in acceleration of 0.5 g.

Register Map – continued

(35h) LP_CNTL

Low Power Control sets the number of samples of accelerometer output to be averaged. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
35h	LP_CNTL	R/W	1	AVC [2:0]			0	0	1	1

default value C3h

Fields	Function
AVC [2:0]	Averaging Filter Control in Low Power Mode, the default setting is 16 samples averaged.

AVC [2:0]	Number of Averaging
0	Do not set
1	2 Samples Averaged
2	4 Samples Averaged
3	8 Samples Averaged
4	16 Samples Averaged
5	32 Samples Averaged
6	64 Samples Averaged
7	128 Samples Averaged

(40h-42h) WUF_TH2, BTS_WUF_TH2, BTS_TH2

Note that to properly change the value of these registers, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
40h	WUF_TH2	R/W	WUFTH2 [7:0]							

default value 80h

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
41h	BTS_WUF_TH2	R/W	Reserved	BTSTH2 [10:8]			Reserved	WUFTH2 [10:8]		

default value 00h

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
42h	BTS_TH2	R/W	BTSTH2 [7:0]							

default value 80h

Fields	Function
BTSTH2 [10:0]	This register sets the threshold for the Back-to-sleep2 function. KX310CR-MZ will ship from the factory with this value set to correspond to a change in acceleration of 0.5 g.

Fields	Function
WUFTH2 [10:0]	This register sets the threshold for the Wake-up2 function. KX310CR-MZ will ship from the factory with this value set to correspond to a change in acceleration of 0.5 g.

Register Map – continued

(43h) WUFC2

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
43h	WUFC2	R/W	WUFC2 [7:0]							

default value 00h

Fields	Function
WUFC2 [7:0]	This register is the initial count register for the Wake-up2 detection timer. Every count is calculated as 1/ODR delay period, where the ODR is user-defined. A new state must be valid as many measurement periods before the change is accepted.

(44h) BTSC2

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
44h	BTSC2	R/W	BTSC2 [7:0]							

default value 00h

Fields	Function
BTSC2 [7:0]	This register is the initial count register for the Back-to-sleep2 detection timer. Every count is calculated as $(1/ODR)x2^{(BTS\_RES2)}$ delay period, where the ODR and BTS_RES2 are user-defined. A new state must be valid as many measurement periods before the change is accepted.

Register Map – continued

(45h) BTS_WUF_CNTL1

Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
45h	BTS_WUF_CNTL1	R/W	WUFE2	BTSE2	OWUF2 [2:0]			OBTS2 [2:0]		

default value 00h

Fields	Function
WUFE2	Enables the Wake-up2 function. WUFE2 = 0 - Wake-up2 function is disabled. WUFE2 = 1 - Wake-up2 function is enabled.
BTSE2	Enables the Back-to-sleep2 function. BTSE2 = 0 - Back-to-sleep2 function is disabled. BTSE2 = 1 - Back-to-sleep2 function is enabled.
OWUF2 [2:0]	Sets the output data rate for the Wake-up2 function. The default ODR is 0.781 Hz.
OBTS2 [2:0]	Sets the output data rate for the Back-to-sleep2 function. The default ODR is 0.781 Hz.

OWUF2 [2:0]	Output Data Rate
0	0.781 Hz
1	1.563 Hz
2	3.125 Hz
3	6.25 Hz
4	12.5 Hz
5	25 Hz
6	50 Hz
7	100 Hz

OBTS2 [2:0]	Output Data Rate
0	0.781 Hz
1	1.563 Hz
2	3.125 Hz
3	6.25 Hz
4	12.5 Hz
5	25 Hz
6	50 Hz
7	100 Hz

Register Map – continued

(46h) BTS_WUF_CNTL2

This register controls Wake-up and Back-to-sleep engine mode. Note that to properly change the value of this register, the PC1 bit in CNTL1 must first be set to '0'.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
46h	BTS_WUF_CNTL2	R/W	0	TH_MODE	C_MODE_BTS	C_MODE_WUF	BTS_RES2 [2:0]			1

default value 41h

Fields	Function
TH_MODE	Determines the threshold mode of Wake-up, Wake-up2, Back-to-sleep and Back-to-sleep2 function. TH_MODE = 0 - Engine is set to absolute threshold mode. TH_MODE = 1 - Engine is set to relative threshold mode.
C_MODE_BTS	Determines the Back-to-sleep and Back-to-sleep2 counter mode. C_MODE_BTS = 0 - The engine counters are set to count up/reset. C_MODE_BTS = 1 - The engine counters are set to count up/down.
C_MODE_WUF	Determines the Wake-up and Wake-up2 function counter mode. C_MODE_WUF = 0 - The engine counters are count up/reset. C_MODE_WUF = 1 - The engine counters are count up/down.
BTS_RES2 [2:0]	Determines the Back-to-sleep2 counter resolution. For detail, see the BTSC2 description.

(60h) SELFTEST

Self-test Enable register.

Register Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
60h	SELFTEST	W	SELFTEST [7:0] (activation key = CAh)							

Fields	Function
SELFTEST [7:0]	Writing activation key (CAh) causes the KX310CR-MZ into the Self-test mode. Writing 00h causes the KX310CR-MZ back to the normal mode.

To perform the Self-test, the following procedure is required:

(1) Set PC1 bit to '0' in CNTL1 register to disable KX310CR-MZ.
(2) Write CAh to this register to enable the Self-test function.
(3) Set PC1 bit to '1' in CNTL1 register to enable KX310CR-MZ.

Once the Self-test function is enabled, electrostatic actuation of the accelerometer, results in a DC shift of the X, Y and Z axis outputs. Calculate the Self-test (ST) response.

ST [g] = | ((OUTPUT_ST_ON [counts]) - (OUTPUT_ST_OFF [counts])) | / Sensitivity [counts/g]

The Self-test response should be compared to the product specifications to determine if the MEMS response is within the specified range (see the Electrical Characteristic table). To disable the Self-test mode, any of the following methods can be used:

(1) Power Cycle KX310CR-MZ.
(2) Perform Software Reset by setting SRST bit to 1 in CNTL2 register.
(3) Set PC1 bit to 0 in CNTL1 register, then write 00h to this register.

Motion Interrupt

KX310CR-MZ features an advanced threshold interrupt by the internal motion detect function. These engines allow the KX310CR-MZ to trigger interrupts when accelerometer activity falls below a defined threshold window (Back-to-sleep and Back-to-sleep2 events) or exceeds a threshold window (Wake-up and Wake-up2 events). Note that this function only generates an interrupt and does not trigger any changes to the part configuration (e.g. power mode, ODR, etc.). KX310CR-MZ has 2 sets of motion detection engines (WUF/BTS and WUF2/BTS2) , and these can be configured with independently.

1. Enabling/Disabling

The Wake-up and Back-to-sleep detection can be enabled/disabled using WUFE/WUFE2 and BTSE/BTSE2 bits and the direction of motion detection can be set for any axis in INC2 register.

2. Debounce Counter

The Motion engines have an internal debounce counter to qualify motion status detection. The debounce counter function can be set by using either C_MODE_BTS or C_MODE_WUF bits. The counter can be configured to either reset or decrement itself if accelerometer data has either fallen below or risen above the threshold for motion detect functionality respectively. Note that each Wake-up Function counter (WUFC/WUFC2) count qualifies 1 (one) user-defined Wake-up function ODR period as set by OWUF/OWUF2 bit. The Back-to-sleep count qualifies 2^{BTS_RES} or 2^{BTS_RES2} user-defined ODR period as set by OBTS/OBTS2 bit. The Back-to-sleep counter has resolution setting which is BTS_RES/BTS_RES2 bits. Following equation shows how to calculate the WUFC/WUFC2 and BTSC/BTSC2 register values for a desired Wake-up and Back-to-sleep delay times.

WUFC (counts) = Wake-up delay time (s) x Wake-up function ODR (Hz)
WUFC2 (counts) = Wake-up delay time (s) x Wake-up function2 ODR (Hz)
BTSC (counts) = Back-to-sleep delay time (s) x Back-to-sleep function ODR (Hz) / $2^{\text{Back-to-sleep Counter resolution}}$
BTSC2 (counts) = Back-to-sleep delay time (s) x Back-to-sleep2 function ODR (Hz) / $2^{\text{Back-to-sleep2 Counter resolution}}$

3. Threshold Resolution

The motion interrupt threshold values are set by WUFTH/WUFTH2 [10:0] and BTSTH/BTSTH2 [10:0] bits. This threshold is compared with MSB 11 bits of 8 g output, and not related to acceleration range setting configured by the GSEL [1:0] bits. The following equation shows threshold resolution.

2048 counts/8 g = 256 counts/g or 3.9 mg/counts.

4. Relative/Absolute Threshold Mode Select

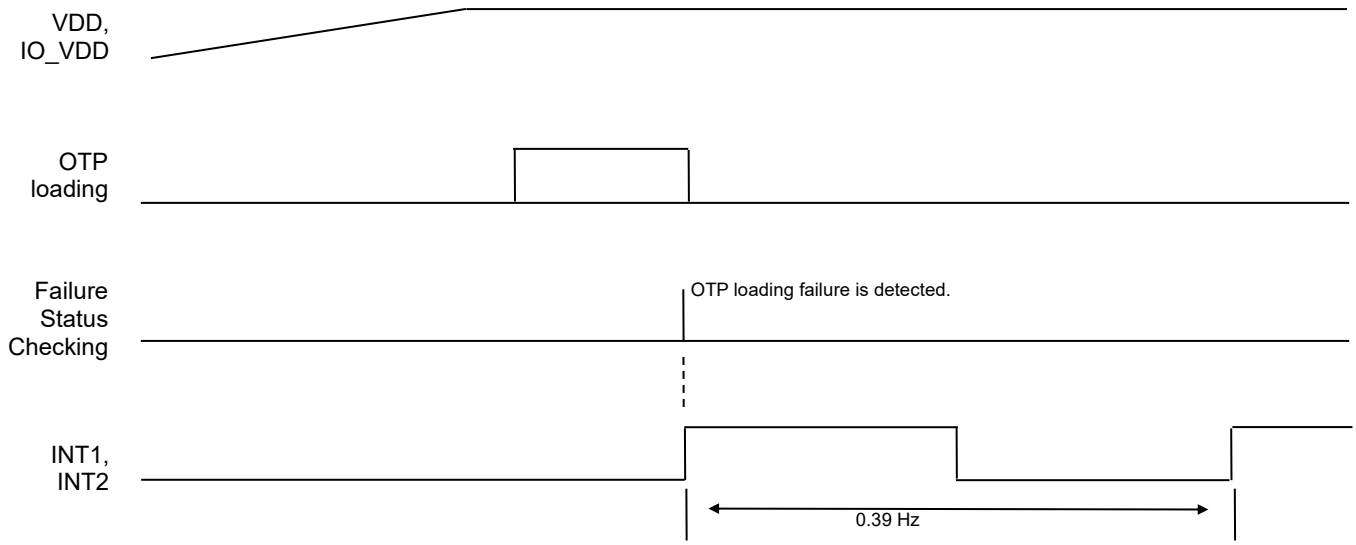
The type of threshold used for motion interrupt is controlled using TH_MODE bit. The threshold can be set to either an absolute acceleration value or a relative acceleration value. In case the relative threshold mode is selected, the threshold value is compared with gap between current and previous acceleration data. In case the absolute threshold mode is selected, the threshold value is compared with current acceleration data.

Failure Report Function

KX310CR-MZ has 2 failure report function which are routed on INT1 and INT2, and the failure is also reported on the CRC_F and PARITY_F bits in the STATUS_REG. Note that the failure report function is prioritized than interrupt function and status override function.

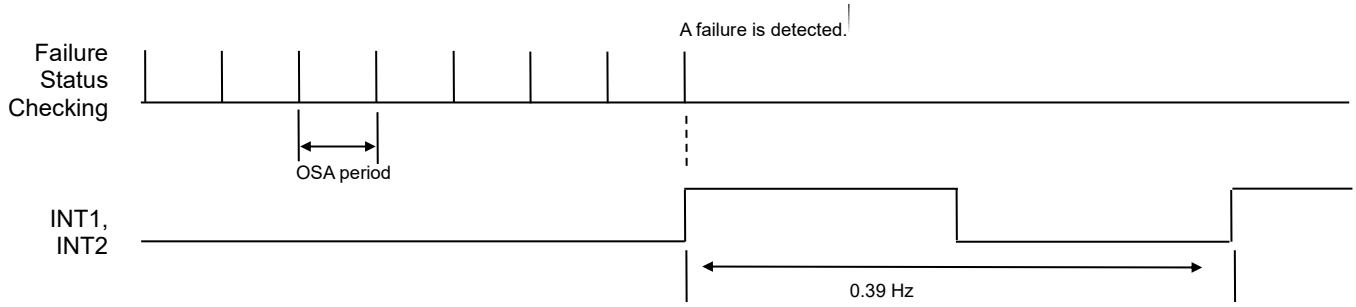
1. OTP load failure

When the failure is detected, the CRC_F bit is set and INT1 and INT2 pins toggle with 0.39 Hz. Perform Software Reset or Power Cycle the device at that case. The failure checking is done only when the device is Power Cycled or Software Reset is initiated. Note KX310CR-MZ is forced to Standby mode if this failure is detected even if the PC1 bit is set.



2. Internal register parity failure

When the failure is detected, the PARITY_F bit is set and INT1 and INT2 pins toggle with 0.39 Hz. Perform Software Reset or Power Cycle the device at that case. This report function is only available with either High Resolution or Low Power Mode. The failure checking is done every OSA cycle.



Typical Performance Curves

(Reference data)

(Unless otherwise specified V_{IO_VDD} = 3.0 V, V_{VDD} = 3.0 V and Ta = 25 °C)

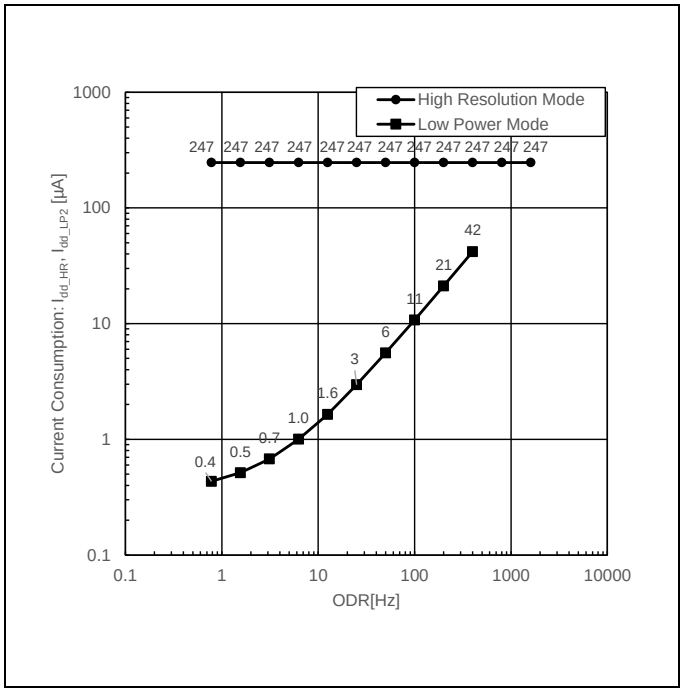


Figure 1. Current Consumption vs ODR

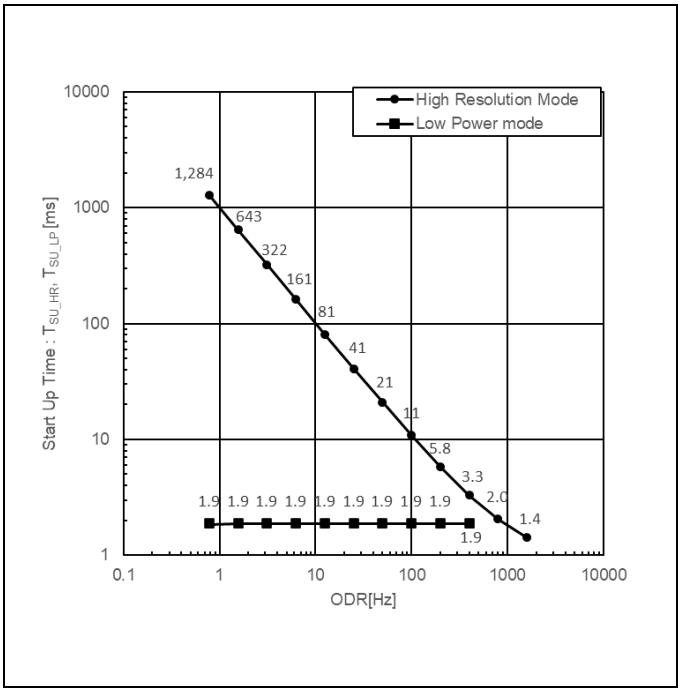
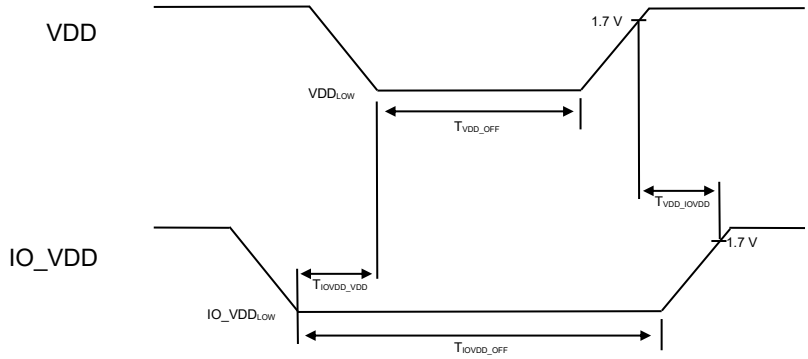


Figure 2. Start Up Time vs ODR

Power On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific power supply profile of individual applications. It is recommended to minimize IO_VDD_{LOW} and VDD_{LOW}, and maximize $T_{IO\_VDD\_OFF}$ and T_{VDD_OFF}. It is also advised that the IO_VDD and VDD ramp up time be monotonic. To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{LOW}, T_{VDD_OFF} and temperature. Bench Testing has demonstrated POR performance regions for a proper POR trigger.



(Unless otherwise specified V_{VDD} = 3.0 V, V_{IO_VDD} = 3.0 V and Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VDD off time	T_{VDD_OFF}	20	-	-	ms	
IO_VDD off time	$T_{IO\_VDD\_OFF}$	20	-	-	ms	
VDD low voltage	VDD_{LOW}	-	-	200	mV	
IO_VDD low voltage	IO_VDD_{LOW}	-	-	200	mV	
IO_VDD low to VDD low time	T_{IOVDD_VDD}	0	-	-	ms	
VDD high to IO_VDD high time	T_{VDD_IOVDD}	0	-	-	ms	

(Note) VDD and IO_VDD must always be monotonic ramps without ambiguous state.

The V_{IO_VDD} must remain ≤ V_{VDD}.

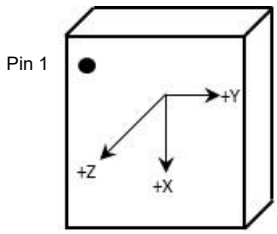
In order to prevent entering an ambiguous state, both VDD and IO_VDD need to be pulled down to GND (≤ 200 mV) for duration of time ≥ 20 ms.

The Power-up time is specified in the Electrical Characteristics table.

It is important the user determines the timing ($T_{IO\_VDD\_OFF}$ and T_{VDD_OFF}) and threshold (IO_VDD_{LOW} and VDD_{LOW}) levels by evaluating the performance in the specific system for which the device will be incorporated.

Orientation

When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.



Static X/Y/Z Output Response versus Orientation to Earth's surface with GSEL [1:0] = 0 (Acceleration Range: ±2 g)

Position	1	2	3	4	5	6
Diagram	Earth's surface	Earth's surface	Earth's surface	Earth's surface	Top / Bottom / Earth's surface	Bottom / Top / Earth's surface
X (counts)	-16384	0	0	+16384	0	0
Y (counts)	0	+16384	-16384	0	0	0
Z (counts)	0	0	0	0	+16384	-16384

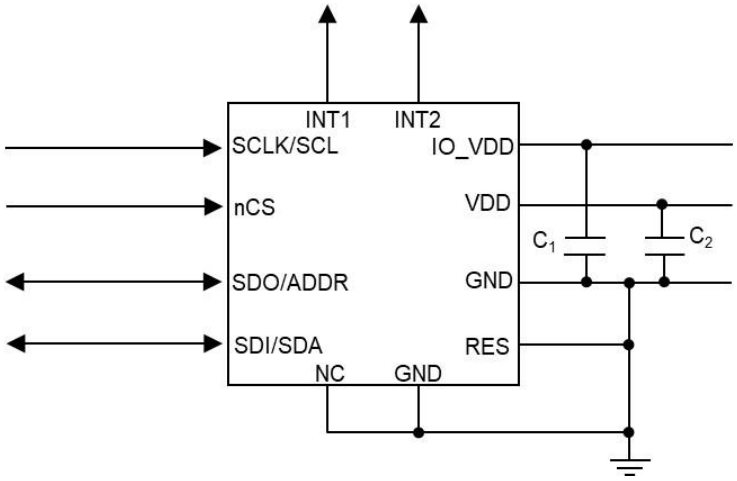
Static X/Y/Z Output Response versus Orientation to Earth's surface with GSEL [1:0] = 1 (Acceleration Range: ±4 g)

Position	1	2	3	4	5	6
Diagram	Earth's surface	Earth's surface	Earth's surface	Earth's surface	Top / Bottom / Earth's surface	Bottom / Top / Earth's surface
X (counts)	-8192	0	0	+8192	0	0
Y (counts)	0	+8192	-8192	0	0	0
Z (counts)	0	0	0	0	+8192	-8192

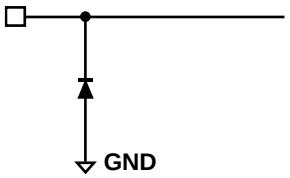
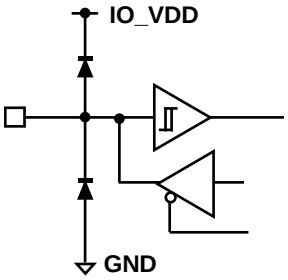
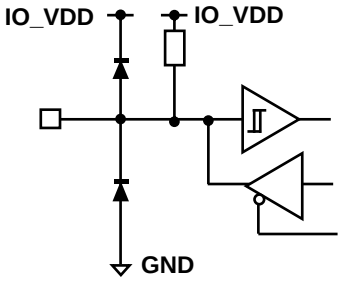
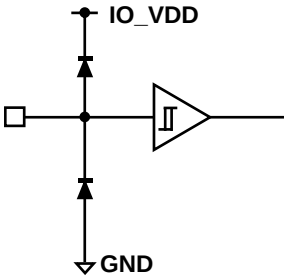
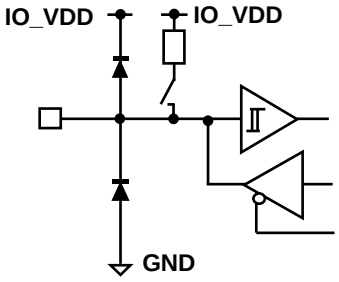
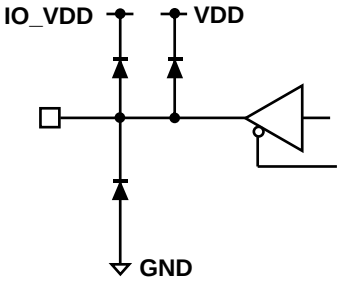
Static X/Y/Z Output Response versus Orientation to Earth's surface with GSEL [1:0] = 2 (Acceleration Range: ±8 g)

Position	1	2	3	4	5	6
Diagram	Earth's surface	Earth's surface	Earth's surface	Earth's surface	Top / Bottom / Earth's surface	Bottom / Top / Earth's surface
X (counts)	-4096	0	0	+4096	0	0
Y (counts)	0	+4096	-4096	0	0	0
Z (counts)	0	0	0	0	+4096	-4096

Application Example



I/O Equivalence Circuits

Pin Name	Equivalence Circuit	Pin Name	Equivalence Circuit
VDD IO_VDD		SDI/SDA	
SDO/ADDR		SCLK/SCL RES	
nCS		INT1 INT2	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

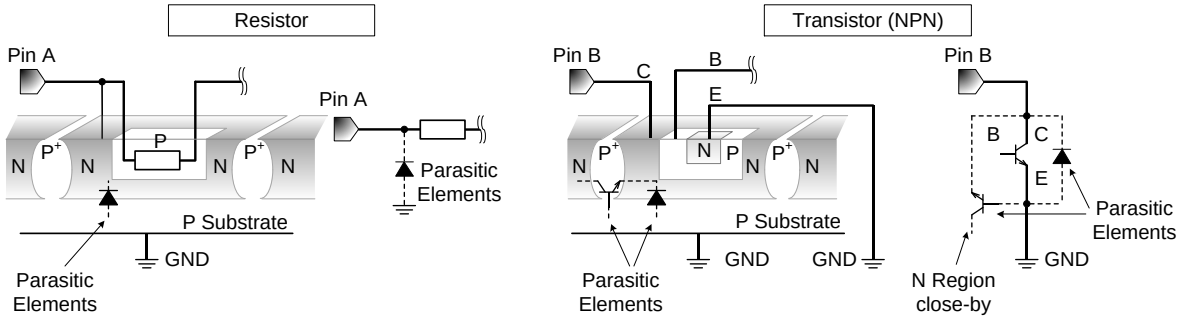


Figure 3. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

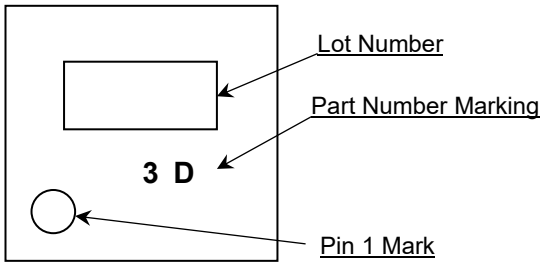
K X 3 1 0 C R	-	MZ E2

Part Number

Product Rank
M: for Automotive
Packaging and forming specification
Z: Outsourced package
E2: Embossed tape and reel

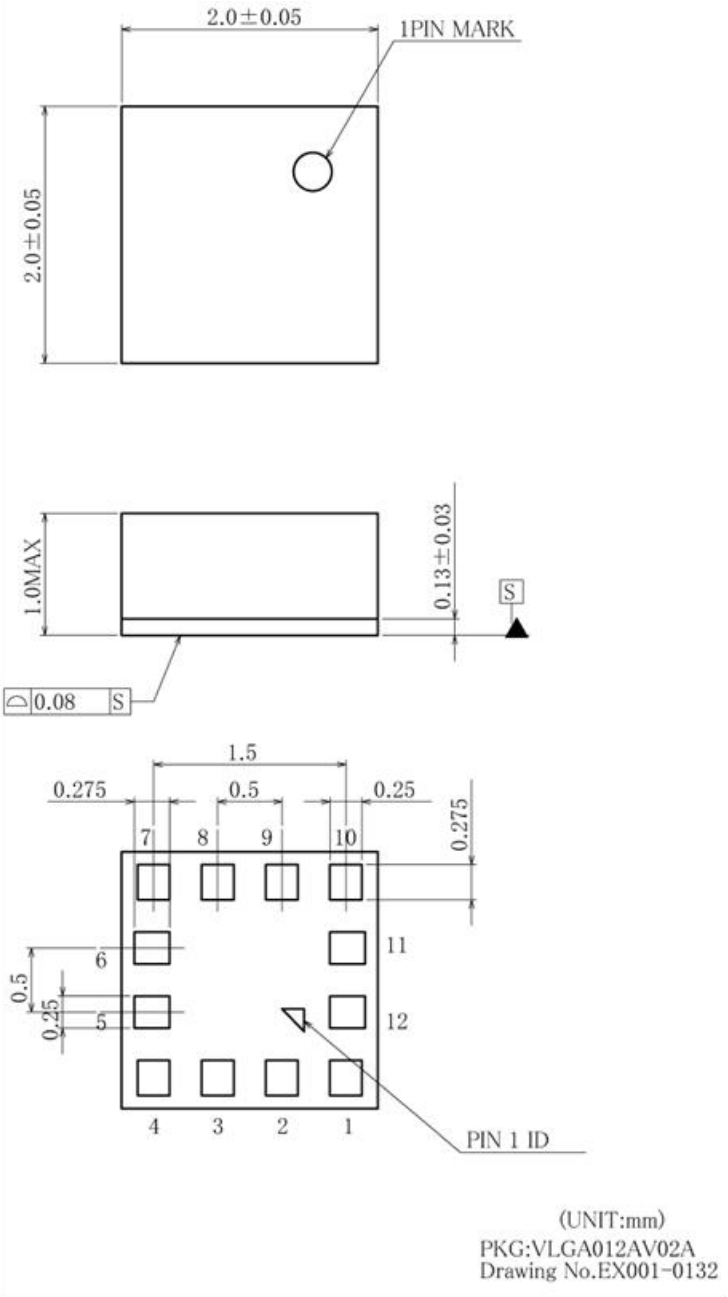
Marking Diagram

VLGA012AV02A
(TOP VIEW)



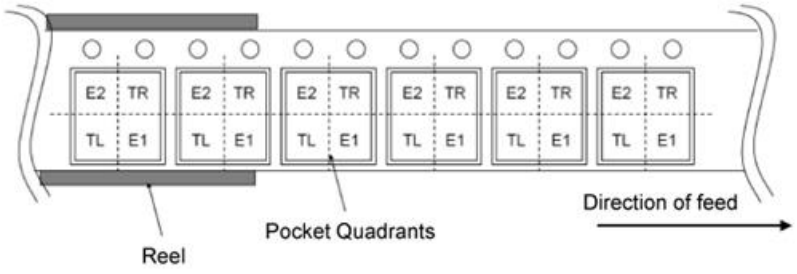
Physical Dimension and Packing Information

Package Name	VLGA012AV02A



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	10000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
26.Mar.2024	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.