

Magnetic Sensor Series Current Sensor IC

BM14270AMUV-LB

General Description

This is the product guarantees long time support in industrial market.

BM14270AMUV-LB is coreless non-contact type current sensor of the magnetic detection using MI sensor. It's possible to measure the current line in non-contact, and therefore it's possible to measure current without loss.

Features

- Long Time Support Product for Industrial Applications
- Current Sensor using MI Element
- I²C Interface
- 14bit Digital Output

Applications

- Industrial Equipment
- Meter for the Power Measurement
- UPS
- Power Conditioner

Key Specifications

) epochicanone	
Input Voltage Range:	2.7 V to 5.5 V
Operating Current (20 SPS):	70 µA(Typ)
Magnetic Measurable Range:	±280 µT(Typ)

- Magnetic Measurable Range: ±280 μ1(1yp)
 Magnetic Sensitivity: 0.045 μT/LSB(Typ)
- Operating Temperature Range: -40 °C to +125 °C
- Operating temperature Range. -40 C to +12

Package

VQFN20QV3535

W(Typ) x D(Typ) x H(Max) 3.50 mm x 3.50 mm x 1.00 mm



Typical Application Circuit and Block Diagram



OProduct structure : Silicon integrated circuit OThis product has no designed protection against radioactive rays

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Pin Configuration



Pin Description

Pin No.	Pin Name	Function
1	NC	No connection (Set to open)
2	NC	No connection (Set to open)
3	NC	No connection (Set to open)
4	NC	No connection (Set to open)
5	NC	No connection (Set to open)
6	NC	No connection (Set to open)
7	VDD	Power supply ^(Note 1)
8	GND	Ground
9	VREG	Internal regulator output ^(Note 2)
10	TEST	Test pin ^(Note 3)
11	NC	No connection (Set to open)
12	NC	No connection (Set to open)
13	NC	No connection (Set to open)
14	NC	No connection (Set to open)
15	NC	No connection (Set to open)
16	ALERT	ALERT output pin
17	SCL	I ² C signal clock input
18	SDA	I ² C signal data I/O
19	ADDR	I ² C programmable address bit ^(Note 4)
20	NC	No connection (Set to open)
-	EXP-PAD	The EXP-PAD connect to GND or floating

(Note 1) Dispose a bypass capacitor between VDD and GND as close as possible to the IC. (Note 2) Dispose a bypass capacitor between VREG and GND as close as possible to the IC. Set a bypass capacitor of 0.22 μF between VREG and GND.

(Note 3) Connect to GND. (Note 4) Connect to VDD or GND.

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{DD}	7.0	V
Input Voltage	V _{IN}	-0.3 to V _{DD} +0.3	V
Storage Temperature Range	Tstg	-40 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
Maximum Exposed Field	Mef	-1000 to +1000	mT

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 5)

Derometer	Sumbol	Thermal Res	Linit		
Parameter	Symbol	1s ^(Note 7)	2s2p ^(Note 8)	Unit	
VQFN20QV3535				1	
Junction to Ambient	θ _{JA}	181.9	50.5	°C/W	
Junction to Top Characterization Parameter ^(Note 6)	Ψ_{JT}	19	7	°C/W	

(Note 5) Based on JESD51-2A(Still-Air).

(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 7)	Using a	PCB	board	based	on .	JESD51-	З.	
(1040 0)	I laina a		le e e e el	In			-	-

(Note 8) Using a PCB board based o	on JESD51-5, 7.					
	Layer Number of Measurement Board	Material	Board Size				
	Single	FR-4	114.3 mm x 76.2 mm >	< 1.57 mmt			
ſ	Тор						
	Copper Pattern	Thickness					
	Footprints and Traces	70 µm					
ſ	Layer Number of	Motorial	Poord Sizo		Thermal \	/ia ^{(Noi}	te 9)
	Measurement Board	Ivialentai	Dualu Size		Pitch	0	Diameter
	4 Layers	FR-4	114.3 mm x 76.2 mm	x 1.6 mmt	1.20 mm	Φ	0.30 mm
ſ	Тор		2 Internal Layers		Botto	om	
	Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	۱	Thickness
ſ	Footprints and Traces	70 µm	74.2 mm x 74.2 mm 35 μm 74.2 mm x 74.2 mm		nm	70 µm	

(Note 9) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage	V _{DD}	2.7	5.0	5.5	V
I ² C Clock Frequency	f _{SCL}	-	-	400	kHz
Operating Temperature	Topr	-40	+25	+125	°C

Magnetic, Electrical Characteristics (Unless otherwise specified V_{DD}=5.0 V Ta=25 °C)

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Current Consumption	1	1	1	L	L	
Operating Average Current	I _{DD}	-	70	140	μA	Output Data Rate = 20 SPS
Power Down Mode Current	I _{SS}	-	5	10	μA	ALL Power Down
Logic						
Low-level Input Voltage	VIL	GND	-	0.3 x V _{DD}	V	
High-level Input Voltage	VIH	0.7 x V _{DD}	-	V_{DD}	V	
Low-level Input Current	١L	-10	-	0	μA	V _{IL} = GND
High-level Input Current	IIH	0	-	10	μA	$V_{IH} = V_{DD}$
Low-level Output Voltage	V _{OL}	GND	-	0.2 x V _{DD}	V	$I_{LOAD} = -0.3 \text{ mA}$
High-level Output Voltage	V _{OH}	0.8 x V _{DD}	-	V_{DD}	V	$I_{LOAD} = 0.3 \text{ mA}$
Serial Communication						
Low-level Input Current	I _{IL2}	-10	-	0	μA	$V_{IL} = GND$
High-level Input Current	I _{IH2}	0	-	10	μA	At HiZ, $V_{IH} = V_{DD}$
Low-level Output Voltage	V _{OL2}	GND	-	0.2 x V _{DD}	V	$I_{LOAD} = -3 \text{ mA}$
Magnetic Sensor	1					
Measurable Range	R _M	-	±280	-	μΤ	
Linearity ^(Note 10)	L _{IN}	-	0.5	2	%FS	
Output Offset	V _{OFS}	-	0	-	LSB	
Magnetic Sensitivity	D _{ELTAV}	-	0.045	-	μT/ LSB	
Measurement Time	t _{MS}	-	0.35	-	ms	

(Note 10) Linearity = Output Error / R_M = (output – ideal output) / R_M

Example of the Current Measurement Configuration

This product has two different sensors of the magnetic field detection direction. It is configuration to output difference of the magnetic field which two sensors detected. (Out = A - B)



Figure 1. Sensor Configuration

This product locates on the board pattern such as follows, then the magnetic field of the different direction is applied to two sensors and can detect magnetic field depending on current. In addition, the disturbance magnetic field is applied to the same direction for two sensors, and can cancel disturbance magnetic field in the operating range.



Figure 2. Example of the Board Pattern





Typical Performance Curves

(Unless otherwise specified, V_{DD} = 5.0 V, GND = 0.0 V, Ta = 25 °C)



Figure 4. Power Down Mode Current vs Supply Voltage

Figure 5. Operating Average Current vs Supply Voltage (20 SPS)



Figure 6. Operating Average Current vs ODR

I²C Bus Timing Characteristics (Unless otherwise specified $V_{DD} = 5.0$ V, Ta = 25 °C)



Parameter	Symbol	Min	Тур	Max	Unit	Conditions
SCL Clock Frequency	f _{SCL}	0	-	400	kHz	
'L' Period of the SCL Clock	t _{LOW}	1.3	-	-	μs	
'H' Period of the SCL Clock	t _{HIGH}	0.6	-	-	μs	
Setup Time for Repeated START Condition	t _{SU;STA}	0.6	-	-	μs	
Hold Time (Repeated) START Condition	t _{HD;STA}	0.6	-	-	μs	
Data Setup Time	t _{SU;DAT}	100	-	-	ns	
Data Hold Time	t _{HD;DAT}	0	-	-	μs	
Setup Time for STOP Condition	t _{SU;STO}	0.6	-	-	μs	
Bus Free Time between a STOP and START Condition	t _{BUF}	1.3	-	-	μs	

I²C Bus Communication

1. Main write format

(1) Indicate register address

S	Slave Address	W 0	ACK	Indicate register address	ACK	Ρ
---	---------------	--------	-----	---------------------------	-----	---

(2) Write to data register after indicating register address

S	Slave Address	W 0	ACK	Indic	ate register address	ACK		
	Data specified at register address field	ACK		ACK	Data specified at rea address field + I	gister N	ACK	Р

2. Main read format

(1) Read data after indicate register address

()								
S	Slave Address W 0		ACK	Indicate register address		ACK		
S	Slave Address	R 1	ACK	ACK Data specified at regis address field		ACK		
	Data specified at register address field + 1 ACK			ACK	ACK Data specified at register address field + N		NACK	Ρ
(2) Read data from the specified register								
S	Slave Address	R 1	ACK	ACK Data specified at register address field ACK				
Data specified at register address field + 1 ACK			ACK	Data specified at rea address field + I	gister N	NACK	Ρ	
	from master to slave from slave to master							

I²C Bus Slave Address

Selectable 2 I²C Slave Addresses by setting ADRR pin (ADDR=L: 0001110, ADDR=H: 0001111)

Register Map^(Note 11)

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x0F	STA1	R	RD_ DRDY	0	0	0	0	0	0	0
0x10	DATA	R				DATA	A [7:0]			
0x11	DATA	R				DATA	[15:8]			
0x1B	CNTL1	RW	PC1	0	RST_ LV	ODR	[1:0]	0	FS1	0
0x1C	CNTL2	RW	0	0	0	0	ALERT _EN	0	0	0
0x1D	CNTL3	RW	0	FORCE	0	0	0	0	0	0
0x5C		W				RSTB_	LV [7:0]			
0x5D	CIVIL+	W				RSTB_I	V [15:8]			

(Note 11) Do not write any commands to other addresses except above. Do not write '1' to the fields in which value is '0' in above table.

It is the following conditions to be able to access each register.

Condition	Accessible Register
Supply Power	CNTL1 CNTL4
Supply Power (CNTL1) PC1=1 (CNTL1) RST_LV=0 (CNTL4) RSTB_LV=1	STA1 CNTL2 CNTL3
Supply Power (CNTL1) PC1=1 (CNTL1) RST_LV=0 (CNTL4) RSTB_LV=1 (CNTL3) FORCE=1 after first access	DATA

Register Map - continued

(0x0F) Status Register

Fields	Function	
RD_DRDY	This bit informs the preparation status of the measured data 0: Waiting for end of measurement 1: Ready OK	

default value 0x00

(0x10/0x11) Output Data Register

Fields	Function
DATA [7:0]	Output value LSB
DATA [15:8]	Output value MSB
	default value 0xXXXX

signed 16 bit -8192d(0xE000) to +8191d(0x1FFF)

(0x1B) Control setting1 Register

Fields	Function
PC1	Power Control 0: Power Down 1: Active
RST_LV	Logic reset control 0: Reset release 1: Reset Reset release at RST_LV(CNTL1)=0 & RSTB_LV(CNTL4)=1
ODR [1:0]	Measurement output data rates 00: 20 Hz Mode 01: 100 Hz Mode 10: 200 Hz Mode 11: 1 kHz Mode
FS1	Measurement mode setting 0: Continuous mode 1: Single mode

default value 0x22

(0x1C) Control setting2 Register

Fields	Function
ALERT_EN	Select output signal of ALERT pin 0: No output 1: DRDY signal(Output RD_DRDY from pin)

default value 0x00

(0x1D) Control setting3 Register

Fields	Function		
FORCE	AD start measurement trigger at continuous mode (FS1=0) and single mode (FS1=1) 1: Start measurement		
	Register is automatic clear "0" after write data "1" Write data "0" is invalid If write data "1" on measurement way, stop and restart measurement		

default value 0x00

(0x5C/0x5D) Control setting4 Register

Fields	Function	
RSTB_LV [7:0]	Reserved (ignore write data)	
RSTB_LV [15:8]	RSTB_LV=1 by write access (ignore write data) Reset release at RST_LV(CNTL1)=0 & RSTB_LV(CNTL4)=1 RSTB_LV=0 by write PC1(CNTL1)=0	

default value 0x00

Control Sequence

- 1. Control Sequence
- 1.1 Power supply start-up sequence

Do the command control by I²C after all powers are supplied.



Figure 8. Timing Chart at Power ON

1.2 Power supply end sequence



Figure 9. Timing Chart at Power OFF

Control Sequence - continued

2. Measurement sequence

There are the following two kinds of measurement modes





2.1 Continuous Mode

(Send command example)

	Register Name	Address	Data
	CNTL1	0x1B	0x80
Step1		0x5C	0x00
	CINTL4	0x5D	0x00
Step2	CNTL2	0x1C	0x08
Step3 CNTL3		0x1D	0x40
	STA1	0x0F	
Step4		0x10	Read
	DAIA	0x11	



Figure 11. Sequence of Continuous Mode

Control Sequence - continued

2.2 Single Mode

(Send command example)

	Register Name	Address	Data
	CNTL1	0x1B	0x82
Step1		0x5C	0x00
	CINTL4	0x5D	0x00
Step2	tep2 CNTL2		0x08
Step3	CNTL3	0x1D	0x40
	STA1	0x0F	
Step4		0x10	Read
	DAIA	0x11	



Figure 12. Sequence of Single Mode

Application Example



Figure 13. Example of Application Circuit

(*Note*) Sensor property may change due to around magnetic parts. We recommend calibrating the sensitivity and origin point of magnetic sensors after mounting.

I/O Equivalence Circuits

Pin Name	Equivalent Circuit Diagram	Pin Name	Equivalent Circuit Diagram
SCL		SDA	
ALERT		ADDR	
TEST		VREG	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Figure 14. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information



Marking Diagram



Physical Dimension and Packing Information Package Name VQFN20QV3535 3.5 ± 0.1 - 5 ± 0 . с. С Q 1 PIN MARK 0 MAX Ş ٦ ÷., 03 2 2) $0. \ 0 \ 2 \ {}^{+0.}_{-0.}$ $\Box 0.08S$ 0. 2. 05 ± 0.1 C0. 2 F U U U U U 20_ $0.5 \pm 0.$ $4\pm 0.$ 2 0. 1.610 \square \square \square \square \square 1511 (UNIT:mm) 0.75PKG: VQFN20QV3535 $0. \ 2 \ 5 \ {}^{+0. \ 0 \ 5}_{-0. \ 0 \ 4}$ 0.5 Drawing No. EX422-5001-1 < Tape and Reel Information > Таре Embossed carrier tape Quantity 2500pcs Direction of feed E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand Ο Ο Ο Ο Ο 0 Ο 0 0 0 Ο 0 E2 TR E2 TR E2 TR E2 TR E2 TR E2 TR ΤL E1 ΤL E1 ΤL E1 TL E1 ΤL E1 ΤL E1 Direction of feed Pocket Quadrants Reel

Revision History

Date	Revision		Changes			
10.Oct.2019	001	New Release				

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(Note1) Medical Equipment Classification of the Specific Application

JAPAN	USA	EU	CHINA
CLASSⅢ		CLASS II b	CLASSI
CLASSⅣ	CLASSI	CLASSⅢ	

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 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
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