Power Management IC for Bay Trail -M/-D/-I Platform

BD9596BMWV (Code name: Jarrell Cove)

General Description

BD9596BMWV (Jarrell Cove) is a Power Management Integrated Circuit (PMIC) designed specifically for use on Bay Trail-M/-D/-I platform for in-vehicle infotainment (IVI) systems, industrial control systems.

Features

- Complicated Power up / down sequence and state control are embedded.
- Fewer external components count / compact size.
- Controlling power regulation for each state (S4/S5, S3 and S0) results in a low power consumption.
- Built-in reference clock (RTCCLK): 32.768kHz±5%.
- Power control logic with processor interface and event detection.
- SVID interface for control and register access.
- Error mode indicator for debugging.
- Built-in UVLO, SCP, OVP and TSD protection.

Support Bay Trail Family

- Intel® Celeron® N2920
- Intel® Celeron® J1900
- Intel® Atom™ E3800 series

Applications

- Industrial control systems
- Intelligent vending systems
- ATM
- Point-of-sale (POS) terminals
- etc

Key Specifications

■Input Voltage Range:	3.5V to 5.5V
■VCC Output Voltage Range:	0.5V to 1.2V
■VCC Output Current:	13.541A (Max)
(Output current depends on external component)	
■VNN Output Voltage Range:	0.5V to 1.2V
■VNN Output Current:	13.207A (Max)
(Output current depends on external component.)	
■V1P0A Output Voltage:	1.0V (Typ)
■V1P0A Output Current:	0.7A (Max)
■V1P0S Output Voltage:	1.0V (Typ)
■V1P0S Output Current:	2.667A (Max)
(Output current depends on external component)	
■V1P05S Output Voltage:	1.05V (Typ)
■V1P05S Output Current:	1.322A (Max)
■V1P24A Output Voltage:	1.24V (Typ)
■V1P24A Output Current:	0.05A (Max)
■V1P24S Output Voltage:	1.24V (Typ)
■V1P24S Output Current:	0.05A (Max)
■VSFR Output Voltage:	1.35V (Typ)
■VSFR Output Current:	0.5A (Max)
■V1P8A Output Voltage:	1.8V (Typ)
■V1P8A Output Current:	1.8A (Max)
■V1P8S Output Voltage:	1.8V (Typ)
■V1P8S Output Current:	0.8A (Max)
■VSDIO Output Voltage:	1.8V or 3.3V (Typ)
■VSDIO Output Current:	0.02A (Max)
■V3P3A Output Voltage:	3.3V (Typ)
■V3P3A Output Current:	0.1A (Max)
■V3P3S Output Voltage:	3.3V (Typ)
■V3P3S Output Current:	0.5A (Max)
■VRTC Output Voltage:	3.3V (Typ)
■VRTC Output Current:	0.12A (Max)
■VDDQ Output Voltage Range:	1.2V to 1.6V
■VDDQ Output Current:	4.51A (Max)
(Output current depends on external component.)	
■VTT Output Voltage:	VDDQ/2 (Typ)
■VTT Output Current:	0.53A (Max)
■Switching Frequency:	1MHz (Typ)
■Pch FET ON Resistance:	120mΩ(Typ)
(V1P0A, V1P8A, V1P05S)	
■Nch FET ON Resistance:	120mΩ(Typ)
(V1P0A, V1P8A, V1P05S)	
■Operating Temperature Range:	-40℃ to +95℃

Package(s)	W(Typ) x D(Typ) x H(Max)
UQFN88MV0100	10.0mm x 10.0mm x 1.00mm

Block Diagram

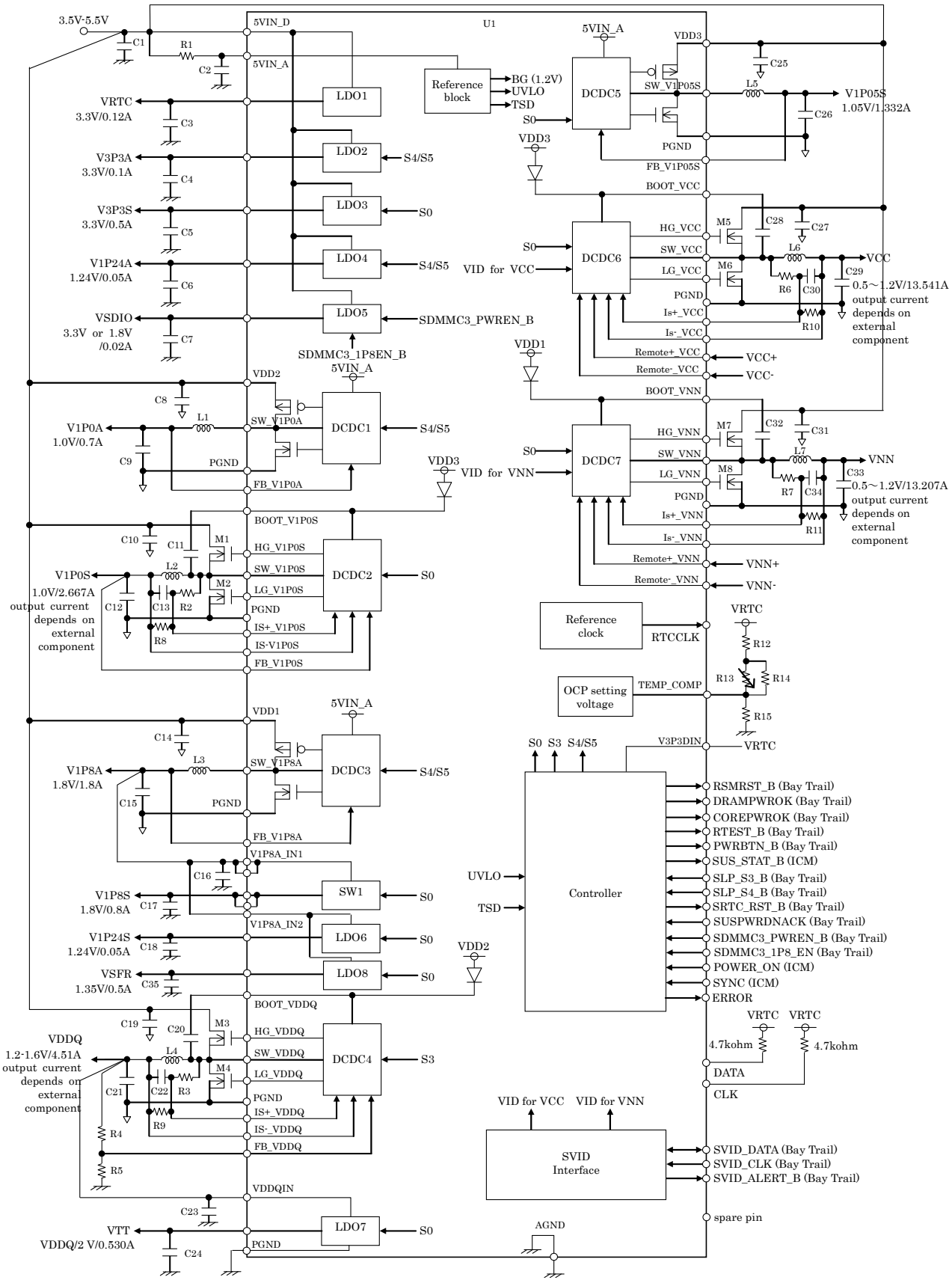


Figure 1. Block Diagram

Component Selection

Table 1: Component Selection

Part No	Value	Company	Part name
U1	-	ROHM	BD9596BMWV
R1	1	ROHM	
R2	560	ROHM	
R3	1k	ROHM	
R4	11k	ROHM	
R5	16k	ROHM	
R6	620	ROHM	
R7	620	ROHM	
R8	1k	ROHM	
R9	2k	ROHM	
R10	910	ROHM	
R11	910	ROHM	
R12	8.2k	ROHM	
R13	10k	MURATA	NCP18X103F0SRB
R14	8.2k	ROHM	
R15	2.7k	ROHM	
L1	6.8uH	Taiyo Yuden	NR3012
L2	1.0uH	Taiyo Yuden	NRS4018
L3	3.3uH	Taiyo Yuden	NRS4018
L4	1.0uH	VISHAY	IHLP-2020-CZ ER1R0MA1e3
L5	3.3uH	Taiyo Yuden	NRS4018
L6	0.33uH	VISHAY	IHLP-2020-CZ ER0R33MA1e3
L7	0.33uH	VISHAY	IHLP-2020-CZ ER0R33MA1e3
M1		ROHM	RF4E080BNTR
M2		ROHM	RF4E080BNTR
M3		ROHM	RF4E080BNTR
M4		ROHM	RF4E080BNTR
M5		Infineon	IPG20N04S4L-08
M6			
M7		Infineon	IPG20N04S4L-08
M8			

Part No	Value	Company	Part name
C1	10uF		
C2	10uF		
C3	10uF		
C4	10uF		
C5	10uF		
C6	10uF		
C7	1uF		
C8	22uF		
C9	47uF		
C10	22uF		
C11	0.1uF		
C12	47uF x 2		
C13	0.1uF		
C14	22uF		
C15	47uF x 2		
C16	10uF		
C17	10uF		
C18	10uF		
C19	10uF x 2		
C20	0.1uF		
C21	47uF x 2		
C22	0.1uF		
C23	10uF		
C24	10uF		
C25	10uF x 2		
C26	47uF x 2		
C27	10uF x 4		
C28	0.1uF		
C29_1	220uF x 2	Panasonic	2R5TAE220M9
C29_2	47uF x 2		
C30	0.1uF		
C31	10uF x 4		
C32	0.1uF		
C33_1	220uF x 2	Panasonic	2R5TAE220M9
C33_2	47uF x 2		
C34	0.1uF		
C35	10uF		

*These values and parts may be changed for improvement etc.

Pin Configuration

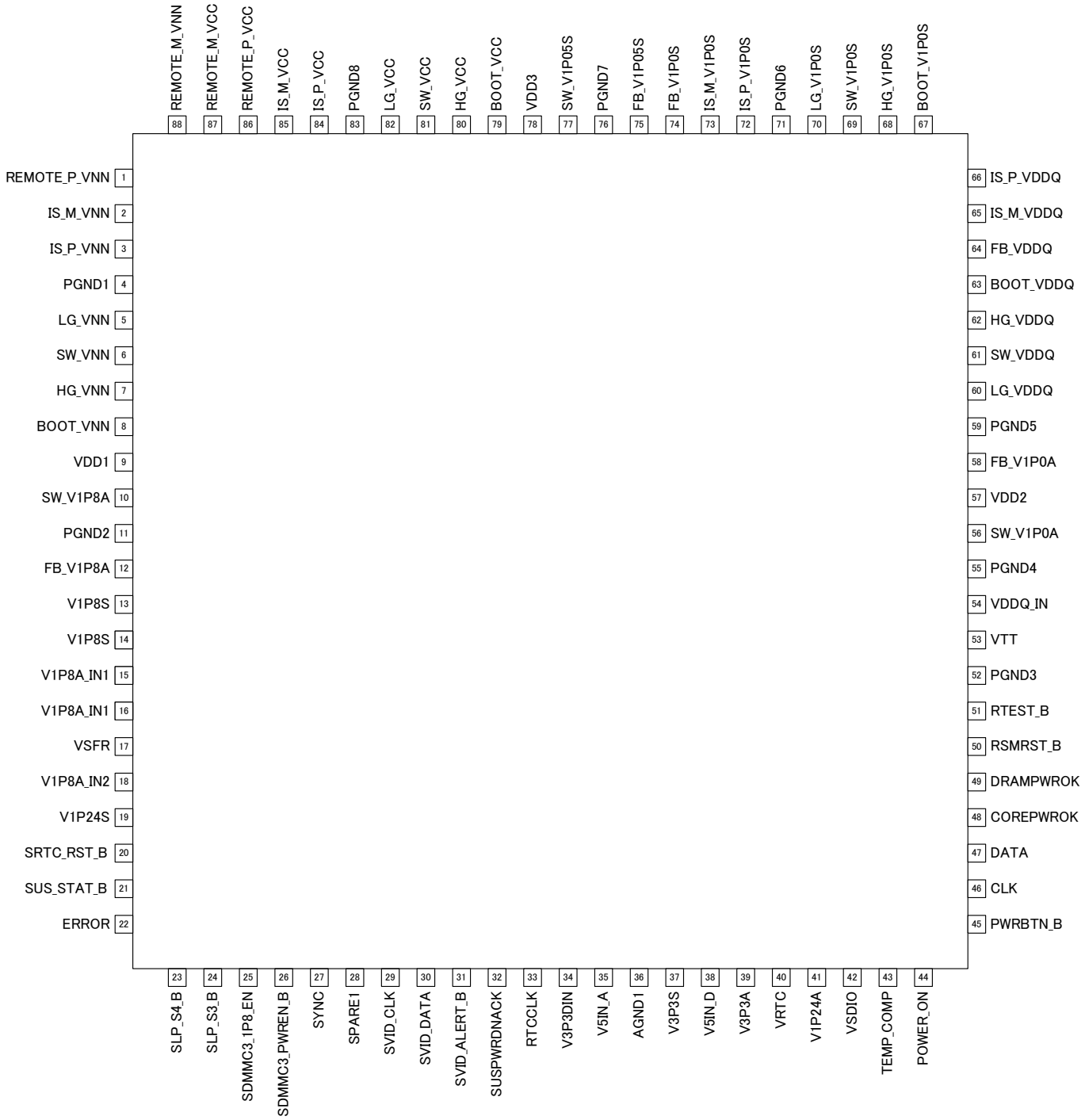


Figure 2. Pin Configuration

Pin Description

Table 2: BD9596BMWV Pin Description

Pin No.	Pin Name	Connect to	I/O	Function
1	REMOTE_P_VNN	PMIC	I	VNN output remote sensing pin
2	IS_M_VNN	PMIC	I	Negative input of current sensing pin for VNN
3	IS_P_VNN	PMIC	I	Positive input of current sensing pin for VNN
4	PGND1	-	-	Power GND pin1
5	LG_VNN	External	O	Low side MOSFET gate driver pin for VNN
6	SW_VNN	External	O	High side MOSFET source pin for VNN
7	HG_VNN	External	O	High side MOSFET gate driver pin for VNN
8	BOOT_VNN	PMIC	I	High side MOSFET driver power supply pin for VNN
9	VDD1	POWER	I	Power supply pin for V1P8A
10	SW_V1P8A	External	O	High side MOSFET source pin for V1P8A
11	PGND2	-	-	Power GND pin2
12	FB_V1P8A	PMIC	I	Feedback pin for V1P8A
13	V1P8S	SOC	O	Output voltage for V1P8S
14	V1P8S	SOC	O	Output voltage for V1P8S
15	V1P8A_IN1	POWER	I	1.8V power supply pin1
16	V1P8A_IN1	POWER	I	1.8V power supply pin1
17	VSFR	SOC	O	Output voltage for VSFR
18	V1P8A_IN2	POWER	I	1.8V power supply pin2
19	V1P24S	SOC	O	Output voltage for V1P24S
20	SRTC_RST_B	SOC	O	RTC detect signal pin
21	SUS_STAT_B	Platform	O	SUS_STAT_B pin
22	ERROR	-	O	ERROR signal pin
23	SLP_S4_B	SOC	I	Input signal from Bay Trail; indicates S4 state entry upon assertion and exit upon de-assertion
24	SLP_S3_B	SOC	I	Input signal form Bay Trail; indicates S3 state entry upon assertion and exit upon de-assertion
25	SDMMC3_1P8_EN	SOC	I	Input signal from SOC (select 1.8V or 3.3V for SD)
26	SDMMC3_PWR_EN_B	SOC	I	Input signal to enable SD card power
27	SYNC	Platform	I	External synchronous clock input
28	SPARE1	-	O (OD)	Spare pin1
29	SVID_CLK	SOC	I	SVID clock
30	SVID_DATA	SOC	I/O (OD)	SVID data

Pin Description – continued

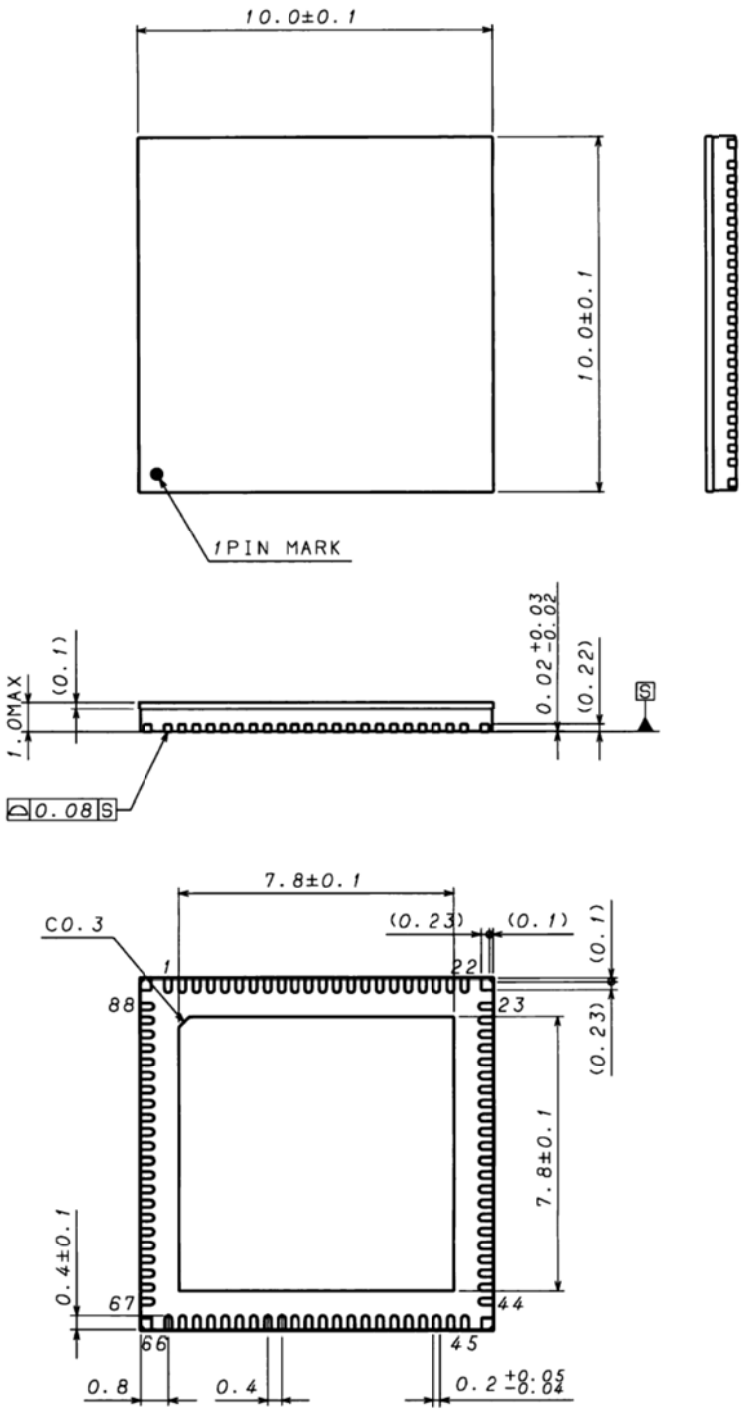
Pin No.	Pin Name	Connect to	I/O	Function
31	SVID_ALERT_B	SOC	O (OD)	SVID alert
32	SUSPWRDNACK	SOC	I	Input signal from Bay Trail that turns off the SUS rails in junction with the assertion of SLP_S4_B.
33	RTCCLK	SOC	O	32kHz clock output pin
34	V3P3DIN	POWER	I	Logic power supply pin
35	V5IN_A	POWER	I	5V power supply pin
36	AGND1	-	-	Analog GND pin1
37	V3P3S	SOC	O	Output voltage for V3P3S
38	V5IN_D	POWER	I	5V power supply pin
39	V3P3A	SOC	O	Output voltage for V3P3A
40	VRTC	-	O	Output voltage for VRTC
41	V1P24A	SOC	O	Output voltage for V1P24A
42	VSDIO	SOC	O	Output voltage for VSDIO
43	TEMP_COMP	PMIC	I	Over current protect voltage setting pin
44	POWER_ON	Platform	I	POWER_ON pin
45	PWRBTN_B	SOC	O (OD)	Boot up signal output pin
46	CLK	-	-	Connect 4.7kohm resisters to VRTC
47	DATA	-	-	Connect 4.7kohm resisters to VRTC
48	COREPWROK	SOC	O (OD)	COREPWROK asserts when all voltage rails that are ON in S0
49	DRAMPWROK	SOC	O (OD)	DRAMPWROK asserts when voltage rail VDDQ is within 10% of its normal voltage
50	RSMRST_B	SOC	O (OD)	RSMRST_B asserts when voltage rail V3P3A is valid
51	RTEST_B	SOC	O (OD)	TEST Pin
52	PGND3	-	-	Power GND pin3
53	VTT	DDR	O	Output voltage for VTT
54	VDDQ_IN	POWER	I	VDDQ power supply pin
55	PGND4	-	-	Power GND pin4
56	SW_V1P0A	External	O	High side MOSFET source pin for V1P0A
57	VDD2	POWER	I	Power supply pin for V1P0A
58	FB_V1P0A	PMIC	I	Feedback pin for V1P0A
59	PGND5	-	-	Power GND pin5
60	LG_VDDQ	External	O	Low side MOSFET gate driver pin for VDDQ
61	SW_VDDQ	External	O	High side MOSFET source pin for VDDQ
62	HG_VDDQ	External	O	High side MOSFET gate driver pin for VDDQ

Pin Description – continued

Pin No.	Pin Name	Connect to	I/O	Function
63	BOOT_VDDQ	PMIC	I	High side MOSFET driver power supply pin for VDDQ
64	FB_VDDQ	PMIC	I	Feedback pin for VDDQ
65	IS_M_VDDQ	PMIC	I	Negative input of current sensing pin for VDDQ
66	IS_P_VDDQ	PMIC	I	Positive input of current sensing pin for VDDQ
67	BOOT_V1P0S	PMIC	I	High side MOSFET driver power supply pin for V1P0S
68	HG_V1P0S	External	O	High side MOSFET gate driver pin for V1P0S
69	SW_V1P0S	External	O	High side MOSFET source pin for V1P0S
70	LG_V1P0S	External	O	Low side MOSFET gate driver pin for V1P0S
71	PGND6	-	-	Power GND pin6
72	IS_P_V1P0S	PMIC	I	Positive input of current sensing pin for V1P0S
73	IS_M_V1P0S	PMIC	I	Negative input of current sensing pin for V1P0S
74	FB_V1P0S	PMIC	I	Feedback pin for V1P0S
75	FB_V1P05S	PMIC	I	Feedback pin for V1P05S
76	PGND7	-	-	Power GND pin7
77	SW_V1P05S	External	O	High side MOSFET source pin for V1P05S
78	VDD3	POWER	I	Power supply pin for V1P05S
79	BOOT_VCC	PMIC	I	High side MOSFET driver power supply pin for VCC
80	HG_VCC	External	O	High side MOSFET gate driver pin for VCC
81	SW_VCC	External	O	High side MOSFET source pin for VCC
82	LG_VCC	External	O	Low side MOSFET gate driver pin for VCC
83	PGND8	-	-	Power GND pin8
84	IS_P_VCC	PMIC	I	Positive input of current sensing pin for VCC
85	IS_M_VCC	PMIC	I	Negative input of current sensing pin for VCC
86	REMOTE_P_VCC	PMIC	I	VCC output remote sensing pin
87	REMOTE_M_VCC	PMIC	I	VCC GND remote sensing pin
88	REMOTE_M_VNN	PMIC	I	VNN GND remote sensing pin

*OD=Open Drain

Package Outline

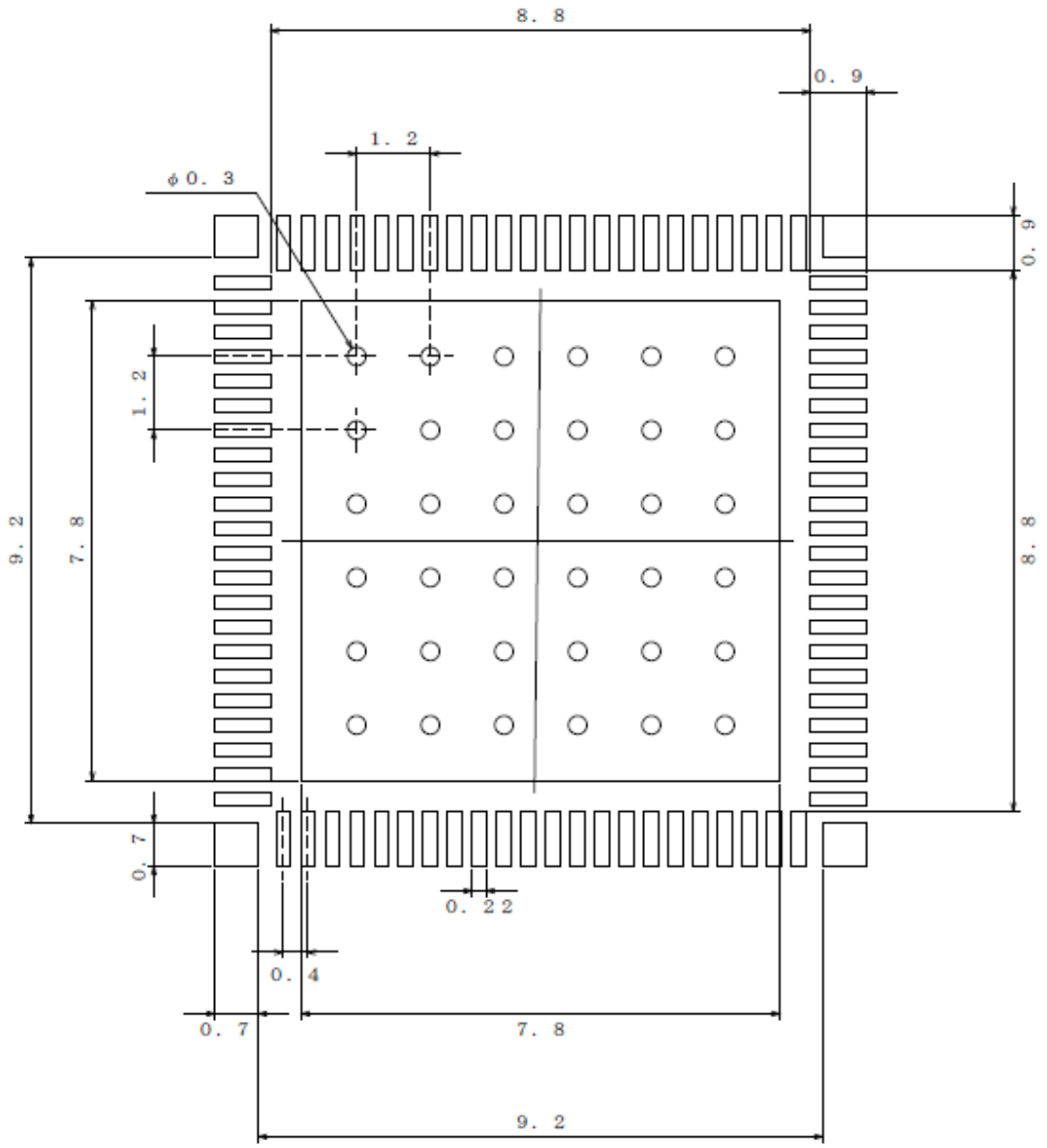


(UNIT: mm)

PKG: UQFN88MV0100

Figure 3. Package Outline

Footprint Dimension



(UNIT: mm)

PKG: UQFN88MV0100

Figure 4. Footprint Dimension

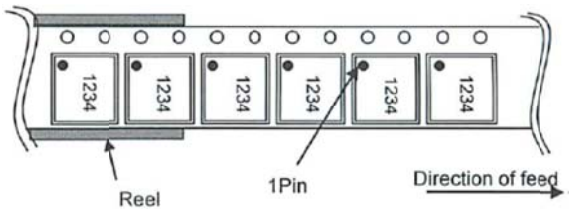
Ordering Information

B D 9 5 9 6 B M W V	E 2
Part Number	Package MWV: UQFN88MV0100
	Packaging and forming specification E2: Embossed tape and reel

Physical Dimension Tape and Reel Information

<Tape and Real Information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2



Marking Diagram

Table 3: Marking Diagram and 3D image of package

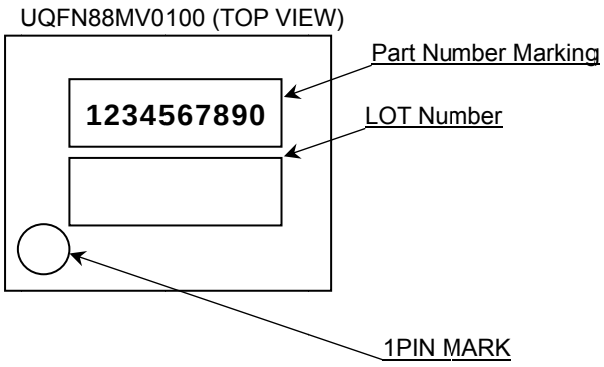
UQFN88MV0100	
10.00mm x 10.00mm x 1.00mm	
	

Table of Contents

1. Device Feature

1.1 Output Features

(Bay Trail)
IMVP7Lite compliant DC/DC regulator VCC (0.5V-1.2V / 13.541A (output current depends on external component))
IMVP7Lite compliant DC/DC regulator VNN (0.5V-1.2V / 13.207A (output current depends on external component))
DCDC regulator V1P0A (1.0V / 0.700A)
DCDC regulator V1P0S (1.0V / 2.667A (output current depends on external component))
DCDC regulator V1P05S (1.05V / 1.322A)
LDO V1P24A (1.24V / 0.050A)
LDO V1P24S (1.24V / 0.050A)
LDO VSFR (1.35V / 0.500A)
DCDC regulator V1P8A (1.8V / 1.800A)
Load switch V1P8S (1.8V / 0.800A)
LDO VSDIO (1.8V or 3.3V / 0.020A)
LDO V3P3A (3.3V / 0.100A)
LDO V3P3S (3.3V / 0.500A)
LDO VRTC (3.3V / 0.120A)
DCDC regulator VDDQ (1.2-1.6V / 4.510A (output current depends on external component))
LDO VTT (VDDQ/2 V / 0.530A)
*IMVP7Lite compliant DC/DC regulators do not have full features. (IMVP7Lite)

1.2 Output Voltage Table

Table 4: Output voltage table of each S-state

	Channel	Rail name	Source [V]	Iomax [mA]	S4/S5	S3	S0
Bay Trail	DCDC1	V1P0A	1.0V	700 (Note 1)	ON	ON	ON
	DCDC2	V1P0S	1.0V	2667 (Note 2)	OFF	OFF	ON
	DCDC3	V1P8A	1.8V	1800 (Note 1)	ON	ON	ON
	DCDC4	VDDQ	1.2-1.6V	4510 (Note 2)	OFF	ON	ON
	DCDC5	V1P05S	1.05V	1322 (Note 1)	OFF	OFF	ON
	DCDC6	VCC	0.5V-1.2V	13541 (Note 2)	OFF	OFF	ON
	DCDC7	VNN	0.5V-1.2V	13207 (Note 2)	OFF	OFF	ON
	SW1	V1P8S	1.8V	800 (Note 1)	OFF	OFF	ON
	LDO1	VRTC	3.3V	120 (Note 1)	ON	ON	ON
	LDO2	V3P3A	3.3V	100 (Note 1)	ON	ON	ON
	LDO3	V3P3S	3.3V	500 (Note 1)	OFF	OFF	ON
	LDO4	V1P24A	1.24V	50 (Note 1)	ON	ON	ON
	LDO5	VSDIO	1.8V or 3.3V	20 (Note 1)	OFF	OFF	ON
	LDO6	V1P24S	1.24V	50 (Note 1)	OFF	OFF	ON
	LDO7	VTT	VDDQ/2 V	530 (Note 1)	OFF	OFF	ON
	LDO8	VSFR	1.35V	500 (Note 1)	OFF	OFF	ON

Note 1 Do not exceed Pd.
Note 2 Iomax depends on the external component.

1.3 **Power Management Diagram for Jarrell Cove PMIC**

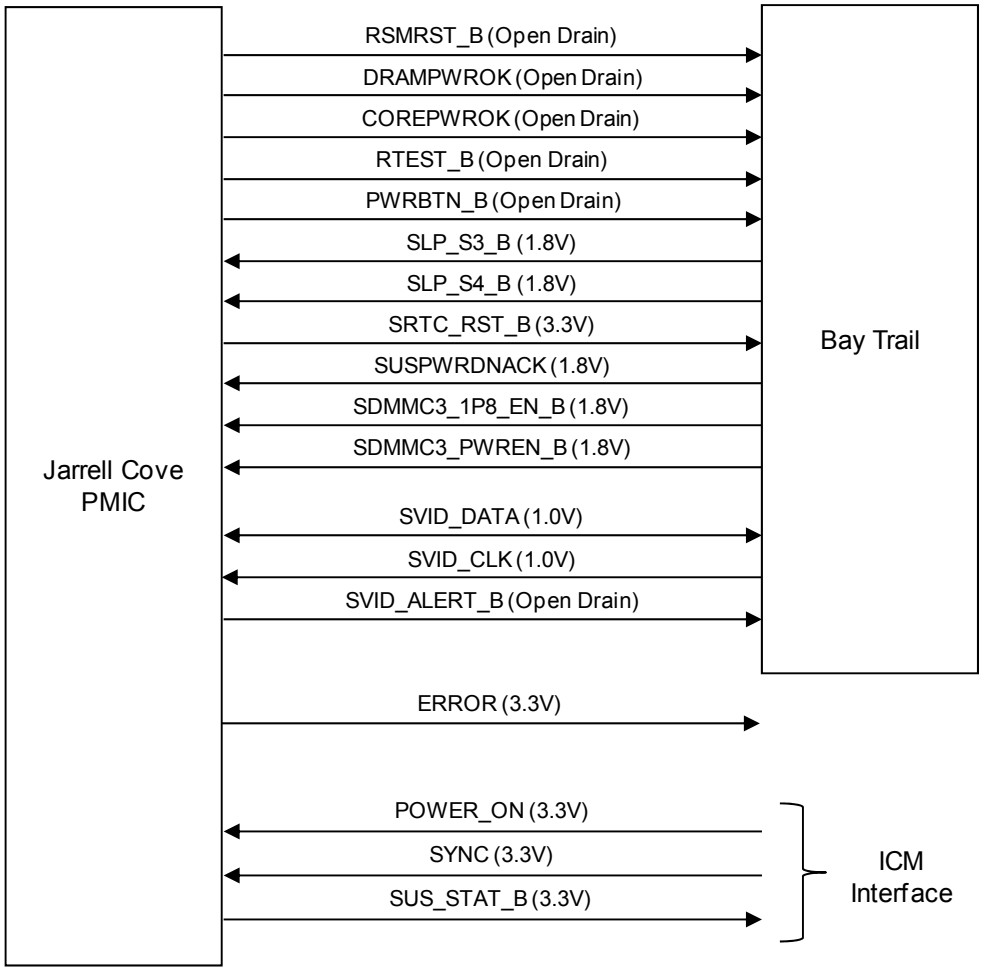


Figure 5. Power Management Diagram for Jarrell Cove PMIC

1.4 Power Rail Diagram for Jarrell Cove PMIC

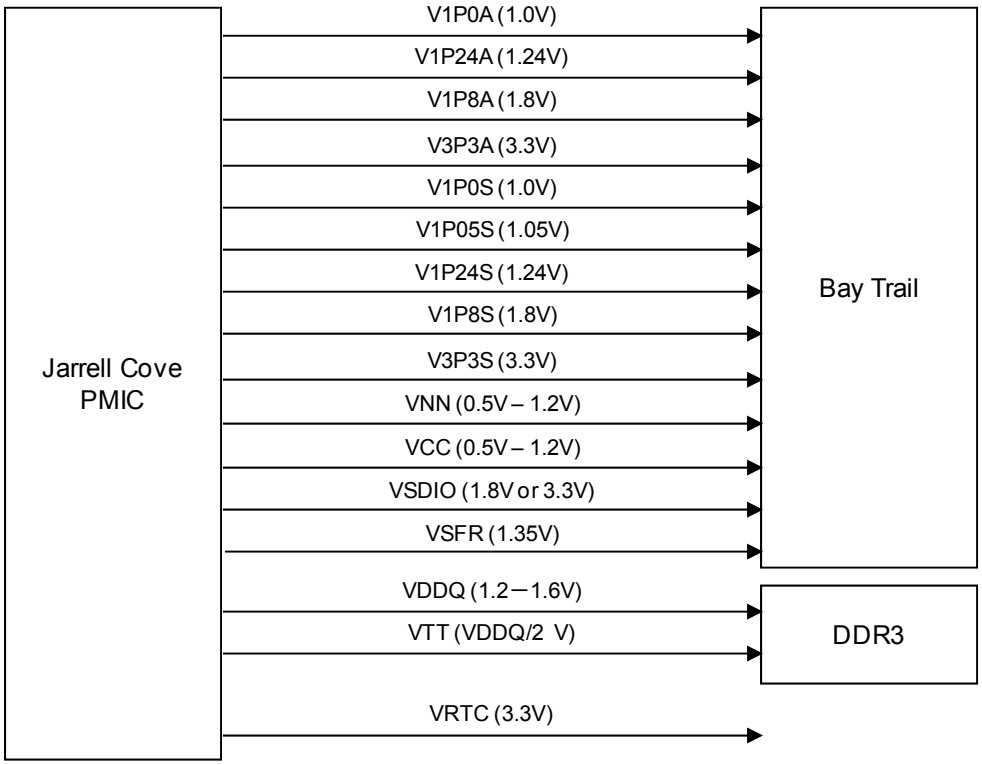
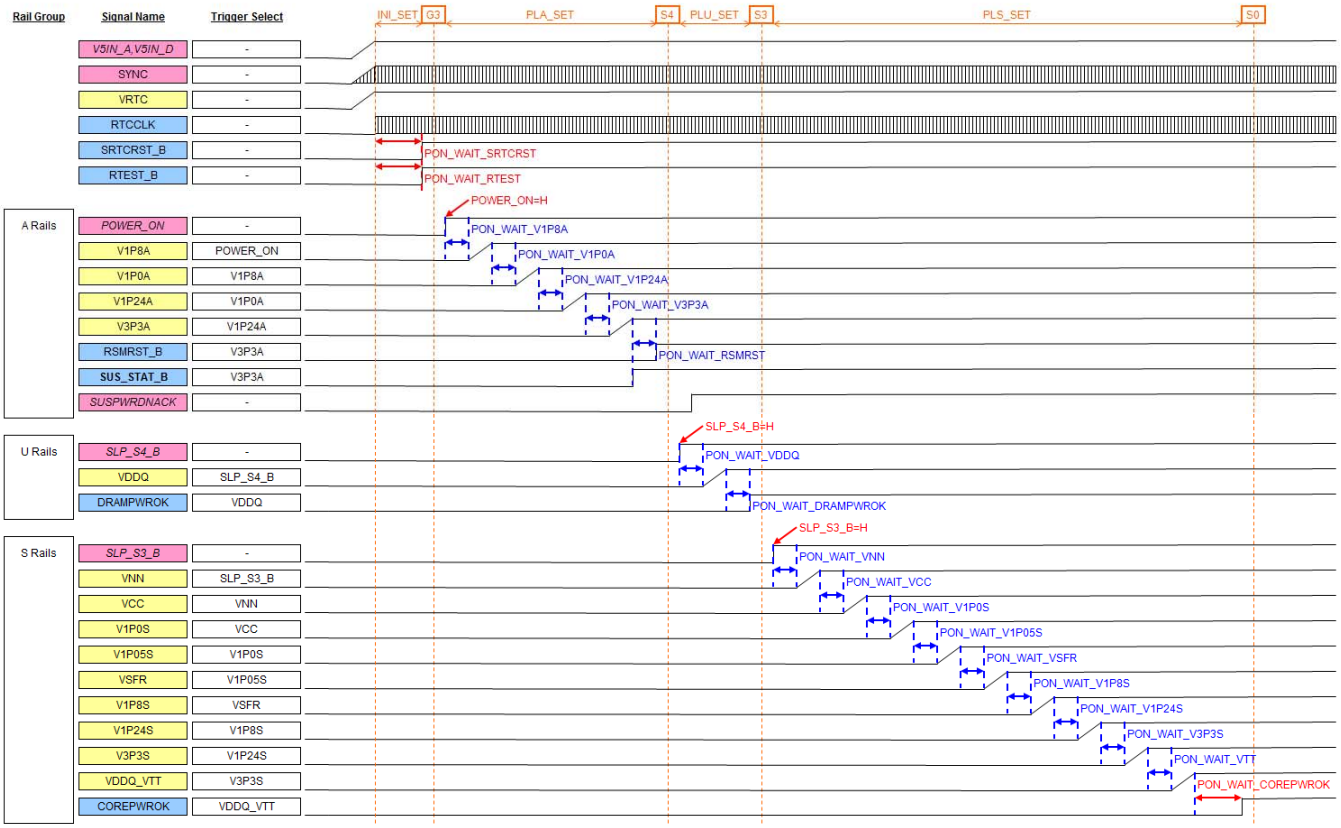


Figure 6. Power Rail Diagram for Jarrell Cove PMIC

2. Application

2.1 Power-up Sequence



(Note)
It is not allowed to move a rail to other rail group and select a signal of other rail group for the trigger.

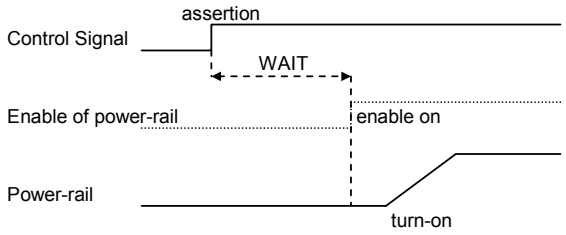
Figure 7. Power-up Sequence

Table 5: Power-up Sequence Wait Time

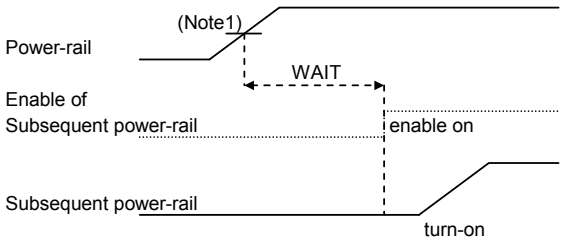
No.	Register Name	Description	Default Setting	Min	Typ	Max	Units
1	PON_WAIT_SRTCRST	VRTC stable to SRTCRST_B high	Specific	9	-	11	ms
2	PON_WAIT_RTEST	VRTC stable to RTEST_B high	Specific	9	-	11	ms
3	PON_WAIT_V1P8A	POWER_ON asserted to first A rail turn-on delay	Short	10	-	16	µs
4	PON_WAIT_V1P0A	Voltage rail to subsequent rail delay	Short	10	-	16	µs
5	PON_WAIT_V1P24A	Voltage rail to subsequent rail delay	Short	10	-	16	µs
6	PON_WAIT_V3P3A	Voltage rail to subsequent rail delay	Short	10	-	16	µs
7	PON_WAIT_RSMRST	A rails valid to RSMRST_B de-assertion	Short	10	-	16	µs
8	PON_WAIT_VDDQ	SLP_S4_B de-assertion to VDDQ turn-on delay	Short	10	-	16	µs
9	PON_WAIT_DRAMPWROK	VDDQ valid to DRAMPWROK assertion	Short	10	-	16	µs
10	PON_WAIT_VNN	SLP_S3_B de-assertion to first S rail turn-on delay	Short	10	-	16	µs
11	PON_WAIT_VCC	Voltage rail to subsequent rail delay	Immediately	0	-	5	µs
12	PON_WAIT_V1P0S	Voltage rail to subsequent rail delay	Immediately	0	-	5	µs
13	PON_WAIT_V1P05S	Voltage rail to subsequent rail delay	Short	10	-	16	µs
14	PON_WAIT_VSFR	Voltage rail to subsequent rail delay	Short	10	-	16	µs
15	PON_WAIT_V1P8S	Voltage rail to subsequent rail delay	Short	10	-	16	µs
16	PON_WAIT_V1P24S	Voltage rail to subsequent rail delay	Short	10	-	16	µs
17	PON_WAIT_V3P3S	Voltage rail to subsequent rail delay	Short	10	-	16	µs
18	PON_WAIT_VTT	Voltage rail to subsequent rail delay	Short	10	-	16	µs
19	PON_WAIT_COREPWROK	S rails valid to COREPWROK assertion	Specific	100	-	140	ms

(Note) Values in the logic block are guaranteed by design
(Note) Values exclude the delay time from “enable-on” to “turn-on”

[No.3,8,10]



[No.4 to 6,11 to 18]



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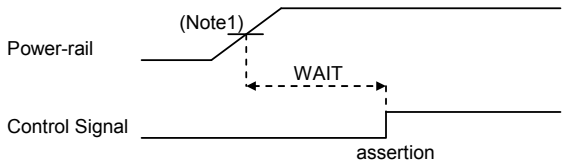
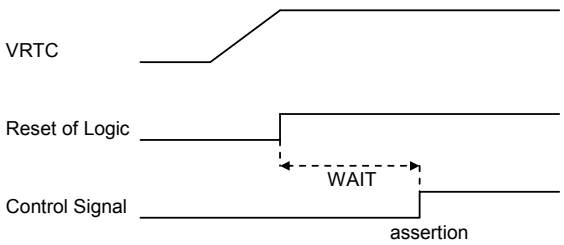
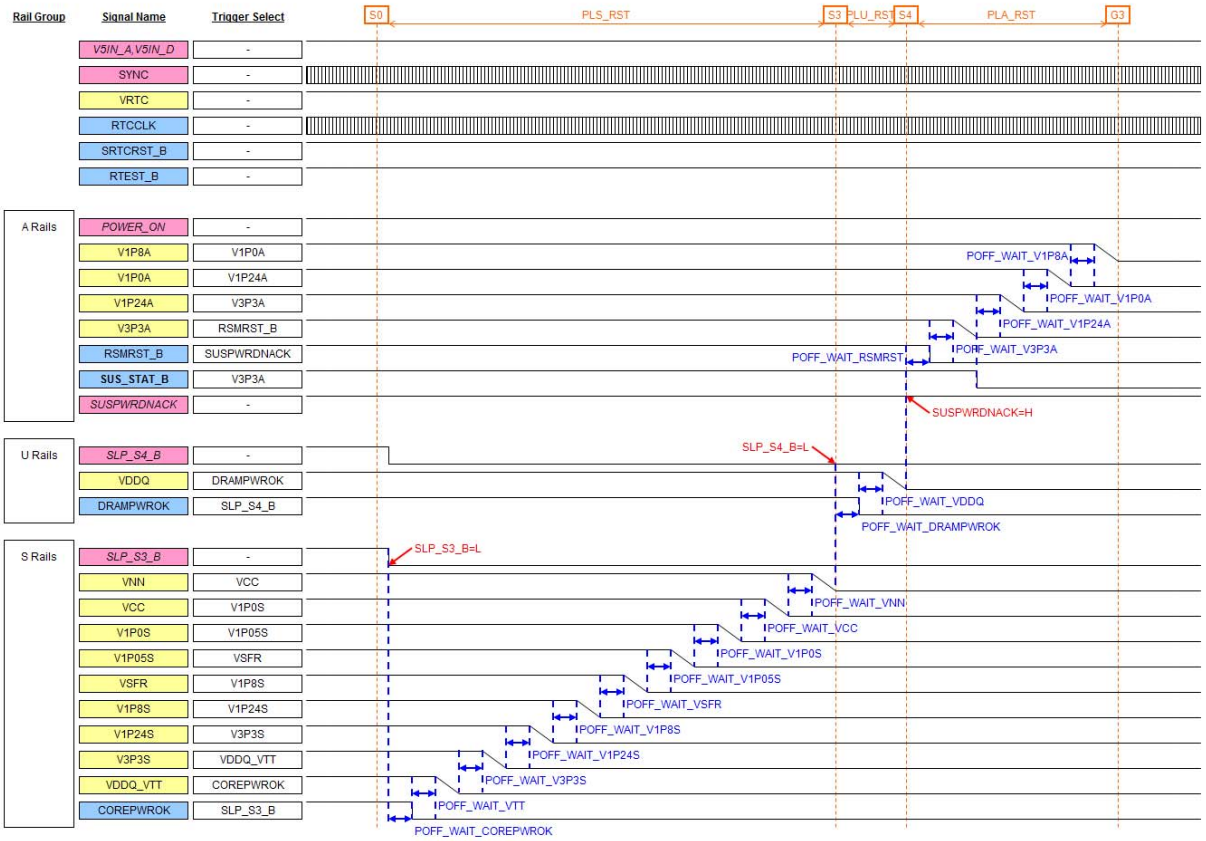


(Note 1) Power-Good Level
100% : VCC,VNN
90% : VDDQ
80% : V1P0A,V1P8A,V1P0S,V1P05S,VTT
70% : V1P24A,V3P3A,V1P8S,V1P24S,V3P3S,VSFR

[No.1,2]



2.2 Power-down Sequence



(Note)
It is not allowed to move a rail to other rail groups and select a signal of other rail groups as the trigger.

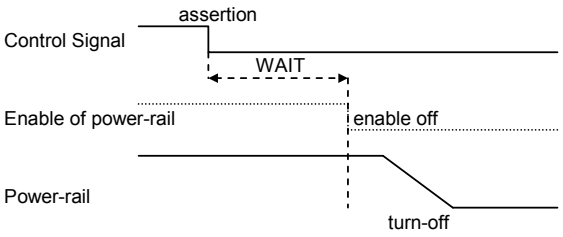
Figure 8. Power Down Sequence

Table 6: Power-down Sequence Wait Time

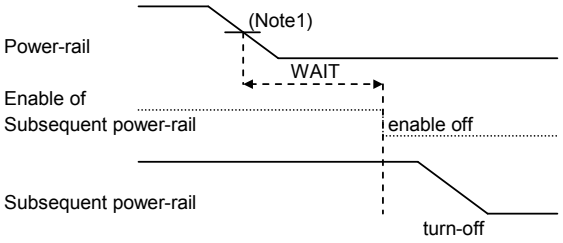
No.	Register Name	Description	Default Setting	Min	Typ	Max	Units
1	POFF_WAIT_COREPWROK	SLP_S3_B assertion to COREPWROK de-assertion	Short	10	-	16	µs
2	POFF_WAIT_VTT	COREPWROK de-assertion to first S rail starts to turn-off	Short	10	-	16	µs
3	POFF_WAIT_V3P3S	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
4	POFF_WAIT_V1P24S	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
5	POFF_WAIT_V1P8S	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
6	POFF_WAIT_VSFR	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
7	POFF_WAIT_V1P05S	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
8	POFF_WAIT_V1P0S	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
9	POFF_WAIT_VCC	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
10	POFF_WAIT_VNN	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
11	POFF_WAIT_DRAMPWROK	SLP_S4_B assertion to DRAMPWROK de-assertion	Short	10	-	16	µs
12	POFF_WAIT_VDDQ	DRAMPWROK de-assertion to VDDQ starts to turn-off	Short	10	-	16	µs
13	POFF_WAIT_RSMRST	VDDQ down to RSMRST_B assertion	Short	10	-	16	µs
14	POFF_WAIT_V3P3A	RSMRST_B de-assertion to first A rail starts to turn-off	Short	10	-	16	µs
15	POFF_WAIT_V1P24A	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
16	POFF_WAIT_V1P0A	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms
17	POFF_WAIT_V1P8A	Voltage rail to subsequent rail delay	Long	0.5	-	1	ms

(Note) Values in the logic block are guaranteed by design
(Note) Values exclude the delay time from “enable-off” to “turn-off”

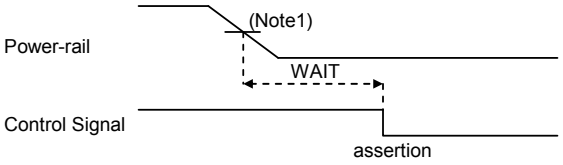
[No.2,12,14]



[No.3 to 10,15 to 17]

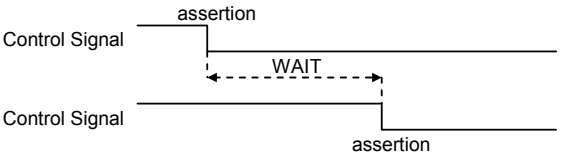


[No.13]



(Note 1) Shut-down Level
0.2V : VCC,VNN,VDDQ
0.5V : other power rails

[No.1,11]



2.3 Logic Block Diagram

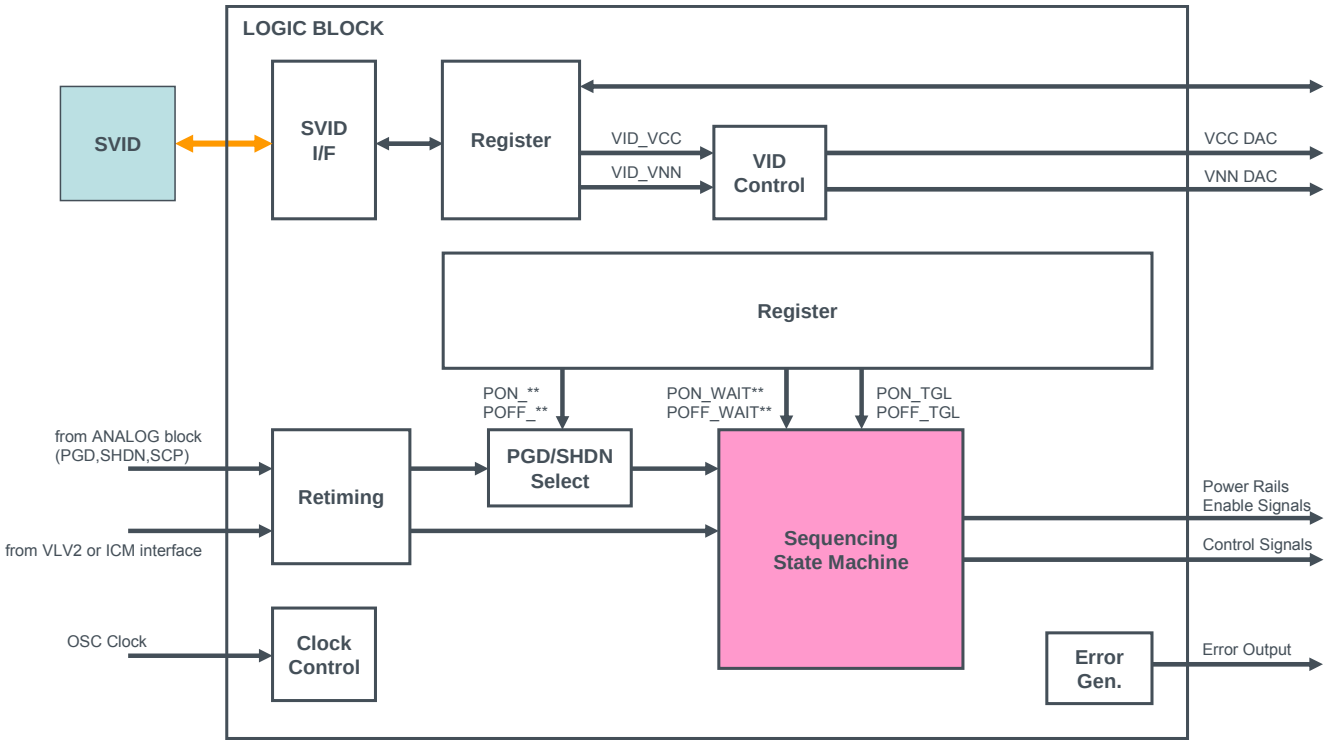


Figure 9. Logic Block Diagram

2.4 Input Capacitor Selection

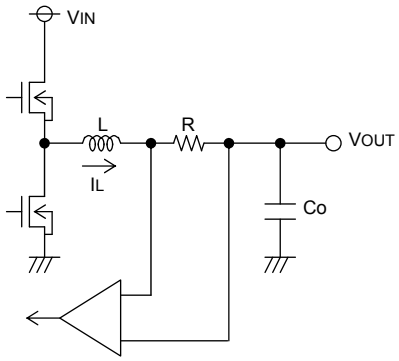
The input capacitor reduces the input voltage ripple caused by the switching current on VDD1, VDD2 and VDD3. Place the input capacitor as close as possible to the VDD1, VDD2 and VDD3 pin. A 22uF or 47uF ceramic capacitor is recommended. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by the following formula.

$$I_{RMS} = I_{OUT}(MAX) \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \cdots (1)$$

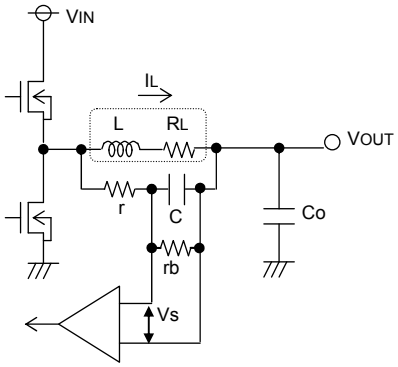
2.5 Bootstrap Capacitor

A 0.1uF ceramic capacitor must be connected between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. The capacitor should have 10V or higher voltage rating.

2.6 Inductor Current Sensing



Current Sense Amplifier



Current Sense Amplifier

The inductor current is sensed by current sense amplifier through resistor R. Current sense amplifier monitors difference voltage (=R*IL) and controls DCDC system. R should be above 5mΩ.

When the inductor current is sensed by inductor DC resistance (=RL), use the r, C and rb.

The resistor r calculated from following formula. ΔVs to be about 12mV, set the value of resistor r.

$$\Delta Vs = \frac{V_{IN} - V_{OUT}}{C \times r \times 1MHz} \times \frac{V_{OUT}}{V_{IN}}$$

Current Limit is determined by the value of rb and Temp_comp Voltage.
Over Current Protection (OCP) operate when Vs larger than Vocp. Vocp and Vs are calculated from following formula.

$$Vocp = 0.091 \times V_{TEMP\_COMP}$$

$$Vs = \frac{\Delta Vs}{2} + R_L \times I_{OUT} \times \frac{rb}{r + rb}$$

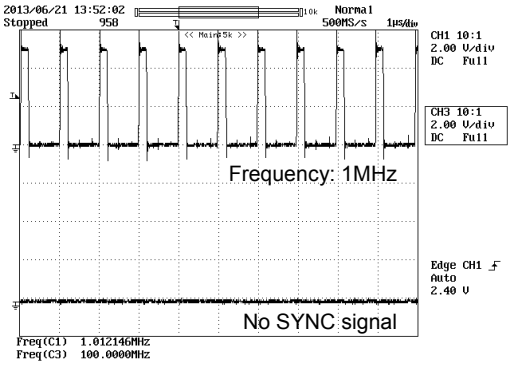
OCP temp coefficiency which is caused by DCR of inductor can be compensated by changing TEMP_COMP voltage with the external temperature. Thermistor can be used to it.

2.7 **SYNC function**

The SYNC pin is used to synchronize the DC/DC switching frequency with external clock. SYNC input frequency range is from 1.8MHz to 2.2MHz, and SYNC input pulse duty range is from 45% to 55%. SYNC input clock is divided to half frequency internally for DC/DC switching clock. Thus DC/DC switching frequency will be 0.9MHz to 1.1MHz. The clock input can be applied at anytime. This pin can be remained open if synchronization is not need. (Default frequency is 1MHz.)

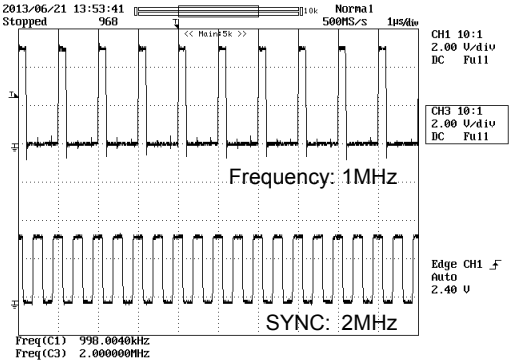
SW_V1P0A (2V/div)

SYNC (2V/div)



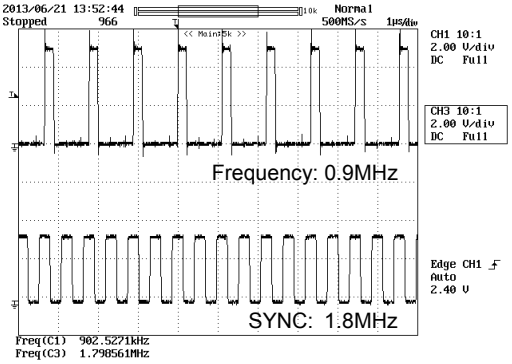
SW_V1P0A (2V/div)

SYNC (2V/div)



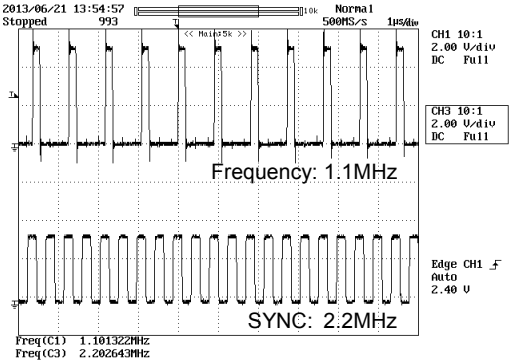
SW_V1P0A (2V/div)

SYNC (2V/div)



SW_V1P0A (2V/div)

SYNC (2V/div)



3. Electrical Characteristics

3.1 **Absolute Maximum Ratings (Ta=25ºC)**

Table 7: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage1	V5IN_D, V5IN_A	7 (Note 1)	V
Input Voltage2	1.8VIN	4.5 (Note 1)	V
Input Voltage3	VDDQIN	4.5 (Note 1)	V
Input Voltage4	VDD1, VDD2, VDD3	7 (Note 1)	V
Input Voltage5	V3P3DIN	4.5	V
BOOT to SW Voltage	BOOT_V1P0S-SW_V1P0S, BOOT_VNN-SW_VNN, BOOT_VCC-SW_VCC, BOOT_VDDQ-SW_ VDDQ	7 (Note 1)	V
SW to GND Voltage	SW_V1P0A, SW_V1P0S, SW_V1P8A, SW_VNN, SW_VCC, SW_VDDQ	7 (Note 1)	V
Logic Input Voltage	SLP_S3_B, SLP_S4_B, SUSPWRDNACK, SDMMC3_PWREN_B, SDMMC3_1P8_EN, SVID_CLK, SVID_DATA, POWER_ON, SYNC, DATA	4.5	V
Logic Output Voltage	RSMRST_B, DRAMPWROK, COREPWROK, RTEST_B, PWRBTN_B, SUS_STAT_B, SVID_ALERT_B, CLK, DATA, SRTC_RSR_B, ERROR, SPARE OUTPUT, SVID_DATA	4.5	V
Logic Output Pin Current Low1	RSMRST_B, DRAMPWROK, COREPWROK, RTEST_B, PWRBTN_B, SUS_STAT_B, CLK, DATA, SRTC_RSR_B, ERROR, SPARE OUTPUT	-3	mA
Logic Output Pin Current Low2	SVID_ALERT_B, SVID_DATA	-20	mA
Logic Output Pin Current High	SUS_STAT_B, SRTC_RSR_B, ERROR	3	mA
Power Dissipation	Pd	9.5(Note 2)	W
Operating Temperature Range	Topr	-40 to +95	°C
Storage Temperature Range	Tstg	-55 to +150 (Note 3)	°C
Junction Temperature Range	Tjmax	+150	°C

(Note 1) Do not exceed Pd.
(Note 2) A measure value at mounting on 8 layers board of 95mm*95mm*1.6mm.
(Surface: product pattern + 7 layers: all copper foil area)
In the case of exceeding Ta=25°C, 75.7 W should be reduced per 1 °C.
(Note 3) Operation is not guaranteed.

3.2 **Recommended Operating Conditions (Ta=25ºC)**

Table 8: Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Power Supply Voltage1	V5IN_D, V5IN_A	3.5	5.0	5.5	V
Power Supply Voltage2	1.8VIN	-	V1P8A	-	V
Power Supply Voltage3	VDDQIN	-	VDDQ	-	V
Power Supply Voltage4	VDD1, VDD2, VDD3	3.5	5.0	5.5	V
Power Supply Voltage5	V3P3DIN	-	VRTC	-	V
BOOT to SW Voltage	BOOT_V1P0S-SW_V1P0S, BOOT_VNN-SW_VNN, BOOT_VCC-SW_VCC, BOOT_VDDQ-SW_ VDDQ	3.5	-	5.5	V
Logic Input Voltage Low1 (3.3V Input)	POWER_ON, SYNC, DATA	-0.3	-	0.7	V
Logic Input Voltage High1 (3.3V Input)	POWER_ON, SYNC, DATA	VRTC-0.7	-	VRTC+0.3	V
Logic Input Voltage Low2 (1.8V Input)	SLP_S3_B, SLP_S4_B, SUSPWRDNACK	-0.3	-	V1P8A*1/3	V
Logic Input Voltage High2 (1.8V Input)	SLP_S3_B, SLP_S4_B, SUSPWRDNACK	V1P8A*2/3	-	V1P8A+0.3	V
Logic Input Voltage Low3 (1.8V Input)	SDMMC3_PWREN_B, SDMMC3_1P8_EN	-0.3	-	V1P8S*1/3	V
Logic Input Voltage High3 (1.8V Input)	SDMMC3_PWREN_B, SDMMC3_1P8_EN	V1P8S*2/3	-	V1P8S+0.3	V
Logic Input Voltage Low4 (1.0V Input)	SVID_CLK, SVID_DATA	-0.3	-	0.45	V
Logic Input Voltage High4 (1.0V Input)	SVID_CLK, SVID_DATA	0.65	-	1.0	V
TEMP_COMP Voltage	TEMP_COMP	0.28	-	1.0	V
SYNC Input Frequency Range	SYNC	1.8	2	2.2	MHz
SYNC Input Pulse Duty Range	SYNC	45	50	55	%

3.3 **DC Characteristics**

Table 9: DC Characteristics
(Unless otherwise noted, Ta=25°C, V5IN_D=V5IN_A=5V, POWER_ON=3.3V)

Parameter	Symbol	Standard value			Unit	Conditions
		MIN	TYP	MAX		
[Total Block]						
Bias Current1	ICC_V5IN_A_1	-	6.5	9.5	mA	S4/S5 state, non-switching FB1=1.15V, FB2=1.9V, IS-3=1.2V, IS-5=1V, FB4=3.4V
Bias Current2	ICC_V5IN_A_2	-	9.0	12.6	mA	S3 state, non-switching FB1=1.15V, FB2=1.9V, IS-3=1.2V, IS-5=1V, FB4=3.4V
Bias Current3	ICC_V5IN_A_3	-	22.0	30.5	mA	S0 state, non-switching FB1=1.15V, FB2=1.9V, IS-3=1.2V, IS-5=1V, FB4=3.4V
[Under Voltage Lock-Out Block]						
V5IN_A Threshold Voltage	V5IN_A_UVLO	3.1	3.3	3.5	V	V5IN_A: Sweep up
V5IN_A Hysterics Voltage	dV5IN_A_UVLO	50	100	150	mV	V5IN_A: Sweep down
(S4/S5 State)						
[VRTC Block]						
Output Voltage	VRTC	3.168	3.300	3.432	V	Io=0mA
On Resistance	Ronvrtc	-	-	1.4	Ω	Ids=50mA
Over Current Protection	OCP_vrtc	140	-	-	mA	
SCP Detecting Voltage	SCP_vrtc	VRTCx0.55	VRTCx0.7	VRTCx0.85	V	
[Reference Clock Block]						
Reference Clock Frequency	F_{RTC}	31.130	32.768	34.406	KHz	
[V3P3A Block]						
Output Voltage	V3P3A	3.234	3.300	3.366	V	Io=0mA
On Resistance	Ronv3p3a	-	-	1.4	Ω	Ids=50mA
Over Current Protection	OCP_v3p3a	140	-	-	mA	
SCP Detecting Voltage	SCP_v3p3a	V3P3Ax0.55	V3P3Ax0.7	V3P3Ax0.85	V	
[V1P24A Block]						
Output Voltage	V1P24A	1.215	1.240	1.265	V	Io=0mA
On Resistance	Ronv1p24a	-	-	10	Ω	Ids=50mA
Over Current Protection	OCP_v1p24a	60	-	-	mA	
SCP Detecting Voltage	SCP_v1p24a	V1P24Ax0.55	V1P24Ax0.7	V1P24Ax0.85	V	
[V1P0A Block]						
Output Voltage	V1P0A	0.980	1.000	1.020	V	Io=0mA
Switching Frequency	Foscv1p0a	900	1000	1100	KHz	
Synchronization Frequency	Fsync	-	1.0	-	MHz	SYNC=2MHz
Soft Start Time	Tss_v1p0a	-	1	-	ms	
Upper Side On Resistance	Ronh_ v1p0a	-	120	-	mΩ	
Lower Side On Resistance	Rohnl_v1p0a	-	120	-	mΩ	
Over Current Protection	OCP_v1p0a	900	-	-	mA	
SCP Detecting Voltage	SCP_v1p0a	V1P0Ax0.55	V1P0Ax0.7	V1P0Ax0.85	V	
OVP Detecting Voltage	OVP_v1p0a	V1P0Ax1.1	V1P0Ax1.2	V1P0Ax1.3	V	
[V1P8A Block]						
Output Voltage	V1P8A	1.764	1.800	1.836	V	Io=0mA
Switching Frequency	Foscv1p8a	900	1000	1100	KHz	
Synchronization Frequency	Fsync	-	1.0	-	MHz	SYNC=2MHz
Soft-Start Time	Tss_v1p8a	-	1	-	ms	
Upper-Side On Resistance	Ronh_ v1p8a	-	120	-	mΩ	
Lower-Side On Resistance	Rohl_v1p8a	-	120	-	mΩ	
Over-Current Protection	OCP_v1p8a	2800	-	-	mA	
SCP Detecting Voltage	SCP_v1p8a	V1P8Ax0.55	V1P8Ax0.7	V1P8Ax0.85	V	
OVP Detecting Voltage	OVP_v1p8a	V1P8Ax1.1	V1P8Ax1.2	V1P8Ax1.3	V	

(S3 state)						
[VDDQ Block for DDR]						
Reference Voltage	VREF_DDR	0.784	0.8	0.816	V	Io=0mA
Switching Frequency	Fosc_DDR	900	1000	1100	KHz	
Synchronization Frequency	Fsync	-	1.0	-	MHz	SYNC=2MHz
Soft-Start Time	Tss_DDR	-	1	-	ms	
HG High-Side ON Resistance	HGHRON	-	-	7	Ω	(Note 1)
HG Low-Side ON Resistance	HGLRON	-	-	5	Ω	(Note 1)
LG High-Side ON Resistance	LGHRON	-	-	8	Ω	(Note 2)
LG Low-Side ON Resistance	LGLRON	-	-	1.5	Ω	(Note 2)
Over-Current Setting Voltage	OCP_DDR	45	50	55	mV	TEMP_COMP=0.55V
SCP Detecting Voltage	SCP_DDR	VDDQx0.55	VDDQx0.7	VDDQx0.85	V	
OVP Detecting Voltage	OVP_DDR	VDDQx1.1	VDDQx1.2	VDDQx1.3	V	
(S0 state)						
[VCC Block]						
Output Setting Voltage Range	VCC	0.5	-	1.2	V	
Output Voltage Accuracy	dVCC	SVIDx0.97	SVID	SVIDx1.03	V	Io=0mA
Switching Frequency	Foscvcc	900	1000	1100	KHz	
Synchronization Frequency	Fsync	-	1.0	-	MHz	SYNC=2MHz
Soft-Start Time	Tss_vcc	-	1	-	ms	
HG High-Side ON Resistance	HGHRON	-	-	7	Ω	(Note 1)
HG Low-Side ON Resistance	HGLRON	-	-	5	Ω	(Note 1)
LG High-Side ON Resistance	LGHRON	-	-	8	Ω	(Note 2)
LG Low-Side ON Resistance	LGLRON	-	-	1.5	Ω	(Note 2)
Over-Current Setting Voltage	OCP_vcc	45	50	55	mV	TEMP_COMP=0.55V
SCP Detecting Voltage	SCP_vcc	SVIDx0.55	SVIDx0.7	SVIDx0.85	V	
OVP Detecting Voltage	OVP_vcc	1.40	1.56	1.72	V	
[VNN Block]						
Output Setting Voltage Range	VNN	0.5	-	1.2	V	
Output Voltage Accuracy	dVNN	SVIDx0.97	SVID	SVIDx1.03	V	Io=0mA
Switching Frequency	Foscvnn	900	1000	1100	KHz	
Synchronization Frequency	Fsync	-	1.0	-	MHz	SYNC=2MHz
Soft-Start Time	Tss_vnn	-	1	-	ms	
HG High-Side ON Resistance	HGHRON	-	-	7	Ω	(Note 1)
HG Low-Side ON Resistance	HGLRON	-	-	5	Ω	(Note 1)
LG High-Side ON Resistance	LGHRON	-	-	8	Ω	(Note 2)
LG Low-Side ON Resistance	LGLRON	-	-	1.5	Ω	(Note 2)
Over-Current Setting Voltage	OCP_vnn	45	50	55	mV	TEMP_COMP=0.55V
SCP Detecting Voltage	SCP_vnn	SVIDx0.55	SVIDx0.7	SVIDx0.85	V	
OVP Detecting Voltage	OVP_vnn	1.40	1.56	1.72	V	
[V3P3S Block]						
Output Voltage	V3P3S	3.234	3.300	3.366	V	Io=0mA
On Resistance	Ronv3p3s	-	-	250	mΩ	Ids=50mA
Over-Current Protection	OCP_v3p3s	600	-	-	mA	
SCP Detecting Voltage	SCP_v3p3s	V3P3Sx0.55	V3P3Sx0.7	V3P3Sx0.85	V	
[V1P8S Block]						
On Resistance	Ron_v1p8s	-	-	85	mΩ	Ids=50mA
Over-Current Protection	OCP_v1p8s		-	-	mA	
[V1P24S Block]						
Output Voltage	V1P24S	1.215	1.240	1.265	V	Io=0mA
On Resistance	Ronv1p24s	-	-	700	mΩ	Ids=50mA
Over-Current Protection	OCP_v1p24s	700	-	-	mA	
SCP Detecting Voltage	SCP_v1p24s	V1P24Sx0.55	V1P24Sx0.7	V1P24Sx0.85	V	

[VTT Block]						
Output Voltage	VTT	1/2×VDDQ-5%	1/2×VDDQ	1/2×VDDQ+5%	V	Io=0mA
High-Side On Resistance	Hron_VTT	-	-	500	mΩ	Ids=50mA
Low-Side On Resistance	Lron_VTT	-	-	500	mΩ	Ids=50mA
SCP Detecting Voltage	SCP_VTT	VTTx0.55	VTTx0.7	VTTx0.85	V	
[VSDIO Block]						
Output Voltage 1	VSDIO18	1.764	1.800	1.836	V	Io=0mA SDMMC3_PWR_EN_B=0 SDMMC3_1P8_EN=1
Output Voltage 2	VSDIO33	3.234	3.300	3.366	V	Io=0mA SDMMC3_PWR_EN_B=0 SDMMC3_1P8_EN=0
On Resistance	Ronvsdio	-	-	5	Ω	Ids=50mA
Over-Current Protection	OCP_vsdio	40	-	-	mA	
SCP Detecting Voltage	SCP_vsdio	VSDIOx0.55	VSDIOx0.7	VSDIOx0.85	V	
[VSFR Block]						
Output Voltage	VSFR	1.323	1.350	1.377	V	
On Resistance	Ronvsfr	-	-	700	mΩ	Ids=50mA
Over-Current Protection	OCP_vsfr	700	-	-	mA	
SCP Detecting Voltage	SCP_vsfr	VSFRx0.55	VSFRx0.7	VSFRx0.85	V	
[V1P0S Block]						
Output Voltage	V1P0S	0.980	1.000	1.020	V	Io=0mA
Switching Frequency	Foscv1p0s	900	1000	1100	KHz	
Synchronization Frequency	Fsync	-	1.0	-	MHz	SYNC=2MHz
Soft-Start Time	Tss_v1p0s	-	1	-	ms	
HG High-Side ON Resistance	HGHRON	-	-	7	Ω	(Note 1)
HG Low-Side ON Resistance	HGLRON	-	-	5	Ω	(Note 2)
LG High-Side ON Resistance	LGHRON	-	-	8	Ω	(Note 2)
LG Low-Side ON Resistance	LGLRON	-	-	1.5	Ω	(Note 2)
Over-Current Setting Voltage	OCP_v1p0s	45	50	55	mV	TEMP_COMP=0.55V
SCP Detecting Voltage	SCP_v1p0s	V1P0Ax0.55	V1P0Ax0.7	V1P0Ax0.85	V	
OVP Detecting Voltage	OVP_v1p0s	V1P0Ax1.1	V1P0Ax1.2	V1P0Ax1.3	V	
[V1P05S Block]						
Output Voltage	V1P05S	1.029	1.050	1.071	V	Io=0mA
Switching Frequency	Foscv1p05s	900	1000	1100	KHz	
Synchronization Frequency	Fsync	-	1.0	-	MHz	SYNC=2MHz
Soft-Start Time	Tss_v1p05s	-	1	-	ms	
Upper-Side On Resistance	Ronh_ v1p05s	-	120	-	mΩ	
Lower-Side On Resistance	Ronl_v1p05s	-	120	-	mΩ	
Over-Current Protection	OCP_v1p05s	2000	-	-	mA	
SCP Detecting Voltage	SCP_v1p05s	V1P05S x0.55	V1P05S x0.7	V1P05S x0.85	V	
OVP Detecting Voltage	OVP_v1p05s	V1P05S x1.1	V1P05S x1.2	V1P05S x1.3	V	

(Note 1) HG swings from SW to BOOT.
(Note 2) LG swings from VDD to PGND.

Table 10: Logic Characteristics
(Unless otherwise noted, Ta=25°C, V5IN_D=V5IN_A=5V, POWER_ON=3.3V)

Parameter	Symbol	Standard Value			Unit	Conditions
		MIN	TYP	MAX		
[Logic Block]						
[Logic Output Voltage High1] (3.3V output)						
SRTC_RST_B SUS_STAT_B RTCCLK ERROR	Logic_out_high1	VRTC-0.7	-	VRTC+0.3	V	Iload=3mA
[Logic Output Voltage Low1] (3.3V output)						
SRTC_RST_B SUS_STAT_B RTCCLK ERROR	Logic_out_low1	-0.3	-	0.7	V	Iload=-3mA
[Logic Output Voltage Low2] (open drain output)						
RSMRST_B DRAM_PWROK COREPWROK RTEST_B PWRBTN_B SPAREOUTPUT CLK,DATA	Logic_out_low2	-0.3	-	0.5	V	Iload=-3mA
[Logic Output Voltage Low3] (SVID output)						
SVID_ALERT_B SVID_DATA	Logic_out_low3	-0.3	-	0.3	V	Iload=-20mA

3.4 Protection Mode (Under Voltage Lock Out)

All power supplies will be shut down at the same time when the UVLO signal is detected. There is no sequence in this shutdown mode and BD9596BMWV cannot receive any external signals during this time.

3.5 Protection Mode (Thermal Shut Down)

A built-in internal shutdown (TSD) circuit is provided to protect the IC from heat destruction. Operation has to be done within the allowable loss range, and continuous use beyond the range will cause chip temperature Tj to increase and reach threshold consequently activating the TSD circuit to shut down all power supplies at the same time and latch OFF. There is no sequence in this shutdown mode and BD9596BMWV cannot receive any external signals during this time. It will reboot, if 5V supply or POWER_ON is toggled OFF and ON.
Hence, make absolutely certain not to use the TSD function in set design.

3.6 Protection Mode

Table 11 : Protection Mode (DC/DC)

Protection Mode	HG	LG	Function
UVLO Protection	Low	Low	Hysteresys
Short Circuit Protection	Low	Low	Timer latch (1ms)
Thermal Protection	Low	Low	Timer latch (10us)
Over Voltage Protection	Low	Low	Timer latch (10us)

Table 12 : Protection mode (LDO)

Protection Mode	Output	Function
UVLO Protection	Low	Hysteresys
Short Circuit Protection	Low	Timer latch (1ms)
Thermal Protection	Low	Timer latch (10us)

Table 13 : Protection mode (SW)

Protection Mode	Output	Function
UVLO Protection	Low	Hysteresys
Short Circuit Protection	Low	Timer latch (1ms)
Thermal Protection	Low	Timer latch (10us)

3.7 DAC Code for VCC and VNN

BD9596BMWV supports 2 SVID voltage regulators – VCC and VNN.
[Address Index]
0h : VCC
1h : VNN

Table 14: DAC Code Table (VCC / VNN)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	DAC Set point Accuracy (Design guarantee)
0	0	0	0	0	0	0	X	OFF	NA
0	0	1	1	0	0	1	X	0.5	+- 8mV
0	0	1	1	0	1	0	X	0.51	+- 8mV
0	0	1	1	0	1	1	X	0.52	+- 8mV
0	0	1	1	1	0	0	X	0.53	+- 8mV
0	0	1	1	1	0	1	X	0.54	+- 8mV
0	0	1	1	1	1	0	X	0.55	+- 8mV
0	0	1	1	1	1	1	X	0.56	+- 8mV
0	1	0	0	0	0	0	X	0.57	+- 8mV
0	1	0	0	0	0	1	X	0.58	+- 8mV
0	1	0	0	0	1	0	X	0.59	+- 8mV
0	1	0	0	0	1	1	X	0.6	+- 8mV
0	1	0	0	1	0	0	X	0.61	+- 8mV
0	1	0	0	1	0	1	X	0.62	+- 8mV
0	1	0	0	1	1	0	X	0.63	+- 8mV
0	1	0	0	1	1	1	X	0.64	+- 8mV
0	1	0	1	0	0	0	X	0.65	+- 5mV
0	1	0	1	0	0	1	X	0.66	+- 5mV
0	1	0	1	0	1	0	X	0.67	+- 5mV
0	1	0	1	0	1	1	X	0.68	+- 5mV
0	1	0	1	1	0	0	X	0.69	+- 5mV
0	1	0	1	1	0	1	X	0.7	+- 5mV
0	1	0	1	1	1	0	X	0.71	+- 5mV
0	1	0	1	1	1	1	X	0.72	+- 5mV
0	1	1	0	0	0	0	X	0.73	+- 5mV
0	1	1	0	0	0	1	X	0.74	+- 5mV
0	1	1	0	0	1	0	X	0.75	+- 5mV
0	1	1	0	0	1	1	X	0.76	+- 5mV
0	1	1	0	1	0	0	X	0.77	+- 5mV
0	1	1	0	1	0	1	X	0.78	+- 5mV
0	1	1	0	1	1	0	X	0.79	+- 5mV
0	1	1	0	1	1	1	X	0.8	+- 5mV
0	1	1	1	0	0	0	X	0.81	+- 5mV
0	1	1	1	0	0	1	X	0.82	+- 5mV
0	1	1	1	0	1	0	X	0.83	+- 5mV
0	1	1	1	0	1	1	X	0.84	+- 5mV
0	1	1	1	1	0	0	X	0.85	+- 5mV

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	DAC Set point Accuracy (Design guarantee)
0	1	1	1	1	0	1	X	0.86	+- 5mV
0	1	1	1	1	1	0	X	0.87	+- 5mV
0	1	1	1	1	1	1	X	0.88	+- 5mV
1	0	0	0	0	0	0	X	0.89	+- 5mV
1	0	0	0	0	0	1	X	0.9	+- 5mV
1	0	0	0	0	1	0	X	0.91	+- 5mV
1	0	0	0	0	1	1	X	0.92	+- 5mV
1	0	0	0	1	0	0	X	0.93	+- 5mV
1	0	0	0	1	0	1	X	0.94	+- 5mV
1	0	0	0	1	1	0	X	0.95	+- 5mV
1	0	0	0	1	1	1	X	0.96	+- 5mV
1	0	0	1	0	0	0	X	0.97	+- 5mV
1	0	0	1	0	0	1	X	0.98	+- 5mV
1	0	0	1	0	1	0	X	0.99	+- 5mV
1	0	0	1	0	1	1	X	1	+- 0.5% VID
1	0	0	1	1	0	0	X	1.01	+- 0.5% VID
1	0	0	1	1	0	1	X	1.02	+- 0.5% VID
1	0	0	1	1	1	0	X	1.03	+- 0.5% VID
1	0	0	1	1	1	1	X	1.04	+- 0.5% VID
1	0	1	0	0	0	0	X	1.05	+- 0.5% VID
1	0	1	0	0	0	1	X	1.06	+- 0.5% VID
1	0	1	0	0	1	0	X	1.07	+- 0.5% VID
1	0	1	0	0	1	1	X	1.08	+- 0.5% VID
1	0	1	0	1	0	0	X	1.09	+- 0.5% VID
1	0	1	0	1	0	1	X	1.1	+- 0.5% VID
1	0	1	0	1	1	0	X	1.11	+- 0.5% VID
1	0	1	0	1	1	1	X	1.12	+- 0.5% VID
1	0	1	1	0	0	0	X	1.13	+- 0.5% VID
1	0	1	1	0	0	1	X	1.14	+- 0.5% VID
1	0	1	1	0	1	0	X	1.15	+- 0.5% VID
1	0	1	1	0	1	1	X	1.16	+- 0.5% VID
1	0	1	1	1	0	0	X	1.17	+- 0.5% VID
1	0	1	1	1	0	1	X	1.18	+- 0.5% VID
1	0	1	1	1	1	0	X	1.19	+- 0.5% VID
1	0	1	1	1	1	1	X	1.2	+- 0.5% VID

*00h is off code that makes SVID bus idle, waiting for next instruction.

3.8 **Serial VID Command**

Table 15: Serial VID Command Table

#	Command	Master payload contents	Slave payload contents	Description
00h	Extended	Extended command index		This command is not supported. The PMIC will respond with Reject acknowledge (11b).
01h	SetVID-fast (Individual address & all call address)	VID code	NA	Applicable for VCC & VNN. Upon setting new VID target, VR changes to reach new VID target with controlled (up or down) slew rate programmed by the VR. When VR receives VID moving up command it will exit all low power states and proceed to the normal state. VR sets VR_settled bit and issues alert when VR has reached new VID target. Note that only one slew rate is supported (SR-fast=SR-slow). (see registers 24h, 25h)
02h	SetVID-slow (Individual address & all call address)	VID code	NA	Applicable for VCC & VNN. Upon setting new VID target, VR changes to reach new VID target with controlled (up or down) slew rate programmed by the VR. When VR receives VID moving up command it will exit all low power states and proceed to the normal state. VR sets VR_settled bit and issues alert when VR has reached new VID target. Note that only one slew rate is supported (SR-fast=SR-slow). (see registers 24h, 25h)
03h	SetVID-decay (Individual address & all call address)	VID code	NA	Applicable for VCC & VNN. Upon setting the VID target, VR changes to reach new VID target with controlled slew rate (mV/us). The SetVID_decay is only used in VID down direction. VR sets VR_settled bit but Alert line is not asserted for SetVID-decay.
04h	SetPS	Byte indicating power status of voltage rail	NA	This command is not supported. Executing this command has no effect to the function of the PMIC. However PMIC responds with ACK=10b for SetPS(00h..03h). SetPS(04h..FFh) should be rejected with ACK=11b as these states are not supported or defined.
05h	SetRegADR (Individual address only. NAK all call address)	Address of the index in the data table	NA	Sets the address pointer in the data register table. Typically the next command SetRegDAT is the payload that gets loaded into this address. However for multiple writes to the same address, only one SetRegADR is needed.
06h	SetRegDAT (Individual address only. NAK all call address)	New data register contents	NA	Writes the contents to the data register that was previously identified by the address pointer with SetRegADR.
07h	GetReg (Individual address only. NAK all call address)	Define which register	Specified register contents	Slave returns the contents of the specified register as the payload; see 3.9 Register Code for list of registers. The majority of the VR monitoring data is accessed through the GetReg command.

For the details of command transaction structure, please refer to VR12/ IMVP7 SVID Protocol (Document number: 456098).

3.9 **Register Code**

Table 16: Register Code Table

#	Register	Description	Access (SOC)	Default
00h	Vendor ID	Required: Uniquely identifies the VR vendor. The vendor ID is assigned by Intel. This register is mandatory and the VR must return the assigned vendor ID.	RO Vendor	Note 1 1Fh
01h	Product ID	Required: Uniquely identifies the VR product. The VR vendor assigns this number.	RO Vendor	Note 1 20h
02h	Product Revision	Required: Uniquely identifies the revision or stepping of the VR control IC. The vendor assigns this data.	RO Vendor	Note 1 06h
03h	Product date Code	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO Vendor	Note 1,3
04h	Lot Code	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 1,3
05h	Protocol ID	Required: PMIC response is ACK=10b. Content of payload is 01h.	RO Vendor	Note 1
06h	Capability	Required: Bit mapped register, identifies the SVID VR capabilities and which of the optional telemetry registers are supported. PMIC responds with ACK=10b, content of payload is 00h indicating none of the functions listed below are supported. Bit0= Iout ADC (15h) bit1= Vout ADC (16h) bit2= Pout ADC (18h) bit3= I input ADC (19h) Bit4= V input ADC (1Ah) bit5= P input ADC (1Bh) bit6= Temperature ADC (17h) bit7= 0 if (15h) is formatted 1A per LSB, Legacy for Servers Only bit7= 1 if (15h) is formatted FFh=Icc_max for Client and optional for server ADC formatting.	RO Vendor	00h Note 2
07h	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
08h	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
09h	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
0Ah	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
0Bh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
0Ch	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
0Dh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
0Eh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
0Fh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3

10h	Status_1	Required: Data register read after the alert# signal is asserted. Conveying the status of the VR. See 6.2.1 in the IMVP7 SVID protocol. In Jarrell Cove, bit2 alerts SCP(OVP) and bit1 alerts TSD.	R-M W-PWM	00h Note 2
11h	Status_2	Required: Data Register showing status_2 data. Conveying the status of the SVID bus. See 6.2.1 in the IMVP7 SVID protocol.	R-M W-PWM	00h Note 2
12h	Temperature Zone	Required, but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	00h Note 2
13h	Current Zones	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
14h	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
15h	Output Current	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	00h Note 2
16h	Output Voltage	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 2,3
17h	VR Temperature	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 2,3
18h	Output Power (Pout)	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 2,3
19h	Input current	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 2,3
1Ah	Input Voltage	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 2,3
1Bh	Input Power	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 2,3
1Ch	Status2_last read	Required: This register contains a copy of the status2 data that was last read with the GetReg (status2) command. In the case of a communications error or parity error, when the VR is sending the payload back to the master, the master can read the Status2_lastread register so the alert data is not lost.	R-M W-PWM	Note 2
1Dh	V1P0A/VDDQ Output Current, Imon (H)	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
1Eh	V1P0A/VDDQ Output Current, Imon (L)	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
1Fh	V1P05S Output Current, Imon (H)	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
20h	V1P05S Output Current, Imon (L)	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
21h	ICC_MAX	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
22h	Temp max	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2

23h	DC_LL	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 2,3
24h	SR-fast	Required: The PMIC supports only one slew rate. Fast slew rate is equal to slow slew rate. The PMIC responds with ACK=10b. Content of payload is 0Ah.	RO	0Ah = 10 mV/us Note 2
25h	SR-slow	Required: The PMIC supports only one slew rate. Fast slew rate is equal to slow slew rate. The PMIC responds with ACK=10b. Content of payload is 0Ah.	RO	0Ah = 10 mV/us Note 2
26h	Vboot	Required: Vboot=1.00V fix for VNN and VCC. No Pin programming is needed. PMIC responds with ACK=10b.Content of payload is 97h.	RO	Note 2
27h	VR tolerance	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
28h	Current-offset	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
29h	Temperature offset	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
2Ah	VCC/VNN Imon Accuracy	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is FFh.	RO	Note 2
2Bh	V1P0A/VDDQ Imon Accuracy	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is FFh.	RO	Note 2
2Ch	V1P05S Imon Accuracy	Required but not supported: This function is not supported. The PMIC responds with ACK=10b. Content of payload is FFh.	RO	Note 2
2Dh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
2Eh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
2Fh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
30h	Vout max	Required: This register is programmable by the master and sets the maximum VID the VR will be able to support. If a higher VID code is received, the VR will respond with “Reject, not supported” acknowledgement. VR12 VID data format. Must be programmed by MASTER during boot up sequence if a value other than default is desired. Offset (33h) does not affect Vout_max IE VID + offset can be >Vout_max	RW master	D3h Note 2
31h	VID setting	Required: Data register containing currently programmed VID voltage. VID data format: Default is 00h, zero volts out, VR off.	RW Master	00h Note 2
32h	Pwr state	Required but not supported: PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2

33h	Offset	Required: Sets offset in VID steps added to the VID setting for voltage margining. Bit7 is sign bit, 0=positive margin 1= negative margin. Remaining 7 BITS are the number of VID steps for the margin 2s complement. 00h= no margin. 01h=+1 VID step, 02h=+2 VID steps FFh=-1 VID step…	RW Master	00h Note 2
34h	Multi VR config	Required but not supported: PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
35h	SetRegADR	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
36h	Trim code 1 revision	Required but not supported: PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
37h	Trim code 2 revision	Required but not supported: PMIC responds with ACK=10b. Content of payload is 00h.	RO	Note 2
38h	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
39h	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
3Ah	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
3Bh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
3Ch	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
3Dh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
3Eh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
3Fh	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3
40h	reserved	Optional: This function is not supported. The PMIC responds with Reject acknowledge (11b).	RO	Note 3

Notes:
1. These registers only appear in 00h voltage rail. (“Reject” for 01h voltage rail.)
2. These registers are per address and not shared.
3. Optional register response – VR should respond with a Reject (11b) ACK if a GetReg command is issued to an optional data register.

Status1 Register bit[2], bit[1] (10h)

In Jarrell Cove, the function of the Status1 Register bit[2] and bit[1] are different from the original SVID Protocol. Bit[2] alerts SCP/OVP while bit[1] alerts TSD, and the ALERT# line is not asserted.

Bit[2] of 00h voltage rail (VCC) shows the status of SCP/OVP for VCC.
Bit[2] of 01h voltage rail (VNN) shows the status of SCP/OVP for VNN.
Bit[1] of both VCC and VNN show the same status of TSD.

The status of SCP/OVP for the power rails other than VCC and VNN are not shown in Status1 Register.

When POWER_ON=0, the timer-latch is reset and the ERROR output is disabled. But the Status1 Register bit[2] and bit[1] are latched until they are read by GetReg command.

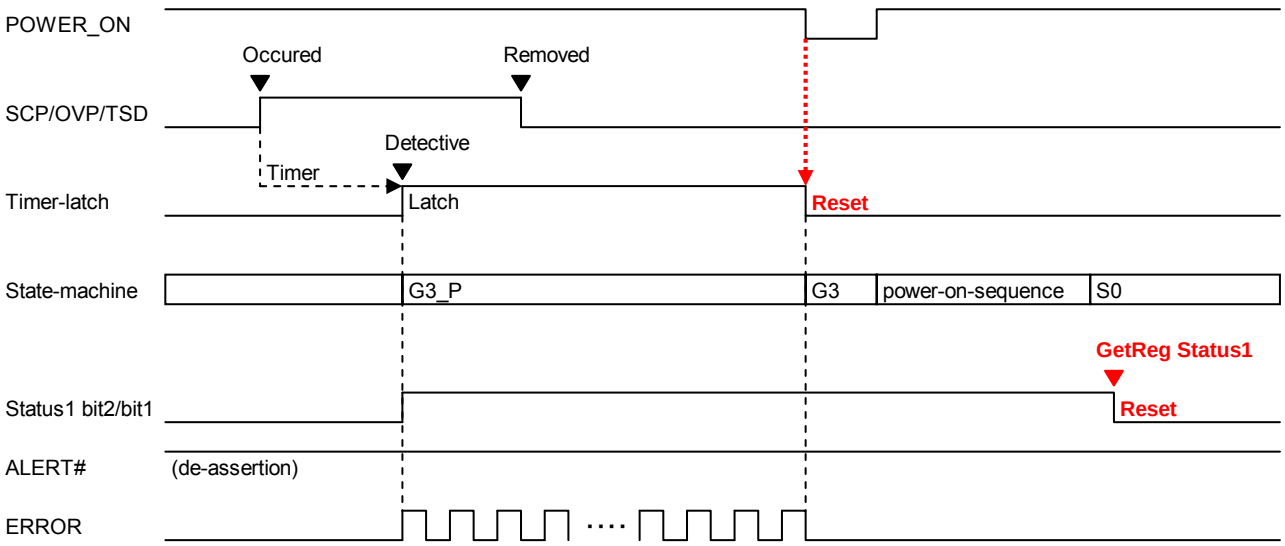


Figure 10. Status1 Timing Chart

4. Typical Performance Curves

4.1 Load Regulation

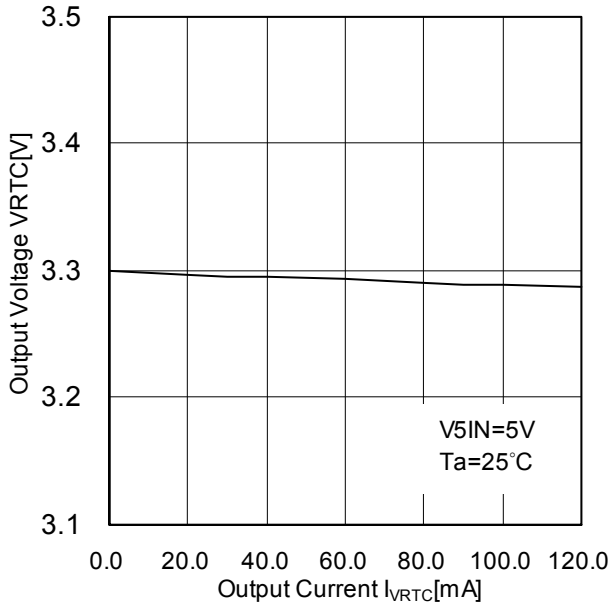


Figure 11. Output Voltage VRTC vs Output Current I_{VRTC}

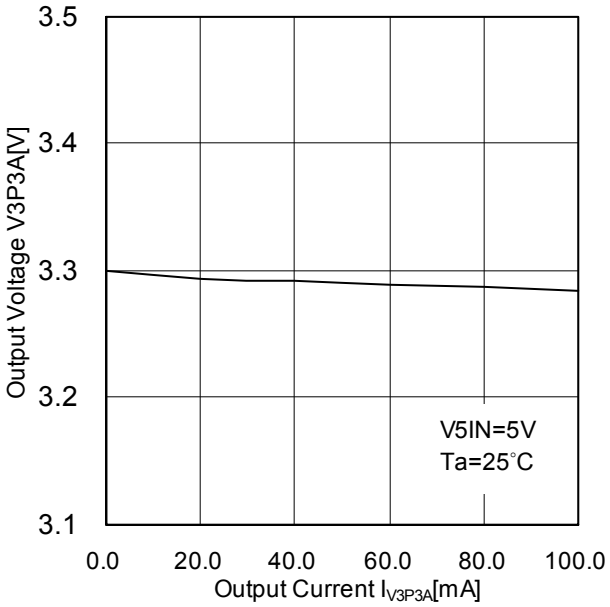


Figure 12. Output Voltage V3P3A vs Output Current I_{V3P3A}

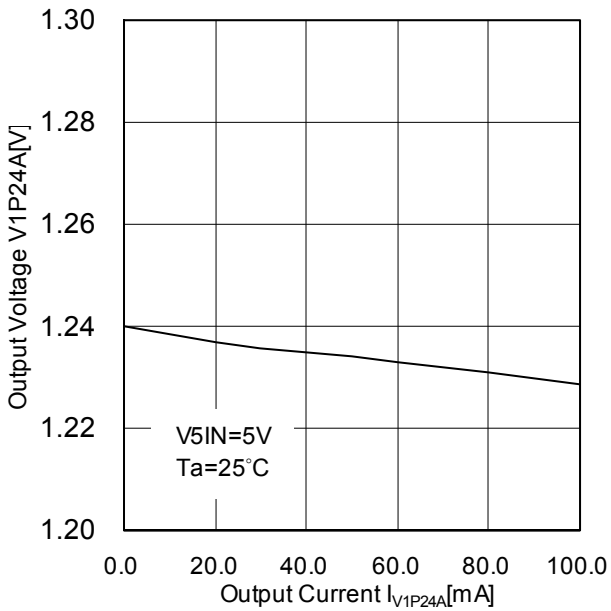


Figure 13. Output Voltage V1P24A vs Output Current I_{V1P24A}

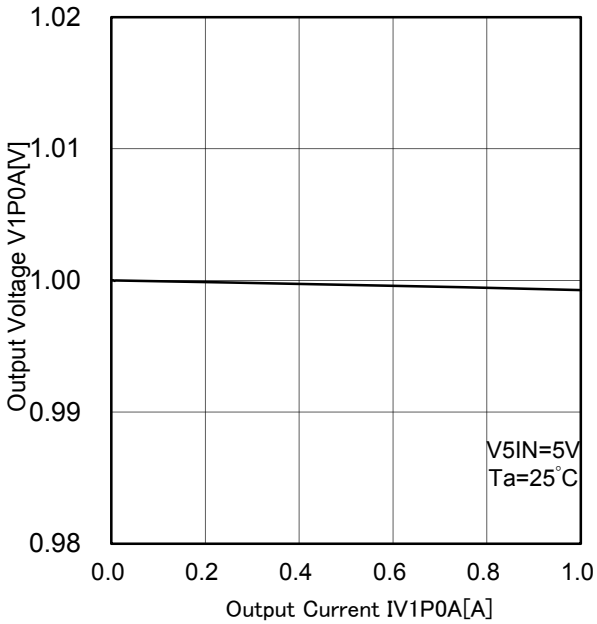


Figure 14. Output Voltage V1P0A vs Output Current I_{V1P0A}

Typical Performance Curves - Continued

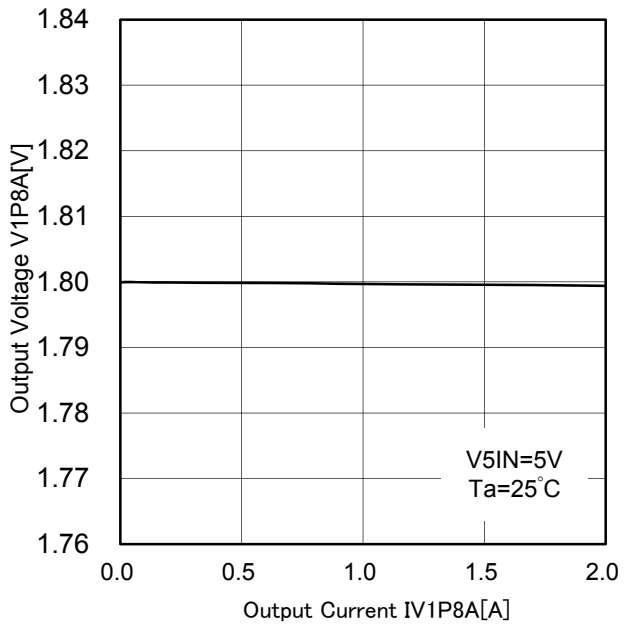


Figure 15. Output Voltage V1P8A vs Output Current I_{V1P8A}

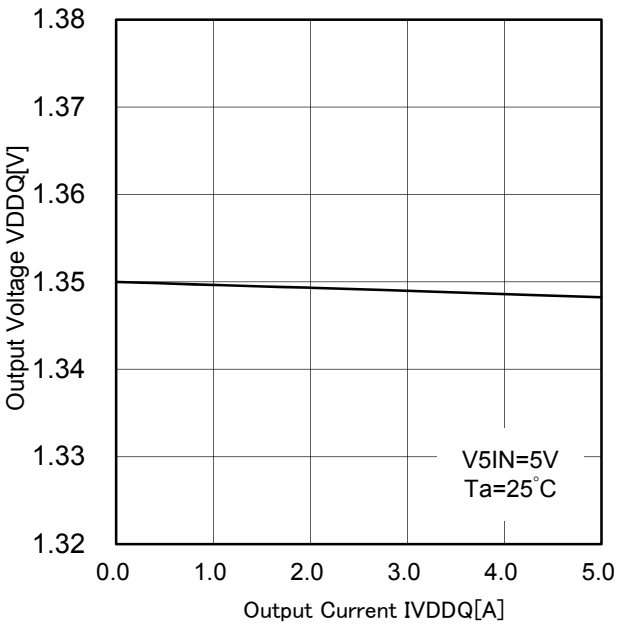


Figure 16. Output Voltage VDDQ vs Output Current I_{VDDQ}

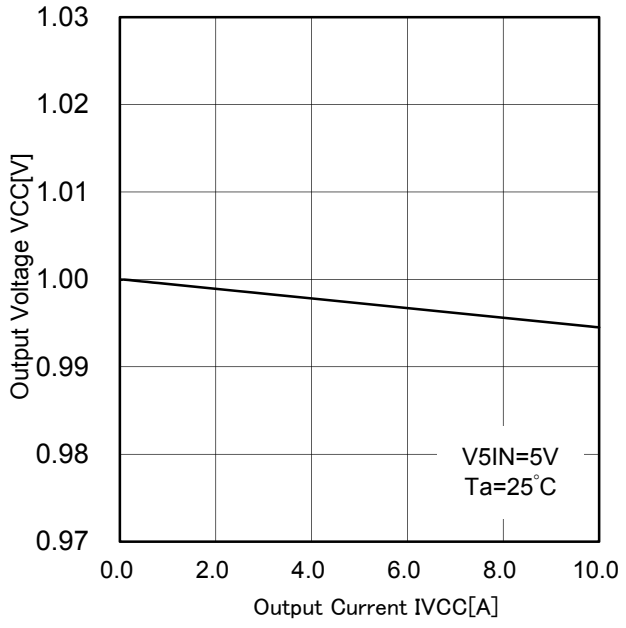


Figure 17. Output Voltage VCC vs Output Current I_{VCC}

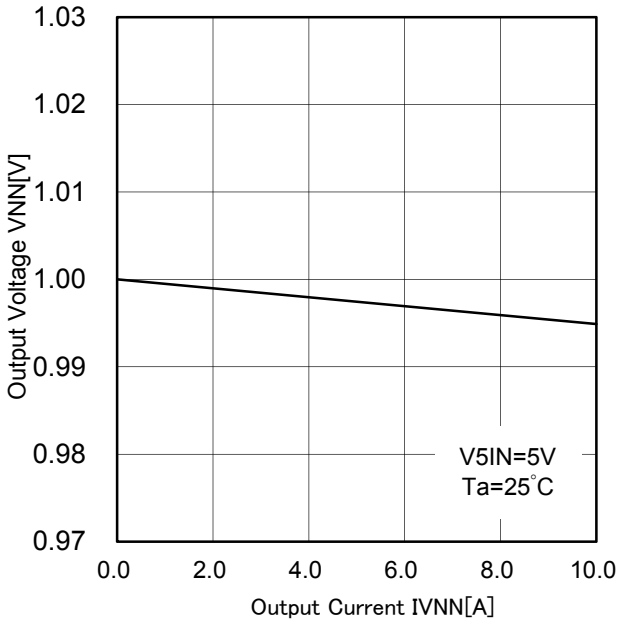


Figure 18. Output Voltage VNN vs Output Current I_{VNN}

Typical Performance Curves - Continued

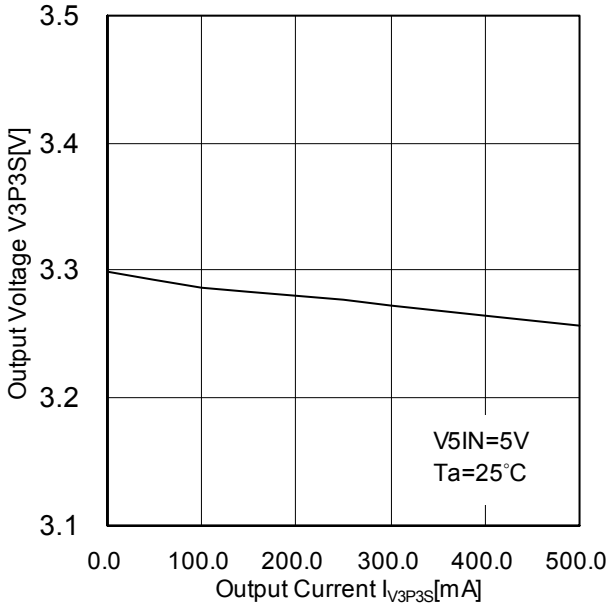


Figure 19. Output Voltage V3P3S vs Output Current I_{V3P3S}

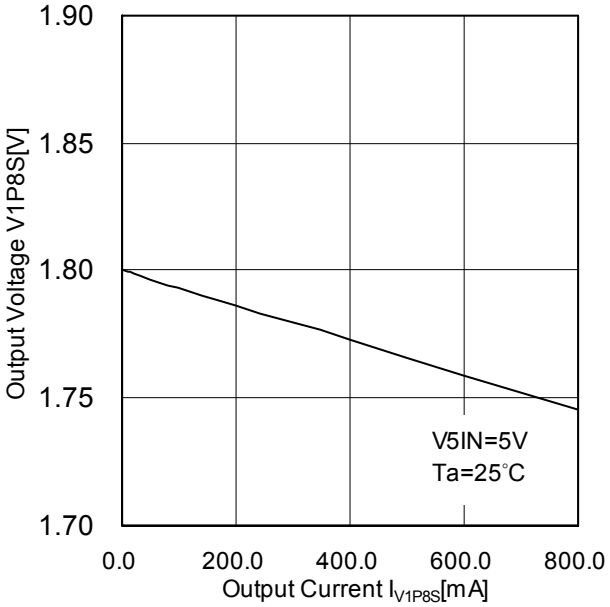


Figure 20. Output Voltage V1P8S vs Output Current I_{V1P8S}

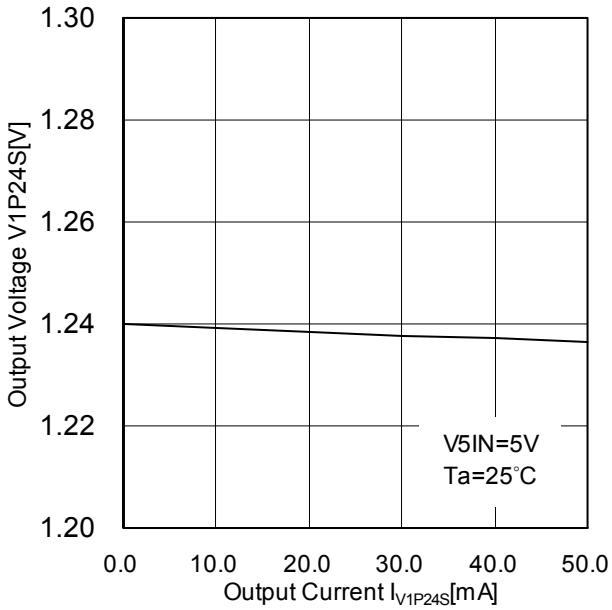


Figure 21. Output Voltage V1P24S vs Output Current I_{V1P24S}

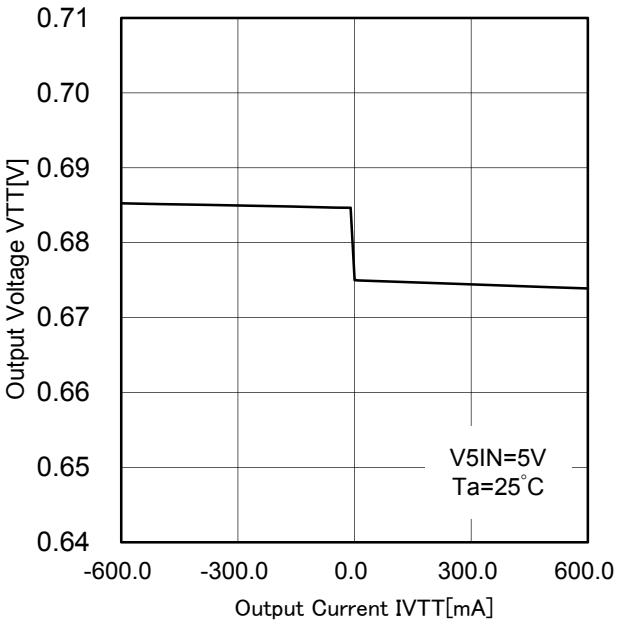


Figure 22. Output Voltage VTT vs Output Current I_{VTT}

Typical Performance Curves - Continued

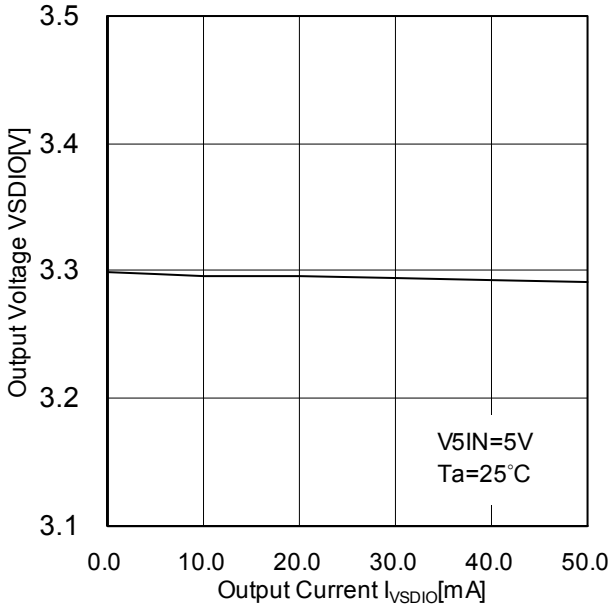


Figure 23. Output Voltage VSDIO vs Output Current I_{VSDIO}
(SDMMC3_1P8_EN = 0V)

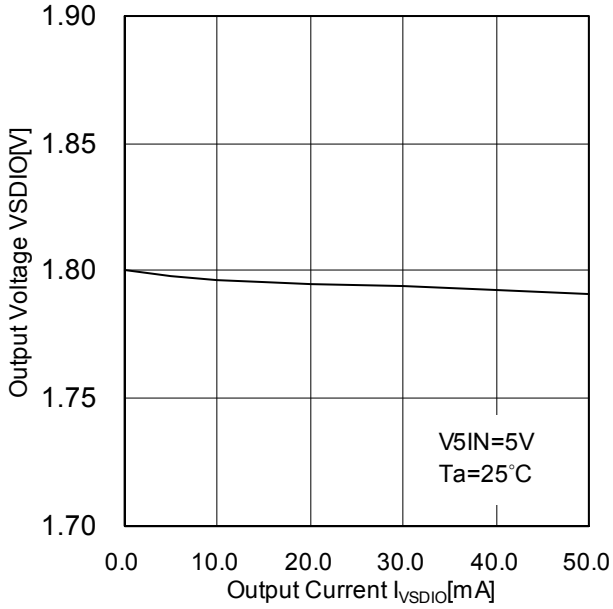


Figure 24. Output Voltage VSDIO vs Output Current I_{VSDIO}
(SDMMC3_1P8_EN = 3.3V)

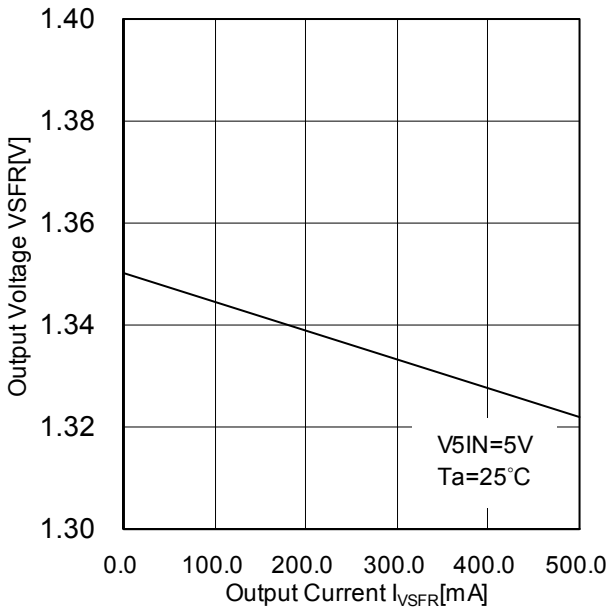


Figure 25. Output Voltage VSFR vs Output Current I_{VSFR}

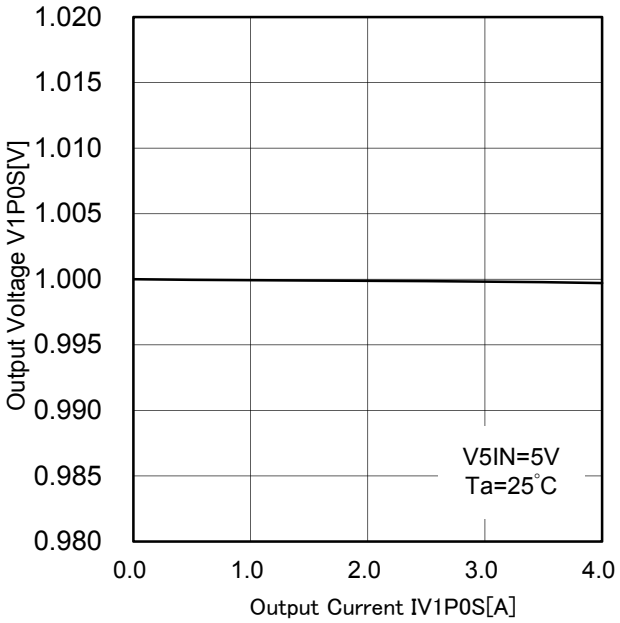


Figure 26. Output Voltage V1P0S vs Output Current I_{V1P0S}

Typical Performance Curves - Continued

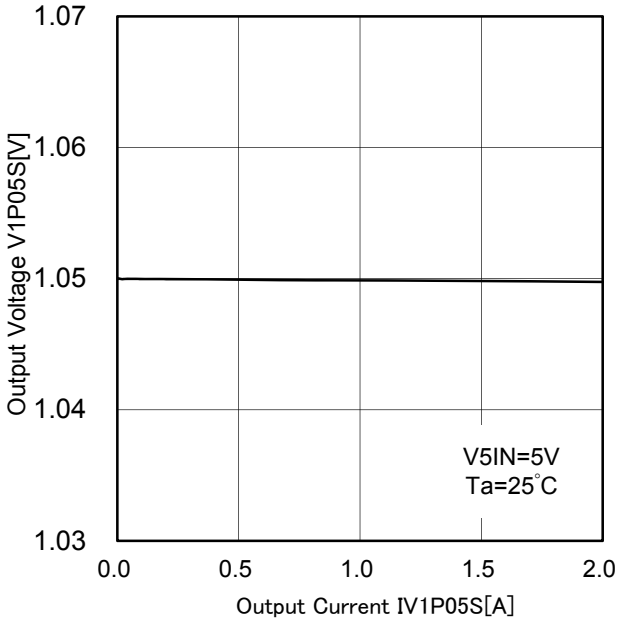


Figure 27. Output Voltage V1P05S vs Output Current I_{V1P05S}

4.2 **Temperature Characteristics**

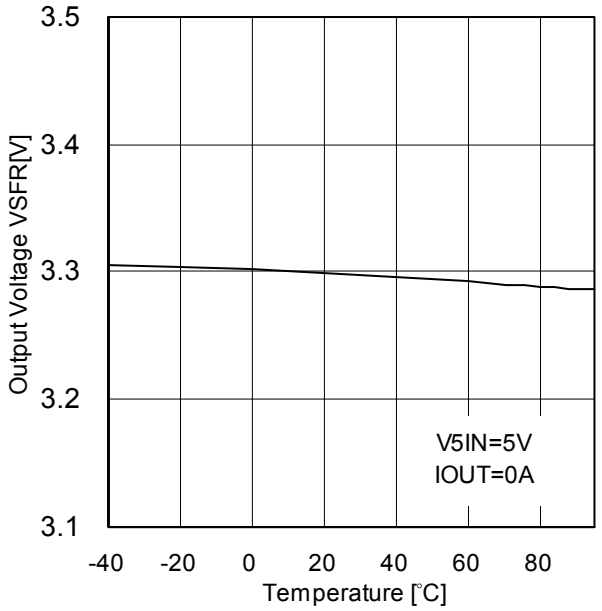


Figure 28. Output Voltage VSFR vs Temperature

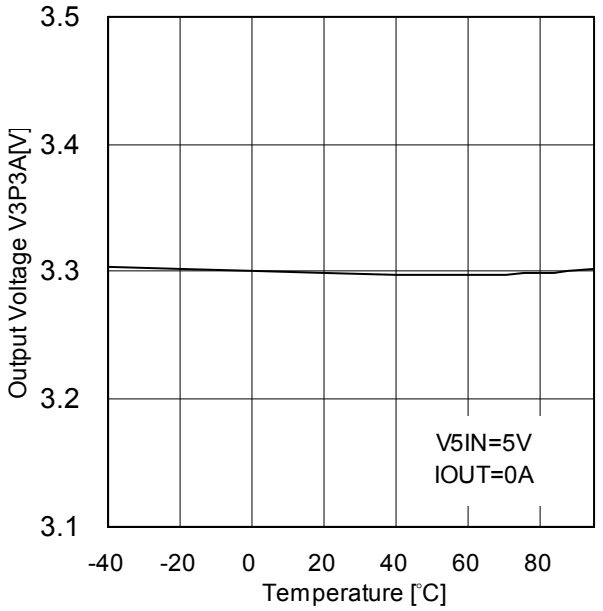


Figure 29. Output Voltage V3P3A vs Temperature

Typical Performance Curves - Continued

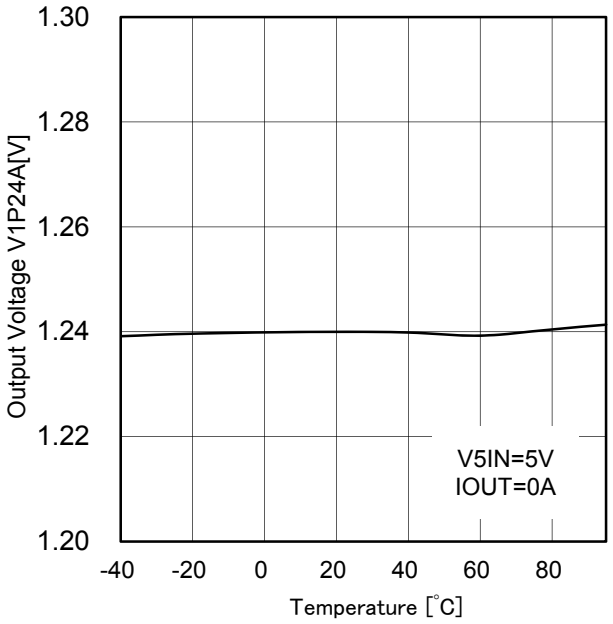


Figure 30. Output Voltage V1P24A vs Temperature

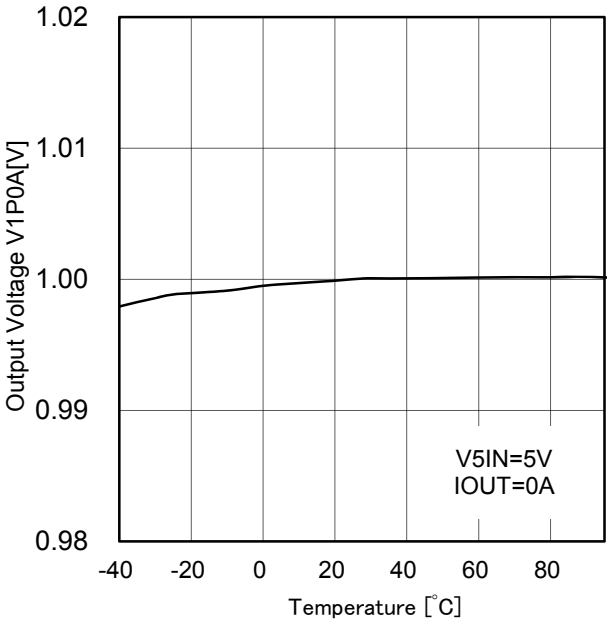


Figure 31. Output Voltage V1P0A vs Temperature

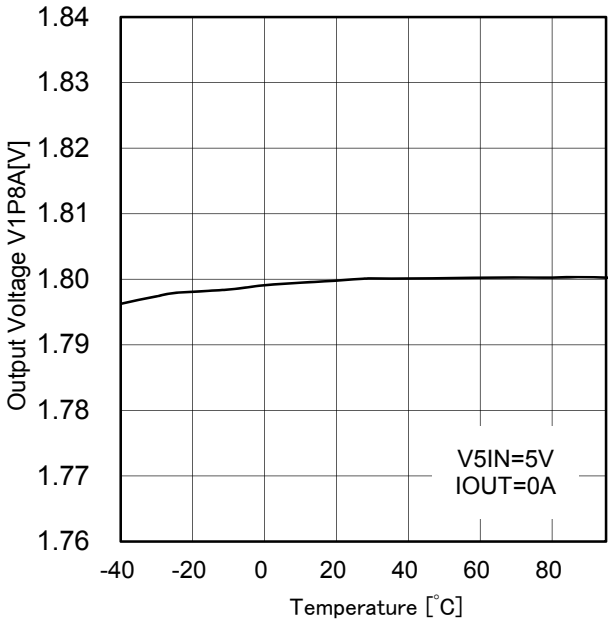


Figure 32. Output Voltage V1P8A vs Temperature

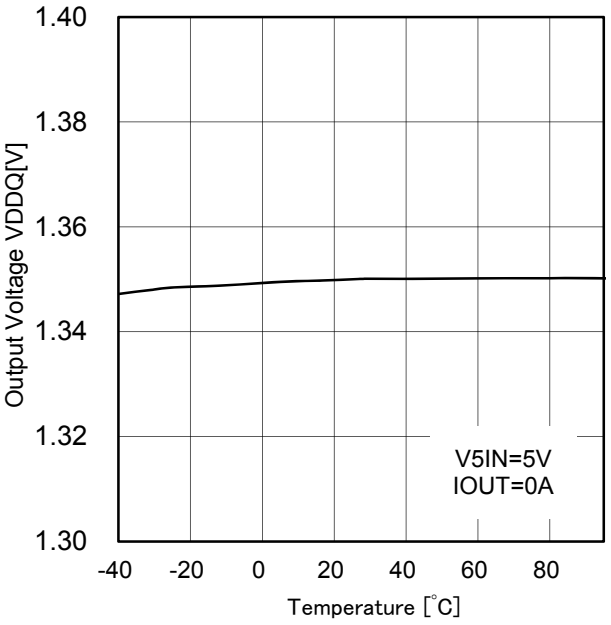


Figure 33. Output Voltage VDDQ vs Temperature

Typical Performance Curves - Continued

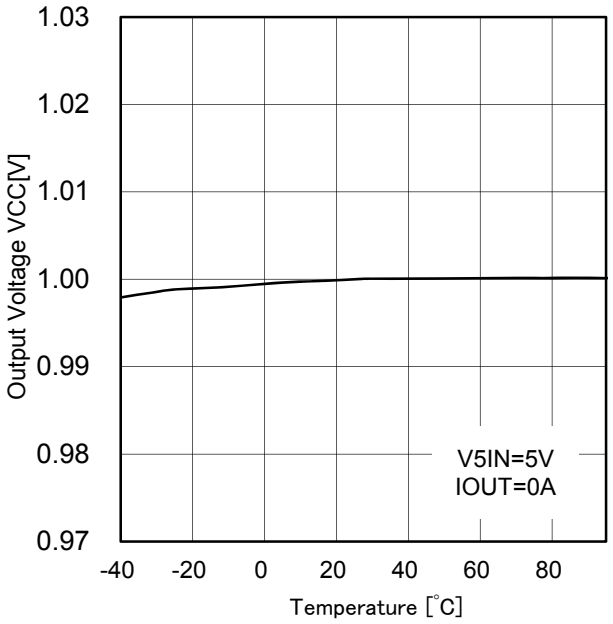


Figure 34. Output Voltage VCC vs Temperature

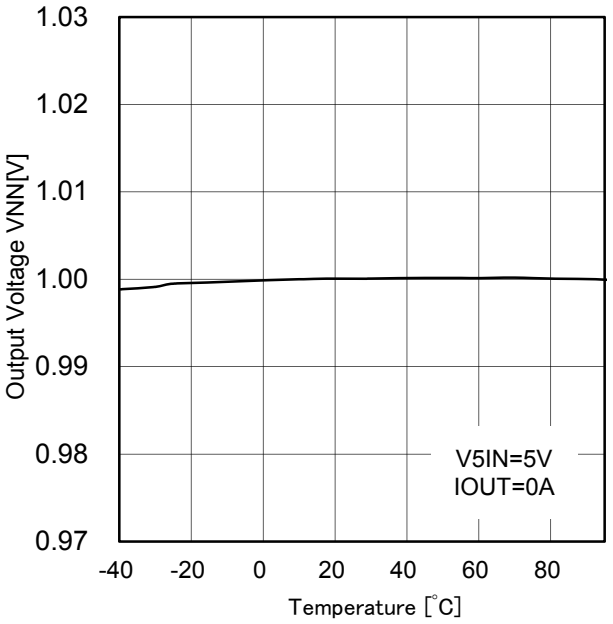


Figure 35. Output Voltage VNN vs Temperature

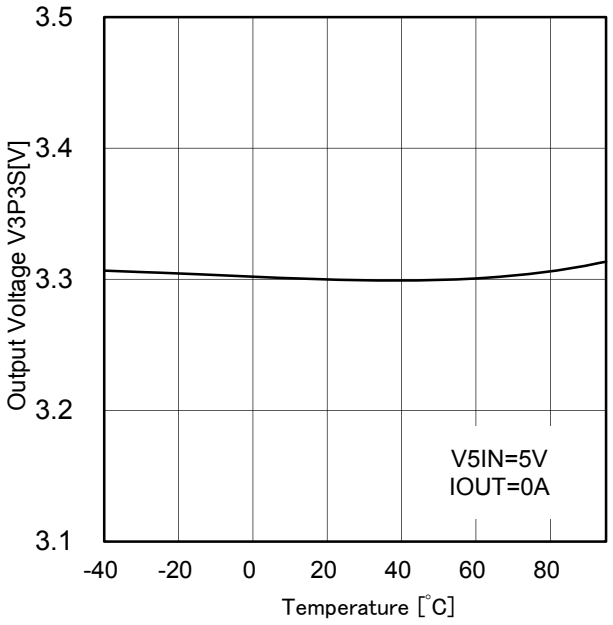


Figure 36. Output Voltage V3P3S vs Temperature

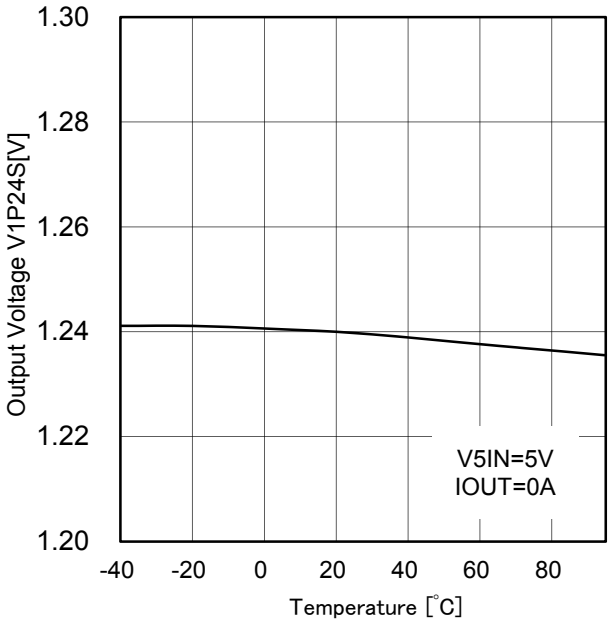


Figure 37. Output Voltage V1P24S vs Temperature

Typical Performance Curves - Continued

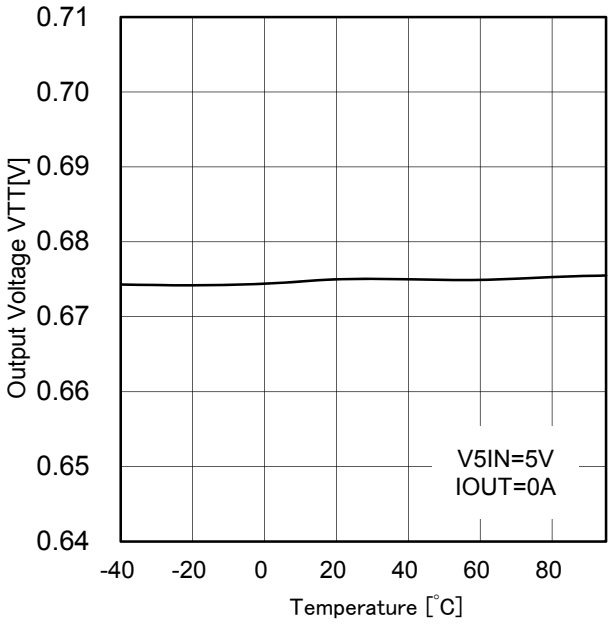


Figure 38. Output Voltage VTT vs Temperature

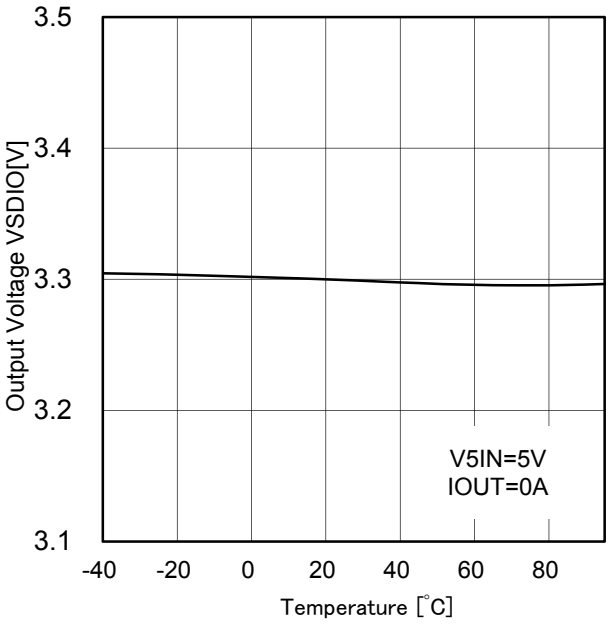


Figure 39. Output Voltage VSDIO vs Temperature
(SDMMC3_1P8_EN = 0V)

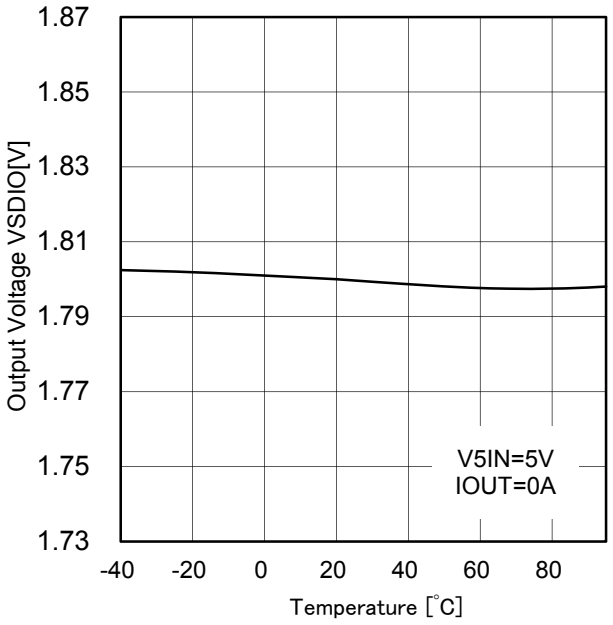


Figure 40. Output Voltage VSDIO vs Temperature
(SDMMC3_1P8_EN = 3.3V)

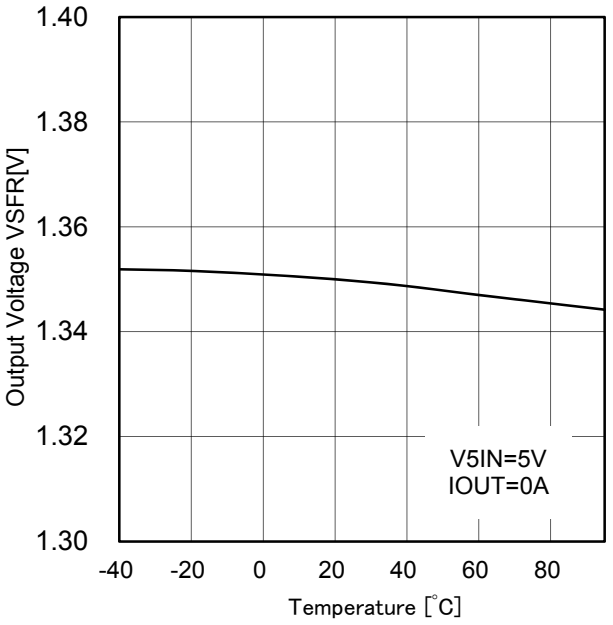


Figure 41. Output Voltage VSFR vs Temperature

Typical Performance Curves - Continued

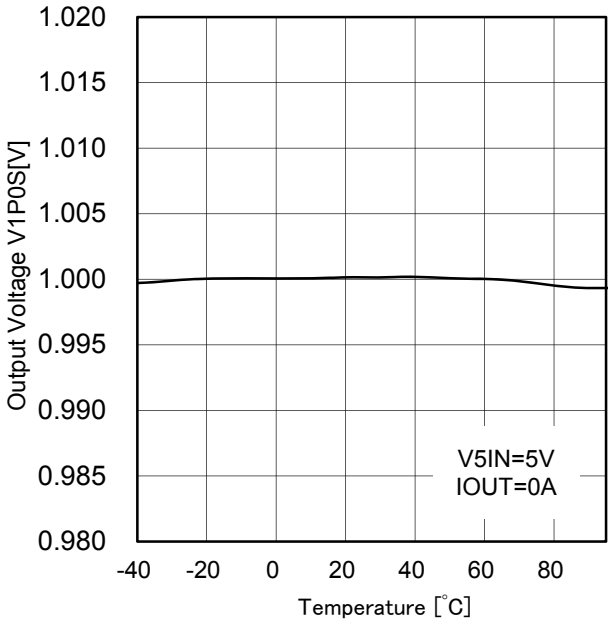


Figure 42. Output Voltage V1P0S vs Temperature

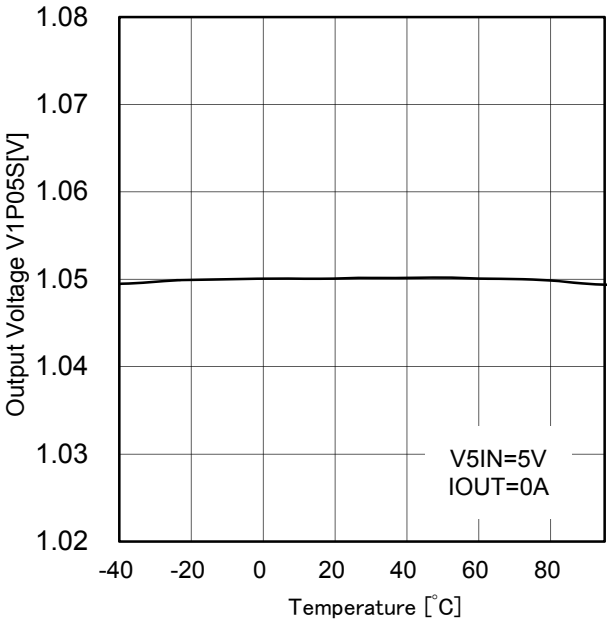


Figure 43. Output Voltage V1P05S vs Temperature

4.3 **Efficiency**

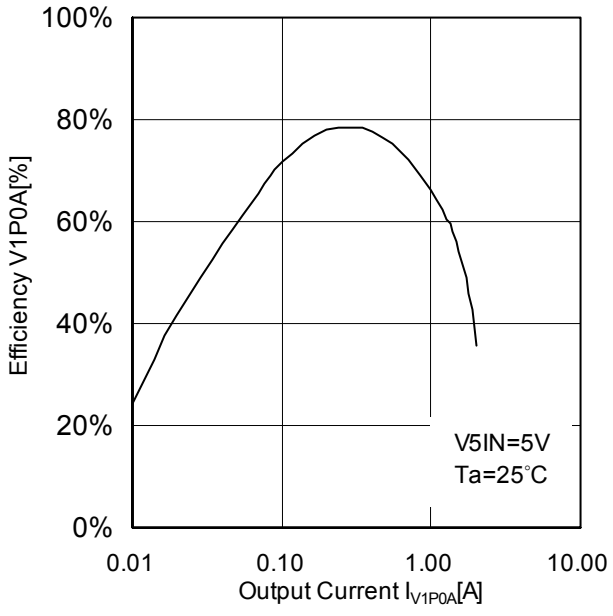


Figure 44. Efficiency V1P0A vs Output Current I_{V1P0A}

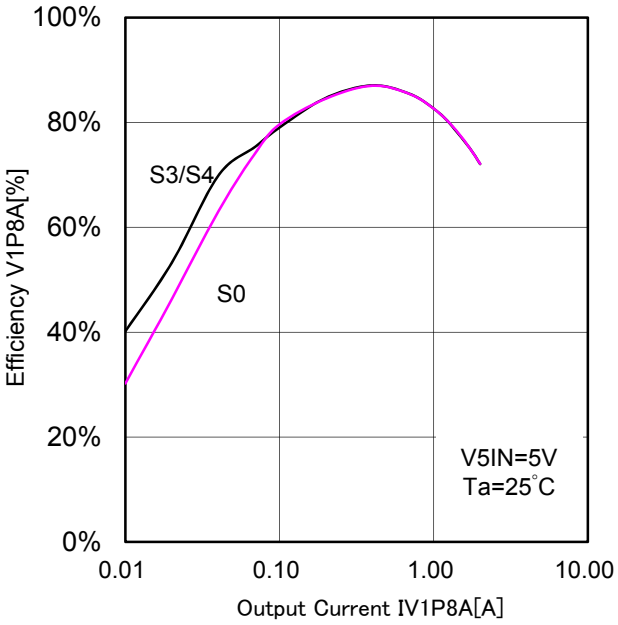


Figure 45. Efficiency V1P8A vs Output Current I_{V1P8A}

Typical Performance Curves - Continued

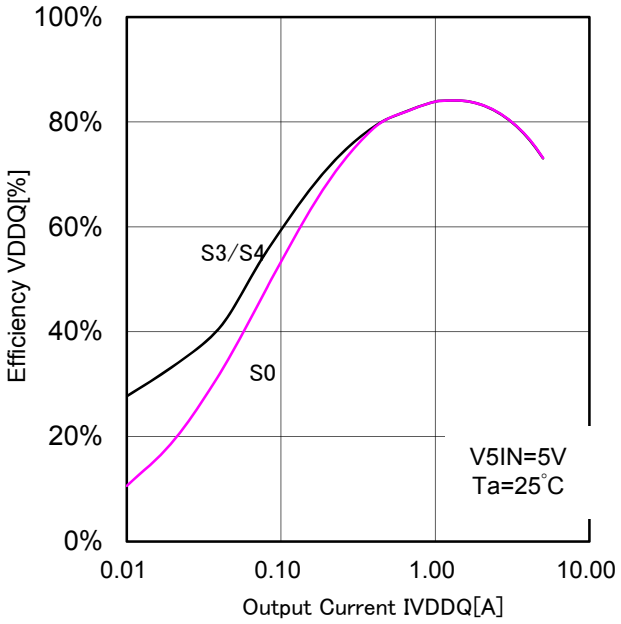


Figure 46. Efficiency VDDQ vs Output Current I_{VDDQ}

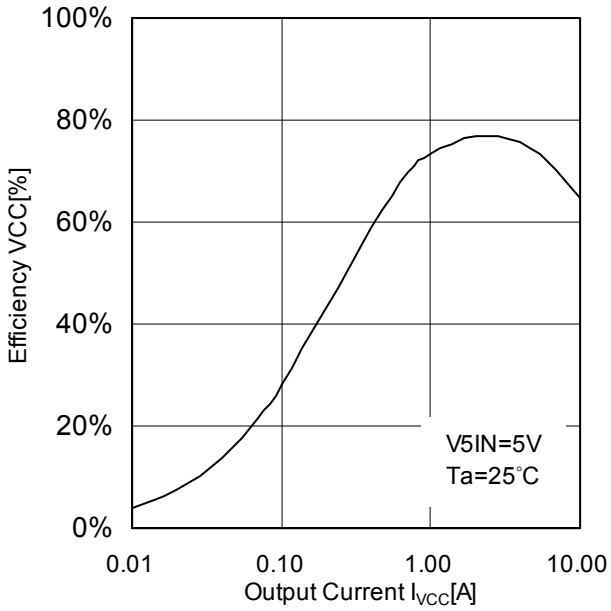


Figure 47. Efficiency VCC vs Output Current I_{VCC}

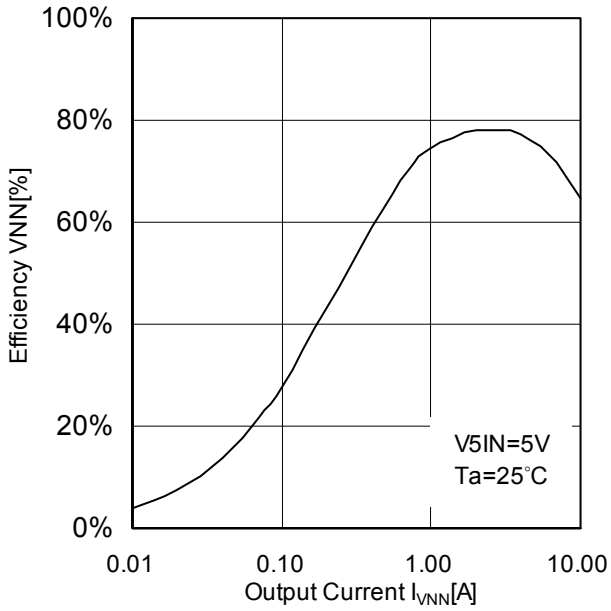


Figure 48. Efficiency VNN vs Output Current I_{VNN}

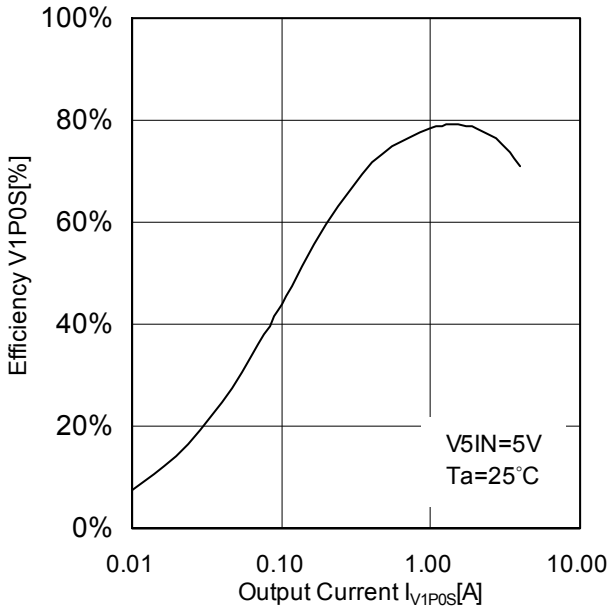


Figure 49. Efficiency V1P0S vs Output Current I_{V1P0S}

Typical Performance Curves - Continued

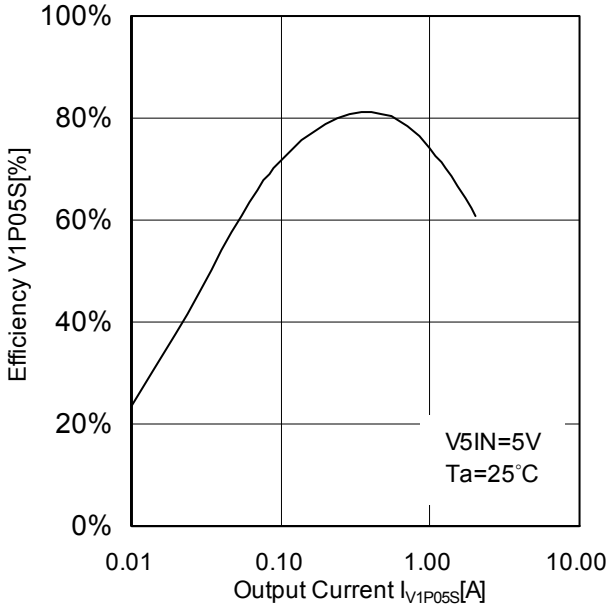


Figure 50. Efficiency V1P05S vs Output Current
I_{V1P05S}

4.4 Transient Response

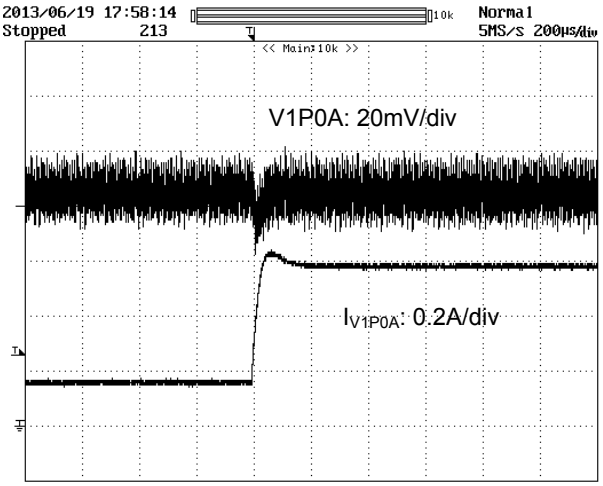


Figure 51. Transient Response V1P0A
(V5INA=5V Ta=25˚C I_{V1P0A} = 160mA to 600mA)

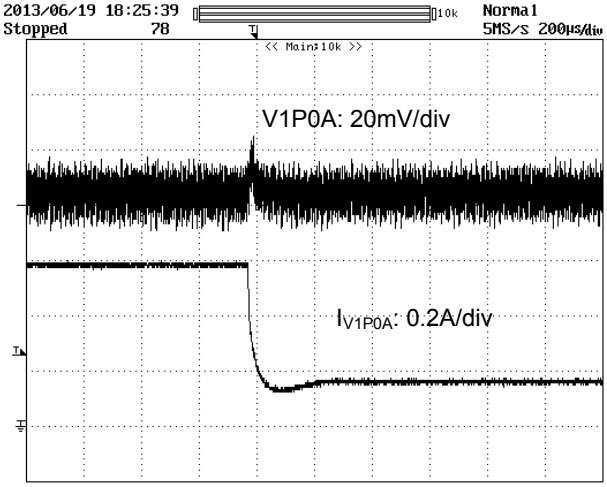


Figure 52. Transient Response V1P0A
(V5INA=5V Ta=25˚C I_{V1P0A} = 600mA to 160mA)

Typical Performance Curves - Continued

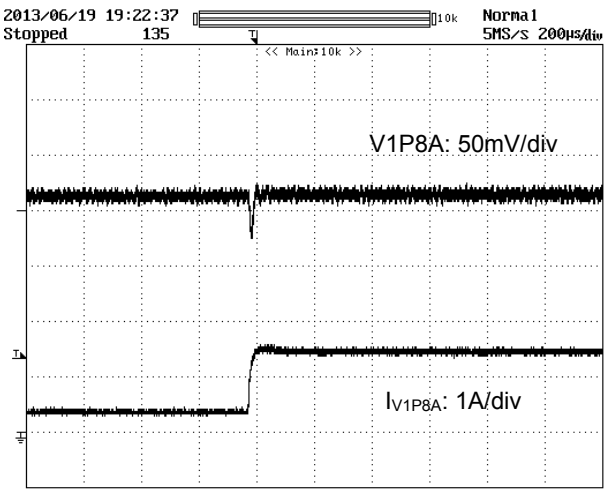


Figure 53. Transient Response V1P8A
(V5INA=5V Ta=25˚C I_{V1P8A} = 360mA to 1440mA)

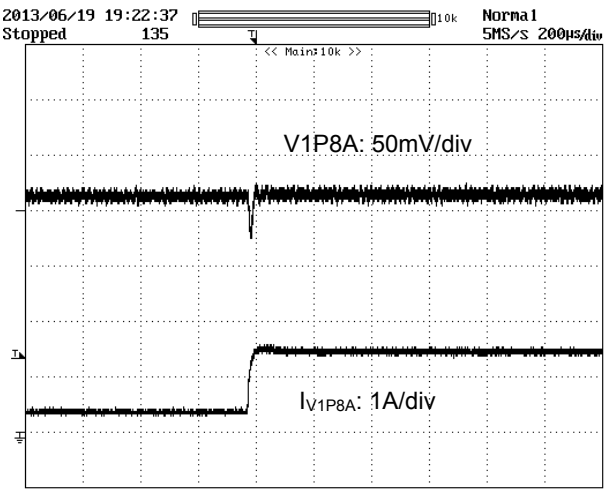


Figure 54. Transient Response V1P8A
(V5INA=5V Ta=25˚C I_{V1P8A} = 1440mA to 360mA)

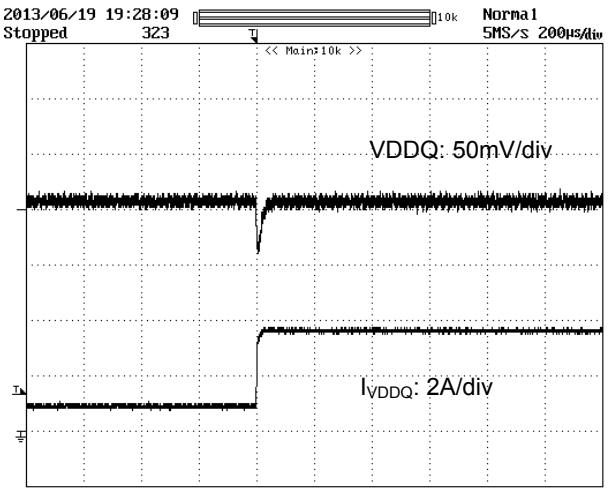


Figure 55. Transient Response VDDQ
(V5INA=5V Ta=25˚C I_{VDDQ} = 800mA to 3800mA)

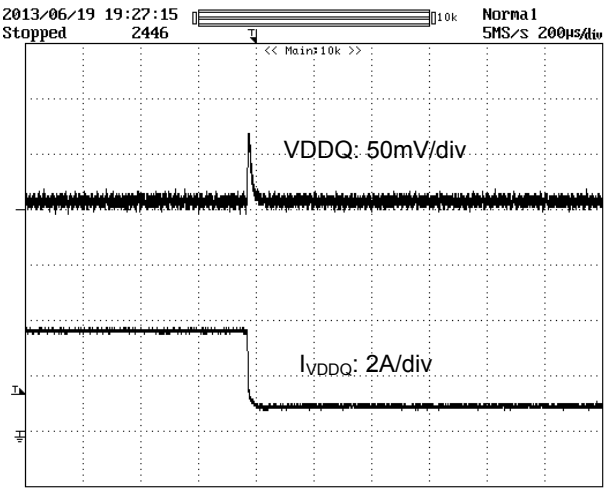


Figure 56. Transient Response VDDQ
(V5INA=5V Ta=25˚C I_{VDDQ} = 3800mA to 800mA)

Typical Performance Curves - Continued

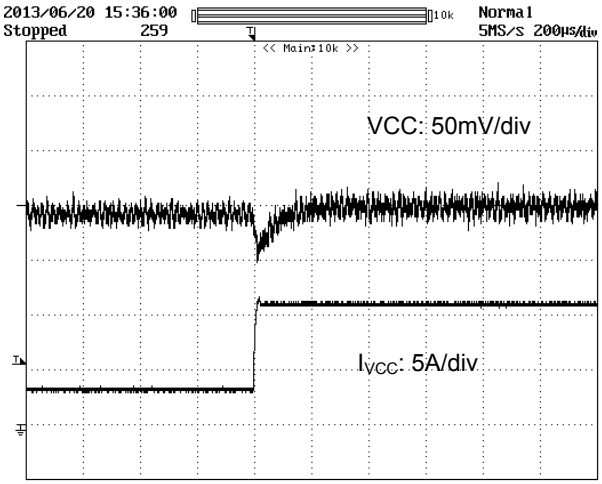


Figure 57. Transient Response VCC
(V5INA=5V Ta=25˚C I_{VCC} = 2.7A to 11A)

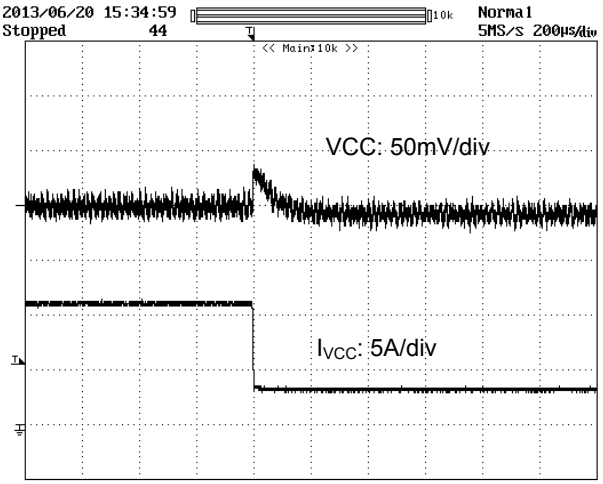


Figure 58. Transient Response VCC
(V5INA=5V Ta=25˚C I_{VCC} = 11A to 2.7A)

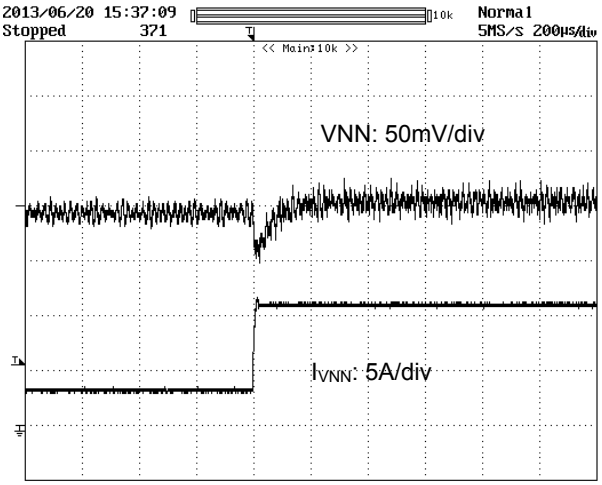


Figure 59. Transient Response VNN
(V5INA=5V Ta=25˚C I_{VNN} = 2.7A to 11A)

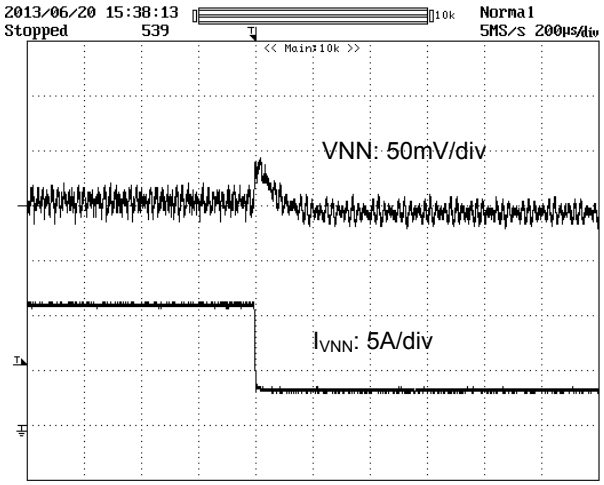


Figure 60. Transient Response VNN
(V5INA=5V Ta=25˚C I_{VNN} = 11A to 2.7A)

Typical Performance Curves - Continued

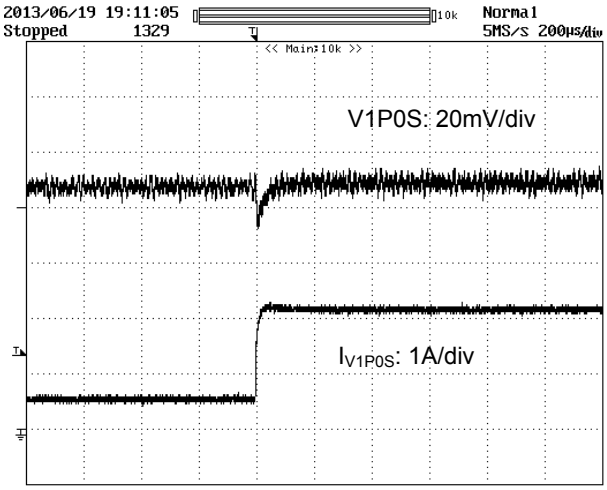


Figure 61. Transient Response V1P0S
(V5INA=5V Ta=25˚C I_{V1P0S} = 533mA to 2135mA)

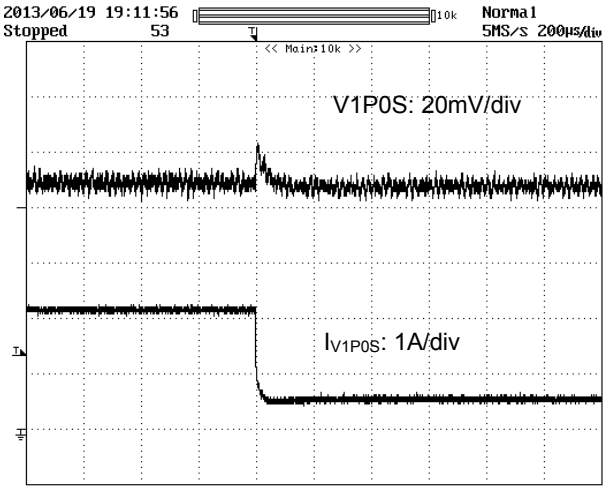


Figure 62. Transient Response V1P0S
(V5INA=5V Ta=25˚C I_{V1P0S} = 2135mA to 533mA)

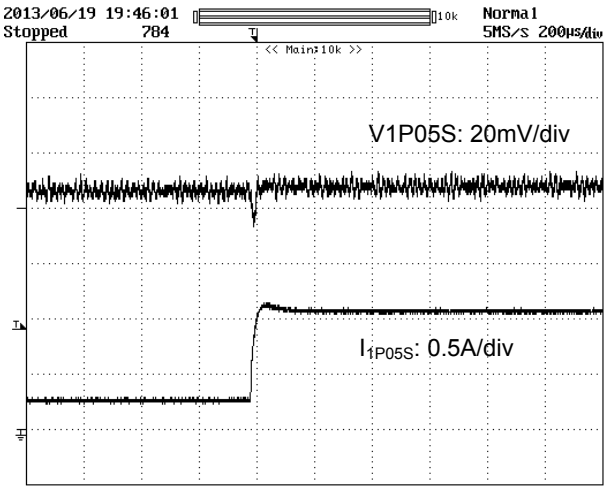


Figure 63. Transient Response V1P05S
(V5INA=5V Ta=25˚C I_{V1P05S} = 264mA to 1058mA)

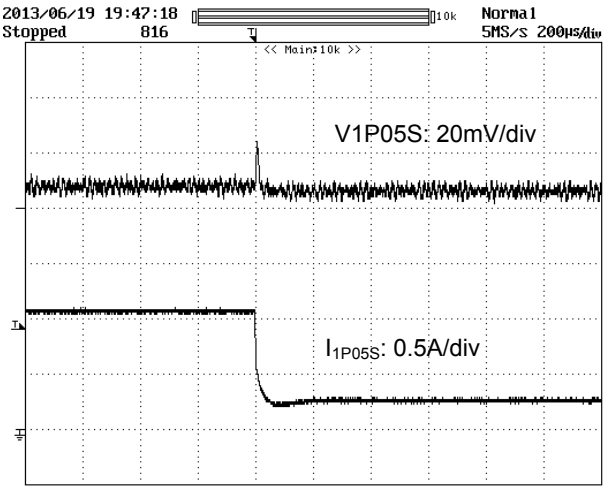
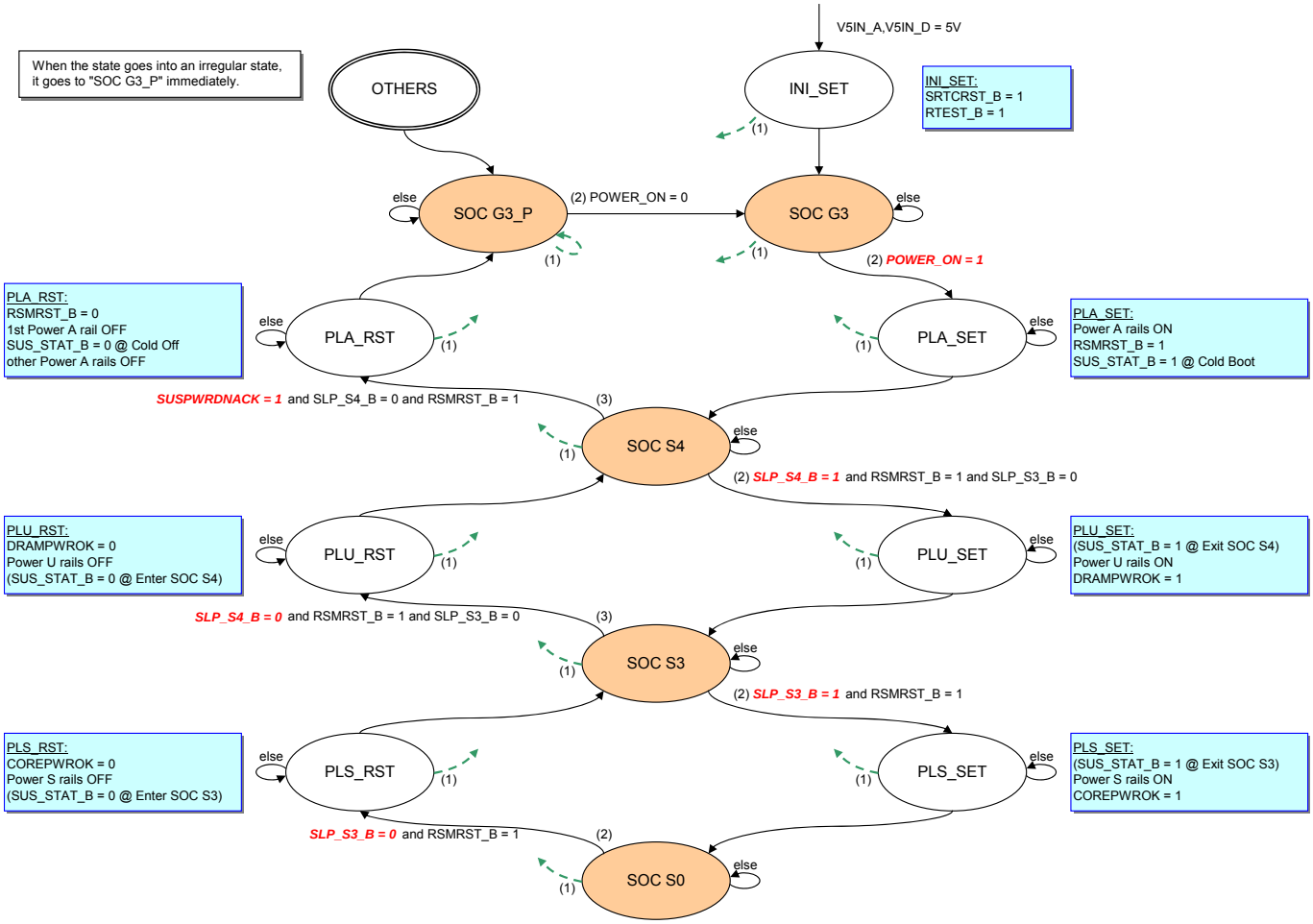


Figure 64. Transient Response V1P05S
(V5INA=5V Ta=25˚C I_{V1P05S} = 1058mA to 264mA)

5. Sequence

5.1 State Machine



- The arrows (1) in the figure show SCP, OVP or TSD.
  When SCP, OVP or TSD is detected in any state, the state goes to "SOC G3_P" immediately.

- (1), (2) and (3) in the figure show priority when events occur simultaneously.

Figure 65. State Machine

5.2 Cold Boot Timing Chart

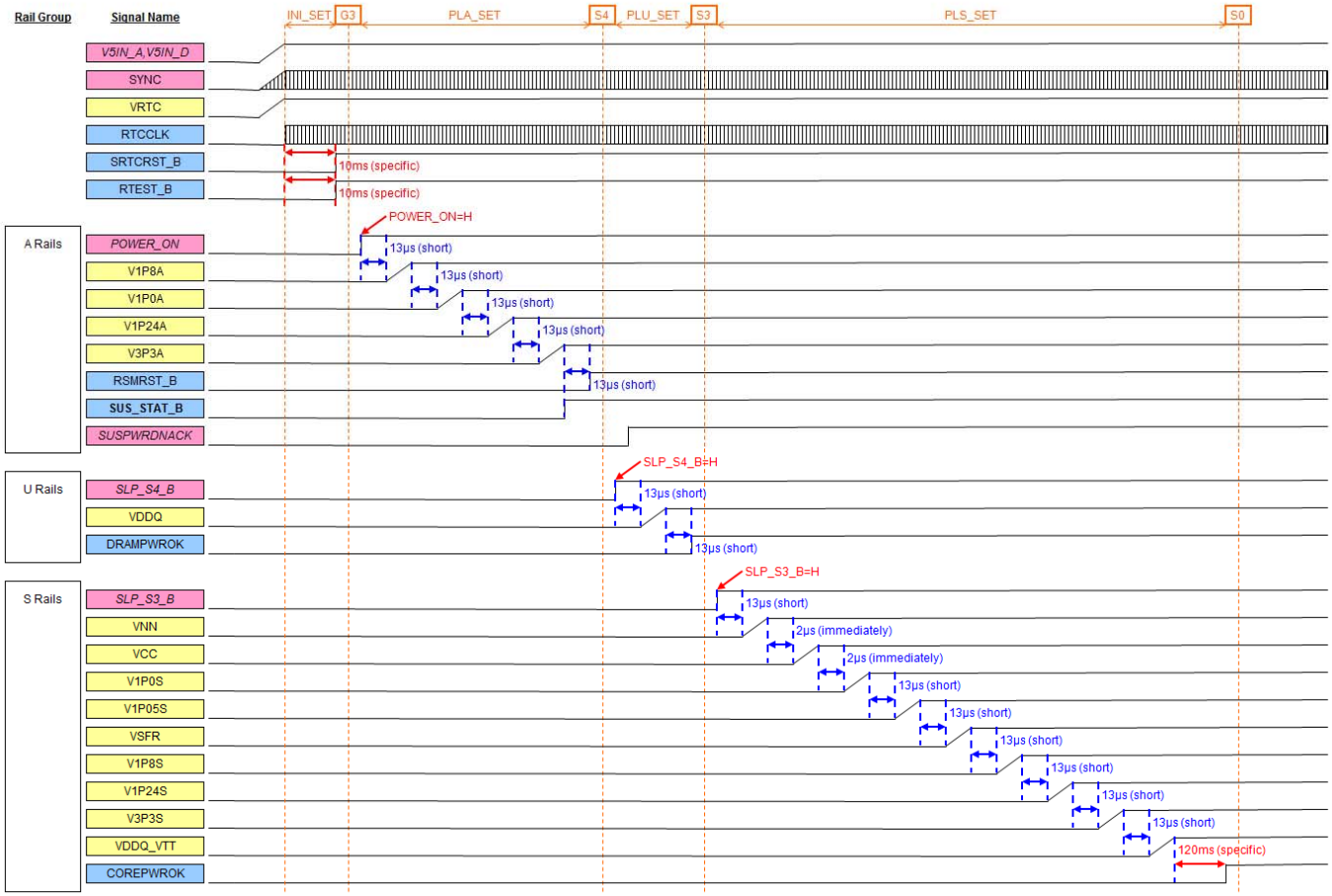


Figure 66. Cold Boot Timing Chart

(*) SRTCRST_B and RTEST_B remain High once they become High at INI_SET state, even when SCP, OVP, or TSD is detected.

5.3 Cold Off Timing Chart

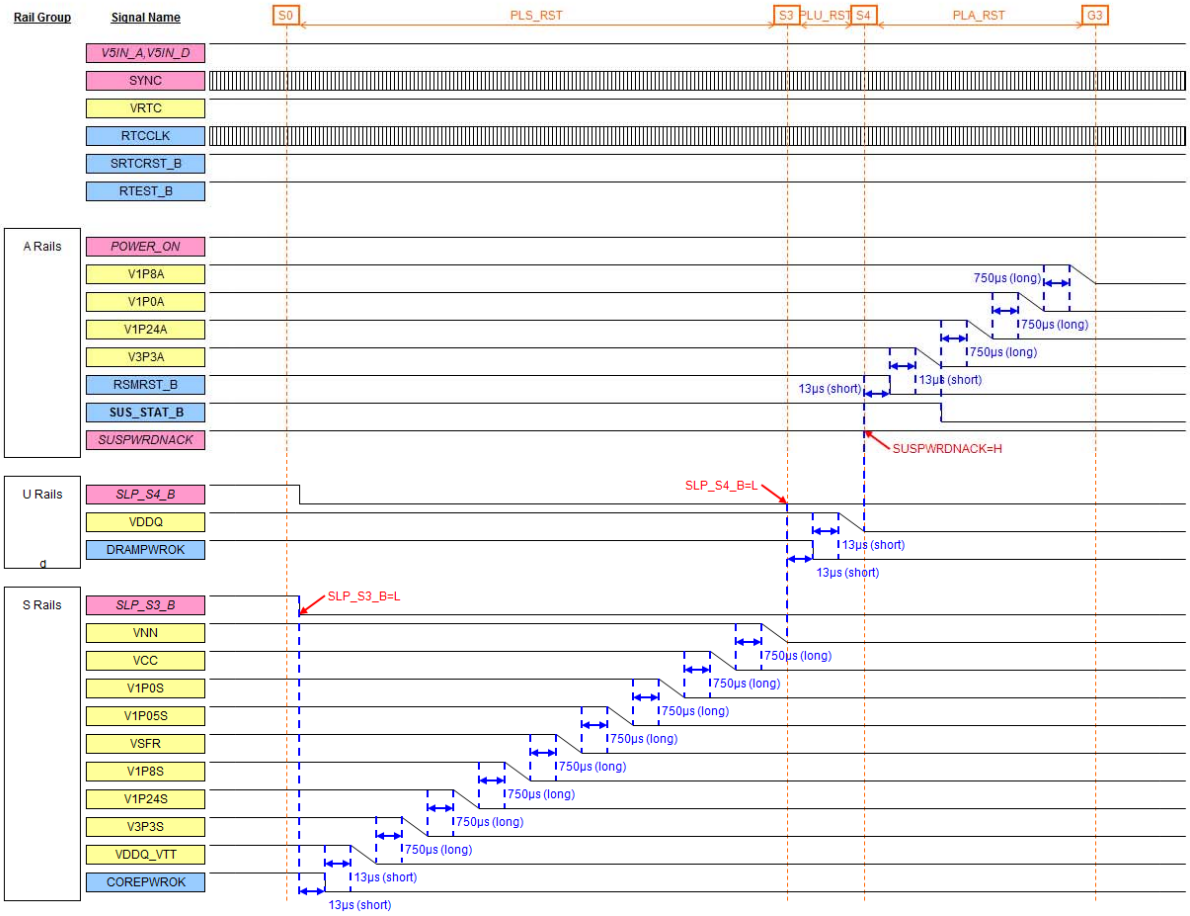


Figure 67. Cold Off Timing Chart

5.4 Enter SOC S4 Timing Chart

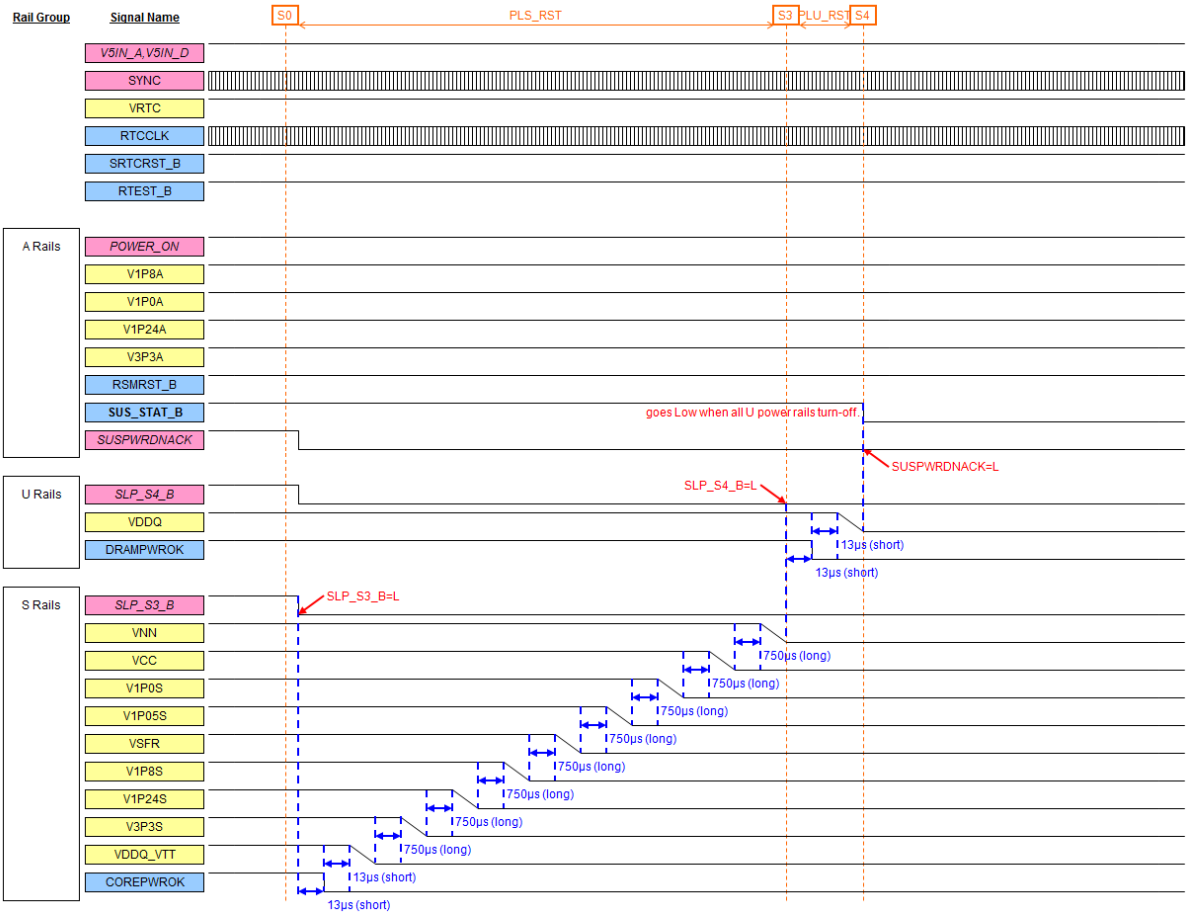


Figure 68. Enter SOC S4 Timing Chart

5.5 Exit SOC S4 Timing Chart

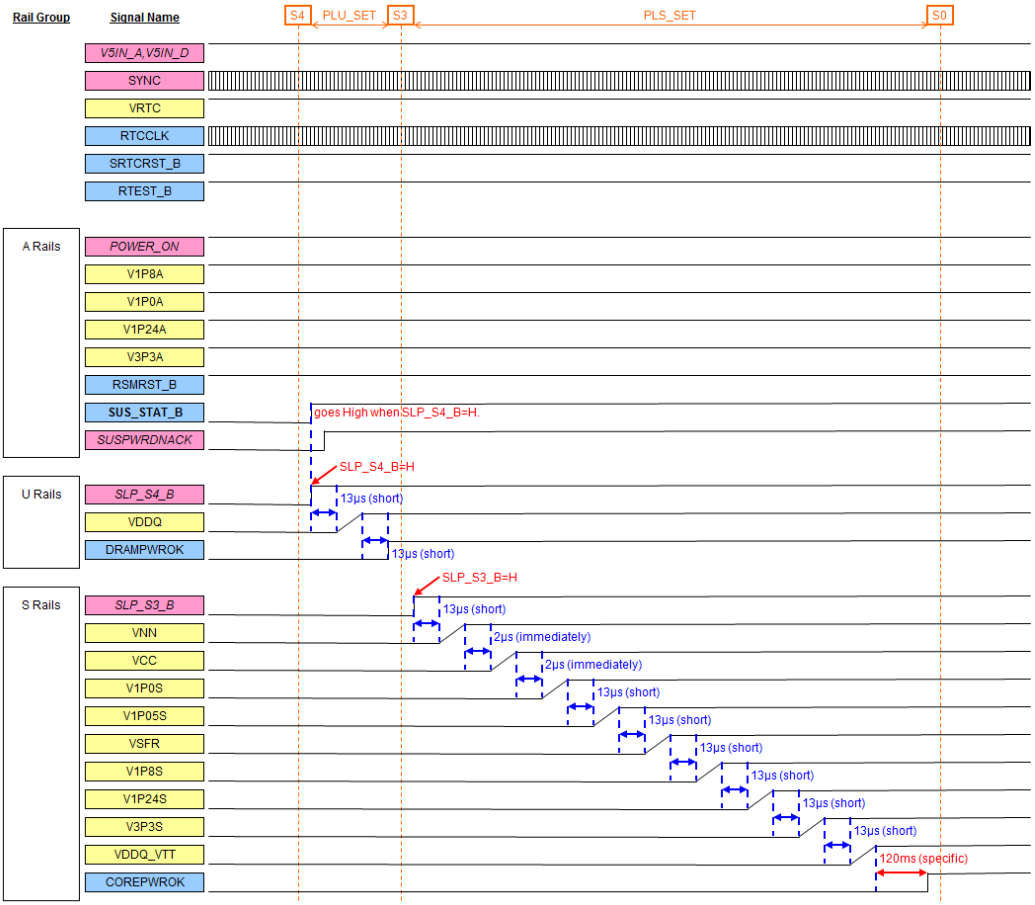


Figure 69. Exit SOC S4 Timing Chart

5.6 Enter SOC S3 Timing Chart

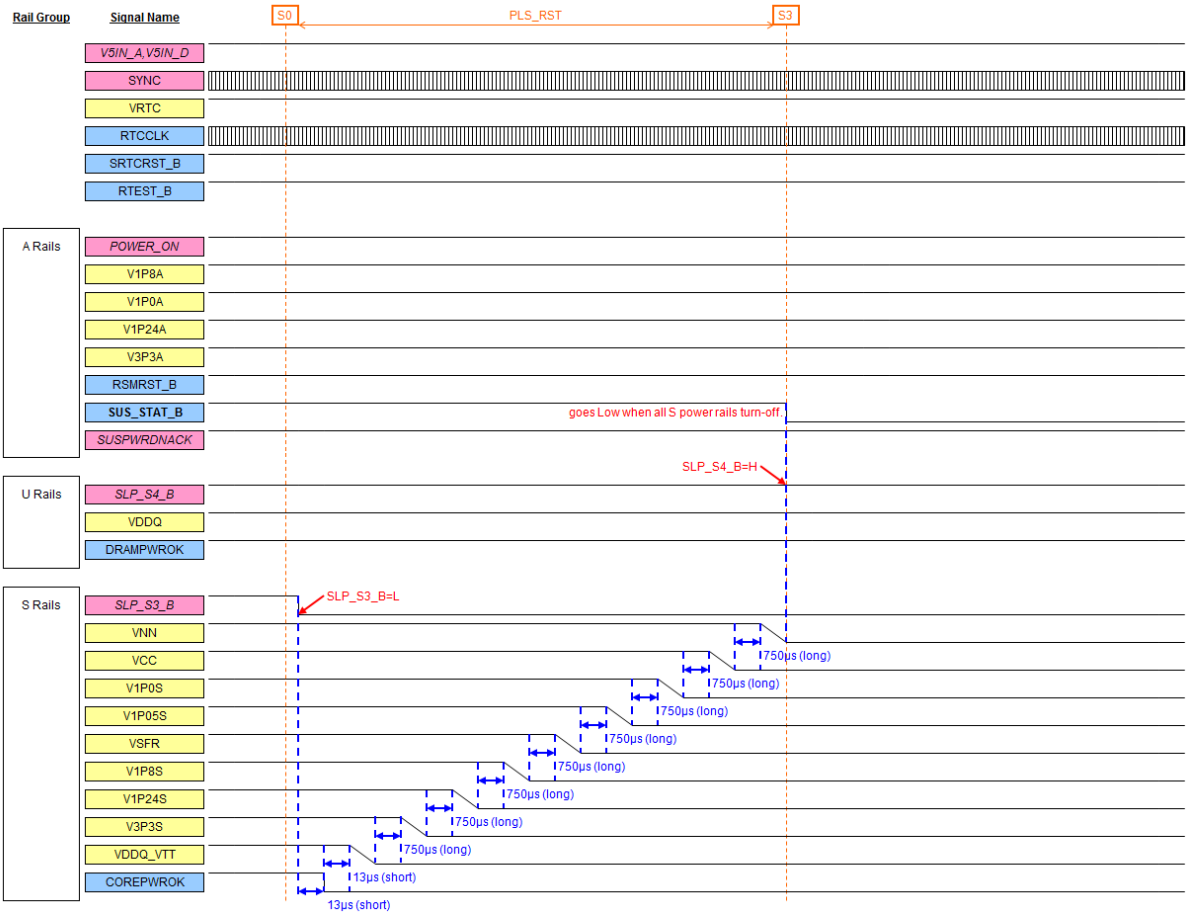


Figure 70. Enter SOC S3 Timing Chart

5.7 Exit SOC S3 Timing Chart

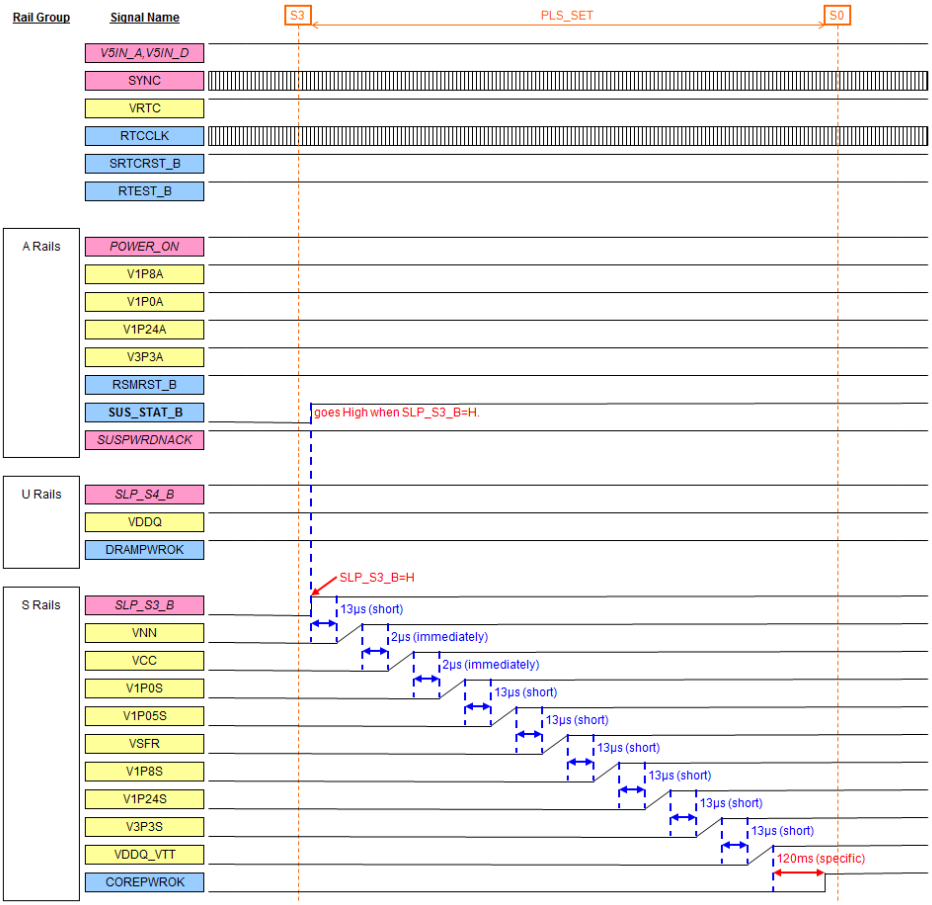


Figure 71. Exit SOC S3 Timing Chart

5.8 I/O Interface Signals

Table 17: I/O Interface Signals Table

Pin Name	Connect to	Description	I/O	Valid while
SLP_S3_B	SOC	Sleep S3 trigger 0=enter S3; 1=exit S3	I	RSMRST_B=1
SLP_S4_B	SOC	Sleep S4 trigger 0=enter S4; 1=exit S4	I	RSMRST_B=1 SLP_S3_B=0
SUSPWRDNACK	SOC	tells the PMIC to turn off the SUS rails in junction with assertion of SLP_S4_B	I	RSMRST_B=1 SLP_S4_B=0
SRTCRST_B	SOC	de-asserted when VRTC is stable, allows to detect when VRTC has been switched off	O	VRTC ON
RSMRST_B	SOC	Resume reset, de-asserted after all SUS rails turned on	O (OD)	-
DRAMPWROK	SOC	asserted after VDDQ turned on	O (OD)	-
COREPWROK	SOC	asserted after all core rails turned on	O (OD)	-
RTEST_B	SOC	Test and debug, de-asserted when VRTC is stable	O (OD)	-
PWRBTN_B	SOC	level shifted copy of POWER_ON	O (OD)	RSMRST_B=1
POWER_ON	Platform	tells the PMIC to switch on the SUS rails	I	-
SUS_STAT_B	Platform	Suspend status, informs platform that the desired suspend state has been reached	O	-
SYNC	Platform	DCDC synchronization clock	I	-
SDMMC3_1P8EN	SOC	select 1.8V or 3.3V for SD card 0=3.3V; 1=1.8V	I	RSMRST_B=1 COREPWROK=1
SDMMC3_PWREN_B	SOC	SD card power (VSDIO) enable 0=ON; 1=OFF	I	RSMRST_B=1 COREPWROK=1
RTCCLK	SOC	32kHz clock output	O	-
ERROR	-	asserted when the PMIC state machine has reached an error state, over current or over temperature condition occurred	O	-
SVID_CLK	SOC	SVID clock	I	State='S0'
SVID_DATA	SOC	SVID data	I/O (OD)	State='S0'
SVID_ALERT_B	SOC	SVID alert	O (OD)	-

OD=Open-drain

PWRBTN_B

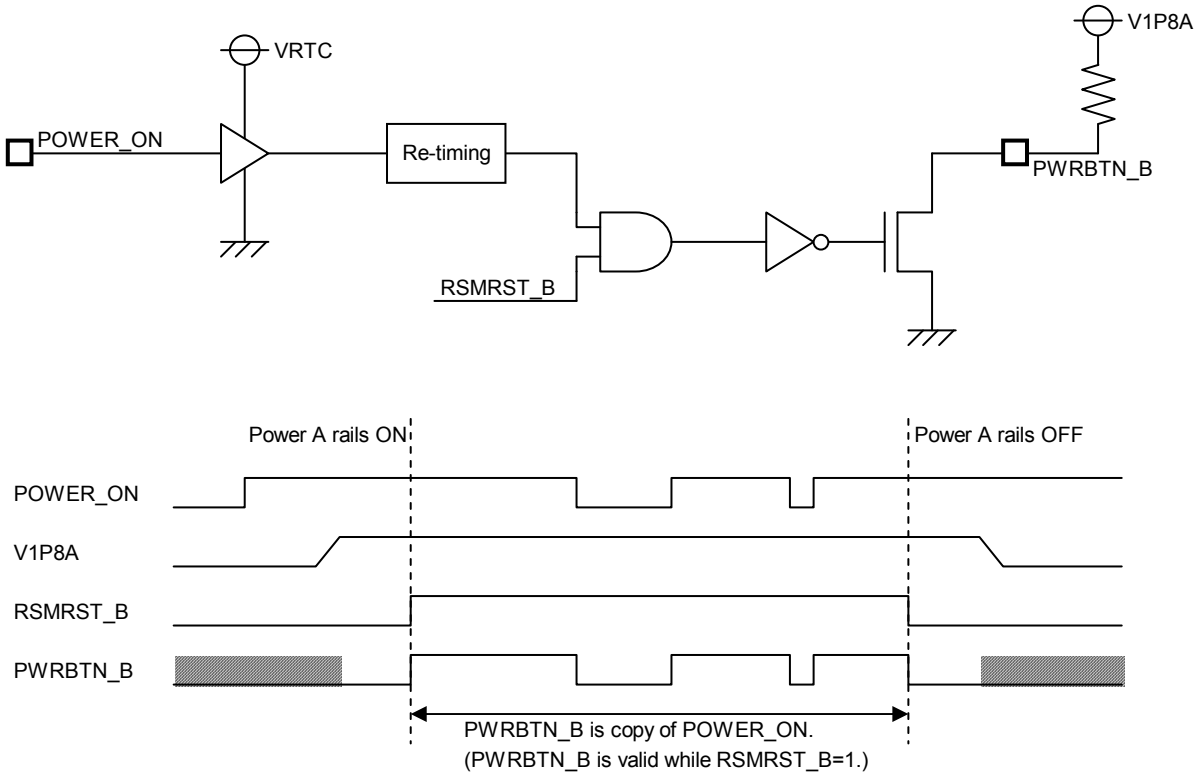


Figure 72. PWRBTN_B Timing Chart

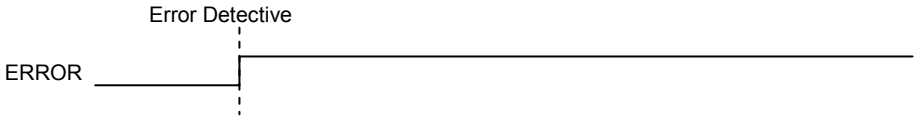
ERROR

Error Detective		Type	Error Output
C1:	Error state	Latch	High
C2:	SCP, OVP	1ms Timer Latch (SCP) 10µs Timer Latch (OVP)	Oscillating (0.5sec period)
C3:	TSD	10µs Timer Latch	Oscillating (12.5sec period)

* Latch is reset by POR(Power-on-reset) or POWER_ON=0.
* In any case, the PMIC state machine goes to "SOC G3_P".

[ERROR Output]

C1 (Error state)



C2 (SCP,OVP), C3 (TSD)

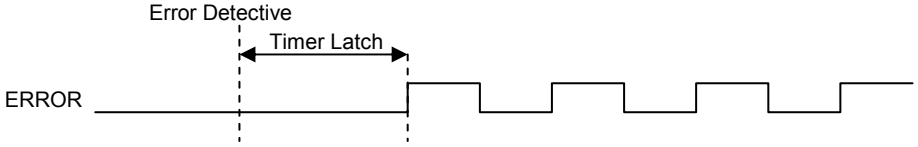
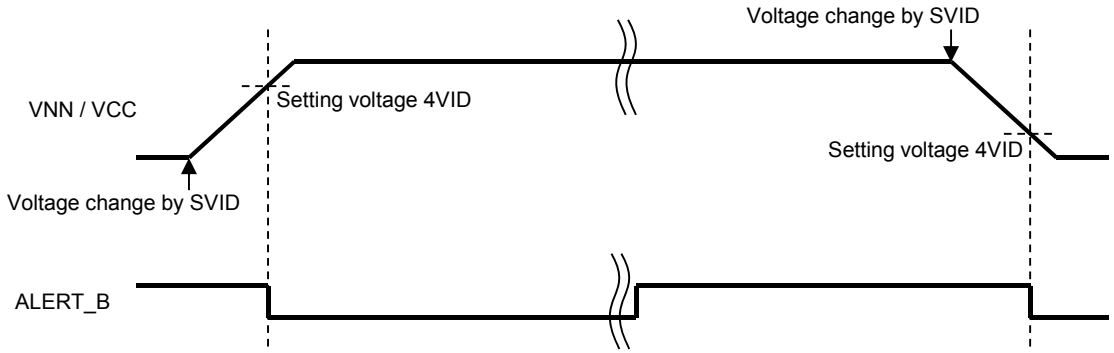


Figure 73. ERROR Timing Chart

ALERT_B

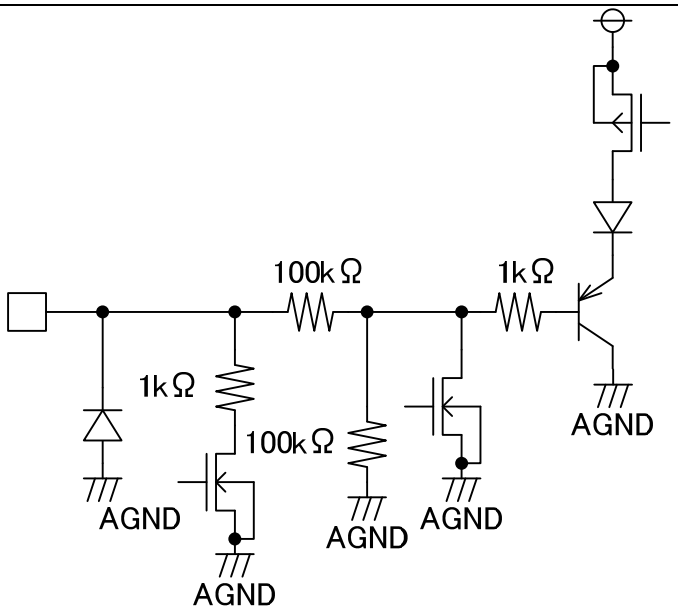
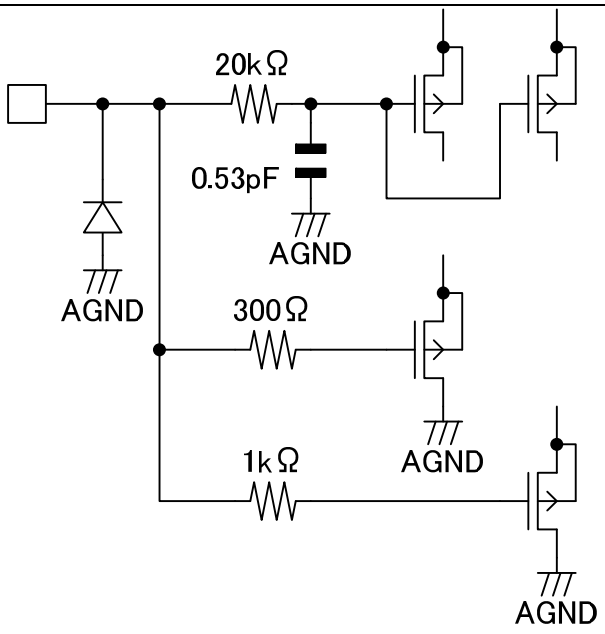
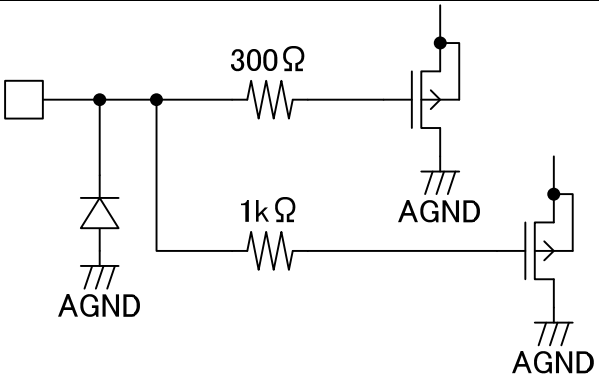


ALERT_B is asserted if VCC/VNN output voltage is within ±4VID of setting voltage.

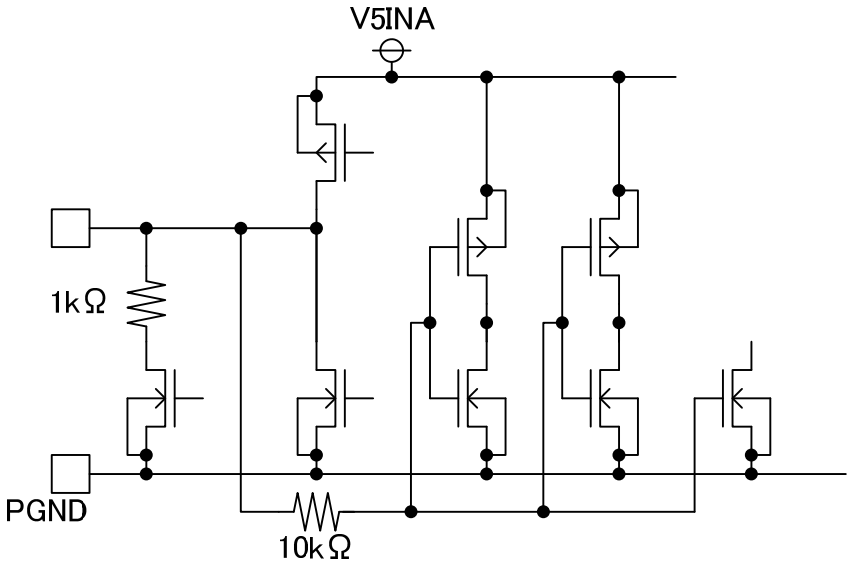
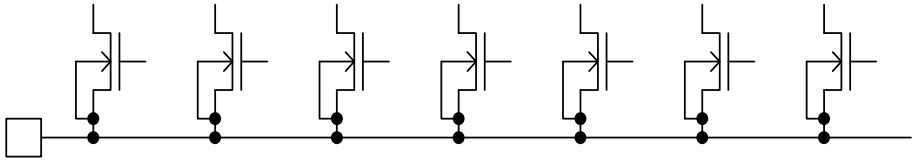
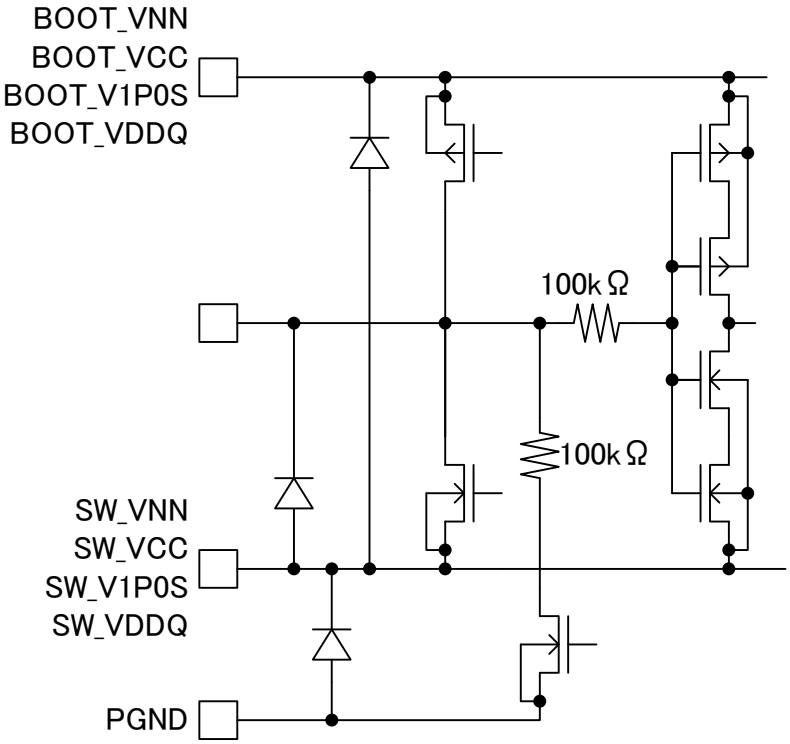
Figure 74. ALERT_B Timing Chart

6. I/O Equivalent Circuit

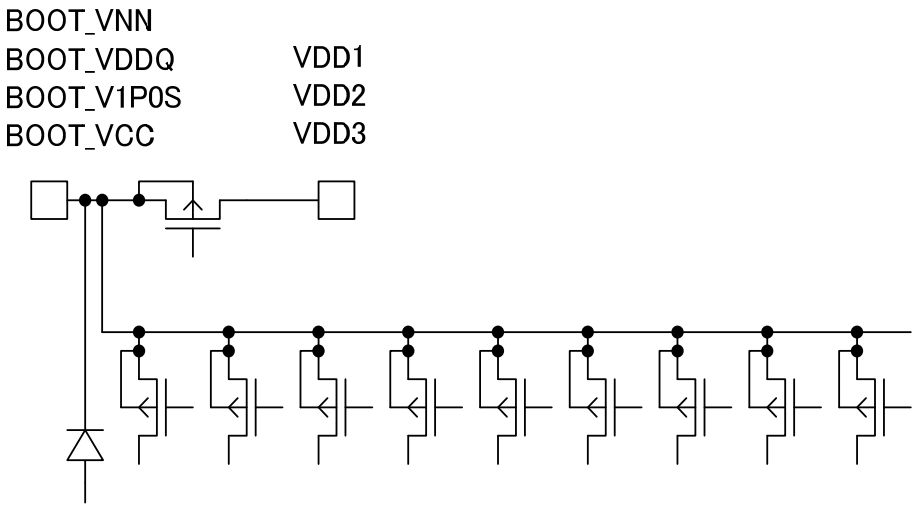
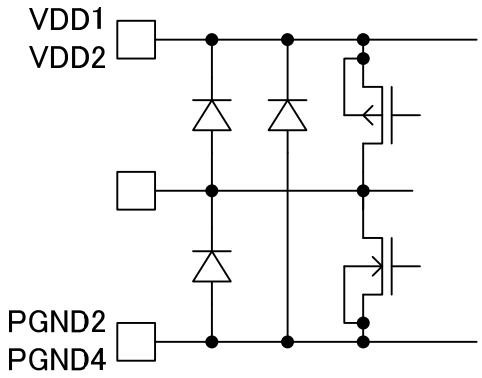
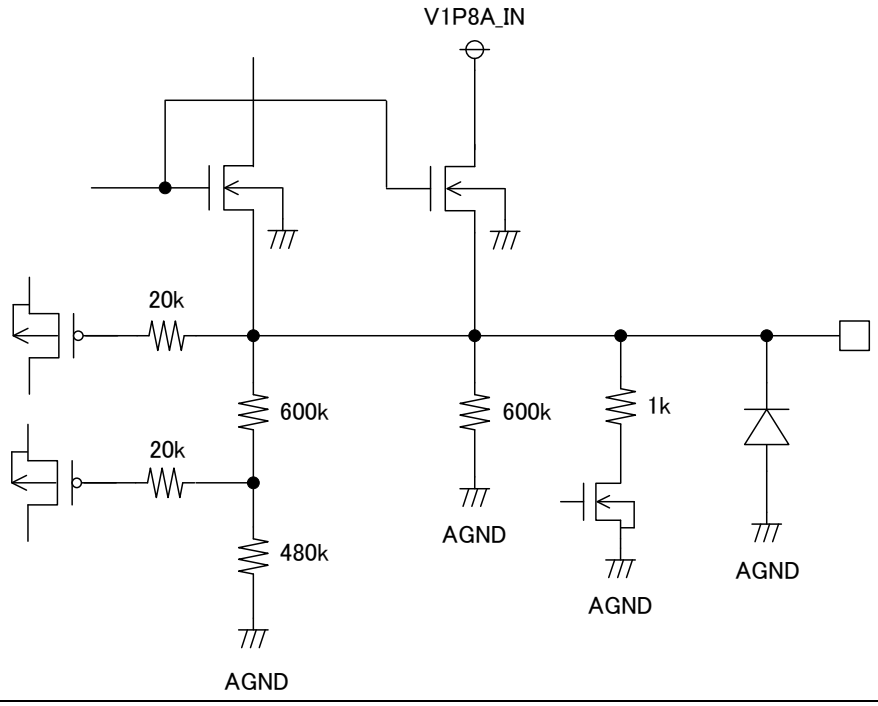
Table 18: Pin Equivalent Circuit

REMOTE_P_VNN (PIN1) REMOTE_P_VCC(PIN86)	
IS_M_VNN (PIN2) IS_M_VCC (PIN85)	
IS_P_VNN (PIN3) IS_P_VCC (PIN84)	

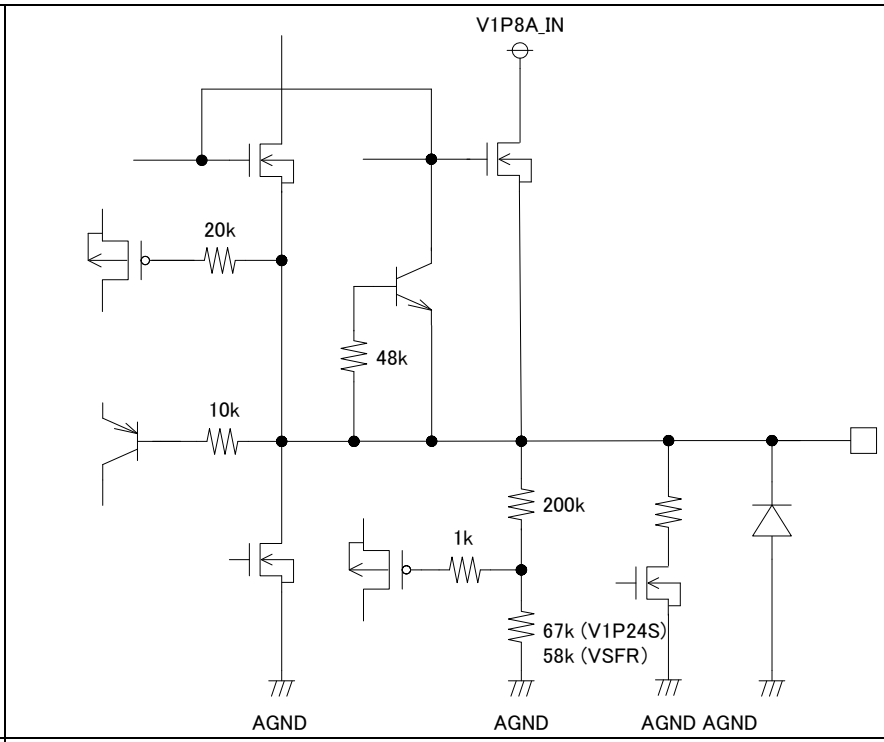
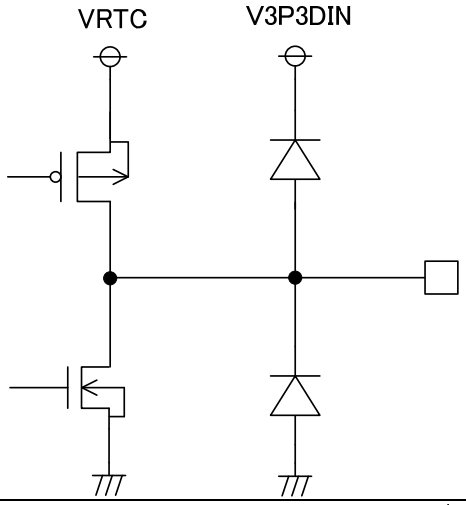
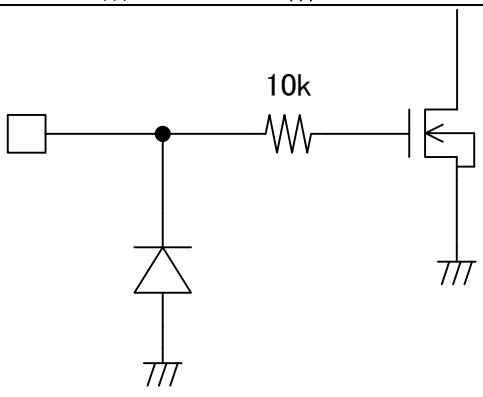
I/O Equivalent Circuit – continued

LG_VNN (PIN5) LG_VDDQ (PIN60) LG_V1P0S (PIN70) LG_VCC (PIN82)	
SW_VNN (PIN6) SW_VCC (PIN81)	
HG_VNN (PIN7) HG_VDDQ (PIN62) HG_V1P0S (PIN68) HG_VCC (PIN80)	

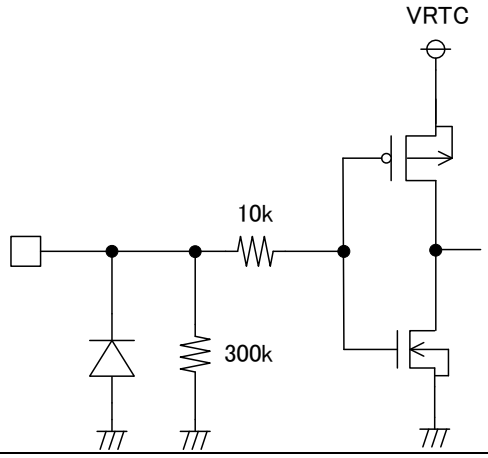
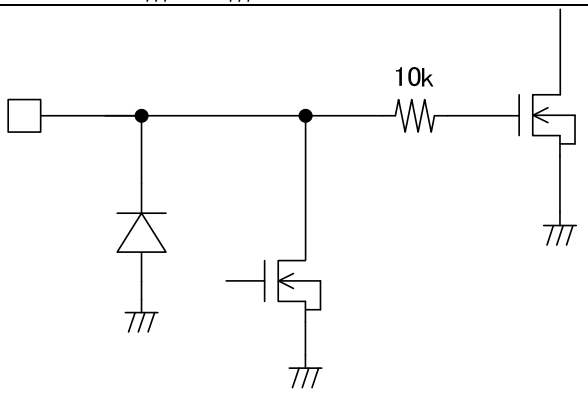
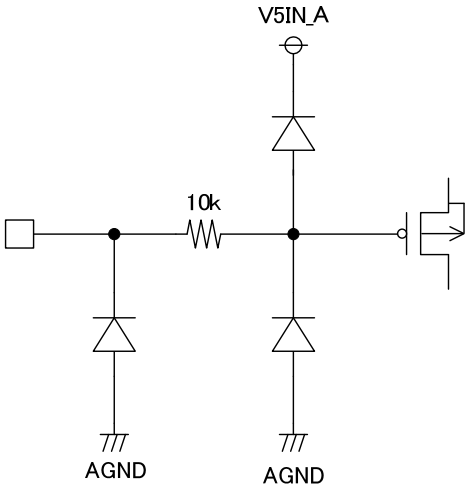
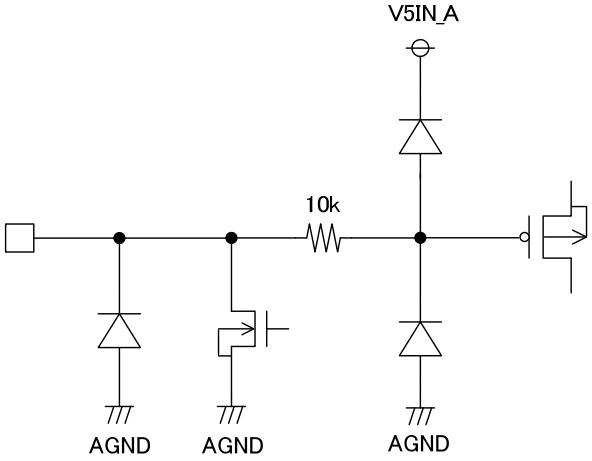
I/O Equivalent Circuit – continued

BOOT_VNN (PIN8) BOOT_VDDQ (PIN63) BOOT_V1P0S (PIN67) BOOT_VCC (PIN79)	
SW_V1P8A (PIN10) SW_V1P0A (PIN58)	
V1P8S (PIN13,14)	

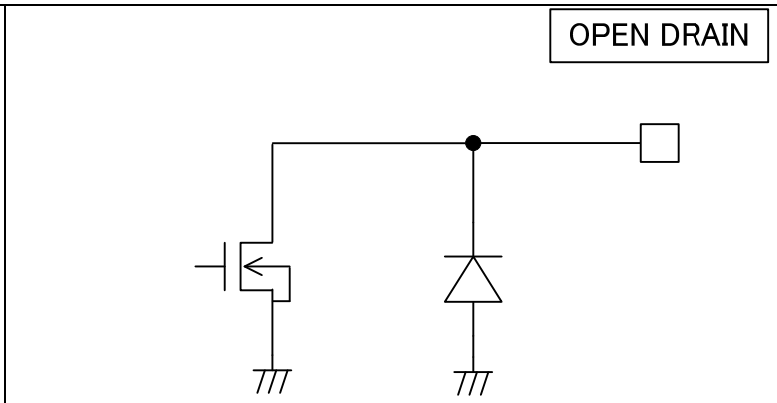
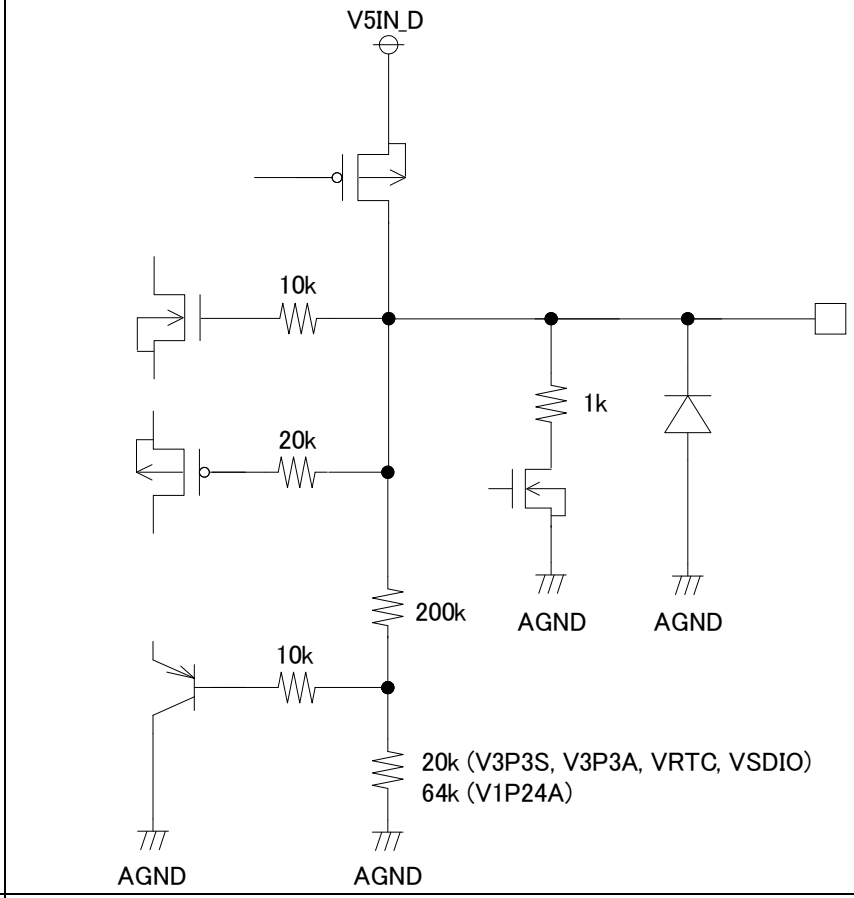
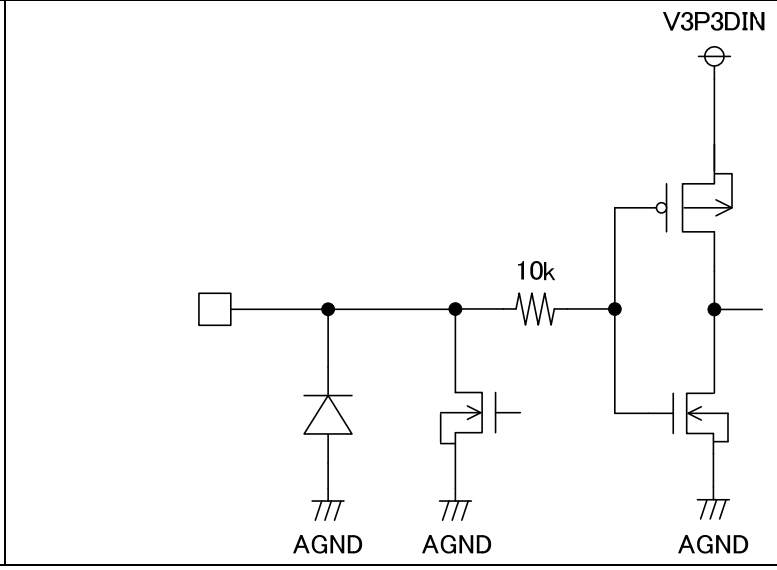
I/O Equivalent Circuit – continued

VSFR (PIN17) V1P24S (PIN19)	
SRTC_RST_B (PIN20) SUS_STAT_B (PIN21) ERROR (PIN22) RTCCLK (PIN33)	
SLP_S4_B (PIN23) SLP_S3_B (PIN24) SDMMC3_V1P8_EN (PIN25) SDMMC3_PWREN_B (PIN26) SUSPWRDNACK (PIN32) POWER_ON (PIN44)	

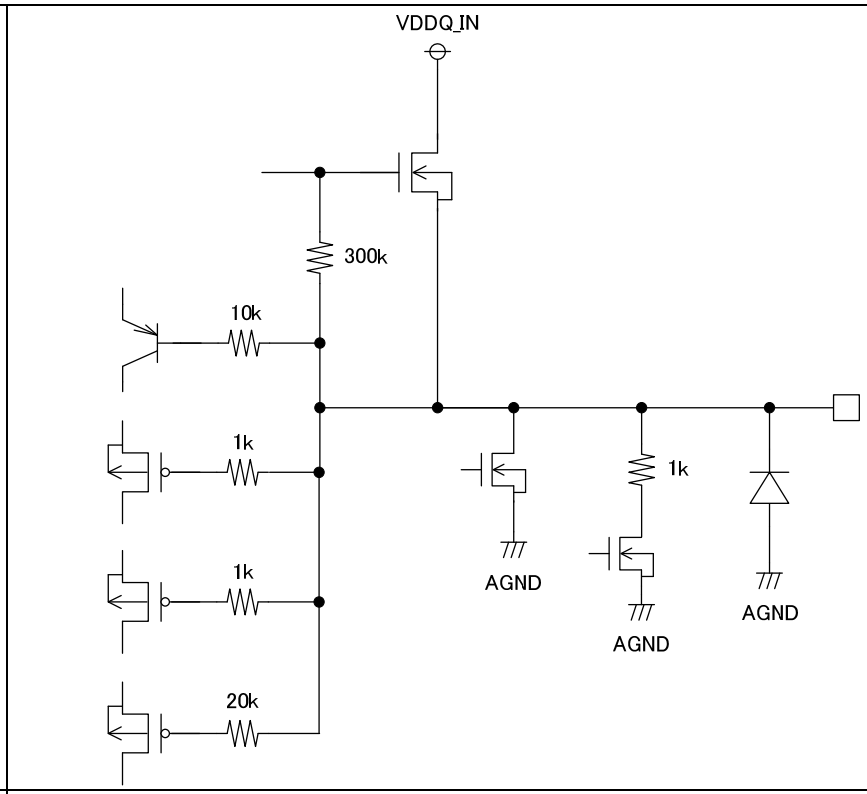
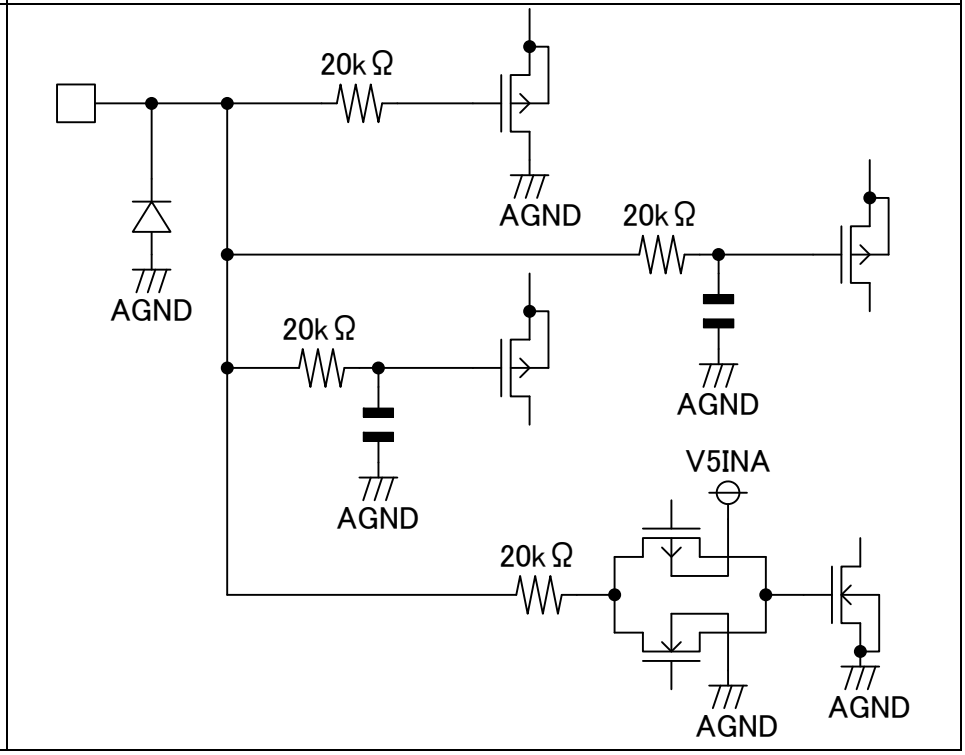
I/O Equivalent Circuit – continued

SYNC (PIN27)	
SPARE (PIN28)	
SVID_CLK (PIN29)	
SVID_DATA (PIN30)	

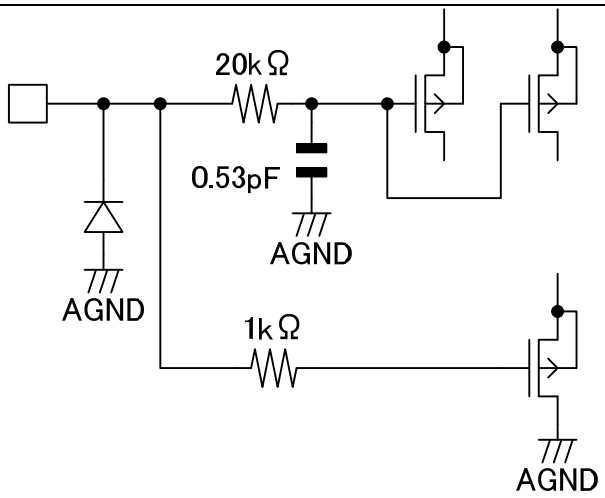
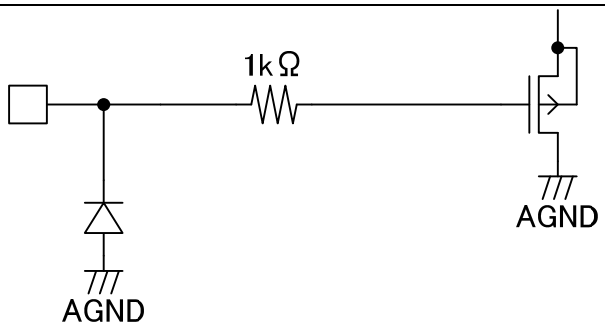
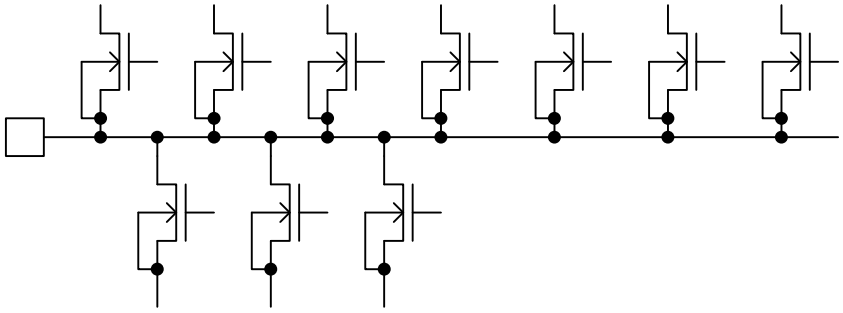
I/O Equivalent Circuit – continued

SVID_ALERT_B (PIN31) PWRBTN_B (PIN45) CLK (PIN46) COREPWROK (PIN48) DRAMPWROK (PIN49) RSMRST_B (PIN50) RTEST_B (PIN51)	
V3P3S (PIN37) V3P3A (PIN39) VRTC (PIN40) V1P24A (PIN41) VSDIO (PIN42)	
DATA (PIN47)	

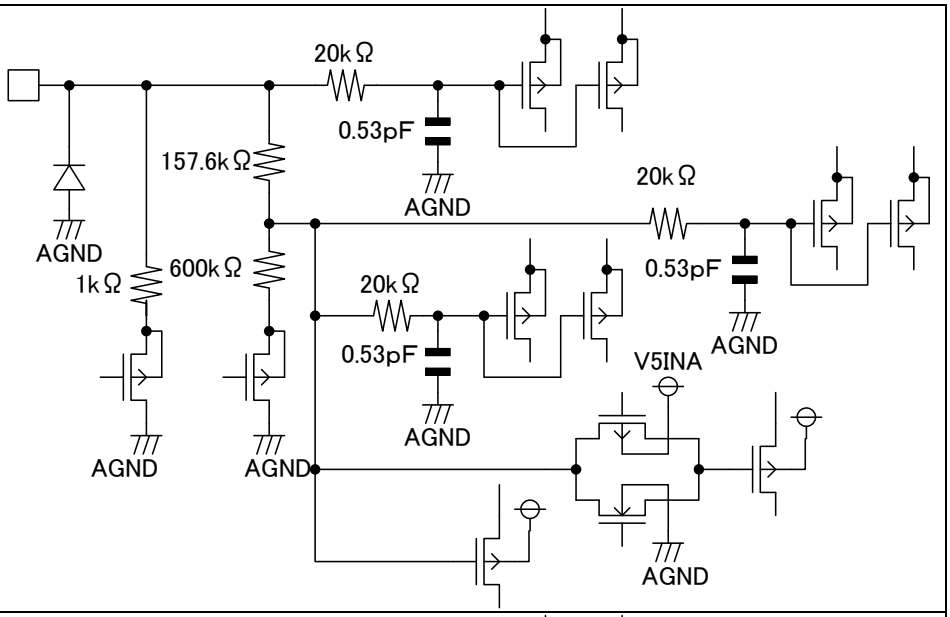
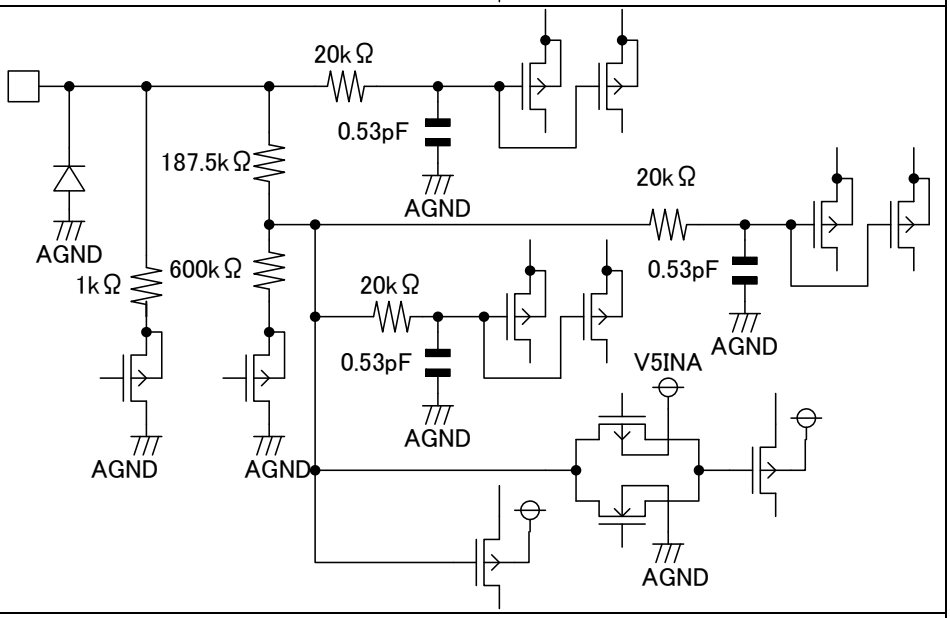
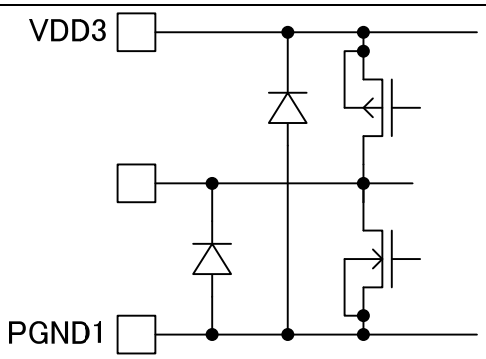
I/O Equivalent Circuit – continued

VTT (PIN53)	
FB_VDDQ (PIN64)	

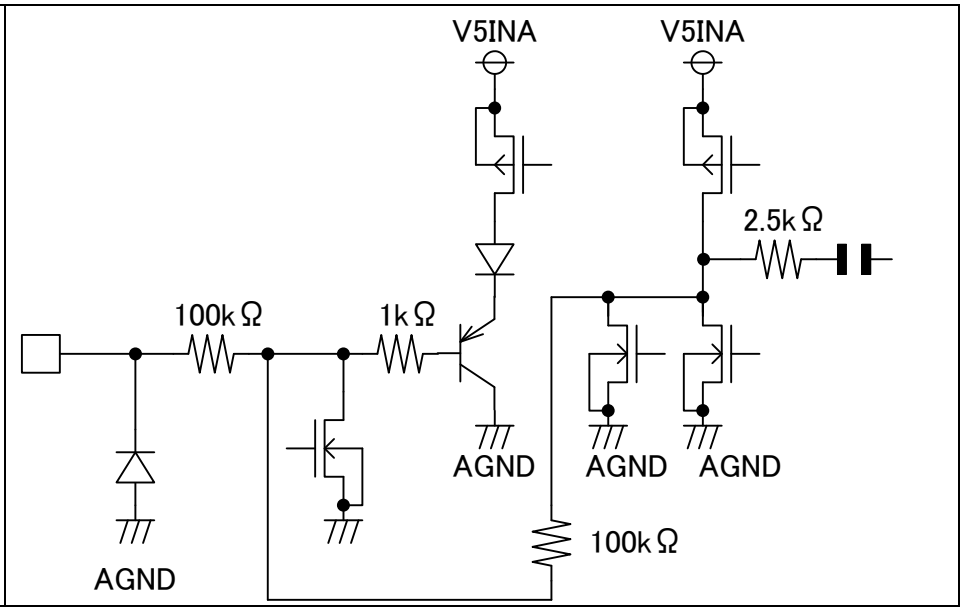
I/O Equivalent Circuit – continued

IS_M_VDDQ (PIN65) IS_M_V1P0S (PIN73)	
IS_P_VDDQ (PIN66) IS_P_V1P0S (PIN72)	
SW_VDDQ (PIN61) SW_V1P0S (PIN69)	

I/O Equivalent Circuit – continued

FB_V1P0S (PIN74)	
FB_V1P05S (PIN75)	
SW_V1P05S (PIN77)	

I/O Equivalent Circuit – continued

REMOTE_M_VCC (PIN87) REMOTE_M_VNN (PIN88)	

7. Operational Notes

(1) Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(2) Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(3) Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

(4) Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

(5) Thermal Consideration

Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

(6) Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(7) Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

(8) Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

(9) Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(10) Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

(11) Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So, unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

(12) Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

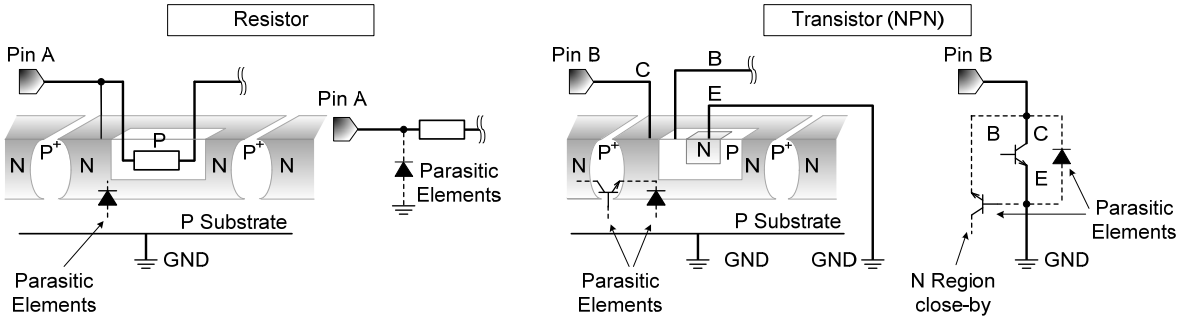


Figure 75. Example of monolithic IC structure

(13) Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

(14) Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

(15) Over Current Protection Circuit (OCP)

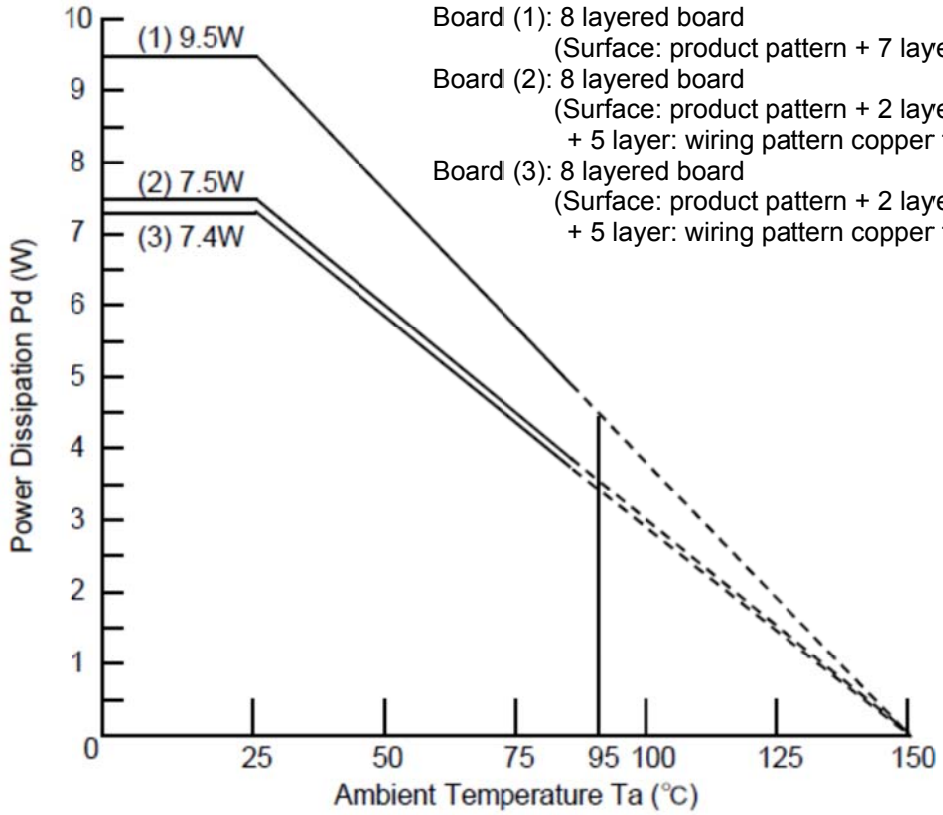
This IC has a built-in overcurrent protection circuit that activates when the output is accidentally shorted. However, it is strongly advised not to subject the IC to prolonged shorting of the output.

8. Power Dissipation

Use of a heat sink may be necessary depending on the environmental condition.

UQFN88MV0100

Measurement machine: TH-156 (Kuwano Denki)
Measurement condition: mounted on a user's specified board size
Board size: 95mm × 95mm × 1.6mmt
(With thermal via)



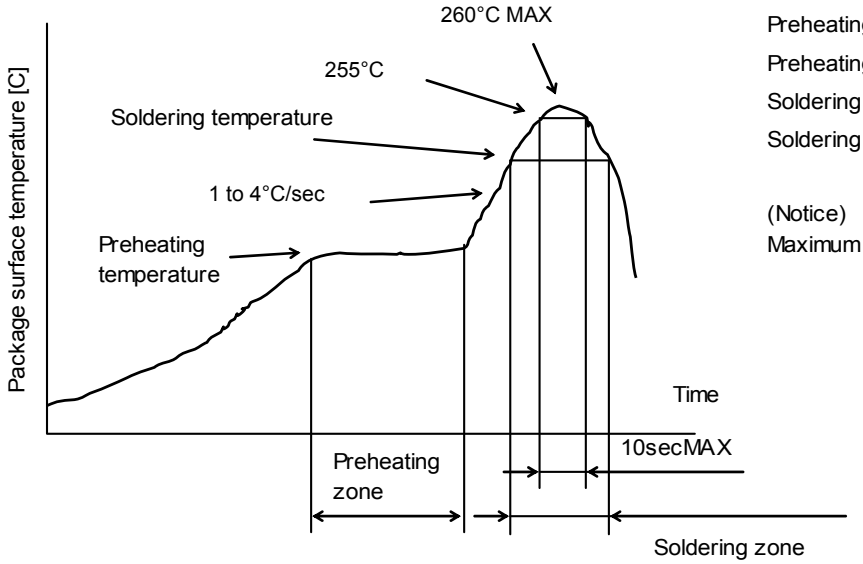
Board (1): 8 layered board
(Surface: product pattern + 7 layers: all copper foil area)
Board (2): 8 layered board
(Surface: product pattern + 2 layers: all copper foil area
+ 5 layer: wiring pattern copper foil 70% occupied)
Board (3): 8 layered board
(Surface: product pattern + 2 layers: all copper foil area
+ 5 layer: wiring pattern copper foil 50% occupied)

(Note) This is a measured value, not guaranteed.

Figure 76. Power Dissipation

9. Soldering Condition

Recommended temperature profile for reflow



Preheating temperature : 130°C to 190°C
Preheating zone : 120sec MAX
Soldering temperature : 220°C to 240°C
Soldering zone : 75sec MAX

(Notice)
Maximum 2-times soldering

The wave soldering method is not supported.

10. History

Table 19: Revision History

Rev.	Date	Notes
Rev.001	2015/01/07	First release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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