Management IC for Automotive Microcontroller

System Regulator for microcontroller for automotive

BD39012EFV-C

General Description

BD39012EFV-C is a power management IC with 1 ch DC / DC convertor, 1 ch LDO, reset and watch dog timer. It can supply the power supply to module from battery directly. LDO has reset built-in and always watches that it supplies stable power supply to module. In addition, window watch dog timer is provided to detect the abnormality of the microcomputer. BD39012EFV-C enables a superior heat dissipation and a compact PCB design by HTSSOP-B24 package.

Key Specifications

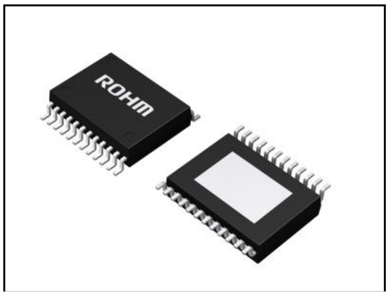
- Input voltage range: 4 V to 45 V
  (Startup voltage needs to be above 4.5V.)
- Output Voltage Accuracy
  Step-down DC / DC Converter FB Voltage: 0.8 V ±2 %
  Secondary LDO: 5.0 V ±2 %
- Output Maximum Current
  Step-down DC / DC Converter: 1.0 A
  Secondary LDO: 0.4 A
- Operating Frequency
  Step-down DC / DC Converter: 200 k to 600 kHz (Typ)
- Standby Current: 0 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Features

- Synchronous rectifier step-down DC / DC converter with built-in FET (Adjustable output)
- Secondary LDO with built-in 5 V output FET
- Monitoring function
  Output over voltage / under voltage detection (PG output), Reset function (LDO)
  Window Watchdog Timer
- Built-in protection function
  Input under voltage protection (UVLO)
  Thermal shut down (TSD)
  Output over current protection (OCP)
- Independent enable control
- HTSSOP-B24 package

Package

Package	W(Typ) x D(Typ) x H(Max)
HTSSOP-B24	7.80 mm x 7.60 mm x 1.00 mm

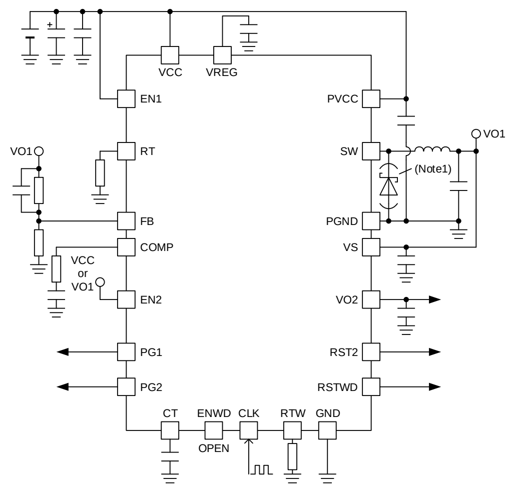


HTSSOP-B24

Applications

- Microcontroller for Automotive

Typical Application Circuit



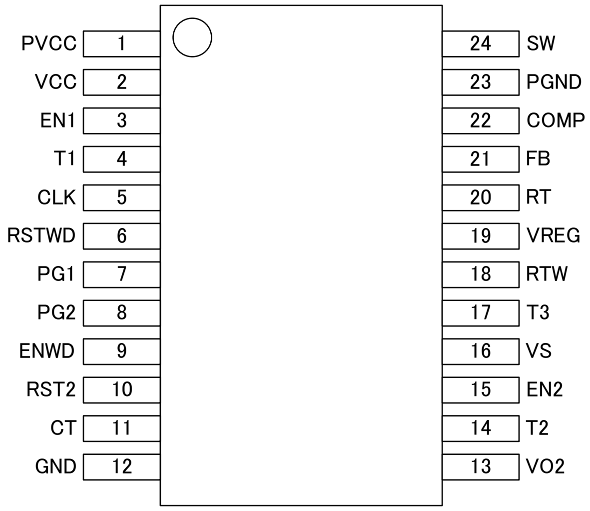
☆These specifications may be changed without a notice.

(Note 1) Please connect when the application is that the load current of VO1 output exceed in 500 mA.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration

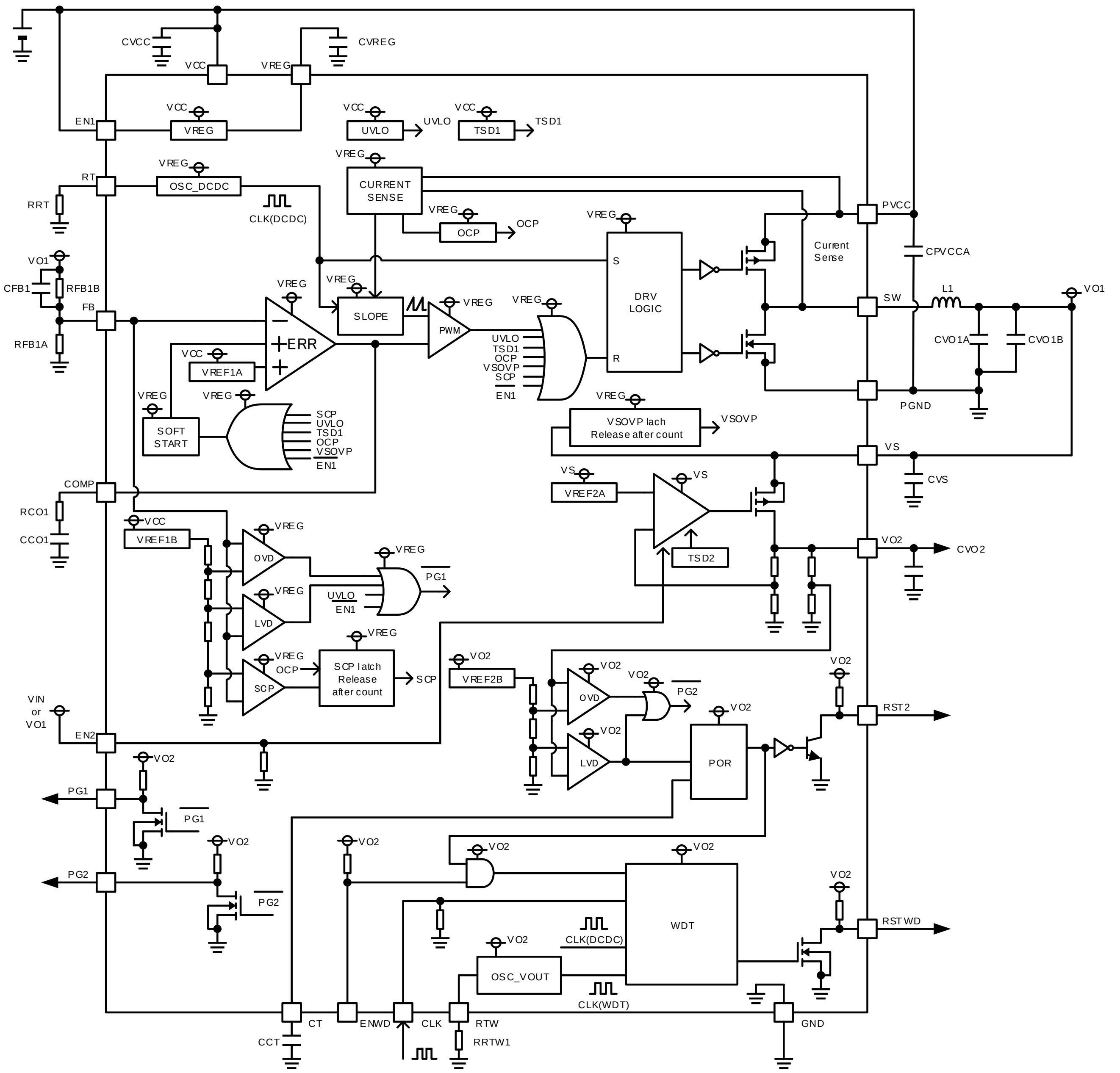


Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	PVCC	Power VCC supply terminal	13	VO2	LDO output terminal
2	VCC	Signal VCC supply terminal	14	T2	Test terminal (Note1)
3	EN1	Enable terminal (DC / DC)	15	EN2	Enable terminal (LDO)
4	T1	Test terminal (Note1)	16	VS	Power supply input terminal for LDO
5	CLK	WDT CLK input terminal	17	T3	Test terminal (Note1)
6	RSTWD	Reset output terminal (WDT monitoring)	18	RTW	Frequency setting terminal for WDT
7	PG1	Power good output terminal (DC / DC monitoring)	19	VREG	Internal power supply terminal
8	PG2	Power good output terminal (LDO monitoring)	20	RT	Frequency setting terminal for DC / DCl
9	ENWD	Enable terminal (WDT)	21	FB	DC / DC output voltage feed buck terminal
10	RST2	Reset output terminal (LDO monitoring)	22	COMP	DC / DC error amp output terminal
11	CT	Power on reset time setting capacitor connect terminal	23	PGND	Power GND terminal
12	GND	Signal GND terminal	24	SW	DC / DC output terminal

(Note 1) Be sure to connect to ground.

Block Diagram



Description of Blocks

- Internal Power Supply (VREG)
  It is the block which generates 4.0 V internal power supply voltage. It is a power supply to supply to the IC inside.
  Please do not be connected to the outside circuit.
  VREG needs to outside capacitor more than 1 μF. Low capacitor of the ESR is recommended.

- Enable (EN1)
  The circuit becomes standby state when EN1 pin becomes less than 0.8 V. Internal power supply and DC / DC convertor are OFF and consumption current from VCC becomes 0 μA (25 °C, Typ) when standby state.
  It can be used when connected to VCC or inputted into the signal from a microcomputer.

- Soft Start (SOFT START)
  The Soft start is a block to prevent over short of the output voltage in the startup and inrush current to an output step.
  With controlling error amp input voltage and increasing switching pulse width gradually, it prevents then.
  Because the soft start time operate an internal counter by oscillation frequency and decides time, it depends on the oscillation frequency setting of the DC / DC converter. It becomes 3.28 ms (Typ) when oscillation frequency is 500 kHz.
  It reboots after an internal SS pin is discharged when VSOVP, TSD1, and SCP are detected.

- Error Amp (ERR)
  The error amp compares the output feedback voltage to the 0.8V reference voltage. This comparison result is output to COMP pin as current. By the voltage of the COMP pin, switching duty is decided. In the startup because soft start is taken, COMP voltage is limited by SOFT START voltage. In addition, COMP pin needs to outside resistance and capacitor for phase compensation.

- PWM COMP (PWM)
  PWM comparator makes a conversion to a continuous duty cycle to control an output transistor in the voltage of COMP pin. The duty becomes 100 % and the high-side output transistor becomes ON state if input voltage becomes less than setting output voltage.

- Oscillation frequency for DC / DC convertor (OSC_DCDC)
  Oscillation frequency is decided by the current which is caused by resistance connected to RT pin.
  The range of oscillation frequency can be set 200 kHz to 600 kHz.
  Short circuit protection starts operating and oscillator stops when RT pin is short-circuited to ground.

- Short Circuit Protection (SCP)
  DC / DC convertor stores with short circuit protection. The short circuit protection starts operation after the short circuit protection circuit considers that the output is in short state when the over current protection starts operation in a state with FB pin voltage less than 0.45 V (Typ) (Except during soft start).
  DC / DC convertor output is OFF when the short circuit protection starts operation. In addition, SOFT START is initialized and COMP pin is discharged. Afterwards, it reboots after 1,024 cycles of the oscillation frequency.

- Reference Voltage of 2 systems
  DC / DC convertor and LDO have a reference voltage which is made from an independent block in both output voltage part and abnormal detection part.
  In this way, even if there was an abnormality in reference voltage of whichever it is suitable for a safe design because abnormality can be informed from PG pin
  Each reference voltage is used as follows.
  VREF1A: Reference of DC / DC convertor output voltage and VREG voltage.
  VREF1B: Reference of DC / DC convertor OVD, LVD, SCP, VSOVP and OCP.
  VREF2A: Reference of LDO output voltage.
  VREF2B: Reference of LDO OVD and LVD.

- Over Voltage Detection (OVD)
  PG1 pin becomes L when reference voltage of DC / DC convertor exceeds 0.95 V (Typ).
  PG2 pin becomes L when output voltage of LDO exceeds 5.38 V (Typ).

- Low Voltage Detection (LVD)
  PG1 pin becomes L when reference voltage of DC / DC convertor is less than 0.65 V (Typ).
  PG2 pin becomes L when output voltage of LDO is less than 4.62 V (Typ).

- Over Current Protection Circuit (OCP, SCP)
  DC / DC convertor and LDO store with over current protection. Current limit is taken in the over current detection of the DC / DC converter, and ON duty cycle is limited, and output voltage decreases. In addition, when it becomes overloaded and FB pin voltage decreases and is less than 0.45 V (Typ), SCP is detected. Afterwards, it reboots after 1,024 cycles of the oscillation frequency. Current limit is taken in the over current detection of the LDO, and output voltage decreases (foldback current limiting characteristic). When it load-short-circuited, it prevents the destruction of the IC, but this protection circuit is effective for prevention of destruction by the sudden accident. It is not supported use at the continuous protection circuit operation and a transitional period.

- DRV LOGIC
  This is the driver block of FET. It drives SW pin.

- Over Voltage Protection Circuit (VSOVP_latch)
  VS pin possesses over voltage protection. If the voltage of the VS pin becomes more than over voltage detection level 13.5 V (Typ), it starts operation. SS and COMP is discharged after DC / DC output is OFF when the over voltage protection circuit starts operation. Afterwards, it reboots after 1,024 cycles of the oscillation frequency from release when VS returned to 13.0 V (Typ). VSOVP is effective for prevention of destruction by the sudden accident. VSOVP is effective for prevention of the destruction by the sudden accident. Please avoid using it at continuous protection circuit operation.

- Under Voltage malfunction prevention circuit (UVLO_VCC)
  DC / DC convertor circuit shuts down after UVLO starts operating when VCC voltage is less than 3.5 V (Typ).
  It starts normal operating after UVLO is released when VCC voltage is more than 4.0 V (Typ).
  Please apply more than 4.45 V to the VCC voltage in initial startup.

- Thermal Shut Down (TSD1, TSD2)
  DC / DC convertor (TSD1) and LDO (TSD2) of BD39012EFV-C, each has thermal shutdown and operates individually.
  The protection is taken when chip temperature Tj exceeds 175 °C (Typ). DC / DC convertor lets the switching OFF.
  The Output is OFF in LDO. In addition, it returns if it becomes less than 150 °C (Typ).

- SLOPE, CURRENT SENCE
  This block is a block to give slope compensation of the current mode of DC / DC convertor and current return.

- LDO Block
  LDO operates by full independence. Even if it is the state that does not contain the voltage in PVCC pin and VCC pin, power on reset (POR), watch dog timer (WDT), PG2 pin, RST pin, RSTWD pin and ENWD pin become effective when a power supply is spent to VS pin.
  But OSC_WDT ERR Detect informing abnormality does not function. (Timing chart 6 (*4))

- Power On Reset (POR)
  POR starts charge to the outside capacitor of CT pin (= CCT) when VO2 of LDO output releases under voltage detect.
  RST2 pin outputs `H` when CT pin voltage becomes more than 1.18 V (Typ). CCT is discharged and RST2 pin outputs `L` when VO2 detects low voltage. Please set the setting range of CCT in the range of 0.001 µF from 10 µF

- Oscillator for Watch Dog Timer (OSC_VOUT)
  This block creates a reference frequency of the Watch Dog Timer. The oscillation frequency is determined by the RTW resistance. The oscillation frequency can be set in the range of 50 kHz to 250 kHz.
  Short circuit protection starts operating and oscillator stops when RTW pin is short-circuited to ground.

- Watch Dog Timer (WDT)
  Microcontroller (µC) operation is monitored with CLK pin. Window watch dog timer is included to enhance the assurance of the system. WDT starts operating when POR and ENWD becomes high. It watches both edges (rising edge, falling edge) of the CLK pin. When the width of both edges is lower than the watch dog lower limit (Fast NG) or more than the watch dog upper limit (Slow NG), RSTWD is made low during WDT reset time (tWRES) (µC ERR Detect).
  Fast NG and Slow NG are decided by the number of the counts of OSC_WDT. Therefore a time change of Fast NG and Slow NG is possible by changing frequency of OSC_WDT. In addition, it lets RSTWD low and informs abnormality when abnormality occurs in OSC_WDT (including the RTW pin ground) (OSC_WDT ERR Detect).

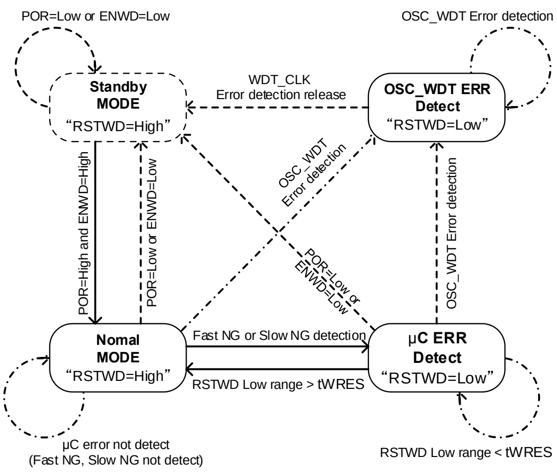


Figure 1. Witch Dog Timer State Change Diagram (WDT FSM)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	-0.3 to 45 (Note 1)	V
Output Switch Pin Voltage	VSW	-0.3 to VCC	V
EN1 Pin Voltage	VEN1	-0.3 to 45	V
VREG Pin Voltage	VREG	-0.3 to 7	V
RT, FB, COMP Pin Voltage	VRT, VFB, VCOMP	-0.3 to 7	V
VS Pin Voltage	VS	-0.3 to 45*1	V
EN2 Pin Voltage	VEN2	-0.3 to 45	V
VO2 Pin Voltage	VO2	-0.3 to 7	V
PG1, PG2 Pin Voltage	VPG1, VPG2	-0.3 to VO2	V
RST2, RSTWD Pin Voltage	VRST2, VRSTWD	-0.3 to VO2	V
CT Pin Voltage	VCT	-0.3 to 7 (Note 2)	V
RTW Pin Voltage	VRTW	-0.3 to 7	V
ENWD Pin Voltage	VENWD	-0.3 to VO2	V
CLK Pin Voltage	VCLK	-0.3 to 7	V
Power Dissipation (Note 3)	Pd	4.0	W
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

(Note 1) Pd, should not be exceeded
(Note 2) VS+0.3 V, should not be exceeded.
(Note 3) Derating in done 32.0 mW / °C for operating above Ta ≥ 25 °C (Mount on 4-layer 70.0mm x 70.0mm x 1.6mm board)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Operating Power Supply Voltage	VCC	4 (Note 4)	-	36 (Note 5)	V
VS Operating Voltage	VS	6.0	-	10	V
Switch Current	ISW	0	-	1	A
Oscillation Frequency	FOSC	200	-	600	kHz
WDT Oscillation Frequency	FOSCW	50	-	250	kHz
LDO Output Current	IVO2	0	-	0.4 (Note 5)	A
Operating Temperature Range	Topr	-40	-	125	°C

(Note 4) Initial startup is over 4.45 V
(Note 5) Pd, should not be exceeded

Electrical Characteristics (Unless otherwise specified Ta = -40 to 125 °C, VCC = 4 to 36 V)

Parameter	Symbol	Min	Typ	Max	Unit	Function
< The Whole >						
Standby Circuit Current 1	ISTB1	-	0	10	µA	VEN1 = 0 V, Ta = 25 °C
Standby Circuit Current 2	ISTB2	-	-	50	µA	VEN1 = 0 V
VCC Circuit Current	IQVCC	-	2	4	mA	FB = 0 V
VS Circuit Current	IQVS	-	505	1100	µA	VS = 6 V, VEN2 = 5 V, ENWD = 0 V, RTW = 24 kΩ, CLK = 0 V, PG1, PG2, RST2, RSTWD = H
UVLO Detection Voltage	VUVLO	3.3	3.5	3.7	V	VCC detection
UVLO Hysteresis Voltage	VUVLOHYS	0.25	0.5	0.75	V	VCC detection
VREG Output Voltage	VVREG	3.6	4.0	4.4	V	
EN1L Threshold Voltage	VEN1L	-	-	0.8	V	
EN1H Threshold Voltage	VEN1H	3.5	-	-	V	
EN1 Inflow Current	IEN1	-	13	26	µA	VEN1 = 5 V
< DCDC >						
Pch MOSFET ON Resistance	RONSWP	-	0.4	1	Ω	ISW = 300 mA
Nch MOSFET ON Resistance	RONSWN	-	0.4	1	Ω	ISW = -300 mA
Over Current Protection	IOLIM	1	-	-	A	
Output Leak Current 1	ISWLK1	-	0	10	µA	VEN1 = 0 V, Ta = 25 °C
Output Leak Current 2	ISWLK2	-	-	50	µA	VEN1 = 0 V
Reference Voltage	VREF	0.784	0.800	0.816	V	VCOMP = VFB
FB Input Bias Current	IFBB	-1	-	1	µA	FB = 0.8 V
Soft Start Time	TSS	2.70	3.28	4.00	ms	RT = 24 kΩ
Oscillation Frequency	FOSC	450	500	550	kHz	RT = 24 kΩ
VS Over Voltage Detection	VVSOVP	11	13.5	16	V	
PG1 Pull-up Resistance	RPUPG1	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
PG1 Output L Voltage	VPG1L	-	-	0.3	V	PG1, PG2, RST2, RSTWD pin short (Note 1)
PG1 Low Voltage Detection Voltage	VLVD1	0.60	0.65	0.70	V	VFB monitor, PG1 output
PG1 Over Voltage Detection Voltage	VOVD1	0.90	0.95	1.00	V	VFB monitor, PG1 output

(Note 1) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of PG1.

Electrical Characteristics – Continued (Unless otherwise specified Ta = -40 to 125 °C, VCC = 4 to 36 V)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
< LDO / Reset >						
Output Voltage	VO2	4.90	5.00	5.10	V	5 mA to 400 mA, VS = 6.0 V to 10 V
Drop Voltage 1	ΔVdd1	-	0.17	0.33	V	VS = 4.75 V, Io = 200 mA
Drop Voltage 2	ΔVdd2	-	0.33	0.67	V	VS = 4.75 V, Io = 400 mA
EN2L Threshold Voltage	VEN2L	-	-	0.8	V	
EN2H Threshold Voltage	VEN2H	2.8	-	-	V	
EN2 Inflow Current	IEN2	-	25	50	μA	VEN2 = 5 V
Under Voltage Detection Detection Voltage	VRST2DET	4.50	4.62	4.75	V	
Under Voltage Detection Hysteresis	VRST2DETH	20	60	100	mV	
Power On Reset Time	tPOR0	10	14	18	ms	CCT = 0.1 μF (Note 2)
RST2 Pull-up Resistance	RPURST2	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
RST2 Output L Voltage	VRST2L	-	0.15	0.30	V	VO2 ≥ 1 V, PG1, PG2, RST2, RSTWD pin short (Note 3)
PG2 Pull-up Resistance	RPUPG2	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
PG2 Output L Voltage	VPG2L	-	-	0.3	V	PG1, PG2, RST2, RSTWD pin short (Note 4)
PG2 Low Voltage Detection Voltage	VLVD2	4.50	4.62	4.75	V	VO2 monitor, PG2 output
PG2 Over Voltage Detection Voltage	VOVD2	5.25	5.38	5.50	V	VO2 monitor, PG2 output

(Note 2) Power on reset time tPOR can be changed by capacity of the capacitor to connect to CT. (Available range 0.001 to 10 μF)
tPOR (ms) ≒ tPOR0 (Reset delay time at the time of the 0.1 μF connection) × CCT (μF) / 0.1 CT capacity: 0.1 ≤ CCT ≤ 10 μF
tPOR (ms) ≒ tPOR0 (Reset delay time at the time of the 0.1 μF connection) × CCT (μF) / 0.1 (±0.1) CT capacity: 0.001 ≤ CCT ≤ 0.1 μF
(Note 3) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of RST2.
(Note 4) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of PG2.

Electrical Characteristics – Continued (Unless otherwise specified Ta = -40 to 125 °C, VCC = 4 to 36 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
< WDT >						
WDT Oscillation Frequency	FOSCW	75	100	125	kHz	RTW = 24 kΩ, VO2 = 4.9 V to 5.1 V
CLK FAST NG Threshold	tWF	123 / FOSCW	128 / FOSCW	133 / FOSCW	s	CLK edge time
CLK SLOW NG Threshold	tWS	865 / FOSCW	870 / FOSCW	875 / FOSCW	s	
WDT Reset Time	tWRES	123 / FOSCW	128 / FOSCW	133 / FOSCW	s	
CLK Detection Minimum Pulse Width	WCLK	1	-	-	µs	
CLK L Threshold Voltage	VCLKL	-	-	0.8	V	
CLK H Threshold Voltage	VCLKH	2.6	-	-	V	
CLK Inflow Current	ICLK	-	25	50	µA	VCLK = 5 V
ENWD L Threshold Voltage	VENWDL	-	-	0.2 × VO2	V	VO2 = 4.9 V to 5.1 V
ENWD H Threshold Voltage	VENWDH	0.8 × VO2	-	-	V	VO2 = 4.9 V to 5.1 V
ENWD Pull-up Resistance	RPURENWD	100	200	300	kΩ	
RSTWD Pull-up Resistance	RPURSTWD	30	50	75	kΩ	Internal Resistance (VO2 Pull-up)
RSTWD Output L Voltage	VRSTWDL	-	-	0.3	V	PG1, PG2, RST2, RSTWD pin short (Note 5)

(Note 5) PG1, PG2, RST2, RSTWD pin is shorted. In the case of ON, it is met only Tr of RSTWD.

Typical Performance Curves

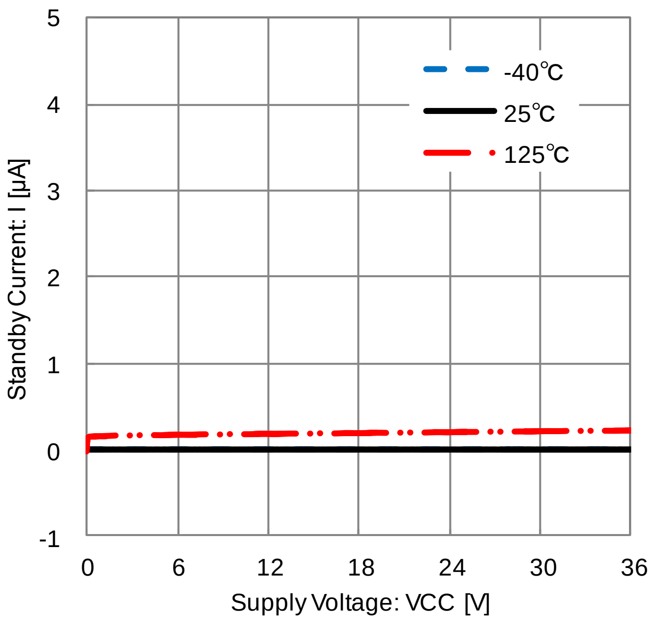


Figure 2. Standby Current vs Supply Voltage
(Standby Circuit Current)

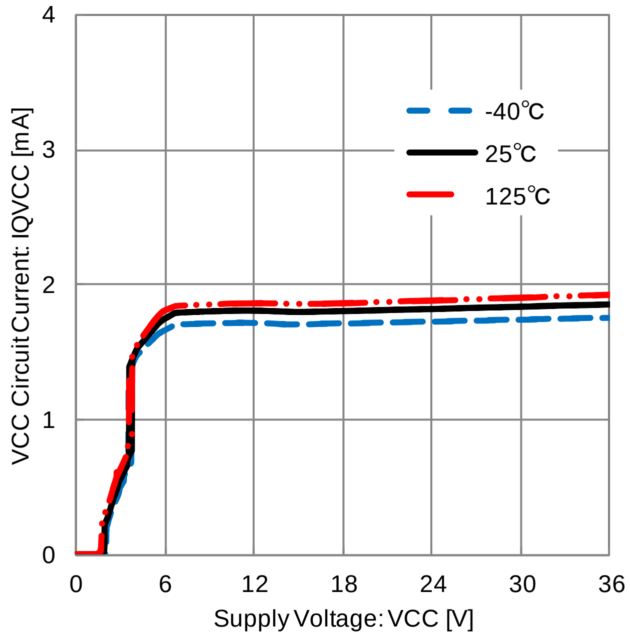


Figure 3. VCC Circuit Current vs Supply Voltage
(VCC Circuit Current)

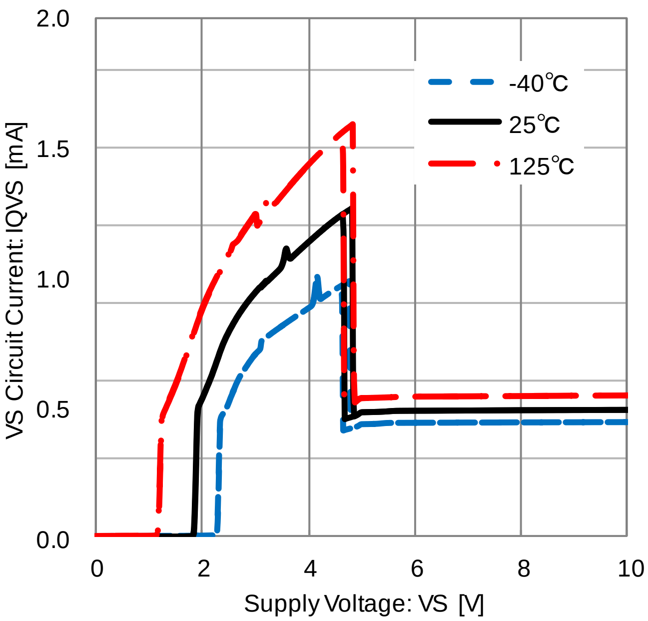


Figure 4. VS Circuit Current vs VS Supply Voltage
(VS Circuit Current)

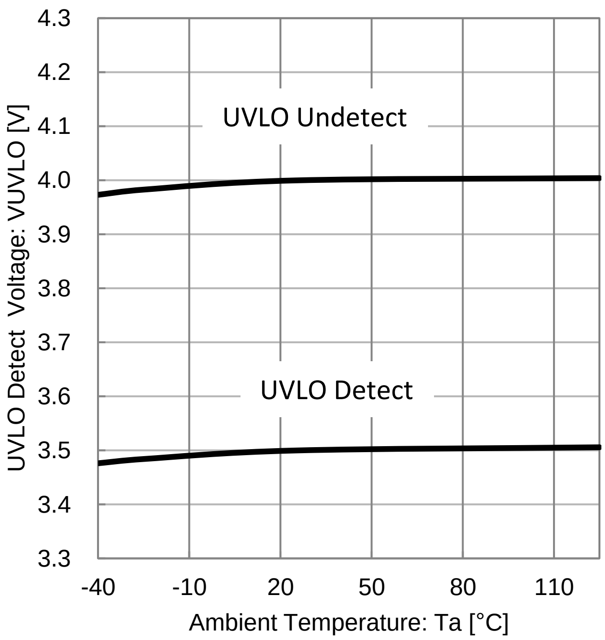


Figure 5. UVLO Detect Voltage vs Ambient Temperature
(UVLO Detection Voltage)

Typical Performance Curves - continued

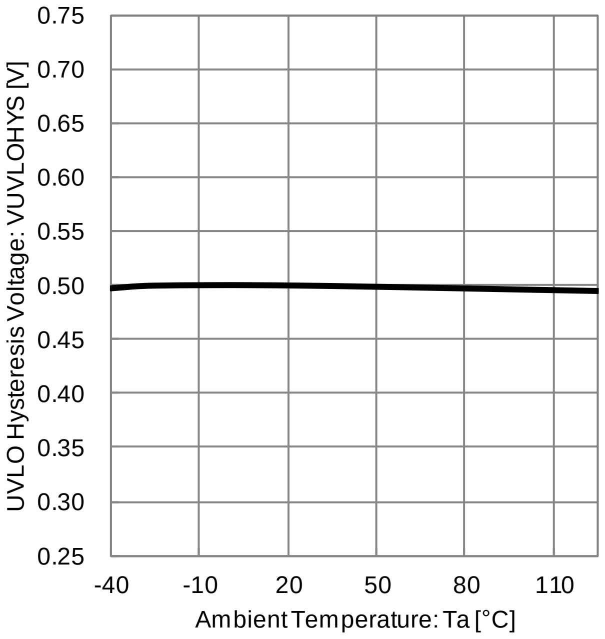


Figure 6. UVLO Hysteresis Voltage vs Ambient Temperature
(UVLO Hysteresis Voltage)

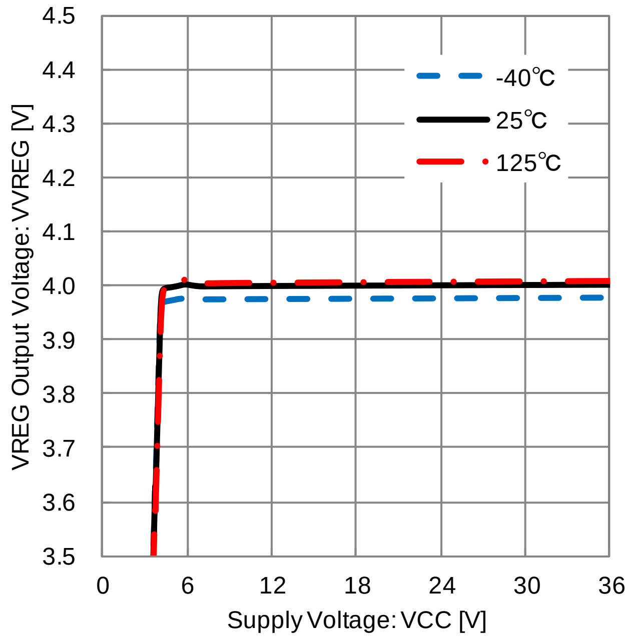


Figure 7. VREG Output Voltage vs Supply Voltage
(VREG Output Voltage)

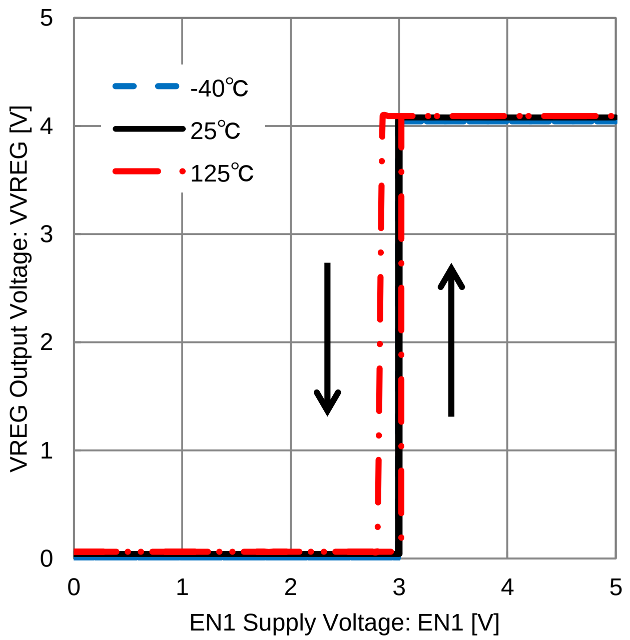


Figure 8. VREG Output Voltage vs EN1 Supply Voltage
(EN Threshold Voltage)

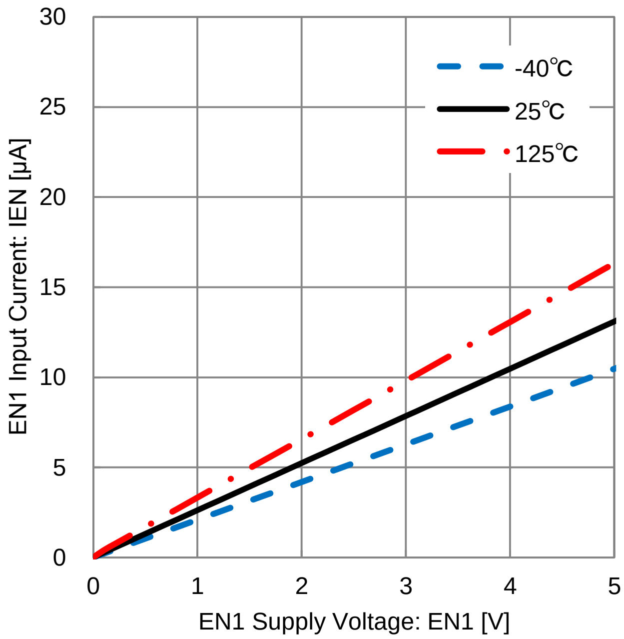


Figure 9. EN1 Input Current vs EN1 Supply Voltage
(EN Inflow Current)

Typical Performance Curves - continued

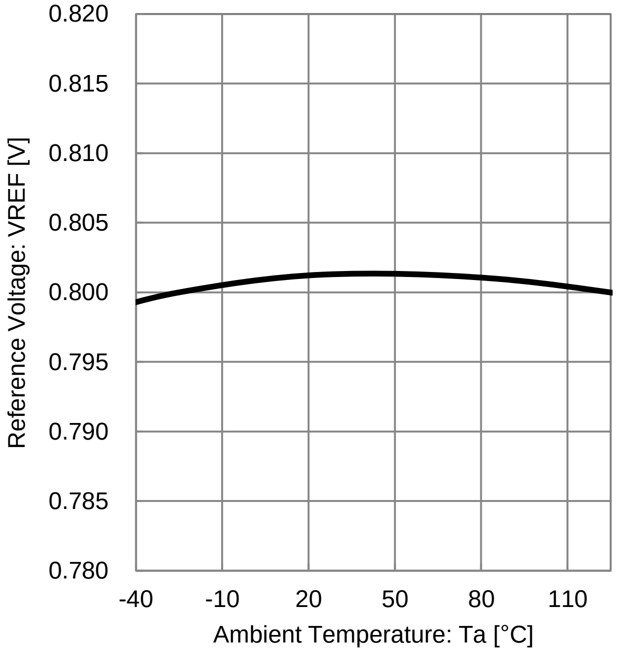


Figure 10. Reference Voltage vs Ambient Temperature
(Reference Voltage)

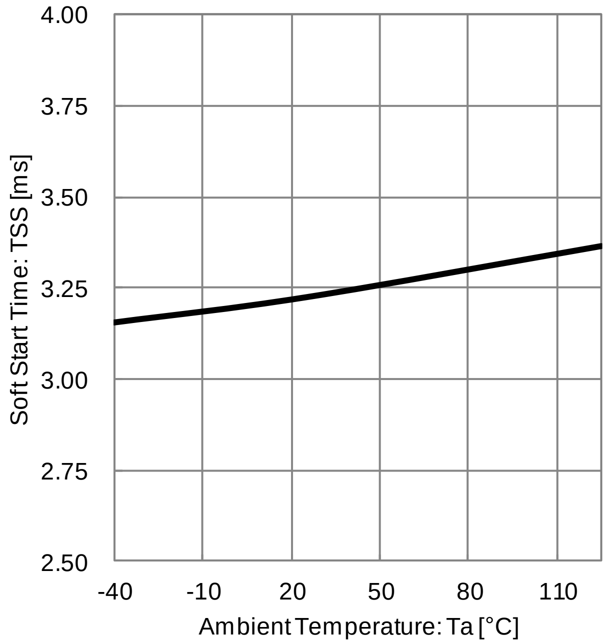


Figure 11. Soft Start Time vs Ambient Temperature
(Soft Start Time)

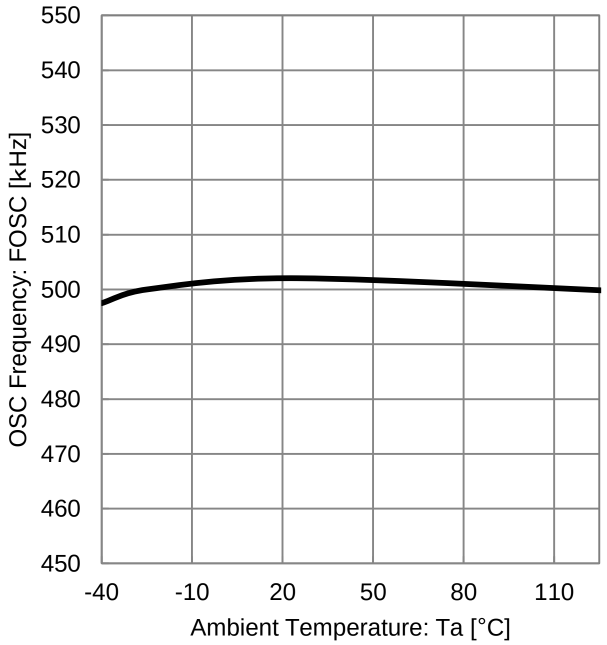


Figure 12. OSC Frequency vs Ambient Temperature
(Oscillation Frequency)

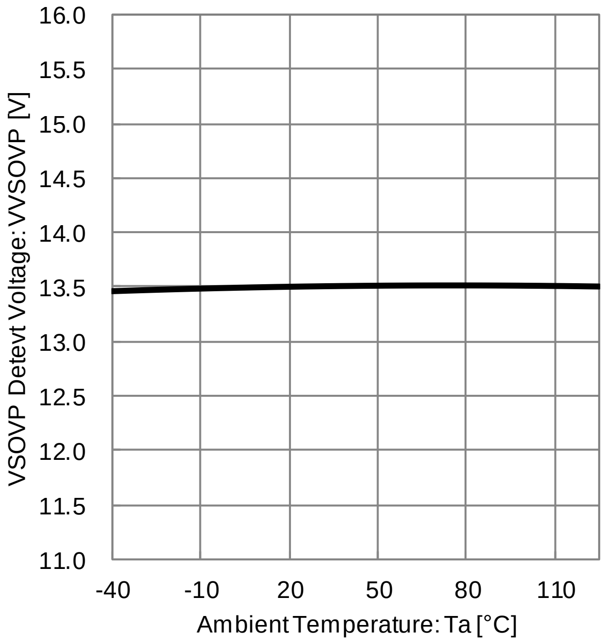


Figure 13. VSOVP Detect Voltage vs Ambient Temperature
(VS Over Voltage Detection)

Typical Performance Curves - continued

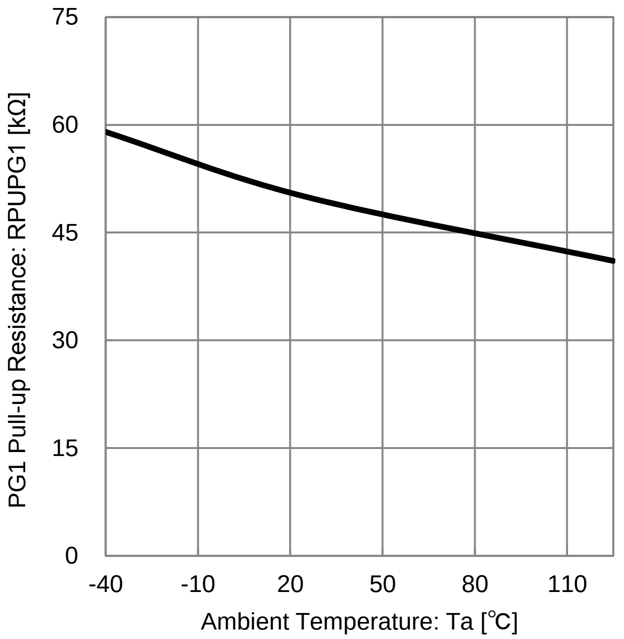


Figure 14. PG1 Pull-up Resistance vs Supply Voltage
(PG1 Pull-up Resistance)

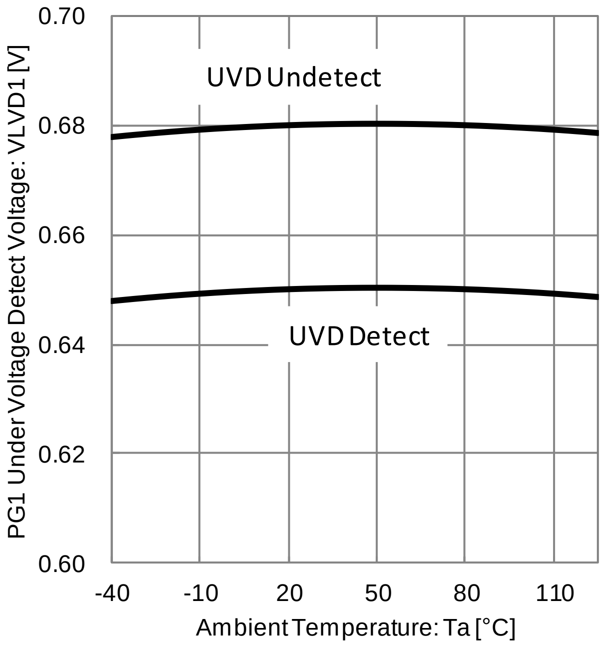


Figure 15. PG1 Under Voltage Detect Voltage
vs Ambient Temperature
(PG1 Low Voltage Detection Voltage)

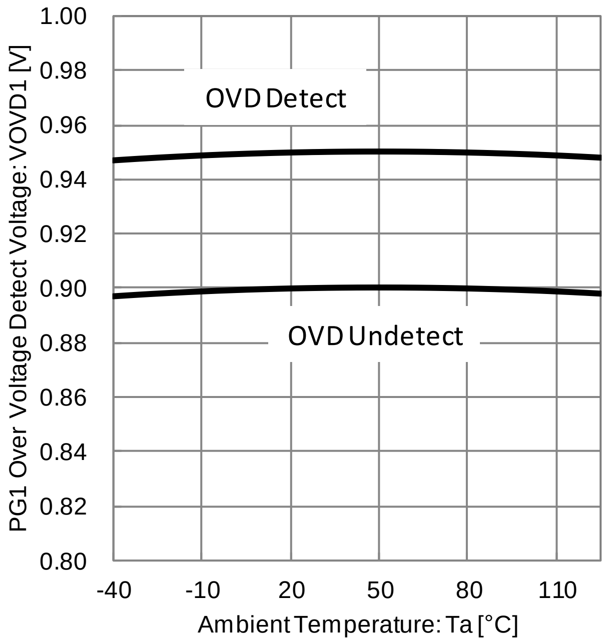


Figure 16. PG1 Over Voltage Detect Voltage
vs Ambient Temperature
(PG1 Over Voltage Detection Voltage)

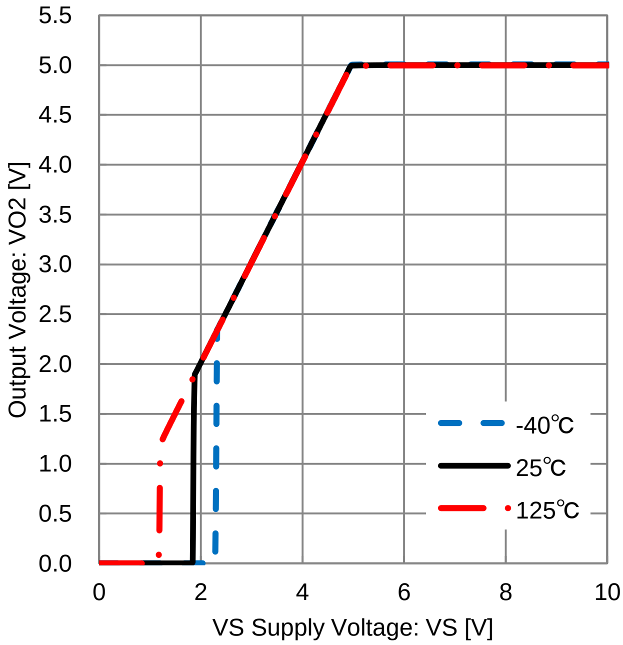


Figure 17. Output Voltage vs VS Supply Voltage
(Output Voltage)

Typical Performance Curves - continued

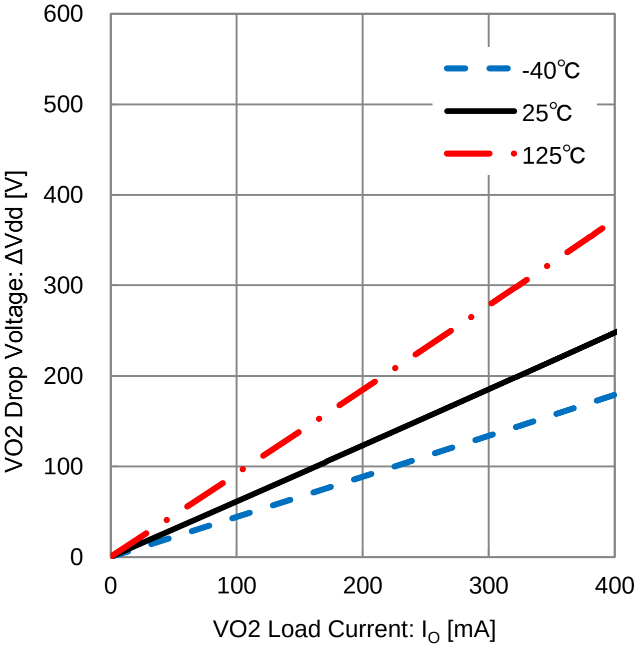


Figure 18. VO2 Drop Voltage vs VO2 Load Current (Drop Voltage)

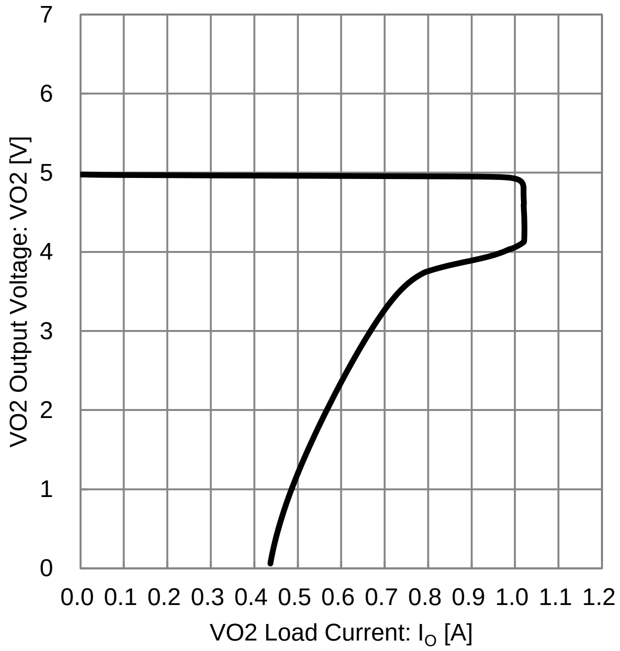


Figure 19. VO2 Output Voltage vs VO2 Load Current (LDO OCP)

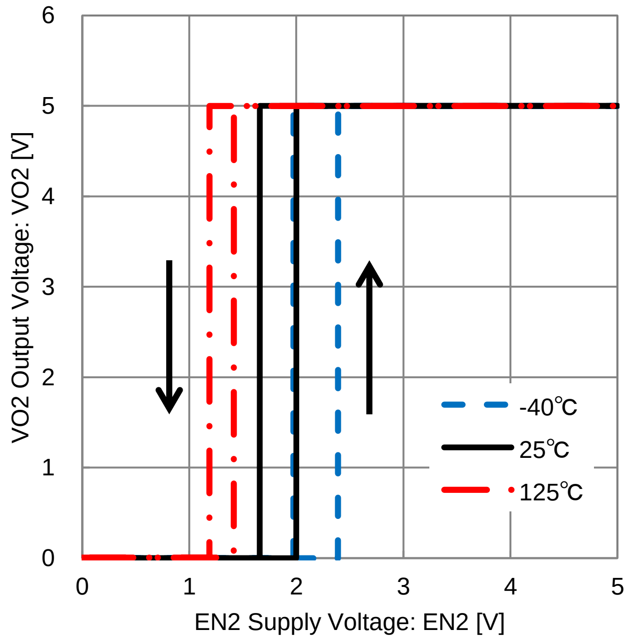


Figure 20. VO2 Output Voltage vs EN2 Supply Voltage (EN2 Threshold Voltage)

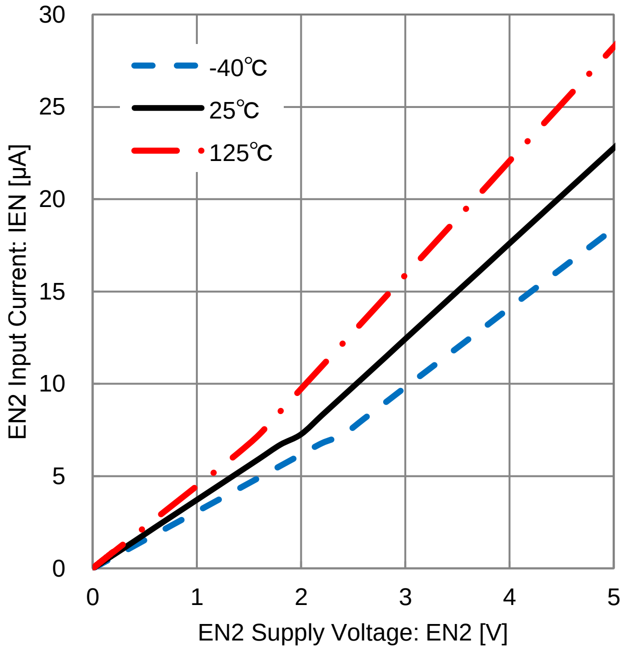


Figure 21. EN2 Input Current vs EN2 Supply Voltage (EN2 Inflow Current)

Typical Performance Curves - continued

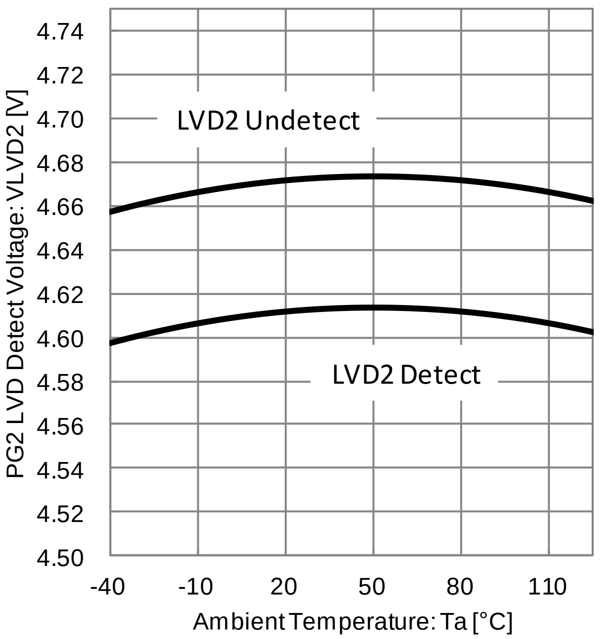


Figure 22. PG2 LVD Detect Voltage vs Ambient Temperature (PG2 Low Voltage Detection Voltage)

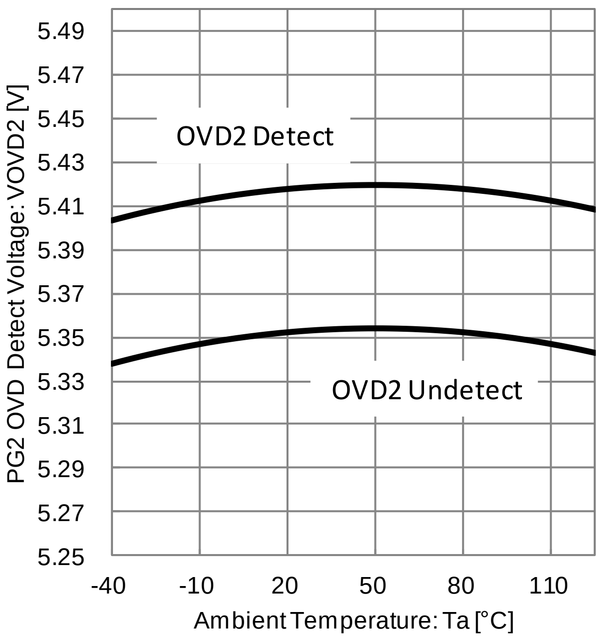


Figure 23. PG2 OVD Detect Voltage vs Ambient Temperature (PG2 Over Voltage Detection Voltage)

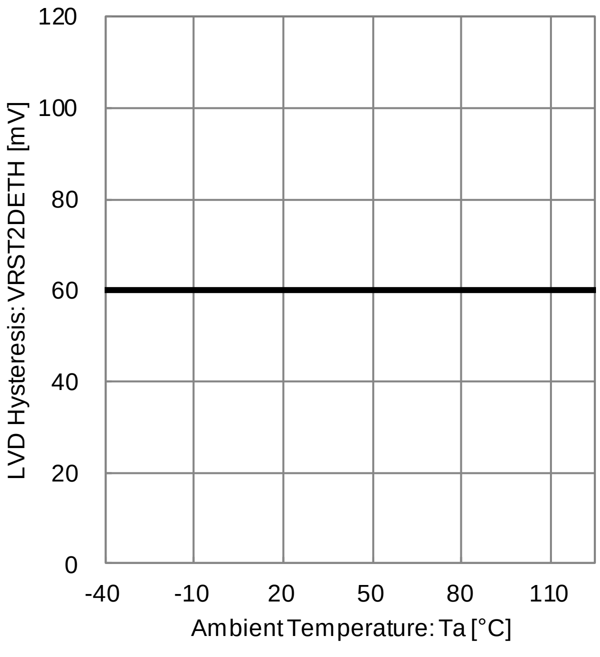


Figure 24. LVD Hysteresis vs Ambient Temperature (Under Voltage Detection Hysteresis)

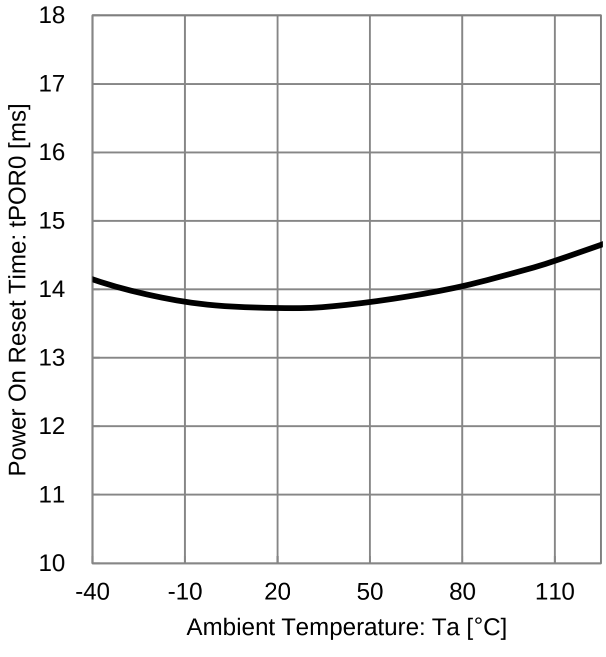


Figure 25. Power On Reset Time vs Ambient Temperature (Power On Reset Time)

Typical Performance Curves - continued

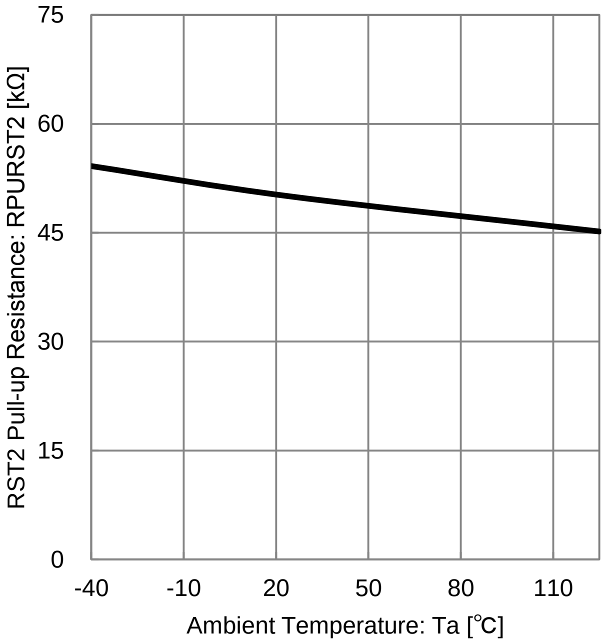


Figure 26. RST2 Pull-up Resistance vs Ambient Temperature (RST2 Pull-up Resistance)

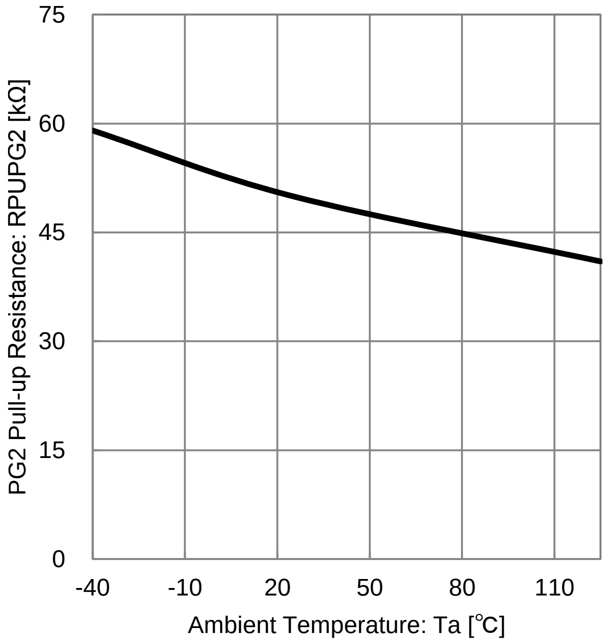


Figure 27. PG2 Pull-up Resistance vs Ambient Temperature (PG2Pull-up Resistance)

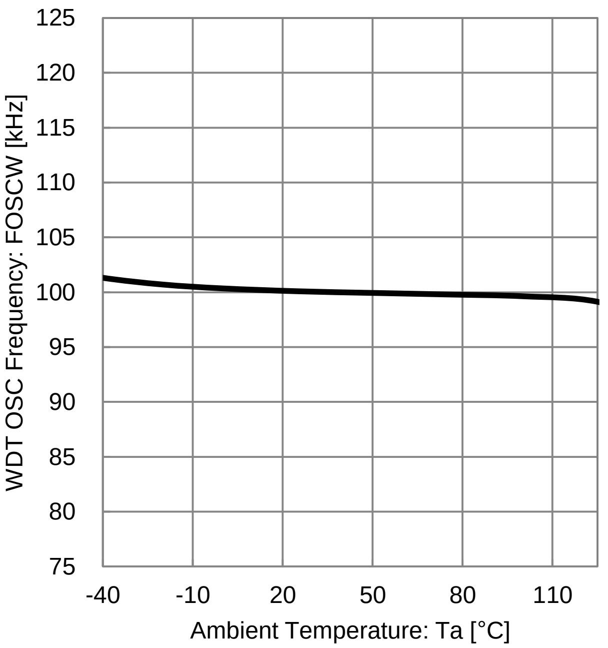


Figure 28. WDT OSC Frequency vs Ambient Temperature (WDT Oscillation Frequency)

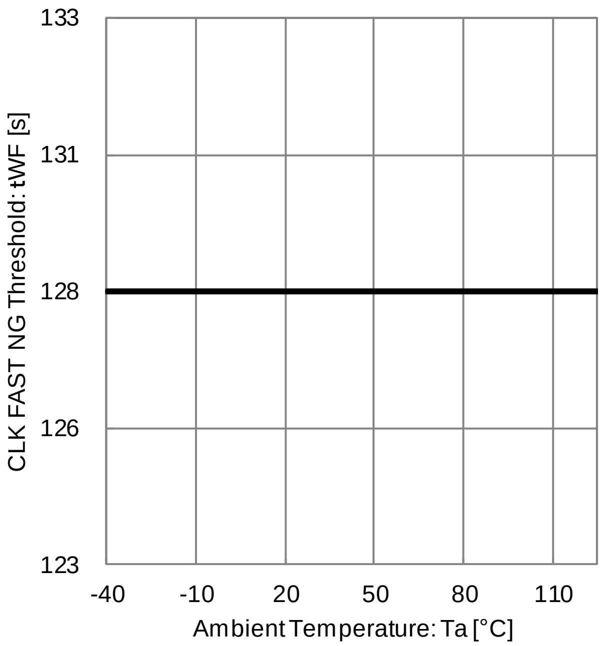


Figure 29. CLK FAST NG Threshold vs Ambient Temperature (CLK FAST NG Threshold)

Typical Performance Curves - continued

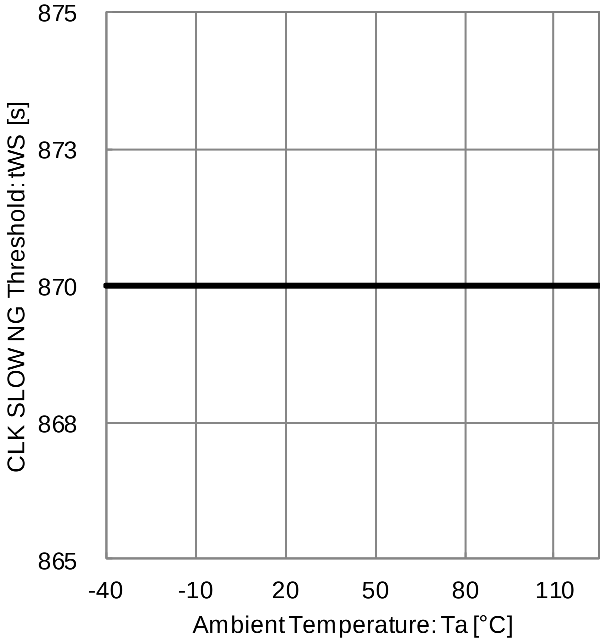


Figure 30. CLK SLOW NG Threshold vs Ambient Temperature (CLK SLOW NG Threshold)

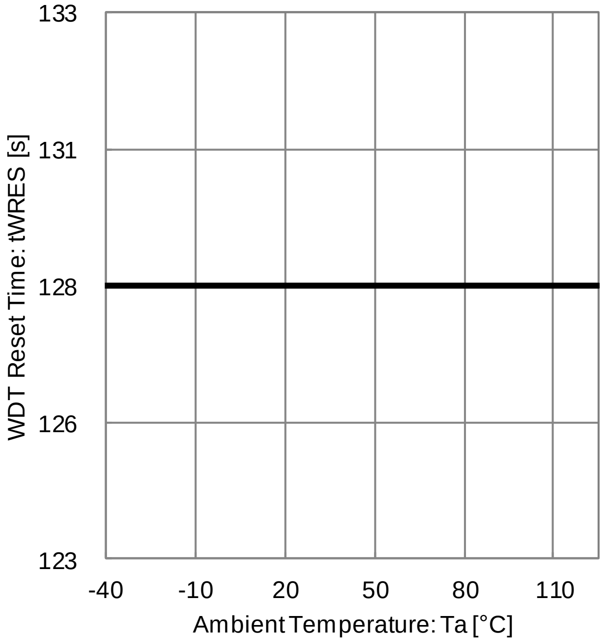


Figure 31. WDT Reset Time vs Ambient Temperature (WDT Reset Time)

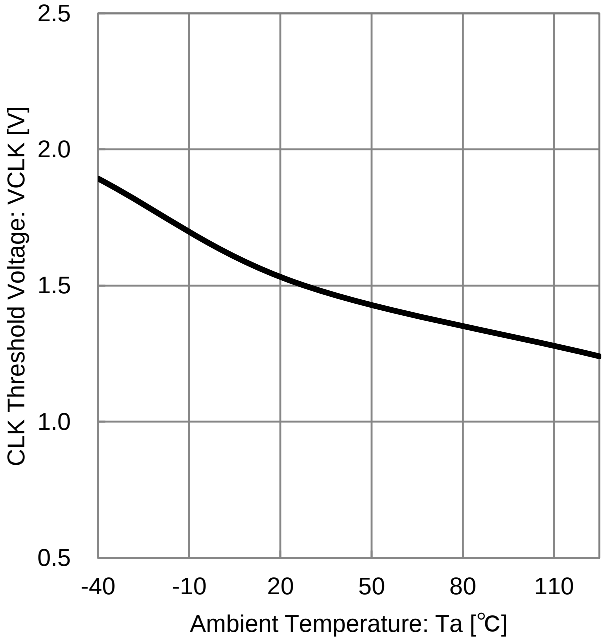


Figure 32. CLK Threshold Voltage vs Ambient Temperature (CLK Threshold Voltage)

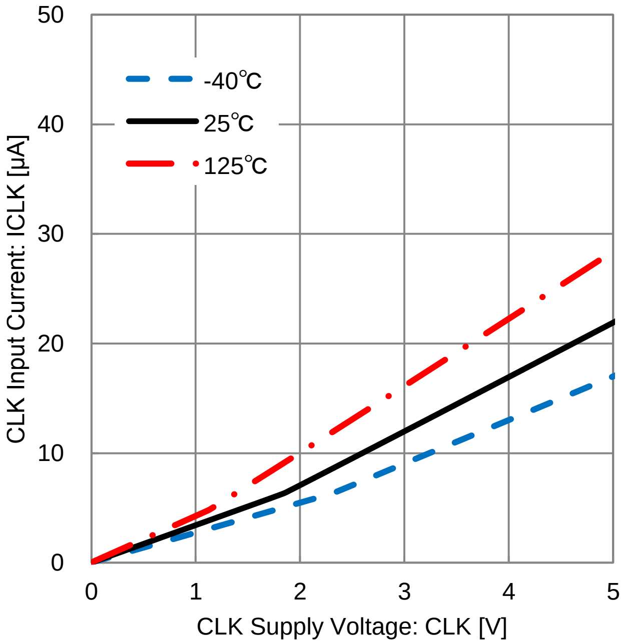


Figure 33. CLK Input Current vs CLK Supply Voltage (CLK Inflow Current)

Typical Performance Curves - continued

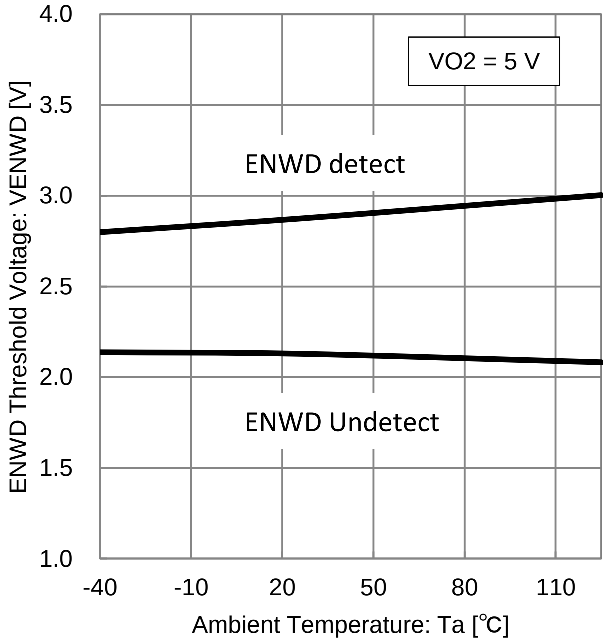


Figure 34. ENWD Threshold Voltage vs Ambient Temperature
(ENWD Threshold Voltage)

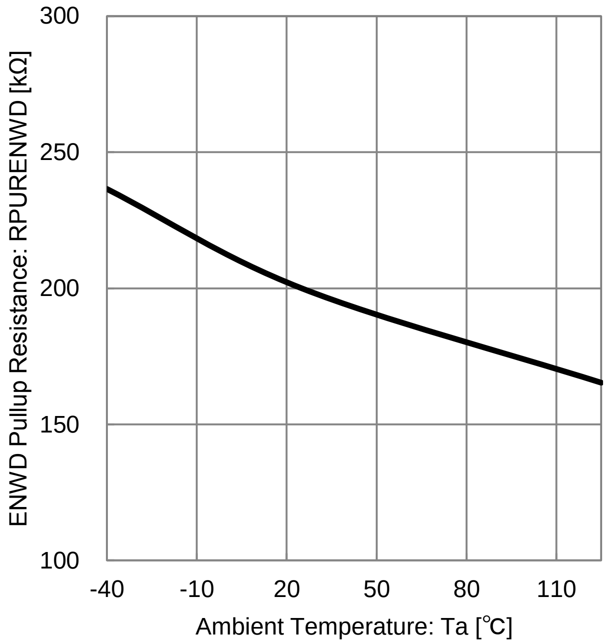


Figure 35. ENWD Pull-up Resistance
vs Ambient Temperature
(ENWD Pull-up Resistance)

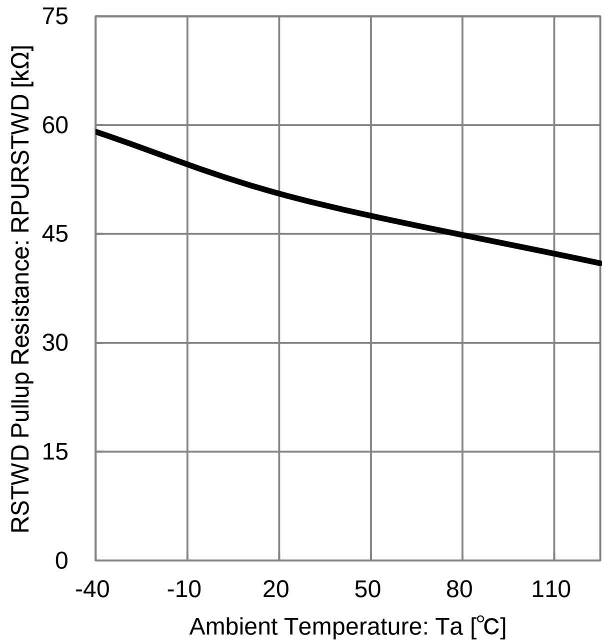
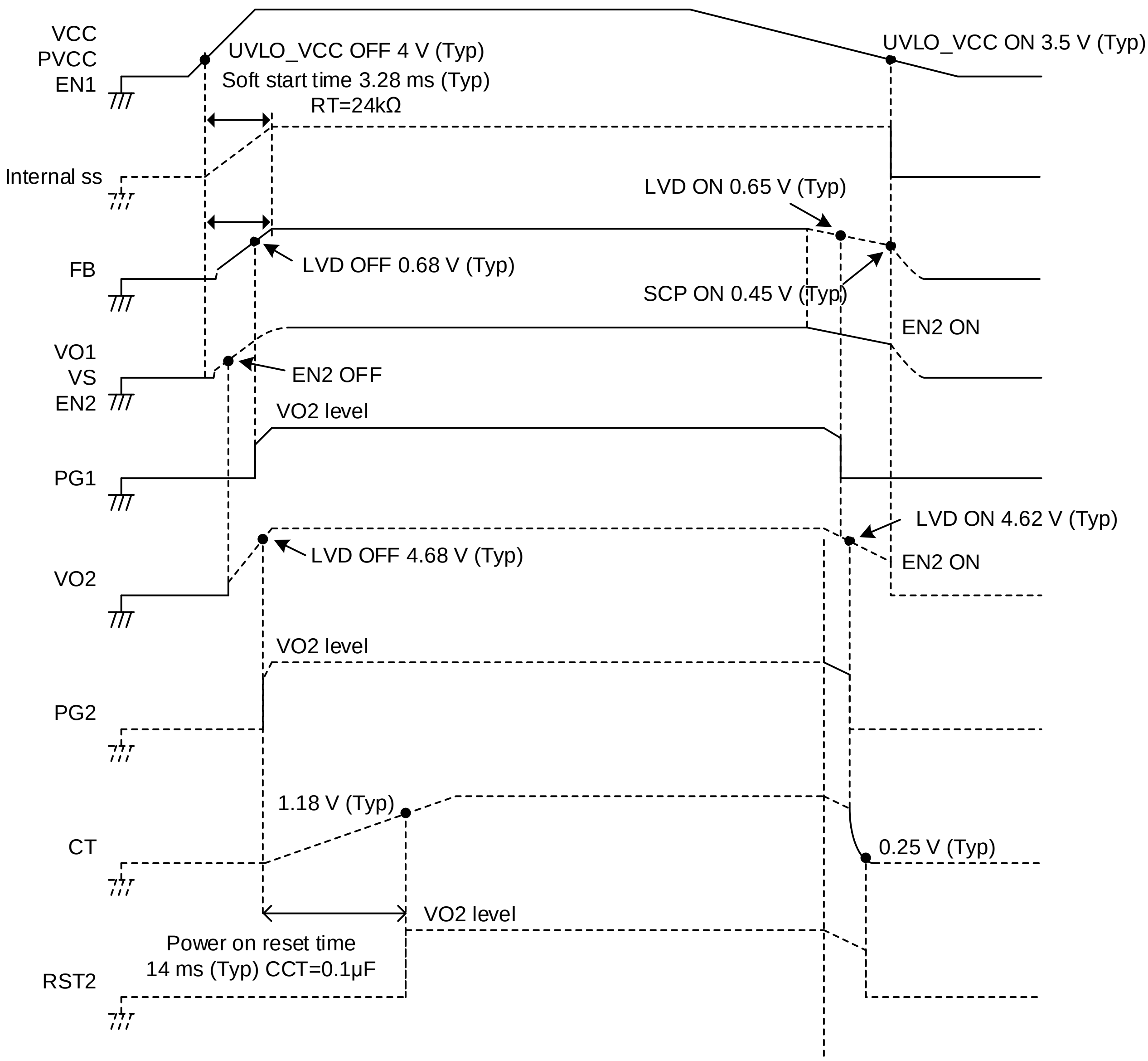


Figure 36. RSTWD Pull-up Resistance
vs Ambient Temperature
(RSTWD Pull-up Resistance)

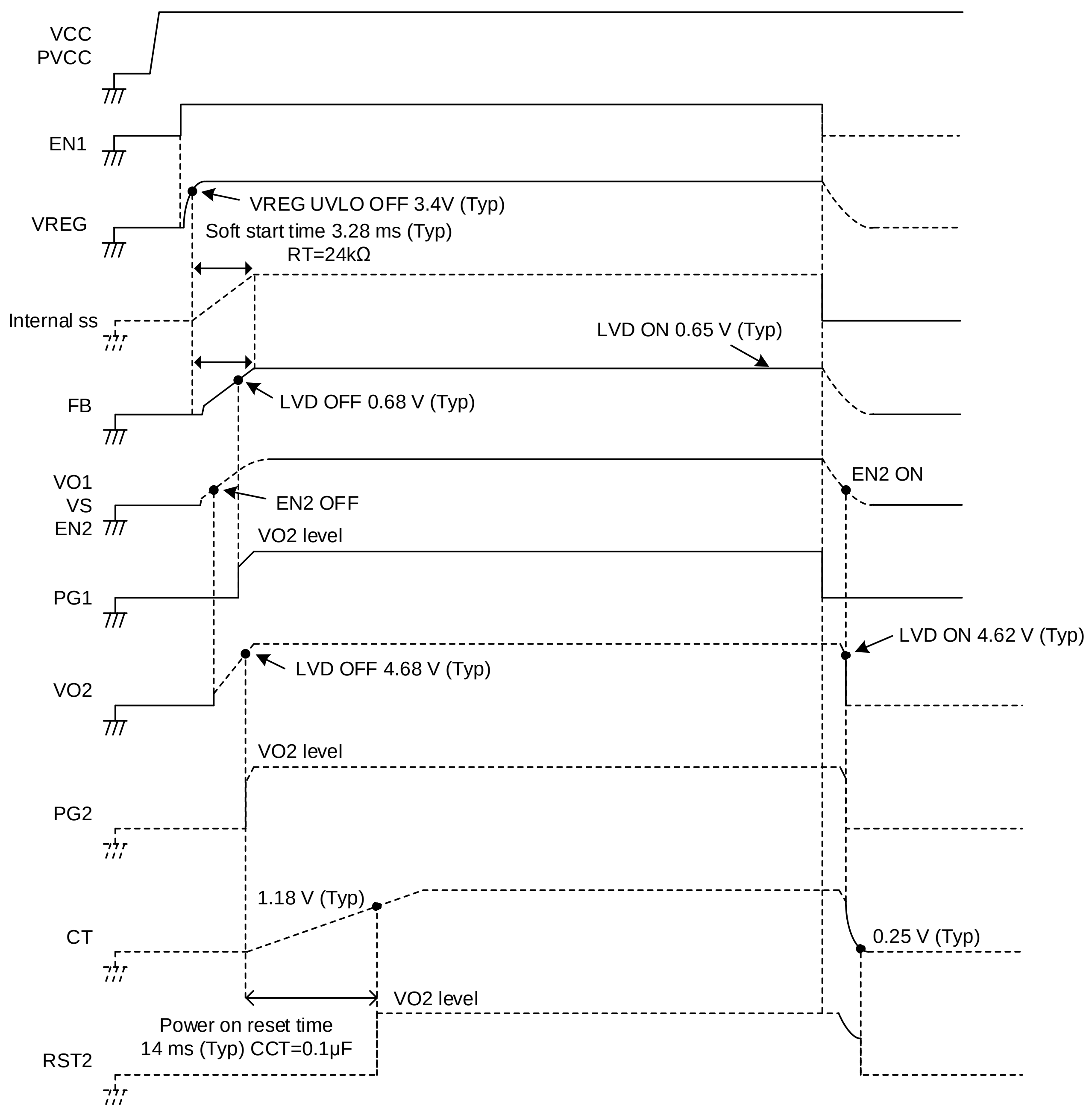
Timing Chart

1. Start up・Stop
   EN1 short to VCC, EN2 short to VS, VOUT = 6 V, load from VO2 is 400 mA.

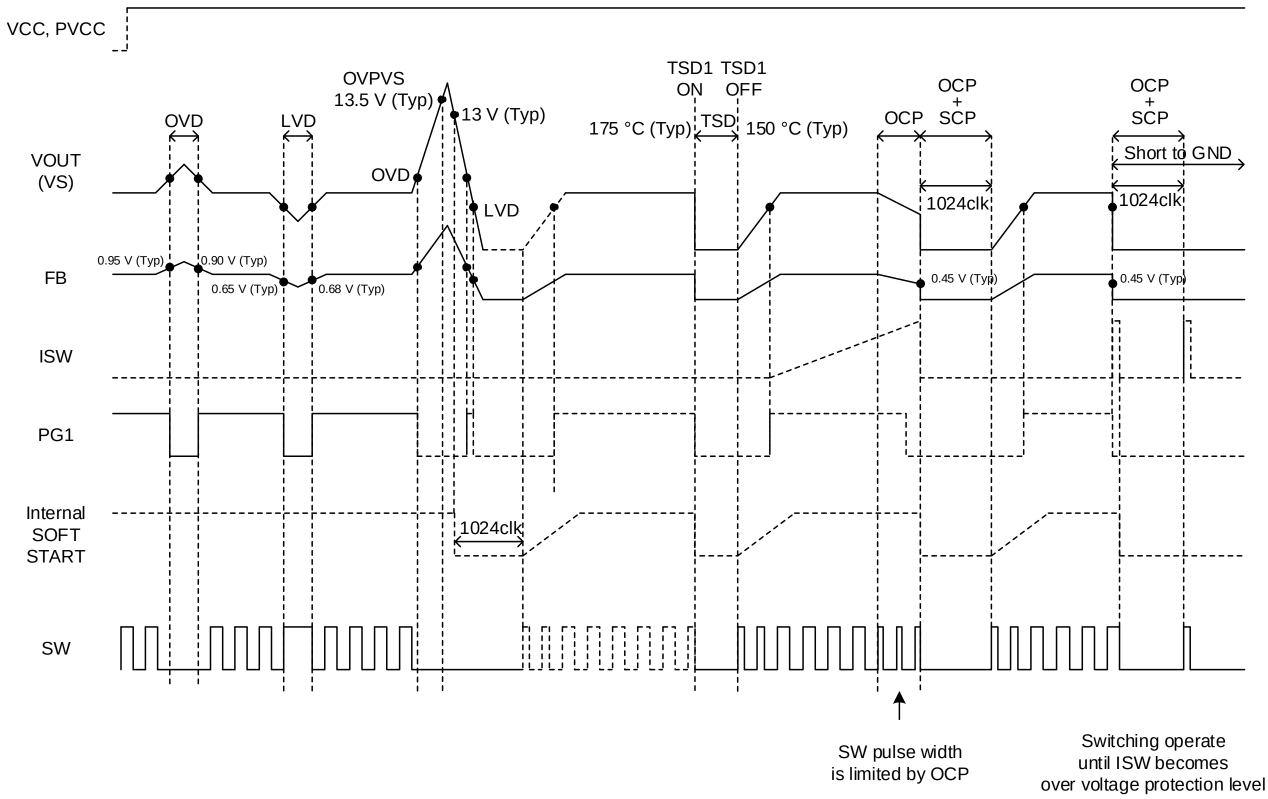


2. Start up・Stop

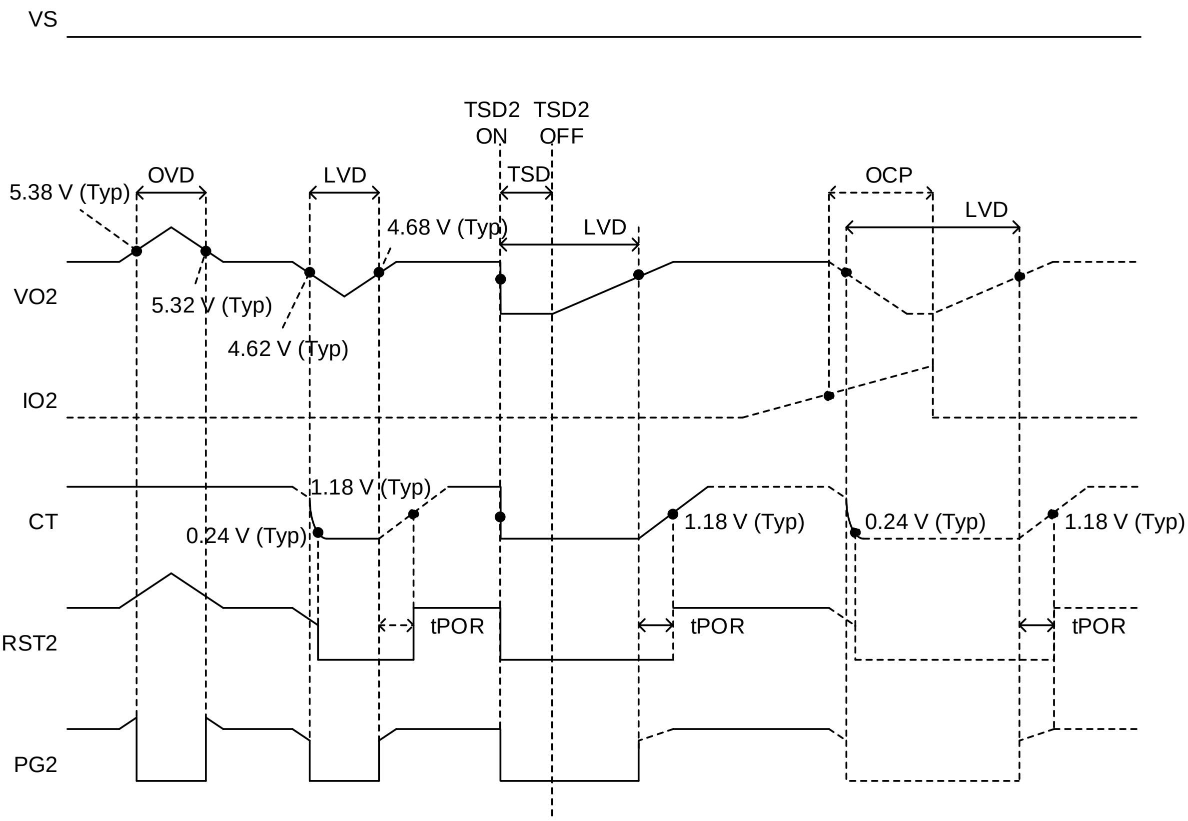
EN1 is controlled, EN2 short to VS, VOUT = 6 V, load from VO2 is 400 mA after VCC starts up.



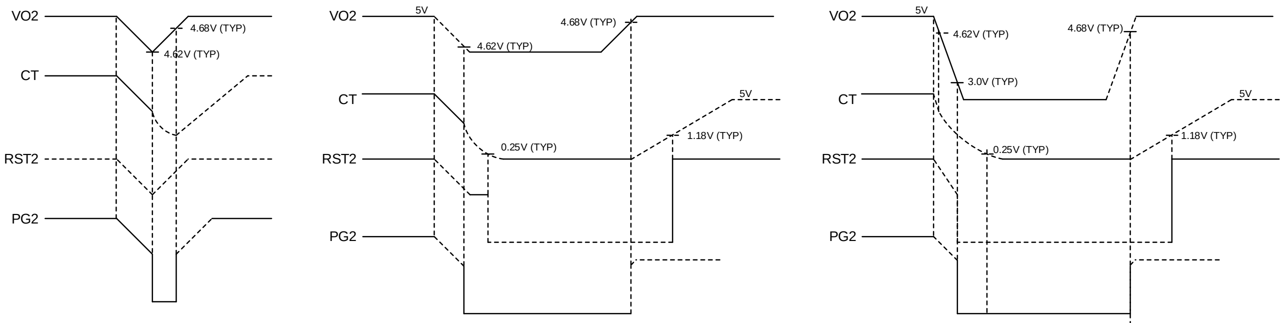
3. DCDC Converter Protection Operations



4. LDO Protection Operations (The Whole)



5. LDO Protection Operations (RESET timing)

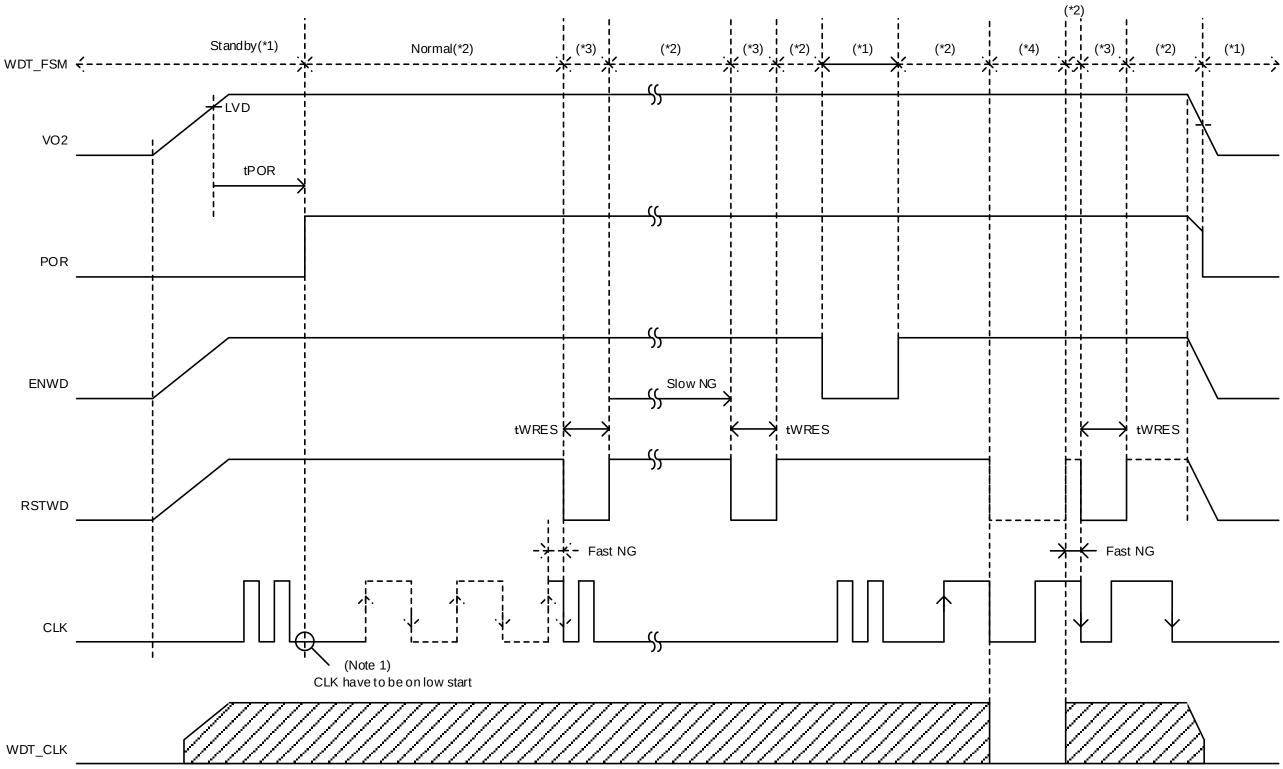


VO2 returns before RESET is detected after LVD is detected

VO2 returns after taking a pause enough after LVD is detected

When VO2 output decreases earlier than discharge time of CT

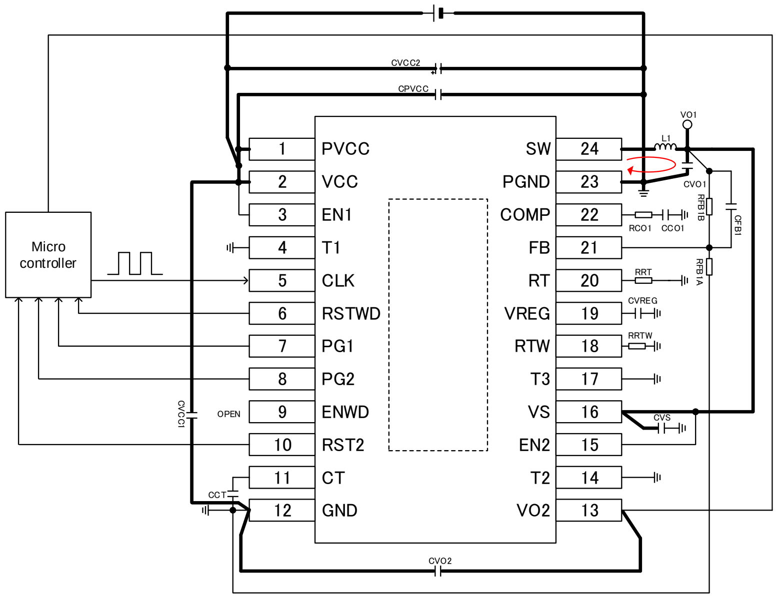
6. WDT



*1：Standby Mode, *2：Normal Mode, *3：μC ERR Detect, *4：OSC_WDT ERR Detect (See Figure 1. WDT FSM)
(Note 1) Please release power on reset in a state of CLK = LOW by all means.

Application Example

*There are many factors (Board layout, variation of the part, etc.) that can affect the characteristics.
Please verify and confirm using practical applications.
*Be sure to connect the T1, T2 and T3 pin to ground.
*In the case of high current application (About more than 500 mA from DC / DC convertor), please insert the schottky barrier diode between SW and PGND



Example of Constant Setting

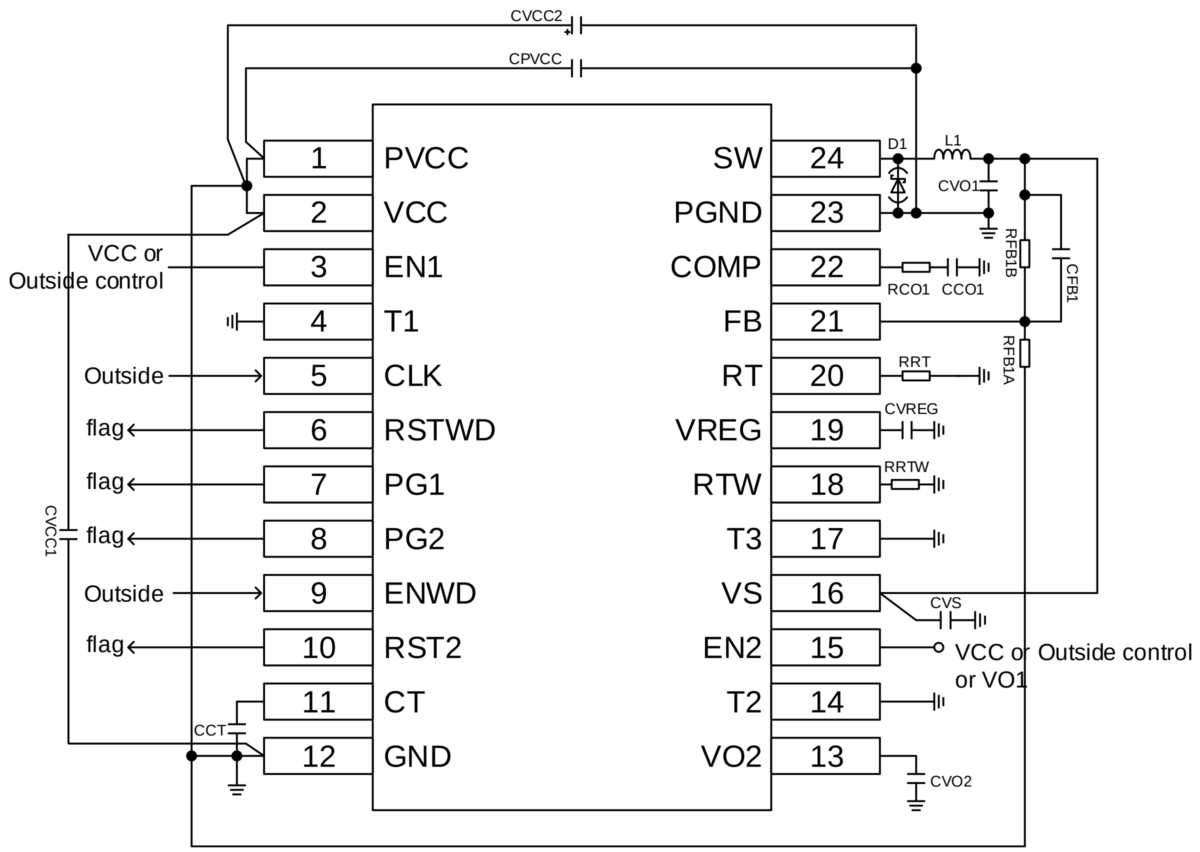
VCC = 13.5 V, VO1 = 6.5 V, fsw = 500 kHz, ILOAD (VO2) = 400 mA, fwdt = 100 kHz

name	Value	Unit	Parts No	size	manufacture
IC	-	-	BD39012EFV-C	7.8mm × 7.6mm	ROHM
L1	4.7	uH	3N1CDH74NP470KC	7.0mm × 7.0mm	SUMIDA
CVCC1	4.7	uF	GCM32ER71H475KA40L	3225	murata
CVCC2	47	uF	-	-	-
CPVCC	4.7	uF	GCM32ER71H475KA40L	3225	murata
CVO1	10 // 2	uF	GCM31CR71C106K	3216	murata
CVS	1	uF	GCM188R71C105K	1608	murata
CCT	0.1	uF	GCM188R11H104K	1608	murata
CVREG	1	uF	GCM188R71C105K	1608	murata
CFB1	100	pF	GCM1882C1H101JA01	1608	murata
CCO1	4700	pF	GCM2162C1H472JA01	1608	murata
CVO2	10	uF	GCM31CR71C106K	3216	murata
RFB1B	22	kΩ	MCR03	1608	ROHM
RFB1A	6.2 // 6.2	kΩ	MCR03	1608	ROHM
RRT	24	kΩ	MCR03	1608	ROHM
RRTW	24	kΩ	MCR03	1608	ROHM
RCO1	12	kΩ	MCR03	1608	ROHM

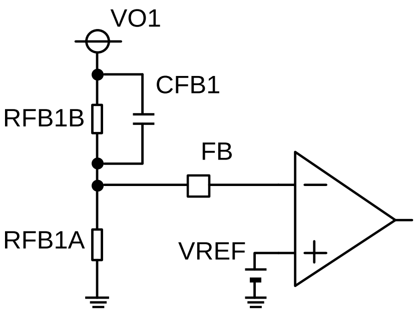
Notes for pattern layout of PCB

1. Design the wirings shown in bold line as short as possible.
2. Place the input ceramic capacitor CVCC1, CVCC2, CPVCC, CVO1, CVS and CVO2 as close to IC as possible.
3. Place RRT and RRTW in GND pin nearest IC not to receive a noise.
4. Place the RFB1A and RFB1B as close to FB pin as possible and provide the shortest wiring from FB pin. In addition, be careful not to arrange it in parallel with SW pin and high current line of L1 because it is the high Impedance line.
5. The loop of the red arrow is the line which high current line. Please layout with the shortest loop as much as possible, and wire with the 1-layer without pass the through hall.
6. Please connect to GND thermal plate of IC back.

Selection of Components Externally Connected



1) Setting the output voltage (RFB1A, RFB1B, CFB1B)
In BD39012EFV-C, VO1 voltage can be set from reference voltage 0.8 V (Typ) and the resistance division ratio of feed buck resistance RFB1A and RFB1B. Output voltage can be calculated as follow.



$$\mathrm{VO1} = 0.8 \times \left(1 + \frac{RFB1B}{RFB1A}\right) [V]$$

[Output voltage setting resistance]

Use of highly precise resistance less than ±1 % is recommended for output voltage setting. It is recommended that it is set around 1 kΩ to 100 kΩ for resistor value. The FB pin is very high impedance and easy to be affected by the noise. By all means connect resistance to nearest an IC. In addition, please layout it not to be affected by the noise of the SW pin without layout nearness. As needed, 0 point is made by assembling CFB1 beside RFB1B, and the stable ratio of the control system can be planned.
The equation of 0 points is as follows.

$$f_{zcf} = \frac{1}{2\pi \times RFB1B \times CFB1} [Hz]$$

2) Setting frequency of DC / DC convertor (RRT)
Internal oscillation frequency can be set by resistor value connecting with RT. (See Figure 37)
Settable range is 200 kHz to 600 kHz. The relations of resistor value and the oscillation frequency is decided as follow.
Because in the setting that deviated from this range, the operation is not guaranteed, please be careful.
When it is affected by the parasitism capacity of a board, it cannot be set to desired frequency.
Therefore please connect it to nearest IC and drop it to ground.

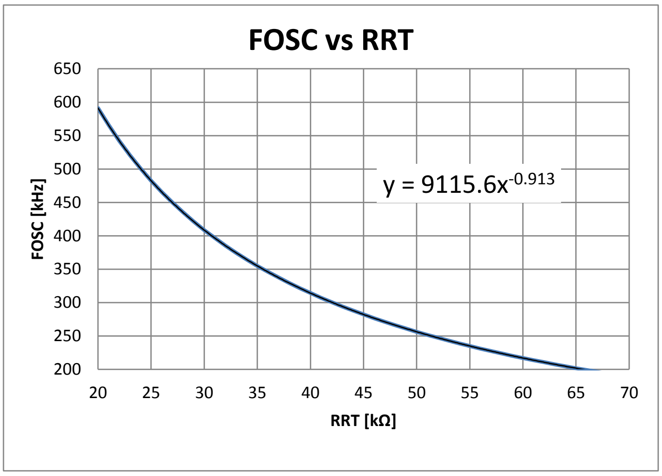


Figure 37. DC / DC oscillation frequency characteristics

3) Duty Cycle
Duty cycle of DC / DC convertor is similar to the following equation.
(Vout = output voltage, Vin = input voltage, η = efficiency)

$$D = \frac{V_{out}}{V_{in}} \times \frac{100}{\eta}\ [\%]$$

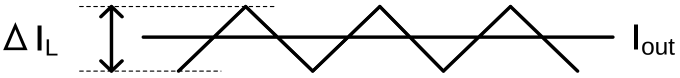
4) Selecting the inductance (L1)
The inductor value is chosen based on a duty cycle of operation frequency (fsw), load current (Iout), ripple current (ΔIL), input voltage (Vin) and output voltage (Vout). The loss of the coil becomes the total of wired resistance of a coil LDCR and loss to occur in ferrite core. It is thought that the most of the loss of coil depend on LDCR when oscillation frequency is to around 2 MHz. Please choose a small thing of LDCR because the range of set frequency of BD39012EFV-C is f = 200 kHz to 600 kHz.
When LDCR is made too much small, inductance value becomes small, and peak current value flowing at ON time grows too much big, and internal loss and power dissipation of coil grow big and efficiency turns worse. When a big inductance value is greatly set too much, LDCR grows big and efficiency in the high load turns worse. Moreover a ferrite core causes magnetic saturation and an inductance value suddenly decreases. Then there is the risk that excessive current flows in. Generally, if it is set to become the ripple current of less than 30 % of output peak loads, in most cases, stable characteristics can be got.
The aim of the smallest inductance level can be calculated by next equation.

$$\Delta I_L = 0.3 \times I_{out} [A]$$

$$L_{min} = \frac{(V_{in} - V_{out}) \times D}{\Delta I_L \times f_{sw}} [H]$$

The inductance value chosen here is one of the indexes insistently.
Please confirm whether peak current can meet the direct current weight characteristics of the inductor enough.
The equation of peak current (Ipeak) is as follows.

$$I_{peak} = I_{out} + \frac{1}{2} \Delta I_L [A]$$



Inductor current waveform

5) Selecting the input capacitor (CVCC1, CPVCC)
Input capacitors reduce the power output impedance that is connected to VCC and PVCC. It is recommended that electrolytic capacitor such as CVCC2 is inserted in the case of the PCB layout which power supply impedance grows big. Please use the capacitor that impedance is low and an implementation area is small (more than at least 2 μF) for the bypass capacitor connected to nearest IC.
The ripple current limit of input capacitor is approached by the following equation.
It is recommended that ceramic capacitor with enough limit current is used.

$$I_{CVCC,CPVCC} \approx I_{out} * \sqrt{D \times (1-D)} [A_{rms}]$$

Minimum input capacity is approached by the following equation based on the input ripple voltage of the aim.
Input capacitor ESR (Cesr)

$$C_{CVCC,CPVCC} \geq \frac{I_{out} \times D \times (1-D)}{\left(\Delta V_{in} - \left(I_{out} + \frac{\Delta I_L}{2}\right) \times C_{esr}\right) \times f_{sw}} [F]$$

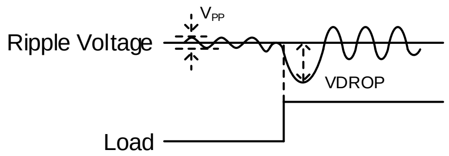
6) Setting of the internal REG input capacitor (CVREG)
Please insert ceramic capacitor of 1μF in nearest VREG pin of internal reference power supply.

7) Setting of the output capacitor (CVO1)
The output capacitor CVO1 has an important role in output ripple voltage, load-responsive and stability of the loop. The output voltage ripple is generally set in less than 1 % of the output voltage and approached by the following equation. (ESR of CVO1 = R_{CVO1})

$$\Delta V_{out} = \Delta I_L \times \left(R_{CVO1} + \frac{1}{8 \times f_{sw} \times C_{VO1}}\right) [V]$$

An output capacitor significantly influences the output voltage change in the load fluctuation. The quantity of change depends on many factors including capacity, parasitism ESR, parasitism inductor phase characteristics and through rate of load. Please use it after confirmation with an actual product enough.
When phase characteristics are enough, the quantity of drop VDROP of the output voltage by the load fluctuation can be approached by following equation. A figure of image is shown as follows.

$$V_{DROP} = I_{pulse} \times C_{VO1esr} + \frac{L \times {I_{pulse}}^2}{C_{VO1} \times (V_{in} - V_{out})} [V]$$

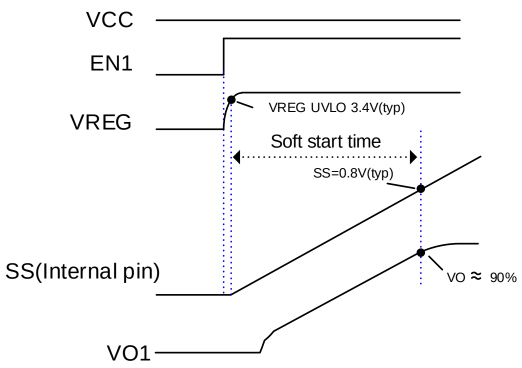


Please use an input capacitor and the output capacitor after considering DC voltage characteristics and temperature characteristics enough. When a ceramic capacitor is used, the capacity comes under a big influence of an applied voltage and temperature, and capacity suddenly decreases. Please consider characteristics enough, and it is necessary to choose the product superior in temperature characteristics such as B characteristics or X7R characteristics. When aluminum electrolytic capacitor is used, large-capacity is got in small size. But it is necessary to inspect temperature characteristics of ESR and the capacity enough because capacity and ESR suddenly change by a temperature change. The capacitor 1.5 times to 2 times larger than a limit is recommended about the pressure-resistant.

8) Setting of the schottky barrier diode of SW pin (D1)
When big load current is pulled, SW pin waggles lower than ground while SW pin is L because BD39012EFV-C is DC / DC convertor of the synchronous rectification system.
Please insert schottky barrier diode between SW and PGND to prevent the IC from malfunctioning by this.
In the case of the setting that load current of DC / DC convertor (Iout) exceeds 500 mA, it is recommended that it is inserted.

9) Setting the soft start time
Soft start is a function to reduce rush current and over shoot. Soft start time of BD39012EFV-C is decided by the oscillation frequency of DC / DC convertor.
When EN1 is released, VREG start up after internal circuit delay operation.
SS pin is counted up when VREG arrives at 3.4 V (Typ). Output voltage VO1 starts up to approximately 90 % when SS pin starts up to 0.8 V.

The time from internal SS pin begins to start up to arrive at 0.8 V can be calculated by the equation as below.



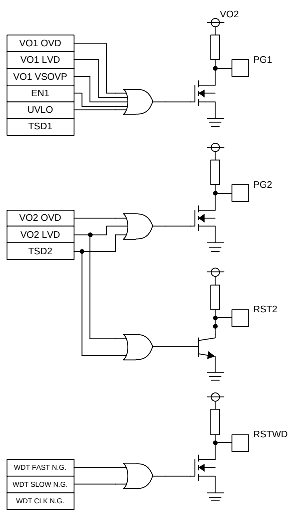
$$Soft\ start\ time = 1638.4 \times \frac{1}{f_{sw}}\ [ms]$$

10) Setting CT pin (CCT)
Power on reset time is decided freely by adding capacitor between CT pin and ground.
As the value of CCT becomes big, power on reset time becomes long. Standard power on reset time corresponded to the list of CCT capacitors is shown below. Please connect to ground nearest the IC not to do wrong operation by noise.

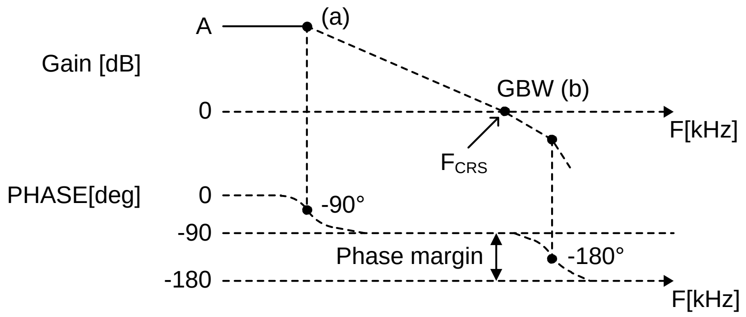
CCT (μF)	Power ON RESET TIME [ms]
10	1400
4.7	658
1	140
0.47	65.8
0.1	14
0.047(Note1)	6.58
0.01(Note1)	1.4
0.0047(Note1)	0.658
0.001(Note1)	0.14

(Note1) Setting time ±100 μs

11) Setting the PG1, PG2, RST2 and RSTWD pin
PG1, PG2, RST2 and RSTWD are the open drain pin that is pulled up inside by VO2 output. When each abnormality is detected each becomes L output. When it come back normally, each becomes H (VO2 output) output.
All these 4 pins can be connected and used to OR output. Logic image by each protection is shown below.



12) Setting the phase compensation circuit (DC / DC Converter)
DC / DC is current mode control and is 2-pole and 1-zero system. It has two poles formed by error amp and output load and one zero added by phase compensation. The appropriate pole point and zero point placement results in good transient response and stability. Generic Bode plot of DC / DC converters is shown below. At point (a), gain starts falling due to the pole formed by output impedance of error amp and C_{CO1} capacitance. After that, in order to cancel out the pole formed by output load, insert zero formed by R_{CO1} and C_{CO1} and offset the fluctuation of gain and phase before reaching out to point (b).



Phase margin level

External component values are determined in this way. The R_{CO1} determines the cross over frequency F_{CRS}, i.e., the frequency at which DC / DC total gain falls down to 0 dB. When F_{CRS} is set high, good transient response is expected but stability is sacrificed on the other hand. When F_{CRS} is set low, good stability is expected but transient response is sacrificed on the other hand.
In this example, component value is set in a way F_{CRS} is 1 / 5 to 1 / 10 of the switching frequency.

(i) R_{CO1} for Phase compensation
Phase compensation resistor R_{CO1} can be obtained by the following equation.

$$R_{CO1} = \frac{2\pi \times V_{O1} \times F_{CRS} \times C_{VO1}}{0.8 \times G_{NP} \times G_{MA}}\ [\Omega]$$

Where：
V_{O1}: $Output\ voltage$
F_{CRS}: $Cross\ over\ frequency$
C_{O1}: $Output\ capacitor, feedbuck\ reference\ voltage\ (0.8V\ (Typ))$
G_{MP}: $Current\ sense\ gain\ (0.2\ A\ /\ V\ (Typ))$
G_{MA}: $Error\ amp\ trance\ conductance\ (300uA\ /\ V\ (Typ))$

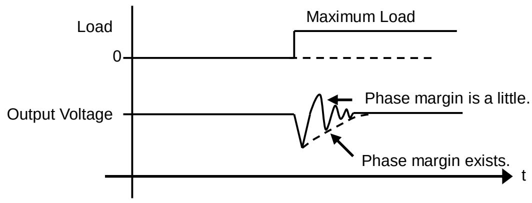
(ii) C_{CO1} for Phase compensation
Phase compensation capacitor C_{CO1} can be obtained by the following equation.

$$C_{CO1} = \frac{V_{O1} \times C_{VO1}}{I_{out} \times R_{CO1}}\ [F]$$

Where：
I_{Out}: $Output\ load$

However these are simple equation and thus adjustment of the value using the actual product may be necessary for optimization. Also compensation characteristics are influenced by PCB layout and load conditions and thus thorough evaluation using the production intent unit is recommended.

13) Setting the phase compensation circuit
It is suitable that the starting point of the phase compensation is set by the following condition equation. Please make a board wire diagram, and confirm whether frequency characteristic to aim for is satisfied. Actually, the characteristics greatly change by layout of PCB, taking wiring around, kind of used parts or terms of use (temperature etc.).
For example, it might resonate after LC resonance point moves by capacity decrease at the low temperature and increase of the ESR when electrolytic capacitor is used for an output capacitor.
To a capacitor for the phase compensation, using such as temperature compensation types is recommended.
Please confirm stability and responsiveness with practical application by all means.
The frequency characteristic with the practical application is confirmed using gain phase analyzer and FRA.
Please refer to each measuring instrument manufacturer for the methods of the measurement. In addition, when there are not these measuring instruments, there is a method to guess margin degree by load reply.
It is said that responsiveness is low when there is much quantity of change, and there are few phase margin when there is much number of ringing times after the change in the case of monitoring change of the output when it was made to fluctuate from a no load state to a peak load.
The aim is ringing more than twice. But the quantitative phase margin level cannot be confirmed.

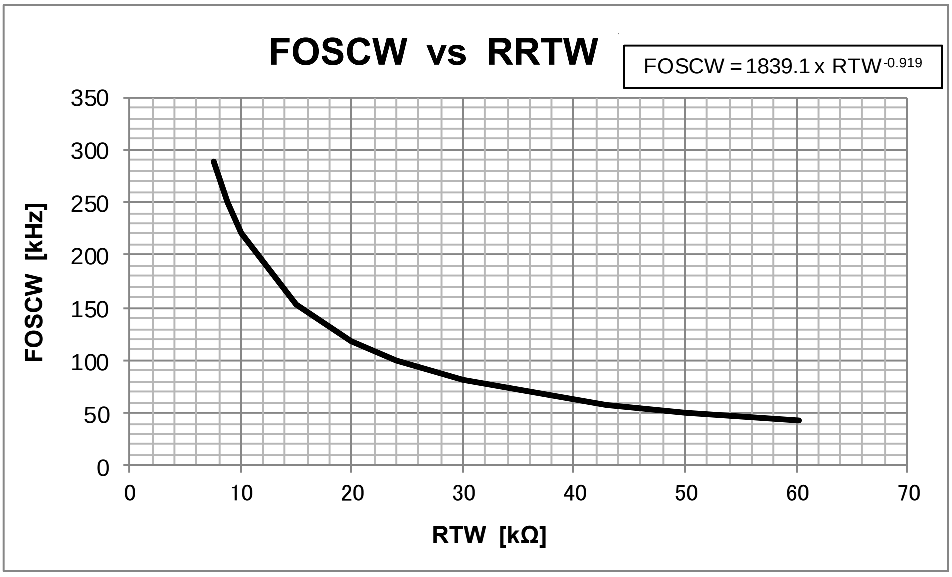


14) Setting the LDO output capacitor (CVO2)
The capacitor must be added between output pin and GND in order to stop from having it oscillated. Please ensure to select the Capacitor higher than 6 µF in the range of voltage and temperature. Please confirm in the last state to use because it changes by wiring impedance of the board, input power supply and load actually.
When selecting a ceramic capacitor, B characteristics or X7R higher is recommended which is good in temperature characteristic and has excellent DC bias characteristic.
Please do final decision of the capacitance after confirming it by practical application enough.

15) Setting the LDO input capacitor (CVS)
Please add the capacitor more than 0.1 µF between VS and GND. Because the capacitance setting varies according to application, confirm and design it with a margin. Capacitors that have good voltage and temperature characteristics are recommended. Do not use it together with CVO1, please insert in the place nearest VS by all means.

16) Oscillator for watch dog timer Setting the frequency (RRTW)
Internal oscillation frequency can be set by resistor value connecting with RTW.
The settable range is 50 kHz to 250 kHz. The relations of resistor value and oscillation frequency is decided like the below figure.

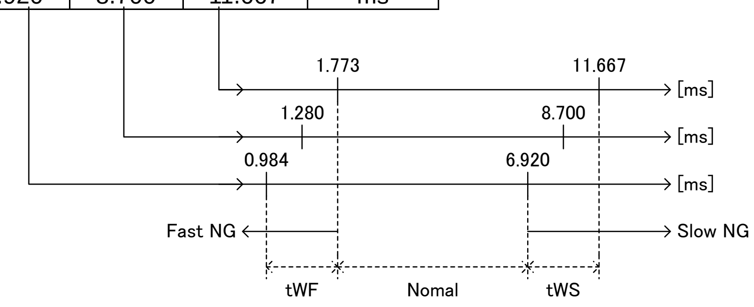
Oscillator for watch dog timer Setting the frequency (FOSCW vs. RTW)



1. Example of WDT setting method

In the case of RTW = 24 kΩ, CLK edge width becomes 1.773 ms to 6.920 ms when it is normal.

Symbol	Min	Typ	Max	Unit
FOSCW	75	100	125	kHz
tWT	0.984	1.280	1.773	ms
tWS	6.920	8.700	11.667	ms



Watch dog setting method

17) ENWD Pin
This pin validates the WDT function. Usually pulled up inside by VO2 pin, the WDT function becomes effective.
To invalidate the WDT function, please short ENWD pin to ground.
Then RSTWD pin always becomes H (VO2 output).

18) RSTWD Pin
H (VO2 output) is usually shown when the normal operating.
The output is changed from H to L when the abnormality is detected in WDT.

19) CLK Pin
Clock input pin for WDT. Please input the signal from a microcomputer depending on WDT set frequency.
Please release power on reset in a state of CLK = LOW by all means.

20) T1, T2, T3 Test Pin
Be sure to connect to GND.

21) EN1, EN2 Pin
Please control EN1 from VCC or microcomputer, and EN2 from VCC or VO1 or microcomputer.

Power Dissipation

Maximum Junction Temperature Tj is 150 °C. If the junction temperature reaches 175 °C or higher, the circuit will be shut down. Please make sure that the junction temperature must not exceed 150C at all time.

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. Ambient temperature Ta is less than 125 °C.
2. Tj is less than 150 °C.

Temperature Tj can be calculated by two ways as below.

1. To obtain Tj from the IC surface temperature Tc in actual use

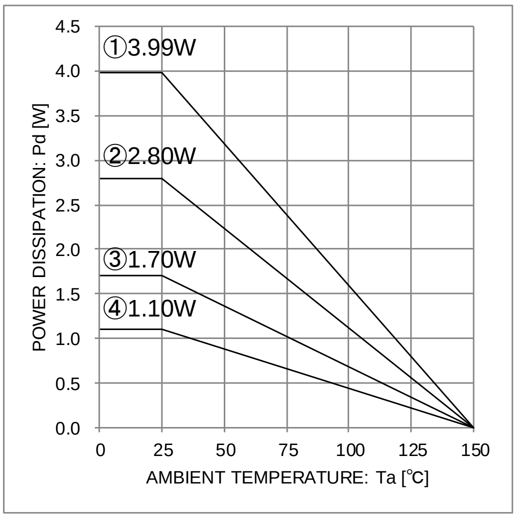
$$Tj = TC + \theta jc \times P_{TOTAL}$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta ja \times P_{TOTAL}$$

Thermal resistance value θja is varied by the number of the layer and copper foil area of the PCB.
See Figure 38 for the thermal design.

Thermal Derating Characteristics

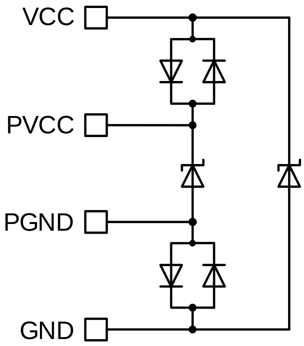
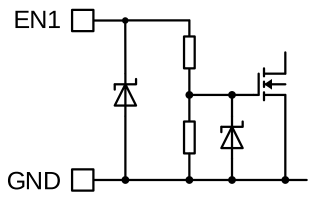
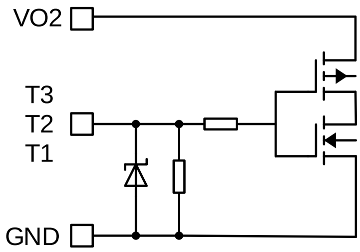
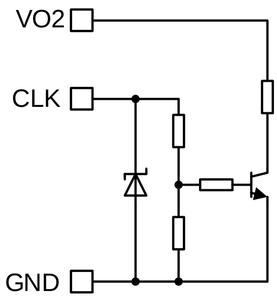
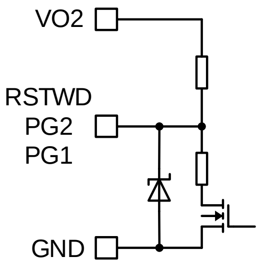
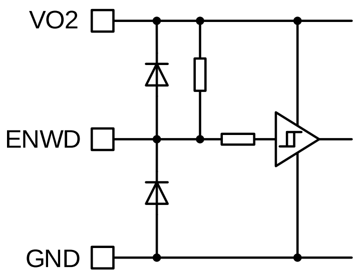
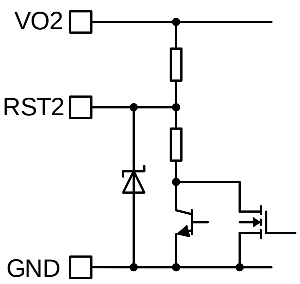
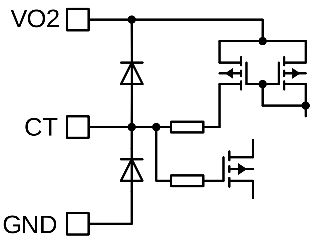
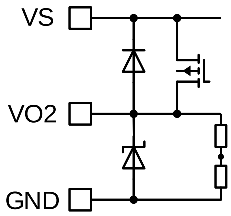


IC mounted on ROHM standard board
・Board size: 70 mm × 70 mm × 1.6 mm
・Board size: 15 mm × 15 mm × 1.6 mm
・PCB and back metal are connected by soldering

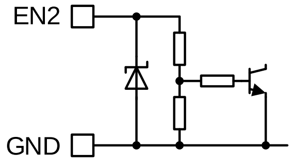
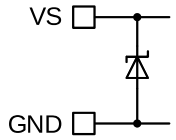
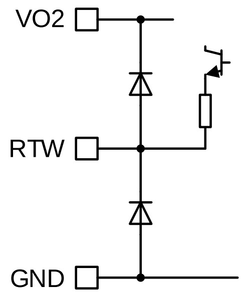
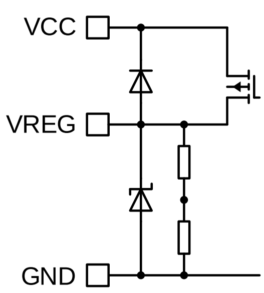
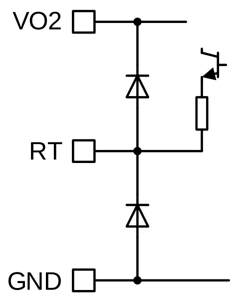
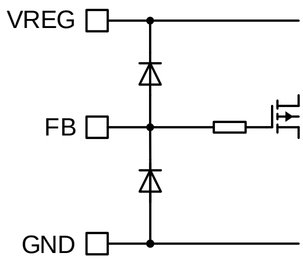
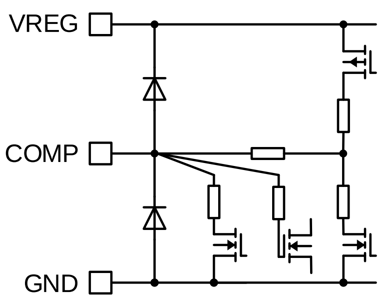
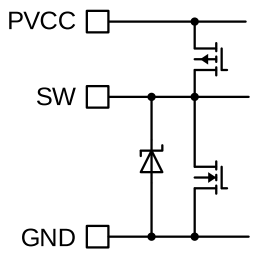
① : 4-layer board 70 × 70 × 1.6mmt
② : 2-layer board 70 × 70 × 1.6mmt
③ : 2-layer board 15 × 15 × 1.6mmt
④ : Single IC

Figure 38. Package data of HTSSOP-B24 (Reference data)

I / O equivalent circuits

1.PVCC, 2.VCC	3.EN1	4.T1, 14.T2, 17.T3
		
5.CLK	6.RSTWD, 7.PG1, 8.PG2	9.ENWD
		
10.RST2	11.CT	13.VO2
		

I / O equivalent circuits - Continued

15.EN2	16.VS	18.RTW
		
19.VREG	20.RT	21.FB
		
22.COMP	24.SW	
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
   When the application pulls load current more than 500 mA from DC / DC convertor, be sure to connect to the schottky barrier diode between SW and PGND.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

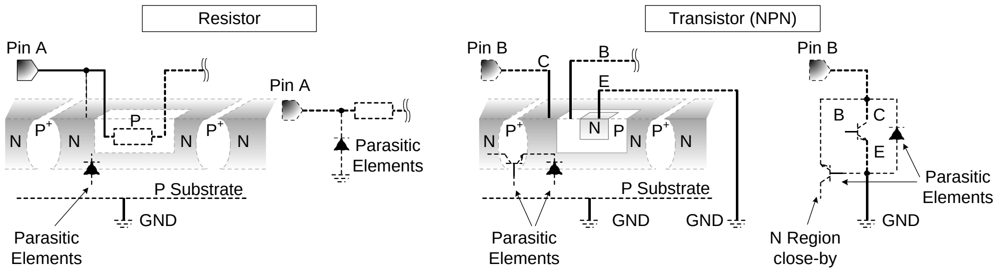
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

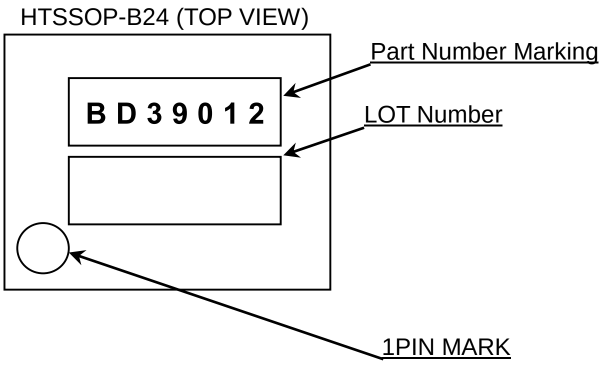
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B D 3 9 0 1 2 E F V - CE 2

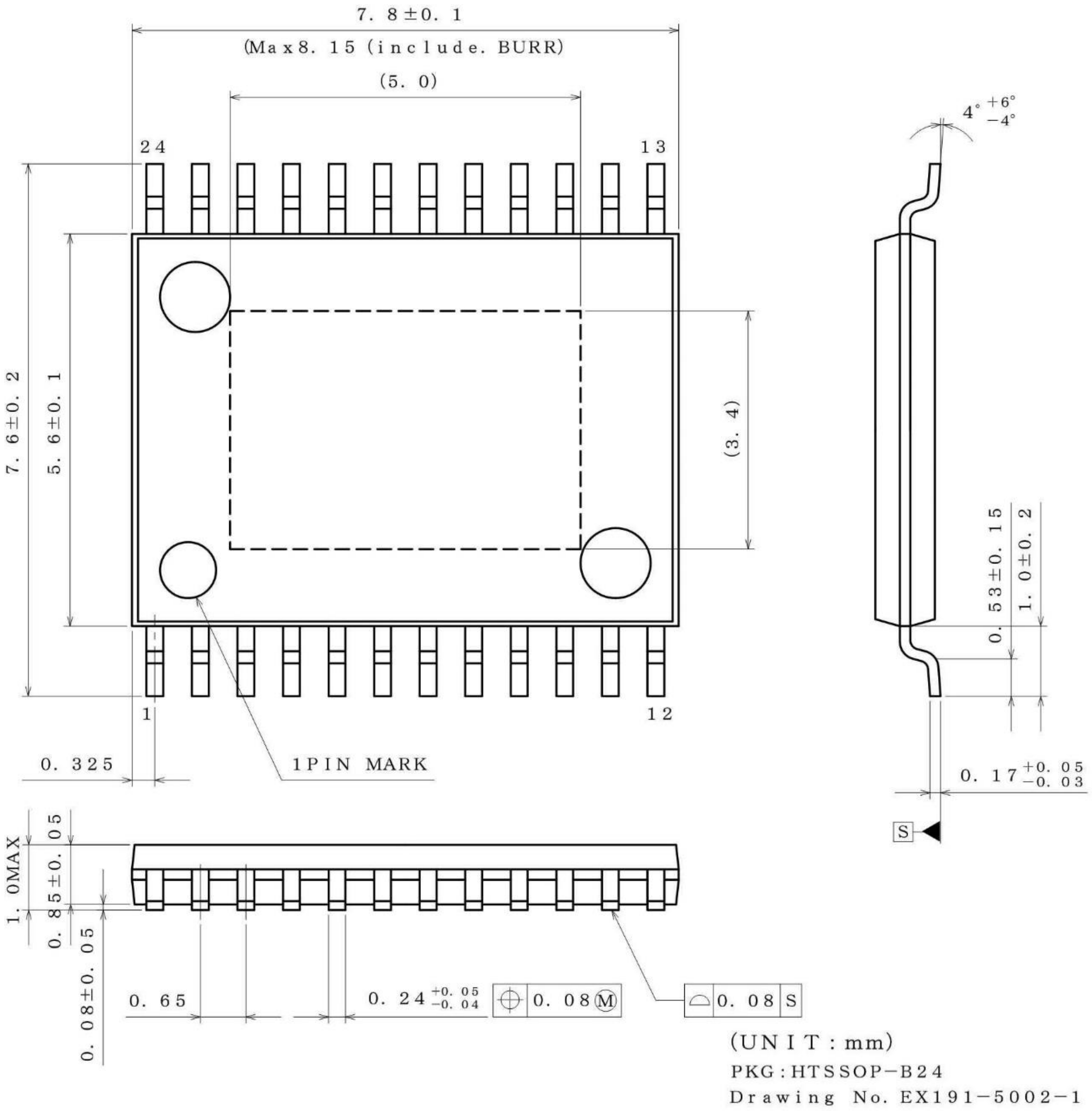
- Part Number
- Package
  EFV: HTSSOP-B24
- Packaging and forming specification
  C: For in-vehicle
  E2: Embossed tape and reel
  (HTSSOP-B24)

Marking Diagrams



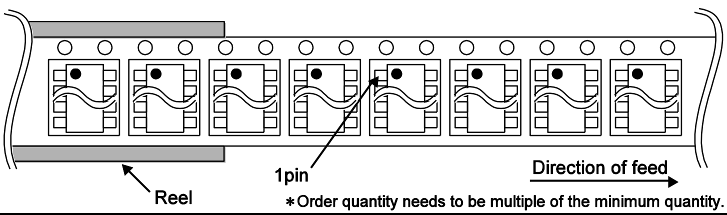
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
11.Sep.2014	002	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

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2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.