

# 2.7 V to 5.5 V Input, 2 A Single Synchronous Buck DC/DC Converter for Automotive

## BD9S209NUX-C

### General Description

BD9S209NUX-C is a synchronous buck DC/DC Converter with built-in low On Resistance power MOSFETs. It is capable of providing current up to 2 A. Small inductor is applicable due to high switching frequency of 2.2 MHz. It is a current mode control DC/DC Converter and features high-speed transient response. It has a built-in phase compensation circuit. Applications can be created with a few external components.

### Features

- AEC-Q100 Qualified<sup>(Note 1)</sup>
- Single Synchronous Buck DC/DC Converter
- Adjustable Soft Start Function
- Output Discharge Function
- Power Good Output
- Input Under Voltage Lockout Protection (UVLO)
- Short Circuit Protection (SCP)
- Output Over Voltage Protection (OVP)
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)

(Note 1) Grade 1

### Applications

- Automotive Equipment
- Other Electronic Equipment

### Key Specifications

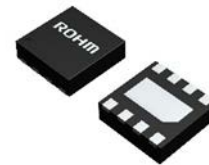
- Input Voltage: 2.7 V to 5.5 V
- Output Voltage Setting: 0.8 V to  $V_{IN}$
- Output Current: 2 A (Max)
- Switching Frequency: 2.2 MHz (Typ)
- High Side FET ON Resistance: 150 m $\Omega$  (Typ)
- Low Side FET ON Resistance: 95 m $\Omega$  (Typ)
- Shutdown Circuit Current: 0  $\mu$ A (Typ)
- Operating Temperature: -40 °C to +125 °C

### Package

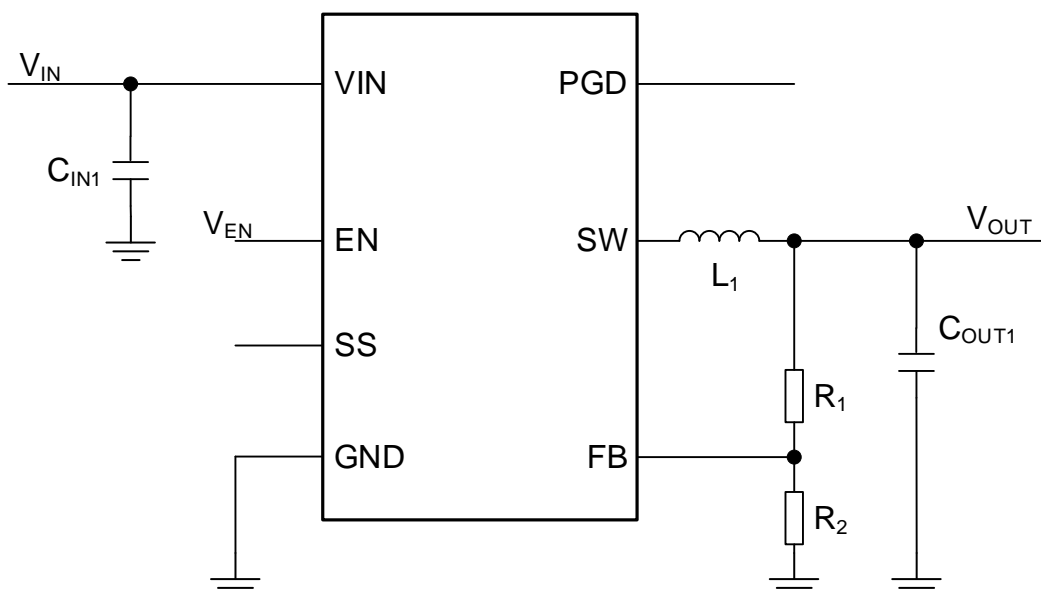
VSON008X2020

W (Typ) x D (Typ) x H (Max)

2.0 mm x 2.0 mm x 0.6 mm



### Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

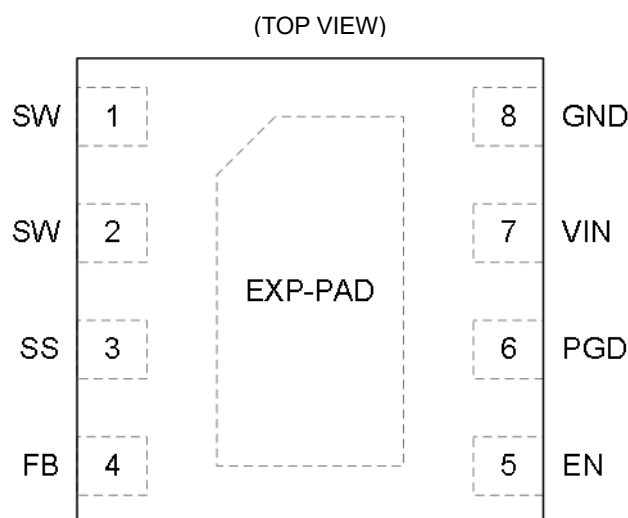
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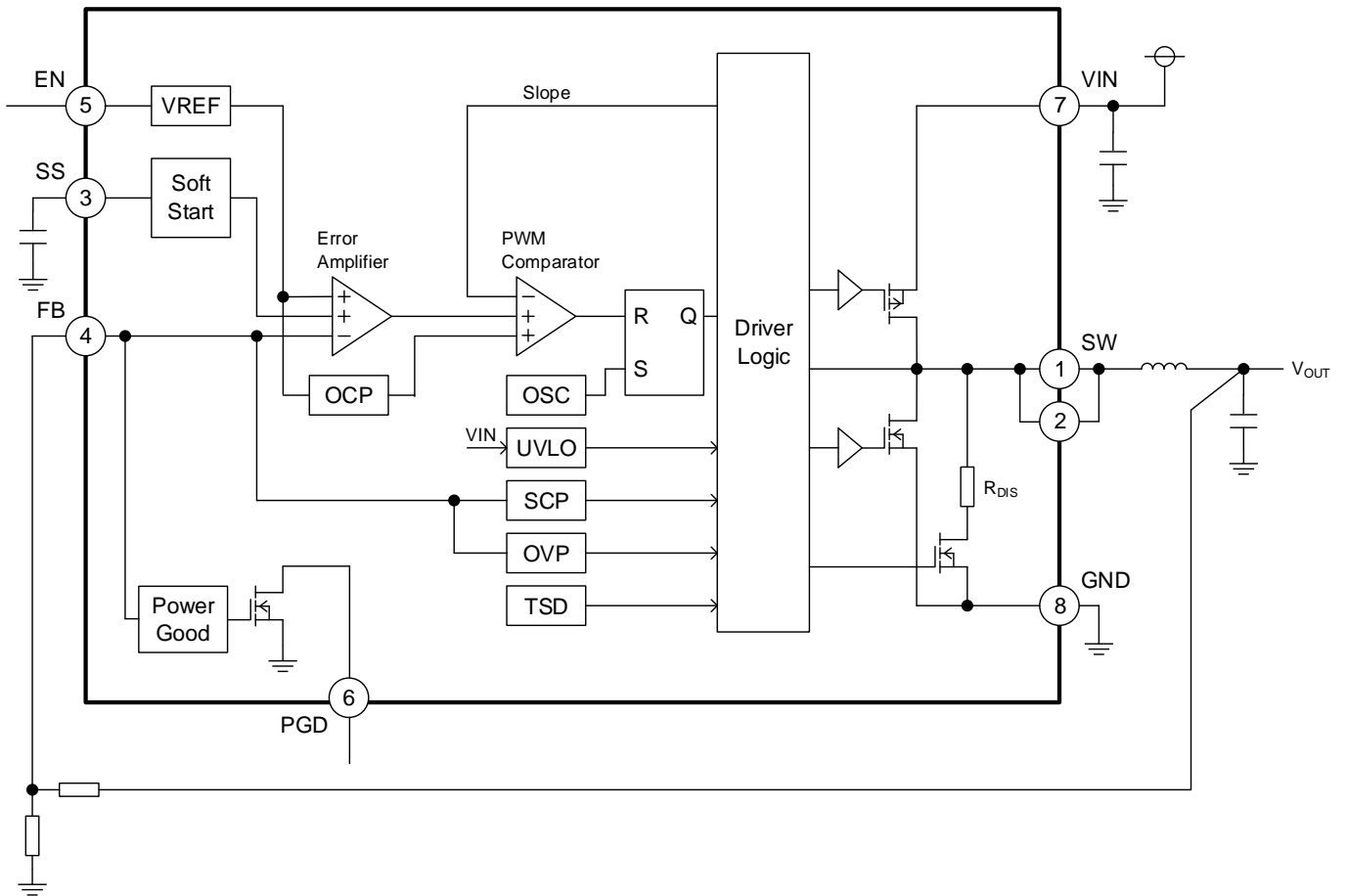
## Pin Configuration



## Pin Descriptions

Pin No.	Pin Name	Function
1, 2	SW	Switch pin. These pins are connected to the drain of the High Side FET and the Low Side FET.
3	SS	Pin for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this pin. See <a href="#">Selection of Components Externally Connected 5. Selection of Soft Start Capacitor</a> for how to calculate the capacitance.
4	FB	$V_{OUT}$ feedback pin. Connect output voltage divider to this pin to set the output voltage. See <a href="#">Selection of Components Externally Connected 2. Selection of Output Voltage Setting</a> on how to compute for the resistor values.
5	EN	Enable pin of the device. Turning this pin Low forces the device to enter the shutdown mode. Turning this pin High makes the device to start up.
6	PGD	Power Good pin, an open drain output. It is need to be pulled up to the power supply with a resistor. See <a href="#">Function Explanations 2. Power Good Output</a> for setting the resistance.
7	VIN	Power supply pin. Connecting a 10 $\mu$ F (Typ) ceramic capacitor is recommended. The detail of a selection is described in <a href="#">Selection of Components Externally Connected 3. Selection of Input Capacitor</a> .
8	GND	Ground pin.
-	EXP-PAD	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using via provides excellent heat dissipation characteristics.

Block Diagram



## Description of Blocks

- VREF**  
The VREF block generates the internal reference voltage.
- UVLO (Under Voltage Lockout)**  
The UVLO block is for under voltage lockout protection. It shuts down the device when the  $V_{IN}$  falls to 2.45 V (Typ) or less. The threshold voltage has a hysteresis of 100 mV (Typ).
- SCP (Short Circuit Protection)**  
This is the short circuit protection circuit. After soft start is judged to be completed, if the FB pin voltage falls to 0.56 V (Typ) or less and remain in that state for 1 ms (Typ), output MOSFETs turn OFF for 14 ms (Typ) and then restart the operation.
- OVP (Over Voltage Protection)**  
This is the output over voltage protection circuit. When the FB pin voltage becomes 0.88 V (Typ) or more, it turns the output MOSFETs OFF. After output voltage falls 0.856 V (Typ) or less, the output MOSFETs return to normal operation.
- TSD (Thermal Shutdown)**  
This is the thermal shutdown circuit. It shuts down the device when the junction temperature ( $T_j$ ) reaches to 175 °C (Typ) or more. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation with hysteresis of 25 °C (Typ).
- OCP (Over Current Protection)**  
The Over Current Protection function operates by limiting the current that flows through High Side FET at each cycle of the switching frequency.
- Soft Start**  
The Soft Start circuit slows down the rise of output voltage during startup, which allows the prevention of output voltage overshoot. The soft start time of the output voltage can be specified by connecting a capacitor to the SS pin. See [Selection of Components Externally Connected 5. Selection of Soft Start Capacitor](#) for how to calculate the capacitance. A built-in soft start function is provided the soft start with Soft Start Time  $t_{ss}$  ([Electrical Characteristics](#)) when the SS pin is open.
- Error Amplifier**  
The Error Amplifier block is an error amplifier and its inputs are the reference voltage and the FB pin voltage.
- PWM Comparator**  
The PWM Comparator block compares the output voltage of the Error Amplifier and the Slope signal to determine the output switching pulse duty.
- OSC (Oscillator)**  
This block generates the oscillating frequency.
- Driver Logic**  
This block controls switching operation and various protection functions.
- Power Good**  
When the FB pin voltage reaches 0.8 V (Typ) within  $\pm 7\%$ , the built-in Nch MOSFET turns OFF and the PGD output turns high. There is a 3 % hysteresis on the threshold voltage, so the PGD output turns low when the FB pin voltage reaches outside  $\pm 10\%$  of 0.8 V (Typ).

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	$V_{IN}$	-0.3 to +7.0	V
EN Voltage	$V_{EN}$	-0.3 to $V_{IN}$	V
PGD Voltage	$V_{PGD}$	-0.3 to +7.0	V
FB, SS Voltage	$V_{FB}, V_{SS}$	-0.3 to $V_{IN}$	V
Maximum Junction Temperature	$T_{jmax}$	150	°C
Storage Temperature Range	$T_{stg}$	-55 to +150	°C

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance<sup>(Note 1)</sup>

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	
VSON008X2020				
Junction to Ambient	$\theta_{JA}$	181.90	47.90	°C/W
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	$\Psi_{JT}$	20.00	7.00	°C/W

(Note 1) Based on JESD51-2A(Still-Air), using a BD9S209NUX-C Chip.

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 $\mu$ m

Layer Number of Measurement Board	Material	Board Size	Thermal Via <sup>(Note 5)</sup>	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	$\Phi$ 0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 $\mu$ m	74.2 mm x 74.2 mm	35 $\mu$ m	74.2 mm x 74.2 mm	70 $\mu$ m

(Note 5) This thermal via connect with the copper pattern of layers 1, 2, and 4. The placement and dimensions obey a land pattern.

## Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Voltage	$V_{IN}$	2.7	5.5	V
Operating Temperature	$T_a$	-40	+125	°C
Output Current	$I_{OUT}$	-	2	A
Output Voltage Setting	$V_{OUT}$	0.8 <sup>(Note 1)</sup>	$V_{IN}$	V
SW Minimum ON Time	$t_{ON\_MIN}$	-	80	ns

(Note 1) Although the output voltage is configurable at 0.8 V and higher, it may be limited by the SW min ON pulse width. For the configurable range, refer to [2. Selection of Output Voltage Setting](#) in Selection of Components Externally Connected.

Electrical Characteristics (Unless otherwise specified Ta = Tj = -40 °C to +125 °C, V<sub>IN</sub> = 5.0 V, V<sub>EN</sub> = 5.0 V, the typical value is defined at Ta = Tj = +25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
<b>VIN</b>						
Shutdown Circuit Current	I <sub>SDN</sub>	-	0	10	μA	V <sub>EN</sub> = 0 V, Ta = 25 °C
Circuit Current	I <sub>CC</sub>	250	400	550	μA	I <sub>OUT</sub> = 0 mA Non-switching, Ta = 25 °C
UVLO Detection Voltage	V <sub>UVLO1</sub>	2.30	2.45	2.60	V	V <sub>IN</sub> Falling
UVLO Release Voltage	V <sub>UVLO2</sub>	2.40	2.55	2.70	V	V <sub>IN</sub> Rising
UVLO Hysteresis Voltage	V <sub>UVLO-HYS</sub>	50	100	125	mV	
<b>ENABLE</b>						
EN Input Voltage High	V <sub>ENH</sub>	1.0	-	V <sub>IN</sub>	V	
EN Input Voltage Low	V <sub>ENL</sub>	GND	-	0.4	V	
EN Input Current	I <sub>EN</sub>	2.0	5.0	8.0	μA	V <sub>EN</sub> = 5.0 V, Ta = 25 °C
<b>Reference Voltage</b>						
FB Pin Voltage	V <sub>FB</sub>	0.788	0.800	0.812	V	(Note 1)
FB Input Current	I <sub>FB</sub>	-	0	0.2	μA	V <sub>FB</sub> = 0.8 V, Ta = 25 °C
<b>Soft Start</b>						
Soft Start Time	t <sub>SS</sub>	0.5	1.0	2.0	ms	V <sub>IN</sub> = 5.0 V, The SS Pin OPEN
		0.6	1.2	2.4	ms	V <sub>IN</sub> = 3.3 V, The SS Pin OPEN
SS Charge Current	I <sub>SS</sub>	-1.4	-1.0	-0.6	μA	
<b>Switching Frequency</b>						
Switching Frequency	f <sub>SW</sub>	2.0	2.2	2.4	MHz	
<b>Power Good</b>						
PGD Falling (Fault) Voltage	V <sub>PGDTH_FF</sub>	V <sub>FB</sub> x 0.87	V <sub>FB</sub> x 0.90	V <sub>FB</sub> x 0.93	V	V <sub>FB</sub> Falling
PGD Rising (Good) Voltage	V <sub>PGDTH_RG</sub>	V <sub>FB</sub> x 0.90	V <sub>FB</sub> x 0.93	V <sub>FB</sub> x 0.96	V	V <sub>FB</sub> Rising
PGD Rising (Fault) Voltage	V <sub>PGDTH_RF</sub>	V <sub>FB</sub> x 1.07	V <sub>FB</sub> x 1.10	V <sub>FB</sub> x 1.13	V	V <sub>FB</sub> Rising
PGD Falling (Good) Voltage	V <sub>PGDTH_FG</sub>	V <sub>FB</sub> x 1.04	V <sub>FB</sub> x 1.07	V <sub>FB</sub> x 1.10	V	V <sub>FB</sub> Falling
PGD Output Leakage Current	I <sub>LEAKPGD</sub>	-	0	2.0	μA	V <sub>PGD</sub> = 5.0 V, Ta = 25 °C
PGD FET ON Resistance	R <sub>PGD</sub>	30	60	120	Ω	
PGD Output Low Level Voltage	V <sub>PGDL</sub>	0.03	0.06	0.12	V	I <sub>PGD</sub> = 1.0 mA
<b>Switch MOSFET</b>						
High Side FET ON Resistance	R <sub>ONH</sub>	80	150	250	mΩ	V <sub>IN</sub> = 5.0 V
		90	175	280	mΩ	V <sub>IN</sub> = 3.3 V
Low Side FET ON Resistance	R <sub>ONL</sub>	55	95	150	mΩ	V <sub>IN</sub> = 5.0 V
		60	100	160	mΩ	V <sub>IN</sub> = 3.3 V
High Side FET Leakage Current	I <sub>LEAKSWH</sub>	-	0	5.0	μA	V <sub>IN</sub> = 5.5 V, V <sub>SW</sub> = 0 V, Ta = 25 °C
Low Side FET Leakage Current	I <sub>LEAKSWL</sub>	-	0	5.0	μA	V <sub>IN</sub> = 5.5 V, V <sub>SW</sub> = 5.5 V, Ta = 25 °C
SW Current of Over Current Protection <sup>(Note 2)</sup>	I <sub>OCP</sub>	2.30	2.85	3.40	A	
SW Discharge Resistance	R <sub>DIS</sub>	20	50	100	Ω	
<b>SCP, OVP</b>						
Short Circuit Protection Detection Voltage	V <sub>SCP</sub>	0.48	0.56	0.64	V	V <sub>FB</sub> Falling
Output Over Voltage Protection Detection Voltage	V <sub>OVP</sub>	0.856	0.880	0.904	V	V <sub>FB</sub> Rising

(Note 1) It is tested in a proprietary test mode that connects FB to the output of the error amplifier.

(Note 2) This is design value. Not production tested.

Typical Performance Curves

Unless otherwise specified  $V_{IN} = V_{EN}$

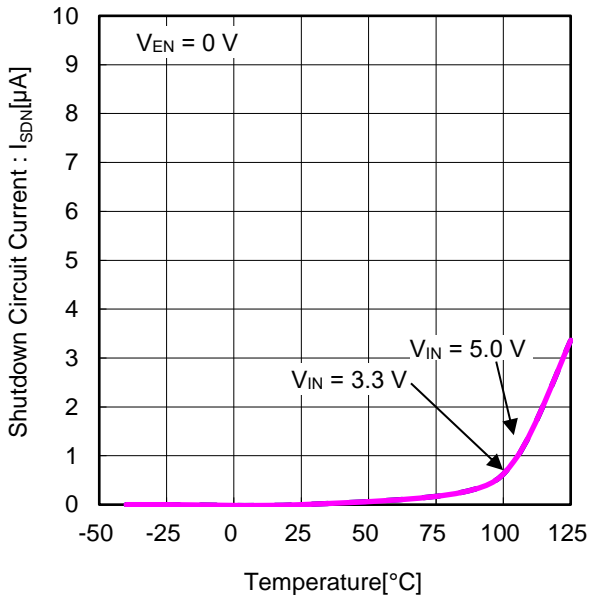


Figure 1. Shutdown Circuit Current vs Temperature

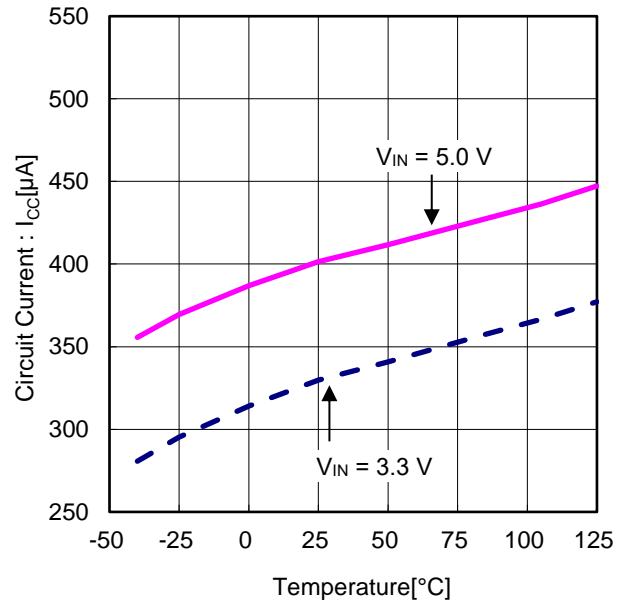


Figure 2. Circuit Current vs Temperature

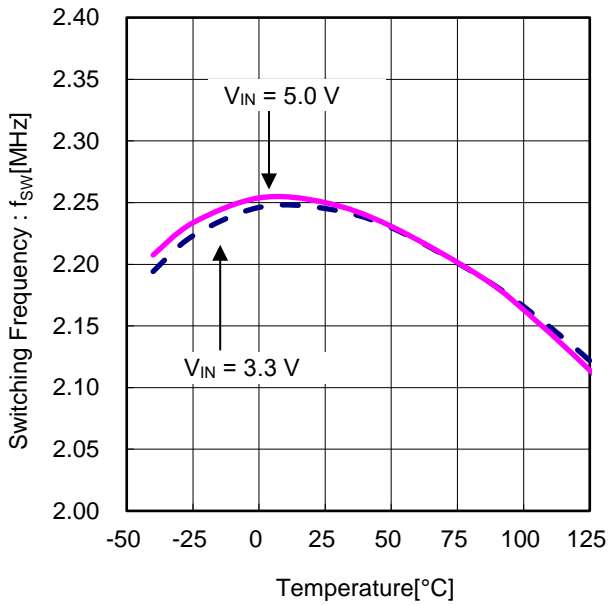


Figure 3. Switching Frequency vs Temperature

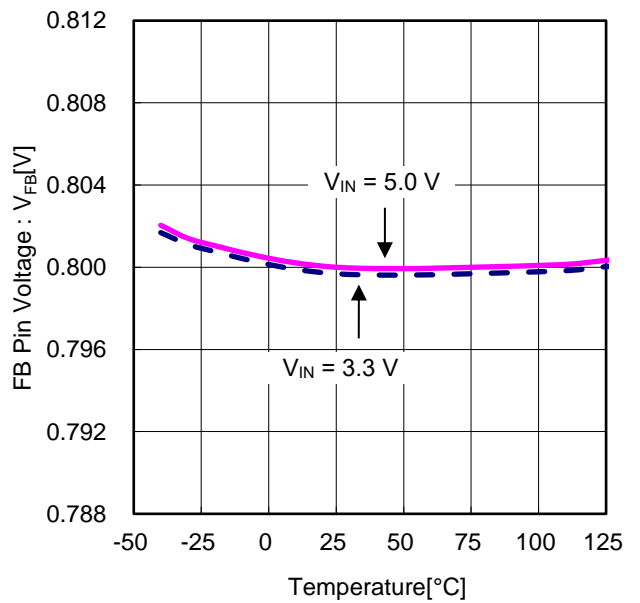


Figure 4. FB Pin Voltage vs Temperature

Typical Performance Curves – continued

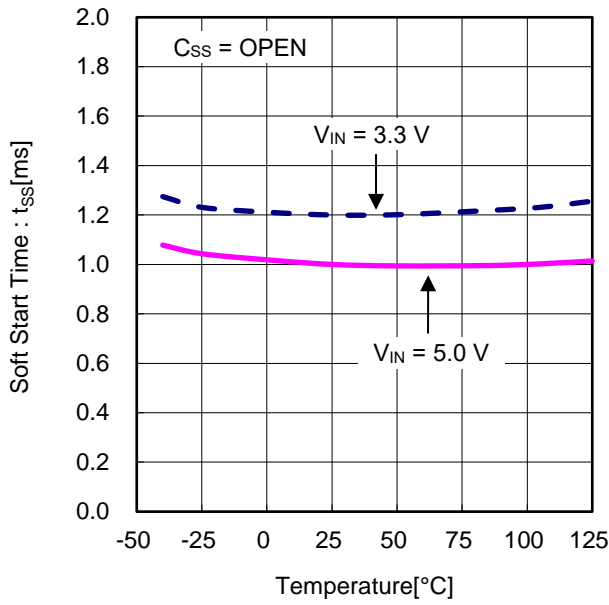


Figure 5. Soft Start Time vs Temperature

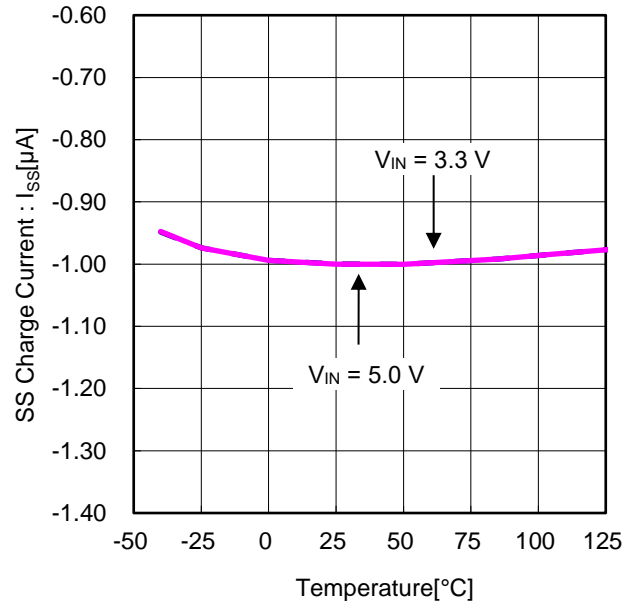


Figure 6. SS Charge Current vs Temperature

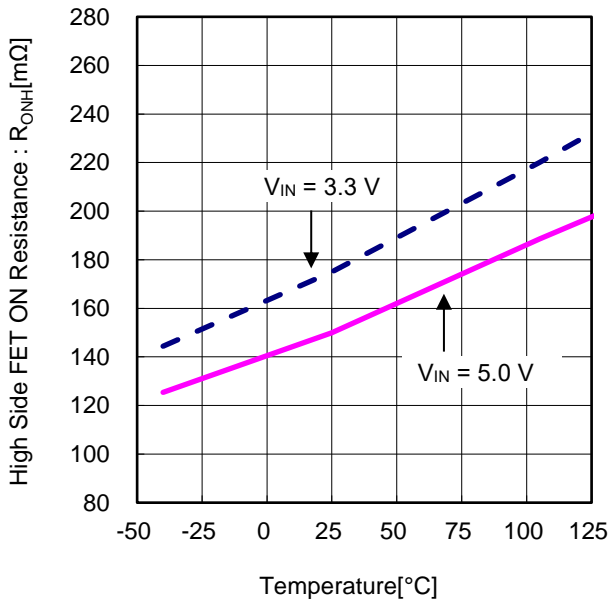


Figure 7. High Side FET ON Resistance vs Temperature

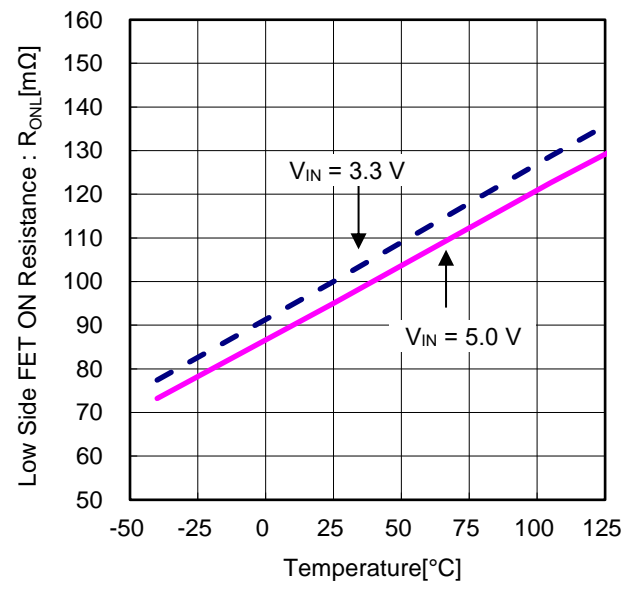


Figure 8. Low Side FET ON Resistance vs Temperature



Typical Performance Curves – continued

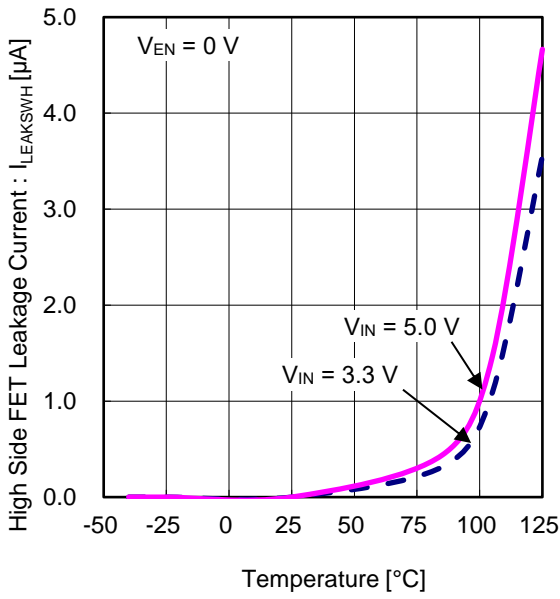


Figure 9. High Side FET Leakage Current vs Temperature

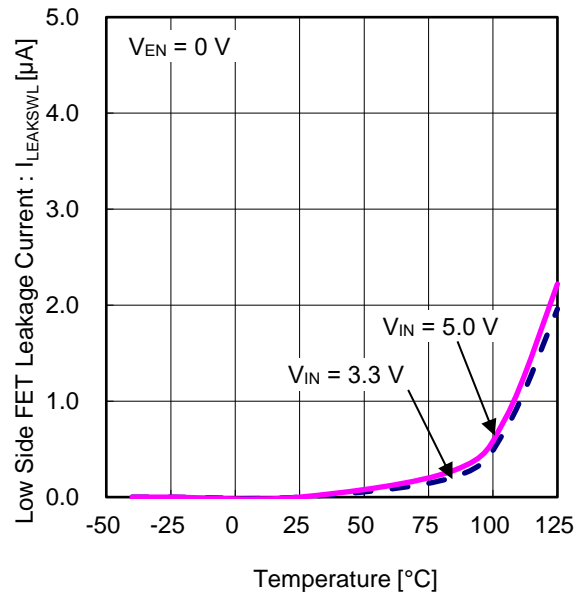


Figure 10. Low Side FET Leakage Current vs Temperature

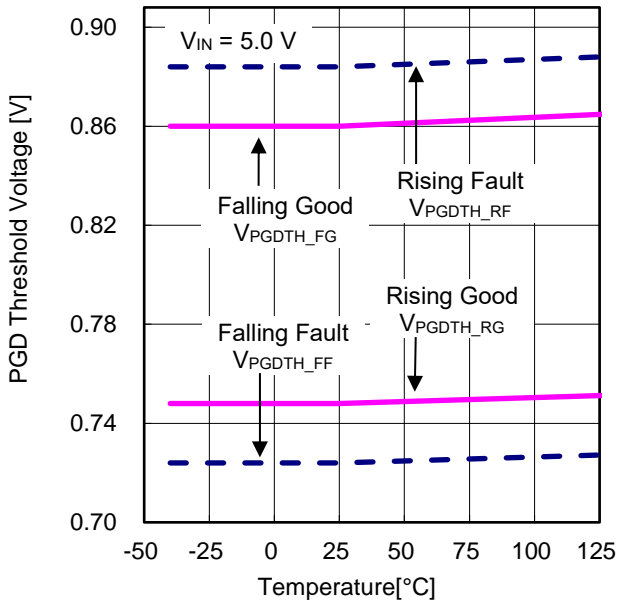


Figure 11. PGD Threshold Voltage vs Temperature

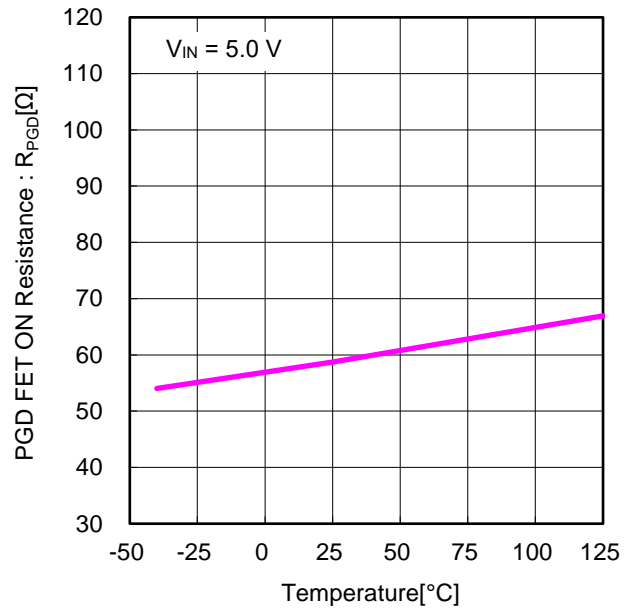


Figure 12. PGD FET ON Resistance vs Temperature

Typical Performance Curves – continued

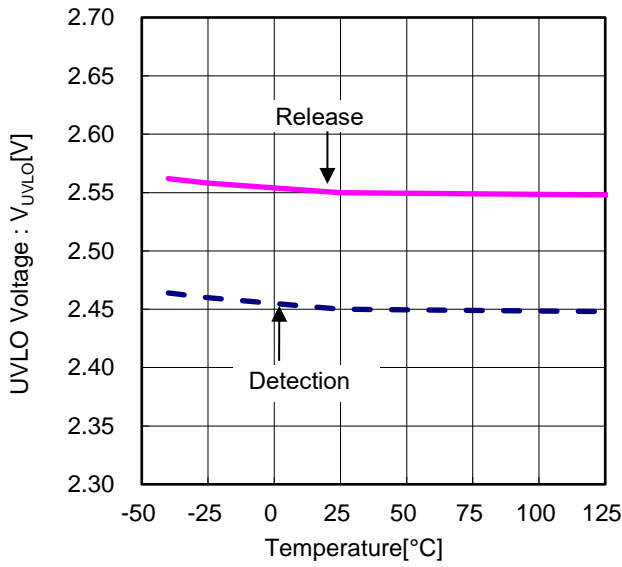


Figure 13. UVLO Voltage vs Temperature

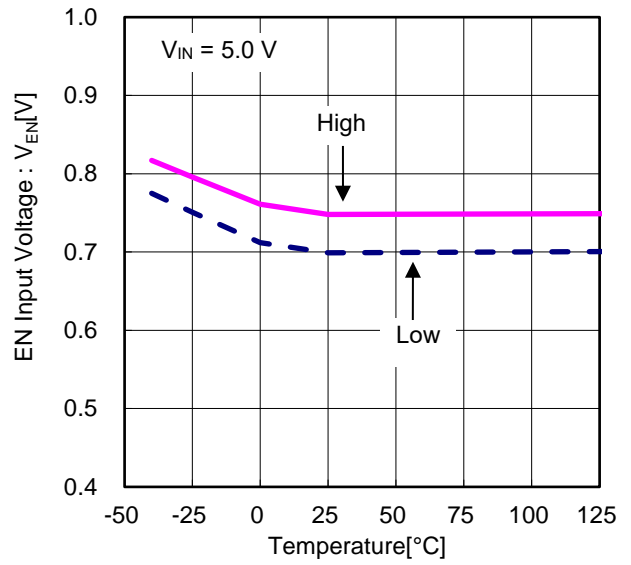


Figure 14. EN Input Voltage vs Temperature

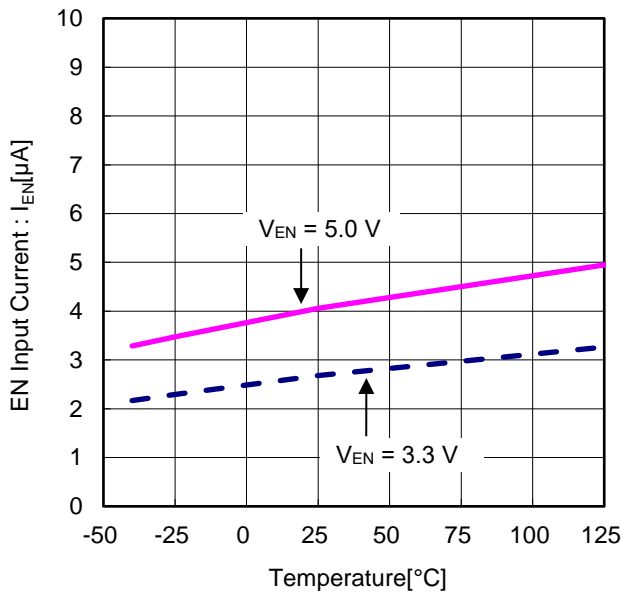


Figure 15. EN Input Current vs Temperature

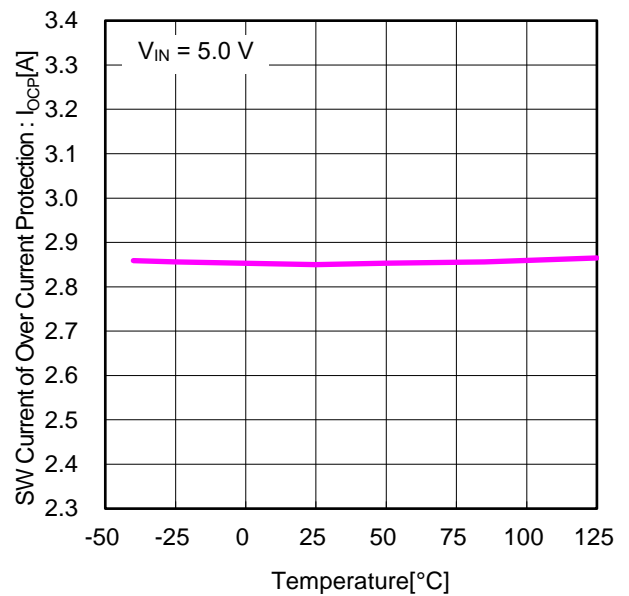


Figure 16. SW Current of Over Current Protection vs Temperature

Typical Performance Curves – continued

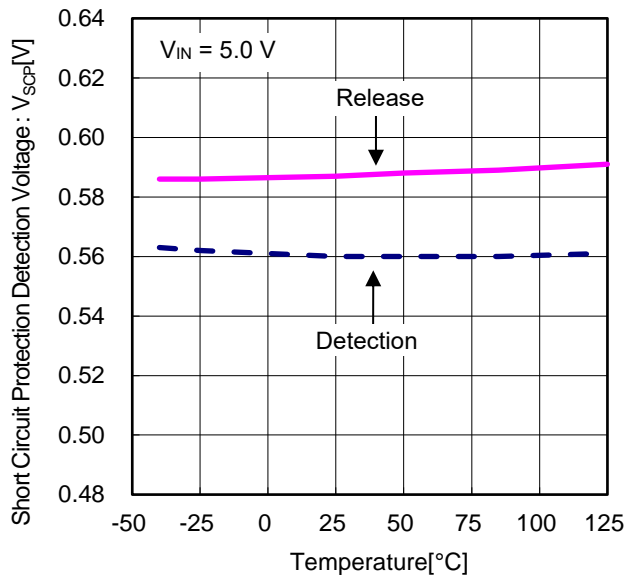


Figure 17. Short Circuit Protection Detection Voltage vs Temperature

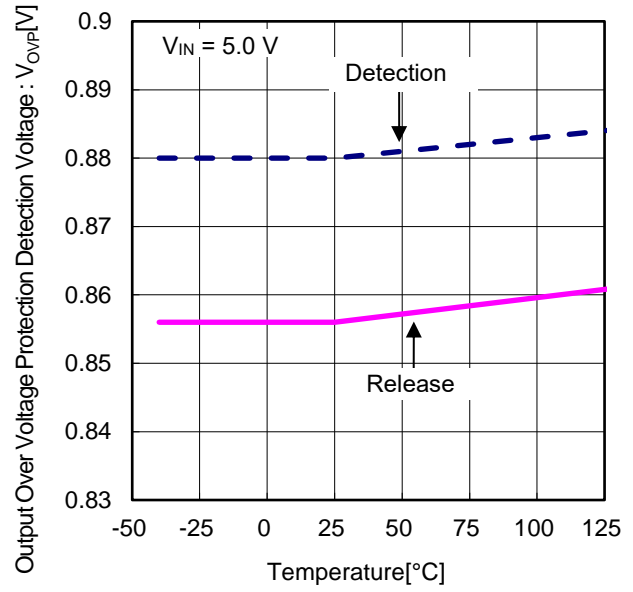


Figure 18. Output Over Voltage Protection Detection Voltage vs Temperature

Function Explanations

1. Enable Control

The device shutdown can be controlled by the voltage applied to the EN pin. When  $V_{EN}$  becomes 1.0 V or more, the internal circuit is activated and the device starts up with soft start. When  $V_{EN}$  becomes 0.4 V or less, the device is shutdown.

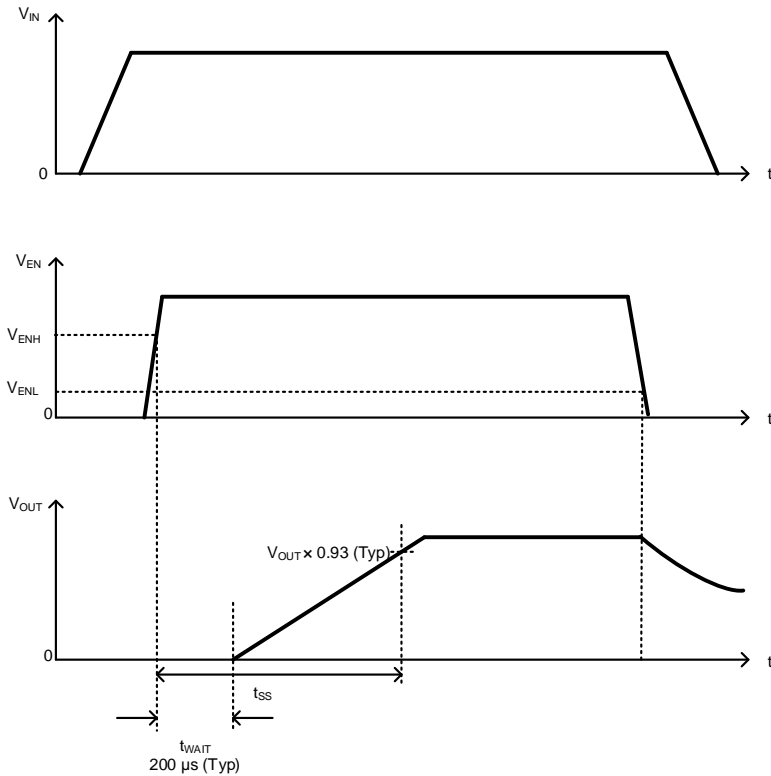


Figure 19. Enable ON/OFF Timing Chart

2. Power Good Output

When the FB pin voltage reaches 0.8 V (Typ) within  $\pm 7\%$ , the PGD pin open drain MOSFET turns OFF and the output turns high. There is a 3% hysteresis on the threshold voltage, so when the FB pin voltage reaches outside  $\pm 10\%$  of 0.8 V (Typ), the PGD pin open drain MOSFET turns ON and the PGD pin is pulled down with impedance of 60  $\Omega$  (Typ). It is recommended to use a pull-up resistor of 2 k $\Omega$  to 100 k $\Omega$  for the power source. If an adjacent short with the EN pin is assumed, control by the EN signal may not be possible if the resistance value is reduced. Check the actual application thoroughly before deciding the resistance value. If the power good function is not used, connect the PGD pin to OPEN or GND.

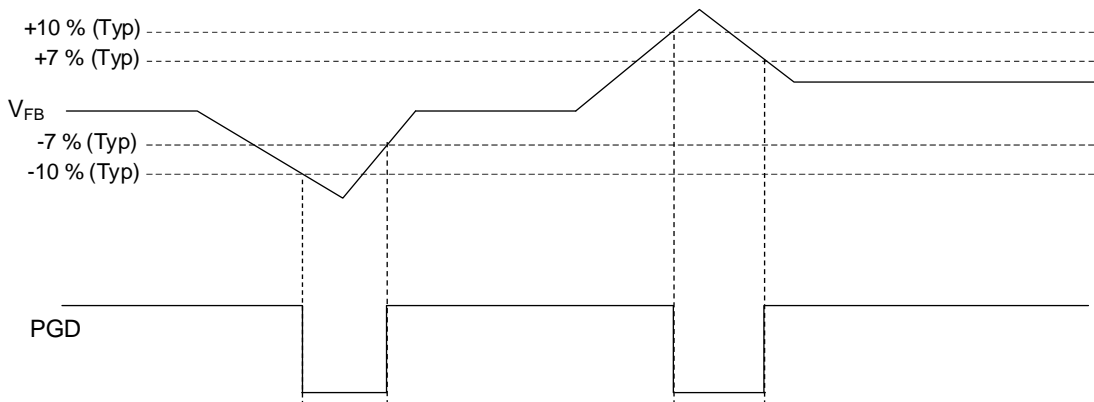


Figure 20. Power Good Timing Chart

## Function Explanations – continued

## 3. Output Discharge Function

When even one of the following conditions is satisfied, output is discharged with 50  $\Omega$  (Typ) resistance through the SW pin.

- $V_{EN}$  becomes 0.4 V or less
- $V_{IN}$  becomes 2.45 V (Typ) or less (UVLO)
- $V_{FB}$  becomes 0.56 V (Typ) or less and remains there for 1 ms (Typ) (SCP)
- $V_{FB}$  becomes 0.88 V (Typ) or more (OVP)
- $T_j$  becomes 175  $^{\circ}\text{C}$  (Typ) or more (TSD)

When all of the above conditions are released, output discharge is stopped.

## 4. Pre-bias Function

The device can start up without to sink large current from the output even when the output is pre-biased. For example, if the device is turned ON/OFF by the EN pin, the output is discharged with the resistor of 50  $\Omega$  (Typ) during the EN OFF section and the delay section  $t_{WAIT}$  of 200  $\mu\text{s}$  (Typ) after restarting, but both output MOSFETs are turned off. After that, when the internal SS voltage reaches the high voltage 40 mV (Typ) than the internal FB voltage, the device starts switching and the output rises to the set voltage with soft start.

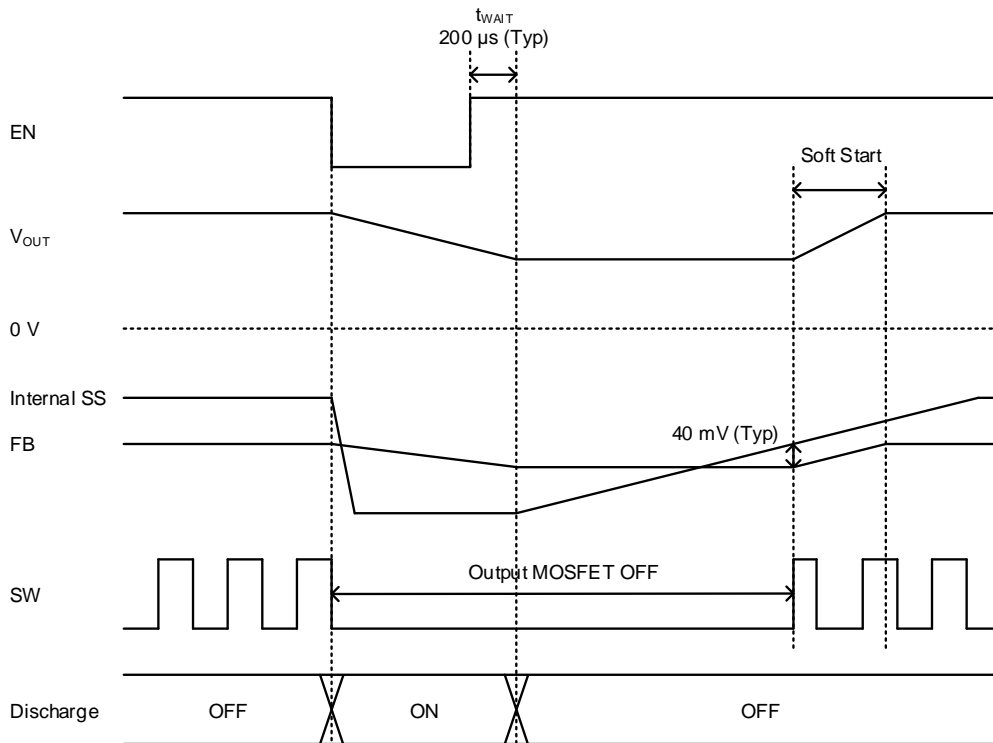


Figure 21. Pre-bias Timing Chart

Protection

1. Short Circuit Protection (SCP)

The Short Circuit Protection block compares the FB pin voltage with the internal reference voltage VREF. When the FB pin voltage has fallen to 0.56 V (Typ) or less and remained there for 1 ms (Typ), SCP stops the operation for 14 ms (Typ) and subsequently initiates a restart. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected at all times).

The EN Pin	The FB Pin	Short Circuit Protection	Short Circuit Protection Operation
1.0 V or more	$\leq 0.56 \text{ V (Typ)}$	Enabled	ON
	$\geq 0.60 \text{ V (Typ)}$		OFF
0.4 V or less	-	Disabled	OFF

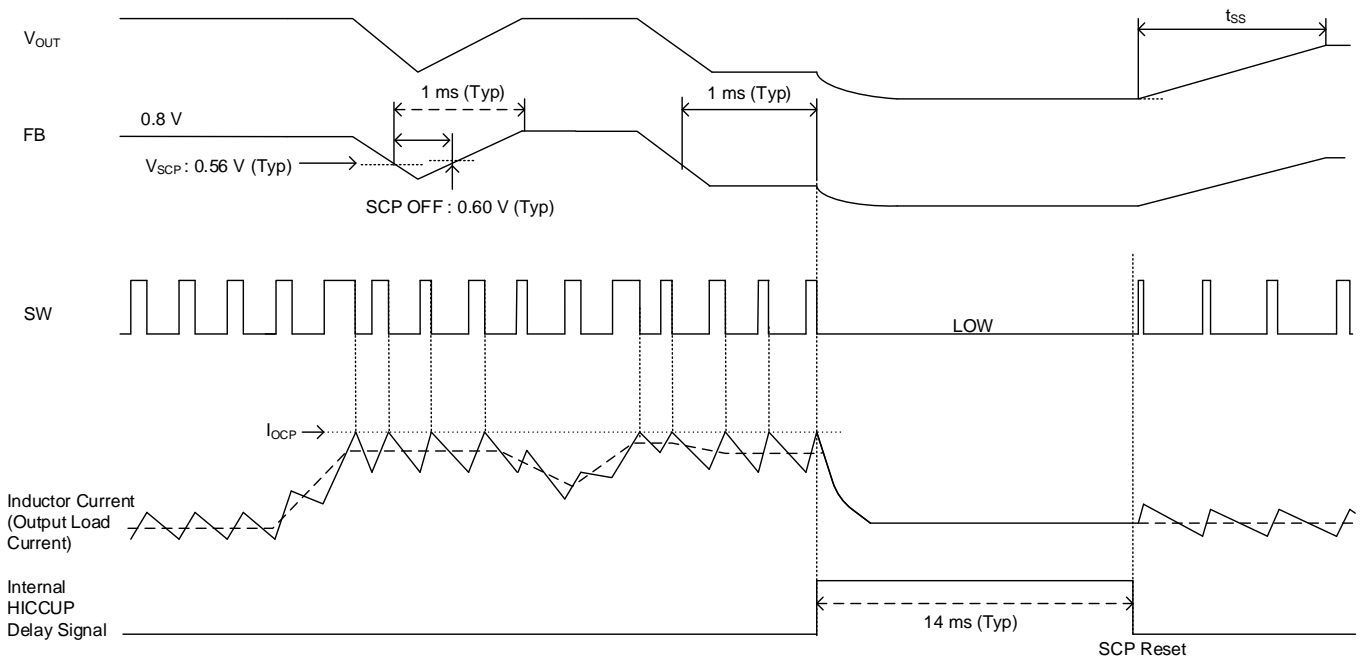


Figure 22. Short Circuit Protection (SCP) Timing Chart

2. Over Current Protection (OCP)

The Over Current Protection function operates by limiting the current that flows through High Side FET at each cycle of the switching frequency. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected at all times).

Protection – continued

3. Under Voltage Lockout Protection (UVLO)

It shuts down the device when the VIN pin falls to 2.45 V (Typ) or less. The threshold voltage has a hysteresis of 100 mV (Typ).

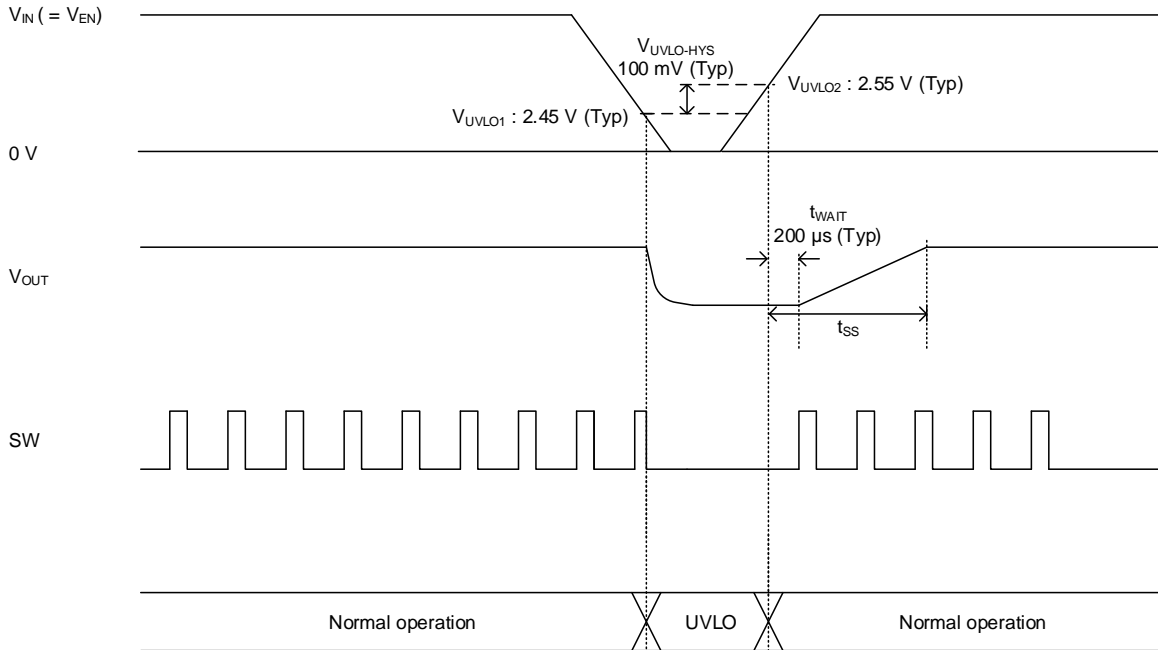


Figure 23. UVLO Timing Chart

4. Thermal Shutdown (TSD)

This is the thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. However, if the rating is exceeded for a continued period and the junction temperature ( $T_j$ ) rises to  $175 \text{ }^\circ\text{C (Typ)}$ , the TSD circuit activates and the output MOSFETs turn OFF. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

5. Over Voltage Protection (OVP)

The device incorporates an over voltage protection circuit to minimize the output voltage overshoot when recovering from strong load transients or output fault conditions. If the FB pin voltage becomes over or equal to  $0.88 \text{ V (Typ)}$ , which is Output Over Voltage Protection Detection Voltage, the MOSFETs on the output stage are turned OFF to prevent the increase in the output voltage. After the detection, the switching operation resumes if the output decreases, the over voltage state is released, and FB pin voltage reaches  $0.8 \text{ V (Typ)}$ . Output Over Voltage Protection Detection Voltage and release voltage have a hysteresis of 3 %.

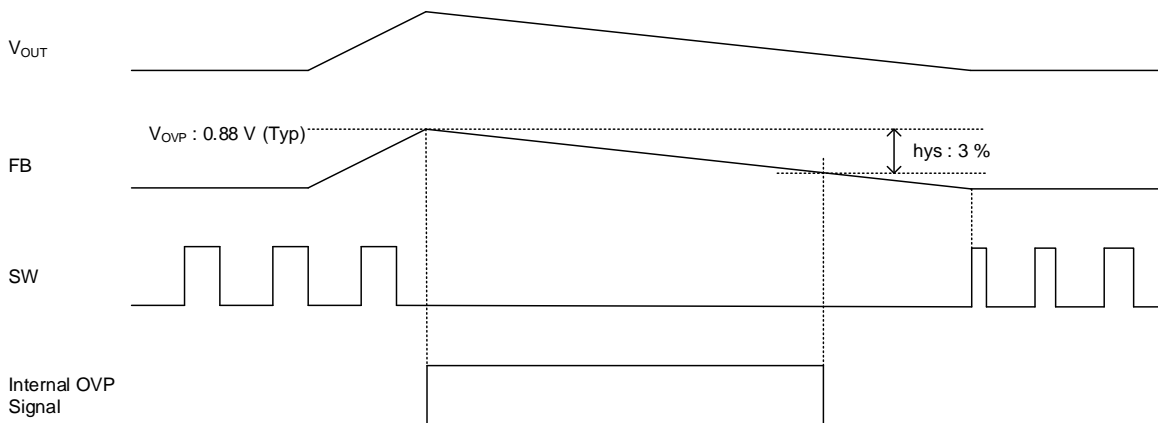


Figure 24. OVP Timing Chart

**Selection of Components Externally Connected**

Contact us if not use the recommended constant in this section.

Necessary parameters in designing the power supply are as follows:

Table 1. Application Specification

Parameter	Symbol	Example Value
Input Voltage	$V_{IN}$	5.0 V
Output Voltage	$V_{OUT}$	1.2 V (Typ)
Switching Frequency	$f_{sw}$	2.2 MHz (Typ)
Output Ripple Current	$\Delta I_L$	0.61 A
Output Capacitor	$C_{OUT}$	10 $\mu$ F
Soft Start Time	$t_{ss}$	8.55 ms (Typ)
Maximum Output Current	$I_{OUTMAX}$	2.0 A

**Application Example**

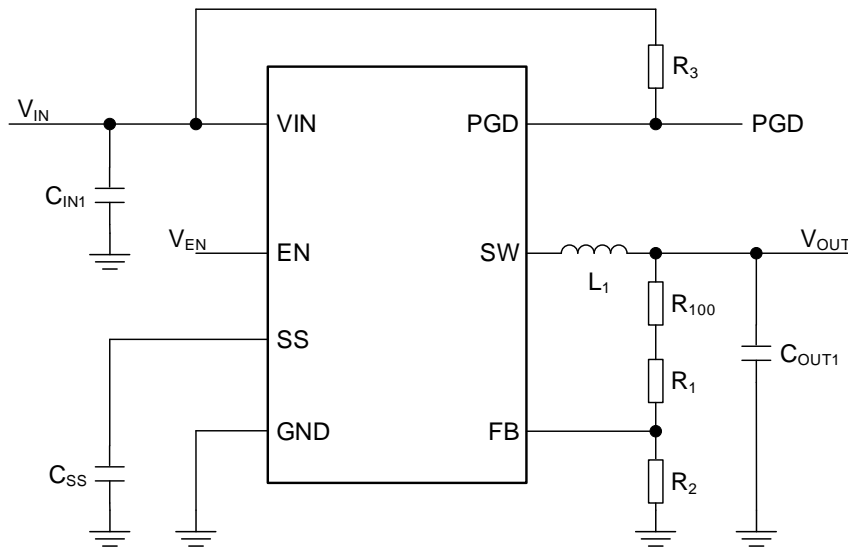


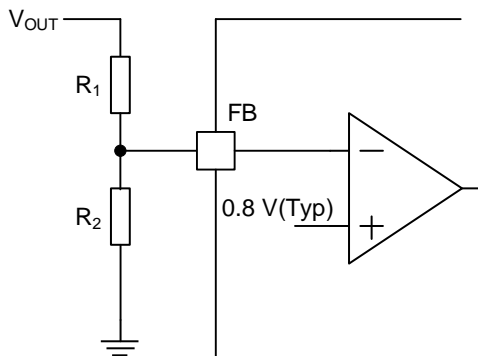
Figure 25. Application Circuit

**1. Switching Frequency**

The switching frequency  $f_{sw}$  is fixed at 2.2 MHz (Typ) inside the IC.

**2. Selection of Output Voltage Setting**

The output voltage value can be set by the feedback resistance ratio.



$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times 0.8 \text{ [V]}$$

※ SW Minimum ON Time that BD9S209NUX-C can output stably in the entire load range is 80 ns. Use this value to calculate the input and output conditions that satisfy the following equation.

$$80 \text{ [ns]} \leq \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Figure 26. Feedback Resistor Circuit



## Selection of Components Externally Connected – continued

### 3. Selection of Input Capacitor

Use ceramic type capacitor for the input capacitor  $C_{IN1}$ .  $C_{IN1}$  is used to suppress the input ripple noise and this capacitor is effective by being placed as close as possible to the  $V_{IN}$  pin. Set the capacitor value for  $C_{IN1}$  so that it does not fall to 4.7  $\mu\text{F}$  against the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. Use components which are comparatively same with the components used in “[Application Example](#)”. Moreover, factors like the PCB layout and the position of the capacitor may lead to IC malfunction. Refer to “[PCB Layout Design](#)”. In addition, the capacitor with value 0.1  $\mu\text{F}$  can be added to suppress the high frequency noise as an option.

### 4. Selection of Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. Use the inductor with value 0.68  $\mu\text{H}$  to 1.0  $\mu\text{H}$ .

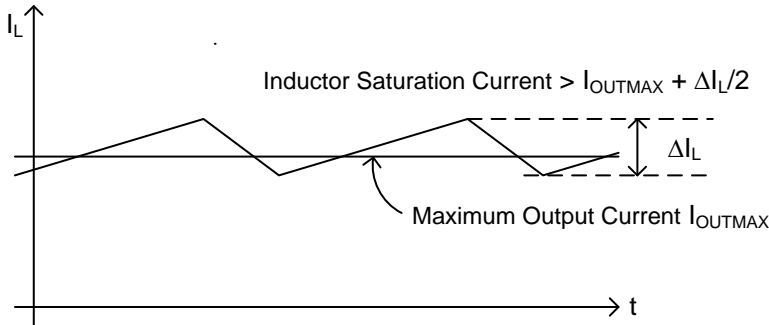


Figure 27. Waveform of Current through Inductor

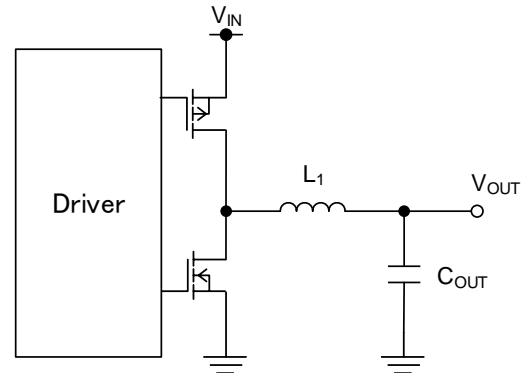


Figure 28. Output LC Filter Circuit

Inductor ripple current  $\Delta I_L$  can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L_1} = 610 \text{ [mA]}$$

where:

$V_{IN}$  is the 5.0 V.

$V_{OUT}$  is the 1.2 V.

$L_1$  is the 0.68  $\mu\text{H}$ .

$f_{SW}$  is the 2.2 MHz (Switching Frequency).

The rated current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current  $\Delta I_L$ .

Use ceramic type capacitor for the output capacitor  $C_{OUT}$ . The capacitance value of  $C_{OUT}$  is recommended in the range between 10  $\mu\text{F}$  and 22  $\mu\text{F}$ .  $C_{OUT}$  affects the output ripple voltage characteristics.  $C_{OUT}$  must satisfy the required ripple voltage characteristics.

The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left( R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \text{ [V]}$$

where:

$R_{ESR}$  is the Equivalent Series Resistance (ESR) of the output capacitor.

The output ripple voltage  $\Delta V_{RPL}$  can be represented by the following equation.

$$\Delta V_{RPL} = 0.610 \text{ A} \times \left( 10 \text{ m}\Omega + \frac{1}{8 \times 10 \mu\text{F} \times 2.2 \text{ MHz}} \right) = 9.57 \text{ [mV]}$$

where:

$C_{OUT}$  is the 10  $\mu\text{F}$ .

$R_{ESR}$  is the 10 m $\Omega$ .

**4. Selection of Output LC Filter – continued**

In addition, for the total value of capacitance in the output line C<sub>OUT</sub> (Max), need to satisfy the value obtained by the following equation.

$$C_{OUT(Max)} < \frac{(t_{SS(Min)} - 200 \mu s) \times (I_{OCP(Min)} - I_{SWSTART})}{V_{OUT}} \text{ [F]}$$

where:

- I<sub>SWSTART</sub> is the maximum output current during startup.
- I<sub>OCP(Min)</sub> is the minimum OCP operation SW current 2.3 A.
- t<sub>SS(Min)</sub> is the minimum Soft Start Time t<sub>SS</sub> ([Electrical Characteristics](#)).
- V<sub>OUT</sub> is the output voltage.

Startup failure may happen if the limits from the above-mentioned are exceeded. Especially if the capacitance value is large, over current protection may be activated by the inrush current at startup and prevented to turn on the output. Confirm this on the actual application.

Stable transient response and the loop is dependent to C<sub>OUT</sub>. Actually, characteristics vary depending on PCB layout, arrangement of wiring, kinds of parts used and use conditions (temperature, etc.). Be sure to check stability and responsiveness with the actual application.

**5. Selection of Soft Start Capacitor**

Turning the EN pin signal high activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time t<sub>SS\_EXT</sub> depends on the value of the capacitor connected to the SS pin. The capacitance value should be set in the range between 4700 pF and 0.1 μF.

$$t_{SS\_EXT} = \frac{(C_{SS} \times 0.8)}{I_{SS}} + t_{OFFSET} \text{ [s]}$$

$$t_{OFFSET} = \frac{(C_{SS} \times 0.04)}{I_{SS}} + 150 \times 10^{-6} \text{ [s]}$$

where:

- t<sub>SS\_EXT</sub> is the Soft Start Time.
- t<sub>OFFSET</sub> is the Internal Delay Time.
- C<sub>SS</sub> is the Capacitor connected to the SS pin.
- I<sub>SS</sub> is the SS Charge Current 1.0 μA (Typ).

With C<sub>SS</sub> = 0.01 μF

$$t_{SS\_EXT} = \frac{(0.01 \mu F \times 0.8)}{1.0 \mu A} + \frac{(0.01 \mu F \times 0.04)}{1.0 \mu A} + 150 \times 10^{-6} = 0.00855 = 8.55 \text{ [ms]}$$

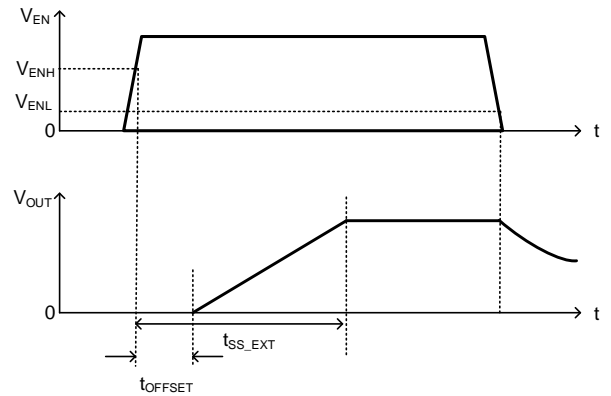


Figure 29. Soft Start Timing Chart

Turning the EN pin High without connecting capacitor to the SS pin and keeping the SS pin either OPEN condition or 10 kΩ to 100 kΩ pull up condition to power source, the output rises in 1 ms (Typ).

**Recommended Parts Manufacturer List**

Shown below is the list of the recommended parts manufacturers for reference.

Table 2. recommended parts manufacturers

Type	Manufacturer	URL
Ceramic capacitor	Murata	<a href="http://www.murata.com">www.murata.com</a>
Ceramic capacitor	TDK	<a href="http://product.tdk.com">product.tdk.com</a>
Inductor	Coilcraft	<a href="http://www.coilcraft.com">www.coilcraft.com</a>
Inductor	Cyntec	<a href="http://www.cyntec.com">www.cyntec.com</a>
Inductor	Murata	<a href="http://www.murata.com">www.murata.com</a>
Inductor	Sumida	<a href="http://www.sumida.com">www.sumida.com</a>
Inductor	TDK	<a href="http://product.tdk.com">product.tdk.com</a>
Resistor	ROHM	<a href="http://www.rohm.com">www.rohm.com</a>

## Application Example 1

Table 3. Specification Example 1

Parameter	Symbol	Example Value
Product Name	IC	BD9S209NUX-C
Input Voltage	$V_{IN}$	5.0 V, 3.3 V
Output Voltage	$V_{OUT}$	1.0 V
Soft Start Time	$t_{SS}$	1.0 ms (Typ)
Maximum Output Current	$I_{OUTMAX}$	2.0 A
Operation Temperature Range	$T_a$	-40 °C to +125 °C

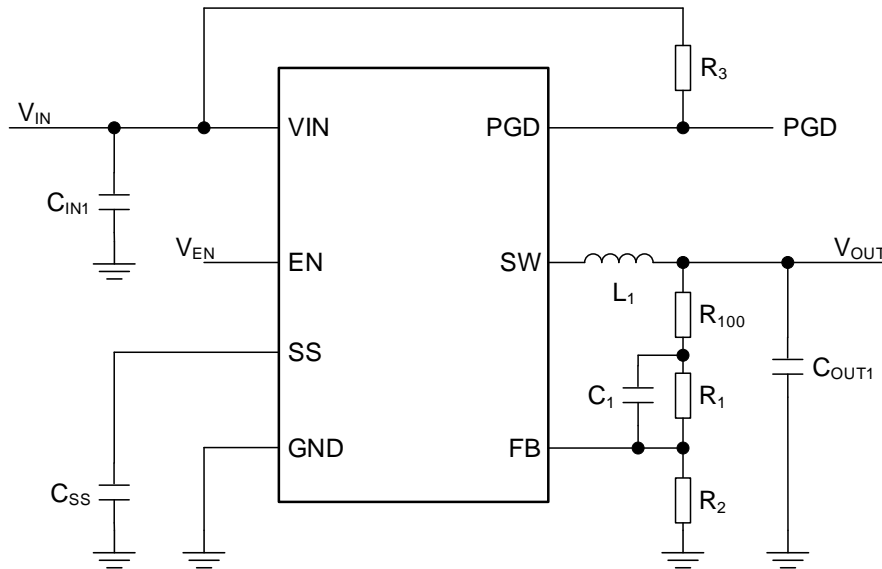


Figure 30. Measurement Circuit 1

Table 4. Parts List 1

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
L1	2520	0.68 $\mu$ H	DFE252012PD-R68M	Inductor	Murata
COUT1	2012	10 $\mu$ F, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
CIN1	2012	10 $\mu$ F, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
R100	-	SHORT	-	-	-
R1	1005	7.5 k $\Omega$ , 1 %, 1/16 W	MCR01MZPF7501	Chip Resistor	ROHM
R2	1005	30 k $\Omega$ , 1 %, 1/16 W	MCR01MZPF3002	Chip Resistor	ROHM
R3	1005	100 k $\Omega$ , 1 %, 1/16 W	MCR01MZPF1003	Chip Resistor	ROHM
CSS	-	-	-	-	-
C1	1005	100 pF, CH, 50 V	GCM1552C1H101JA01	Ceramic Capacitor	Murata

Characteristic Data (Application Examples 1)

$V_{IN} = V_{EN}$ ,  $T_a = 25\text{ }^\circ\text{C}$

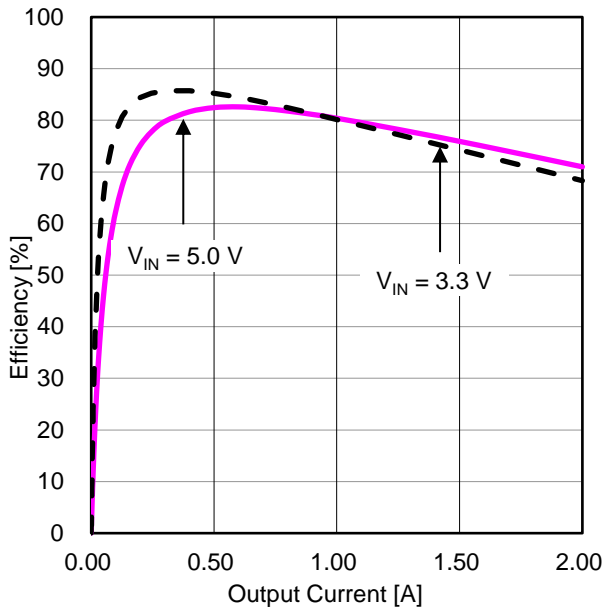


Figure 31. Efficiency vs Output Current

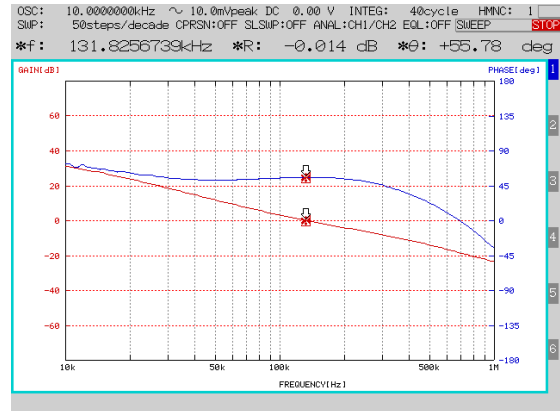


Figure 32. Frequency Characteristics ( $I_{OUT} = 0.5\text{ A}$ )

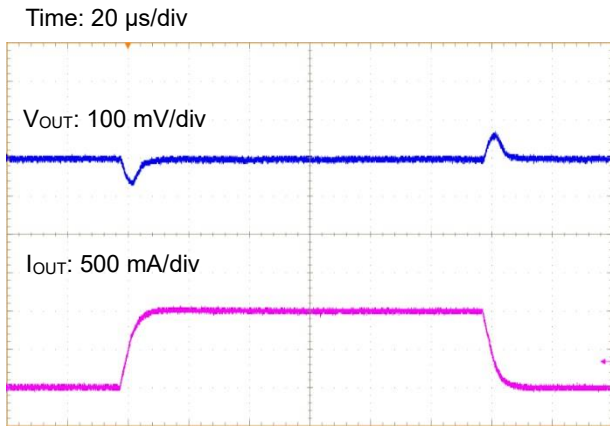


Figure 33. Load Transient Response ( $I_{OUT} = 0\text{ A} \leftrightarrow 1\text{ A}$ )

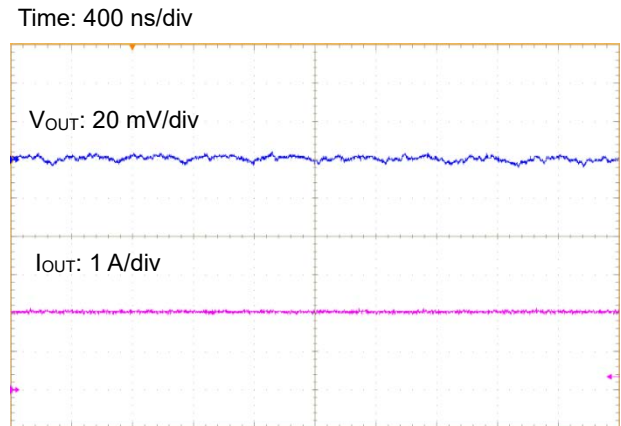


Figure 34. Output Ripple Voltage ( $I_{OUT} = 2\text{ A}$ )

## Application Example 2

Table 5. Specification Example 2

Parameter	Symbol	Example Value
Product Name	IC	BD9S209NUX-C
Input Voltage	$V_{IN}$	5.0 V, 3.3 V
Output Voltage	$V_{OUT}$	1.2 V
Soft Start Time	$t_{SS}$	1.0 ms (Typ)
Maximum Output Current	$I_{OUTMAX}$	2.0 A
Operation Temperature Range	$T_a$	-40 °C to +125 °C

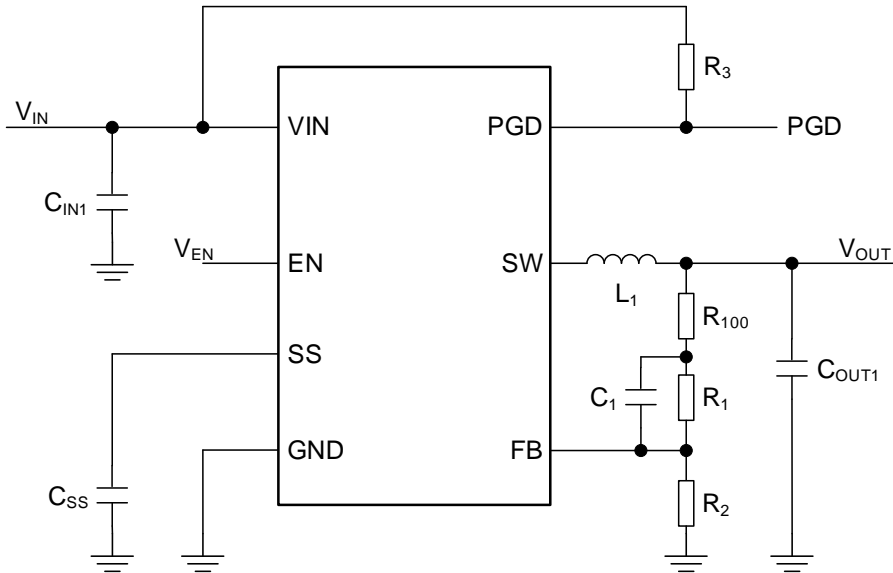


Figure 35. Measurement Circuit 2

Table 6. Parts List 2

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
L <sub>1</sub>	2520	0.68 μH	DFE252012PD-R68M	Inductor	Murata
C <sub>OUT1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
C <sub>IN1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
R <sub>100</sub>	-	SHORT	-	-	-
R <sub>1</sub>	1005	10 kΩ, 1 %, 1/16 W	MCR01MZPF1002	Chip Resistor	ROHM
R <sub>2</sub>	1005	20 kΩ, 1 %, 1/16 W	MCR01MZPF2002	Chip Resistor	ROHM
R <sub>3</sub>	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF1003	Chip Resistor	ROHM
C <sub>SS</sub>	-	-	-	-	-
C <sub>1</sub>	1005	100 pF, CH, 50 V	GCM1552C1H101JA01	Ceramic Capacitor	Murata

Characteristic Data (Application Examples 2)

$V_{IN} = V_{EN}$ ,  $T_a = 25\text{ }^\circ\text{C}$

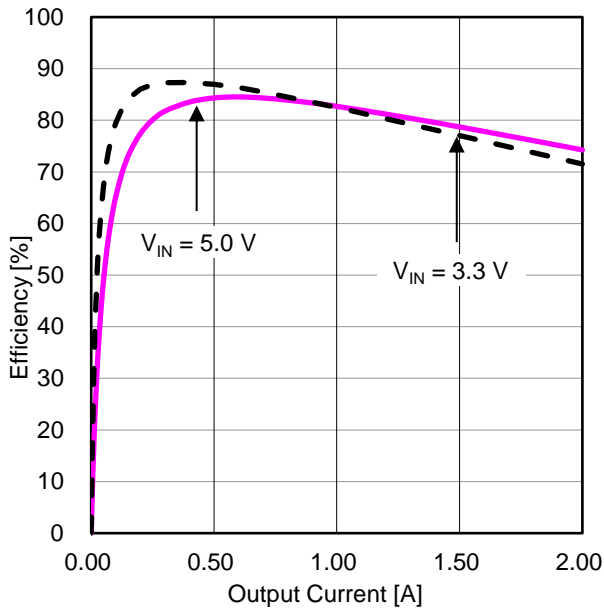


Figure 36. Efficiency vs Output Current

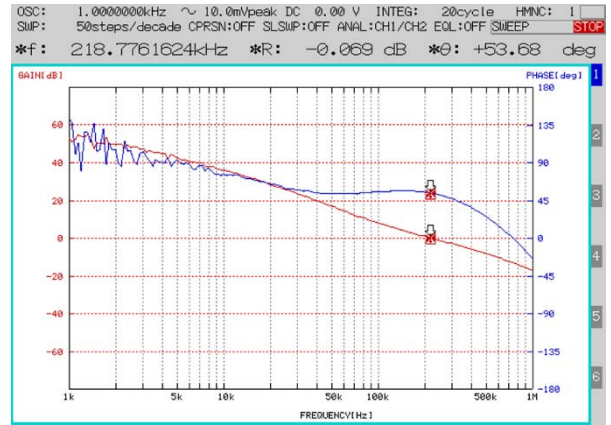


Figure 37. Frequency Characteristics ( $I_{OUT} = 0.5\text{ A}$ )

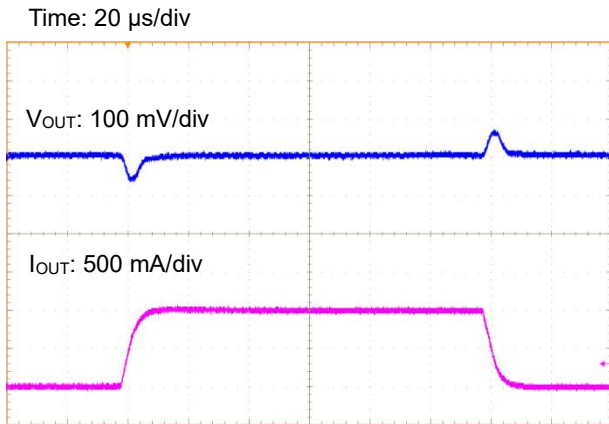


Figure 38. Load Transient Response ( $I_{OUT} = 0\text{ A} \leftrightarrow 1\text{ A}$ )

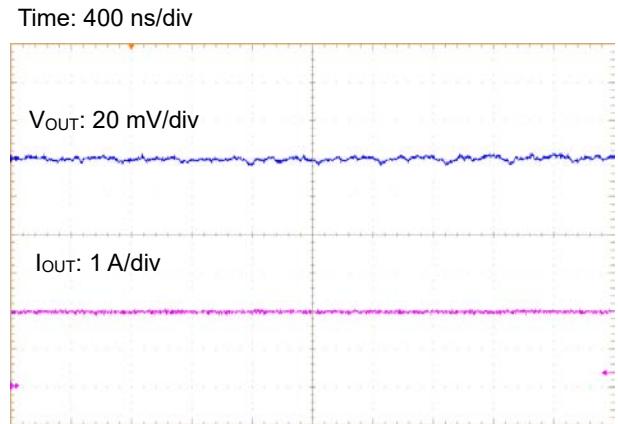


Figure 39. Output Ripple Voltage ( $I_{OUT} = 2\text{ A}$ )

Application Example 3

Table 7. Specification Example 3

Parameter	Symbol	Example Value
Product Name	IC	BD9S209NUX-C
Input Voltage	$V_{IN}$	5.0 V, 3.3 V
Output Voltage	$V_{OUT}$	1.5 V
Soft Start Time	$t_{SS}$	1.0 ms (Typ)
Maximum Output Current	$I_{OUTMAX}$	2.0 A
Operation Temperature Range	$T_a$	-40 °C to +125 °C

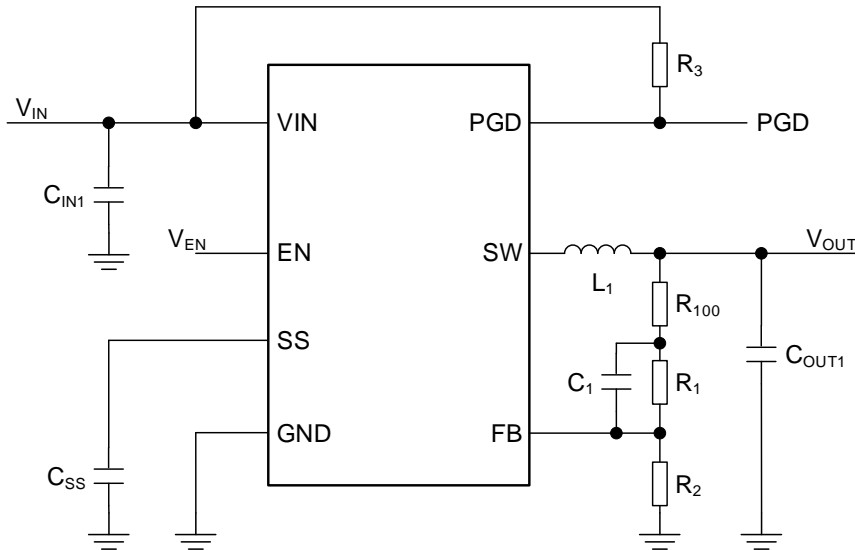


Figure 40. Measurement Circuit 3

Table 8. Parts List 3

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
L <sub>1</sub>	2520	0.68 μH	DFE252012PD-R68M	Inductor	Murata
C <sub>OUT1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
C <sub>IN1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
R <sub>100</sub>	-	SHORT	-	-	-
R <sub>1</sub>	1005	16 kΩ, 1 %, 1/16 W	MCR01MZPF1602	Chip Resistor	ROHM
R <sub>2</sub>	1005	18 kΩ, 1 %, 1/16 W	MCR01MZPF1802	Chip Resistor	ROHM
R <sub>3</sub>	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF1003	Chip Resistor	ROHM
C <sub>SS</sub>	-	-	-	-	-
C <sub>1</sub>	1005	100 pF, CH, 50 V	GCM1552C1H101JA01	Ceramic Capacitor	Murata

Characteristic Data (Application Examples 3)

$V_{IN} = V_{EN}$ ,  $T_a = 25\text{ }^\circ\text{C}$

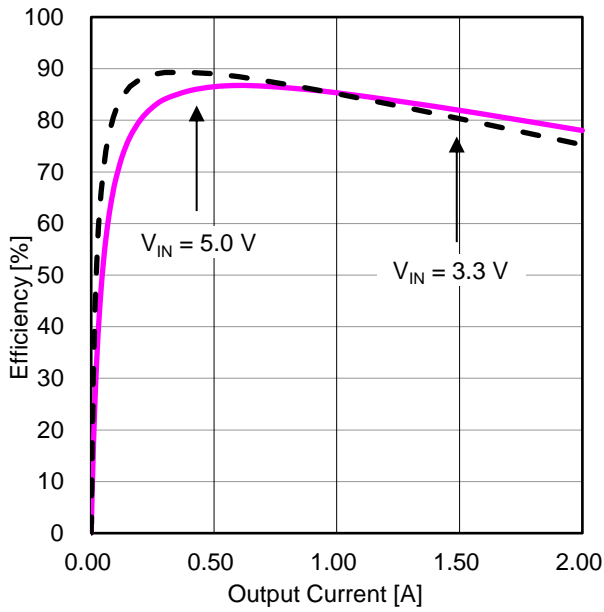


Figure 41. Efficiency vs Output Current

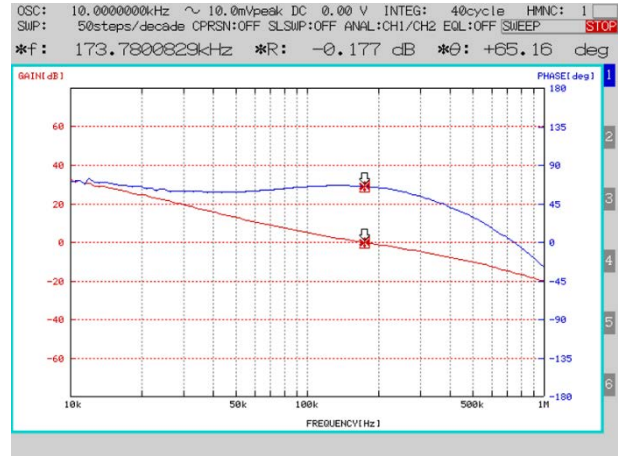


Figure 42. Frequency Characteristics ( $I_{OUT} = 0.5\text{ A}$ )

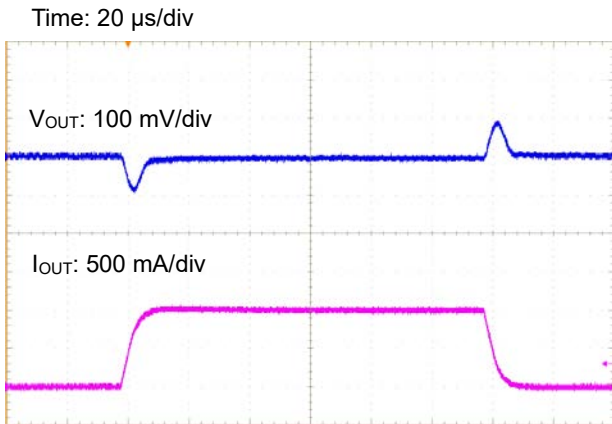


Figure 43. Load Transient Response ( $I_{OUT} = 0\text{ A} \leftrightarrow 1\text{ A}$ )

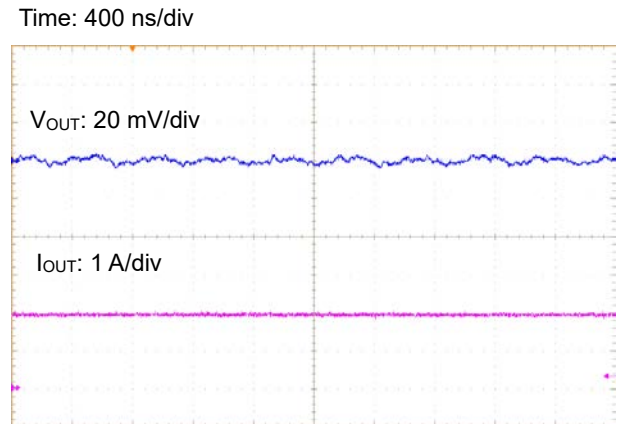


Figure 44. Output Ripple Voltage ( $I_{OUT} = 2\text{ A}$ )



Application Example 4

Table 9. Specification Example 4

Parameter	Symbol	Example Value
Product Name	IC	BD9S209NUX-C
Input Voltage	$V_{IN}$	5.0 V, 3.3 V
Output Voltage	$V_{OUT}$	1.8 V
Soft Start Time	$t_{SS}$	1.0 ms (Typ)
Maximum Output Current	$I_{OUTMAX}$	2.0 A
Operation Temperature Range	$T_a$	-40 °C to +125 °C

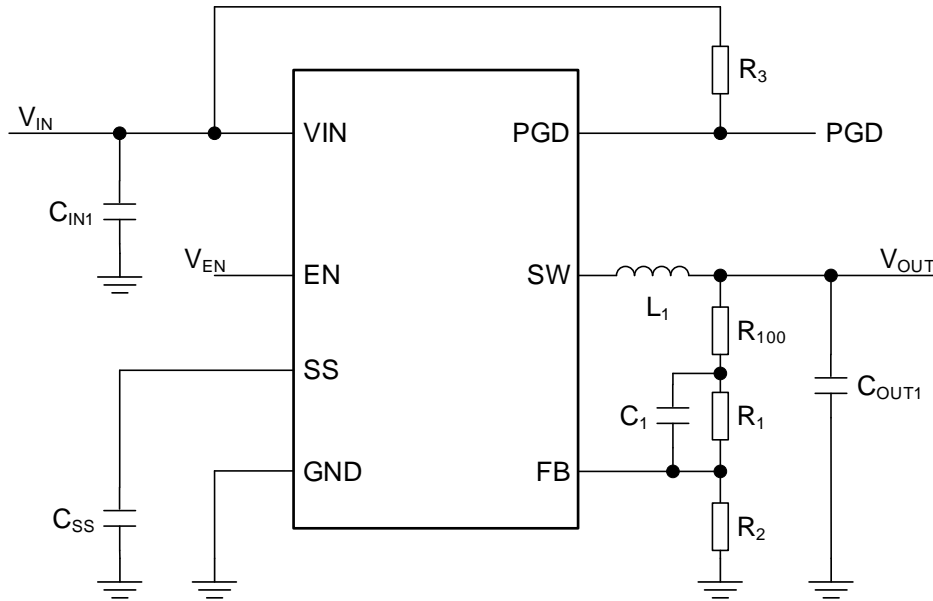


Figure 45. Measurement Circuit 4

Table 10. Parts List 4

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
L <sub>1</sub>	2520	1.0 μH	TFM252012ALMA1R0M	Inductor	TDK
C <sub>OUT1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
C <sub>IN1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
R <sub>100</sub>	-	SHORT	-	-	-
R <sub>1</sub>	1005	30 kΩ, 1 %, 1/16 W	MCR01MZPF3002	Chip Resistor	ROHM
R <sub>2</sub>	1005	24 kΩ, 1 %, 1/16 W	MCR01MZPF2402	Chip Resistor	ROHM
R <sub>3</sub>	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF1003	Chip Resistor	ROHM
C <sub>SS</sub>	-	-	-	-	-
C <sub>1</sub>	1005	100 pF, CH, 50 V	GCM1552C1H101JA01	Ceramic Capacitor	Murata

Characteristic Data (Application Examples 4)

$V_{IN} = V_{EN}$ ,  $T_a = 25\text{ }^\circ\text{C}$

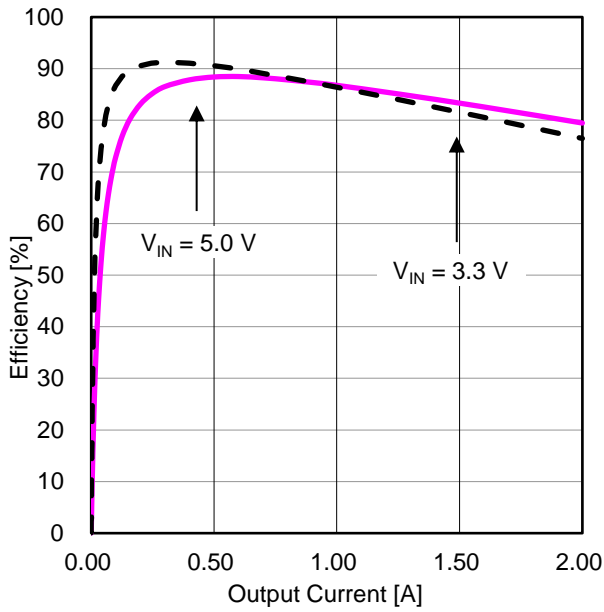


Figure 46. Efficiency vs Output Current

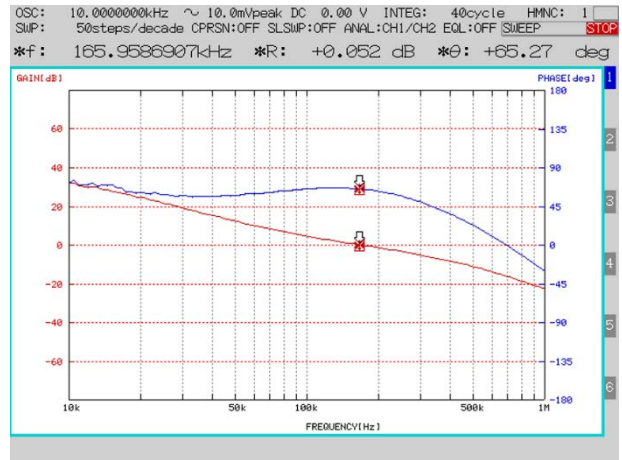


Figure 47. Frequency Characteristics ( $I_{OUT} = 0.5\text{ A}$ )

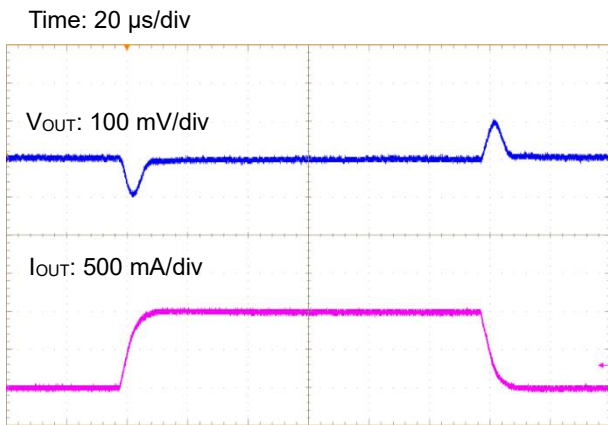


Figure 48. Load Transient Response ( $I_{OUT} = 0\text{ A} \leftrightarrow 1\text{ A}$ )

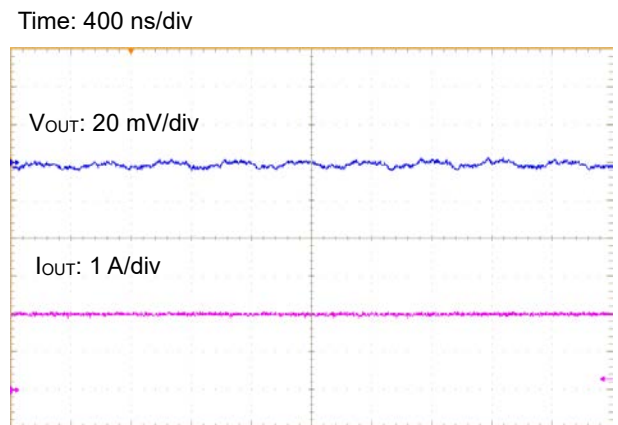


Figure 49. Output Ripple Voltage ( $I_{OUT} = 2\text{ A}$ )

Application Example 5

Table 11. Specification Example 5

Parameter	Symbol	Example Value
Product Name	IC	BD9S209NUX-C
Input Voltage	$V_{IN}$	5.0 V
Output Voltage	$V_{OUT}$	3.3 V
Soft Start Time	$t_{SS}$	1.0 ms (Typ)
Maximum Output Current	$I_{OUTMAX}$	2.0 A
Operation Temperature Range	$T_a$	-40 °C to +125 °C

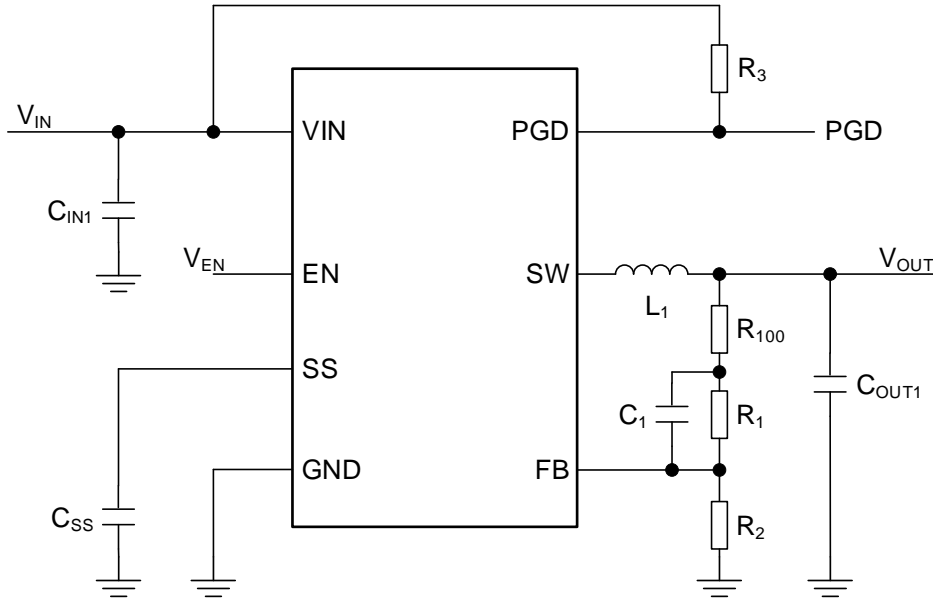


Figure 50. Measurement Circuit 5

Table 12. Parts List 5

No	Package	Parameters	Part Name (Series)	Type	Manufacturer
L <sub>1</sub>	2520	1.0 μH	TFM252012ALMA1R0M	Inductor	TDK
C <sub>OUT1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
C <sub>IN1</sub>	2012	10 μF, X7R, 10 V	GCM21BR71A106KE21	Ceramic Capacitor	Murata
R <sub>100</sub>	-	SHORT	-	-	-
R <sub>1</sub>	1005	75 kΩ, 1 %, 1/16 W	MCR01MZPF7502	Chip Resistor	ROHM
R <sub>2</sub>	1005	24 kΩ, 1 %, 1/16 W	MCR01MZPF2402	Chip Resistor	ROHM
R <sub>3</sub>	1005	100 kΩ, 1 %, 1/16 W	MCR01MZPF1003	Chip Resistor	ROHM
C <sub>SS</sub>	-	-	-	-	-
C <sub>1</sub>	1005	100 pF, CH, 50 V	GCM1552C1H101JA01	Ceramic Capacitor	Murata

Characteristic Data (Application Examples 5)

$V_{IN} = V_{EN}$ ,  $T_a = 25\text{ }^\circ\text{C}$

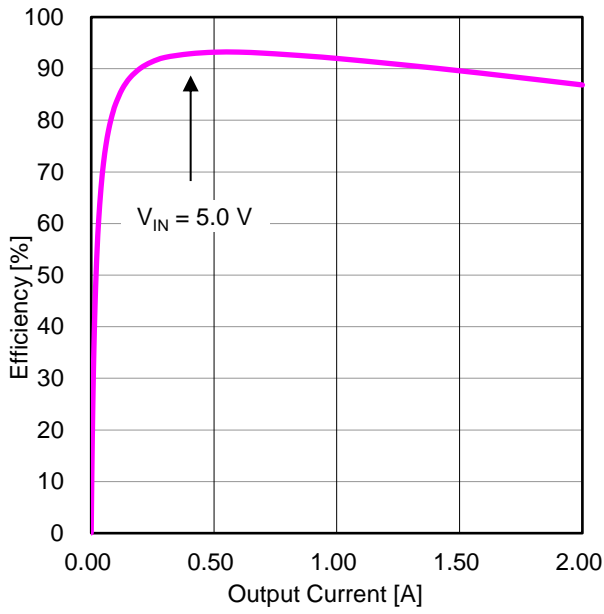


Figure 51. Efficiency vs Output Current



Figure 52. Frequency Characteristics ( $I_{OUT} = 0.5\text{ A}$ )

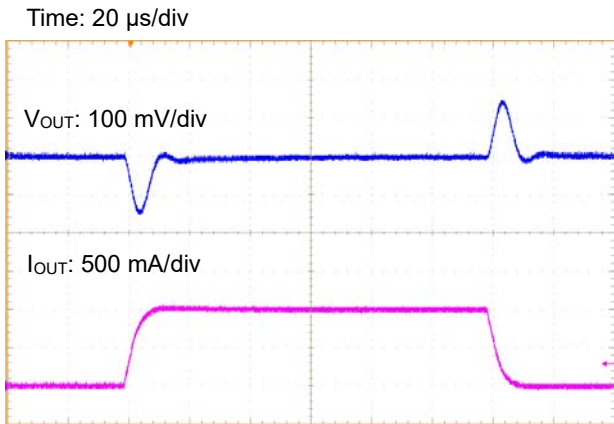


Figure 53. Load Transient Response ( $I_{OUT} = 0\text{ A} \leftrightarrow 1\text{ A}$ )

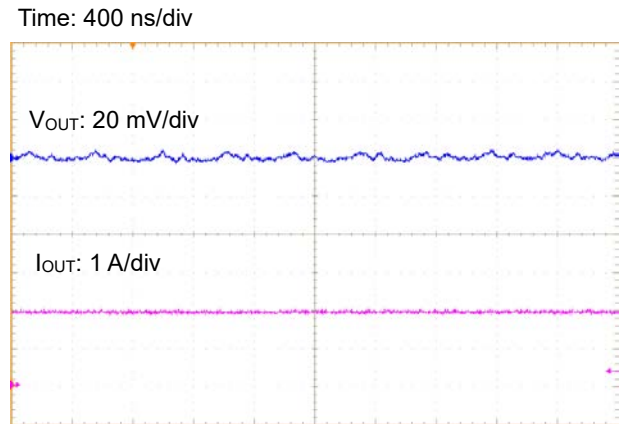


Figure 54. Output Ripple Voltage ( $I_{OUT} = 2\text{ A}$ )

PCB Layout Design

PCB layout design for DC/DC converter is very important. Appropriate layout can avoid various problems concerning power supply circuit. Figure 55 to 57 show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 55 is a current path when High Side Switch is ON and Low Side Switch is OFF, the Loop 2 in Figure 56 is when High Side Switch is OFF and Low Side Switch is ON. The thick line in Figure 57 shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element High Side and Low Side FET change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series "PCB Layout Techniques of Buck Converter".

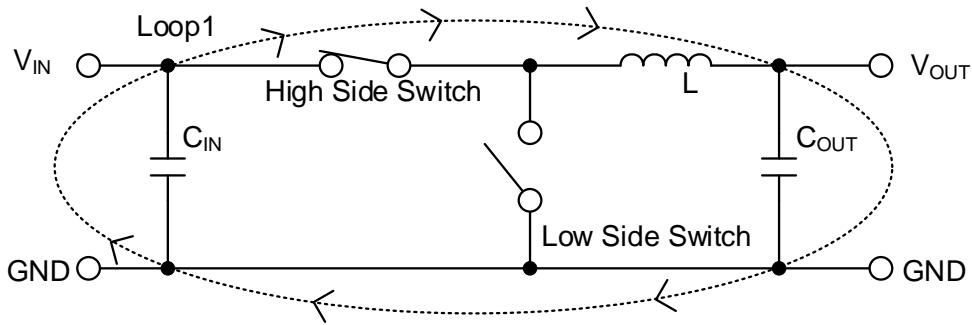


Figure 55. Current Path when High Side Switch = ON, Low Side Switch = OFF

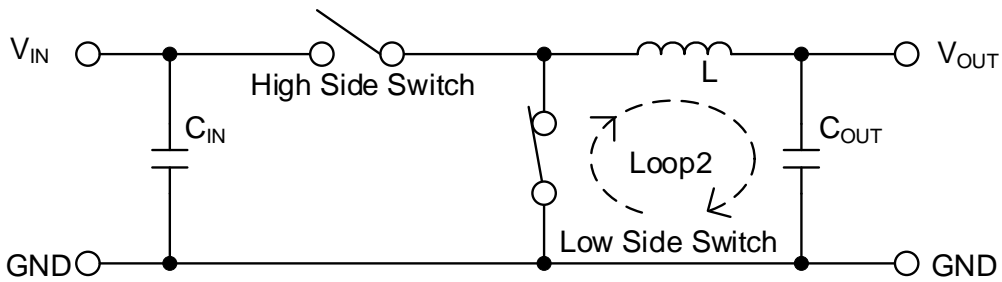


Figure 56. Current Path when High Side Switch = OFF, Low Side Switch = ON

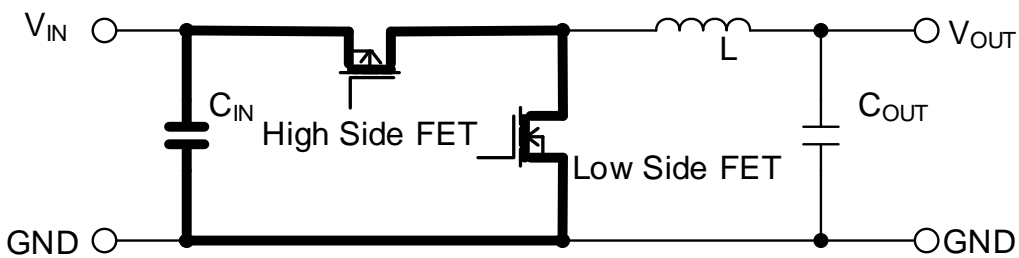
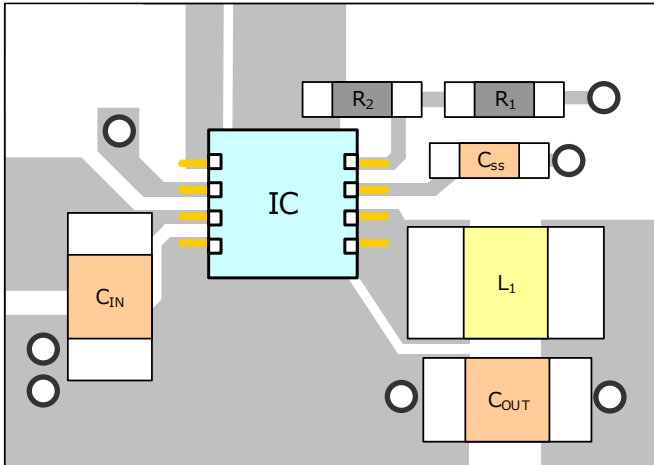


Figure 57. Difference of Current and Critical Area in Layout

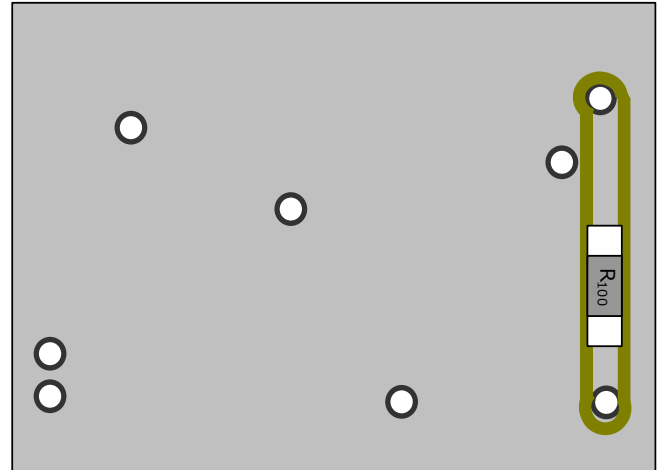
**PCB Layout Design – continued**

When designing the PCB layout, Pay extra attention to the following points.

- Connect the input capacitor  $C_{IN}$  as close as possible to the VIN pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern as thick and as short as possible.
- $R_1$  and  $R_2$  shall be located as close as possible to the FB pin and the wiring between  $R_1$  and  $R_2$  to the FB pin shall be as short as possible.
- Provide line connected to FB far from the SW nodes.
- $R_{100}$  is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into  $R_{100}$ , it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc.  $R_{100}$  is short-circuited for normal use.



Example of Evaluation Board Layout (Top View)



Example of Evaluation Board Layout (Bottom View)

Figure 58. Example of Evaluation Board Layout

**Power Dissipation**

For thermal design, be sure to operate the IC within the following conditions.  
 (Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature  $T_a$  is to be 125 °C or less.
2. The chip junction temperature  $T_j$  is to be 150 °C or less.

The chip junction temperature  $T_j$  can be considered in the following two patterns:

1. To obtain  $T_j$  from the package surface center temperature  $T_t$  in actual use

$$T_j = T_t + \psi_{JT} \times W \text{ [}^\circ\text{C]}$$

2. To obtain  $T_j$  from the ambient temperature  $T_a$

$$T_j = T_a + \theta_{JA} \times W \text{ [}^\circ\text{C]}$$

where:

$\psi_{JT}$  is junction to top characterization parameter ([Thermal Resistance](#)).

$\theta_{JA}$  is junction to ambient ([Thermal Resistance](#)).

The heat loss  $W$  of the IC can be obtained by the formula shown below:

$$W = R_{ONH} \times I_{OUT}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times I_{OUT}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{CC} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \text{ [W]}$$

where:

$R_{ONH}$  is the High Side FET ON Resistance ([Electrical Characteristics](#)) [ $\Omega$ ].

$R_{ONL}$  is the Low Side FET ON Resistance ([Electrical Characteristics](#)) [ $\Omega$ ].

$I_{OUT}$  is the Output Current [A].

$V_{OUT}$  is the Output Voltage [V].

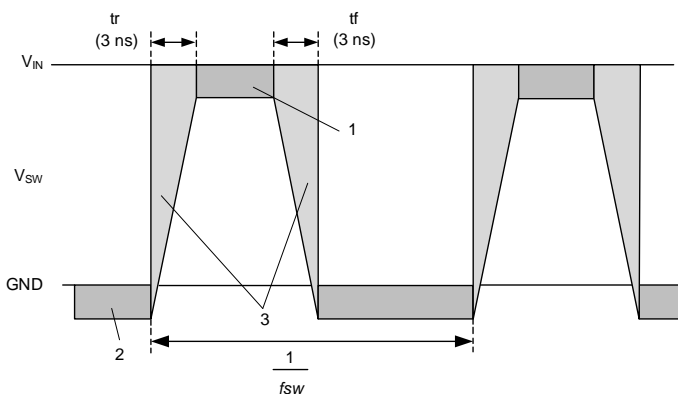
$V_{IN}$  is the Input Voltage [V].

$I_{CC}$  is the Circuit Current ([Electrical Characteristics](#)) [A].

$tr$  is the Switching Rise Time [s] (Typ:3 ns).

$tf$  is the Switching Fall Time [s] (Typ:3 ns).

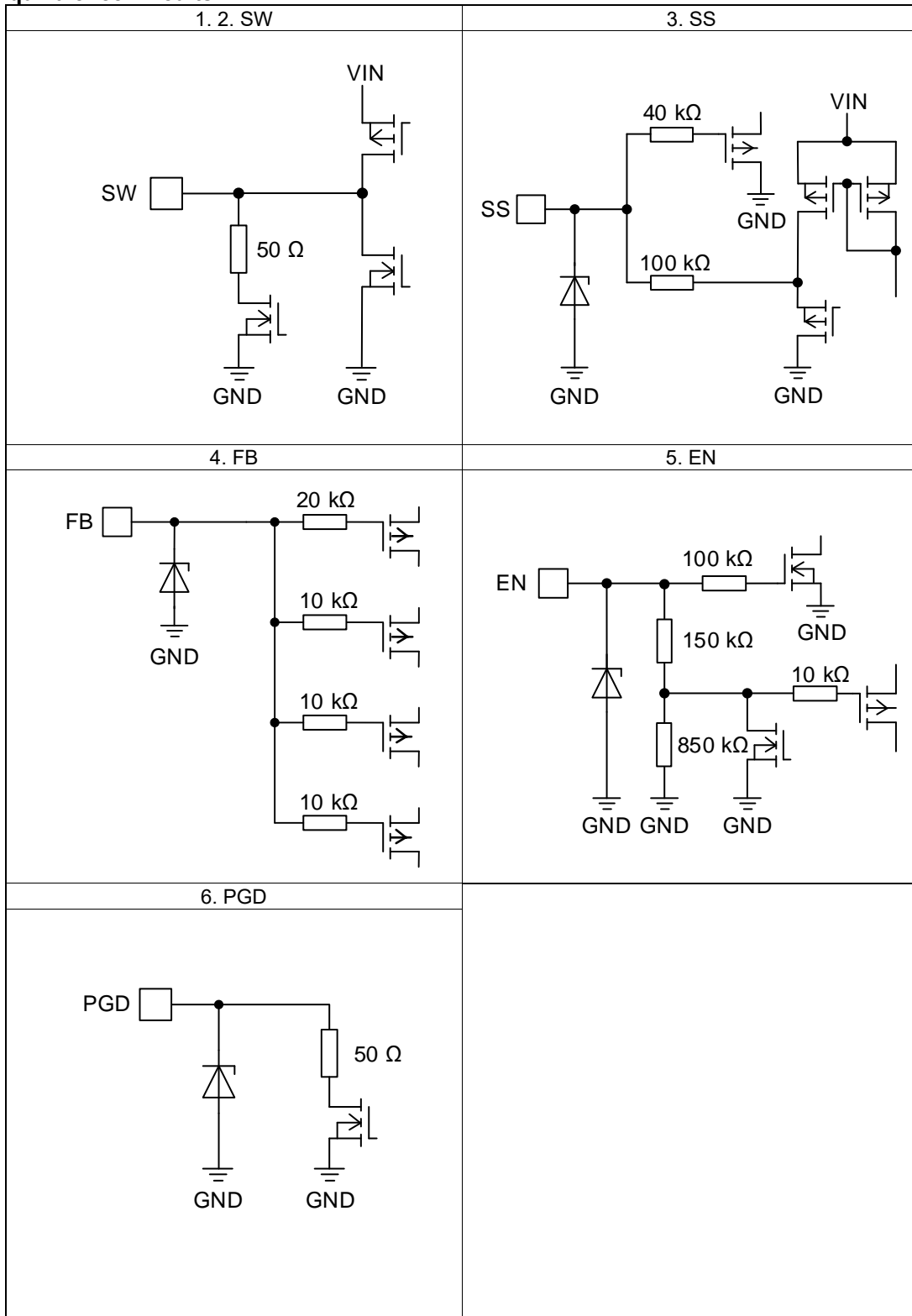
$f_{SW}$  is the Switching Frequency ([Electrical Characteristics](#)) [Hz].



1.  $R_{ONH} \times I_{OUT}^2$
2.  $R_{ONL} \times I_{OUT}^2$
3.  $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW}$

Figure 59. SW Waveform

I/O Equivalence Circuits (Note 1)



(Note 1) Resistance value is Typical.



## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes – continued

**10. Regarding the Input Pin of the IC**

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

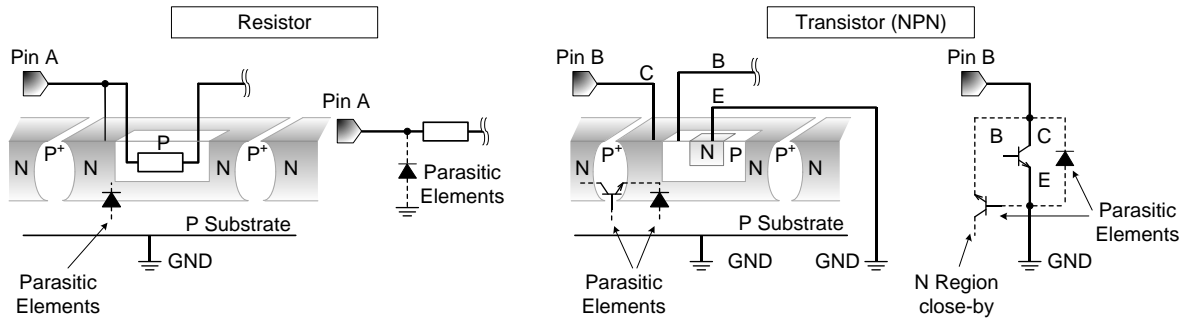


Figure 60. Example of Monolithic IC Structure

**11. Ceramic Capacitor**

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**12. Thermal Shutdown Circuit (TSD)**

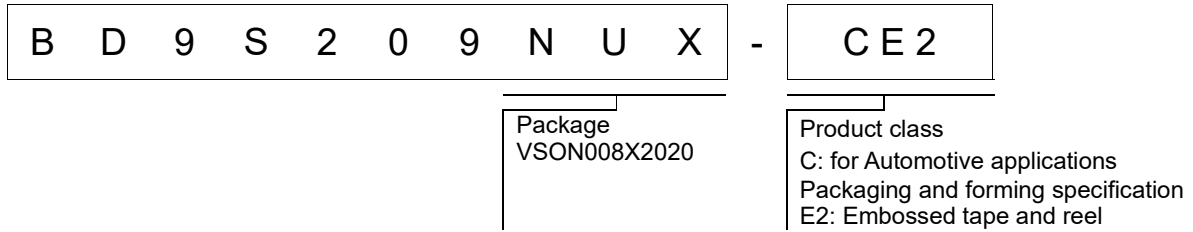
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

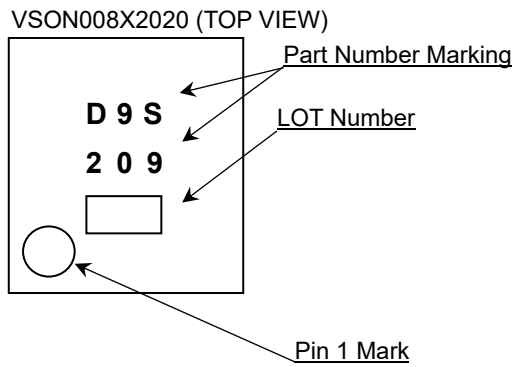
**13. Over Current Protection Circuit (OCP)**

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

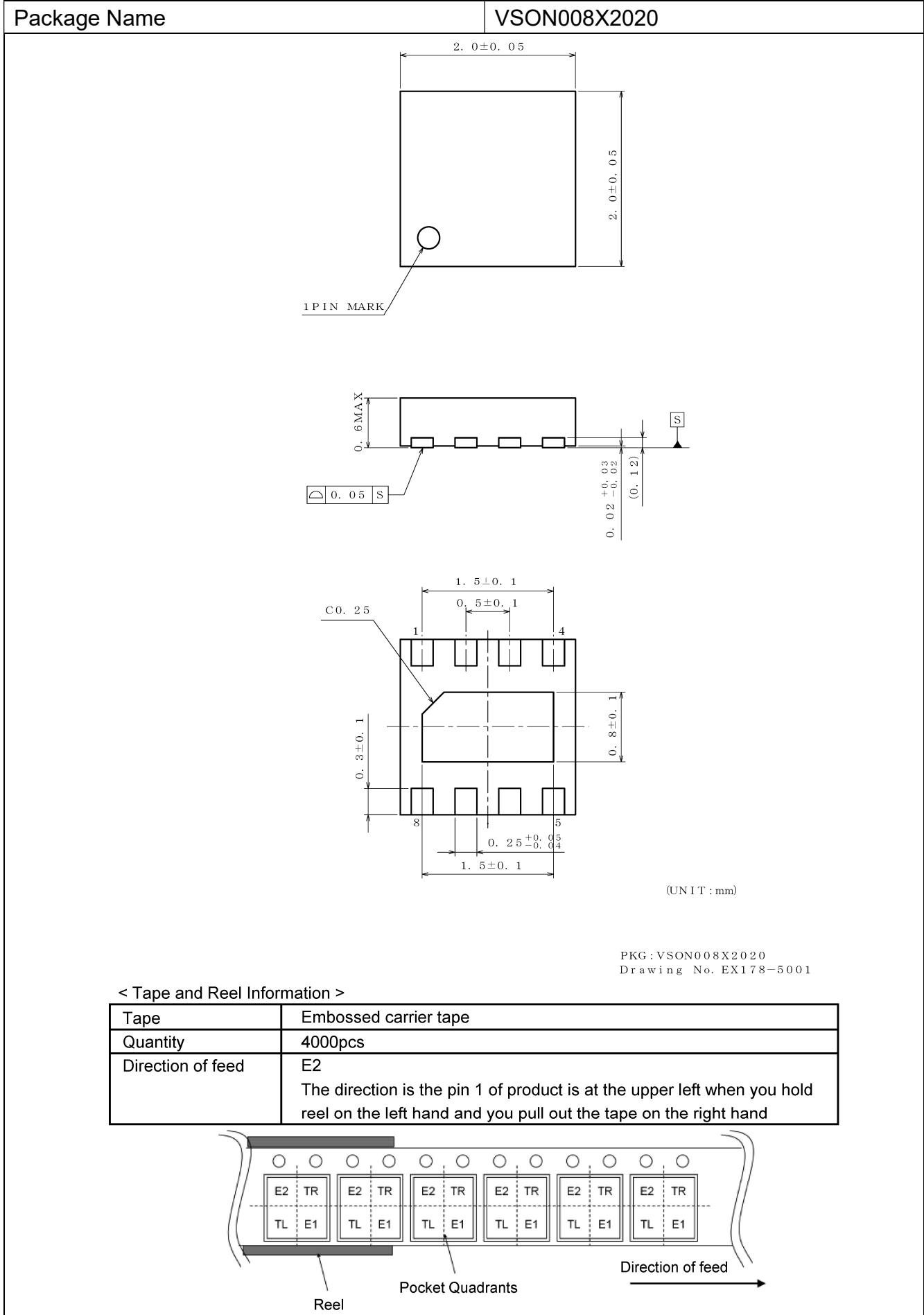
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
06.Apr.2022	001	New Release

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JAPAN	USA	EU	CHINA
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CLASS IV		CLASS III	

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  - [h] Use of the Products in places subject to dew condensation
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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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  - [d] the Products are exposed to high Electrostatic
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