

For Automotive 45 V Input 50 mA Fixed Output LDO Regulators

BD7xxL05G-C Series

General Description

The BD7xxL05G-C linear regulators are designed as low current consumption products for power supplies in various automotive applications.

These products are designed for up to 45 V absolute maximum supply voltage and operate until 50 mA output current with low current consumption of 6 μ A (Typ). It can regulate the output at a very high accuracy of ± 2 %.

This device features an integrated Over Current Protection to keep the device from a damage that is caused by short-circuit or overload. This product also integrates a Thermal Shutdown protection to avoid the damage from overheating.

Furthermore, low ESR ceramic capacitors are sufficiently applicable for the output phase compensation.

Applications

- Power Train
- Body
- Car Infotainment etc.

Key Specifications

- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Operating Input Voltage Range: 3 V to 45 V
- Low Current Consumption: 6 μ A (Typ)
- Output Current: 50 mA (Max)
- Output Voltage: 2.5 V / 3 V / 3.3 V / 5.0 V (Typ)
- High Output Voltage Accuracy: ± 2 %

Package

- | | |
|----------|-----------------------------|
| | W (Typ) x D (Typ) x H (Max) |
| ■ SSOP5: | 2.9 mm x 2.8 mm x 1.25 mm |

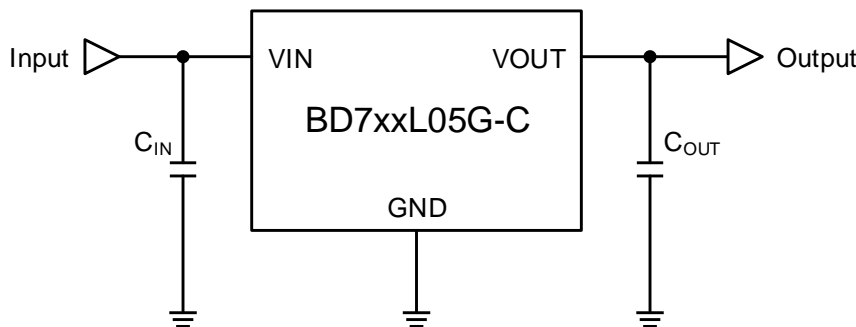


Features

- AEC-Q100 Qualified^(Note 1)
- Functional Safety Supportive Automotive Products
- Qualification Planned for Automotive Application
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)
(Note 1) Grade 1

Typical Application Circuit

- Components Externally Connected
Capacitor^(Note 2): $0.1 \mu\text{F} \leq C_{\text{IN}} (\text{Min})$, $0.5 \mu\text{F} \leq C_{\text{OUT}} (\text{Min})$
(Note 2) Electrolytic, tantalum, and ceramic capacitors can be used.



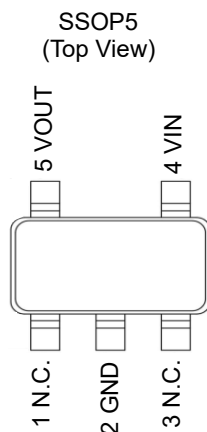
○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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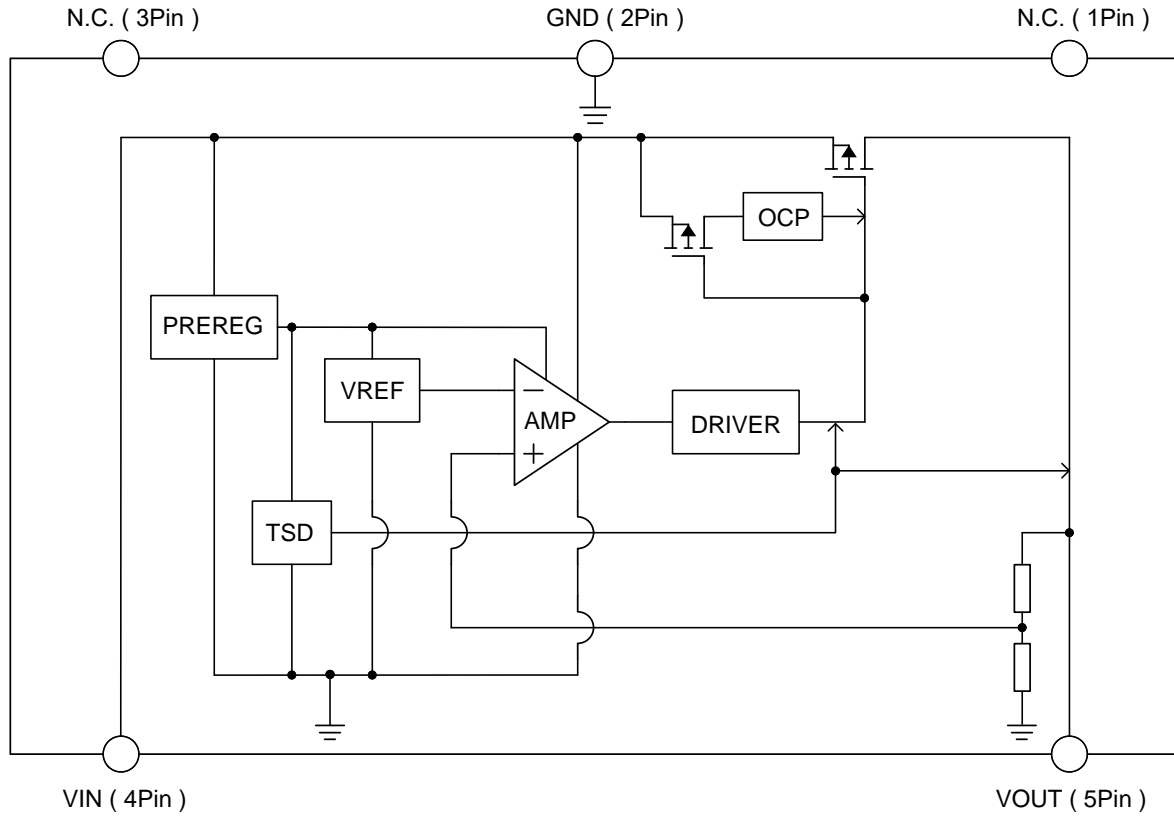
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function	Descriptions
1	N.C.	Not Connected	This pin is not connected to the chip. It can kept open or it's also possible to connect to GND.
2	GND	Ground Pin	This is the Ground pin. It should be connected to the lowest potential.
3	N.C.	Not Connected	This pin is not connected to the chip. It can kept open or it's also possible to connect to GND.
4	VIN	Supply Voltage Input Pin	This pin supplies the input voltage. It is necessary to connect a capacitor which is 0.1 μF (Min) or higher between VIN pin and GND. The detailed selecting guide is described in Selection of External Components .
5	VOUT	Output Pin	This pin outputs the voltage setting. It is necessary to connect a capacitor which is 0.5 μF (Min) or higher between the VOUT pin and GND. The detailed selecting guide is described in Selection of External Components .

Block Diagram



Description of Blocks

Block Name	Function	Description of Blocks
PREREG	Internal Power Supply	Provides Power Supply for the Internal Circuit.
TSD	Thermal Shutdown	In case maximum power dissipation is exceeded or the ambient temperature is higher than the Maximum Junction Temperature, overheating causes the chip temperature (T _J) to rise. The TSD protection circuit detects this and forces the output to turn off in order to protect the device from overheating. When the junction temperature decreases, the output turns on automatically. Output pin is discharged when the TSD protection circuit is operating.
VREF	Reference Voltage	Generates the Reference Voltage.
AMP	Error Amplifier	The Error Amplifier amplifies the difference between the divided feedback voltage and the reference voltage, and then it regulates Output Power Tr. via the DRIVER.
DRIVER	Output MOSFET Driver	Drives the Output MOSFET (Power Tr.).
OCP	Over Current Protection	If the output current increases higher than the maximum Output Current, it will be limited by the Over Current Protection in order to protect the device from damage that will be caused by over current. At this operating condition, the output voltage may decrease because the output current is limited. If an abnormal state is removed, and the output current value returns normally, the output voltage will also return to normal state.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Input Supply Voltage ^(Note 1)	V _{IN}	-0.3 to +45	V
Output Voltage ^(Note 2)	V _{OUT}	-0.3 to +18	V
Junction Temperature Range	T _j	-40 to +150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Maximum Junction Temperature	T _{jmax}	150	°C
ESD Withstand Voltage (HBM) ^(Note 3)	V _{ESD_HBM}	± 2000	V
ESD Withstand Voltage (CDM) ^(Note 4)	V _{ESD_CDM}	± 750	V

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance and power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Do not exceed T_{jmax}.

(Note 2) Do not exceed V_{IN} + 0.3 V.

(Note 3) ESD susceptibility Human Body Model "HBM"; base on ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).

(Note 4) ESD susceptibility Charged Device Model "CDM"; base on JEDEC JESD22-C101.

Thermal Resistance^(Note 6)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 8)	2s2p ^(Note 9)	
SSOP5				
Junction to Ambient	θ _{JA}	247.3	155.5	°C/W
Junction to Top Characterization Parameter ^(Note 7)	Ψ _{JT}	43	33	°C/W

(Note 6) Based on JESD51-2A (Still-Air). Using BD750L05G-C Chips.

(Note 7) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 8) Using a PCB board based on JESD51-3.

(Note 9) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Operating Conditions

Parameter		Symbol	Min	Max	Unit
Input Supply Voltage ^(Note 1) ($I_{OUT} \leq 50$ mA)	BD725L05G-C / BD730L05G-C	V_{IN}	3.5	42.0	V
	BD733L05G-C	V_{IN}	3.8	42.0	V
	BD750L05G-C	V_{IN}	5.6	42.0	V
Start-up Voltage ^(Note 2)		$V_{IN \text{ Start-up}}$	3	-	V
Output Current		I_{OUT}	0	50	mA
Input Capacitor ^(Note 3)		C_{IN}	0.1	-	μF
Output Capacitor ^(Note 4)		C_{OUT}	0.5	1000	μF
Output Capacitor Equivalent Series Resistance ^(Note 5)		ESR (C_{OUT})	-	100	Ω
Operating Temperature		T_a	-40	+125	$^{\circ}\text{C}$

(Note 1) Minimum Input Supply Voltage must be $V_{IN \text{ Start-up}} = 3$ V or more.

Consider that the output voltage would be reduced (Dropout Voltage) by the output current.

(Note 2) When $I_{OUT} = 0$ mA

(Note 3) If the inductance of power supply line is high, adjust input capacitor value.

(Note 4) Set the value of the capacitor so that it does not fall below the minimum value. Take into consideration the temperature characteristics and DC device characteristics.

(Note 5) Refer to [Selection of External Components](#) and select the parts.

Electrical Characteristics

Unless otherwise specified, $T_j = -40\text{ }^\circ\text{C}$ to $+150\text{ }^\circ\text{C}$, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$

Typical values are defined at $T_j = 25\text{ }^\circ\text{C}$, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$.

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Circuit Current	I_{CC}	-	6	9	μA	$I_{OUT} = 0\text{ mA}$ $T_j \leq +25\text{ }^\circ\text{C}$
		-	6	12	μA	$I_{OUT} = 0\text{ mA}$ $T_j \leq +105\text{ }^\circ\text{C}$
		-	6	13	μA	$I_{OUT} = 0\text{ mA}$ $T_j \leq +125\text{ }^\circ\text{C}$
		-	6	15	μA	$I_{OUT} \leq 50\text{ mA}$ $T_j \leq +150\text{ }^\circ\text{C}$
Output Voltage Accuracy	ΔV_{OUT}	-2	-	+2	%	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 42\text{ V}$ $100\text{ }\mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$
		-2	-	+2	%	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 42\text{ V}$ $I_{OUT} \leq 100\text{ }\mu\text{A}$ $T_j \leq +125\text{ }^\circ\text{C}$
Dropout Voltage ^(Note 1) (BD730L05G-C / BD733L05G-C)	ΔV_d	-	100	200	mV	$V_{IN} = V_{OUT} \times 0.95 (= 2.85\text{ V} / 3.135\text{ V})$ $I_{OUT} = 0.1\text{ mA}$
		-	180	280	mV	$V_{IN} = V_{OUT} \times 0.95 (= 2.85\text{ V} / 3.135\text{ V})$ $I_{OUT} = 20\text{ mA}$
		-	300	400	mV	$V_{IN} = V_{OUT} \times 0.95 (= 2.85\text{ V} / 3.135\text{ V})$ $I_{OUT} = 50\text{ mA}$
Dropout Voltage (BD750L05G-C)	ΔV_d	-	200	350	mV	$V_{IN} = V_{OUT} \times 0.95 (= 4.75\text{ V})$ $I_{OUT} = 0.1\text{ mA}$
		-	260	410	mV	$V_{IN} = V_{OUT} \times 0.95 (= 4.75\text{ V})$ $I_{OUT} = 20\text{ mA}$
		-	350	500	mV	$V_{IN} = V_{OUT} \times 0.95 (= 4.75\text{ V})$ $I_{OUT} = 50\text{ mA}$
Ripple Rejection	R.R.	55	60	-	dB	$f = 120\text{ Hz}$ $V_{ripple} = 1\text{ V}_{rms}$ $I_{OUT} = 50\text{ mA}$
Line Regulation	Reg.I	-	0.1	0.6	$\% \times V_{OUT}$	$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 42\text{ V}$
Load Regulation	Reg.L	-	0.1	0.6	$\% \times V_{OUT}$	$100\text{ }\mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$
Thermal Shutdown	TSD	151	175	-	$^\circ\text{C}$	T_j at TSD ON
Over Current Protection	I_{OCP}	51	120	-	mA	

(Note 1) Minimum Input Supply Voltage of BD725L05G-C must be $V_{IN\text{ Start-up}} = 3\text{ V}$ or more.

Typical Performance Curves (BD725L05G-C)

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

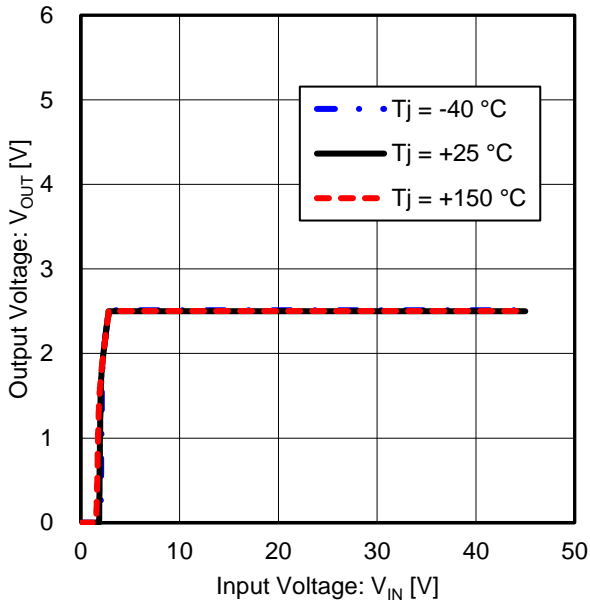


Figure 1. Output Voltage vs Input Voltage

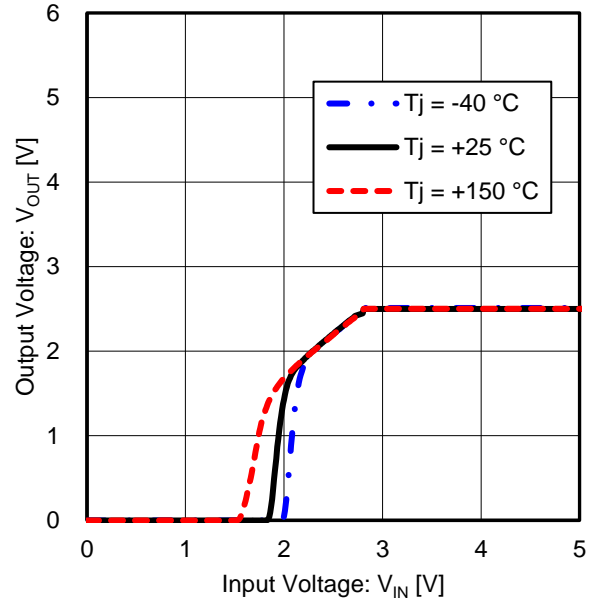


Figure 2. Output Voltage vs Input Voltage - Enlarged view

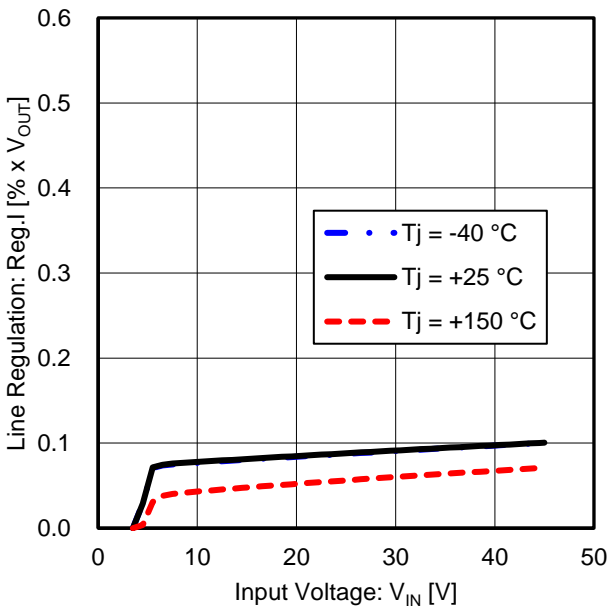


Figure 3. Line Regulation vs Input Voltage ($V_{IN} = 3.5\text{ V to }45\text{ V}$)

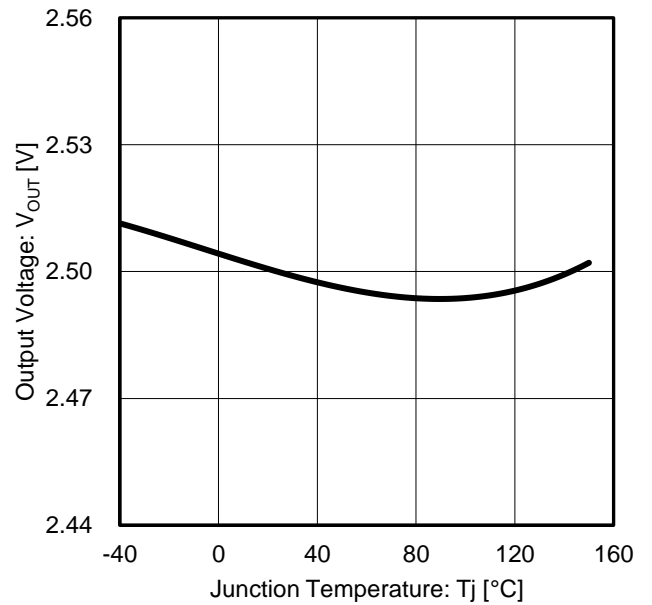


Figure 4. Output Voltage vs Junction Temperature

Typical Performance Curves (BD725L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

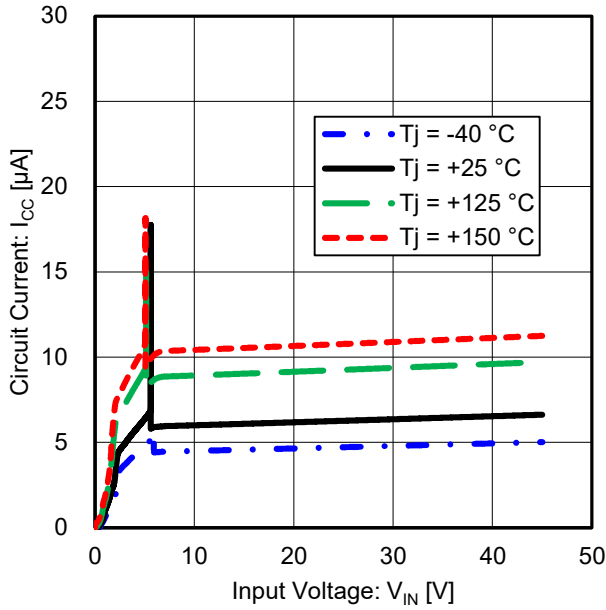


Figure 5. Circuit Current vs Input Voltage ($I_{OUT} = 0\text{ mA}$)

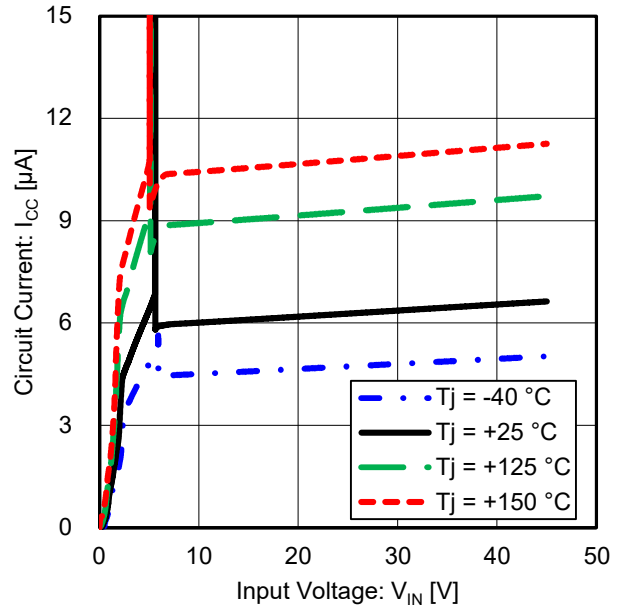


Figure 6. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 0\text{ mA}$)

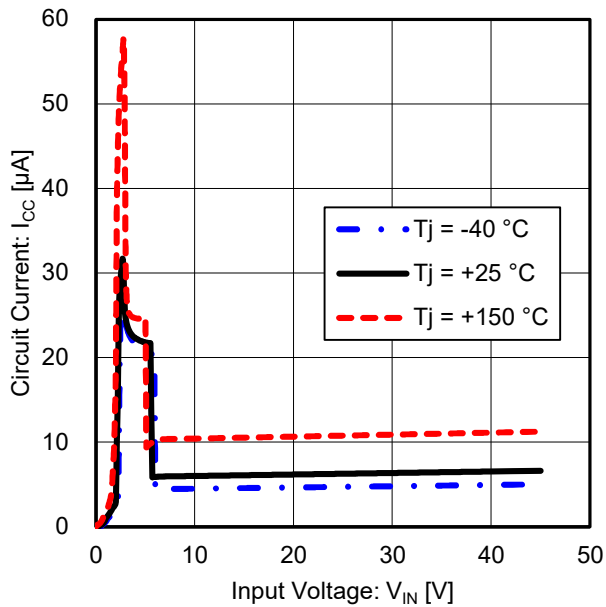


Figure 7. Circuit Current vs Input Voltage ($I_{OUT} = 50\text{ mA}$)

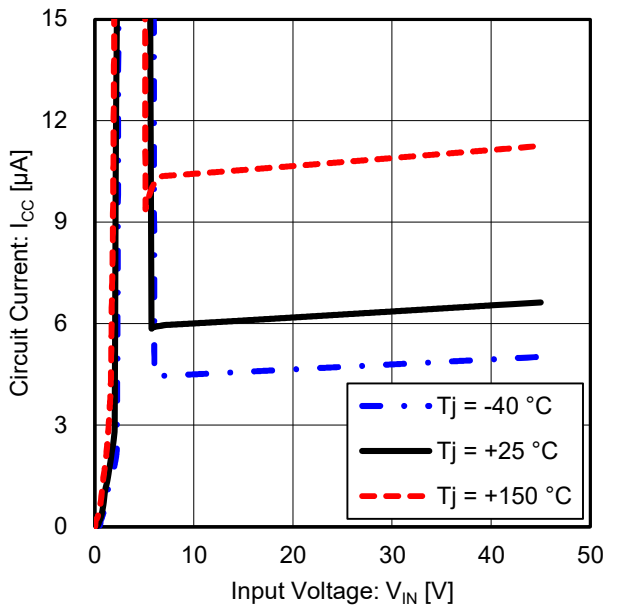


Figure 8. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 50\text{ mA}$)

Typical Performance Curves (BD725L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

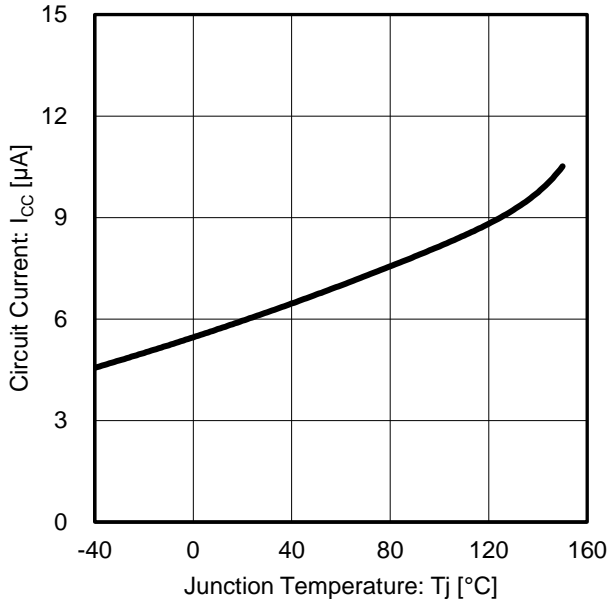


Figure 9. Circuit Current vs Junction Temperature ($I_{OUT} = 0\text{ mA}$)

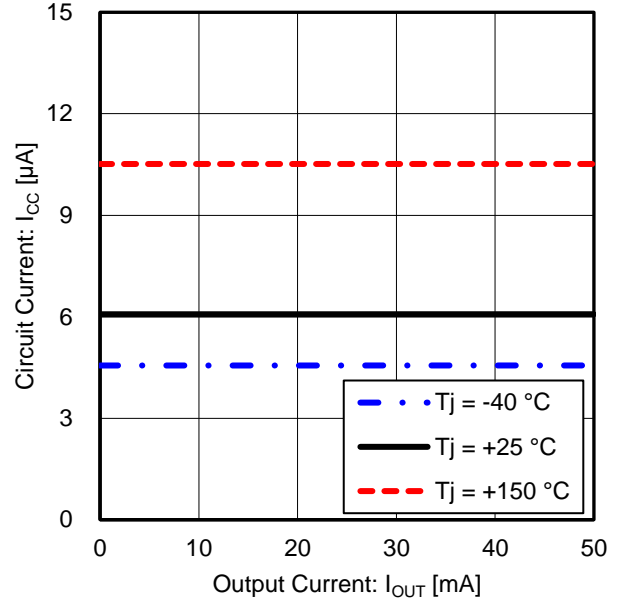


Figure 10. Circuit Current vs Output Current

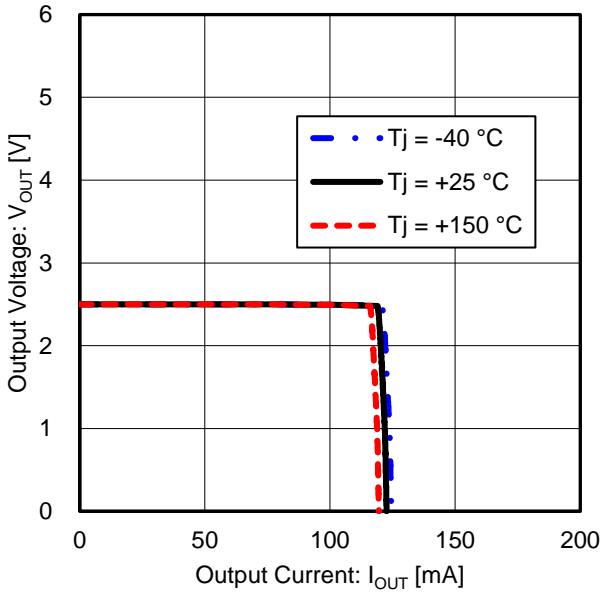


Figure 11. Output Voltage vs Output Current (Over Current Protection)

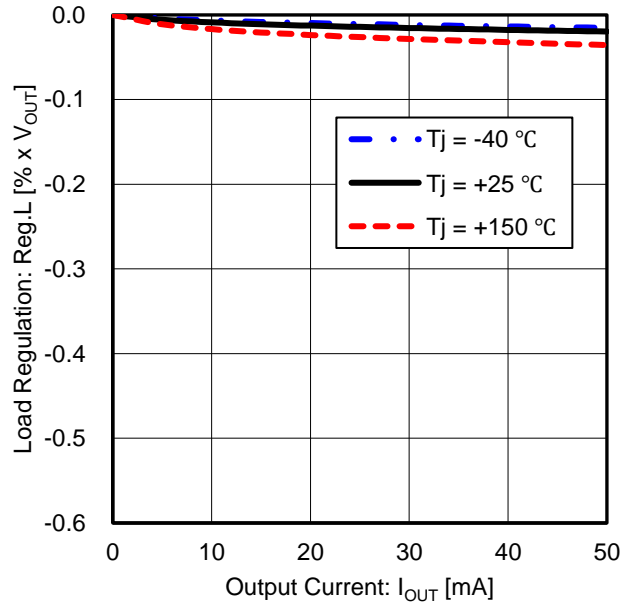


Figure 12. Load Regulation vs Output Current ($I_{OUT} = 100\text{ }\mu\text{A}$ to 50 mA)

Typical Performance Curves (BD725L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

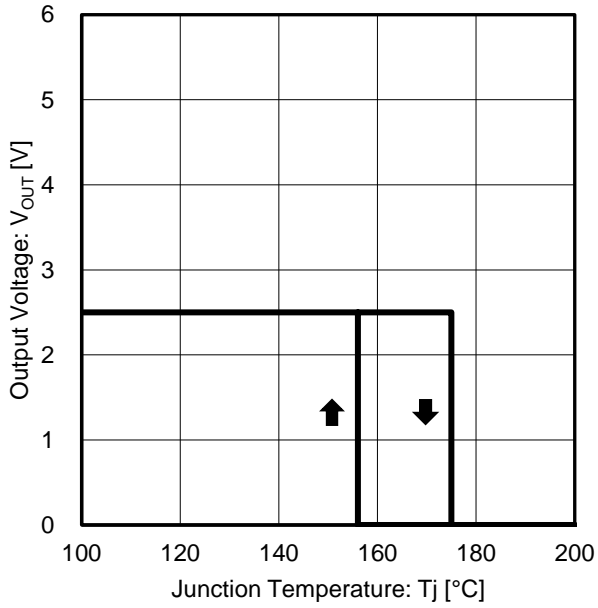


Figure 13. Output Voltage vs Junction Temperature (Thermal Shutdown Protection)

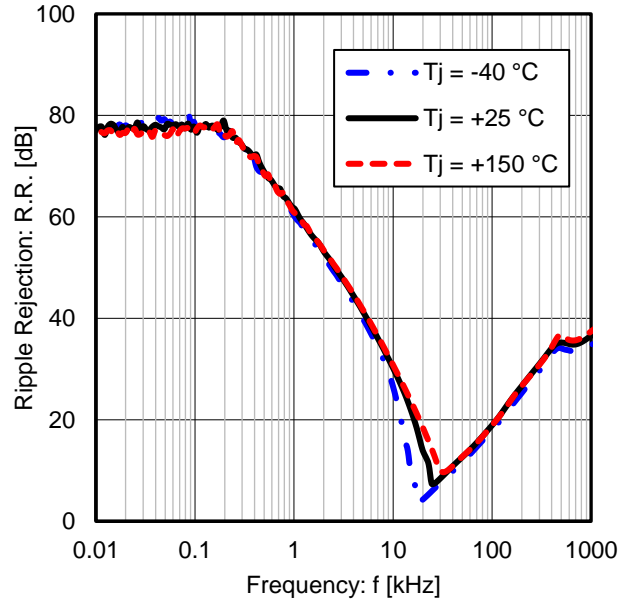


Figure 14. Ripple Rejection vs Frequency ($I_{OUT} = 50\text{ mA}$)

Typical Performance Curves (BD730L05G-C)

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

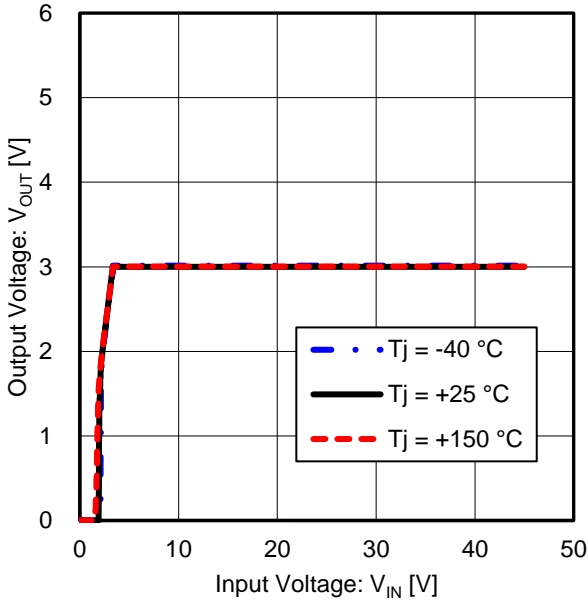


Figure 15. Output Voltage vs Input Voltage

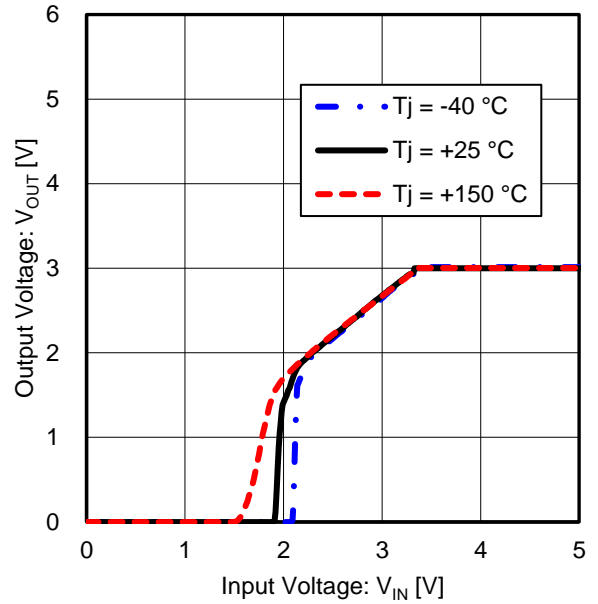


Figure 16. Output Voltage vs Input Voltage - Enlarged view

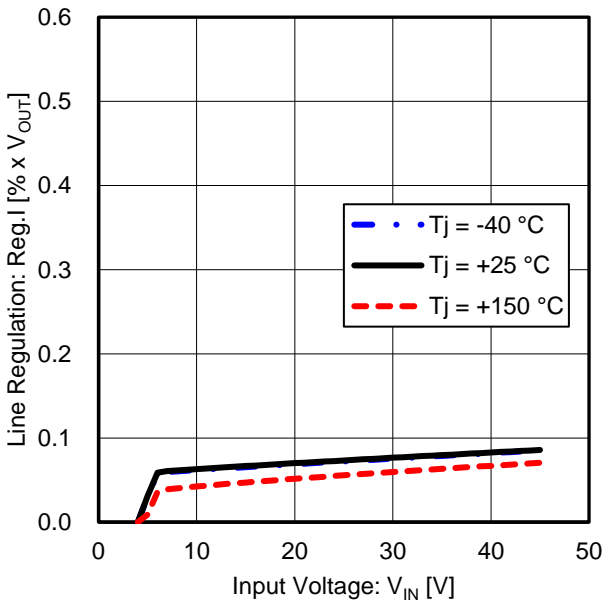


Figure 17. Line Regulation vs Input Voltage ($V_{IN} = 4\text{ V to }45\text{ V}$)

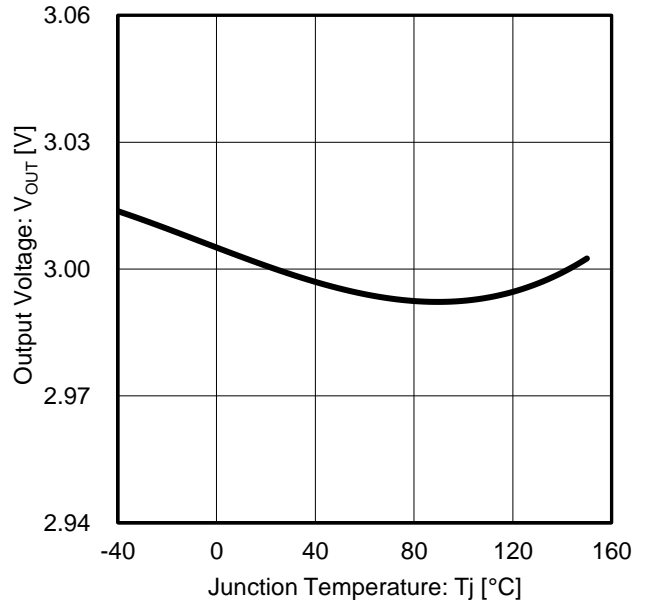


Figure 18. Output Voltage vs Junction Temperature

Typical Performance Curves (BD730L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

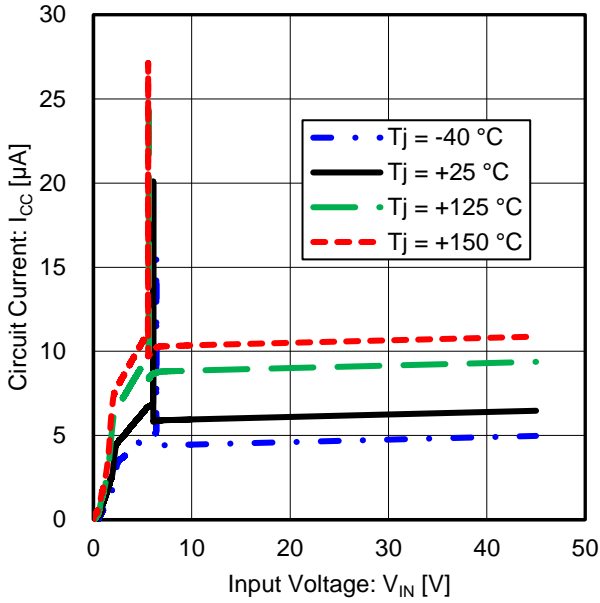


Figure 19. Circuit Current vs Input Voltage ($I_{OUT} = 0\text{ mA}$)

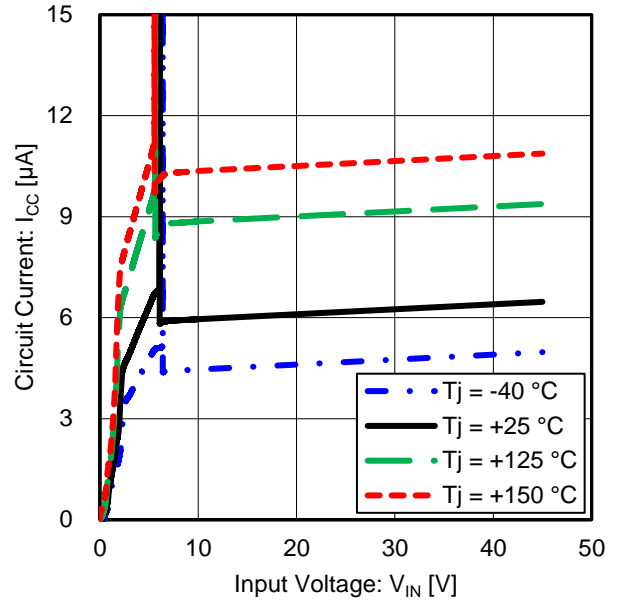


Figure 20. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 0\text{ mA}$)

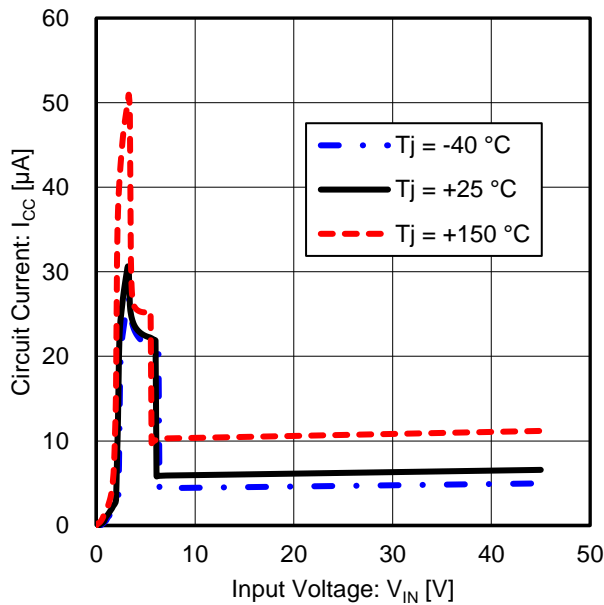


Figure 21. Circuit Current vs Input Voltage ($I_{OUT} = 50\text{ mA}$)

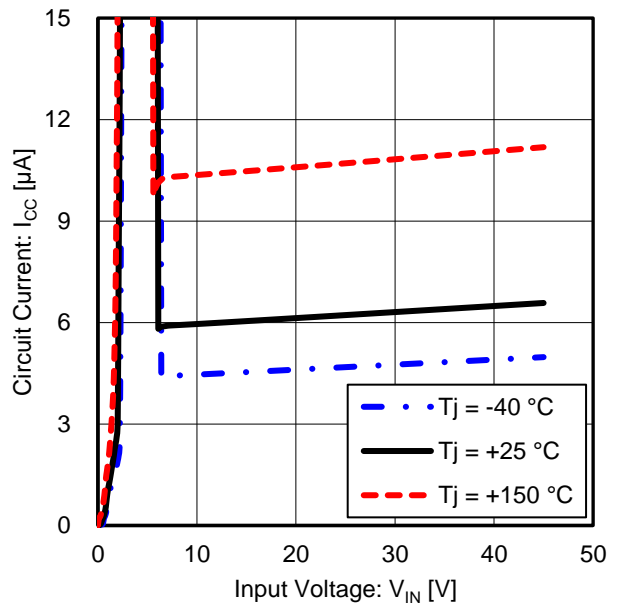


Figure 22. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 50\text{ mA}$)

Typical Performance Curves (BD730L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

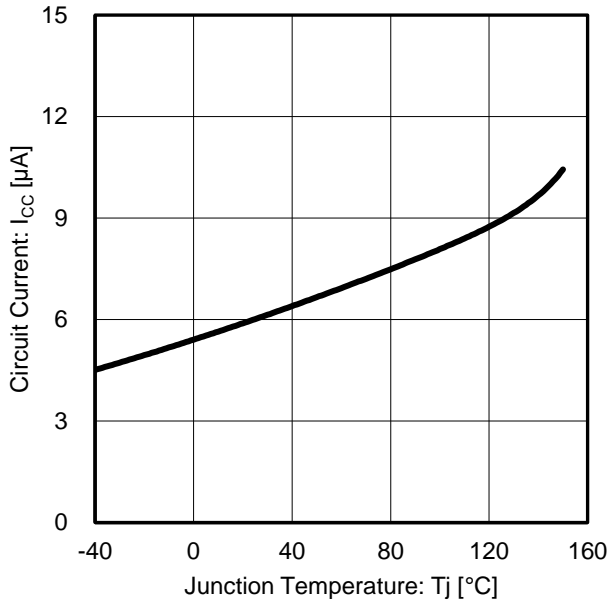


Figure 23. Circuit Current vs Junction Temperature ($I_{OUT} = 0\text{ mA}$)

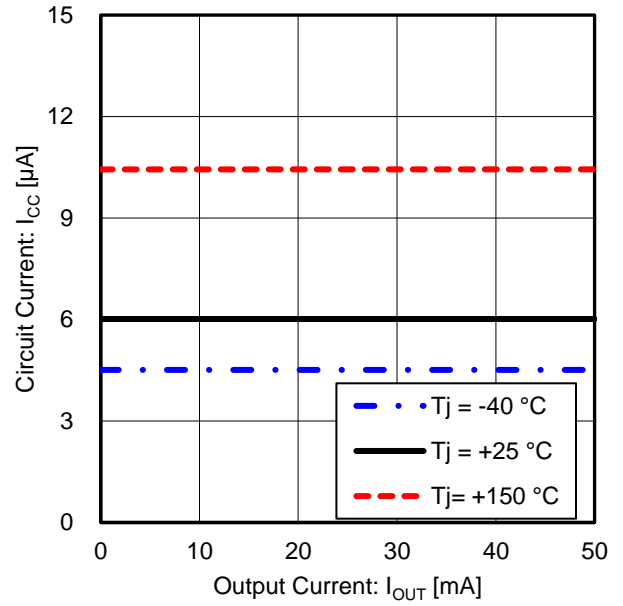


Figure 24. Circuit Current vs Output Current

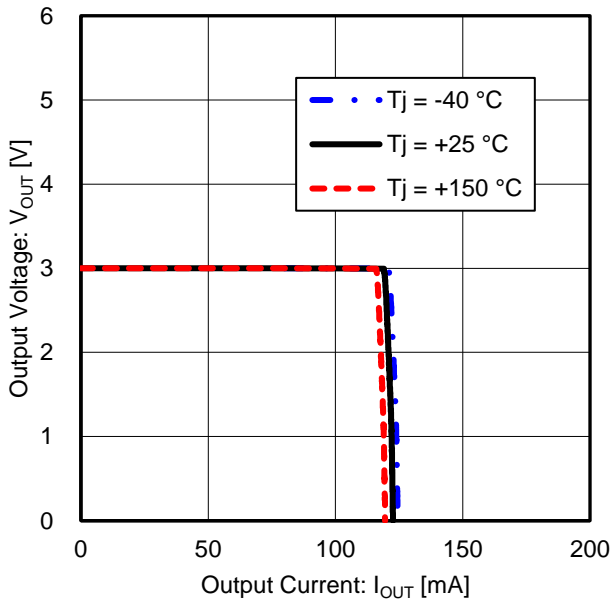


Figure 25. Output Voltage vs Output Current (Over Current Protection)

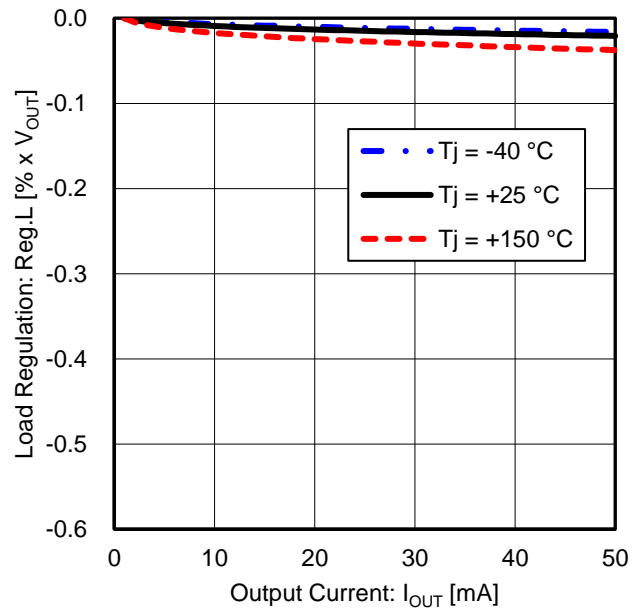


Figure 26. Load Regulation vs Output Current ($I_{OUT} = 100\text{ }\mu\text{A}$ to 50 mA)

Typical Performance Curves (BD730L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

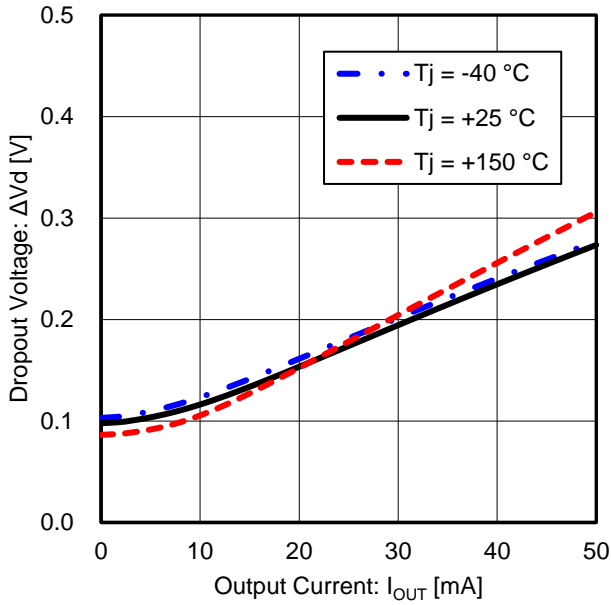


Figure 27. Dropout Voltage vs Output Current
($V_{IN} = V_{OUT} \times 0.95 = 2.85\text{ V}$)

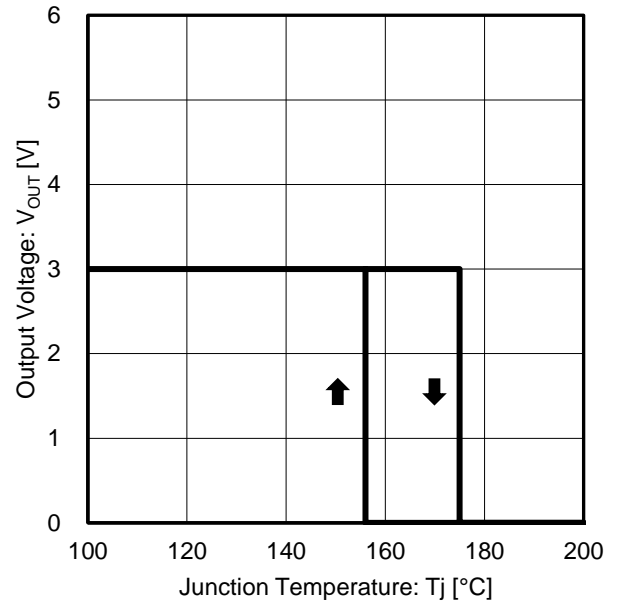


Figure 28. Output Voltage vs Junction Temperature
(Thermal Shutdown Protection)

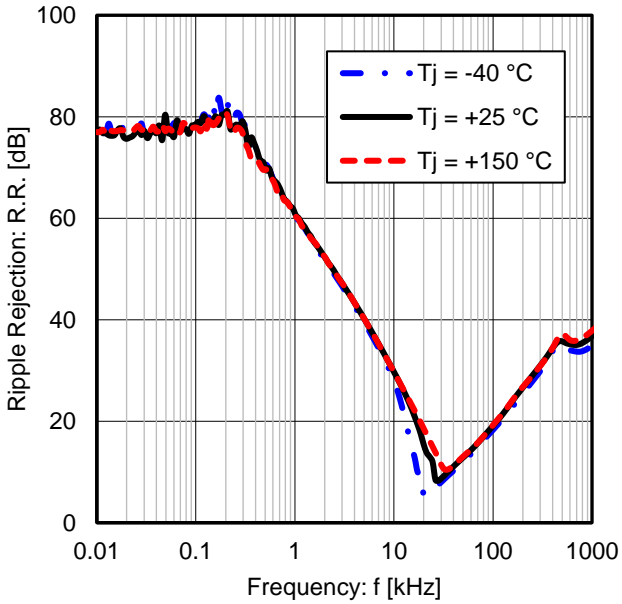


Figure 29. Ripple Rejection vs Frequency
($I_{OUT} = 50\text{ mA}$)

Typical Performance Curves (BD733L05G-C)

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

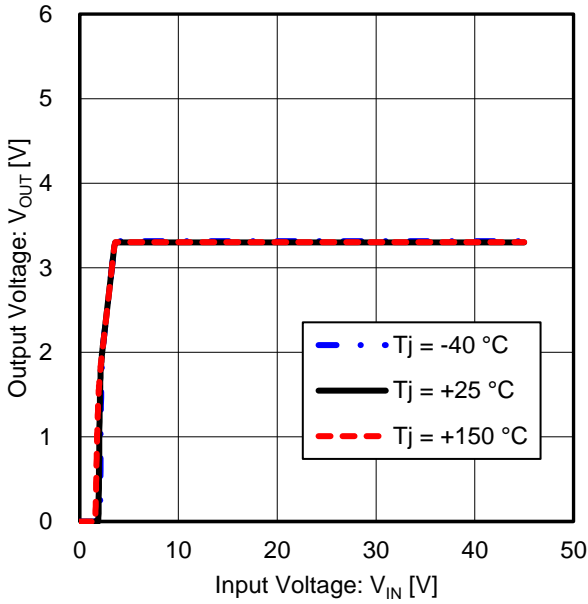


Figure 30. Output Voltage vs Input Voltage

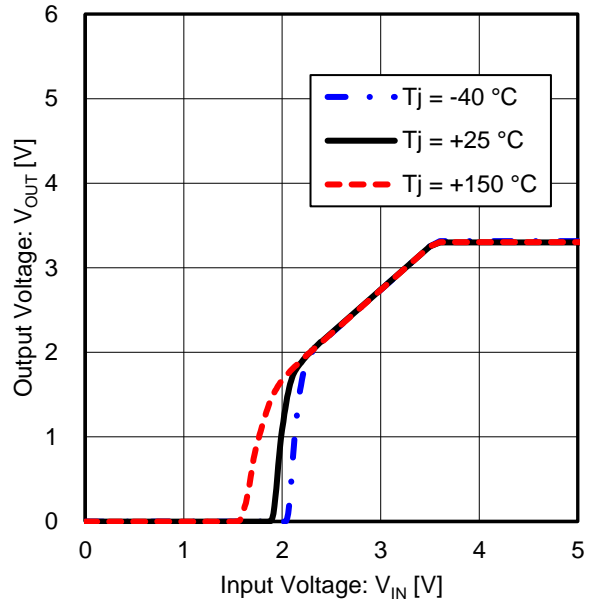


Figure 31. Output Voltage vs Input Voltage - Enlarged view

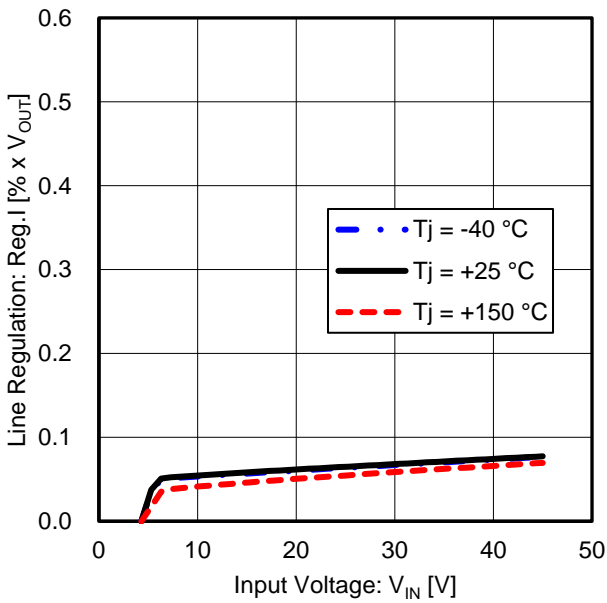


Figure 32. Line Regulation vs Input Voltage ($V_{IN} = 4.3\text{ V to }45\text{ V}$)

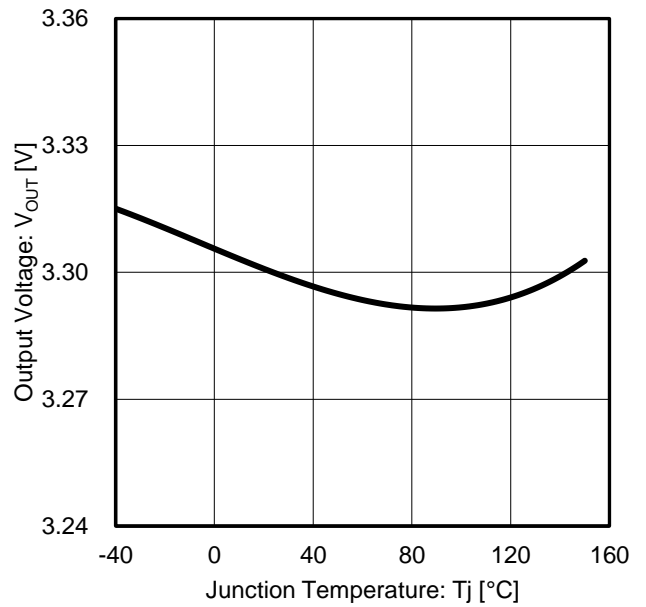


Figure 33. Output Voltage vs Junction Temperature

Typical Performance Curves (BD733L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

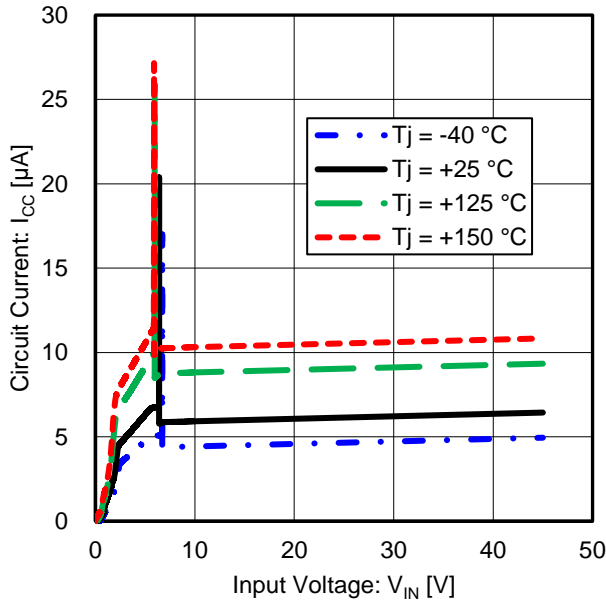


Figure 34. Circuit Current vs Input Voltage ($I_{OUT} = 0\text{ mA}$)

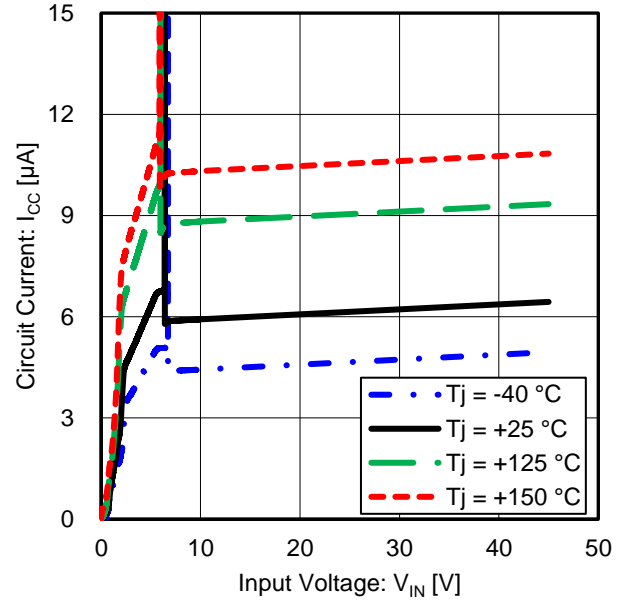


Figure 35. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 0\text{ mA}$)

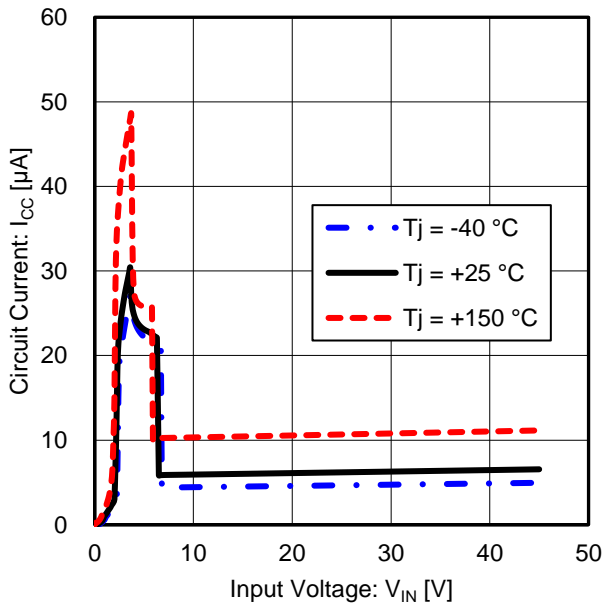


Figure 36. Circuit Current vs Input Voltage ($I_{OUT} = 50\text{ mA}$)

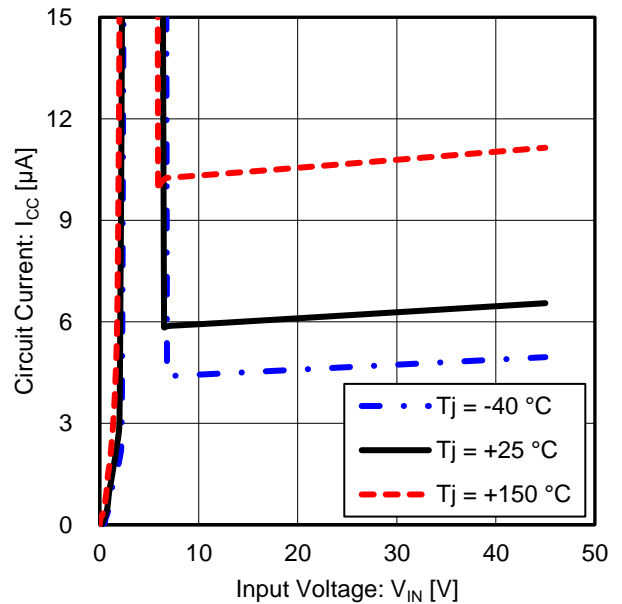


Figure 37. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 50\text{ mA}$)

Typical Performance Curves (BD733L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

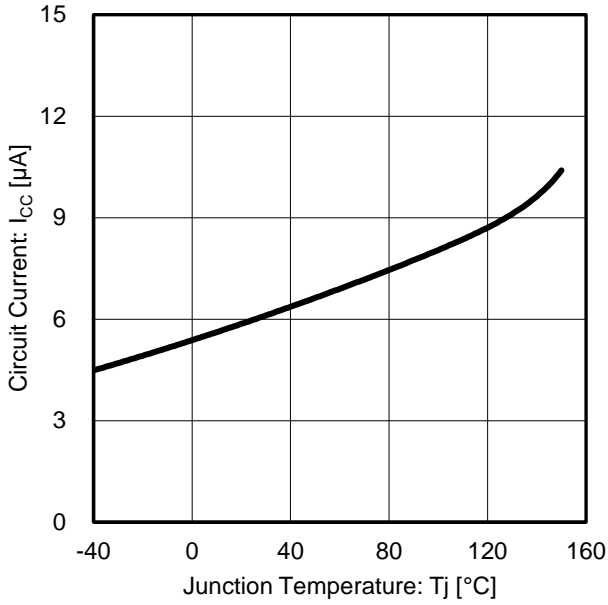


Figure 38. Circuit Current vs Junction Temperature ($I_{OUT} = 0\text{ mA}$)

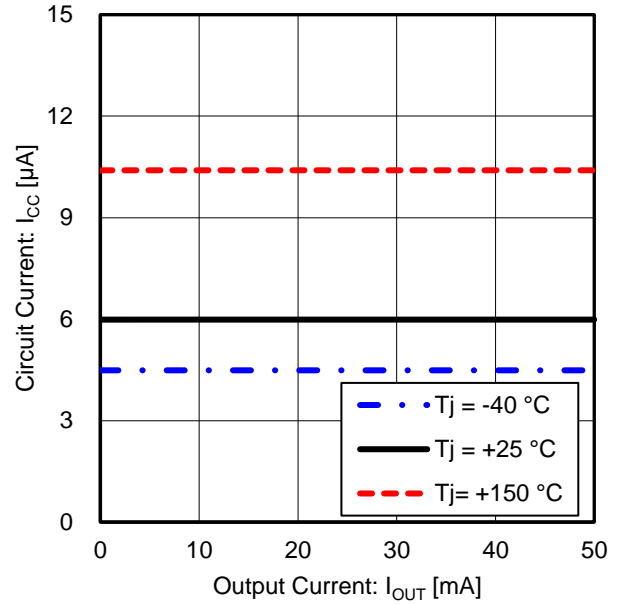


Figure 39. Circuit Current vs Output Current ($I_{OUT} = 0\text{ mA}$)

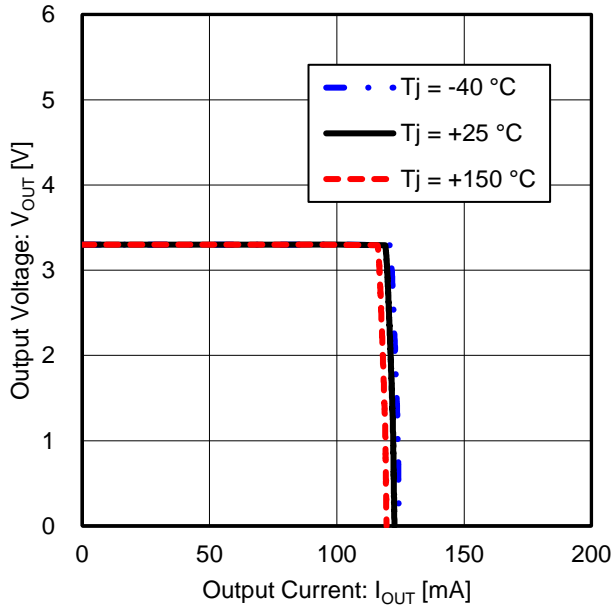


Figure 40. Output Voltage vs Output Current (Over Current Protection)

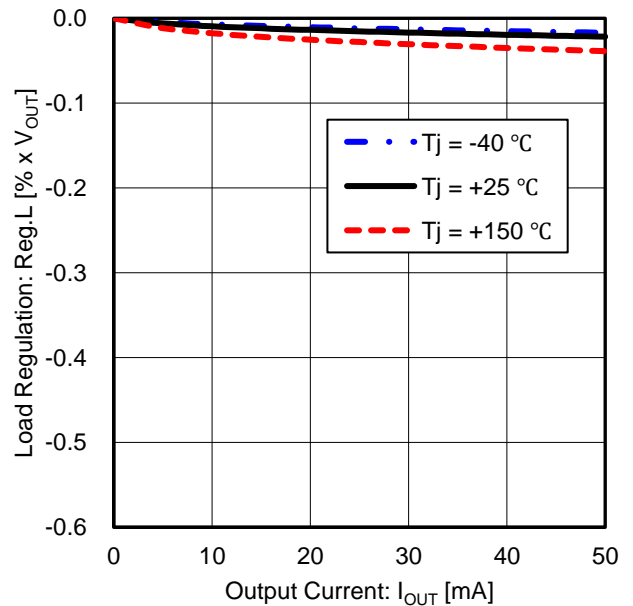


Figure 41. Load Regulation vs Output Current ($I_{OUT} = 100\text{ }\mu\text{A}$ to 50 mA)

Typical Performance Curves (BD733L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

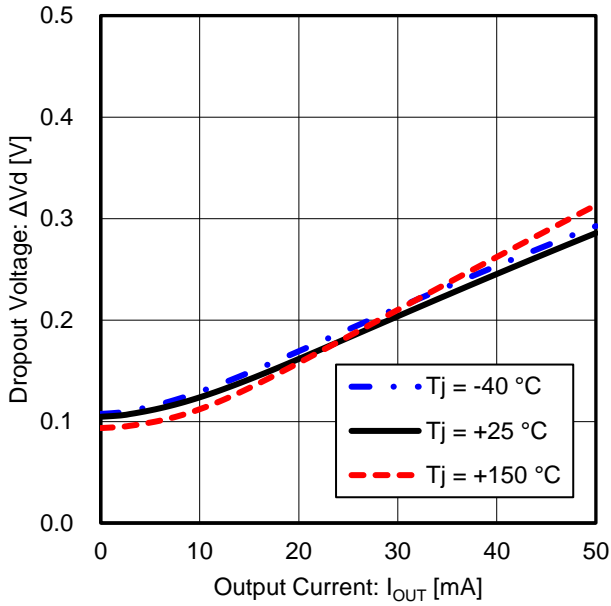


Figure 42. Dropout Voltage vs Output Current
($V_{IN} = V_{OUT} \times 0.95\text{ V} = 3.135\text{ V}$)

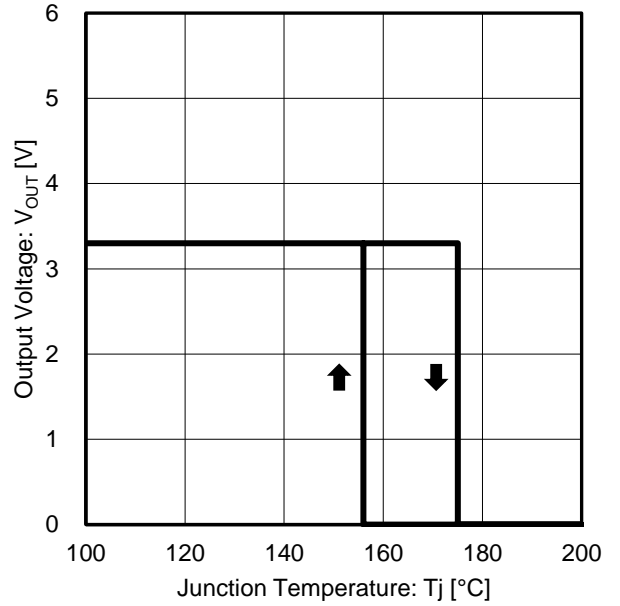


Figure 43. Output Voltage vs Junction Temperature
(Thermal Shutdown Protection)

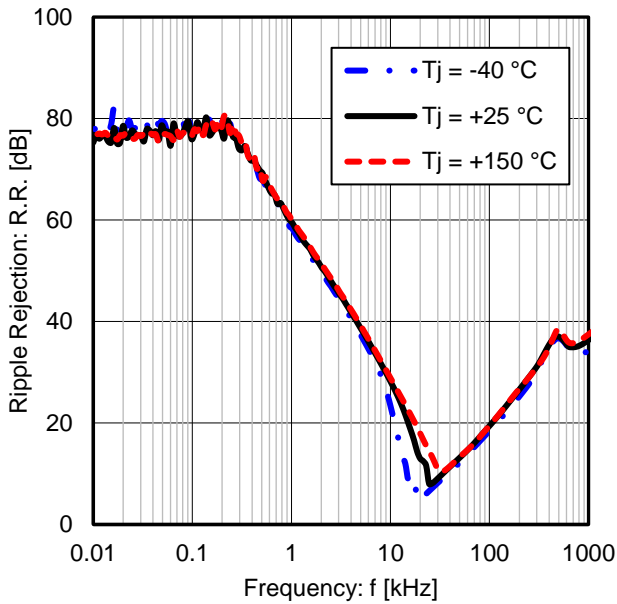


Figure 44. Ripple Rejection vs Frequency
($I_{OUT} = 50\text{ mA}$)

Typical Performance Curves (BD750L05G-C)

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

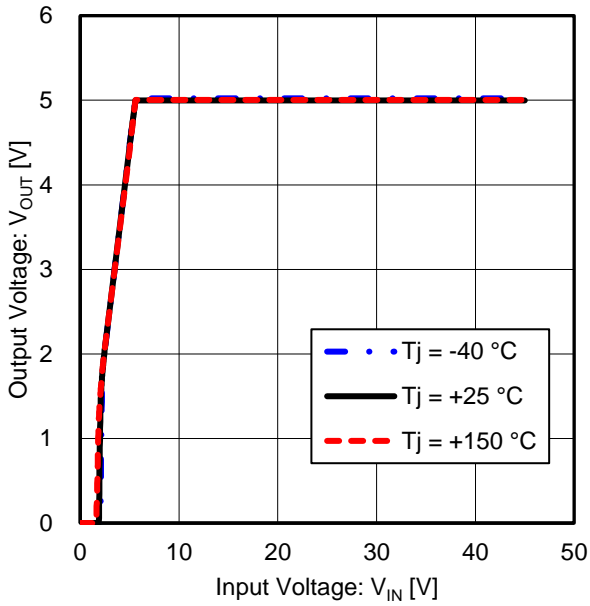


Figure 45. Output Voltage vs Input Voltage

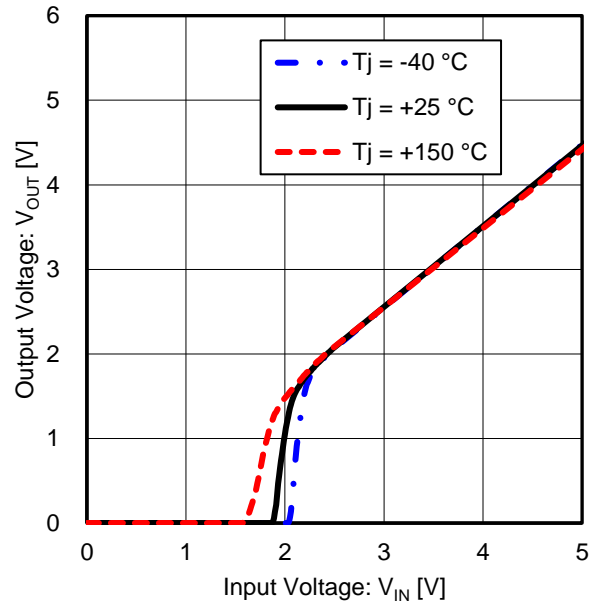


Figure 46. Output Voltage vs Input Voltage - Enlarged view

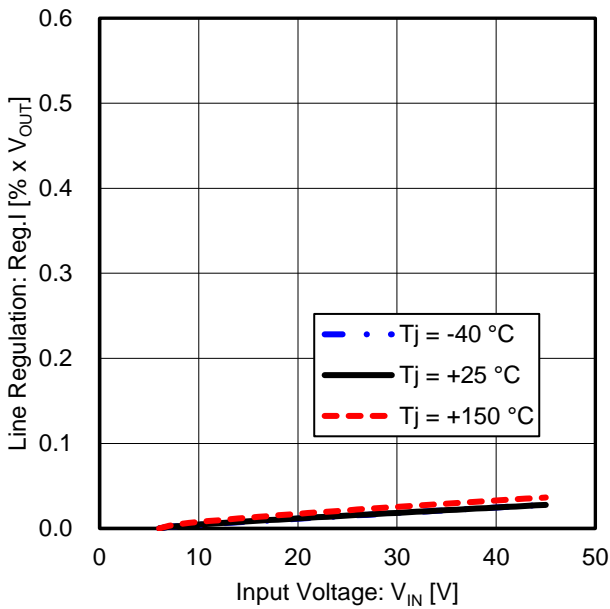


Figure 47. Line Regulation vs Input Voltage ($V_{IN} = 6\text{ V to }45\text{ V}$)

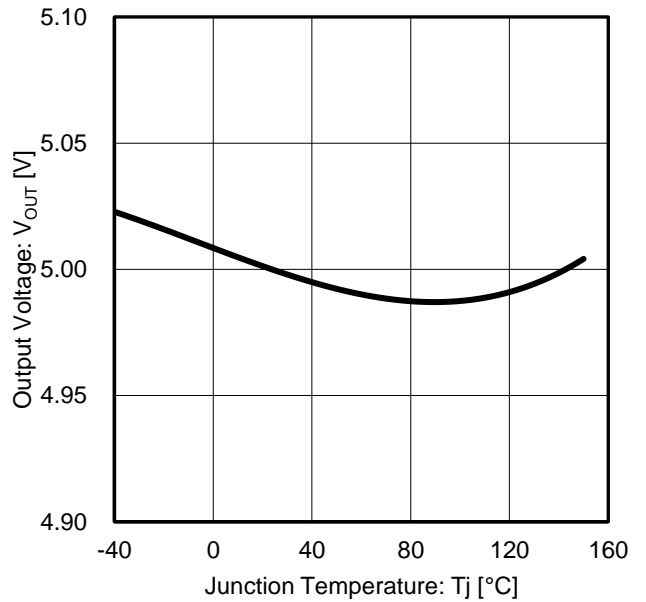


Figure 48. Output Voltage vs Junction Temperature

Typical Performance Curves (BD750L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

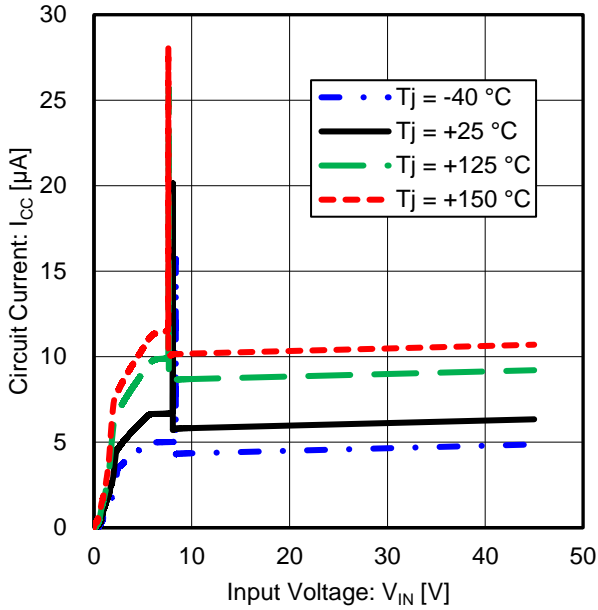


Figure 49. Circuit Current vs Input Voltage ($I_{OUT} = 0\text{ mA}$)

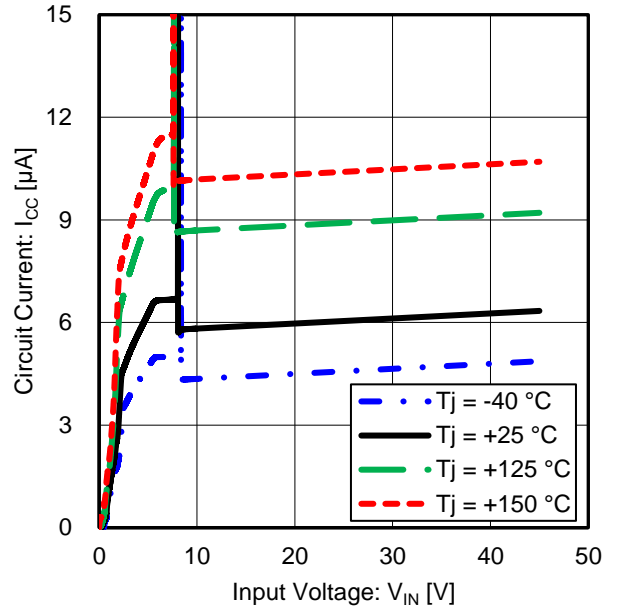


Figure 50. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 0\text{ mA}$)

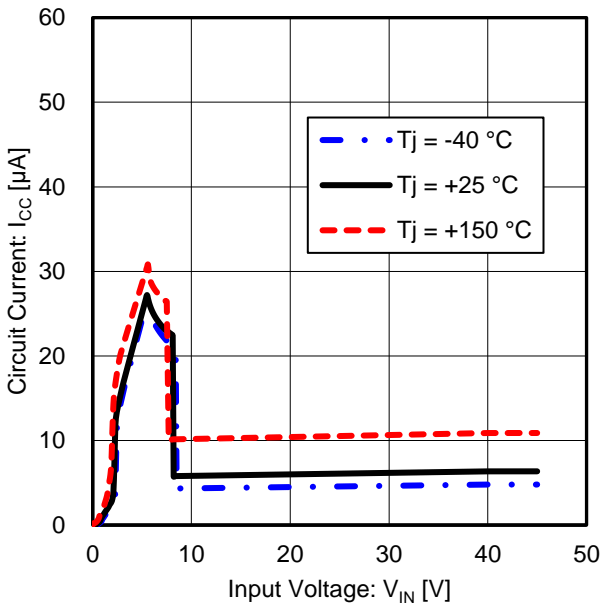


Figure 51. Circuit Current vs Input Voltage ($I_{OUT} = 50\text{ mA}$)

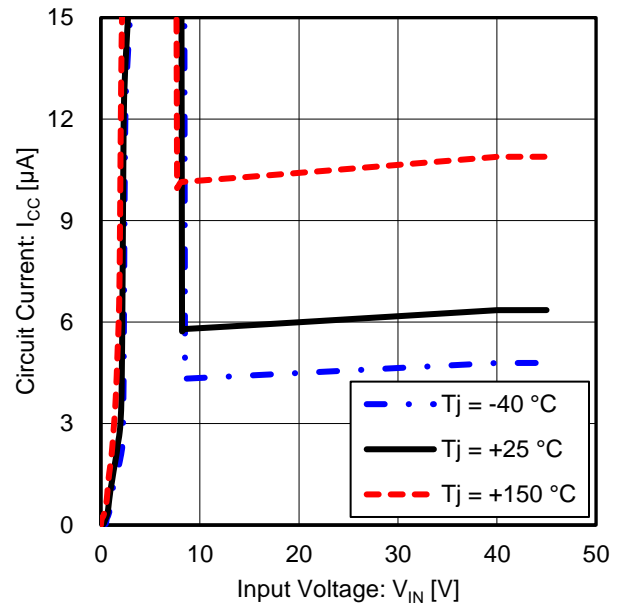


Figure 52. Circuit Current vs Input Voltage - Enlarged view ($I_{OUT} = 50\text{ mA}$)

Typical Performance Curves (BD750L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

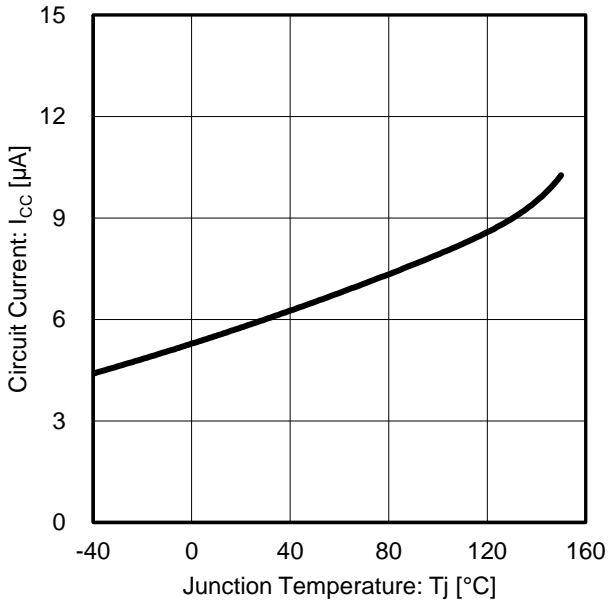


Figure 53. Circuit Current vs Junction Temperature ($I_{OUT} = 0\text{ mA}$)

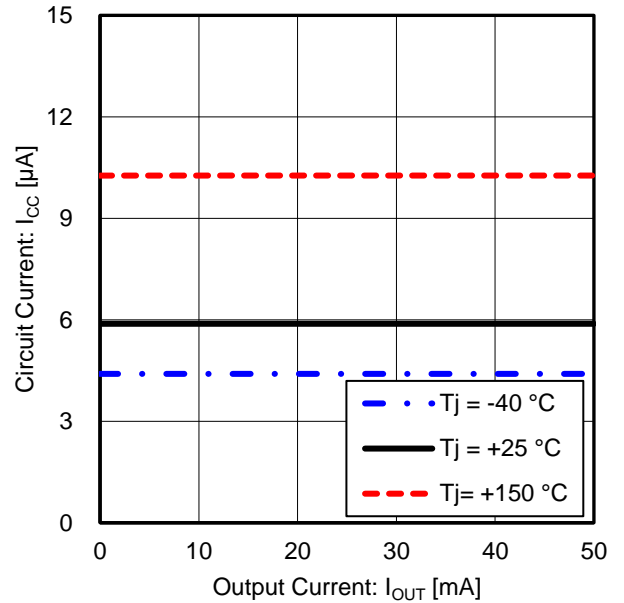


Figure 54. Circuit Current vs Output Current

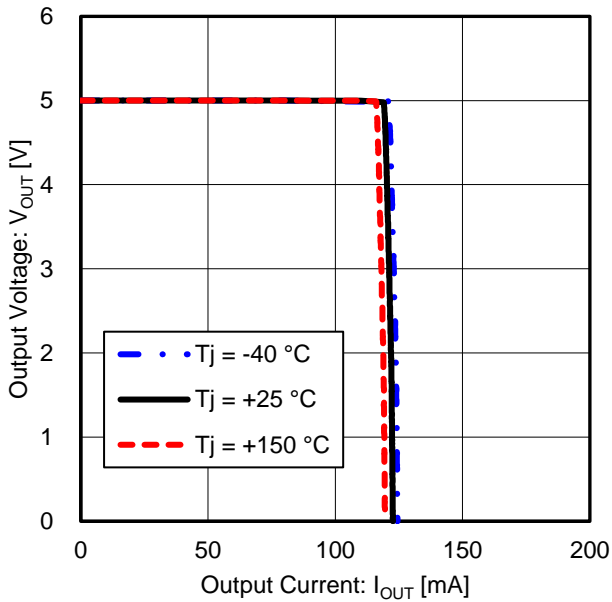


Figure 55. Output Voltage vs Output Current (Over Current Protection)

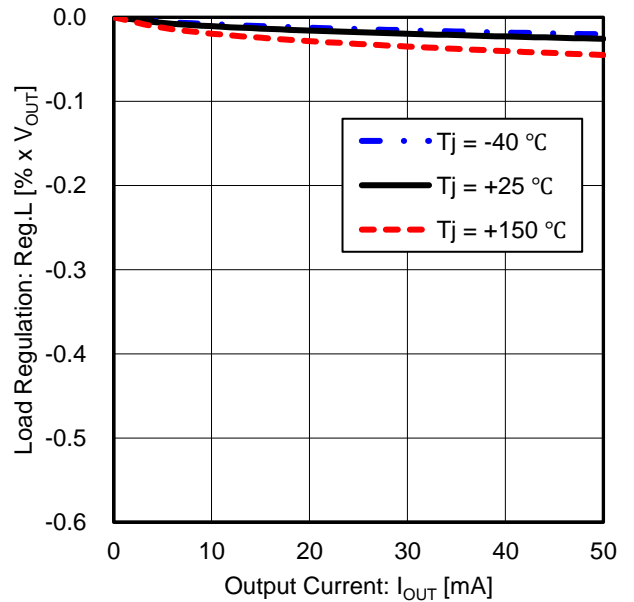


Figure 56. Load Regulation vs Output Current ($I_{OUT} = 100\text{ }\mu\text{A}$ to 50 mA)

Typical Performance Curves (BD750L05G-C) – continued

Unless otherwise specified, $V_{IN} = 13.5\text{ V}$, $I_{OUT} = 0\text{ mA}$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$

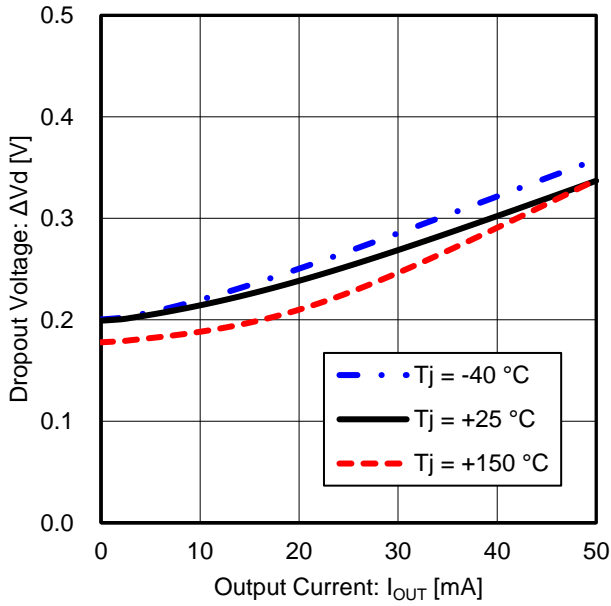


Figure 57. Dropout Voltage vs Output Current
($V_{IN} = V_{OUT} \times 0.95\text{ V} = 4.75\text{ V}$)

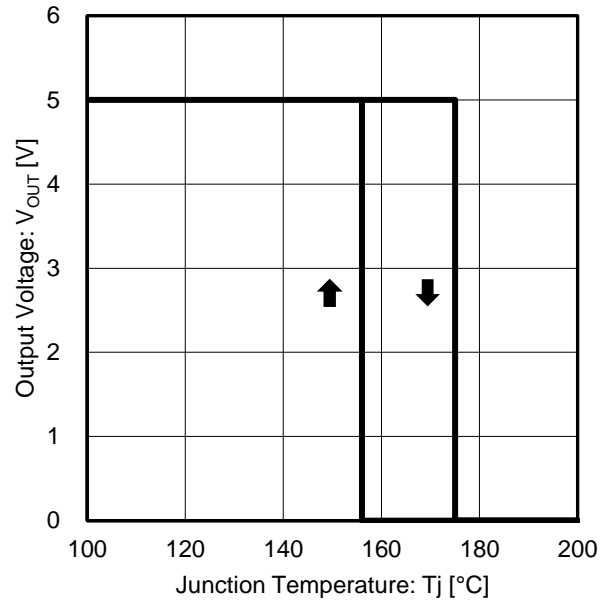


Figure 58. Output Voltage vs Junction Temperature
(Thermal Shutdown Protection)

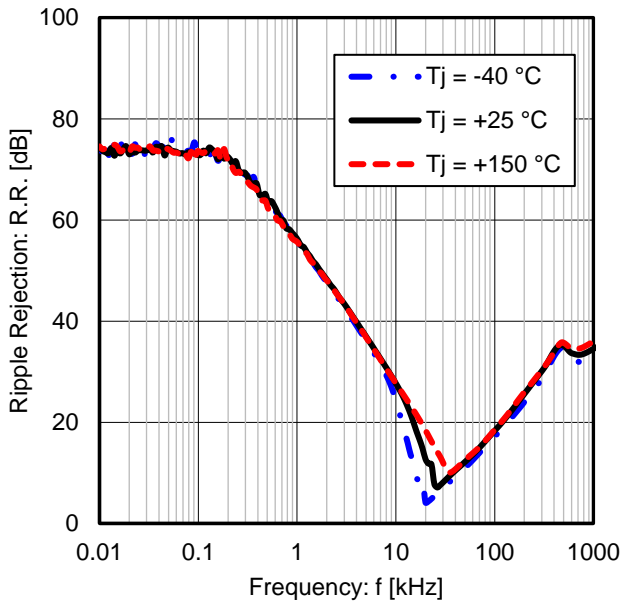
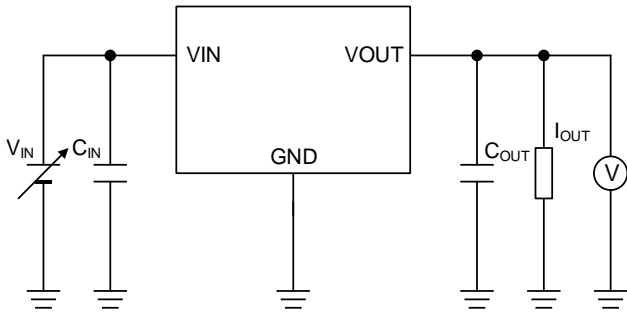
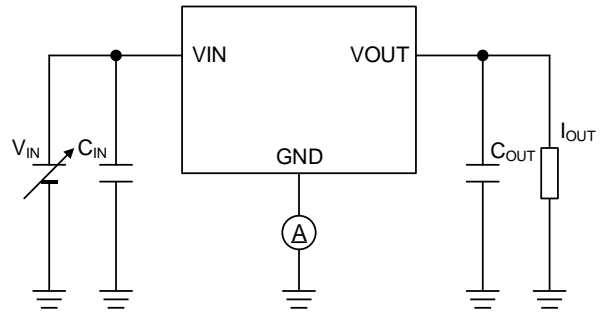


Figure 59. Ripple Rejection vs Frequency
($I_{OUT} = 50\text{ mA}$)

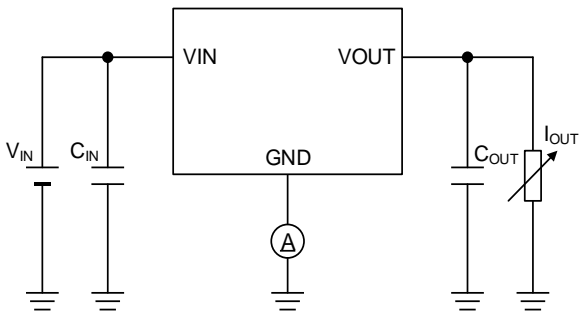
Measurement Circuit for Typical Performance Curves



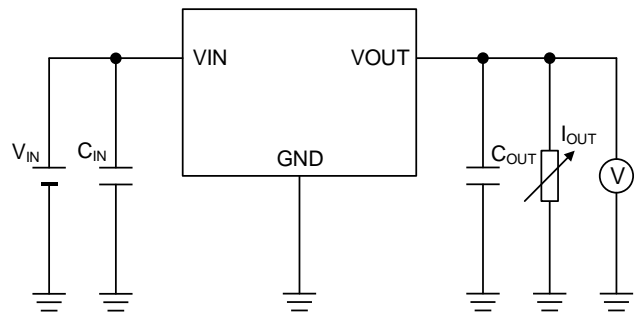
Measurement Setup for
Figure 1, 2, 3, 4, 13,
Figure 15, 16, 17, 18, 28,
Figure 30, 31, 32, 33, 43,
Figure 45, 46, 47, 48, 58



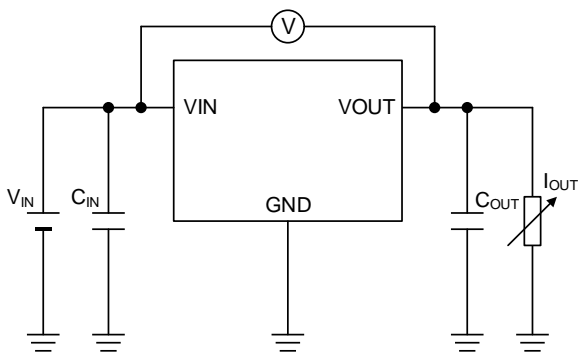
Measurement Setup for
Figure 5, 6, 7, 8, 9,
Figure 19, 20, 21, 22, 23,
Figure 34, 35, 36, 37, 38,
Figure 49, 50, 51, 52, 53



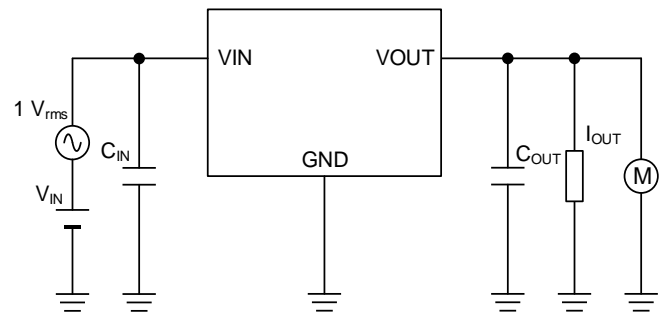
Measurement Setup for
Figure 10, 24, 39, 54



Measurement Setup for
Figure 11, 12, 25, 26,
Figure 40, 41, 55, 56



Measurement Setup for
Figure 27, 42, 57



Measurement Setup for
Figure 14, 29, 44, 59

Application and Implementation

Notice: The following information is given as a reference or hint for the application and the implementation. Therefore, it does not guarantee its operation on the specific function, accuracy or external components in the application. In the application, it shall be designed with sufficient margin by enough understanding about characteristics of the external components, e.g. capacitor, and also by appropriate verification in the actual operating conditions.

Selection of External Components

Input Pin Capacitor

If the battery is placed far from the regulator or the impedance of the input-side is high, higher capacitance is required for the input capacitor in order to prevent the voltage-drop at the input line. The input capacitor and its capacitance should be selected depending on the line impedance which is between the input pin and the smoothing filter circuit of the power supply. At this time, the capacitance value setting is different each application. Generally, the capacitor with capacitance value of 0.1 μF (Min) or more with good high frequency characteristic is recommended for this regulator.

In addition, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic. All input capacitors mentioned above are recommended to have a good DC bias characteristic and a temperature characteristic (approximately $\pm 15\%$, e.g. X7R, X8R) with being satisfied high absolute maximum voltage rating based on EIA standard. These capacitors should be placed close to the input pin and mounted on the same board side of the regulator not to be influenced by implementation impedance.

Output Pin Capacitor

The output capacitor is mandatory that stop oscillation for the regulator in order to realize stable operation. The output capacitor with effective capacitance value $\geq 0.5 \mu\text{F}$ (Min) and ESR up to 100 Ω (Max) must be required between the output pin and the GND pin. By using a ceramic capacitor, enables to expect smaller set and long-life.

A proper selection of appropriate both the capacitance value and ESR for the output capacitor can improve the transient response of the regulator and can also keep the stability with better regulation loop. The correlation of the output capacitance value and ESR is shown in the graph ([Figure 60 Output Capacitance \$C_{OUT}\$, ESR Stable Available Area](#)) on the next page as the output capacitor's capacitance value and the stability region for ESR. As described in this graph, this regulator is designed to be stable with ceramic capacitors as of MLCC, with the capacitance value from 0.5 μF to 1000 μF and with ESR value within almost 0 Ω to 100 Ω . The frequency range of ESR can be generally considered as within about 10 kHz to 100 kHz.

Note that the provided the stable area of the capacitance value and ESR in the graph is obtained under a specific set of conditions which is based on the measurement result in single IC on our board with a resistive load. In the actual environment, the stability is affected by wire impedance on the board, input power supply impedance and also loads impedance. Therefore, note that a careful evaluation of the actual application, the actual usage environment and the actual conditions should be done to confirm the actual stability of the system.

Generally, in the transient event which is caused by the input voltage fluctuation or the load fluctuation beyond the gain bandwidth of the regulation loop, the transient response ability of the regulator depends on the capacitance value of the output capacitor. Basically the capacitance value of $\geq 1.0 \mu\text{F}$ (Typ) for the output capacitor is recommended. Using bigger capacitance value can be expected to improve better the output voltage fluctuation in a high frequency. Various types of capacitors can be used for the output capacitor with high capacity which includes electrolytic capacitor, electro-conductive polymer capacitor and tantalum capacitor. Noted that, depending on the type of capacitors, its characteristics such as ESR ($\leq 100 \Omega$) absolute value range, a temperature dependency of capacitance value and increased ESR at cold temperature needs to be taken into consideration. Especially when the ESR is large, the voltage generated by charge current and discharge current to capacitor and ESR are large. When transient response such that charge current and discharge current flow, noted that output voltage fluctuation.

In addition, the same consideration should be taken as the input pin capacitor, to prevent an influence to the regulator's characteristic from the deviation or the variation of the external capacitor's characteristic. All output capacitors mentioned above are recommended to have a good DC bias characteristic and a temperature characteristic (approximately $\pm 15\%$, e.g. X7R, X8R) with being satisfied high absolute maximum voltage rating based on EIA standard. These capacitors should be placed close to the output pin and mounted on the same board side of the regulator not to be influenced by implementation impedance.

Output Pin Capacitor - continued

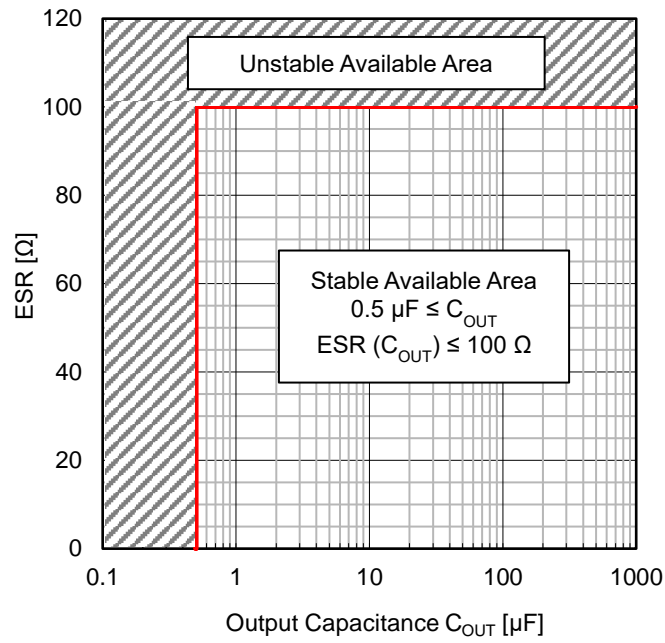
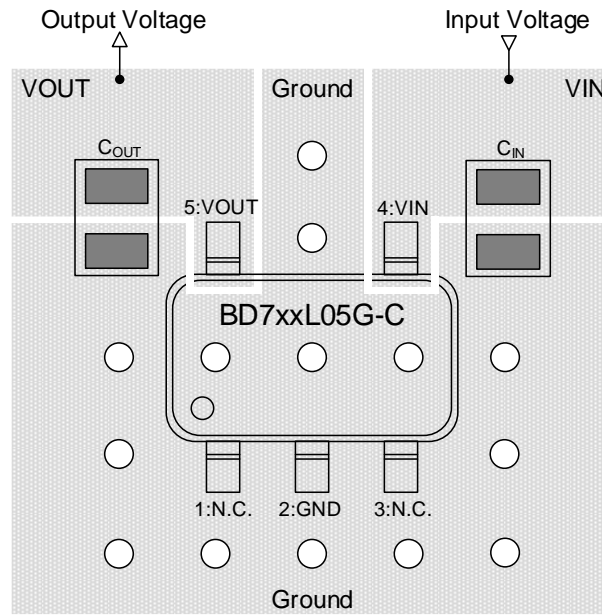


Figure 60. Output Capacitance C_{OUT} , ESR Stable Available Area

Parameter		Symbol	Conditions
Input Supply Voltage	BD725L05G-C / BD730L05G-C	V_{IN}	$3.5 \text{ V} \leq V_{IN} \leq 42.0 \text{ V}$
	BD733L05G-C	V_{IN}	$3.8 \text{ V} \leq V_{IN} \leq 42.0 \text{ V}$
	BD750L05G-C	V_{IN}	$5.6 \text{ V} \leq V_{IN} \leq 42.0 \text{ V}$
Output Current		I_{OUT}	$0 \text{ mA} \leq I_{OUT} \leq 50 \text{ mA}$
Junction Temperature		T_j	$-40 \text{ }^\circ\text{C} \leq T_j \leq +150 \text{ }^\circ\text{C}$

Typical Application and Layout Example



Parameter		Symbol	Recommended Value
Output Current Range		I_{OUT}	$I_{OUT} \leq 50 \text{ mA}$
Output Capacitor		C_{OUT}	$1 \mu\text{F} \leq C_{OUT} \leq 1000 \mu\text{F}$
Output Capacitor ESR for stability ^(Note 1)		ESR (C_{OUT})	$ESR \leq 100 \Omega$
Input Voltage Range ^(Note 2)	BD725L05G-C / BD730L05G-C	V_{IN}	$3.5 \text{ V} \leq V_{IN} \leq 42.0 \text{ V}$
	BD733L05G-C	V_{IN}	$3.8 \text{ V} \leq V_{IN} \leq 42.0 \text{ V}$
	BD750L05G-C	V_{IN}	$5.6 \text{ V} \leq V_{IN} \leq 42.0 \text{ V}$
Input Capacitor ^(Note 3)		C_{IN}	$0.1 \mu\text{F} \leq C_{IN}$

(Note 1) Refer to [Selection of External Components](#) and select the parts.

(Note 2) Minimum Input Supply Voltage must be $V_{IN \text{ Start-up}} = 3 \text{ V}$ or more.

Consider that the output voltage would be reduced (Dropout Voltage) by the output current.

(Note 3) If the inductance of power supply line is high, adjust input capacitor value.

Application and Implementation - continued

Surge Voltage Protection for Linear Regulators

The following shows some helpful tips to protect ICs from possible inputting surge voltage which exceeds absolute maximum ratings.

Positive surge to the input

If there is any potential risk that positive surges higher than absolute maximum ratings 45 V, it is applied to the input, a Zener Diode should be inserted between the VIN pin and the GND to protect the device as shown in Figure 61.

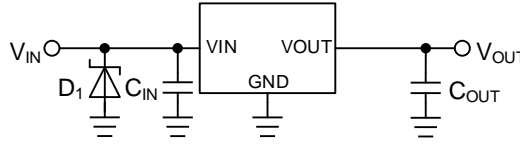


Figure 61. Surges Higher than 45 V is Applied to the Input

Negative surge to the input

If there is any potential risk that negative surges below the absolute maximum ratings, (e.g.) -0.3 V, is applied to the input, a Schottky barrier diode should be inserted between the VIN pin and the GND to protect the device as shown in Figure 62.

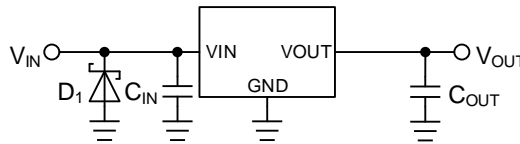


Figure 62. Surges Lower than -0.3 V is Applied to the Input

Reverse Voltage Protection for Linear Regulators

A linear regulator integrated circuit (IC) requires the input voltage to be always higher than the regulated voltage. Output voltage, however, may become higher than the input voltage under specific situations or circuit configurations. In such circumstances reverse voltage and current may cause damage to the IC. A reverse polarity connection of power supply or certain inductor components can also cause a polarity reversal between the input and output pins. The following provides instructions on reversed voltage polarity protection for ICs.

Protection against Reverse Input/Output Voltage

In the MOS linear regulator, a parasitic body diode between the drain-source of MOSFET generally exists. If the output voltage becomes higher than the input voltage and if its voltage difference exceeds V_F of the body diode, a reverse current flows from the output to the input through the body diode as shown in Figure 63. The current flows in the parasitic body diode is not limited in the protection circuit because it is the parasitic element, therefore too much reverse current may cause damage to degrade or destroy the semiconductor elements of the regulator.

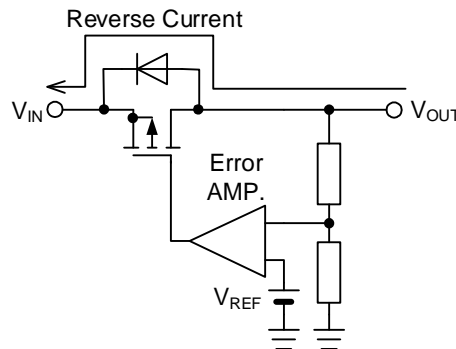


Figure 63. Reverse Current Path in a MOS Linear Regulator

Protection against Reverse Input/Output Voltage – continued

An effective solution for this problem is to implement an external bypass diode in order to prevent the reverse current flow inside the IC as shown in Figure 64. Note that the bypass diode must be turned on prior to the internal body diode of the IC. This external bypass diode should be chosen as being lower forward voltage V_F than the internal body diode. If the reverse current of this bypass diode is large, even if the output is OFF, a lot of diode leakage current flows from the input to the output, so it is necessary to select one with a small value. It should be selected a diode which has a rated reverse voltage greater than the IC's input maximum voltage and also which has a rated forward current greater than the anticipated reverse current in the actual application.

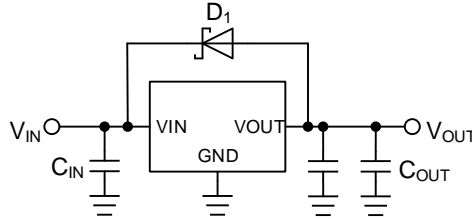


Figure 64. Bypass Diode for Reverse Current Diversion

A Schottky barrier diode which has a characteristic of low forward voltage (V_F) can meet to the requirement for the external diode to protect the IC from the reverse current. However, it also has a characteristic that the leakage (I_R) caused by the reverse voltage is bigger than other diodes. Therefore, it should be taken into the consideration to choose it because if I_R is large, it may cause increase of the current consumption, or raise of the output voltage in the light-load current condition. I_R characteristic of Schottky diode has positive temperature characteristic, which the details shall be checked with the datasheet of the products, and the careful confirmation of behavior in the actual application is mandatory.

Even in the condition when the input/output voltage is inverted, if the VIN pin is open as shown in Figure 65, or if the VIN pin becomes high-impedance condition as designed in the system, it cannot damage or degrade the parasitic element. It's because a reverse current via the pass transistor becomes extremely low. In this case, therefore, the protection external diode is not necessary.

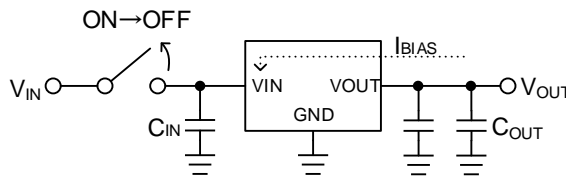


Figure 65. Open VIN

Protection against Input Reverse Voltage

When the input of the IC is connected to the power supply, accidentally if plus and minus are routed in reverse, or if there is a possibility that the input may become lower than the GND pin, it may cause to destroy the IC because a large current passes via the internal electrostatic breakdown prevention diode between the input pin and the GND pin inside the IC as shown in Figure 66.

The simplest solution to avoid this problem is to connect a Schottky barrier diode or a rectifier diode in series to the power supply line as shown in Figure 67. However, it causes the voltage drop by a forward voltage V_F at the supply voltage while normal operation.

Generally, since the Schottky barrier diode has lower V_F , so it contributes to rather smaller power loss than rectifier diodes. If IC has load currents, this external diode generates heat more, therefore select a diode with enough margin in power dissipation. On the other hand, a reverse current passes this diode in the reverse connection condition, however, it is negligible because its small amount.

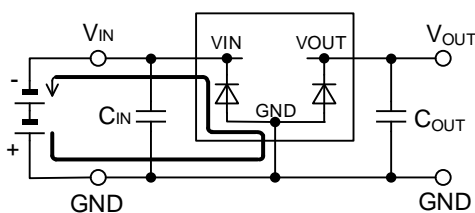


Figure 66. Current Path in Reverse Input Connection

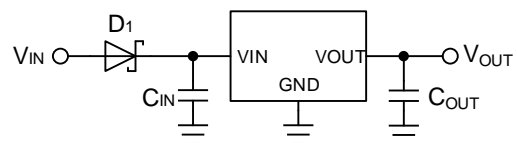


Figure 67. Protection against Reverse Polarity 1

Protection against Input Reverse Voltage - continued

Figure 68 shows a circuit in which a P-channel MOSFET is connected in series to the power. The body diode (parasitic element) is located in the drain-source junction area of the MOSFET. Since the Pch MOSFET is turned on in the correct connection, the drop voltage in a forward connection is calculated from the on state resistance of the MOSFET and the output current I_{OUT} . It is smaller than the drop voltage by the diode as shown in Figure 67 and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off in Figure 68.

If the gate-source voltage exceeds maximum rating of MOSFET gate-source junction with derating curve in consideration, reduce the gate-source junction voltage by connecting resistor voltage divider as shown in Figure 69.

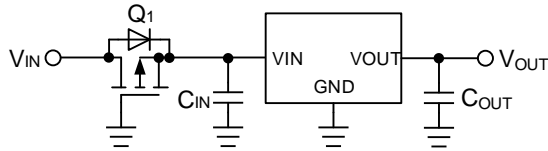


Figure 68. Protection against Reverse Polarity 2

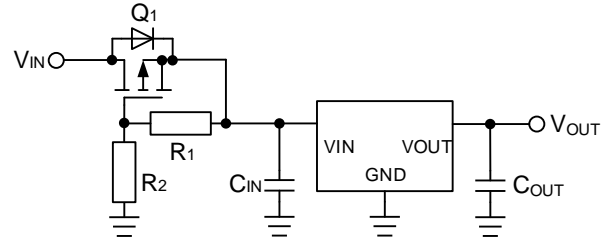


Figure 69. Protection against Reverse Polarity 3

Protection against Reverse Output Voltage when the Output is connected to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground at the moment that the output voltage is turned off. IC integrates ESD protection diodes between the IC output and ground pins. A large current may flow in such condition finally resulting on destruction of the IC. To prevent this situation, connect a Schottky barrier diode in parallel to the integrated diodes as shown in Figure 70.

Further, if a long wire is in use for the connection between the output pin of the IC and the load, confirm that the negative voltage is not generated at the VOUT pin when the output voltage is turned off by observation of the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is required for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

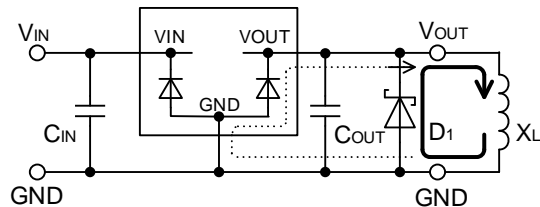
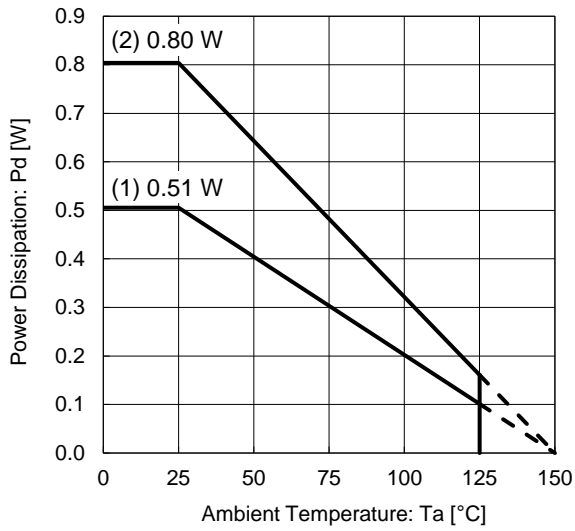


Figure 70. Current Path in Inductive Load (Output: Off)

Power Dissipation

SSOP5



(1): 1-layer PCB
 (Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
 Board material: FR-4
 Board size: 114.3 mm × 76.2 mm × 1.57 mm
 Top copper foil: Footprints and Traces, 70 μm copper.

(2): 4-layer PCB
 (Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm)
 Board material: FR-4
 Board size: 114.3 mm × 76.2 mm × 1.6 mm
 Top copper foil: Footprints and Traces, 70 μm copper.
 2 inner layers copper foil area of PCB:
 74.2 mm × 74.2 mm, 35 μm copper.
 Bottom copper foil area of PCB:
 74.2 mm × 74.2 mm, 70 μm copper.

Condition (1): $\theta_{JA} = 247.3 \text{ }^\circ\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 43 \text{ }^\circ\text{C/W}$
 Condition (2): $\theta_{JA} = 155.5 \text{ }^\circ\text{C/W}$, $\Psi_{JT} \text{ (top center)} = 33 \text{ }^\circ\text{C/W}$

Figure 71. Power Dissipation Graph (SSOP5)

Thermal Design

The power consumption of the IC is decided by the dropout voltage condition, the load current and the current consumption. Refer to power dissipation curves illustrated in [Figure 71](#) when using the IC in an environment of $T_a \geq +25\text{ }^\circ\text{C}$. Even if the ambient temperature T_a is at $+25\text{ }^\circ\text{C}$, chip junction temperature (T_j) can be very high depending on the input voltage and the load current. Consider the design to be $T_j \leq T_{j\max} = +150\text{ }^\circ\text{C}$ in whole operating temperature range.

Should by any condition the maximum junction temperature $T_{j\max} = +150\text{ }^\circ\text{C}$ rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal resistance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Therefore, need to be careful because it might be different from the actual use condition. Verify the application and allow sufficient margins in the thermal design by the following method to calculate the junction temperature T_j . T_j can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature T_j with ambient temperature T_a .

$$T_j = T_a + P_C \times \theta_{JA} \text{ [}^\circ\text{C]}$$

Where:

- T_j is the Junction Temperature
- T_a is the Ambient Temperature
- P_C is the Power Consumption
- θ_{JA} is the Thermal Resistance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature T_j with top center of case's (mold) temperature T_T .

$$T_j = T_T + P_C \times \Psi_{JT} \text{ [}^\circ\text{C]}$$

Where:

- T_j is the Junction Temperature
- T_T is the Top Center of Case's (mold) Temperature
- P_C is the Power consumption
- Ψ_{JT} is the Thermal Resistance (Junction to Top Center of Case)

3. The following method is used to calculate the power consumption P_C (W).

$$P_C = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \text{ [W]}$$

Where:

- P_C is the Power Consumption
- V_{IN} is the Input Voltage
- V_{OUT} is the Output Voltage
- I_{OUT} is the Load Current
- I_{CC} is the Current Consumption

Calculation Example

If $V_{IN} = 13.5\text{ V}$, $V_{OUT} = 3.0\text{ V}$, $I_{OUT} = 10\text{ mA}$, $I_{CC} = 6\text{ }\mu\text{A}$, the power consumption P_C can be calculated as follows:

$$\begin{aligned} P_C &= (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \\ &= (13.5\text{ V} - 3.0\text{ V}) \times 10\text{ mA} + 13.5\text{ V} \times 6\text{ }\mu\text{A} \\ &\approx 0.11\text{ W} \end{aligned}$$

At the maximum ambient temperature $T_{\max} = 85\text{ }^\circ\text{C}$,
the thermal resistance (Junction to Ambient) $\theta_{JA} = 155.5\text{ }^\circ\text{C/W}$ (4-layer PCB)

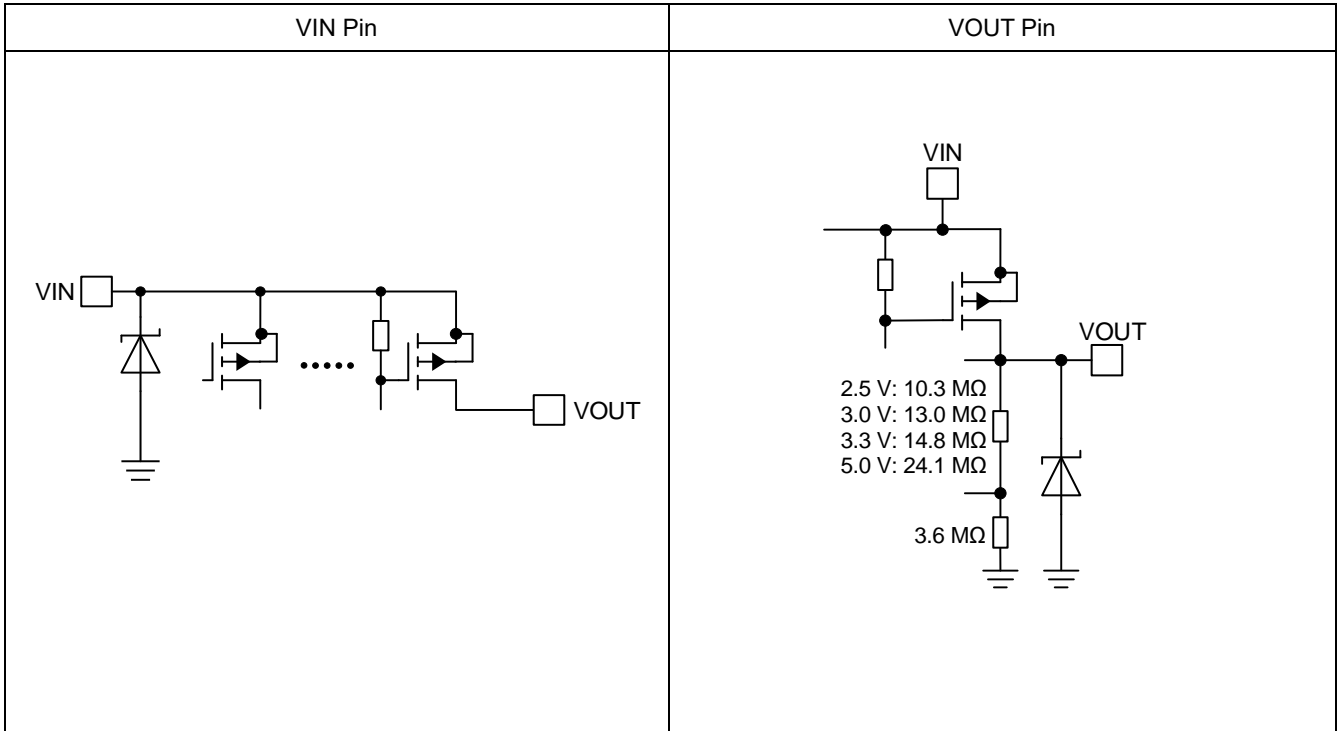
$$\begin{aligned} T_j &= T_{\max} + P_C \times \theta_{JA} \\ &= 85\text{ }^\circ\text{C} + 0.11\text{ W} \times 155.5\text{ }^\circ\text{C/W} \\ &\approx 102.1\text{ }^\circ\text{C} \end{aligned}$$

When operating the IC, the top center of case's (mold) temperature $T_T = 100\text{ }^\circ\text{C}$, $\Psi_{JT} = 43\text{ }^\circ\text{C/W}$ (1-layer PCB)

$$\begin{aligned} T_j &= T_T + P_C \times \Psi_{JT} \\ &= 100\text{ }^\circ\text{C} + 0.11\text{ W} \times 43\text{ }^\circ\text{C/W} \\ &= 104.7\text{ }^\circ\text{C} \end{aligned}$$

If it is difficult to ensure the margin by the calculations above, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad for optimum thermal performance.

I/O Equivalence Circuit^(Note 1)



(Note 1) Resistance value is Typical.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

9. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

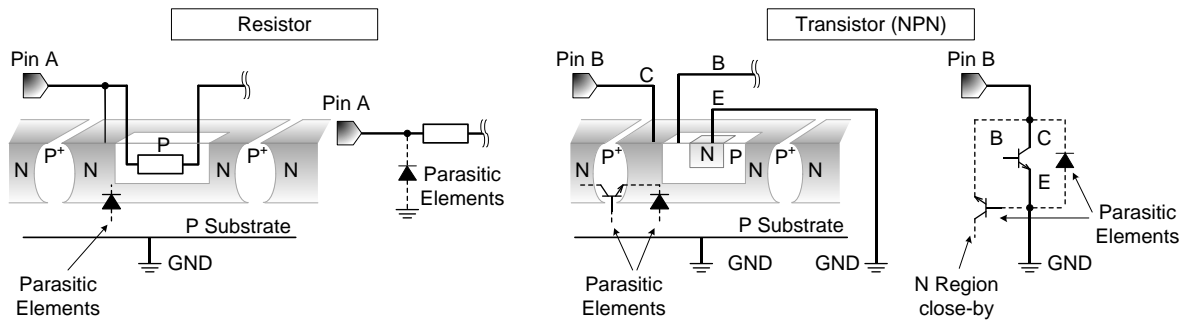


Figure 72. Example of Monolithic IC Structure

10. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

11. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

12. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

13. Thermal Consideration

The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. The amount of heat generation depends on the voltage difference between the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the P_d rating. If Junction temperature is over T_{jmax} ($= 150\text{ }^\circ\text{C}$), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

14. Functional Safety

"ISO 26262 process compliant to support ASIL-*"

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety mechanism is implemented to support functional safety (ASIL-*)"

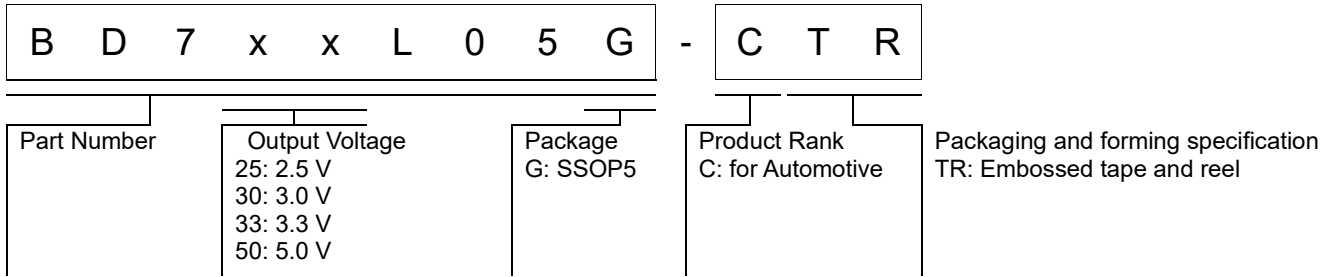
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional safety supportive automotive products"

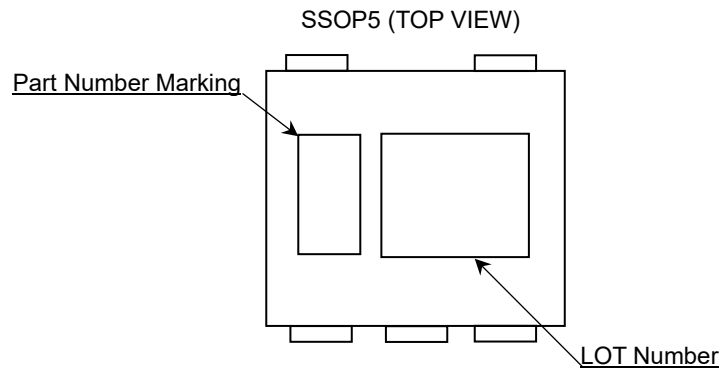
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information



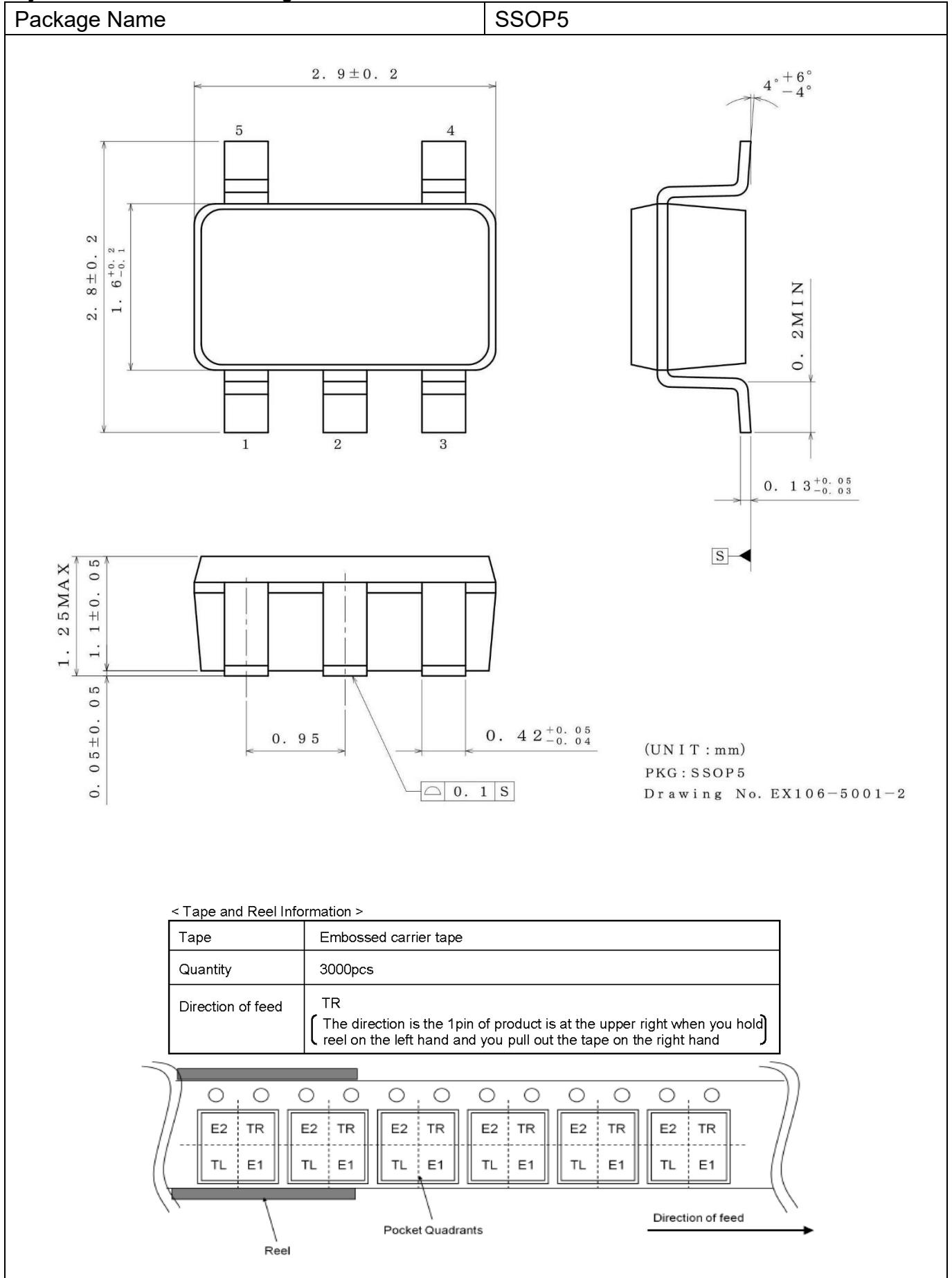
Marking Diagram



Lineup

Part Number Marking	Output Voltage	Orderable Part Number
dq	2.5 V	BD725L05G-CTR
du	3.0 V	BD730L05G-CTR
dr	3.3 V	BD733L05G-CTR
dy	5.0 V	BD750L05G-CTR

Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
29.Mar.2022	001	New Release
18.Nov.2022	002	Added about functional safety

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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 - [d] the Products are exposed to high Electrostatic
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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