Datasheet

For Automotive Sequential Winker

8 ch Internal By-pass Switch LED Driver

BD18364EFV-M

General Description

The BD18364EFV-M is a buck-boost LED driver with built-in 8 ch By-pass switch. Sequential winker and animation lamp light circuits are made possible in this circuit. The By-pass switch can be controlled ON and OFF individually by micro-controller communication. In By-pass switch control, generating high current can be prevented from the current limit circuit.

Features

- AEC-Q100 Qualified*(Note 1)*
- Functional Safety Supportive Automotive Products
- Buck-boost LED Driver (Boost to VIN)
- Prevents High Current During LED Switching
- 8 ch By-pass Switch
- DC Dimming (10 bit)
- Over Voltage Protection (OVP)
- By-pass Switch Independent PWM Dimming
- UART Communication Interface (Supports CAN and LIN)
- LED Abnormality Detection Function
- Spread Spectrum Frequency Modulation (Variable)
- 8-bit A/D Converter

(Note 1) Grade 1

Key Specifications

- Input Voltage Range: 5.5 V to 45.0 V
- Maximum Voltage Output: 60 V
- Maximum LED Current 0.8 A
- LED Current Accuracy: ±3 %
- LED Voltage/Channel 1.5 V to 13.5 V
- By-pass Switch ON Resistance: 0.3 Ω (Typ)
- Junction Temperature Range: -40 °C to +150 °C

Applications

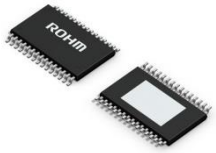
- Automotive Exterior Lamps
- Sequential Winker
- Animation Lamps, etc.

Package

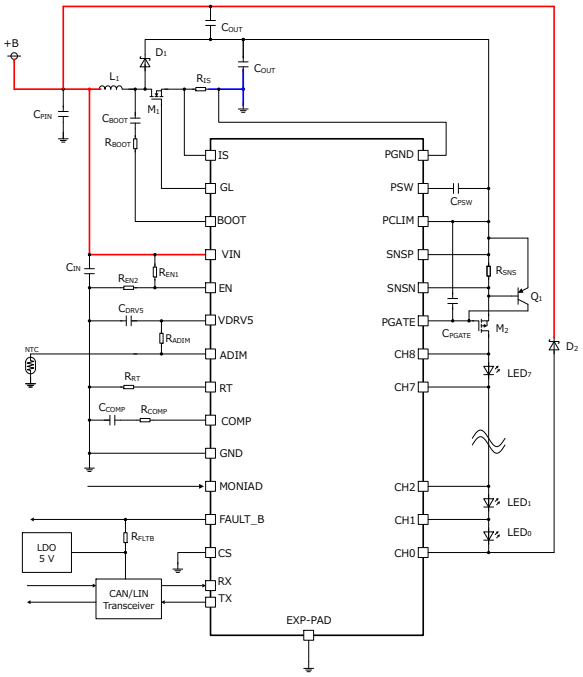
HTSSOP-B30

W (Typ) x D (Typ) x H (Max)

10.0 mm x 7.6 mm x 1.0 mm

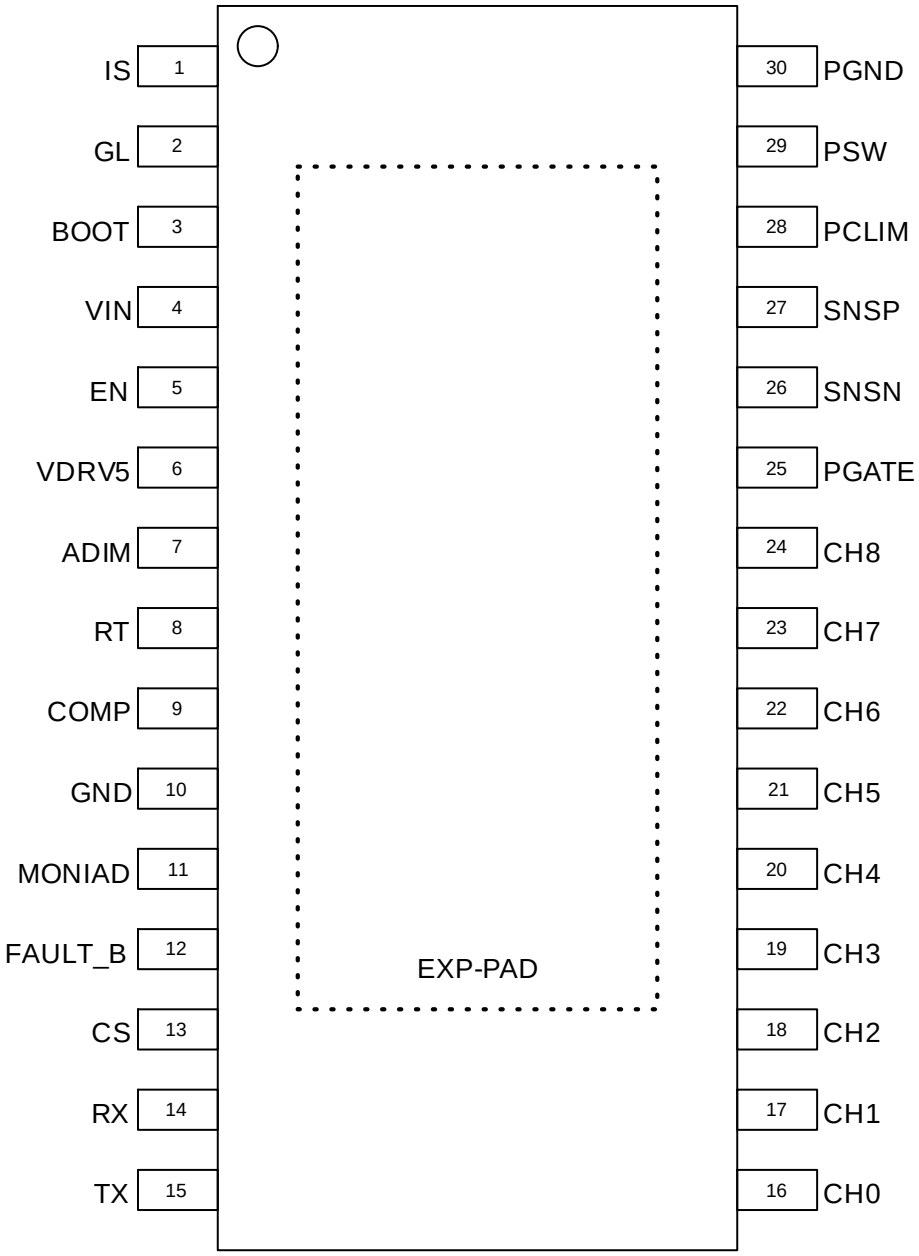


Typical Application Circuit



Pin Configuration

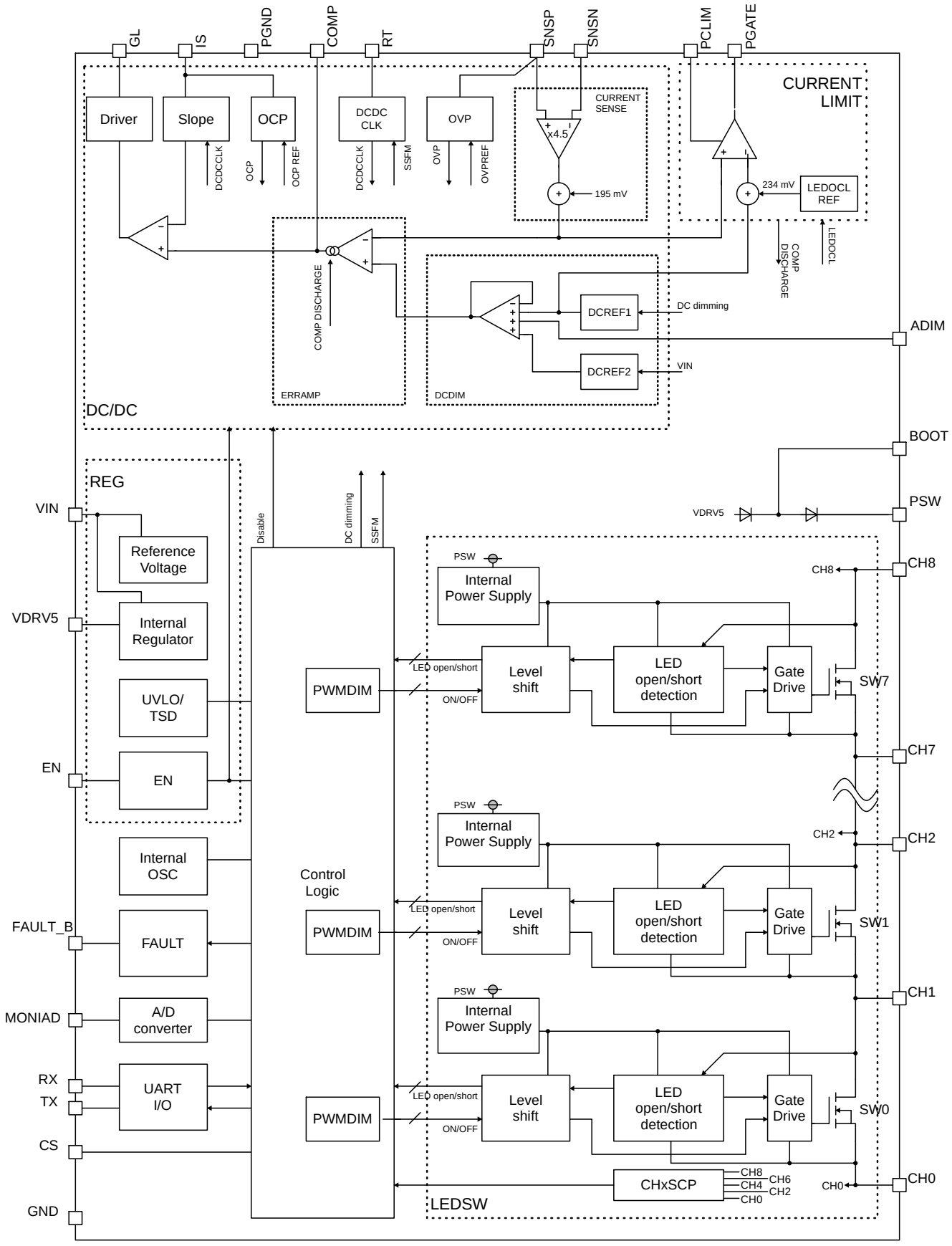
HTSSOP-B30
(TOP VIEW)



Pin Descriptions

Pin No	Pin Name	Function
1	IS	Inductor current sense input.
2	GL	Output for N-ch MOSFET gate drive.
3	BOOT	Power supply voltage capacitor connection for switch drive.
4	VIN	Power supply voltage input.
5	EN	Enable input.
6	VDRV5	Capacitor connection for gate drive 5 V output.
7	ADIM	Analog dimming input.
8	RT	Resistance connection for switching frequency setting.
9	COMP	Phase compensation capacitor connection.
10	GND	GND
11	MONIAD	A/D input.
12	FAULT_B	LED abnormality detection output (Open drain).
13	CS	Chip select (Pull up to VDRV5 or Pull down to GND).
14	RX	UART Interface
15	TX	UART Interface
16	CH0	LED0 cathode connection.
17	CH1	LED0 anode and LED1 cathode connection.
18	CH2	LED1 anode and LED2 cathode connection.
19	CH3	LED2 anode and LED3 cathode connection.
20	CH4	LED3 anode and LED4 cathode connection.
21	CH5	LED4 anode and LED5 cathode connection.
22	CH6	LED5 anode and LED6 cathode connection.
23	CH7	LED6 anode and LED7 cathode connection.
24	CH8	LED7 anode connection.
25	PGATE	Current limit MOS drive output.
26	SNSN	Current sense input (-).
27	SNSP	Current sense input (+).
28	PCLIM	Current limit circuit power supply.
29	PSW	Power supply voltage capacitor connection for By-pass switch drive.
30	PGND	Power GND
	EXP-PAD	Connect EXP-PAD to GND.

Block Diagram



Description of Blocks

1. Total Function

BD18364EFV-M is a buck-boost LED driver with built-in 8 ch By-pass switch. Individual ON and OFF control of LED is possible and by this Sequential winker and Animation lamps are made possible. In the By-pass switch, one or two serial connection of LED is possible. The By-pass switch can be set ON, OFF and PWM dimming by UART communication. LED open detection and short detection functions are built in the By-pass switch. The LED driver is configured with Buck-boost (Boost to VIN). Damages from high current in LED when rush current is generated from output capacitor when By-pass switch switches from OFF to ON (light of LED turns OFF) can be suppressed by current limiting circuit.

2. LED Driver Section

2.1 LED Current Setting (CURRENT SENSE)

LED current can be set by resistor R_{SNS} that is connected in between the SNSP pin and the SNSN pin.

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} \quad [A]$$

2.2 Analog Dimming (DCDIM)

Analog Dimming can be set by DCDIM register (10-bit)

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \left(\frac{DCDIM\ [9:0]}{1024} \times V_{FSR} - 0.195\ V \right) \times \frac{1}{4.5 \times R_{SNS}}$$

Where:

V_{FSR} is the internal ADC converter Full-Scale-Range Voltage 2.5 V (Typ).

2.3 Analog Dimming (ADIM)

With voltage input in the ADIM pin, analog dimming is made possible.

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \frac{V_{ADIM} - 0.195\ V}{4.5 \times R_{SNS}}$$

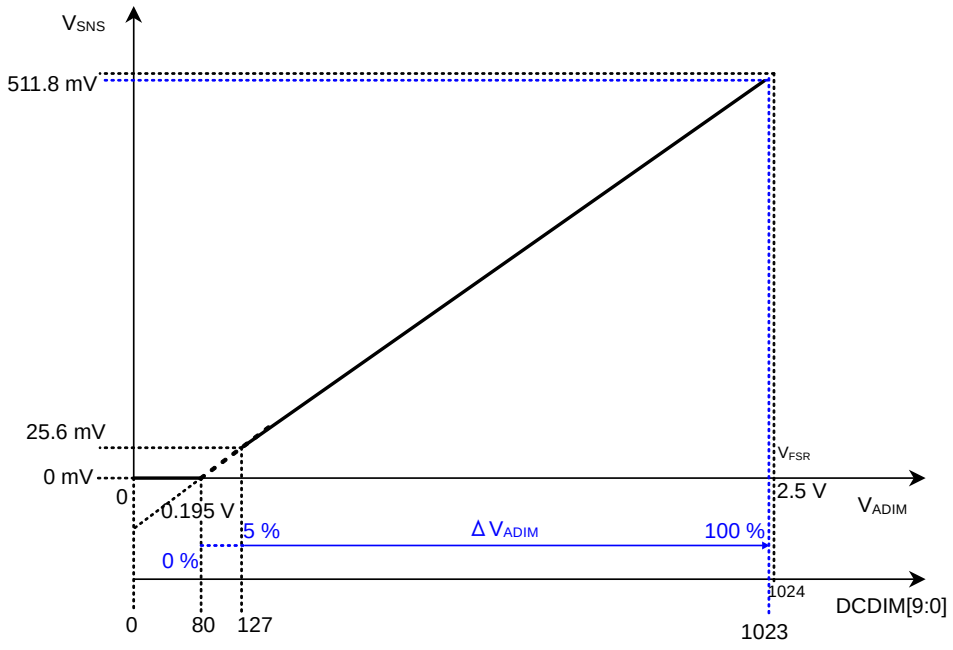


Figure 1. Analog Dimming (DCDIM/ADIM) Setting

2. LED Driver Section – continued

2.4 Input Voltage (VIN) Derating

When input voltage drops, output current can be dropped, depending on input voltage, to prevent increase in input current. Derating starting voltage can be set in register.

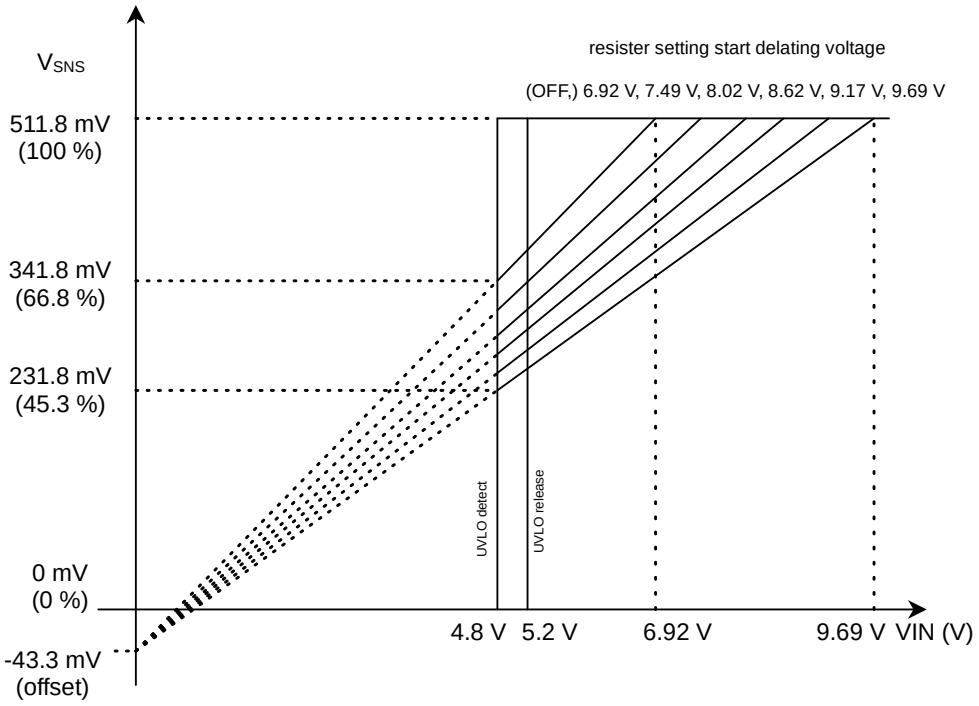


Figure 2. Input Voltage Derating Setting

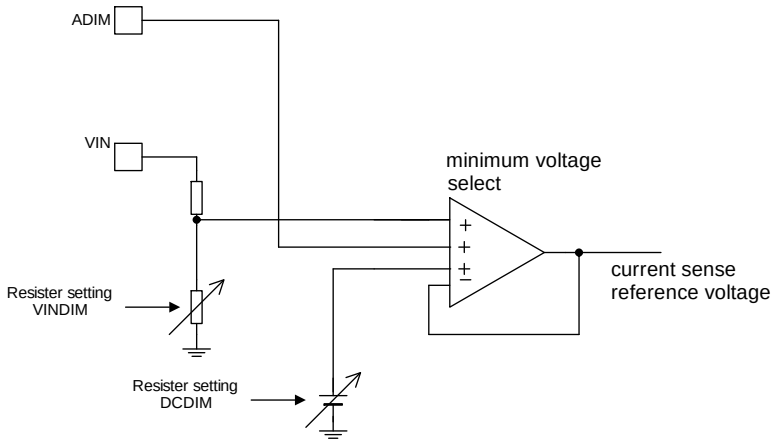


Figure 3. Analog Dimming Circuit

2.4 Input Voltage (VIN) Derating – continued

The DCDIM pin, the ADIM pin and input voltage derating becomes as the circuit configuration such as shown in Figure 3. It will be as the current value that was set at the lowest.
For example, the V_{SNS} voltage characteristics base on ADIM when current value was set to 50 % in the DCDIM is such as shown in Figure 4.

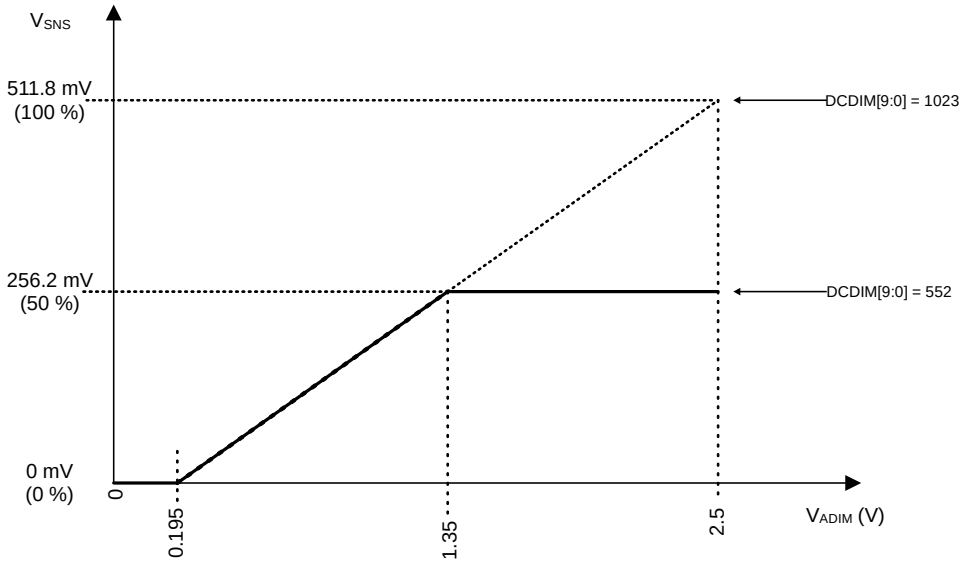


Figure 4. Example of DCDIM and ADIM Dimming

2.5 DC/DC Switching Frequency (OSC)

The switching frequency can be set based on the formula below depending on the external resistor R_{RT}.

$$f_{osc} \fallingdotseq \frac{9900}{R_{RT}} \times 10^3 \text{ [kHz]}$$

2.6 Spread Spectrum Frequency Modulation (SSFM)

With built-in spread spectrum function to reduce DC/DC switching noise peak level. Frequency modulation range is within ± 6 %. The modulation period is set from the register.

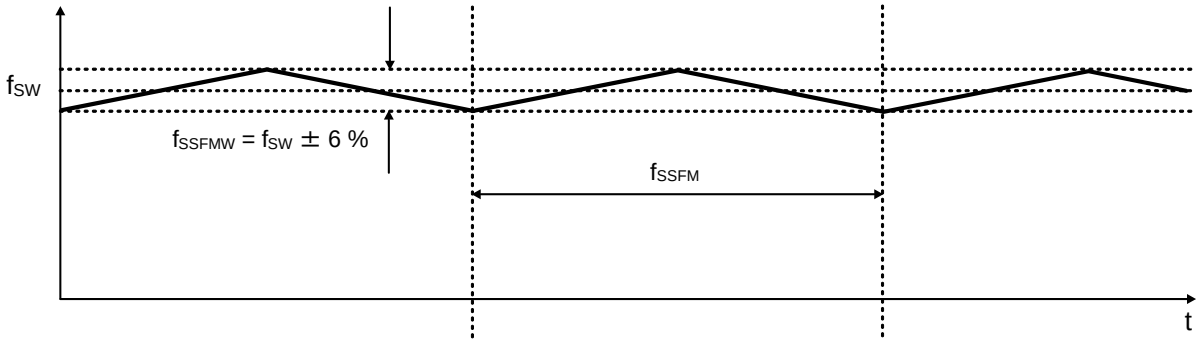


Figure 5. Spread Spectrum Frequency Modulation

2. LED Driver Section – continued

2.7 Protection

2.7.1 Over Voltage Protection (DCDCOVP)

The DC/DC output voltage is monitored by the SNSP pin voltage. If the SNSP pin voltage becomes higher than V_{OVP} voltage, DC/DC will stop. The COMP pin is discharged until GND level voltage. The PMOS for current limit turns OFF. The OVPDET of ERRDET register updates into 1. If the SNSP pin voltage becomes less than V_{OVP_HYS} voltage, the DC/DC reboots. After rebooting, the OVPDET of ERRDET register will update to 0 after t_{OVP}.

Over Voltage Protection threshold can be set by UART communication as following.

$$V_{OVP} = OVPSET\,[3:0] \times 2.18 + 34.8\ [\mathrm{V}]$$

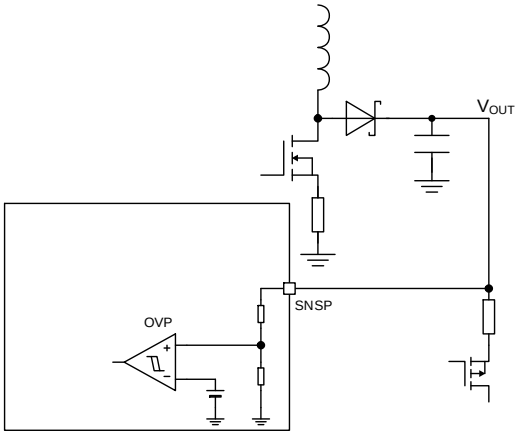


Figure 6. DCDCOVP

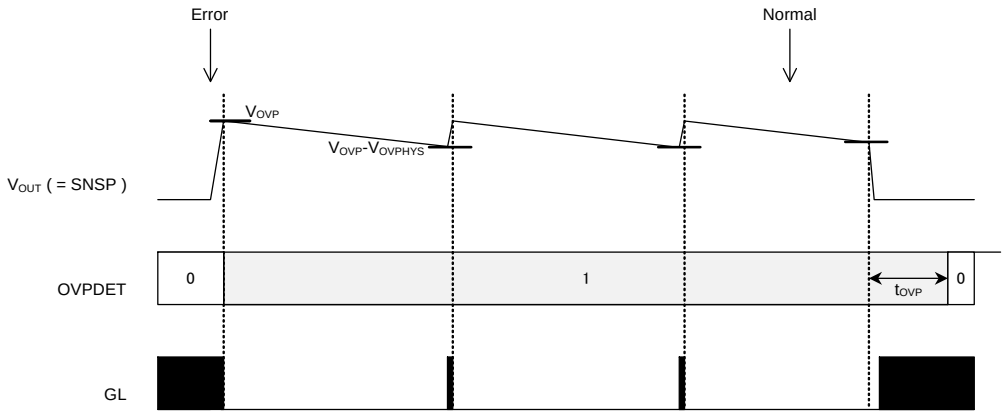


Figure 7. DCDCOVP Timing Chart (OVP)

2.7 Protection – continued

2.7.2 CHx pin Short Circuit Protection (CHxSCP)

During the CH0 to CH8 pin ground, when V_{OUT} voltage is higher than LED voltage, the current to be decided by current limit circuit will flow. IC has built-in ground short protection circuit to prevent overheating of the PMOS for current limitation. DC/DC stops when the CH0 to CH8 pin falls below V_{SCP} voltage and t_{SCP} elapses. The current limit PMOS turns off. SCPDET in the ERRDET register is updated to 1. When the CH0 to CH8 pin becomes higher than the V_{SCP_HYS} voltage, and t_{SCPREC} elapses, DC/DC reboots. SCPDET of the ERRDET register is updated to 0. Setting SCPEN of the SWRST register to 0, disables the ground fault protection function. When each CH pin is grounded, be sure to insert a backflow prevention diode between CH0 and VIN to prevent current from flowing through the parasitic diode of the By-pass switch inside the IC.

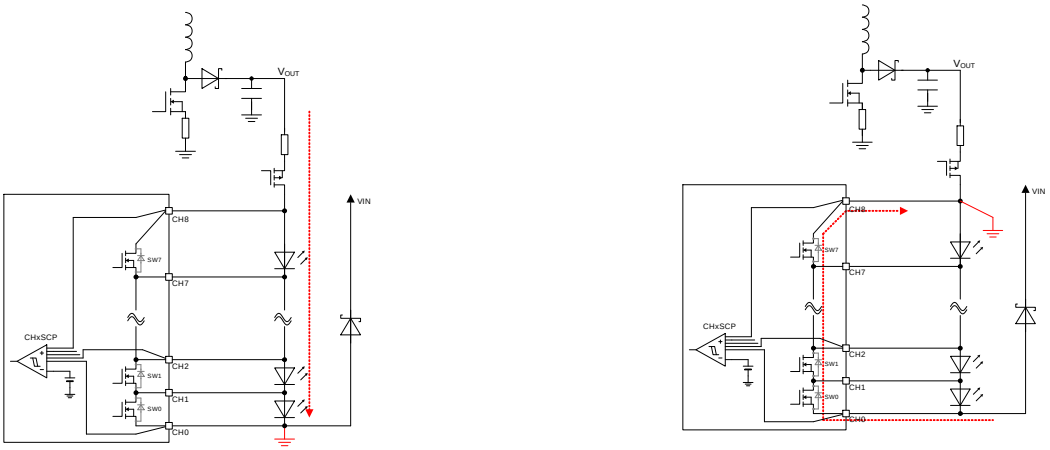


Figure 8. CHxSCP

3. Current limit part

LED Current Limit Pch-FET Drive Circuit (CURLIM)

Damages from high current in LED when rush current is generated from output capacitor when By-pass switch switches from OFF to ON (light of LED turns OFF) can be suppressed by current limit circuit. Rush current is limited by V_{SNS} + ΔV_{SNS_LIM} . To prevent overshoot brought by delayed current-limiting circuit, when the bypass switch is switched from off to on (lighting off operation), the PMOS is first turned off for 50 µs (Typ), And the bypass switch is switched while the current is limited by the PMOS.

$$I_{LED\_LIM} = \frac{V_{SNS} + \Delta V_{SNS\_LIM}}{R_{SNS}}$$

Refer to Table 20 (OCLIM Description) for ΔV_{SNS_LIM}.

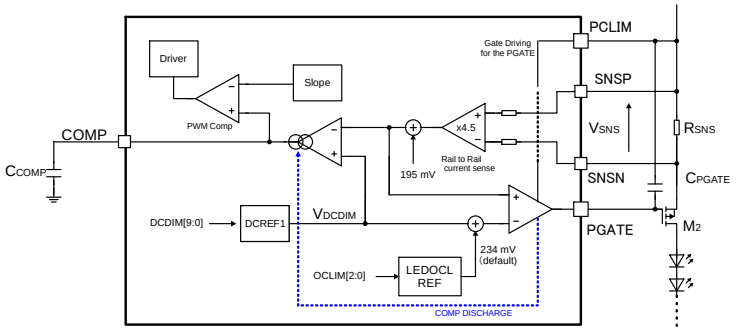


Figure 9. CURLIM

Description of Blocks – continued

4. By-pass Switch Section

4.1 By-pass Switch On/Off Control

The 8 ch By-pass switch is built-in and used by connecting a LED between CHn and CHn+1 of each switch. If 1 is set in register LEDEN, the By-pass switch turns OFF and the LED lights up with the configured duty. If set to 0, the By-pass switch is on and the LED turns off. Each By-pass switch can be individually PWM dimmed and light depends on duty set in register PWMDIM [n]. However, the PWM signal is output from the next PWM period with 1 set in LEDEN. Also, if 1 is set in register LEDFC [n], By-pass switch is turned off and the LED lights up regardless of the duty set in PWMDIM [n].

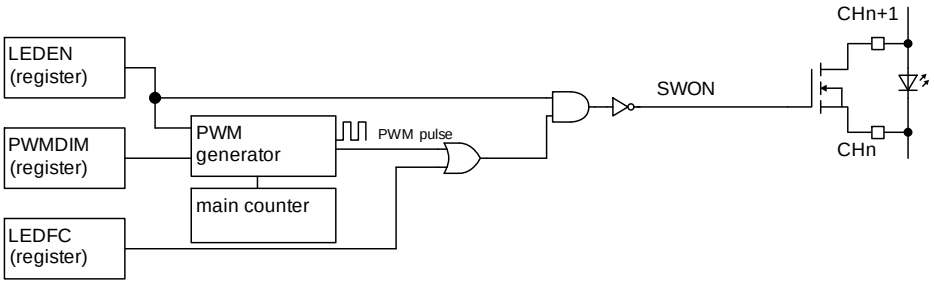


Figure 10. By-pass Switch on-off Control

It is possible to connect two LEDs in series and control them at the same time. The number of wire harnesses can be reduced. However, be careful in the design of the maximum output voltage.

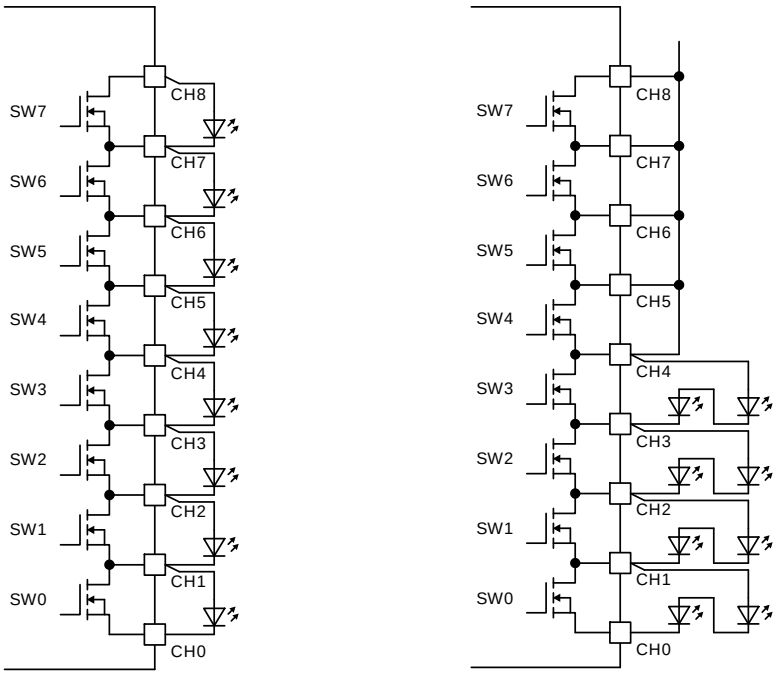
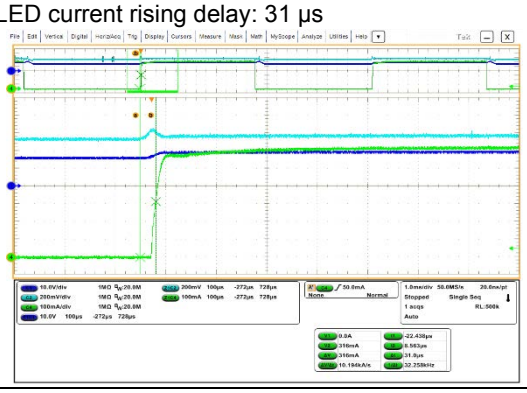
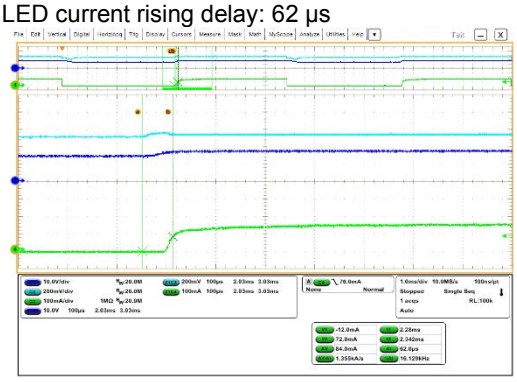
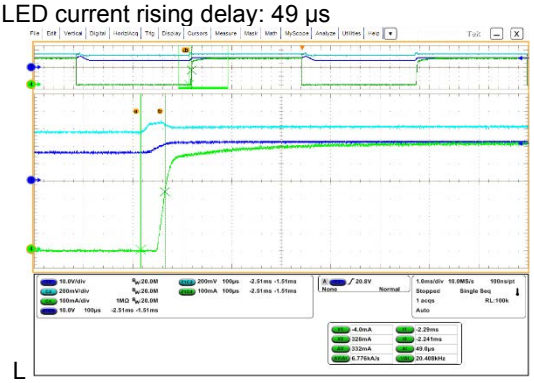
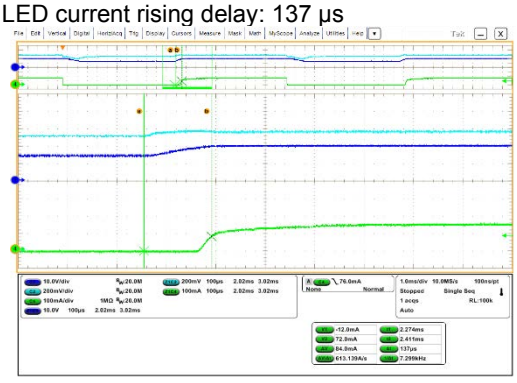
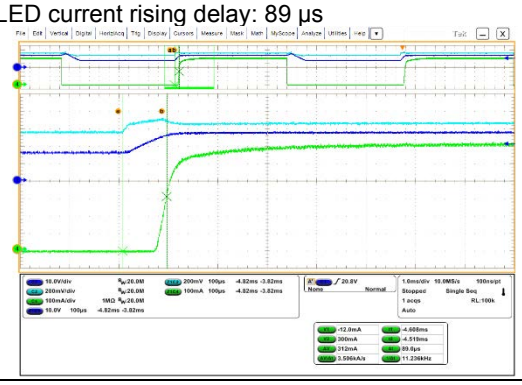
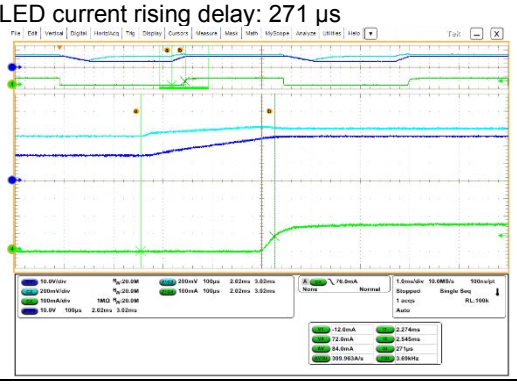
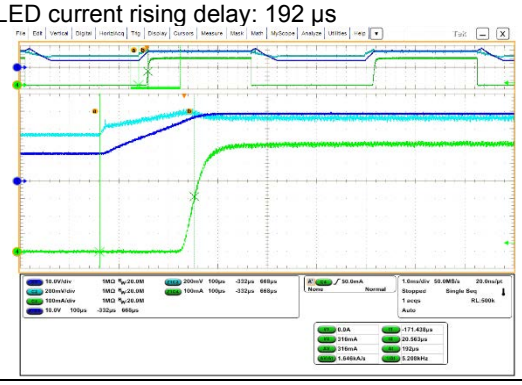


Figure 11. Example of LED8 Light Connection

4.1 By-pass Switch On/Off Control – continued

The LED current rising delay during PWM dimming by the bypass switch depends on the rising delay of the boosted voltage of the DC/DC converter. Therefore, it is determined by the number of simultaneous LED lighting, LED current setting and the COMP pin setting. The measured waveforms of the LED current rise delay for the number of simultaneous LED lights, LED current setting, and the COMP pin setting are shown below.

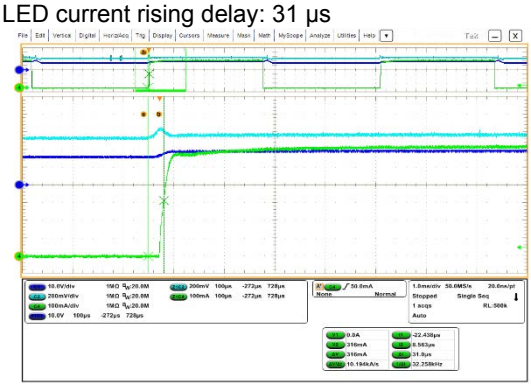
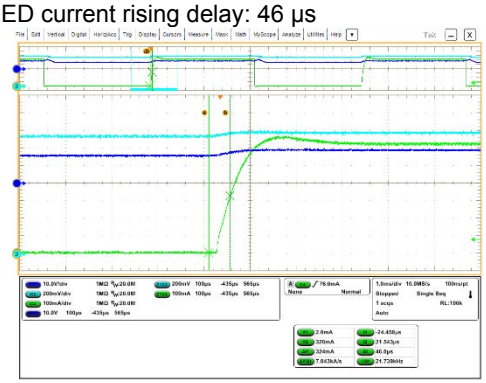
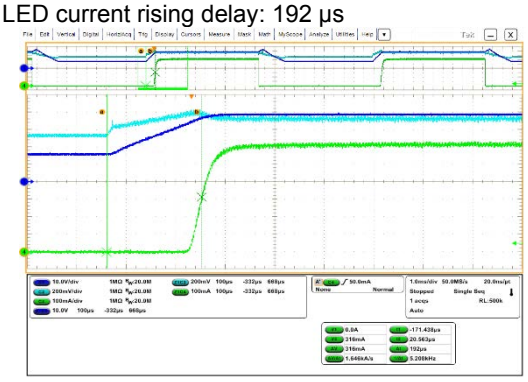
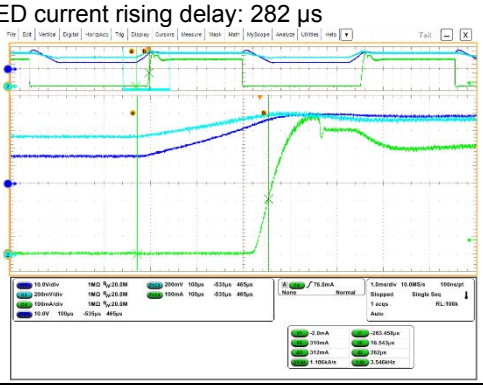
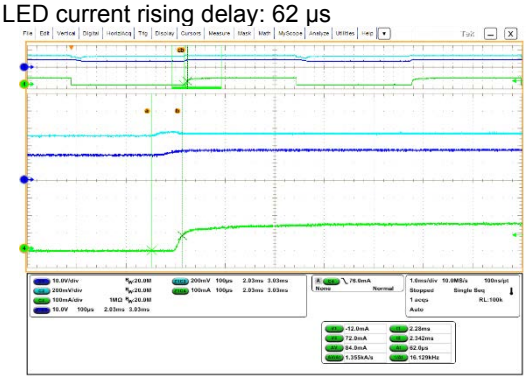
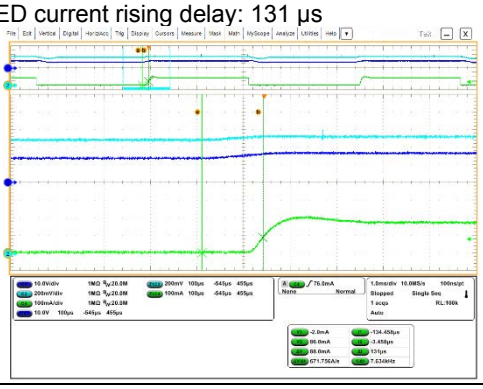
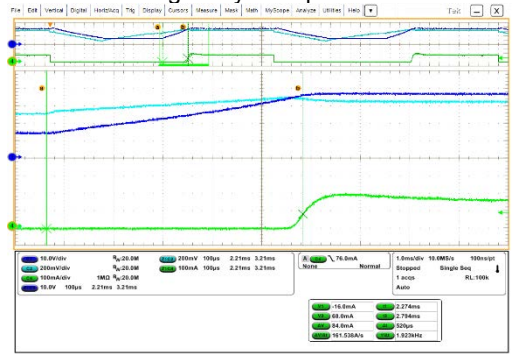
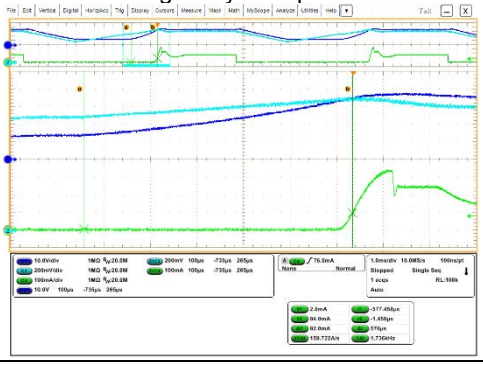
The Number of Simultaneous LED Lights: 0 LED -> 1 LED, 2 LED, 4 LED, 8 LED (LED Vf 3.0 V)
VIN = 13 V, Ta = 25 °C, C_{OUT} = 12.5 µF, C_{COMP} = 0.22 µF, R_{COMP} = 470 Ω, R_{SNS} = 0.82 Ω, R_{IS} = 0.051 Ω
PWM frequency 200 Hz (50 % duty), COMPDIS [1:0] = 0

	V_{SNS_100} (DCDIM [9:0] = 1023) Waveforms	V_{SNS_26} (DCDIM [9:0] = 325) Waveforms
PWM 1 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 31 µs 	LED current rising delay: 62 µs 
PWM 2 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 49 µs 	LED current rising delay: 137 µs 
PWM 4 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 89 µs 	LED current rising delay: 271 µs 
PWM 8 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 192 µs 	LED current rising delay: 520 µs 

4.1 By-pass Switch On/Off Control – continued

R_{COMP} = 470 Ω / 0 Ω, The Number of Simultaneous LED Lights: 0 LED -> 1 LED, 8 LED (LED Vf 3.0 V)

VIN = 13 V, Ta = 25°C, C_{OUT} = 12.5 µF, C_{COMP} = 0.22 µF, R_{SNS} = 0.82 Ω, R_{IS} = 0.05 Ω,
PWM frequency 200 Hz (50 % duty), COMPDIS [1:0] = 0.

	V_{SNS_100} (DCDIM [9:0] = 1023) waveforms R_{COMP} = 470 Ω	V_{SNS_100} (DCDIM [9:0] = 1023) waveforms R_{COMP} = 0 Ω
PWM 1 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 31 µs 	LED current rising delay: 46 µs 
PWM 8 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 192 µs 	LED current rising delay: 282 µs 
	V_{SNS_26} (DCDIM [9:0] = 325) waveforms R_{COMP} = 470 Ω	V_{SNS_26} (DCDIM [9:0] = 325) waveforms R_{COMP} = 0 Ω
PWM 1 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 62 µs 	LED current rising delay: 131 µs 
PWM 8 LED 1 ch: V_{OUT} Voltage (200 mV/div) 2 ch: COMP Voltage (10 V/div) 4 ch: LED Current (100 mA/div)	LED current rising delay: 520 µs 	LED current rising delay: 576 µs 

4. By-pass switch section – continued

4.2 Phase Shift

When the By-pass switch turns on, DC/DC output voltage decreases significantly. It is possible to shift the timing at which each switch is turned on to suppress voltage fluctuations.
For details, refer to the explanation of the page 30 "PHEN" register setting.

4.3 LED Short Detection

Each By-pass switch has LED Short detection function.

Detect
The voltage between CHn+1 and CHn are monitored while (LED current is generated and under the SGB release condition, and) the By-pass switch is off. When less than LED Short detection voltage (V_{CHLS}), LED Short time tLS passes detect LED Short. The LEDSHORT [n] of diagnostic register LEDSHORT and LEDSHORTALL of ERRDET are updated into 1.

Release
The voltage between CHn+1 and CHn are monitored while (LED current is generated and under the SGB release condition, and) the By-pass switch is off. When higher than LED Short detection voltage (V_{CHLS}), LED Short time t_{LS} passes, LEDSHORT [n] of diagnostic register LEDSHORT [n] and LEDSHORTALL of ERRDET are updated to 0.
When LEDEN [n] is set to 0, LEDSHORT [n] of diagnostic register LEDSHORT and LEDSHORTALL of ERRDET are updated to 0.

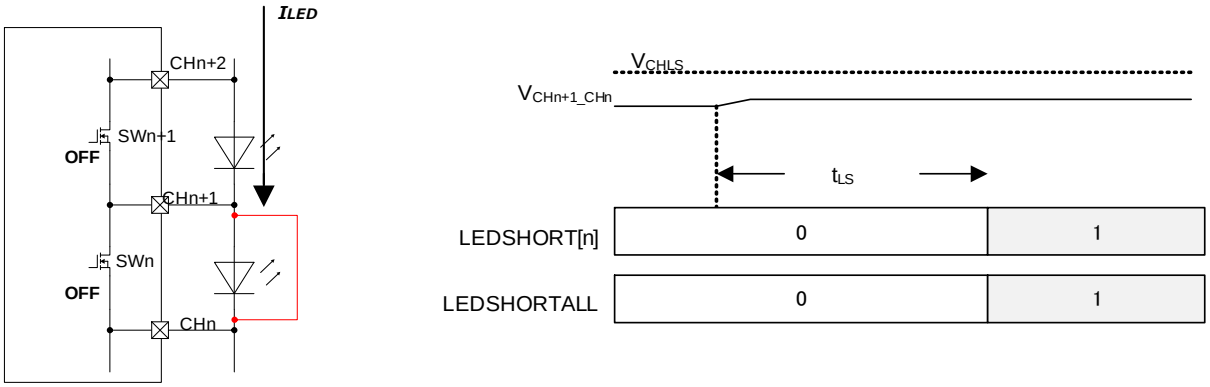


Figure 12. LED Short Detection

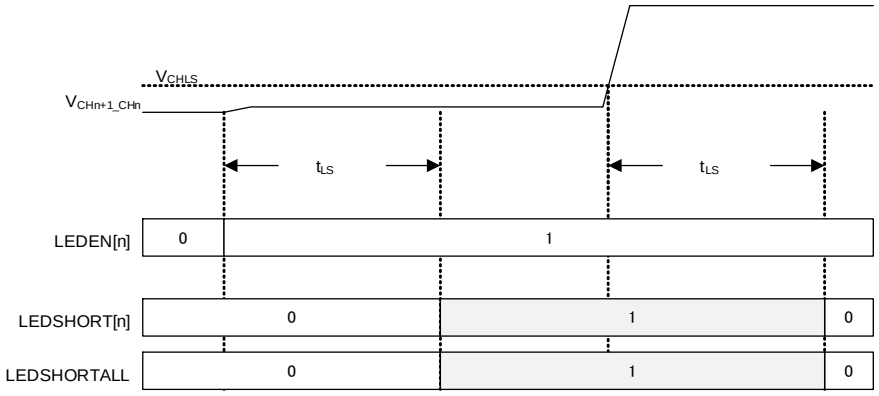


Figure 13. LED Short Detection Release

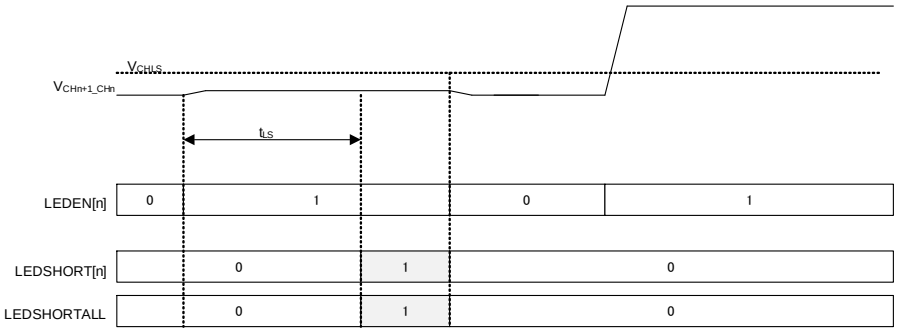


Figure 14. LED Short Detection Release (LEDEN Control)

4.3 LED Short Detection – continued

This section describes the mask time t_{LS} counting operation for LED Short detection.

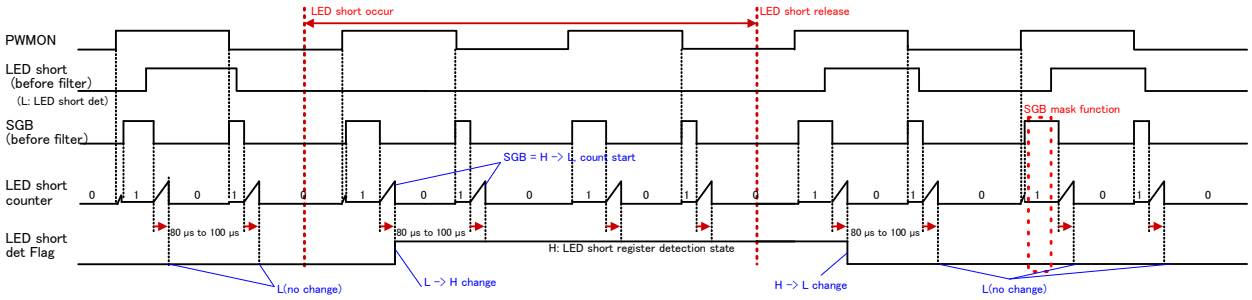


Figure 15. LED Short detection and release
(During PWM control, SGB signal and counter status)

The figure above is the timing chart LED Short detection and SGB signal (detection state at high: LED current is not sufficiently generated).
LED short is detected with low condition (PWMON = H) and SGB = low, and LED short detection flag = 1.
Since the LED short function at DC/DC startup is masked with SGB = high, LED short is not erroneously detected.

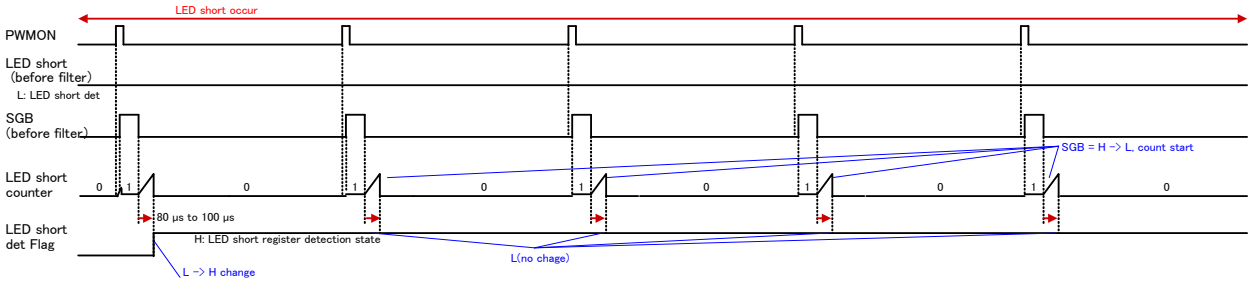


Figure 16. LED Short Detection
(In the case of low duty that cannot be sufficiently boosted LED voltage during PWM control.)

If the LED voltage is not boosted sufficiently due to low PWM duty, the LED short detection flag = 1 will be set in the logic of the LED short state detected when PWMON = H after SGB = H -> L.

4.3 LED Short detection – continued

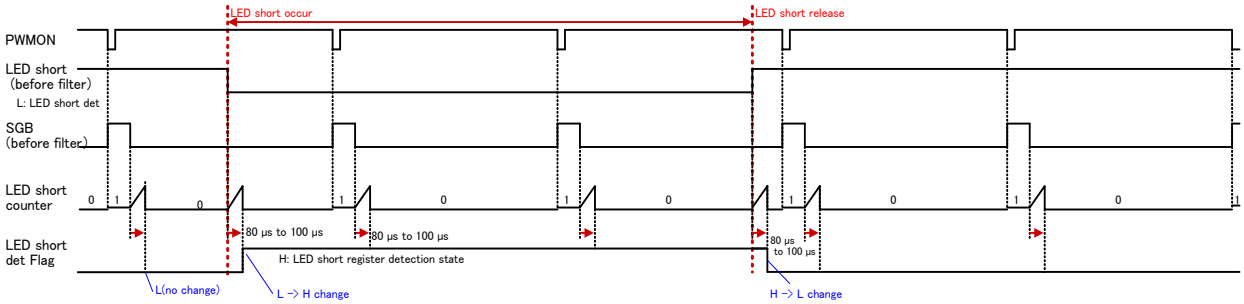


Figure 17. LED Short detection (Maximum Duty, During PWM Control)

LED short is detected with detection condition (PWMON = H) and SGB = low, and LED short detection flag = 1.

4.4 LED Open Detection

Each By-pass switch has LED open detection function.

Detection

CHn and CHn+1 voltages are monitored while the By-pass switch is off to detect LED open when it becomes greater than LED open detection voltage (V_{CHLO1}, V_{CHLO2}). When detecting LED open, the By-pass switch turns on to prevent destruction. (Latch) LEDOPEN [n] of the diagnostic register LEDOPEN and LEDOPENALL of ERRDET are updated to 1.

Release

If LEDEN [n] is set to 0, the latch is released. LEDOPEN [n] of diagnostic register LEDOPEN and LEDOPENALL of ERRDET are updated to 0.

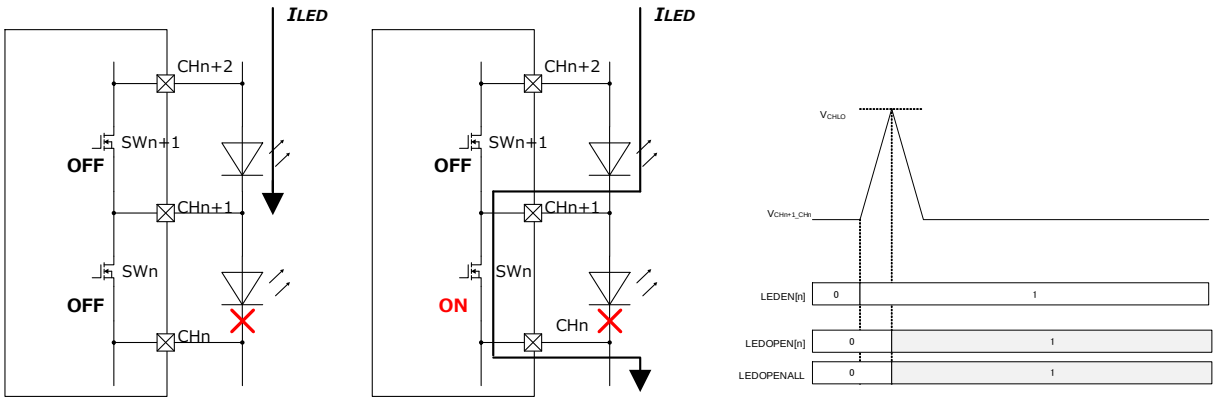


Figure 18. LED Open Detection

4.4 LED open detection – continued

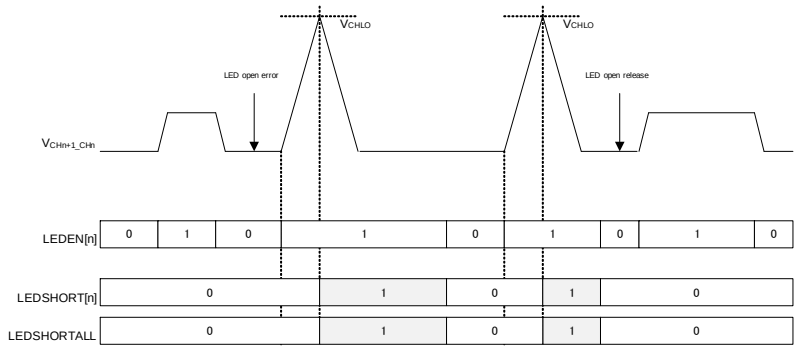


Figure 19. LED Open Detection Release (When LEDEN Control)

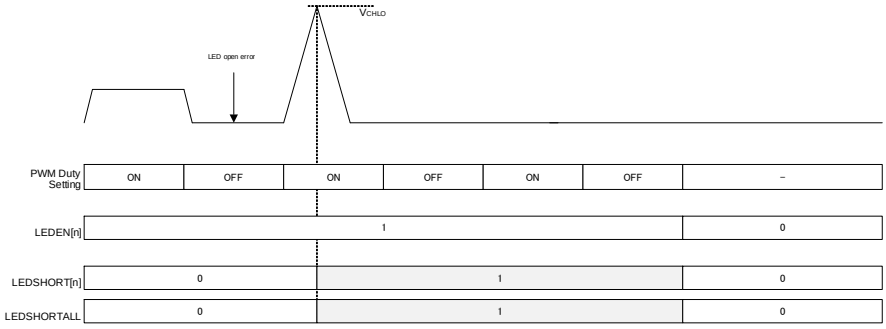
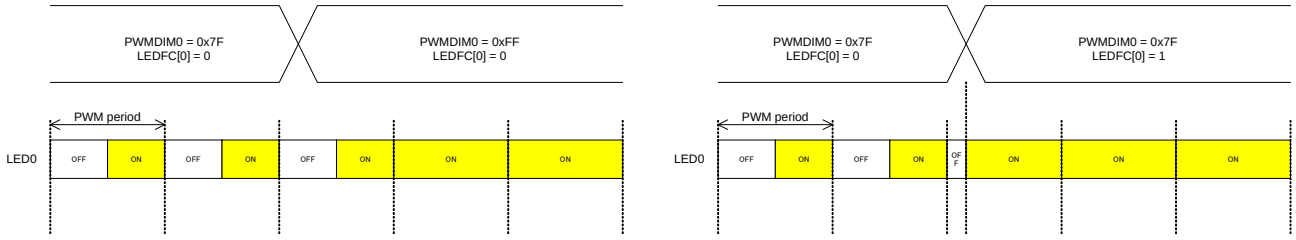


Figure 20. LED Open Detection Release (PWM Control)

4.5 Forced-LED Lighting Control

When switching from PWM dimming to 100 % Duty, updating with the PWMDIM register setting may delay the switch depending on the timing of the communication. Setting LEDFC [n] = 1 in the LEDFC register does not affect the PWM period when transmitting data, and the By-pass switch is turned off.



(a) Control by PWM dimming settings (b) Control by forced LED lighting

Figure 21. Forced LEDON Control

4. By-pass switch section – continued

4.6 Open Drain Outputs For Abnormal Status (FAULT_B)

When LEDOPENALL and LEDSHORTALL of the register are updated to 1, the FAULT_B pin outputs the L level. When the register is updated to 0, the FAULT_B pin outputs Hi-z.

Table 1. Abnormal Detection/Protection Function

Function	Detecting Condition (All The Value is Typical)		Description in Detecting					
	Detection	Release	DC/DC	By-pass Switch	PGATE	COMP	Register	FAULT_B output
EN (Low)	EN pin < 0.9 V	EN pin > 1.0 V	OFF	All SWn on (LED OFF) *(Note 2)*	High (= SNSP)	Discharge	Reset	Hiz
VIN UVLO Detect	VIN pin < 4.80 V	VIN pin < 5.20 V	OFF	All SWn on (LED OFF) *(Note 2)*	High (= SNSP)	Discharge	Reset	Hiz
VDRV5 UVLO	VDRV5 < 4.10 V	VDRV5 > 4.40 V	OFF	All SWn on (LED OFF) *(Note 2)*	High (= SNSP)	Discharge	Reset	Hiz
TSD Detect	Tj > 175 °C *(Note 1)*	Tj < 150 °C	OFF	All SWn on (LED OFF) *(Note 2)*	High (= SNSP)	Discharge	Reset	Low
DC/DC OCP Detect (BSTEN = 1)	IS Pin > 300 mV	IS Pin < 300 mV	OFF	-	-	-	-	Hiz
OVP Detect (OVPSET [3:0] = 10) (BSTEN = 1)	SNSP Pin > 56.6 V	SNSP Pin < 54.8 V	OFF	-	High (= SNSP)	Discharge	OVPDET (Release after 20 ms)	Low (Release after 20 ms)
CHxSCP (BSTEN = 1)	CHx Pin < 0.9 V And After 50 µs	CHx Pin > 2.0 V And After 20 ms	OFF	-	High (= SNSP)	Discharge	SCPDET (Release after 20 ms)	Low (Release after 20 ms)
LED Short Detect	LEDEN = 1, V_{CHn+1_CHn} < 1.0 V and V_{SNS} > 13.6 mV After 100 µs	LEDEN = 1, V_{CHn+1_CHn} > 1.0 V and V_{SNS} > 13.6 mV After 100 µs or LEDEN = 0	- Don't care	- Don't care	- Don't care	- Don't care	LED SHORT [n] LEDSHORT ALL	Low
LED Open Detect (LEDOPSETn = 0)	LEDEN = 1, V_{CHn+1_CHn} > 6.0 V	LEDEN = 0	- Don't care	SWn on (LED OFF) Depend on detect ch	- Don't care	- Don't care	LEDOPEN [n] LEDOPEN ALL	Low
LED Average Current Status (BSTEN = 1)	V_{SNS} Voltage < 11.1 mV After 10 ms	V_{SNS} Voltage > 13.6 mV After 1 ms	- Don't care	- Don't care	- Don't care	- Don't care	SGB	Hiz
CRC Error	CRC Error	ERRCLR = 1	- Don't care	- Don't care	- Don't care	- Don't care	CRCER	Low
Watch Dog Timer Error	WDTEN = 1 No Access Over 100 ms	ERRCLR = 1	- Don't care	- Don't care	- Don't care	- Don't care	WDTDET	Low

(Note 1) TSD does not work below Tj = 150 °C.

(Note 2) Due to the reset condition, the bypass switch section has SW ON logic, but the boost DC/DC section stops, so the PSW pin voltage, which is the power supply for the SW section, drops, and finally the SW turns OFF. At the same time, PGATE turns off PMOS, so the LED turns off.

Description of Blocks – continued

5. UART

5.1 UART Protocol and AC Electrical Characteristics

UART Interface (UART) controls the IC with RX and TX signals. In the start of UART communication the initial value of RX and TX is 'Hi-z' (high). The format of a frame consist of 10-bits: start bit, 8-bit data and stop bit. Data is sent from LSB first. This IC synchronizes timing every stop/start bit. Hence, when MCU read data, it is synchronized every stop/start bit.

Figure 22. Data Format of a Frame

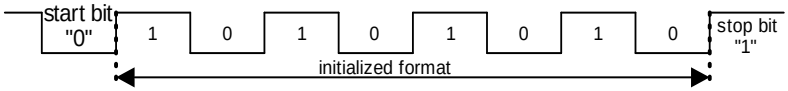


Figure 23. Clock Synchronization (SYNC)

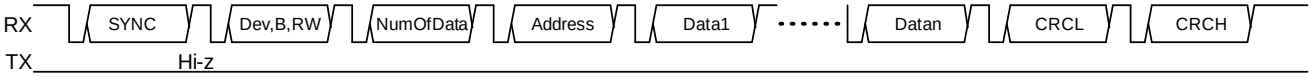


Figure 24. UART Protocol (Write)

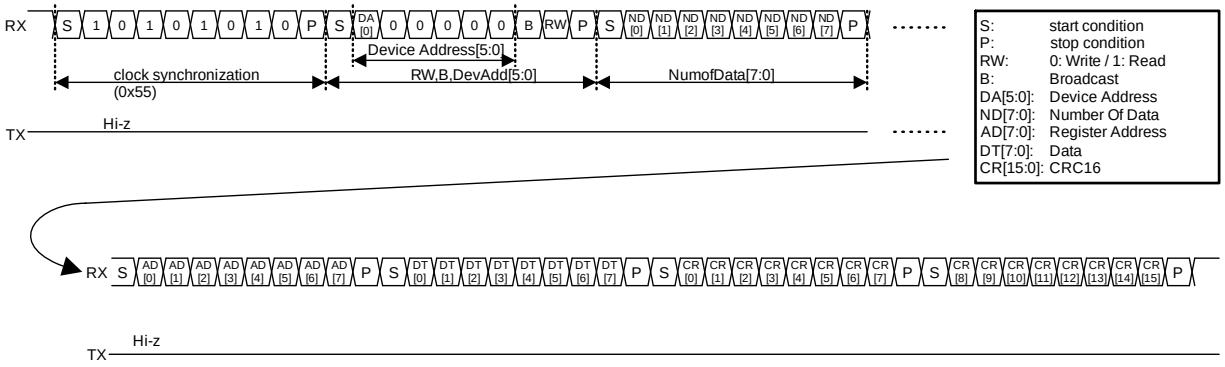


Figure 25. Detail of UART Protocol (Write)

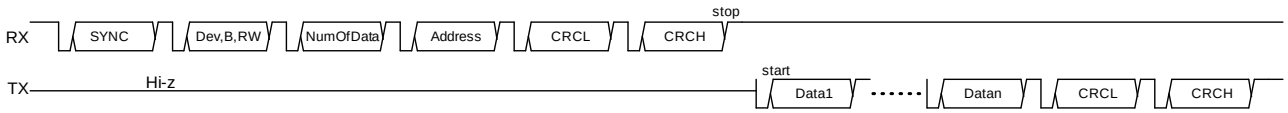


Figure 26. UART Protocol (Read)

Communication Reset

This IC has a communication reset function. This interface circuit can be recovered from abnormal condition of UART communication with this function. Set RX to Low for 12 consecutive cycles based on baud rate used. Set RX to Low over 500 µs to invoke communication reset. If communication reset is executed, register value do not change, it will not affect LED Dimming.

5. UART – continued

5.2 UART AC Timing chart

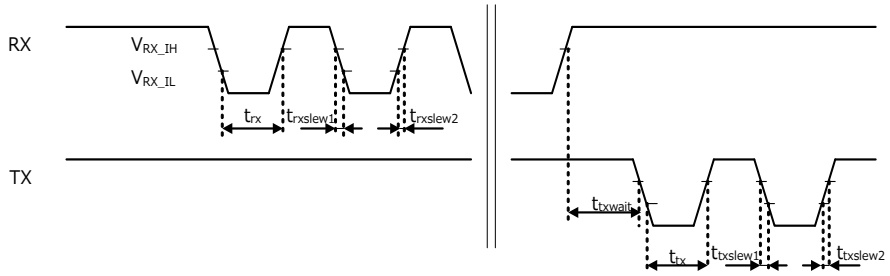


Figure 27. UART AC Timing

Table 2. UART AC characteristics

Recommended Operation Condition (Unless otherwise specified, Tj = -40 °C to +150 °C, VIN = 13 V)

Parameter	Symbol	Rating			Unit	Comments
		Min	Typ	Max		
RX Transfer Time	t_{rx}	2	-	20	µs	
TX Transfer Time	t_{tx}	2	-	20	µs	
TX Output Delay Time	t_{txwait}	0.5	1	1.5	bit	
RX Slew Rate High -> Low	$t_{rxslew1}$	-	-	t_{rx} x 10 %	µs	
RX Slew Rate Low -> High	$t_{rxslew2}$	-	-	t_{rx} x 10 %	µs	
TX Slew Rate High -> Low	$t_{txslew1}$	-	-	t_{tx} x 10 %	µs	
TX Slew Rate Low -> High	$t_{txslew2}$	-	-	t_{tx} x 10 %	µs	
TX Output Tolerance	TX_{tore1}	-6.25	-	+6.25	%	Baud rate at 500 kHz to 200 kHz, use synchronized to each START bit.
	TX_{tore2}	-3.75	-	+3.75	%	Baud rate under 200 kHz, use synchronized to each START bit.

(Output load capacitance: 15 pF)

5. UART – continued

5.3 UART Protocol

5.3.1 Initialize Format

bit 7	bit 6	bit 5	bit 4	Bit 3	Bit 2	bit 1	bit 0
0	1	0	1	0	1	0	1

MCU sends 55 h (0101_0101b) to the IC to adjust communication rate. IC will receive the data and determine the baud rate of the incoming command. IC generates internal sampling time based on the computed baud rate (1-bit period / 2).

After sending SYNC byte, BD18364EFV-M expects succeeding frames have the same data rate as that of SYNC frame. If incorrect input timing occurred it will trigger CRC error.

5.3.2 Device address, Broadcast, Write/Read

bit 7	bit 6	bit 5	bit 4	Bit 3	Bit 2	bit 1	bit 0
RW	B	DA [5:0]					

bit	Parameter	Function
DA [5:0]	Device Address	We can set “000000b” or “000001b”. DA [0] = CS setting DA [1] = 0 DA [2] = 0 DA [3] = 0 DA [4] = 0 DA [5] = 0

bit	Parameter	Function
B	Broadcast	0: It accesses register to device which matched device address. 1: It accesses register to all device.

Note:
1. Broadcast is not possible for Read access.
2. If Broadcast = 1; ignore device address setting.

bit	Parameter	Function
RW	Read/Write	0: Write access 1: Read access

5.3.3 Number of Data

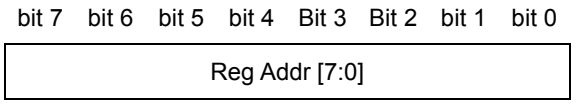
bit 7	bit 6	bit 5	bit 4	Bit 3	Bit 2	bit 1	bit 0
Num of Data [7:0]							

bit	Parameter	Function
Num of Data [7:0]	Number of Data transferred	It is available to use from 1 to 10

Note:
1. Available data buffer for multiple write access is maximum 10 data.
2. Num of Data = 0 is not valid
3. Num of Data > 10 is not valid

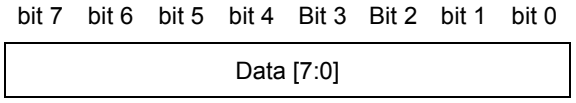
5.3 UART Protocol – continued

5.3.4 Register Address



bit	Parameter	Function
Reg Addr [7:0]	Register Address	It is available to access from 0x00 to 0x15

5.3.5 Data



bit	Parameter	value
Data [7:0]	Data	0x00 to 0xFF

5.3 UART Protocol – continued

5.3.6 CRC

16 bit LSB First
Cyclic Redundancy Check (CRC)

The CRC-16 (BUYPASS) is used to detect errors in the I/F transaction data.
CRC is calculated in the order of Device address, Number of Data, Address Data, Write or Read Data.

For Write Sequence
This received CRC 2 byte data will then be compared to the computed CRC checksum.
If CRC data is the same with the computed CRC checksum, Register Map will be updated with all the written data.
Else, All written data will be disregarded.

CRC Polynomial
CRC Polynomial is expressed as :
CRC16-IBM

$$x^{16} + x^{15} + x^2 + 1$$

Bit order LSB First
The CRC calculation starts with LSB and proceeds from bit [0] to bit [7] of each byte.

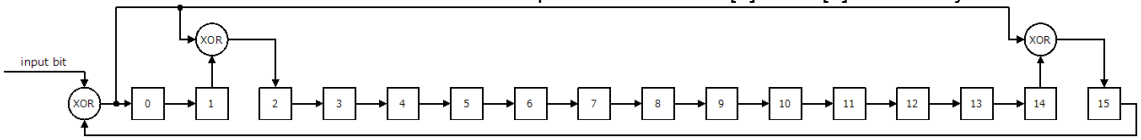


Figure 28. Polynomial

CRC Initial Setting
The initial value is “0000h”.
The CRC calculate registers are reset to the initial value of “0000h” prior to each CRC bytes calculation.

Example for

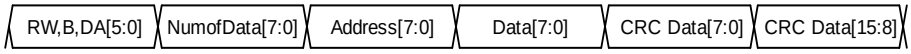


Figure 29. CRC Data format

RW, B, DA [5:0]:	DA [7:0]	= 0x01
Num Of Data [7:0]:	ND [7:0]	= 0x01
Address [7:0]:	AD [7:0]	= 0x02
Data [7:0]:	DT [7:0]	= 0xAA
CRC Data [7:0]:	CR [7:0]	= 0xC4
CRC Data [15:8]:	CR [15:8]	= 0x8B

5.3.7 Example of UART Protocol

Single device, 1 byte Write (Write to Device #1)

B =	0:	Target Device Receives the Data
RW =	0:	Write
Dev Addr [5:0] =	0x01:	Target Device Address
Num Of Data [7:0] =	1:	1 byte Write Mode
Reg Addr [7:0] =	0x02:	Address
Data [7:0] =	0xAA:	Data

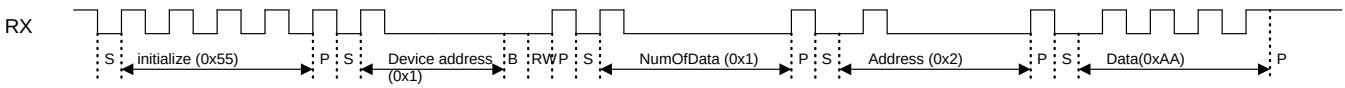


Figure 30. UART Protocol of the 1 byte Write to Device #1

5. UART – continued

5.4 Register Map

All registers except PWMDIM (LEDEN = 0 -> 1) are updated immediately.
PWMDIM function is applied on the next PWM timing.

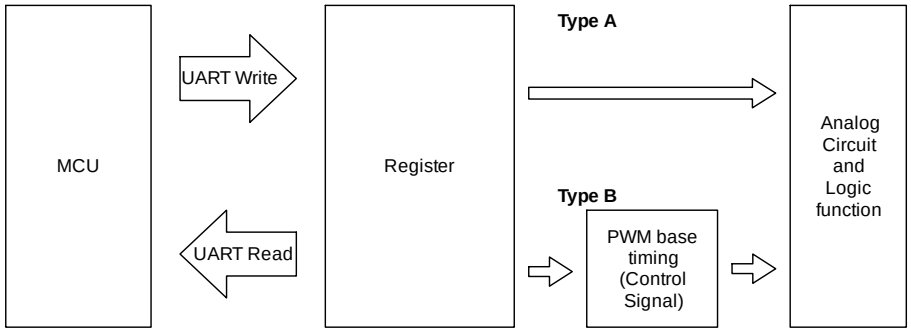
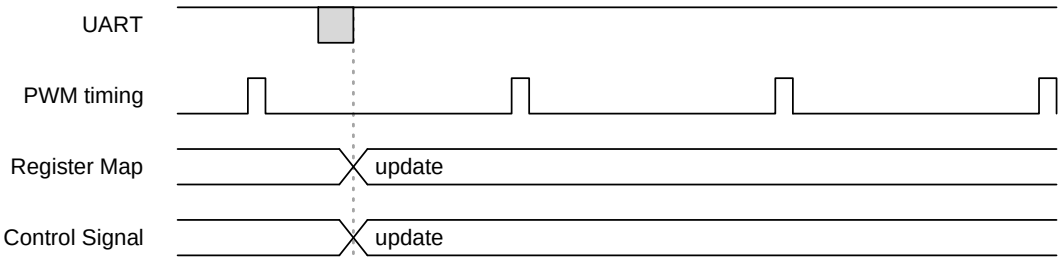


Figure 31. Data Update Image

Type A update immediately:
All registers except for TypeB registers



Type B update at internal PWM timing:
PWMDIMn, LEDEN(only 0 -> 1 setting)

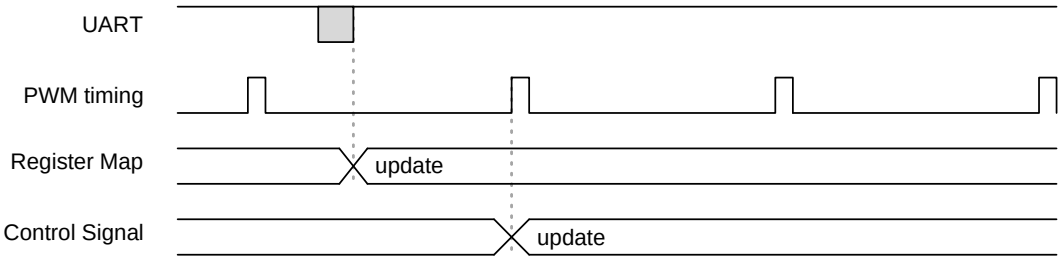


Figure 32. Data Update Image Timing Chart

5.4 Register Map – continued

Table 3. Register MAP

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	initial	update timing
SWRST	0x00	ERRCLR	FAULTBCNT	FAULTBEN	SYNCEREN	WDTEN	CURLIMEN	SCPEN	SWRST	R/W	0x06	Type A
SYSSET1	0x01	-	VINDIM[2:0]			SSFM[2:0]			BSTEN	R/W	0x00	Type A
SYSSET2	0x02	COMPDIS_EN	COMPDIS[1:0]		-	OVPSET[3:0]				R/W	0x0A	Type A
LEDOPSET	0x03	LEDOPSET[7:0]								R/W	0x00	Type A
SYSSET3	0x04	reserved		PWMSYNCEN	PHEN	FPWM[3:0]				R/W	0xC1	Type A
ADCTRL	0x05	-	-	-	-	-	-	-	AD_TRIG	WO	0x00	Type A
ADSTORE	0x06	AD_STORE[7:0]								RO	0x00	Type A
DCDIMH	0x07	DCDIM[9:2]								R/W	0x8A	Type A
DCDIML	0x08	OCLIM[2:0]			-	-	-	DCDIM[1:0]		R/W	0x00	Type A
PWMDIM0	0x09	PWMDIM0[7:0]								R/W	0xFF	Type B
PWMDIM1	0x0A	PWMDIM1[7:0]								R/W	0xFF	Type B
PWMDIM2	0x0B	PWMDIM2[7:0]								R/W	0xFF	Type B
PWMDIM3	0x0C	PWMDIM3[7:0]								R/W	0xFF	Type B
PWMDIM4	0x0D	PWMDIM4[7:0]								R/W	0xFF	Type B
PWMDIM5	0x0E	PWMDIM5[7:0]								R/W	0xFF	Type B
PWMDIM6	0x0F	PWMDIM6[7:0]								R/W	0xFF	Type B
PWMDIM7	0x10	PWMDIM7[7:0]								R/W	0xFF	Type B
LEDEN	0x11	LEDEN[7:0]								R/W	0x00	Type B
LEDFC	0x12	LEDFC[7:0]								R/W	0x00	Type A
ERRDET	0x13	CRCER	SGB	-	WDTDET	LEDSHORTALL	LEDOPENALL	SCPDET	OVPDET	RO	0x00	Type A
LEDOPEN	0x14	LEDOPEN[7:0]								RO	0x00	Type A
LEDSHORT	0x15	LEDSHORT[7:0]								RO	0x00	Type A

Reset Condition
EN = Low, VDRV5 UVLO, VIN UVLO, TSD, SWRST = 1 (Except for SWRST register)
R/W: Read/Write, WO: Write only, RO: Read only
There are two Update timing for LEDEN. LEDEN (0 -> 1 setting) is Type B. LEDEN (1 -> 0 setting) is Type A.

5. UART – continued

5.5 Description of Registers

●Address 0x00: SWRST Software reset [Read/Write] initial value 0x06

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	ERRCLR	FAULTBCNT	FAULTBEN	SYNCEREN	WDTEN	CURLIMEN	SCPEN	SWRST
Initial value	0	0	0	0	0	1	1	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit [0] SWRST
Set '1' in this register when you want to reset digital circuit.
SWRST register return '0' automatically.

Table 4. SWRST Description

SWRST	reset
0	Normal
1	Reset for digital circuit (return '0' automatically)

bit [1] SCPEN
This register is enabled for "CHx pin Short Circuit Protection " function.

Table 5. SCPEN Description

SCPEN	operation
0	It is not available to use SCP function. SCPDET register is '0'.
1	It is available to use SCP function

bit [2] CURLIMEN
This register is enabled for current limiter.

Table 6. CURLIMEN Description

CURLIMEN	operation
0	It is not available to control AMP for current limit. (OFF)
1	It is available to control AMP for current limit.

bit [3] WDTEN
This register is setting of WDT enable. This timer is reset by CRC OK.
FAULT_B = Low and WDTDET = 1 when WDTEN = 1 and no UART access during 100 ms (Typ).

Table 7. WDTEN Description

WDTEN	operation
0	UART Watch Dog Timer is disable
1	UART Watch Dog Timer is enable

bit [4] SYNCEREN
Set only '0'. '1' is prohibit.

Table 8. SYNCEREN Description

SYNCEREN	operation
0	Default. (do not change)
1	prohibit

5.5 Description of Registers – continued

bit [5] FAULTBEN
bit [6] FAULTBCNT
When FAULTBEN = 1, the FAULT_B pin is controlled by FAULTBCNT register.

Table 9. FAULTBEN and FAULTBCNT Description

FAULTBEN	FAULTBCNT	FAULT_B
0	0	error status
	1	
1	0	Low
	1	High (Hi-z)

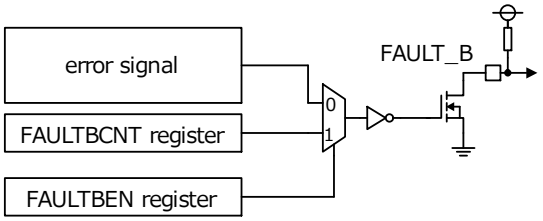


Figure 33. FAULT_B Controlled

bit [7] ERRCLR
"UART Watch Dog Timer Error condition" and "CRC error" clear.
The WDTDET and CRCER register are cleared by set '1' in this register.
FAULT_B will de-assert.
ERRCLR register return '0' automatically.

Table 10. ERRCLR Description

ERRCLR	operation
0	Normal
1	WDTDET and CRCER are cleared and FAULT_B de-asserts.

5.5 Description of Registers – continued

●Address 0x01: SYSSET1 system setting1 [Read / Write] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	-	VINDIM [2:0]			SSFM [2:0]			BSTEN
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit [0] BSTEN
This register controls Boost enable.

Table 11. BSTEN Setting

BSTEN	DC/DC operation
0	DC/DC OFF
1	DC/DC ON

bit [3:1] SSFM [2:0]
This register controls SSCG ON/OFF and modulation frequency.

Table 12. SSFM Setting

SSFM[2:0]	SSCG modulation ratio
0	SSCG OFF (Fixed frequency of DC/DC)
1	137 Hz
2	183 Hz
3	275 Hz
4	366 Hz
5	549 Hz
6	732 Hz
7	1,099 Hz

bit[6:4] VINDIM
VIN derating start voltage setting.
This IC has protection for input current. If input voltage (VIN) is down, it flows big current. So it controls output current for decreasing input current. This register is setting of voltage of “derating start threshold”. If VIN voltage is down and under UVLO, it controls V_{SNS} = 0 V. Refer description (Description of Blocks “2. LED Driver Section / 2.4 Input Voltage (VIN) Derating”)

Table 13. VINDIM Start Setting

VINDIM	Setting
0	OFF
1	6.92 V
2	7.49 V
3	8.02 V
4	8.62 V
5	9.17 V
6	9.69 V
7	

5.5 Description of Registers – continued

●Address 0x02: SYSSET2 system setting2 [Read / Write] initial value 0x0A

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	COMPDIS_EN	COMPDIS [1:0]		-	OVPSET [3:0]			
Initial value	0	0	0	0	1	0	1	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit [3:0] OVPSET
OVP Setting Value
This register controls the threshold of voltage OVP detection.

$$V_{OVP} = OVPSET\,[3:0] \times 2.18 + 34.8\ [\mathrm{V}]$$

bit [6:5] COMPDIS
COMP Discharge current setting in “LED over current detection”

bit [7] COMPDIS_EN
COMP Discharge function setting in “LED over current detection”

Table 14. COMPDIS, COMPDIS_EN

COMPDIS_EN	COMPDIS	operation
0	*	No COMP Discharge
1	0	x1 (discharge current 180 μA)
1	1	x2 (360 μA)
1	2	x4 (720 μA)
1	3	x6 (1080 μA)

●Address 0x03: LEDOPSET LED open error detection voltage setting [Read / Write] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	LEDOPSET [7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit [7:0] LEDOPSET
This register is setting of detection voltage of LED open error.
Set this register when LEDEN = 0x00.

Table 15. LEDOPSET

LEDOPSET	Monitor	operation
[0]	SW0	0: LED open error detection voltage1 (V_{CHLO1}). 1: LED open error detection voltage2 (V_{CHLO2}).
[1]	SW1	
[2]	SW2	
[3]	SW3	
[4]	SW4	
[5]	SW5	
[6]	SW6	
[7]	SW7	

5.5 Description of Registers – continued

●Address 0x04: SYSSET3 system setting3 [Read/Write] initial value 0xC1

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	Reserved		PWMSYNCEN	PHEN	FPWM [3:0]			
Initial value	1	1	0	0	0	0	0	1

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit [3:0] FPWM

This register control PWM frequency when PWMSYNCEN register = 0.
Set this register when LEDEN = 0x00 (Set this register before starting PWM dimming and keep this value until reset.)

Table 16. PWM Frequency Setting

FPWM	PWM frequency [Hz]
0x0	200
0x1	252
0x2	300
0x3	347
0x4	400
0x5	446
0x6	504
0x7	558
0x8	600
0x9	651
0xA	710
0xB	
0xC	
0xD	
0xE	
0xF	

5.5 Description of Registers – continued

bit [4] PHEN:
Phase Shift function enable.
This register controls phase in PWM dimming.
Set this register when LEDEN = 0x00 (Set this register before starting PWM dimming and keep this value until reset.)

Table 17. PHEN Description

PHEN	Phase Shift (Delay value)	
	PWMSYNCEN	
	0	
1	SW0	0/8 x (1/FPWM)
	SW1	1/8 x (1/FPWM)
	SW2	2/8 x (1/FPWM)
	SW3	3/8 x (1/FPWM)
	SW4	4/8 x (1/FPWM)
	SW5	5/8 x (1/FPWM)
	SW6	6/8 x (1/FPWM)
	SW7	7/8 x (1/FPWM)
0	Phase Shift function is disable.	

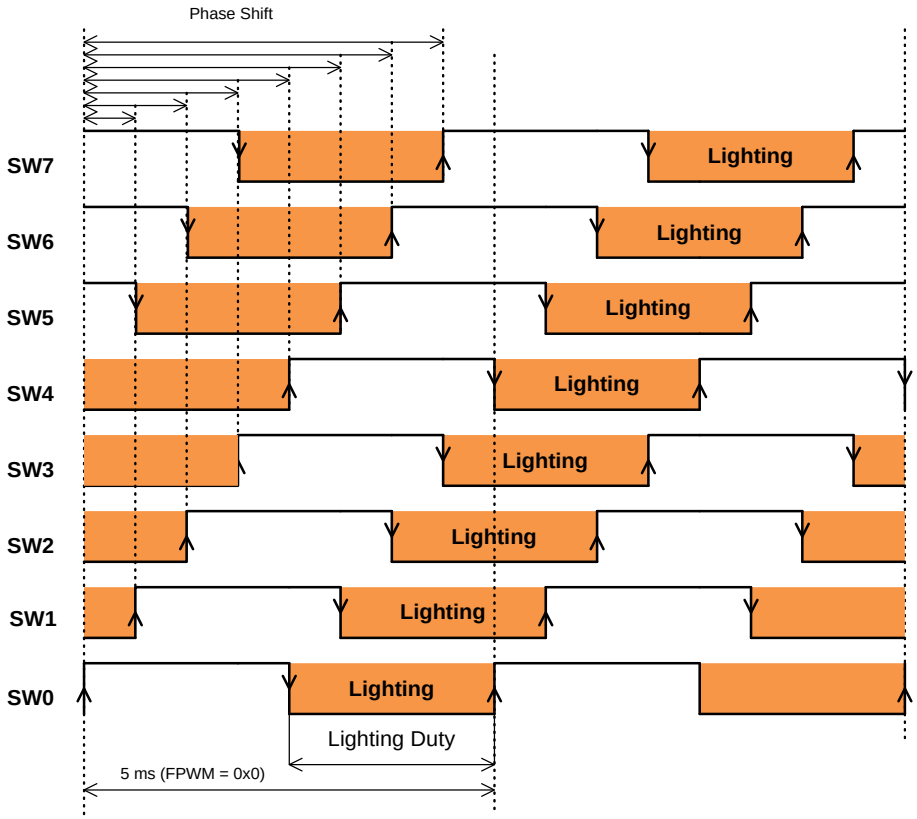


Figure 34. Phase Shift Function

5.5 Description of Registers – continued

bit [5] PWMSYNCEN
Set only '0'. '1' is prohibit.

Table 18. PWMSYNCEN Description

PWMSYNCEN	operation
0	Default (do not change)
1	Prohibit

bit [7:6] (Reserved)
Set only '3'. '0,1,2' is prohibit.

Table 19. SYSSET3 bit [7:6] Description

bit [7:6] (Reserved)	operation
0, 1, 2	Prohibit
3	Do not change

●Address 0x05: ADCTRL A/D Control [Write] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	-	-	-	-	-	-	-	AD_TRIG
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit [0] AD_TRIG
A/D Sampling Start
When this register is set to '1', A/D sampling (1 sample) will commence.
This register will auto-reset to '0' after A/D sampling finishes.

●Address 0x06: ADSTORE A/D Store Value [Read] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	AD_STORE [7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit [7:0] AD_STORE
A/D Stored Value
This register contains the sampled 8-bit value of the A/D converter.

5.5 Description of Registers – continued

●Address 0x07: DCDIMH DC current setting bit 9 to 2 [Read / Write] initial value 0x8A

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	DCDIM[9:2]							
Initial value	1	0	0	0	1	0	1	0

Update: Immediately

●Address 0x08: DCDIML DC current setting bit 1 to 0 [Read / Write] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	OCLIM [2:0]			-	-	-	DCDIM [1:0]	
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

DCDIMH, DCDIML
bit [7:0]
bit [1:0] DCDIM [9:0]:
Analog Dimming Setting by Adjusting 10-bit Reference Voltage (V_{DCDIM}) for LED current sense Voltage V_{SNS}.

$$V_{SNS} = \left(\frac{DCDIM\ [9:0]}{1024} \times 2.5\ V - 0.195\ V\right) \times \frac{1}{4.5}$$

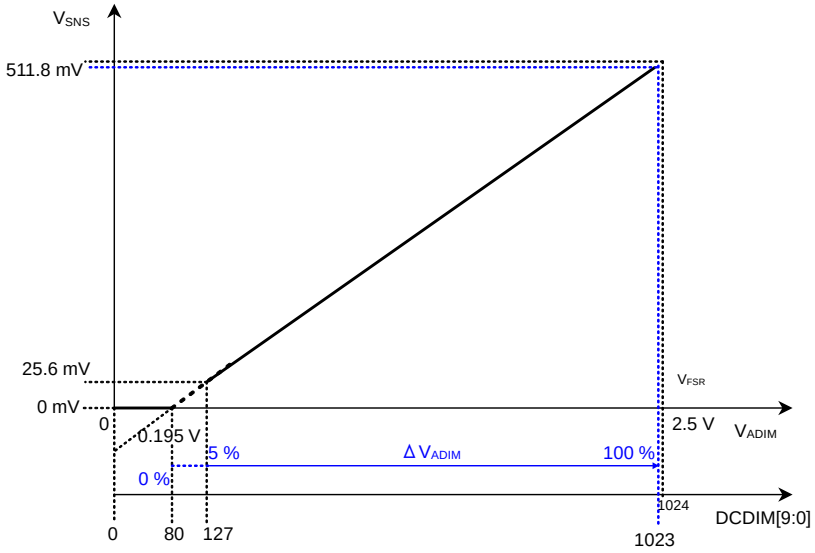


Figure 35. DCDIM Setting

bit [4:2] -

bit [7:5] OCLIM [2:0]
LED over current detection threshold is programmed by this register.

Table 20. OCLIM Description

OCLIM[2:0]	ΔV_{SNS_LIM} [V]
0	0.0520
1	0.0869
2	0.1216
3	0.1563
4	0.1910
5	0.2256
6	0.2606
7	0.2952

5.5 Description of Registers – continued

●Address 0x09: PWMDIM0 PWM dimming setting for SW0 [Read / Write] initial value 0xFF

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	PWMDIM0 [7:0]							
Initial value	1	1	1	1	1	1	1	1

Update: PWM

bit [7:0] PWMDIM0
PWM Dimming Setting for SW0
This register controls Lighting PWM duty (By-pass Switch OFF) when LEDEN [0] = 1 and LEDFC [0] = 0.
Lighting position is tail as Figure 36.

Table 21. PWMDIM0 Description

PWMDIM0	Lighting Duty [%]
0x00	0 %
0x01	0 %
0x02	0 %
0x03	0 %
0x04	0 %
0x05	2.34 %
0x06	2.73 %
0x07	3.12 %
to	
Xx	(PWMDIM0 + 1) /256
to	
0xFD	99.22 %
0xFE	99.61 %
0xFF	100.00 %

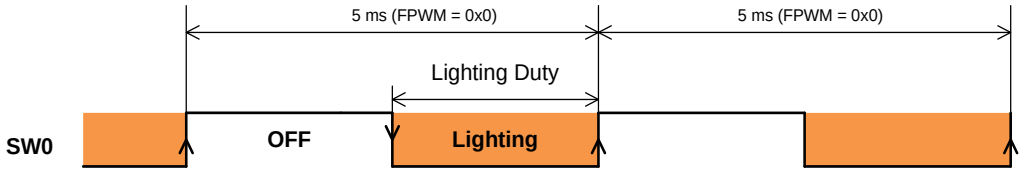


Figure 36. PWM Dimming Setting

●Address 0x0A to 0x10: PWMDIMn (n = 1 to 7)
This register is used to make PWM setting for SW1 to SW7. The setting procedure is the same as that for SW0 of Address 0x09.

5.5 Description of Registers – continued

●Address 0x11: LEDEN LED enable [Read / Write] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	LEDEN [7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: PWM/immediately

bit [7:0] LEDEN [7:0]
This register controls channel enable.
LEDEN = 1 -> 0 is updated immediately. But LEDEN = 0 -> 1 is updated same as PWMDIMn (n = 0 to 7).

Table 22. LEDEN Setting

LEDEN[n]	Description
0	LED is light OFF. (SWn = ON) If it detects “LED open error” or “LED short error”, it releases these error latched condition.
1	It is available to control PWM dimming and detect “LED open error” and “LED short error” protection.

n = 0 to 7

●Address 0x12: LEDFC LED force 100 % duty lighting [Read / Write] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	LEDFC [7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: immediately

bit [7:0] LEDFC [7:0]
This register controls PWM dimming or not. If this register is 1, PWM Duty is fixed by 100 %.

Table 23. LEDFC Setting

LEDFC[n]	Description
0	By-pass switch is controlled by PWMDIMn and LEDEN [n].
1	100 % duty lighting (SWn = OFF). Update immediately. Asynchronous with PWM cycle.

n = 0 to 7

5.5 Description of Registers – continued

●Address 0x13: ERRDET SG and Error status register [Read] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	CRCER	SGB	-	WDTDET	LEDSHORTALL	LEDOPENALL	SCPDET	OVPDET
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

bit [0] OVPDET

Table 24. OVPDET Operation

OVPDET	Description
0	Not detect “Over Voltage Protection”.
1	Detect “Over Voltage Protection”. It outputs FAULT_B = Low.

bit [1] SCPDET

This register is “CHx pin Short Circuit Protection error” status. This register is programmed by SCPEN. This status register doesn’t become 1 when SCPEN = 0.

Table 25. SCPDET Operation

SCPDET	Description
0	Not detect “CHx pin Short Circuit Protection”.
1	Detect “CHx pin Short Circuit Protection”. It outputs FAULT_B = Low.

bit [2] LEDOPENALL

This register is logical OR of each bit of LEDOPEN register.

Table 26. LEDOPENALL Operation

LEDOPENALL	Description
0	Not detect “LED open error” each SW.
1	Detect “LED open error” any of SW. It outputs FAULT_B = Low. LEDOPENALL becomes 0 when LEDOPEN [7:0] = 0x00.

bit [3] LEDSHORTALL

This register is logical OR of each bit of LEDSHORT register.

Table 27. LEDSHORTALL Operation

LEDSHORTALL	Description
0	Not detect “LED short error” in all SW.
1	Detects “LED short error” in any of SW. It outputs FAULT_B = Low. LEDSHORTALL becomes 0 when LEDSHORT [7:0] = 0x00.

bit [4] WDTDET

This register is “Watch Dog Timer error” status. This register is programmed by WDTEN. If MCU don’t communicate with this IC over 100 ms, this IC detects error. This status register doesn’t become 1 when WDTEN = 0.

Table 28. WDTDET Setting

WDTDET	Description
0	Not detect “Watch Dog Timer error”
1	Detects “Watch Dog Timer error” . It outputs FAULT_B = Low. WDTDET becomes 0 when ERRCLR = 1.

5.5 Description of Registers – continued

bit [5] -

Table 29. ERRDET bit [5]

ERRDET Bit[5]	Description
0	Default.

bit [6] SGB
LED average current status. Detect SGB condition, V_{SNS} Voltage < SGB Detect Voltage.

Table 30. LED Average Current Status

SGB	Description
0	“LED Average Current” status is good.
1	“LED Average Current” status is not good. Only monitor status. It doesn’t control FAULT_B.

bit [7] CRCER
CRC error status.

Table 31. CRC Error

CRCER	Description
0	Not detect “CRC Error”.
1	Detect “CRC Error”. FAULT_B = Low when CRCER = 1. CRCER becomes 0 by ERRCLR = 1

5.5 Description of Registers – continued

●Address 0x14: LEDOPEN LED open error status register [Read] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	LEDOPEN [7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

Table 32. LEDOPEN Setting

LEDOPEN[n]	Description
0	Not detect “LED open error” SWn.
1	Detect “LED open error” SWn Keep this value until writing LEDENn = 0

(n = 0 to 7)

●Address 0x15: LEDSHORT LED short error status register [Read] initial value 0x00

bit No	bit [7]	bit [6]	bit [5]	bit [4]	bit [3]	bit [2]	bit [1]	bit [0]
Name	LEDSHORT [7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

Table 33. LEDSHORT Setting

LEDSHORT[n]	Description
0	Not detect “LED short error” SWn.
1	Detect “LED short error” SWn Keep this value until writing LEDENn = 0 or released “LED short error”

(n = 0 to 7)

5. UART – continued

5.6 Lighting Pattern Example

No.	Dimming type	LEDEN register	LEDFC register	PWMDIM register
1	Sequential Winker (Sequential LED ON)	0xFF	Control	0x00 (0 % setting)
2	Sequential Winker (Sequential LED ON)	Control	0x00	0xFF (100 % setting)
3	Sequential Winker OFF 1 (Sequential LED OFF)	Control	0xFF	0xXX (all setting)
4	Sequential Winker OFF 2 (Sequential LED OFF)	Control	0x00	0xFF (100 % setting)

5.6.1 Sequential Winker 1 (Sequential LED ON)

LEDEN: 0xFF
LEDFC: Control
PWMDIMn: 0 % Duty Setting (All SW)

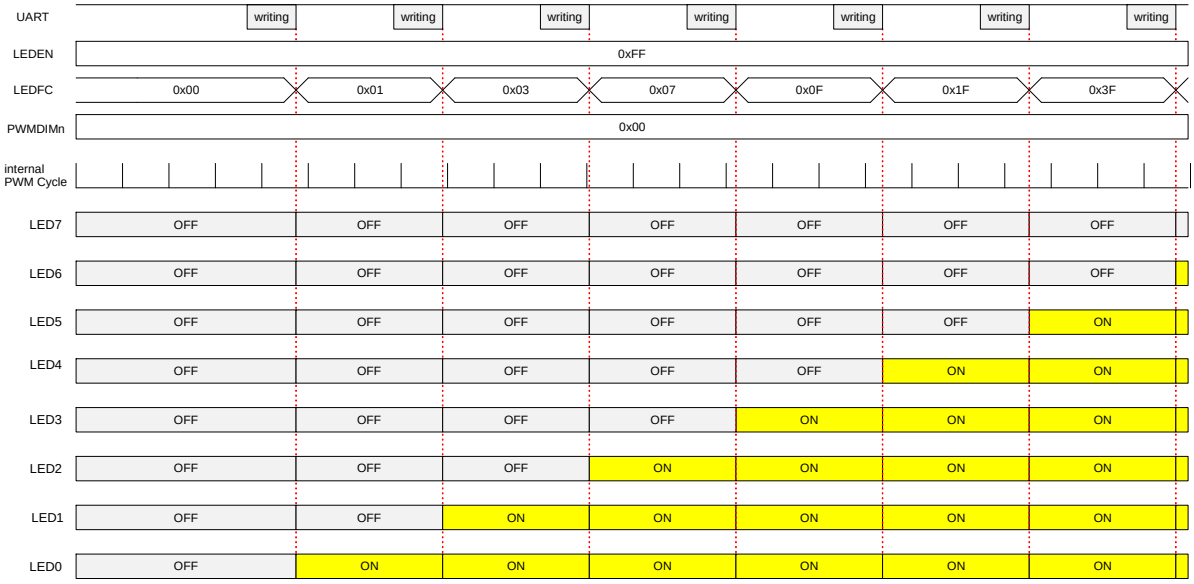


Figure 37. Sequential Winker 1 (Sequential LED ON) LEDFC Controlled

5.6 Lighting Pattern Example – continued

5.6.2 Sequential Winker 2 (Sequential LED ON)

LEDEN: Control
LEDFC: 0x00
PWMDIMn: 100 % Duty Setting (All SW)

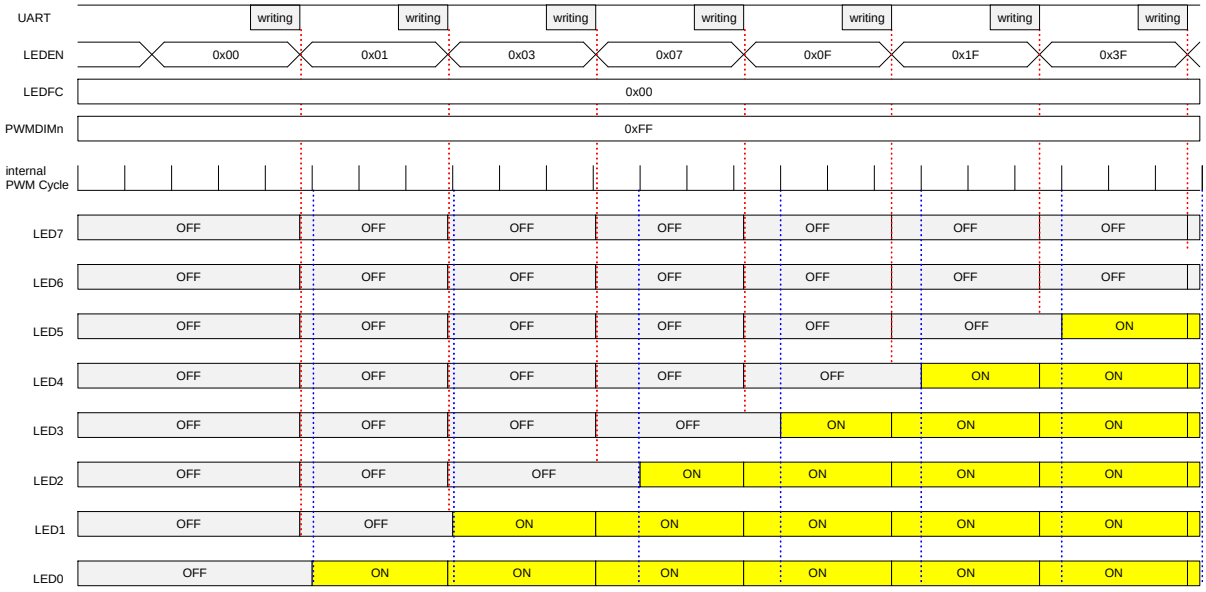


Figure 38. Sequential Winker 2 (Sequential LED ON) LEDEN Controlled

5.6.3 Sequential Winker OFF 1 (Sequential LED OFF)

LEDEN: Control
LEDFC: 0xFF
PWMDIMn: All Setting

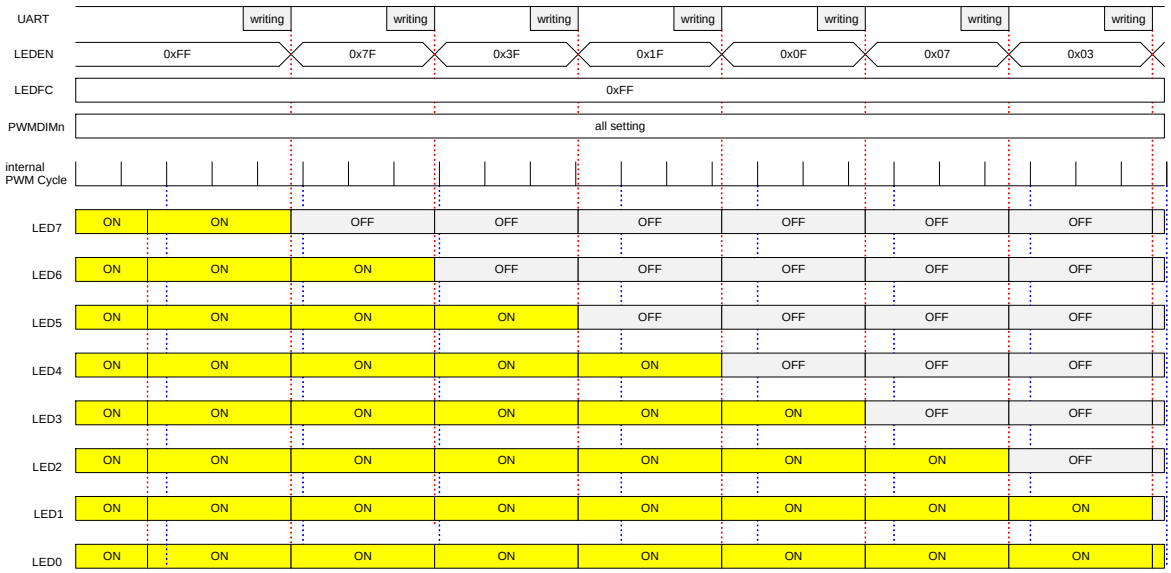


Figure 39. Sequential Winker 1 (Sequential LED OFF) LEDEN controlled

5.6 Lighting Pattern Example – continued

5.6.4 Sequential Winker OFF 2 (Sequential LED OFF)

LEDEN: Control
LEDFC: 0x00
PWMDIMn: 100 %

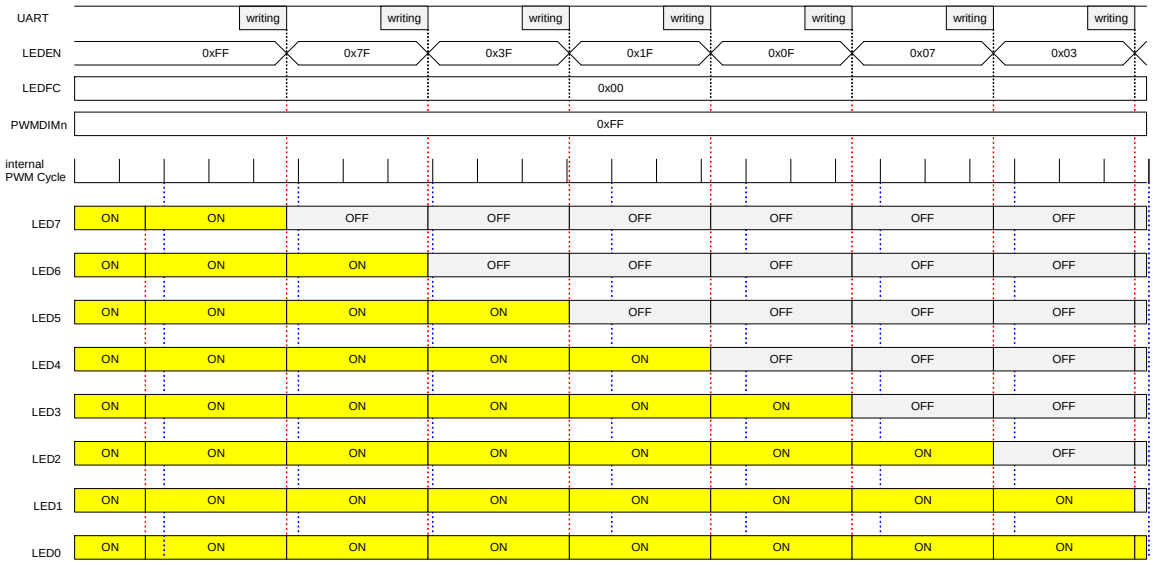


Figure 40. Sequential Winker 2 (Sequential LED OFF) LEDEN Controlled

5.6 Lighting Pattern Example – continued

5.6.5 PWM Dimming

PWM Frequency: FPWM Register
FPWM Setting: Valid
PWMSYNCEN: 0
RX Status in No Communication: High

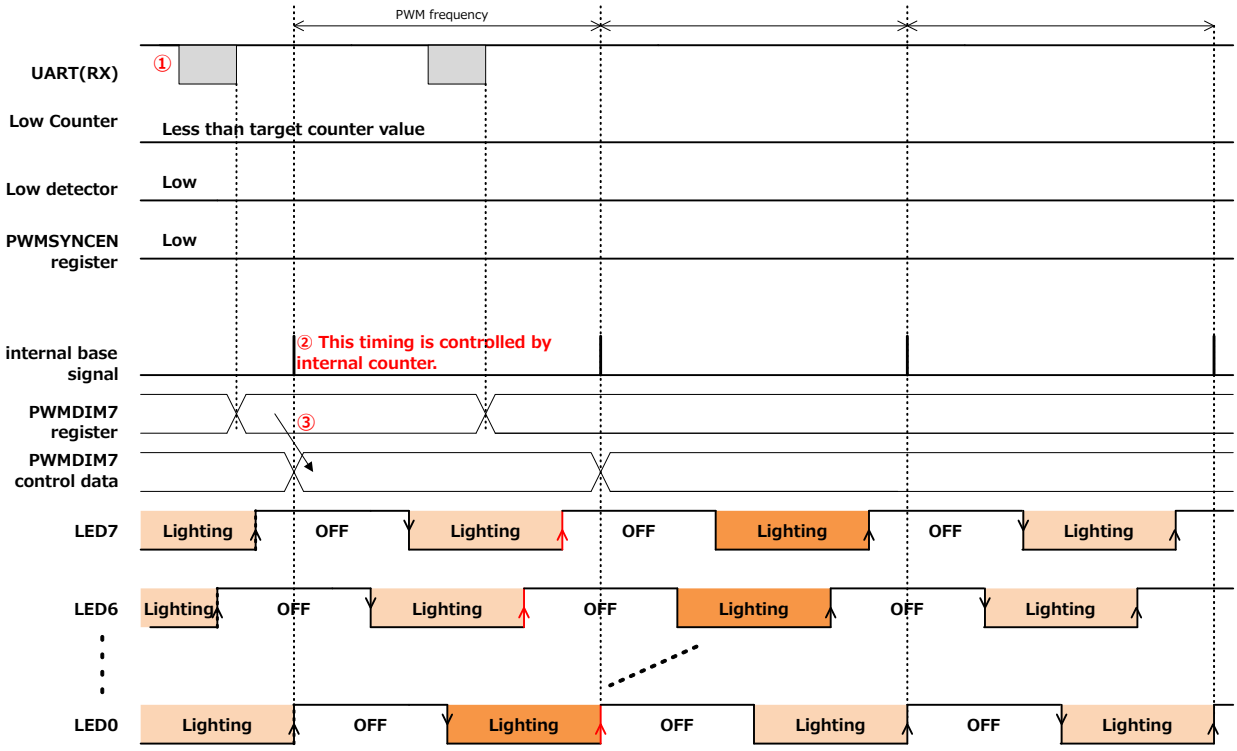


Figure 41. PWM Dimming

1 PWMDIMn register is written.
2 This Timing is controlled by internal counter.
3 PWMDIMn setting is updated from register every timing of internal base signal.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage (VIN)	V_{IN}	-0.3 to +50	V
EN Voltage	V_{EN}	-0.3 to +50	V
VDRV5 Voltage	V_{DRV5}	-0.3 to +7	V
VIN to VDRV5 Voltage	V_{VIN_VDRV5}	-0.3 to +50	V
PCLIM Voltage	V_{PCLIM}	-0.3 to +72	V
PSW to PCLIM Voltage	V_{PSW_PCLIM}	-0.3 to +7	V
BOOT Voltage	V_{BOOT}	-0.3 to V_{PSW_PCLIM} + V_{PCLIM}	V
SNSP, SNSN Voltage	V_{SNSP}, V_{SNSN}	-0.3 to V_{PCLIM}	V
SNSP to SNSN Voltage	V_{SNS}	-0.3 to +0.6	V
PGATE Voltage	V_{PGATE}	-0.3 to V_{PCLIM}	V
PCLIM to PGATE Voltage	V_{PCLIM_PGATE}	-0.3 to +7	V
CHn Voltage	V_{CHn}	-0.3 to V_{PCLIM}	V
CHn to CHn_{-1} Voltage	V_{CHn+1_CHn}	-0.3 to +20	V
MONIAD, RX, TX, CS Voltage	V_{MONIAD}, V_{RX}, V_{TX}, V_{CS}	-0.3 to +7	V
FAULT_B Voltage	V_{FAULT_B}	-0.3 to +7	V
GL, IS, ADIM, RT, COMP Voltage	V_{GL}, V_{IS}, V_{ADIM}, V_{RT}, V_{COMP}	-0.3 to V_{DRV5}	V
Maximum Junction Temperature	Tjmax	+150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSSOP-B30				
Junction to Ambient	θ_{JA}	86.40	31.80	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	13.00	9.00	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD18364EFV-M Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (VIN) *(Note 1)*	V_{IN}	5.5	13.0	45.0	V
Output Voltage (PCLIM)	V_{PCLIM}	-	-	60	V
LED Voltage (V_{CHn+1_CHn})	V_{CHn+1_CHn}	1.5	-	13.5	V
PWM Minimum Pulse Width (V_{SNS_100} 1 LED: 3.0 V Vf Condition)*(Note 2)*	t_{MIN_100}	50	-	-	µs
PWM Minimum Pulse Width (V_{SNS_26} 1 LED : 3.0 V Vf Condition)*(Note 2)*	t_{MIN_26}	100	-	-	µs
Switching Frequency Setting Range	f_{SW}	200	-	550	kHz
CHx Pin Allowable Pulse Current*(Note 3)*	I_{PLSCHx}	2.0	-	-	A
Operating Temperature	Topr	-40	+25	+125	°C

(Note 1) ASO should not be exceeded.
(Note 2) C_{OUT} = 12.5 µF, C_{COMP} = 0.22 µF, R_{COMP} = 470 Ω, R_{SNS} = 0.82 Ω, R_{IS} = 0.051 Ω, PWM frequency 200 Hz , COMPDIS [1:0]: 0,
Time when the LED current reaches 50 % of the setting from the start of PWM dimming lighting. Please refer to page 11 for the measured waveform.
(Note 3) Pulse width time 100 µs, Pulse current cycle 800 ms.

Recommended Setting Parts Range

Parameter	Symbol	Min	Typ	Max	Unit
Capacitor Connecting to the VIN Pin*(Note 4)*	C_{IN}	1.0	2.2	-	µF
Capacitor Connecting to the VDRV5 Pin*(Note 4)*	C_{VDRV5}	1.0	2.2	3.3	µF
Capacitor Connecting to the COMP Pin*(Note 4)*	C_{COMP}	0.10	0.22	0.30	µF
PGATE－PCLIM Capacitor*(Note 4), (Note 5)*	C_{PGATE}	700	1000	1500	pF
BOOT, PSW Capacitor*(Note 4)*	C_{BOOT}, C_{PSW}	0.047	0.1	0.15	µF
DC/DC Output Capacitor*(Note 4)*	C_{OUT}	4.7	-	20	µF
Resistor Connecting to the COMP Pin	R_{COMP}	0	470	750	Ω
Resistor Connecting to the BOOT Pin	R_{BOOT}	38	47	56	Ω
Resistor Connecting to the RT Pin	R_{RT}	15	-	49	kΩ

(Note 4) Set the capacitor taking temperature characteristics, DC bias characteristics, etc. into consideration.
(Note 5) Regarding PMOS (M2), ROHM's: RSQ015P10 and ON semiconductor's: FDC3535 are assumed as basic parts.

Electrical Characteristics (Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Total]						
VIN Circuit Current 1	I_{IN1}	-	5	10	mA	V_{EN} = 0 V
VIN Circuit Current 2	I_{IN2}	-	10	20	mA	V_{EN} = 5 V
VIN UVLO Detect Voltage	V_{INUVD}	4.57	4.80	5.04	V	VIN Falling
VIN UVLO Release Voltage	V_{INUVR}	4.95	5.20	5.46	V	VIN Rising
VIN UVLO Hysteresis Voltage	$V_{INUVHYS}$	-	0.4	-	V	
VDRV5 UVLO Detect Voltage	$V_{DRV5UVD}$	3.94	4.10	4.26	V	V_{DRV5} Falling
VDRV5 UVLO Release Voltage	$V_{DRV5UVR}$	4.22	4.40	4.58	V	V_{DRV5} Rising
VDRV5 UVLO Hysteresis Voltage	$V_{DRV5UVHYS}$	-	0.3	-	V	$V_{DRV5UVR}$ - $V_{DRV5UVD}$
[Reference Voltage]						
VDRV5 Reference Voltage	V_{DRV5}	4.85	5.00	5.15	V	C_{VDRV5} = 2.2 µF I_{VDRV5} = 0 mA to 10 mA
VDRV5 Current Limit	I_{DRV5LM}	45	-	-	mA	
[EN]						
EN Pull Down Current	I_{EN}	0.6	1.2	1.8	µA	V_{EN} = 5 V
EN High Level Threshold Voltage	V_{ENIH}	0.96	1.00	1.04	V	V_{EN} Rising
EN Low Level Threshold Voltage	V_{ENIL}	0.86	0.90	0.94	V	V_{EN} Falling
EN Hysteresis Voltage	V_{ENHYS}	-	0.1	-	V	V_{ENIH} - V_{ENIL}
[OSCILLATOR]						
Switching Frequency	f_{SW}	270	300	330	kHz	R_{RT} = 33 kΩ
RT Output Voltage	V_{RT}	-	0.8	-	V	SSFM Disable
Spread Spectrum Sweep Frequency	f_{SSFM}	220	275	330	Hz	SSFM [2:0] = 3
Spread Spectrum Frequency Sweep Width	f_{SSFMW}	-	±6	-	%	

Electrical Characteristics – continued (Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[N-ch Gate Driver]						
GL ON Resistor High	R_{GLH}	-	1	2.5	Ω	I_{GL} = -10 mA
GL ON Resistor Low	R_{GLL}	-	0.6	1.5	Ω	I_{GL} = 10 mA
Minimum OFF Time	t_{OFFMIN}	-	60	-	ns	R_{RT} = 33 kΩ
[DC/DC Current Detection]						
Over Current Detection Threshold Voltage	V_{ISOCP}	279	300	321	mV	
Leading Edge Blanking Time	t_{ISBLK}	-	120	-	ns	
Slope Compensation Current Ramp Peak	I_{ISSLPP}	-	50	-	μA	
IS to COMP Level Shift Voltage	$V_{ISCMPLS}$	-	1.26	-	V	No Slope Compensation Added
[Error Amplifier]						
Trans Conductance	g_M	-	120	-	μs	V_{SNS} = 256 mV
COMP Sink Current	I_{COMPSI}	65	130	260	μA	V_{SNS} = 512 mV
COMP Source Current	I_{COMPSO}	65	130	260	μA	V_{SNS} = 0 V
ADIM OFF Threshold Voltage	V_{ADIM_0}	150	195	240	mV	ADIM falling
VINDIM Start Voltage	$V_{VINDIM1}$	6.40	6.92	7.48	V	V_{SNS} = 511.8 mV VINDIM = 1
	$V_{VINDIM2}$	6.93	7.49	8.10	V	V_{SNS} = 511.8 mV VINDIM = 2
	$V_{VINDIM3}$	7.41	8.02	8.67	V	V_{SNS} = 511.8 mV VINDIM = 3
	$V_{VINDIM4}$	7.97	8.62	9.32	V	V_{SNS} = 511.8 mV VINDIM = 4
	$V_{VINDIM5}$	8.47	9.17	9.90	V	V_{SNS} = 511.8 mV VINDIM = 5
	$V_{VINDIM6}$	8.95	9.69	10.46	V	V_{SNS} = 511.8 mV VINDIM = 6
	$V_{VINDIM7}$	8.95	9.69	10.46	V	V_{SNS} = 511.8 mV VINDIM = 7
VINDIM Derating Gain	$g_{VINDIM1}$	75	80	85	mV/V	VINDIM = 1
	$g_{VINDIM2}$	70	74	78	mV/V	VINDIM = 2
	$g_{VINDIM3}$	65	69	73	mV/V	VINDIM = 3
	$g_{VINDIM4}$	60	64	68	mV/V	VINDIM = 4
	$g_{VINDIM5}$	57	61	64	mV/V	VINDIM = 5
	$g_{VINDIM6}$	54	57	60	mV/V	VINDIM = 6
	$g_{VINDIM7}$	54	57	60	mV/V	VINDIM = 7

Electrical Characteristics – continued (Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Current Sense Amplifier]						
Current Sense Voltage	V_{SNS_100}	496.4	511.8	527.1	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V, DCDIM [9:0] = 1023
	V_{SNS_50}	248.5	256.2	263.9	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 552 (default)
	V_{SNS_35}	173.8	179.2	184.6	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 410
	V_{SNS_26}	128.4	133.1	137.7	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 325
	V_{SNS_21}	103.2	107.6	111.9	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 278
	V_{SNS_05}	21.7	25.6	29.5	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 127
SNSN Voltage Dependence Characteristics of Current Sense Voltage	ΔV_{SNS_LINE}	-0.5	-	+0.5	%	V_{SNSN} = 6 V to 40 V DCDIM [9:0] = 552 (default)
Current Sense Threshold Resolution	ΔV_{SNS_LSB}	-	2.5/4.5 /1024	-	mV	
Current Sense Threshold Differential Non-linearity	ΔV_{SNS_DNL}	-3	-	+3	LSB	
Current Sense Input Voltage Range	V_{SNSND}	4.0	-	-	V	V_{SNSN} Rising
SNSP Input Current	I_{SNSP}	49	95	140	µA	V_{SNSP_SNSN} = 511.8 mV V_{SNSN} = 60 V
SNSN Input Current	I_{SNSN}	18	31	43	µA	V_{SNSP_SNSN} = 511.8 mV V_{SNSN} = 60 V
LED Over Current Limit Voltage	ΔV_{SNS_LIM7}	241.8	295.2	348.6	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 552 (default) OCLIM [2:0] = 7
	ΔV_{SNS_LIM3}	116.2	156.3	196.3	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 552 (default) OCLIM [2:0] = 3
	ΔV_{SNS_LIM0}	25.3	52.0	78.7	mV	V_{SNSP} - V_{SNSN}, V_{SNSN} = 40 V DCDIM [9:0] = 552 (default) OCLIM [2:0] = 0 (default)
Low Voltage between PCLIM – PGATE Pin	$V_{PCLIM-PGATE}$	4.7	5.1	5.5	V	
SGB Detect Voltage	V_{SGBDET}	3.0	11.1	20.7	mV	V_{SNS} Falling
SGB Release Voltage	V_{SGBREL}	4.0	13.6	21.7	mV	V_{SNS} Rising
[Over Voltage Protection]						
Over Voltage Protection Voltage	V_{OVP_15}	65.0	67.5	70.0	V	V_{SNSP} Rising OVPSET [3:0] = 15
	V_{OVP_10}	54.1	56.6	59.1	V	V_{SNSP} Rising OVPSET [3:0] = 10 (default)
	V_{OVP_5}	43.2	45.7	48.2	V	V_{SNSP} Rising OVPSET [3:0] = 5
	V_{OVP_0}	32.3	34.8	37.3	V	V_{SNSP} Rising OVPSET [3:0] = 0
Over Voltage Protection Hysteresis Voltage	V_{OVPHYS}	-	1.8	-	V	V_{SNSP} Falling
Over Voltage Register Recovery Time	t_{OVP}	17	20	23	ms	

Electrical Characteristics – continued (Unless otherwise specified VIN = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[CH0 to CH8 Short Circuit Protection]						
CH0, CH2, CH4, CH6, CH8 Short Circuit Protection Voltage	V_{CH8SCP}	1.6	2.0	2.4	V	V_{CH0}, V_{CH2}, V_{CH4}, V_{CH6}, V_{CH8} Falling Monitor
CH1, CH3, CH5, CH7 Short Circuit Protection Voltage	V_{CH7SCP}	0.7	1.4	2.1	V	V_{CH1}, V_{CH3}, V_{CH5}, V_{CH7} Falling Monitor
CHx Short Circuit Protection Hysteresis Voltage	V_{SCP_HYS}	-	0.2	-	V	V_{CH0} to V_{CH8} Rising
CHxSCP Detect Time	t_{SCP}	30	50	70	µs	
CHxSCP Recovery Time	t_{SCPREC}	17	20	23	ms	
[By-pass Switch]						
By-pass Switch ON Resistor 1	R_{CH}	-	0.30	0.75	Ω	Between CHn+1, CHn I_{SW} = 300 mA
By-pass Switch ON Resistor 2	R_{CH80}	-	1.70	4.25	Ω	Between CH8, CH0 I_{SW} = 300 mA
LED Short Detection Voltage	V_{CHLS}	0.7	1.0	1.5	V	V_{CHn+1_CHn} Falling
LED Open Detection Voltage 1	V_{CHLO1}	4.5	6.0	7.0	V	V_{CHn+1_CHn} Rising (LEDOPSETn = 0)
LED Open Detection Voltage 2	V_{CHLO2}	13.5	15.0	16.5	V	V_{CHn+1_CHn} Rising (LEDOPSETn = 1)
LED Short Time	t_{LS}	80	100	120	µs	
PWM Dimming Frequency	f_{PWM}	170	200	230	Hz	FPWM [3:0] = 0
[A/D Convertor]						
A/D Resolution	RES_{ADC}	-	8	-	bit	MONIAD Input
A/D Conversion time	t_{ADC}	-	-	150	µs	
A/D Full Scale Reference Voltage	V_{FSRADC}	-	V_{DRV5}	-	V	MONIAD Input
Integral Non-linearity	INL	-2	-	+2	LSB	
Differential Non-linearity	DNL	-2	-	+2	LSB	
[Interface]						
FAULT_B Output Voltage Low	V_{FAULT_BOL}	-	0.1	0.4	V	I_{FAULT_B} = 5 mA
FAULT_B Leak Current	I_{FAULT_B}	-	0	1	µA	V_{FAULT_B} = 5.5 V
RX Input High Voltage	V_{RX_IH}	2.2	-	-	V	
RX Input Low Voltage	V_{RX_IL}	-	-	0.8	V	
RX Input Current	I_{RX_IN}	-	0	1	µA	V_{RX} = 5 V
RX Output Current	I_{RX_OUT}	-1	0	-	µA	V_{RX} = 0 V
TX Output Voltage High	V_{TX_OH}	V_{DRV5}-0.4	-	V_{DRV5}	V	I_{TX} = -1 mA
TX Output Voltage High	V_{TX_OL}	-	-	0.4	V	I_{TX} = 1 mA

Typical Performance Curves
(Unless otherwise specified VIN = 13 V, Tj = +25 °C)

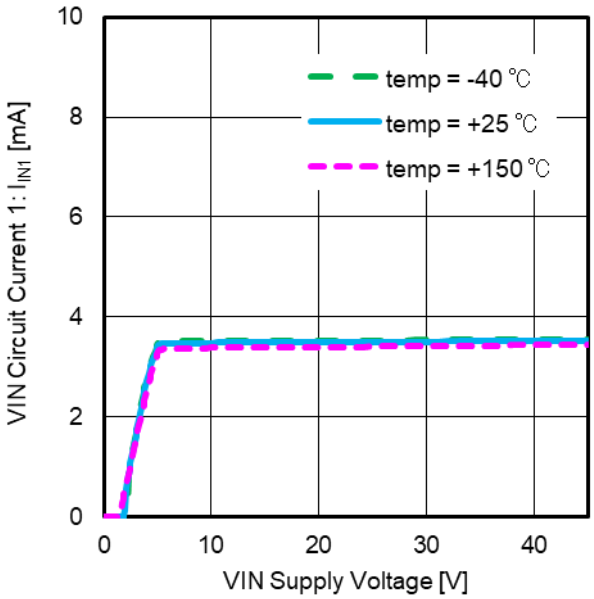


Figure 42. VIN Circuit Current 1 vs VIN Supply Voltage (EN = 0 V)

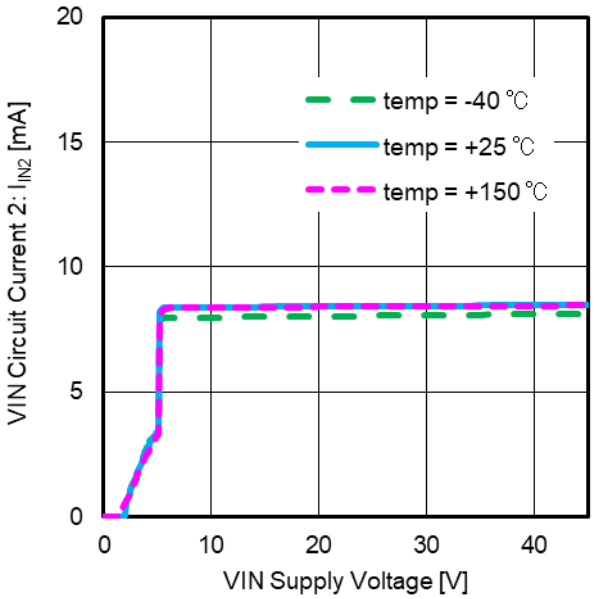


Figure 43. VIN Circuit Current 2 vs VIN Supply Voltage (EN = 5 V)

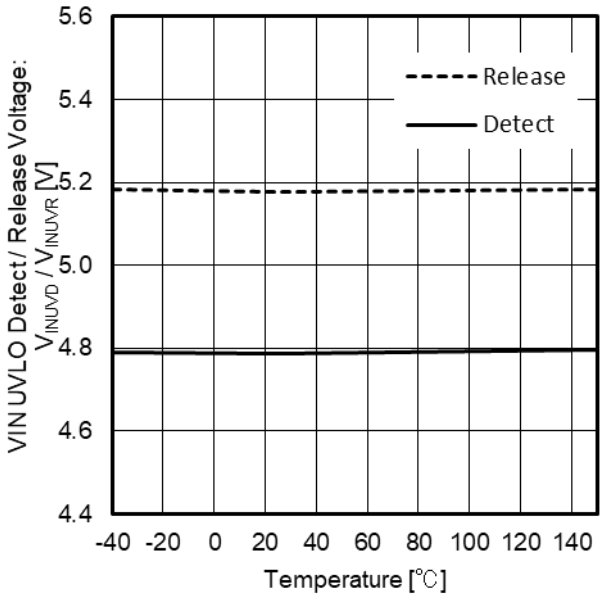


Figure 44. VIN UVLO Detect/Release Voltage vs Temperature

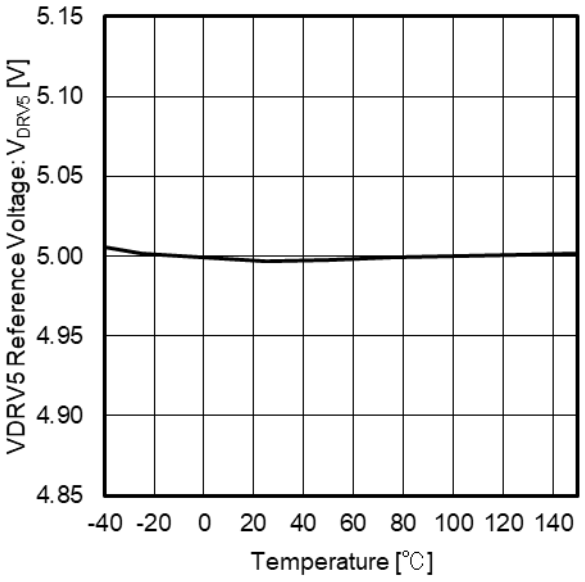


Figure 45. VDR5 Reference Voltage vs Temperature

Typical Performance Curves – continued
(Unless otherwise specified VIN = 13 V, Tj = +25 °C)

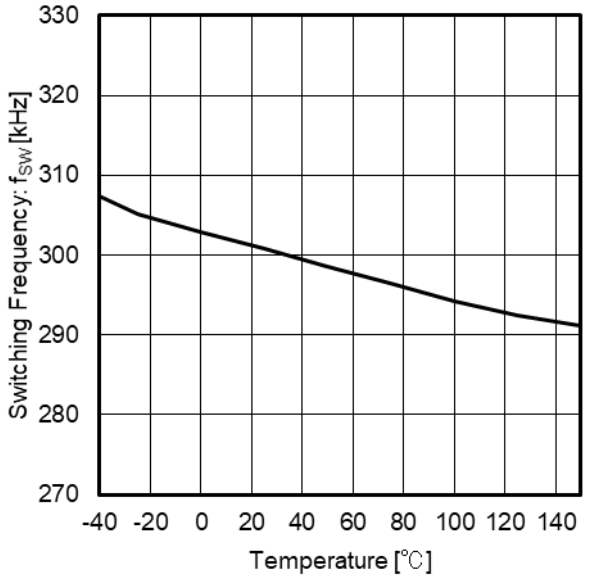


Figure 46. Switching Frequency vs Temperature
(R_{RT} = 33 kΩ)

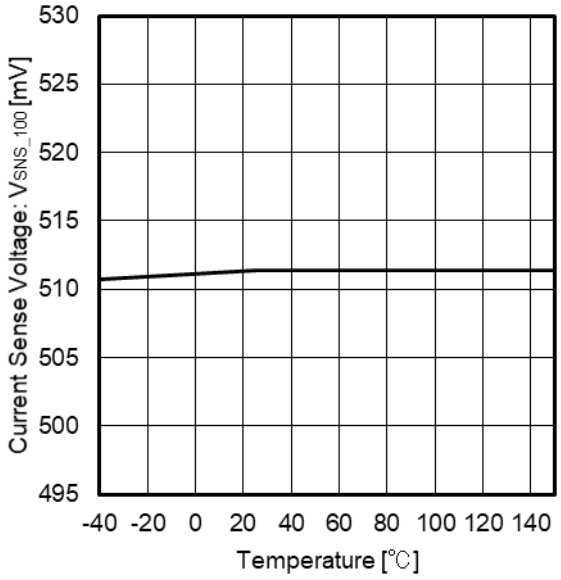


Figure 47. Current Sense Voltage V_{SNS_100} vs Temperature
(DCDIM [9:0] = 1023)

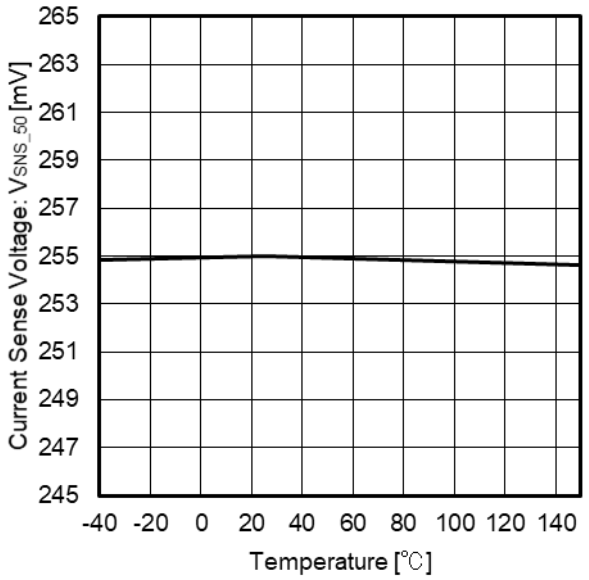


Figure 48. Current Sense Voltage V_{SNS_50} vs Temperature
(DCDIM [9:0] = 552)

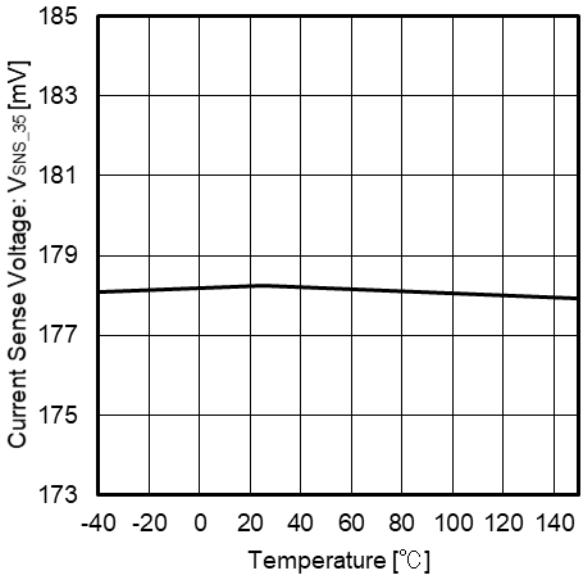


Figure 49. Current Sense Voltage V_{SNS_35} vs Temperature
(DCDIM [9:0] = 410)

Typical Performance Curves – continued
(Unless otherwise specified VIN = 13 V, Tj = +25 °C)

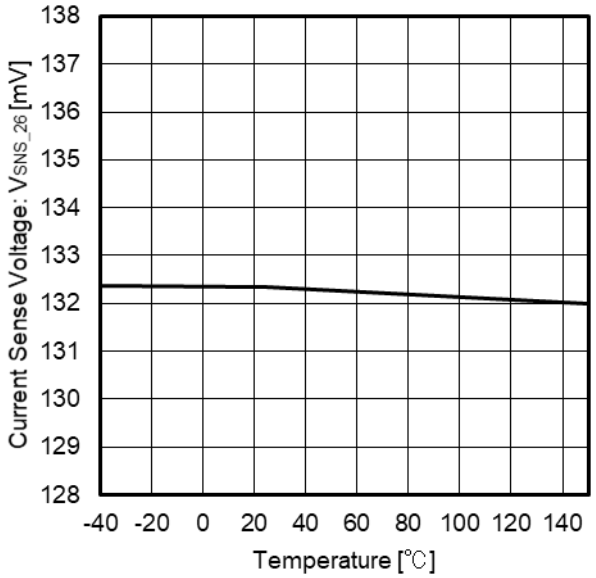


Figure 50. Current Sense Voltage V_{SNS_26} vs Temperature
(DCDIM [9:0] = 325)

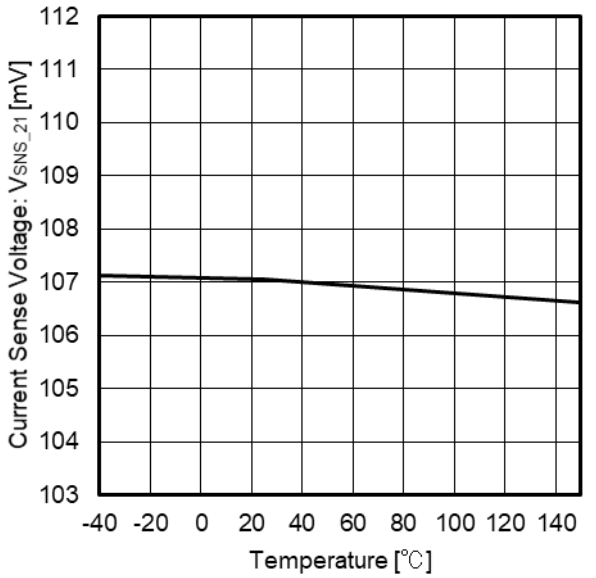


Figure 51. Current Sense Voltage V_{SNS_21} vs Temperature
(DCDIM [9:0] = 278)

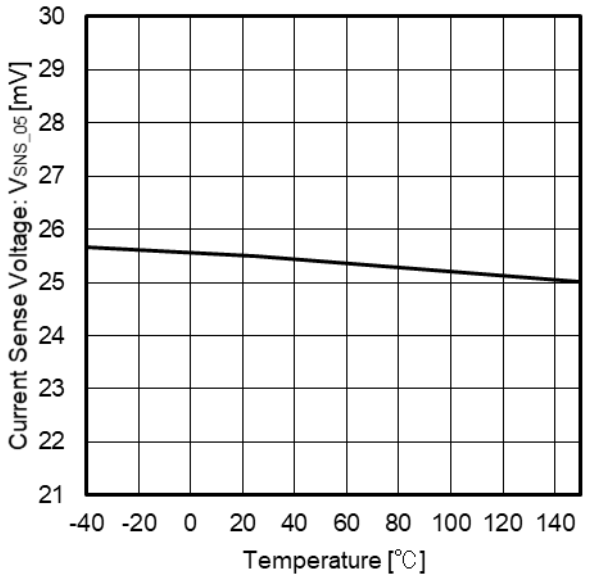


Figure 52. Current Sense Voltage V_{SNS_05} vs Temperature
(DCDIM [9:0] = 127)

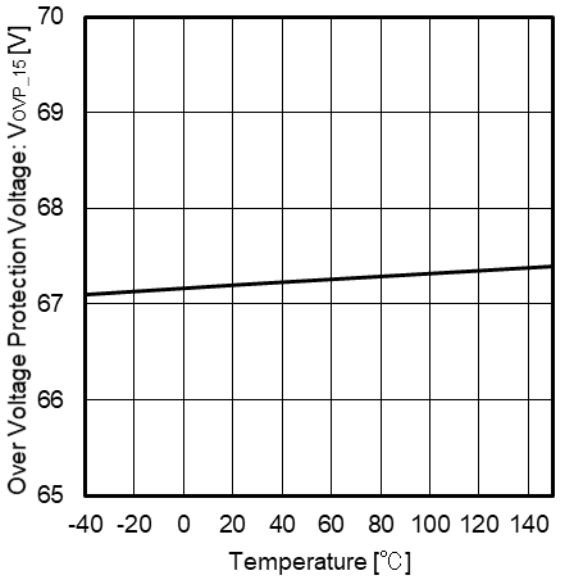


Figure 53. Over Voltage Protection Voltage V_{OVP_15} vs Temperature
(OVPSET [3:0] = 15)

Typical Performance Curves – continued
(Unless otherwise specified VIN = 13 V, Tj = +25 °C)

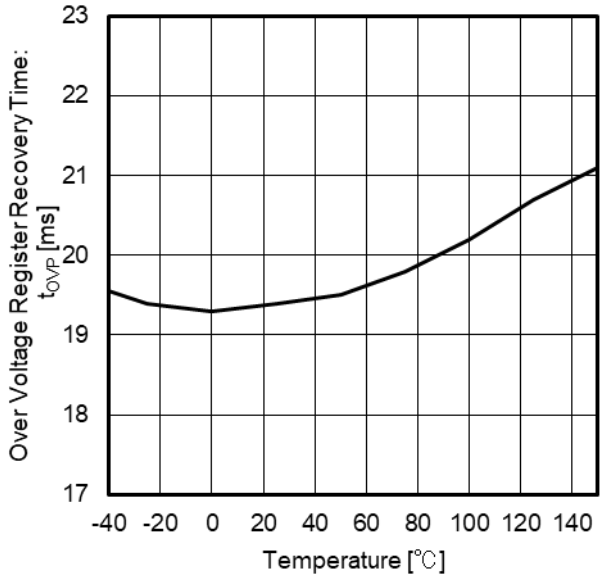


Figure 54. Over Voltage Resister Recovery Time vs Temperature

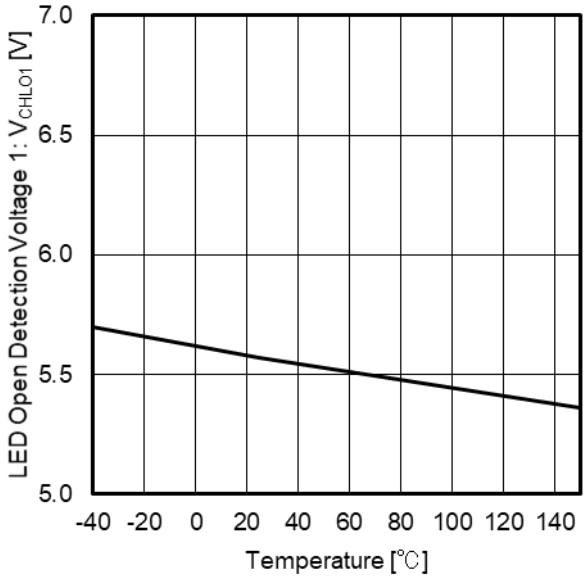


Figure 55. LED Open Detection Voltage 1 vs Temperature (LEDOPSETn = 0)

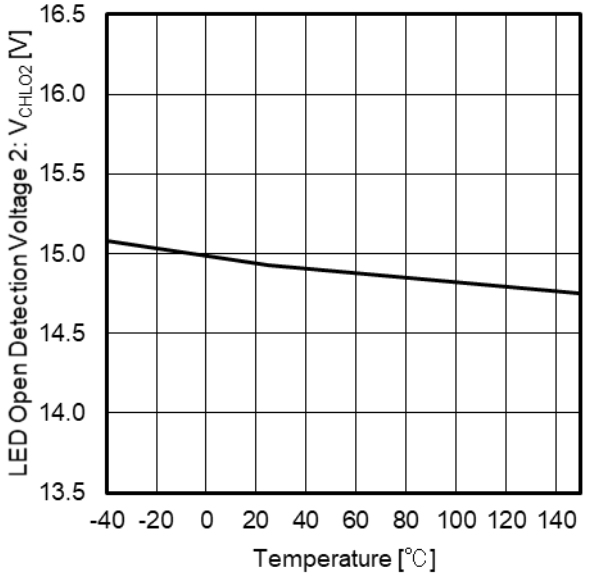


Figure 56. LED Open Detection Voltage 2 vs Temperature (LEDOPSETn = 1)

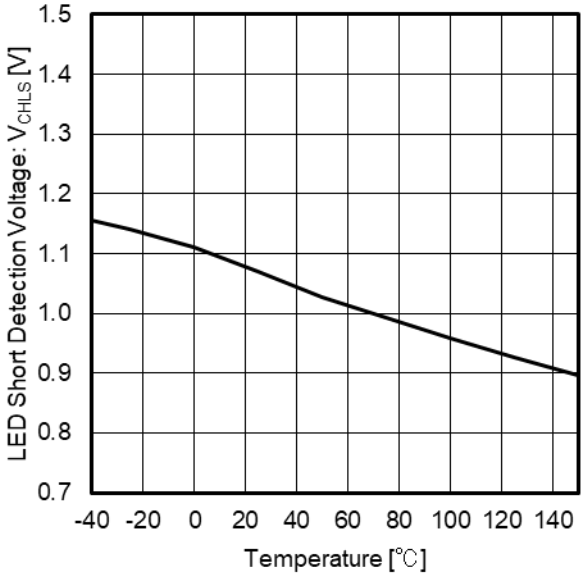


Figure 57. LED Short Detection Voltage vs Temperature

Typical Performance Curves – continued
(Unless otherwise specified VIN = 13 V, Tj = +25 °C)

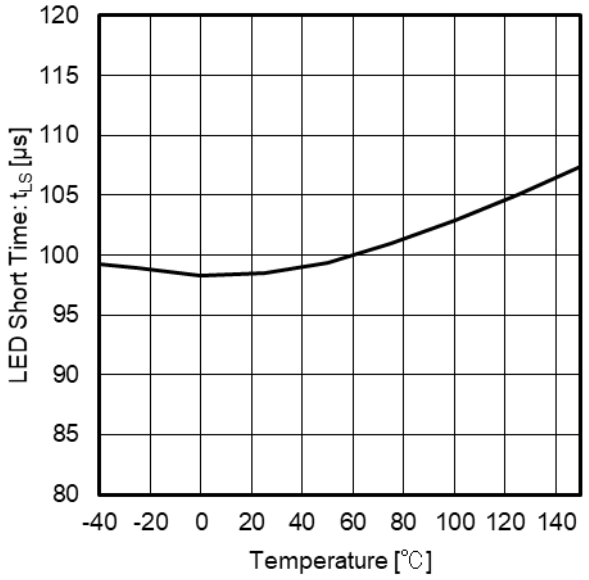


Figure 58. LED Short Time vs Temperature

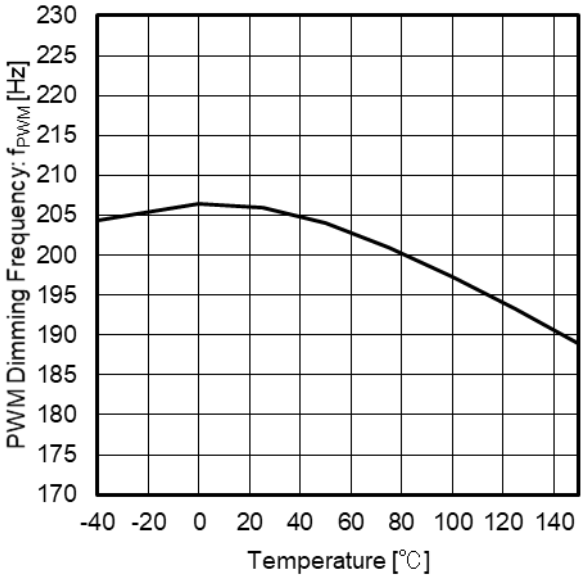


Figure 59. PWM Dimming Frequency vs Temperature (FPWM [3:0] = 0)

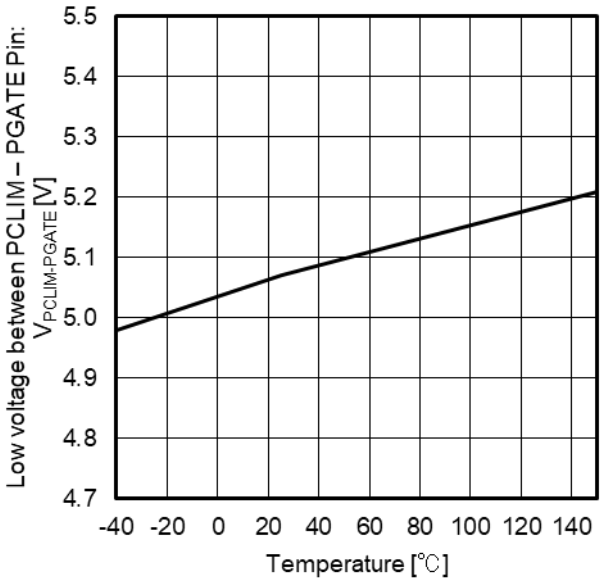


Figure 60. Low voltage between PCLIM – PGATE Pin vs Temperature

Application Examples

(VIN = 13 V, ILED = 316 mA at DCDIM [9:0] = 552, 8 LED)

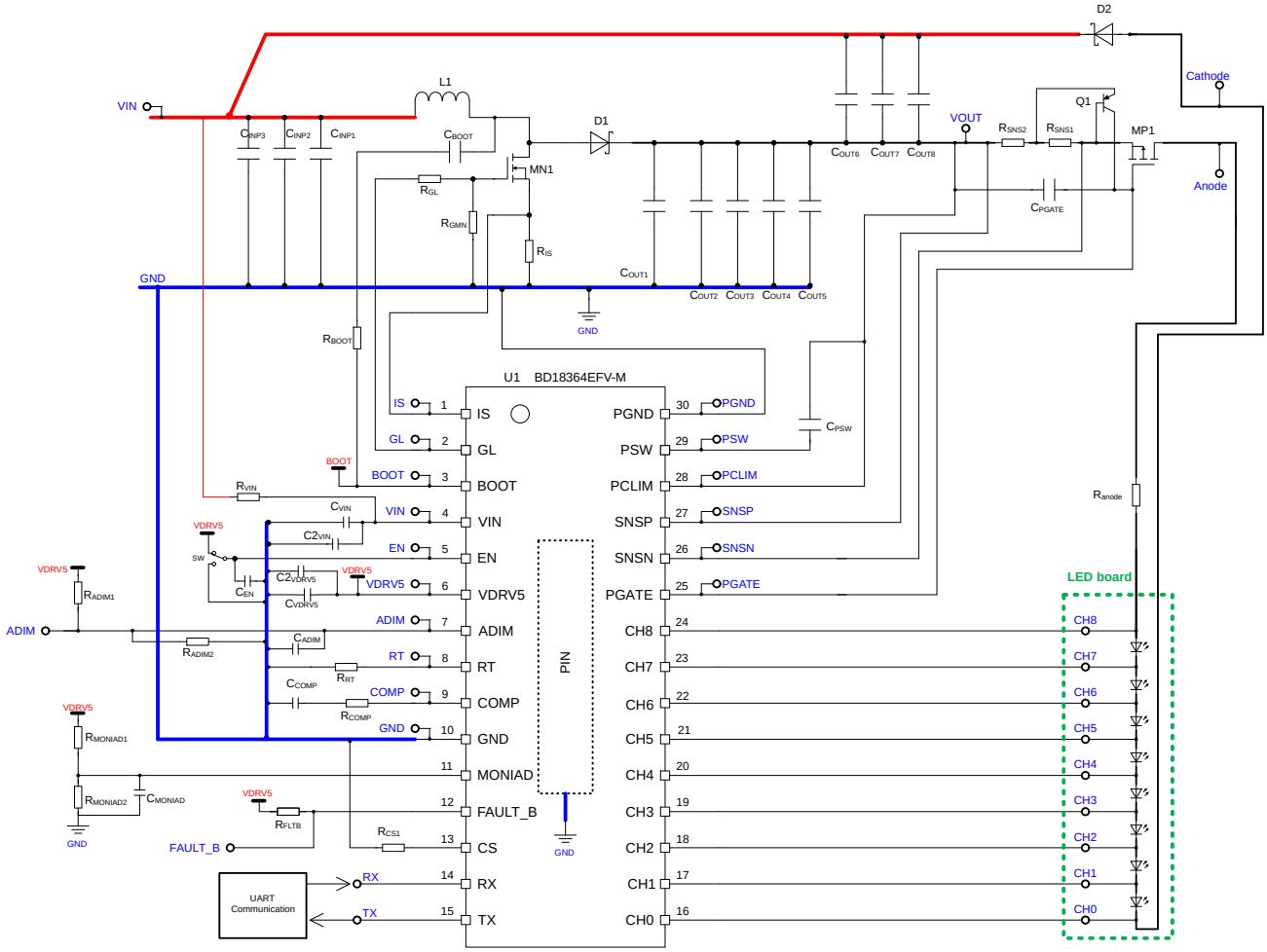
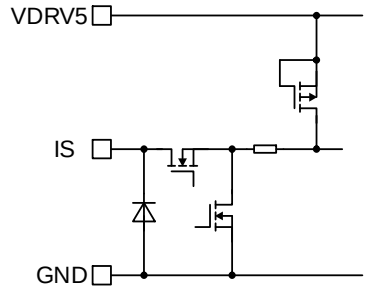
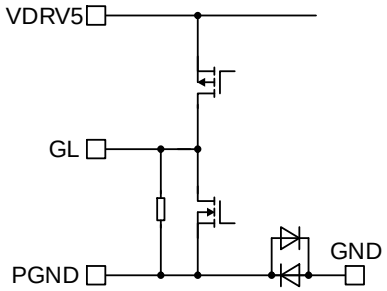
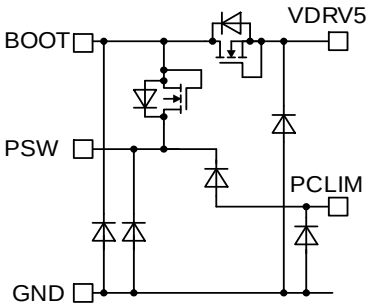
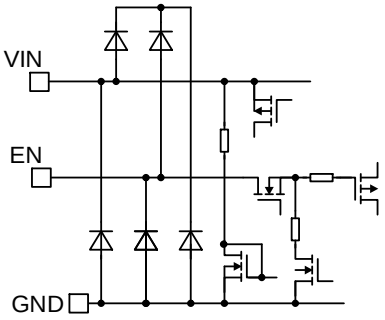
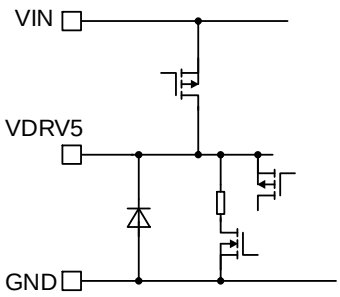
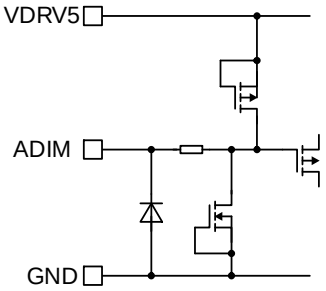
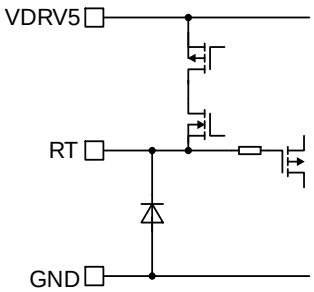
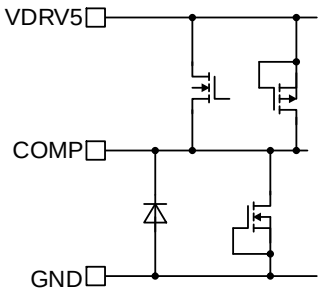


Figure 61. Application Circuit

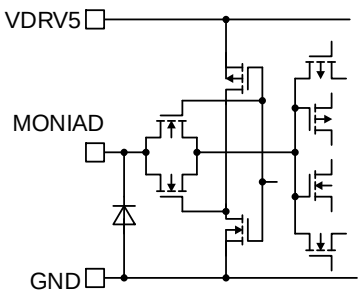
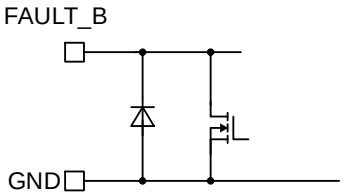
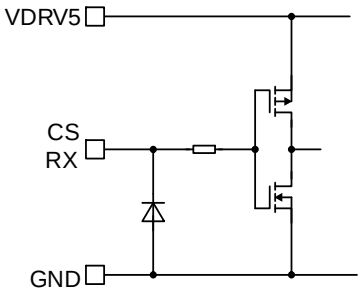
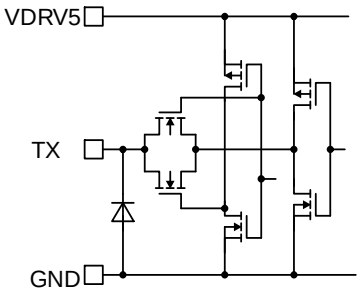
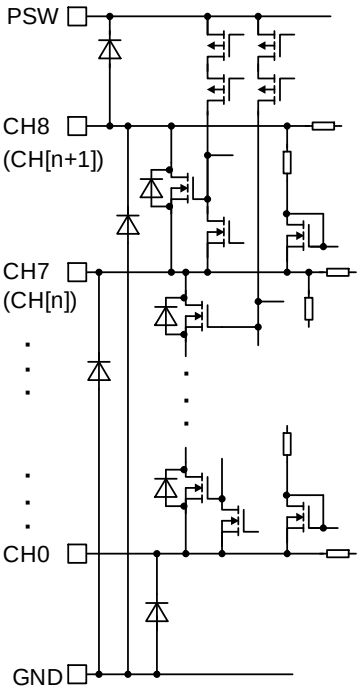
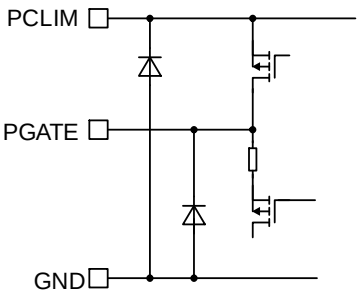
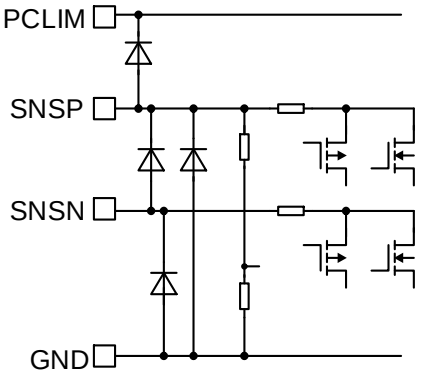
Application Parts Choice Example

Parts	Component Name	Value	Product Name	Manufacture
Capacitor	C_{INP1}	4.7 µF	GCM32ER71H475KA55#_X7R_±10 %	Murata
	C_{INP2}	4.7 µF	GCM32ER71H475KA55#_X7R_±10 %	Murata
	C_{INP3}	Open	-	-
	C_{VIN}	0.1 µF	GCM188L81H104KA57#_-_±10 %	Murata
	$C2_{VIN}$	1000 pF	GCM1882C1H102JA01#_CH_±5 %	Murata
	C_{VDRV5}	2.2 µF	GCM21BR71E225KA73#_X7R_±10 %	Murata
	$C2_{VDRV5}$	1000 pF	GCM1882C1H102JA01#_CH_±5 %	Murata
	C_{EN}	1000 pF	GCM188R92A102KA37#_X8R_±10 %	Murata
	C_{ADIM}	0.01 µF	GCM188L81H103KA03#_-_±10 %	Murata
	C_{COMP}	0.22 µF	GCG188R91H224KA01#_X8R_±10 %	Murata
	C_{MONIAD}	0.01 µF	GCM188L81H103KA03#_-_±10 %	Murata
	C_{BOOT}	0.1 µF	GCJ188R72A104KA01#_X7R_±10 %	Murata
	C_{PSW}	0.1 µF	GCJ188R72A104KA01#_X7R_±10 %	Murata
	C_{PGATE}	1000 pF	GCM188R92A102KA37#_X8R_±10 %	Murata
	C_{OUT1}	0.1 µF	GCJ188R72A104KA01#_X7R_±10 %	Murata
	C_{OUT2}	4.7 µF	GCM32DC72A475KE02#_X7S_±10 %	Murata
	C_{OUT3}	Open	-	-
	C_{OUT4}	Open	-	-
	C_{OUT5}	Open	-	-
	C_{OUT6}	4.7 µF	GCM32DC72A475KE02#_X7S_±10 %	Murata
	C_{OUT7}	4.7 µF	GCM32DC72A475KE02#_X7S_±10 %	Murata
	C_{OUT8}	Open	-	-
Resistor	R_{IS}	0.051 Ω	LTR18	ROHM
	R_{GL}	10 Ω	MCR03	ROHM
	R_{GMN}	Open	-	-
	R_{BOOT}	47 Ω	MCR03	ROHM
	R_{VIN}	10 Ω	MCR03	ROHM
	R_{ADIM1}	100 kΩ	MCR03	ROHM
	R_{ADIM2}	Open	-	-
	R_{RT}	33 kΩ	MCR03	ROHM
	R_{COMP}	470	MCR03	ROHM
	$R_{MONIAD1}$	100 kΩ	MCR03	ROHM
	$R_{MONIAD2}$	100 kΩ	MCR03	ROHM
	R_{FLTB}	10 kΩ	MCR03	ROHM
	R_{CS1}	100 kΩ	MCR03	ROHM
	R_{SNS1}	0.51 Ω	LTR18	ROHM
	R_{SNS2}	0.30 Ω	LTR18	ROHM
	R_{anode}	Short	-	-
Coil	L1	10 µH	MSS1278-103MLB	Coilcraft
Tr	MN1		IRLR3110ZTRPBF	Infineon
	MP1		FDC3535	ON Semiconductor
	Q1		SST2907AHZG	ROHM
Diode	D1		RB098BM100FH	ROHM
	D2		RB098BM100FH	ROHM
IC	U1		BD18364EFV-M	ROHM

I/O Equivalence Circuits

Pin No	Pin Name	I/O Equivalence Circuits	Pin No	Pin Name	I/O Equivalence Circuits
1	IS		2 30	GL PGND	
3 29	BOOT PSW		4 5	VIN EN	
6	VDRV5		7	ADIM	
8	RT		9	COMP	

I/O Equivalence Circuits - continued

Pin No	Pin Name	I/O Equivalence Circuits	Pin No	Pin Name	I/O Equivalence Circuits
11	MONIAD		12	FAULT_B	
13 14	CS RX		15	TX	
16 17 18 19 20 21 22 23 24	CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8		25 28	PGATE PCLIM	
			26 27	SNSN SNSP	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

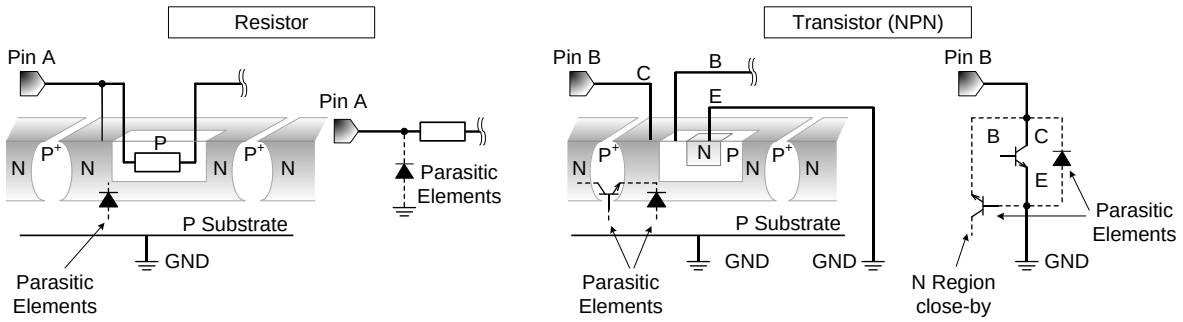


Figure 62. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"

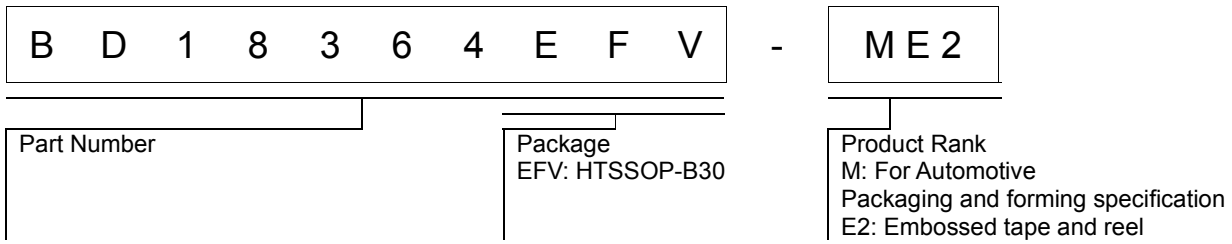
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"

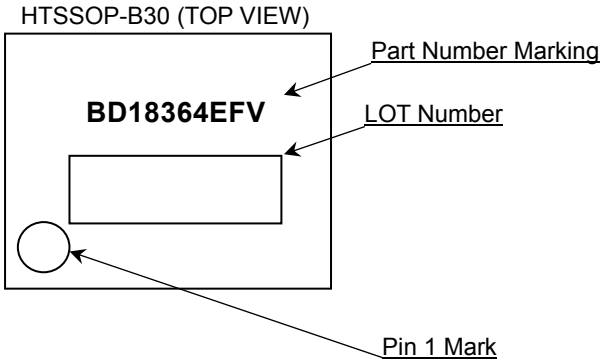
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

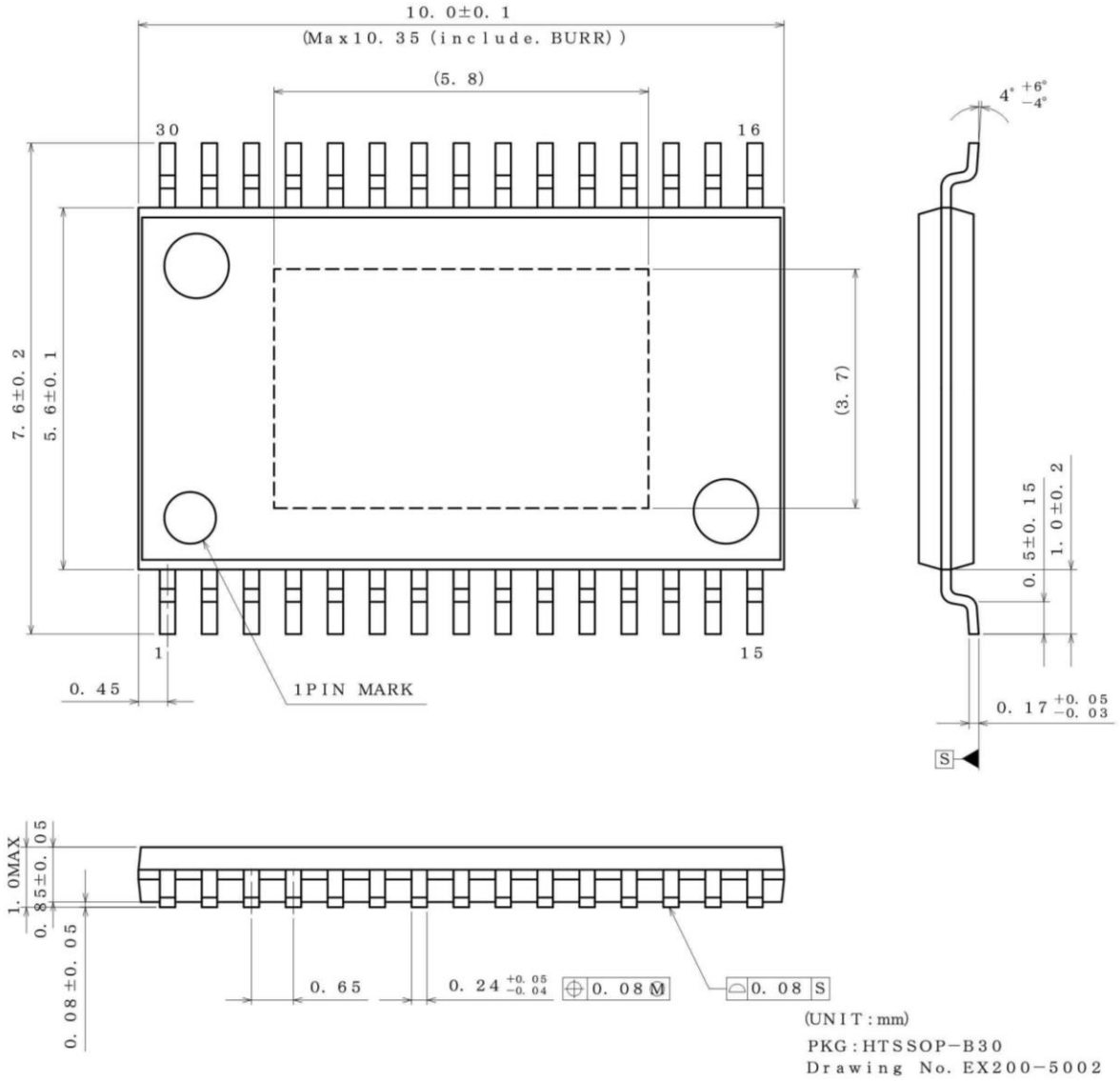


Marking Diagram



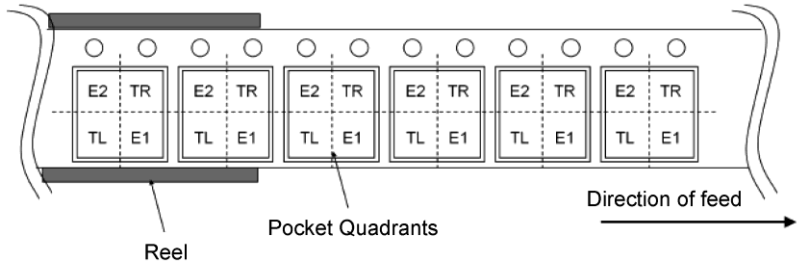
Physical Dimension and Packing Information

Package Name	HTSSOP-B30



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
23.May.2022	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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