Boost LED Driver

1ch High Current LED Controller for Automotive

BD18353EFV-M BD18353MUF-M

General Description

BD18353EFV-M/MUF-M is a 1ch LED Controller. High side current detection amplifier is built-in. PWM dimming duty can be freely set with built-in PWM generation circuit. PWM dimming realizes by driving an external P-ch MOSFET. Outputs abnormal LED status to the FAULT_B pin. Two systems of analog dimming are built-in. High precision 3.0 V output power supply for analog dimming and PWM dimming setting is built-in.

Key Specifications

- Input Voltage Range: 5 V to 65 V
- Maximum Output Voltage: 65 V
- LED Current Sense Voltage Accuracy: ±3 %
- Setting Frequency Switching Range: 200 kHz to 2.5 MHz
- Operating Ambient Temperature: -40 °C to +125 °C

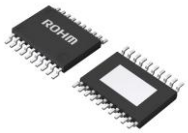
Features

- AEC-Q100 Qualified*(Note 1)*
- Rail-to-Rail Current Sense Amplifier
- PWM Dimming Signal Generator
- Over Voltage Protection (OVP)
- Short Circuit Protection (SCP)
- Analog Dimming (two systems)
- DRL Mode (100 % Duty) Enable
- Outputs Abnormal LED Status (FAULT_B)
- Spread Spectrum Frequency Modulation ON/OFF (SSFM_B)

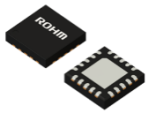
(Note 1) Grade1

Packages

	W (Typ) x D (Typ) x H (Max)
HTSSOP-B20	6.5 mm x 6.4 mm x 1.0 mm
VQFN20FV3535	3.5 mm x 3.5 mm x 1.0 mm



HTSSOP-B20

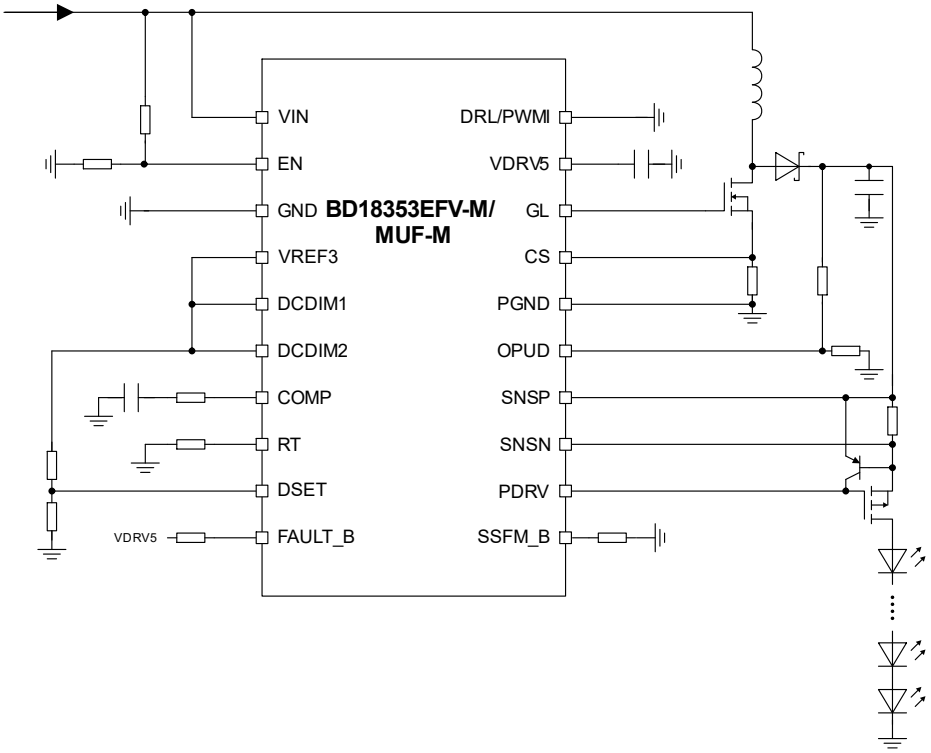


VQFN20FV3535

Applications

- Automotive Exterior Lamps
  Rear, Turn, DRL/Position, Fog, High/Low Beam etc.

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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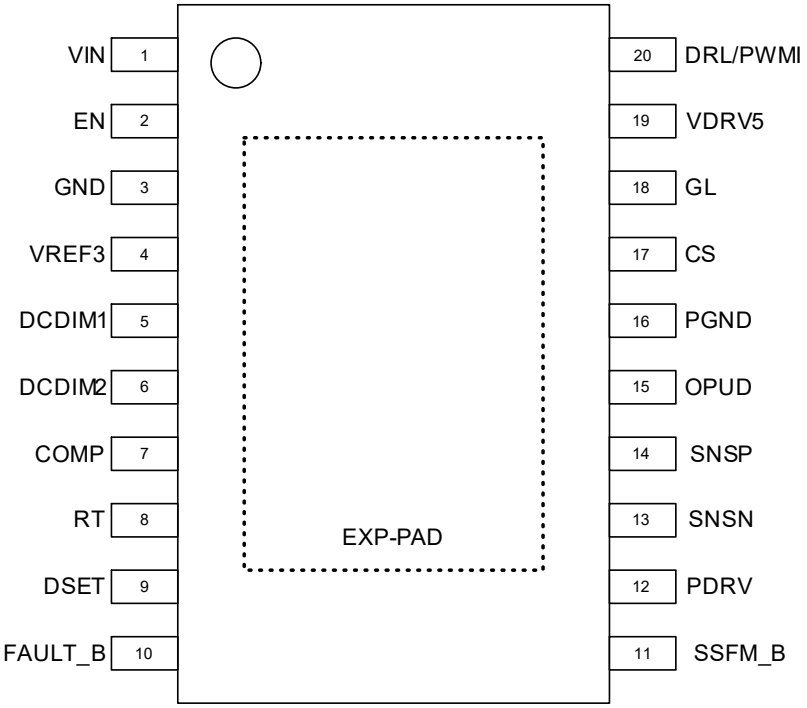
Pin Configuration (HTSSOP-B20)

HTSSOP-B20
(TOP VIEW)



Pin Description (HTSSOP-B20)

Pin No.	Pin Name	Function
1	VIN	Power supply input
2	EN	Enable input
3	GND	GND
4	VREF3	Reference voltage for analog dimming and PWM dimming duty setting
5	DCDIM1	Analog dimming input
6	DCDIM2	Analog dimming input
7	COMP	Connect capacitor to set feedback compensation
8	RT	Connect resistor to set switching frequency
9	DSET	PWM dimming duty setting voltage input (connect to resistor divider from VREF3 to GND)
10	FAULT_B	Open drain output for fault state flag
11	SSFM_B	Spread spectrum frequency modulation enable input (SSFM enable @SSFM_B = Low)
12	PDRV	P-ch MOSFET gate drive for PWM dimming and LED protection
13	SNSN	Current sense input (-)
14	SNSP	Current sense input (+)
15	OPUD	Output voltage monitor for over voltage protection and under voltage detection (connect to resistor divider from output voltage to GND)
16	PGND	Power GND
17	CS	Inductor current sense input
18	GL	Output for N-ch MOSFET gate drive
19	VDRV5	Bypass with capacitor to provide 5 V bias supply for gate drive
20	DRL/PWMI	DRL mode (100 % duty) enable input / External PWM dimming signal input
-	EXP-PAD	Heat radiation pad. The EXP-PAD is connected to GND.

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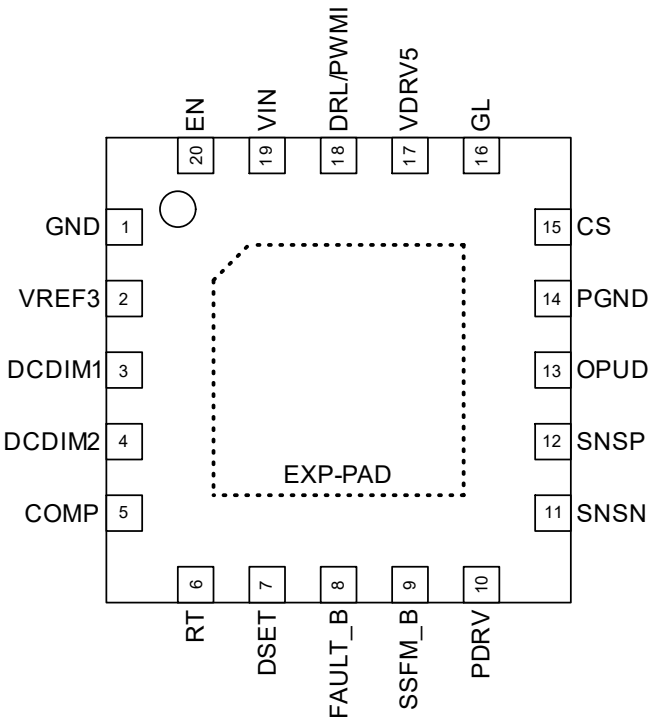
Pin Configuration (VQFN20FV3535)

VQFN20FV3535
(TOP VIEW)



Pin Description (VQFN20FV3535)

Pin No.	Pin Name	Function
1	GND	GND
2	VREF3	Reference voltage for analog dimming and PWM dimming duty setting
3	DCDIM1	Analog dimming input
4	DCDIM2	Analog dimming input
5	COMP	Connect capacitor to set feedback compensation
6	RT	Connect resistor to set switching frequency
7	DSET	PWM dimming duty setting voltage input (connect to resistor divider from VREF3 to GND)
8	FAULT_B	Open drain output for fault state flag
9	SSFM_B	Spread spectrum frequency modulation enable input (SSFM enable @SSFM_B = Low)
10	PDRV	P-ch MOSFET gate drive for PWM dimming and protection
11	SNSN	Current sense input (-)
12	SNSP	Current sense input (+)
13	OPUD	Output voltage monitor for over voltage protection and under voltage detection (connect to resistor divider from output voltage to GND)
14	PGND	Power GND
15	CS	Inductor current sense input
16	GL	Output for N-ch MOSFET gate drive
17	VDRV5	Bypass with capacitor to provide 5 V bias supply for gate drive
18	DRL/PWMI	DRL mode (100 % duty) enable input / External PWM dimming signal input
19	VIN	Power supply input
20	EN	Enable input
-	EXP-PAD	Heat radiation pad. The EXP-PAD is connected to GND.

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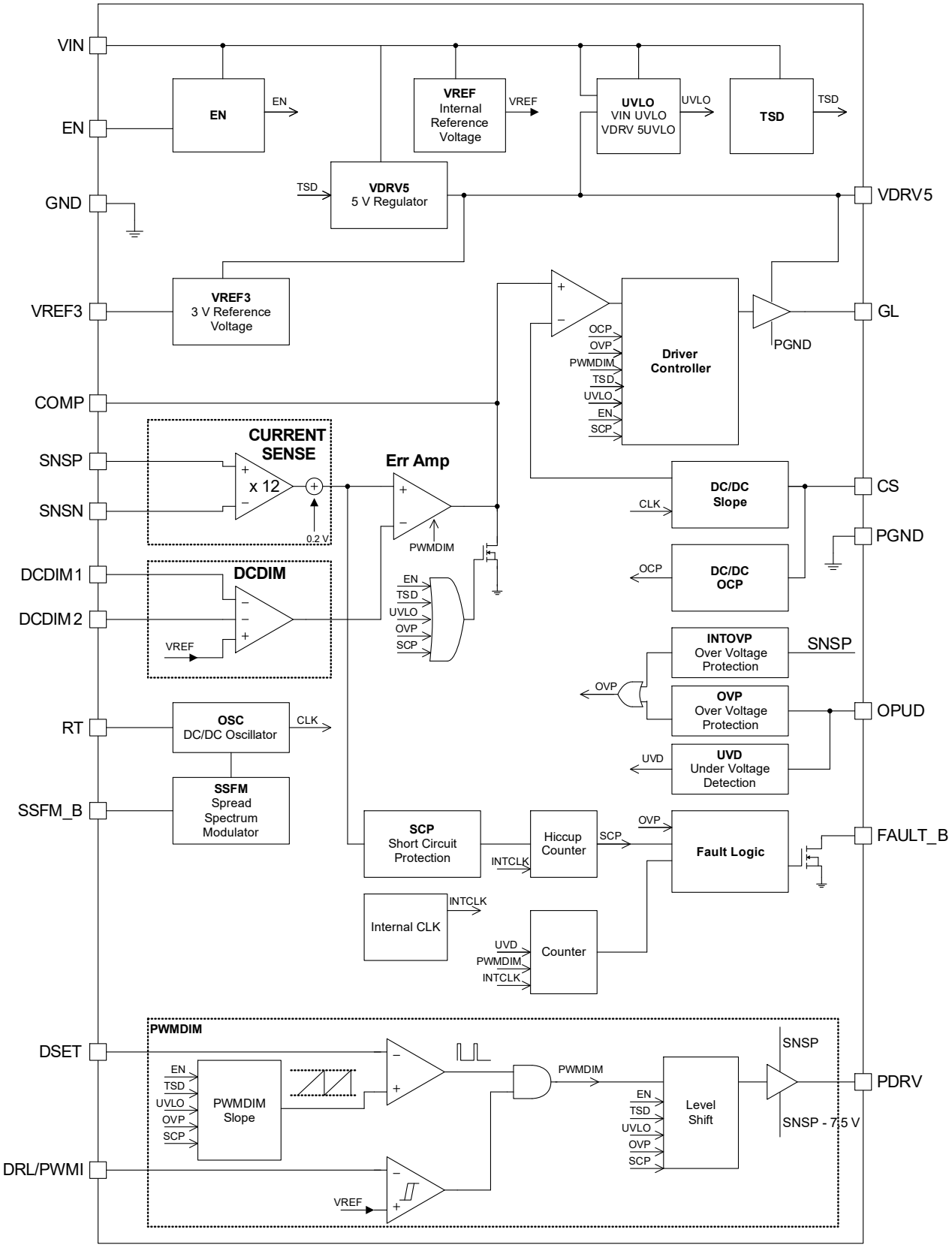
Block Diagram



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Description of Blocks

1 Power Supply for N-ch MOSFET Gate Driver and Internal Circuit (VDRV5)

The VDRV5 voltage 5.0 V (Typ) is generated from the VIN pin voltage. This voltage is used as the internal power supply of the IC and the power supply for driving the DC/DC N-ch MOSFET. It also supplies current to the FAULT_B pin pull up resistor.

The total current supplied to the DC/DC N-ch MOSFET and the resistor must be I_{DRV5LM} (VDRV5 Output Current Limit) or less.

The current supplied to the DC/DC N-ch MOSFET (I_{MOSFET}) can be calculated by the following formula.

$$I_{MOSFET} = Q_G \times f_{SW}$$

Where:

Q_G is the gate charge of the MOSFET.

f_{SW} is the switching frequency.

Connect C_{VDRV5} = 2.2 µF as feedback compensation capacitor to the VDRV5 pin. Place ceramic capacitor close to the IC to minimize trace length to the VDRV5 pin and also to the IC ground.

Do not use the VDRV5 as a power supply other than this IC.

2 High Accuracy Reference Voltage (VREF3)

The VREF3 voltage 3.0 V (Typ) is generated from the VDRV5 pin voltage. VREF3 is used as a reference voltage for PWM dimming duty and analog dimming setting. Input the voltage set by resistor dividing from the VREF3 pin to the DSET pin, the DCDIM1 pin, and the DCDIM2 pin.

Do not connect a capacitor to the VREF3 pin.

Do not use the VREF3 as a power supply other than this IC.

3 LED Current Setting (CURRENT SENSE)

LED current (I_{LED}) can be set by resistor R_{SNS} connected between the SNSP pin and the SNSN pin.

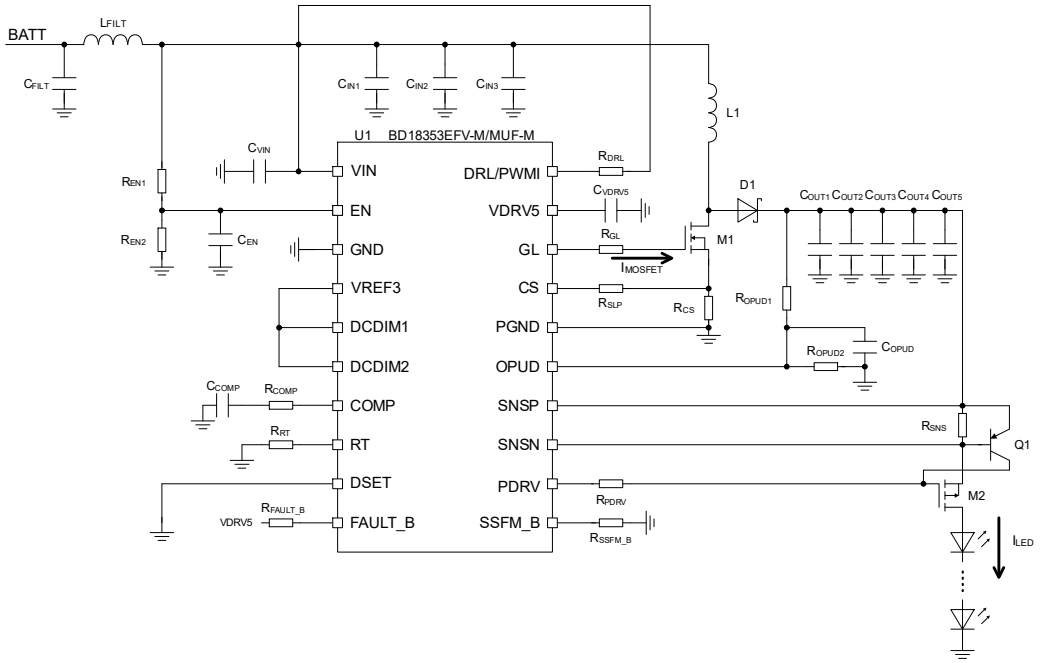
$$I_{LED} = \frac{V_{SNS_100\ \%}}{R_{SNS}} \quad [A]$$

When:

V_{DCDIM1}, V_{DCDIM2} > $V_{DCD_100\ \%}$

Where:

$V_{SNS_100\ \%}$ is the Current sense threshold voltage.



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Description of Blocks - continued

4 PWM Dimming (PWMDIM)

4.1 External P-ch MOSFET Drive

The PDRV pin drives an external P-ch MOSFET to achieve PWM dimming. Connect the gate of the P-ch MOSFET to the PDRV pin. The PDRV pin outputs SNSP and SNSP - 7.5 V (Typ).
At start up and restart (After UVLO, TSD, SCP, OVP is released or after EN = High input.), after DC/DC starts switching, the PDRV pin can output SNSP - 7.5 V (Typ).
The PDRV output voltage and the DC/DC output voltage (SNSP voltage) have the characteristics shown below figure.
When the number of LED lights is small, design and evaluate in consideration of the characteristics shown below figure. There is a possibility that the external P-ch MOSFET cannot be driven.

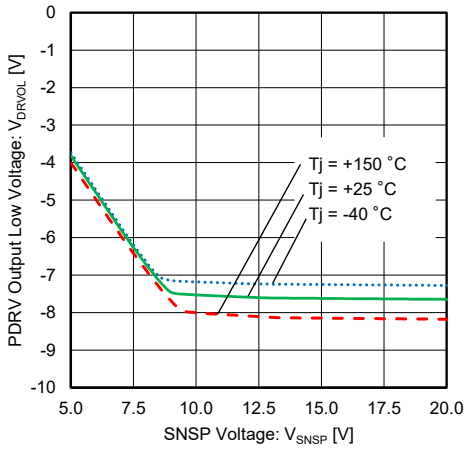


Figure 1. PDRV Output Low Voltage vs SNSP Voltage

4.2 PWM Dimming Duty Setting

The BD18353EFV-M/MUF-M has a built-in PWM dimming pulse generation circuit. The PWM dimming duty is set by the internal ramp waveform and the voltage input to the DSET pin. The DSET pin voltage is set from VREF3 by a resistor voltage divider.
Setting duty D_{PWM} can be calculated by the following formula.

$$D_{PWM} = \frac{V_{DSET} - V_{RAMPB}}{V_{RAMPP} - V_{RAMPB}} \times 100 \quad [\%]$$

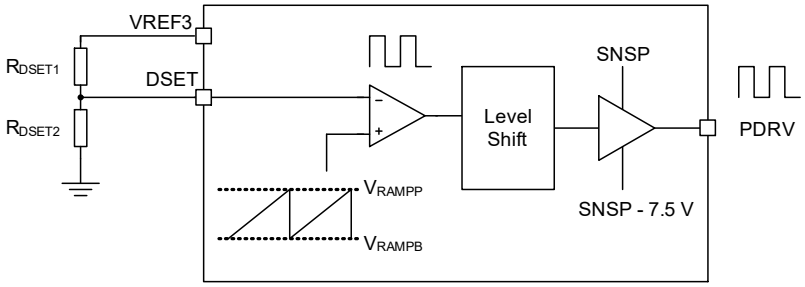
Where:
R_{DSET1}, R_{DSET2} are the PWM dimming duty setting resistor.

$$D_{PWM} = \frac{V_{REF3} \times \frac{R_{DSET2}}{R_{DSET1} + R_{DSET2}} - V_{RAMPB}}{V_{RAMPP} - V_{RAMPB}} \times 100 \quad [\%]$$

If:
R_{DSET1} = 20 kΩ, R_{DSET2} = 10 kΩ

$$D_{PWM}\ (Typ) = \frac{3.00 \times \frac{10\ k\Omega}{20\ k\Omega + 10\ k\Omega} - 0.40}{2.40 - 0.40} \times 100 = 30.0 \quad [\%]$$

Where:
V_{RAMPP} is the internal ramp peak voltage = 2.40 V (Typ).
V_{RAMPB} is the internal ramp bottom voltage = 0.40 V (Typ).



At UVLO detection, OVP detection, SCP detection (during hiccup operation), TSD detection or EN = Low input, the internal ramp waveform becomes V_{RAMPB} voltage.

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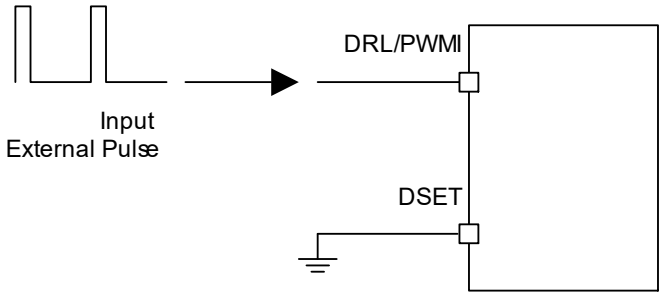
4 PWM Dimming (PWMDIM) - continued

4.3 PWM Dimming by External Pulse Signal Input

When the DRL/PWMI pin voltage is V_{DRLIH} or more, it operates at PWM 100 % duty setting. When the DRL/PWMI pin voltage is V_{DRLIL} or less, it operates at the PWM dimming duty set by the DSET pin. Therefore, to control PWM dimming with external PWM pulse signal, connect the DSET pin to GND and input the PWM signal to the DRL/PWMI pin.

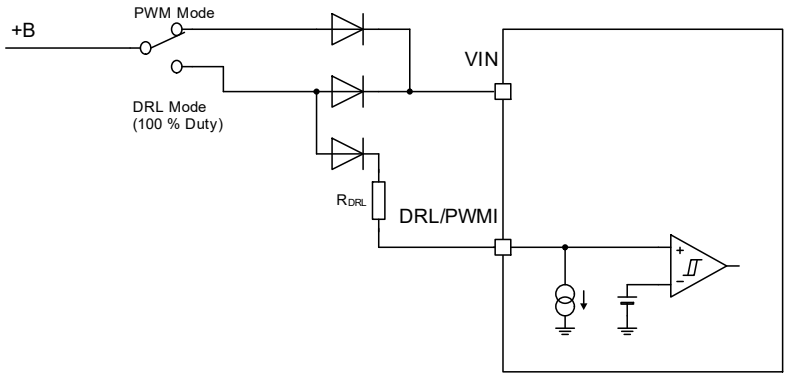


4.4 DRL Mode (100 % Duty) Enable Input

Switching between PWM dimming mode and DRL mode (100 % Duty) can be done with the input voltage at DRL/PWMI pin. When the DRL/PWMI pin voltage is V_{DRLIH} or more, it operates at PWM 100 % duty setting. When the DRL/PWMI pin voltage is V_{DRLIL} or less, it operates at the PWM dimming duty set by the DSET pin.

Because the DRL/PWMI pin is composed of a high-voltage element, it is possible to directly input the battery voltage. The DRL/PWMI pin is pulled down by current.

Considering the short circuit between the DRL/PWMI pin and the VDRV5 pin, it is recommended to insert a limiting resistor R_{DRL} (47 kΩ or more) as shown below figure.



DRL Mode (100 % Duty) Switching Application Example

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Description of Blocks - continued

5 Analog Dimming (DCDIM)

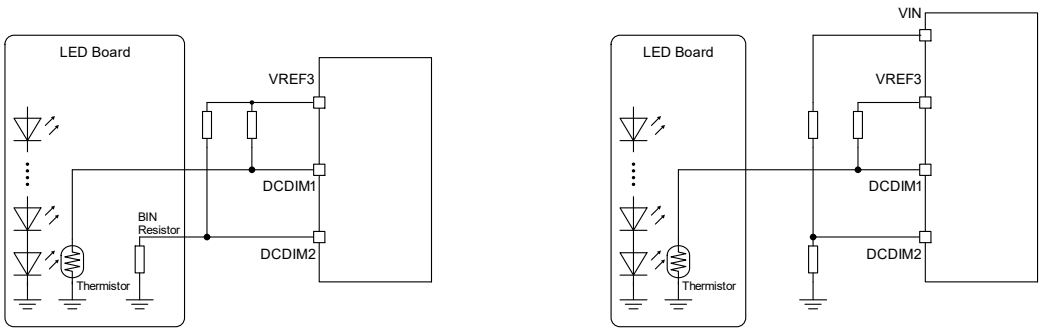
BD18353EFV-M/MUF-M has two systems of analog dimming function. For example, it can be used as in Figure 2. (a) Thermal Derating Function and BIN Setting Function or in Figure 2. (b) Thermal Derating Function and Input Low Voltage Derating Function.

When the DCDIM1 or DCDIM2 pin (The lower voltage takes precedence) becomes 2.2 V (Typ) or less, the LED current decreases.

When not using the analog dimming function, set it to 2.5 V or more, such as connecting DCDIM1, DCDIM2 voltage to the VREF3 pin.

When the analog dimming rate is low, DC/DC control may become unstable and the LED may flicker.

Confirm enough in the evaluation.



(a) Thermal Derating Function and BIN Setting Function

(b) Thermal Derating Function and Input Low Voltage Derating Function

Figure 2. Analog Dimming Application Example

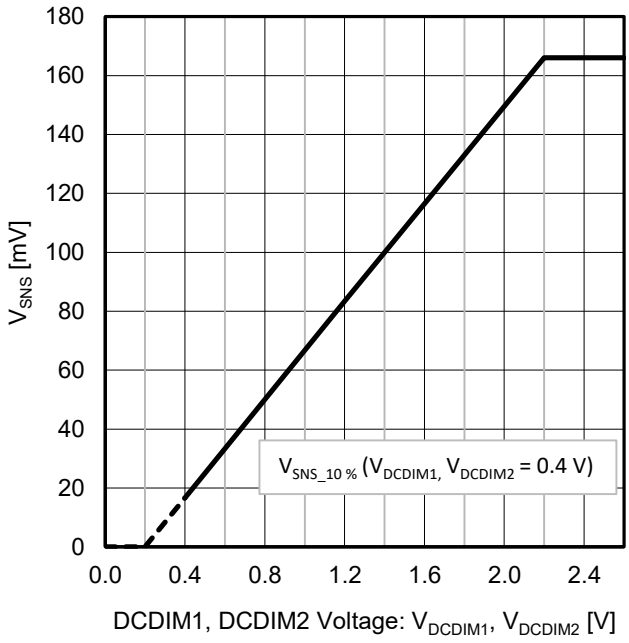


Figure 3. V_{SNS} vs DCDIM1, DCDIM2 Voltage

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Description of Blocks - continued

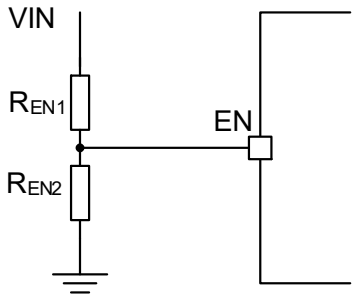
6 Enable Setting (EN)

The BD18353EFV-M/MUF-M can be ON/OFF controlled by the EN pin. It is possible to set the EN pin voltage by a resistor voltage divider from VIN.

$$V_{INON} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times V_{ENIH} \quad [V]$$

$$V_{INOFF} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times V_{ENIL} \quad [V]$$

Where:
V_{ENIH} is the EN High level threshold voltage = 1.0 V (Typ).
V_{ENIL} is the EN Low level threshold voltage = 0.9 V (Typ).



When the EN pin voltage becomes V_{ENIL} or less, the PDRV pin outputs High level to turn off external P-ch MOSFET. DC/DC is stopped and the GL pin outputs Low level.
When pulling up to the VIN pin to fix the EN pin to High, considering the short circuit between the EN pin and the GND pin, it is recommended to insert a limiting resistor.

7 Switching Frequency Setting (OSC)

The switching frequency of the DC/DC can be set by the resistor R_{RT} connected to the RT pin.

$$f_{SW1} \fallingdotseq \frac{9900}{R_{RT}} \times 10^3 \quad \text{[kHz] (200 kHz to 700 kHz)}$$

$$f_{SW2} \fallingdotseq \frac{9000}{R_{RT}} \times 10^3 \quad \text{[kHz] (2.0 MHz to 2.5 MHz)}$$

8 Spread Spectrum Frequency Modulation (SSFM)

BD18353EFV-M/MUF-M has built-in spread spectrum function. It operates at a frequency of ±6 % (Typ) around the frequency f_{SW} set by R_{RT}. The spread spectrum function can be set to ON/OFF by the SSFM_B pin.
To use the spread spectrum function, pull down the SSFM_B pin to GND.
In case the spread spectrum function will not be used, pull up the SSFM_B pin to the VDRV5 pin.
Considering a short circuit between the SSFM_B pin and the PDRV pin, it is recommended to insert a pull up resistor or a pull down resistor (47 kΩ or more).

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Description of Blocks - continued

9 Protection Function

9.1 Under Voltage Lock Out (UVLO)

UVLO is a protection circuit that prevents IC malfunction at power-on or power-off.
When the VIN pin voltage becomes V_{INUVD} or less or the VDRV5 pin voltage becomes $V_{DRV5UVD}$ or less, the PDRV pin outputs high level to turn off external P-ch MOSFET. DC/DC is stopped and GL outputs low level.

9.2 Thermal Shutdown (TSD)

TSD shuts down circuits at 175 °C (Typ) and release them at 150 °C (Typ).

9.3 Over Current Protection (OCP)

When the CS pin voltage becomes V_{CSOCP} or more, over current is detected and the GL pin outputs Low until the next switching cycle.

9.4 Over Voltage Protection (OVP)

OVP voltage can be set by dividing resistors R_{OPUD1}, R_{OPUD2} connected between DC/DC output and GND.
LED open failure can also be detected by the OVP function.
The detection voltage V_{OUT_OVP} is set by the following formula.

$$V_{OUT_OVP} = \frac{R_{OPUD1} + R_{OPUD2}}{R_{OPUD2}} \times V_{OVP} \quad [V]$$

Where:
V_{OVP} is the over voltage protection detect voltage = 1.00 V (Typ).

When OVP is detected, the PDRV pin outputs high level to turn off the external P-ch MOSFET. DC/DC stops and GL outputs low level. FAULT_B outputs low level and outputs error detection.
OVP has hysteresis, and when the OPUD pin voltage becomes V_{OVP} - V_{OVPHYS} or less, DC/DC restarts. When the LED is open, OVP is detected again and the OVP detection operation is repeated.
When OVP is released and the voltage between the SNSP pin and the SNSN pin becomes V_{SG} (Status Good Voltage) or more, FAULT_B outputs high level. FAULT_B holds low output until t_{FAULT_BL} elapses after OVP is released.

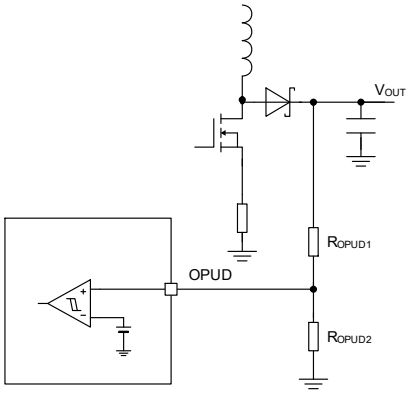

Figure 4. OVP Setting Circuit

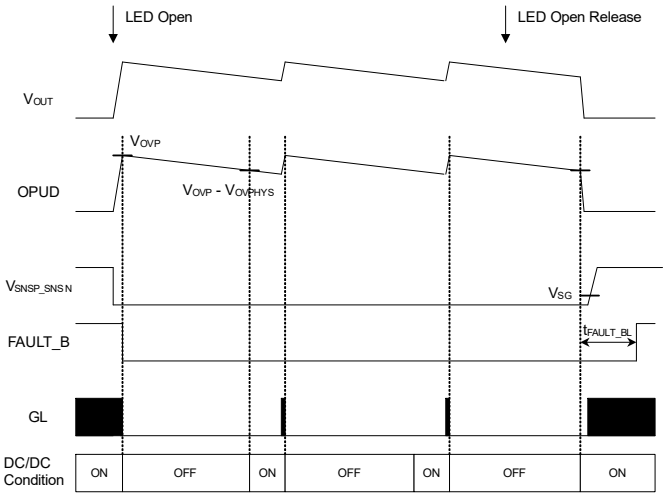

Figure 5. Timing Chart (OVP)

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9 Protection - continued

9.5 Internal Over Voltage Protection (INTOVP)

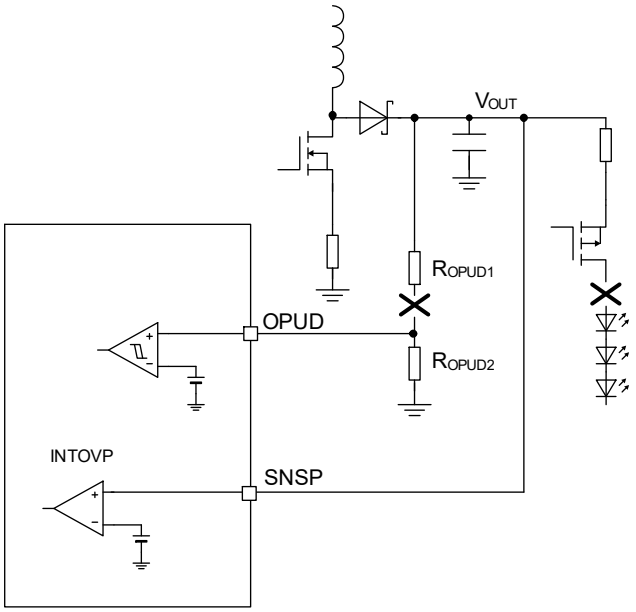
If the LED opens with the resistor R_{OPUD1} open or the OPUD pin grounded (dual fail), the DC/DC is over voltage and the IC destroyed.

The BD18353EFV-M/MUF-M has an internal OVP circuit that monitors the SNSP pin voltage and prevents destruction of the IC.

However, since the threshold value is fixed (V_{INTOVP}), when the absolute voltage of the external parts is low, the parts may be destroyed.

When INTOVP is detected, the PDRV pin outputs High level to turn off the external P-ch MOSFET. DC/DC stops and GL outputs low level. FAULT_B outputs Low level and outputs error detection. When INTOVP is released and the voltage between the SNSP pin and the SNSN pin becomes V_{SG} or more, FAULT_B outputs high level.

FAULT_B holds low output until t_{FAULT_BL} elapses after OVP is released.



INTOVP Circuit

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9 Protection - continued

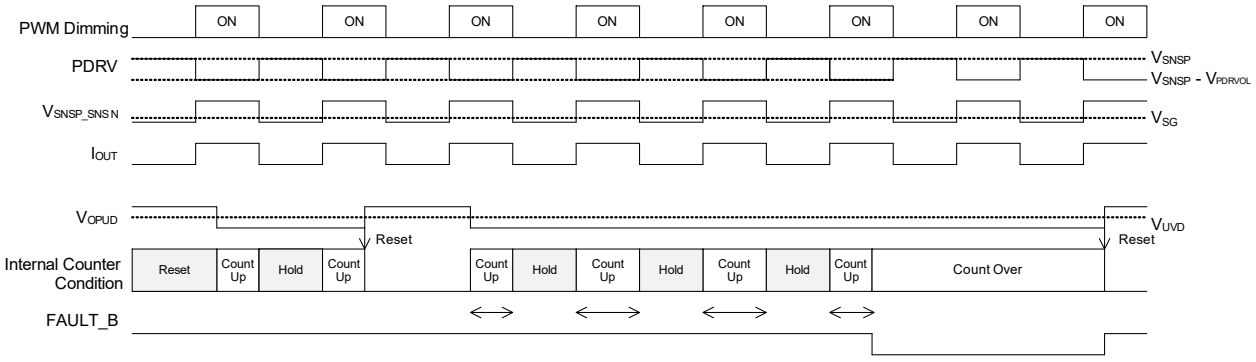
9.6 Under Voltage Detection (UVD)

UVD voltage can be set by dividing resistors R_{OPUD1}, R_{OPUD2} connected between DC/DC output and GND.
The detection voltage (V_{OUT_UVD}) is set by the following formula.

$$V_{OUT_UVD} = \frac{R_{OPUD1}+R_{OPUD2}}{R_{OPUD2}} \times V_{UVD} \quad [V]$$

Where:
V_{UVD} is the under voltage detection threshold voltage = 100 mV (Typ).

UVD is detected when the OPUD pin voltage become V_{UVD} or less. UVD is monitored when the voltage between the SNSP pin and the SNSN pin becomes V_{SG} or more in the ON section of PWM dimming.
After detection the internal counter starts. When the voltage between the SNSP pin and the SNSN pin becomes V_{SG} or more in the ON section of PWM dimming, it counts up. When the total time reaches t_{UVD}, the FAULT_B outputs becomes Low.
After UVLO, TSD, SCP, OVP is released or after EN = High input, until t_{UVDDIS} has elapsed, UVD does not be detected.



Timing Chart (UVD)

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9 Protection - continued

9.7 Short Circuit Protection (SCP)

When the anode of the LED is shorted to GND, the voltage between the SNSP pin and the SNSN pin can be monitored and protected by SCP.

When the voltage between the SNSP pin and the SNSN pin become V_{SCPON} or more, SCP is detected after SCP delay time (t_{SCPDLY}).

When SCP is detected, the PDRV pin outputs High level to turn off the external P-ch MOSFET. DC/DC stops and GL outputs Low level. FAULT_B outputs Low level and outputs error detection.

Restart after hiccup time (t_{HICCUP}) elapses. If the anode of the LED is shorted to GND, the SCP is detected again and the operation is repeated.

FAULT_B holds Low output until t_{FAULT_BL} after restart.

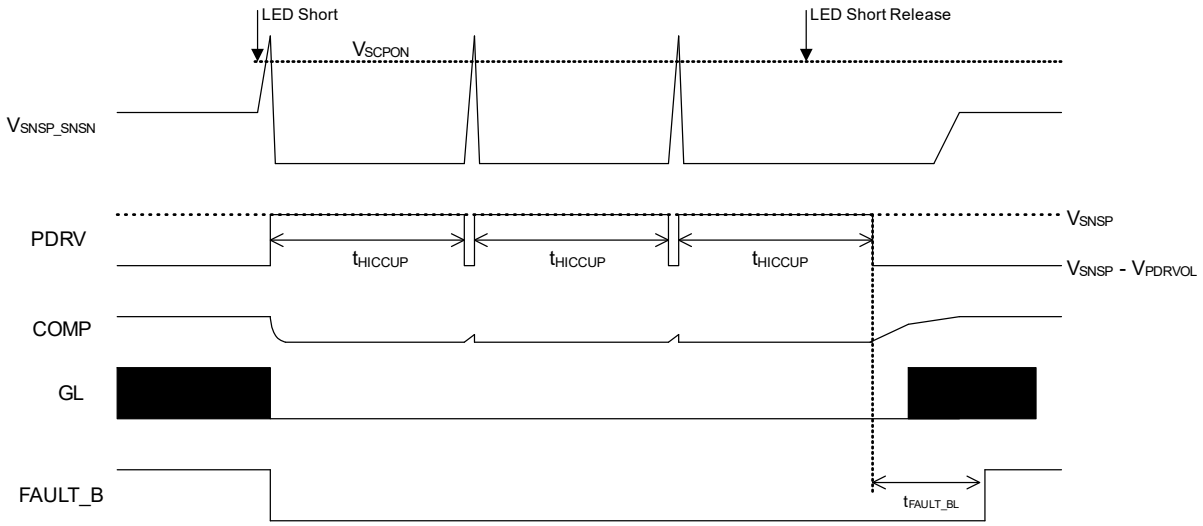

Figure 6. Timing Chart (SCP)

When the anode of the LED is shorted to GND, the voltage between the SNSP pin and the SNSN pin may exceed the absolute voltage. It is recommended to insert a PNP transistor as shown below figure and clamp the voltage. Design to take full consideration of power dissipation of R_{SNS} and P-ch MOSFET.

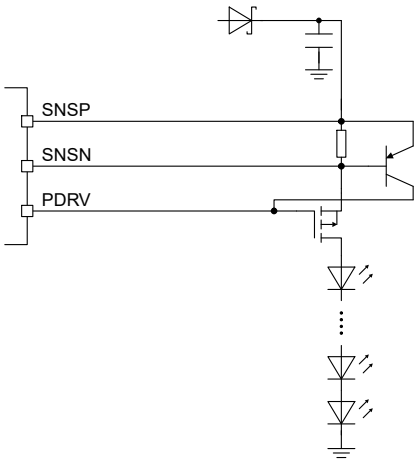

Figure 7. Example of Current Clamp Circuit

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Description of Blocks - continued

10 Outputs Abnormal Status (FAULT_B)

The following table summarizes the device behavior under fault condition.

Fault Description Operations

Protection Function	Operation at Detection			FAULT_B Output
	DC/DC	PDRV Pin	COMP Pin	
EN = Low Detect	OFF	High (= SNSP)	Discharge	Hiz
VIN UVLO Detect	OFF	High (= SNSP)	Discharge	Hiz
VDRV5 UVLO Detect	OFF	High (= SNSP)	Discharge	Hiz
TSD Detect	OFF	High (= SNSP)	Discharge	Hiz
DC/DC OCP Detect	OFF	-	-	-
DC/DC OVP Detect	OFF	High (= SNSP)	Discharge	Low
DC/DC INTOVP Detect	OFF	High (= SNSP)	Discharge	Low
DC/DC UVD Detect	-	-	-	Low (after counting t_{UVD})
SCP Detect	OFF	High (= SNSP)	Discharge	Low

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Absolute Maximum Ratings (Tj = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Pin Voltage (VIN)	V_{IN}	-0.3 to +70	V
EN, DRL/PWMI Pin Voltage	V_{EN}, $V_{DRL/PWMI}$	-0.3 to +70	V
SNSP, SNSN Pin Voltage	V_{SNSP}, V_{SNSN}	-0.3 to +70	V
PDRV Pin Voltage	V_{PDRV}	-0.3 to +70	V
OPUD, SSFM_B Pin Voltage	V_{OPUD}, V_{SSFM_B}	-0.3 to +70	V
SNSP to OPUD Pin Voltage	V_{SNSP_OPUD}	-7 to +70	V
SNSP to SSFM_B Pin Voltage	$V_{SNSP_SSFM_B}$	-7 to +70	V
SNSP to SNSN Pin Voltage	V_{SNSP_SNSN}	-0.3 to +0.6	V
SNSP to PDRV Pin Voltage	V_{SNSP_PDRV}	-0.3 to +10	V
VDRV5 Pin Voltage	V_{DRV5}	-0.3 to +7	V
VIN to VDRV5 Pin Voltage	V_{VIN_VDRV5}	-0.3 to +70	V
VREF3, DCDIM1, DCDIM2, COMP, RT, DSET Pin Voltage	V_{REF3}, V_{DCDIM1}, V_{DCDIM2}, V_{COMP}, V_{RT}, V_{DSET}	-0.3 to +7	V
GL, CS Pin Voltage	V_{GL}, V_{CS}	-0.3 to +7	V
FAULT_B Pin Voltage	V_{FAULT_B}	-0.3 to +7	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

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Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSSOP-B20				
Junction to Ambient	θ_{JA}	143.0	26.8	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	8	4	°C/W
VQFN20FV3535				
Junction to Ambient	θ_{JA}	181.9	50.5	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	19	7	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of all layers.

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Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (VIN)*(Note 1)*	V_{IN}	5	13	65	V
Output Voltage (SNSP)	V_{SNSP}	-	-	65	V
PWM Frequency Input	f_{PWMI}	30	-	2000	Hz
PWM Minimum Pulse Width	t_{MIN}	10	-	-	μs
Switching Frequency	f_{SW}	200	-	2500	kHz
Operating Ambient Temperature	Topr	-40	-	+125	°C

(Note 1) ASO should not be exceeded.

Recommended Setting Parts Range

Parameter	Symbol	Min	Typ	Max	Unit
Capacitor Connecting to the VIN Pin*(Note 2)*	C_{VIN}	1.4	2.2	-	μF
Capacitor Connecting to the VDRV5 Pin*(Note 2)*	C_{VDRV5}	1.4	2.2	3.3	μF
Capacitor Connecting to the COMP Pin*(Note 2)*	C_{COMP}	0.6	1.0	1.5	μF
Total DC/DC Output Capacitor*(Note 2)*	C_{OUT}	10	-	-	μF
Resistor Connecting to the EN Pin	R_{EN1}, R_{EN2}	4.7	-	100	kΩ
Resistor Connecting to the COMP Pin	R_{COMP}	-	33	100	Ω
Resistor Connecting to the RT Pin	R_{RT}	3.9	-	49	kΩ
Resistor Connecting to the DSET1,DSET2 Pin	R_{DSET1}, R_{DSET2}	4.7	-	100	kΩ
Resistor Connecting to the FAULT_B Pin	R_{FAULT_B}	10	-	-	kΩ
Resistor Connecting to the SSFM_B Pin	R_{SSFM_B}	47	-	-	kΩ
Resistor Connecting to the DRL/PWMI Pin	R_{DRL}	47	-	-	kΩ
Resistor Connecting to the Upper Side of the OPUD Pin	R_{OPUD1}	450	-	1000	kΩ

(Note 2) Set the capacitor in consideration of temperature characteristics and DC bias characteristics.

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Electrical Characteristics
(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Total]						
VIN Circuit Current 1	I_{IN1}	-	380	580	μA	V_{EN} = 0 V, No switching
VIN Circuit Current 2	I_{IN2}	-	1.7	2.3	mA	V_{EN} = 5 V $V_{SNSP_SNSN} > V_{SNS_100\ \%}$ $V_{DCDIM1} = V_{DCDIM2}$ = 3.0 V
VIN UVLO Detect Voltage	V_{INUVD}	4.10	4.30	4.49	V	VIN falling
VIN UVLO Release Voltage	V_{INUVR}	4.49	4.70	4.91	V	VIN rising
VIN UVLO Hysteresis Voltage	$V_{INUVHYS}$	-	0.4	-	V	V_{INUVR} - V_{INUVD}
VDRV5 UVLO Detect Voltage	$V_{DRV5UVD}$	3.94	4.15	4.38	V	V_{DRV5} falling
VDRV5 UVLO Release Voltage	$V_{DRV5UVR}$	4.22	4.45	4.68	V	V_{DRV5} rising
VDRV5 UVLO Hysteresis Voltage	$V_{DRV5UVHYS}$	-	0.3	-	V	$V_{DRV5UVR}$ - $V_{DRV5UVD}$
[Reference Voltage]						
VDRV5 Reference Voltage	V_{DRV5}	4.76	5.00	5.25	V	C_{VDRV5} = 2.2 μF I_{VDRV5} = 0 mA to 10 mA load
VDRV5 Drop Voltage	V_{DRV5DP}	-	0.25	0.65	V	VIN = 4.75 V I_{VDRV5} = 10 mA load
VDRV5 Output Current Limit	I_{DRV5LM}	45	-	-	mA	
VREF3 Reference Voltage	V_{REF3}	2.91	3.00	3.09	V	I_{VREF3} = 0 mA to 2 mA load
VREF3 Output Current Limit	I_{REF3LM}	2	-	-	mA	
[EN]						
EN Pull Down Current	I_{EN}	0.6	1.2	1.8	μA	V_{EN} = 5 V
EN High Level Threshold Voltage	V_{ENIH}	0.96	1.00	1.04	V	V_{EN} rising
EN Low Level Threshold Voltage	V_{ENIL}	0.86	0.90	0.94	V	V_{EN} falling
EN Hysteresis Voltage	V_{ENHYS}	-	0.1	-	V	V_{ENIH} - V_{ENIL}
[OSCILLATOR Circuit]						
Switching Frequency 1	f_{SW1}	270	300	330	kHz	R_{RT} = 33 kΩ
Switching Frequency 2	f_{SW2}	2070	2300	2530	kHz	R_{RT} = 3.9 kΩ
RT Output Voltage	V_{RT}	-	0.8	-	V	V_{SSFM_B} = 4 V
Spread Spectrum Frequency	f_{SSFM}	-	f_{SW}/1024	-	Hz	V_{SSFM_B} = 0 V
Spread Spectrum Frequency Modulation Width	f_{SSFMW}	-	±6	-	%	V_{SSFM_B} = 0 V
SSFM_B High Level Input Voltage	V_{SSFM_BIH}	3.0	-	-	V	Spread spectrum disable
SSFM_B Low Level Input Voltage	V_{SSFM_BIL}	-	-	0.4	V	Spread spectrum enable
SSFM_B Pull Down Resistor	R_{SSFM_BD}	200	400	800	kΩ	SSFM_B = 4 V

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Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[N-ch Gate Driver]						
GL ON Resistor High	R_{GLH}	-	1.0	2.5	Ω	I_{GL} = 10 mA load
GL ON Resistor Low	R_{GLL}	-	0.6	1.5	Ω	I_{GL} = 10 mA input
Minimum OFF Time 1	$t_{OFFMIN1}$	-	60	-	ns	R_{RT} = 33 kΩ
Minimum OFF Time 2	$t_{OFFMIN2}$	-	35	-	ns	R_{RT} = 3.9 kΩ
[DC/DC Current Detection]						
Over Current Detection Voltage	V_{CSOCP}	275	300	321	mV	V_{CS} rising
CS Pin Leading Edge Blanking Time	t_{CSBLK}	-	120	-	ns	
Slope Compensation Current Peak	I_{CSSLPP}	-	50	-	µA	
CS to COMP Level Shift Voltage	$V_{CSCMPLS}$	-	1.26	-	V	No slope compensation added
[Error Amplifier]						
Trans Conductance	g_M	-	1300	-	µS	V_{SNSP_SNSN} = 166.5 mV
COMP Sink Current	I_{COMPSI}	-	200	-	µA	V_{SNSP_SNSN} = 83.3 mV V_{DCDIM1} = V_{DCDIM2} = 0 V
COMP Source Current	I_{COMPSO}	-	200	-	µA	V_{SNSP_SNSN} = 83.3 mV V_{DCDIM1} = V_{DCDIM2} = 3.0 V

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Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Current Sense Amplifier]						
LED Current Sense Voltage 100 %	$V_{SNS_100\ \%}$	165.0	166.7	171.7	mV	Tj = +25 °C $V_{SNS_100\ \%} = V_{SNSP} - V_{SNSN}$ V_{SNSN} = 0 V, 30 V $V_{DCDIM1} = V_{DCDIM2}$ = 2.5 V
		161.7	166.7	171.7	mV	Tj = -40 °C to +125 °C $V_{SNS_100\ \%} = V_{SNSP} - V_{SNSN}$ V_{SNSN} = 0 V, 30 V $V_{DCDIM1} = V_{DCDIM2}$ = 2.5 V
LED Current Sense Voltage 90 %	$V_{SNS_90\ \%}$	146	150	153	mV	$V_{SNS_90\ \%} = V_{SNSP} - V_{SNSN}$ V_{SNSN} = 0 V, 30 V V_{DCDIM1} = 2.0 V V_{DCDIM2} = 2.5 V
LED Current Sense Voltage 10 %	$V_{SNS_10\ \%}$	13.7	16.7	19.7	mV	$V_{SNS_10\ \%} = V_{SNSP} - V_{SNSN}$ V_{SNSN} = 0 V, 30 V V_{DCDIM1} = 0.4 V V_{DCDIM2} = 2.5 V
Common-mode Input Range High Side Voltage Detection	V_{SNSN_HSS}	1.9	2.0	2.1	V	V_{SNSN} rising
Common-mode Input Range Low Side Voltage Detection	V_{SNSN_LSS}	1.8	1.9	2.0	V	V_{SNSN} falling
SNSP Pin Input Current High Side Voltage	I_{SNSP_HSS}	160	330	530	µA	V_{SNSP_SNSN} = 166.5 mV V_{SNSN} = 60 V
SNSN Pin Input Current High Side Voltage	I_{SNSN_HSS}	18	35	54	µA	V_{SNSP_SNSN} = 166.5 mV V_{SNSN} = 60 V
SNSP Pin Input Current Low Side Voltage	I_{SNSP_LSS}	-8	-4	-2	µA	V_{SNSP_SNSN} = 166.5 mV V_{SNSN} = 0 V
SNSN Pin Input Current Low Side Voltage	I_{SNSN_LSS}	-92	-50	-28	µA	V_{SNSP_SNSN} = 166.5 mV V_{SNSN} = 0 V
Short Circuit Protection Threshold Voltage	V_{SCPON}	325	350	375	mV	V_{SNSP_SNSN} rising
Short Circuit Protection Delay Time	t_{SCPDLY}	40	50	60	µs	
Hiccup Time	t_{HICCUP}	33	40	48	ms	Short circuit detect
[Over Voltage Protection / Under Voltage Detection]						
Over Voltage Protection Detect Voltage	V_{OVP}	0.96	1.00	1.04	V	V_{OPUD} rising
Over Voltage Protection Hysteresis Voltage	V_{OVPHYS}	-	0.1	-	V	
Under Voltage Detection Threshold Voltage	V_{UVD}	-	100	-	mV	
Internal Over Voltage Protection Detect Voltage	V_{INTOVP}	65	-	-	V	V_{SNSP} monitor

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Electrical Characteristics - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[PWM Dimming]						
PWM Dimming Frequency	f_{PWM}	320	400	480	Hz	
Internal Ramp Bottom Voltage	V_{RAMPB}	V_{REF3} / 3 x 0.4 - 0.02	V_{REF3} / 3 x 0.4	V_{REF3} / 3 x 0.4 + 0.02	V	
Internal Ramp Peak Voltage	V_{RAMPP}	V_{REF3} / 3 x 2.4 - 0.02	V_{REF3} / 3 x 2.4	V_{REF3} / 3 x 2.4 + 0.02	V	
DSET Pin Input Current	I_{DSET}	-	0	1	µA	V_{DSET} = 3.0 V
PDRV Pull Up ON Resistor	R_{PDRV_U}	-	20	50	Ω	I_{PDRV} = 10 mA load V_{SNSP} = 30 V V_{DSET} = 0 V, $V_{DRL/PWMI}$ = 0 V
PDRV Pull Down Current	I_{PDRV_D}	17	38	65	mA	V_{SNSP_PDRV} = 0 V, V_{SNSP} = 30 V V_{DSET} = 5 V, $V_{DRL/PWMI}$ = 0 V
PDRV Output Low Voltage	V_{PDRVOL}	6.5	7.5	9.0	V	V_{SNSP_PDRV}, V_{SNSP} = 30 V
[DRL Mode]						
DRL/PWMI Threshold Voltage DRL Mode	V_{DRLIH}	1.42	1.50	1.58	V	$V_{DRL/PWMI}$ rising
DRL/PWMI Threshold Voltage PWM Mode	V_{DRLIL}	0.95	1.00	1.05	V	$V_{DRL/PWMI}$ falling
DRL/PWMI Hysteresis Voltage	$V_{DRLIHYS}$	-	0.5	-	V	V_{DRLIH} - V_{DRLIL}
DRL/PWMI Pull Down Current	$I_{DRL/PWMI}$	0.5	1.0	2.0	µA	$V_{DRL/PWMI}$ = 5 V
[Analog Dimming]						
DCDIM1, DCDIM2 0 % Threshold Voltage	$V_{DCD_0\ \%}$	0.17	0.20	0.23	V	V_{DCDIM1}, V_{DCDIM2}
DCDIM1, DCDIM2 100 % Threshold Voltage	$V_{DCD_100\ \%}$	2.14	2.20	2.26	V	V_{DCDIM1}, V_{DCDIM2}
DCDIM1, DCDIM2 Pin Input Current	I_{DCD}	-	0	1	µA	V_{DCDIM1} = V_{DCDIM2} = 3.0 V
[Outputs LED Status]						
FAULT_B Output Low Voltage	V_{FAULT_BOL}	-	0.1	0.4	V	I_{FAULT_B} = 5 mA input
FAULT_B Leak Current	I_{FAULT_B}	-	0	1	µA	V_{FAULT_B} = 5.5 V
Under Voltage Detection Time	t_{UVD}	16	20	24	ms	
Under Voltage Detection Disable Time	t_{UVDDIS}	16	20	24	ms	EN = Low to High VIN UVLO release VDRV5 UVLO release TSD release
FAULT_B Pin Holds Low Output Time	t_{FAULT_BL}	16	20	24	ms	SCP release OVP release
Status Good Voltage	V_{SG}	-	20	-	mV	V_{SNSP_SNSN} rising

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Typical Performance Curves
(Unless otherwise specified V_{IN} = 13 V, Tj = +25 °C)

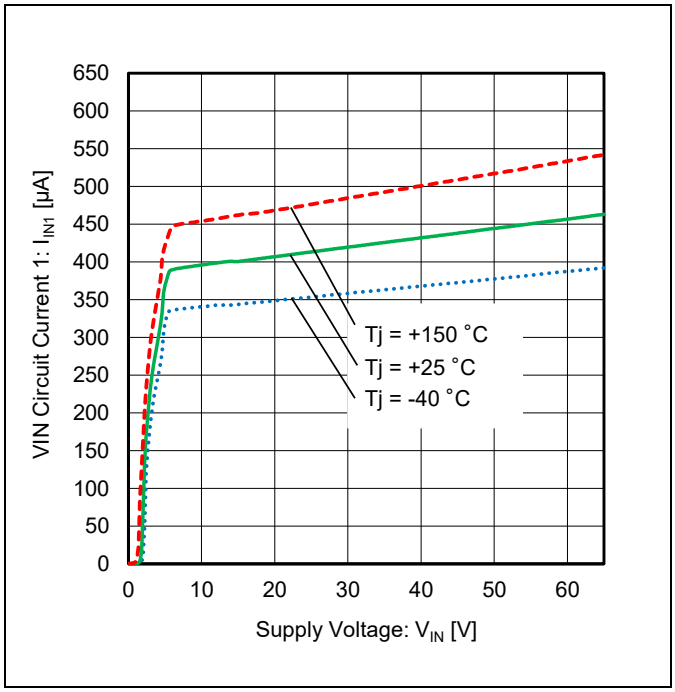

Figure 8. VIN Circuit Current 1 vs Supply Voltage

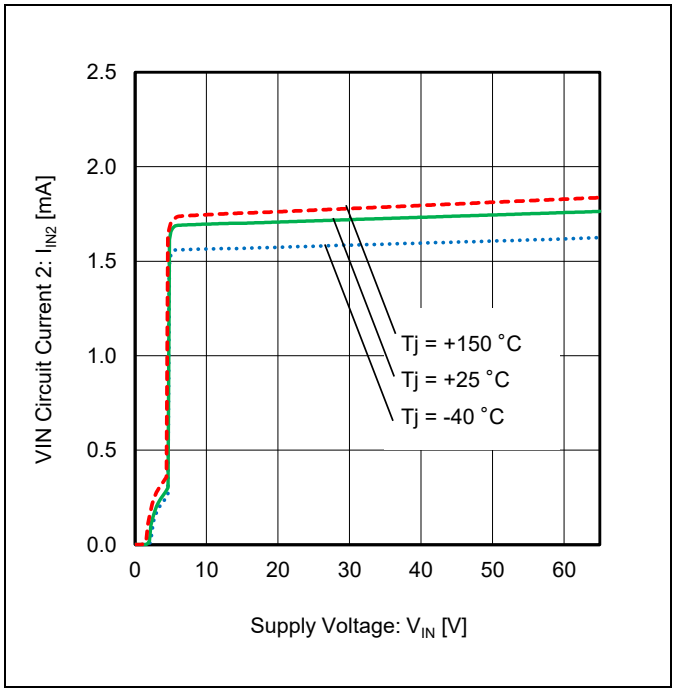

Figure 9. VIN Circuit Current 2 vs Supply Voltage

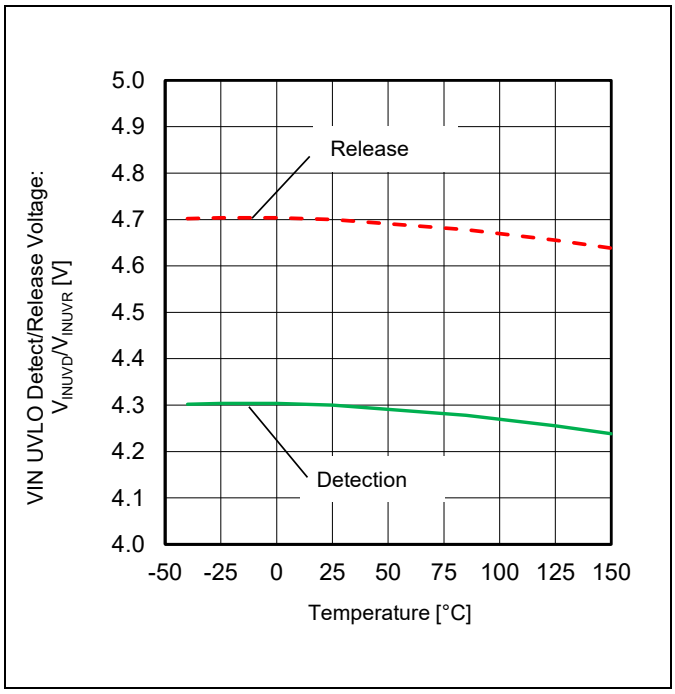

Figure 10. VIN UVLO Detect/Release Voltage vs Temperature

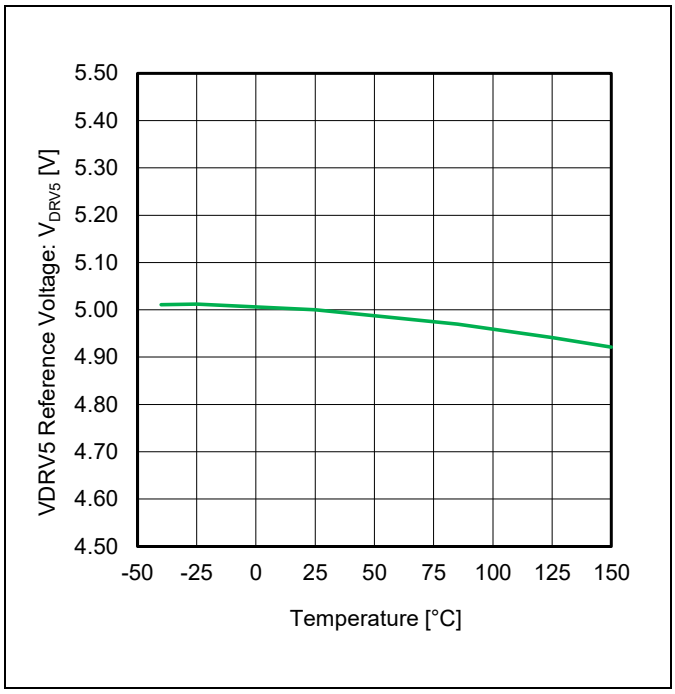

Figure 11. VDRV5 Reference Voltage vs Temperature

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = +25 °C)

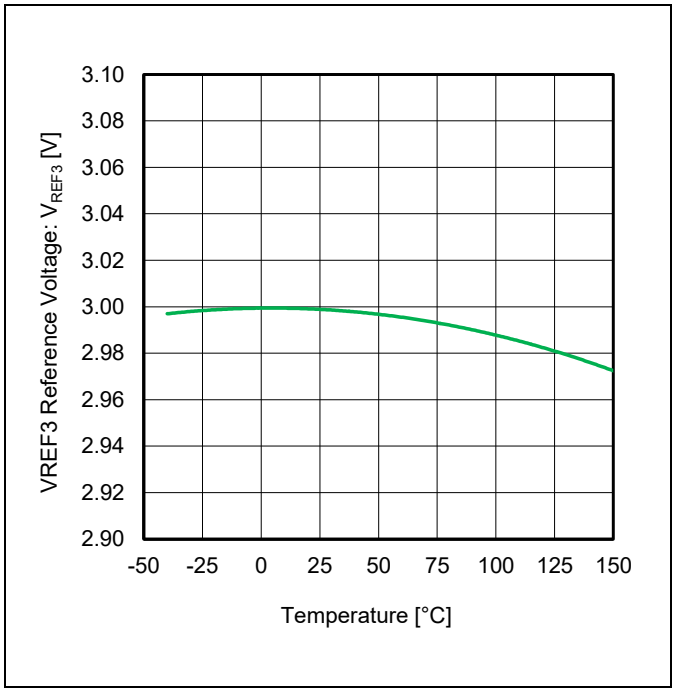

Figure 12. VREF3 Reference Voltage vs Temperature
(I_{VREF3} = 0 mA to 2 mA load)

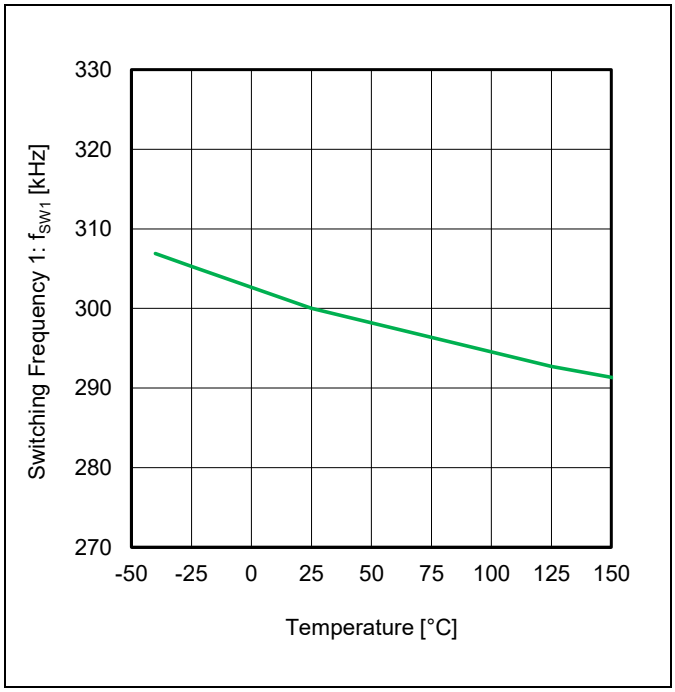

Figure 13. Switching Frequency 1 vs Temperature
(R_{RT} = 33 kΩ)

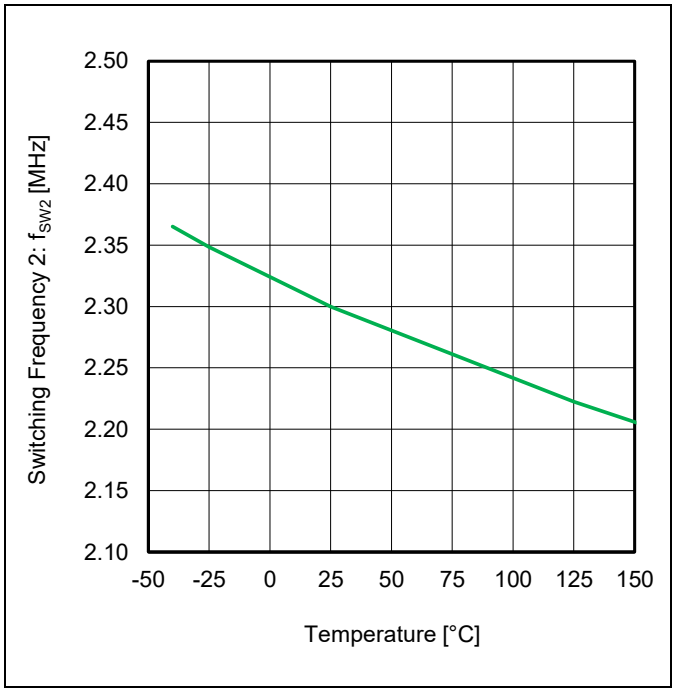

Figure 14. Switching Frequency 2 vs Temperature
(R_{RT} = 3.9 kΩ)

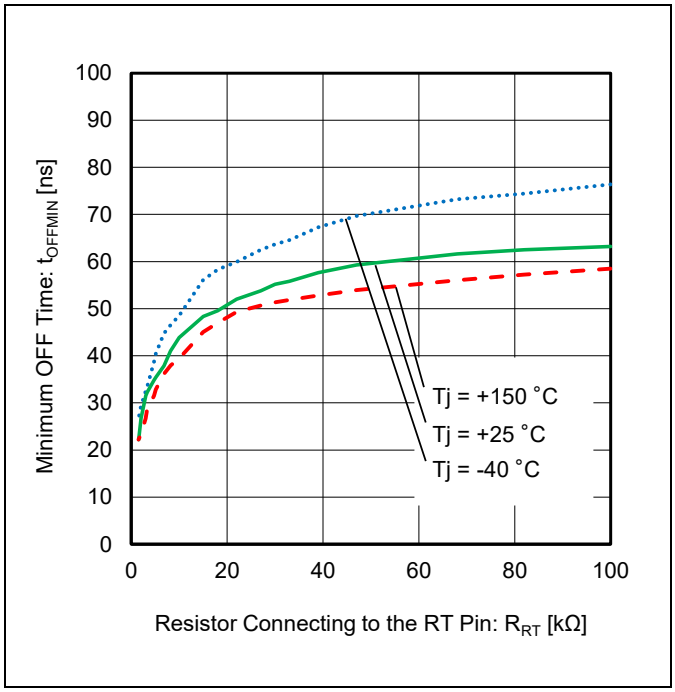

Figure 15. Minimum OFF Time vs
Resistor Connecting to the RT Pin

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = +25 °C)

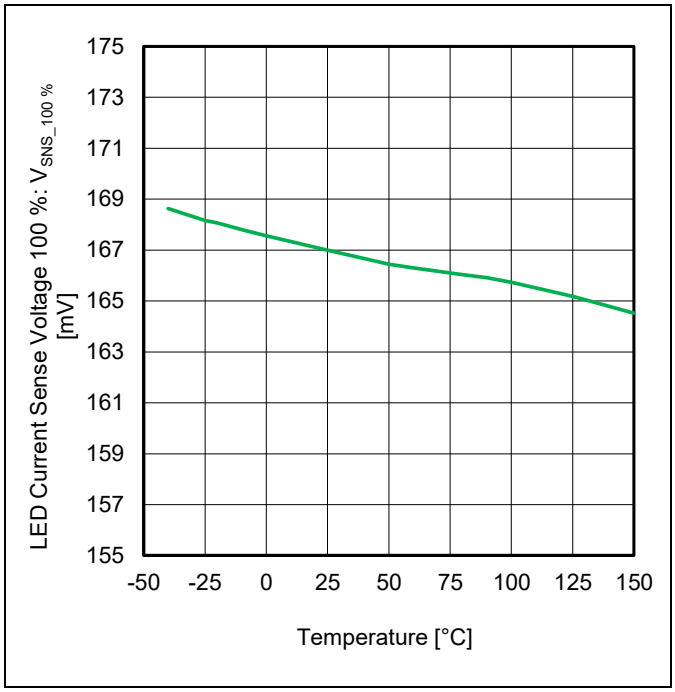

Figure 16. LED Current Sense Voltage 100 % vs Temperature
(V_{DCDIM1} = V_{DCDIM2} = 2.5 V)

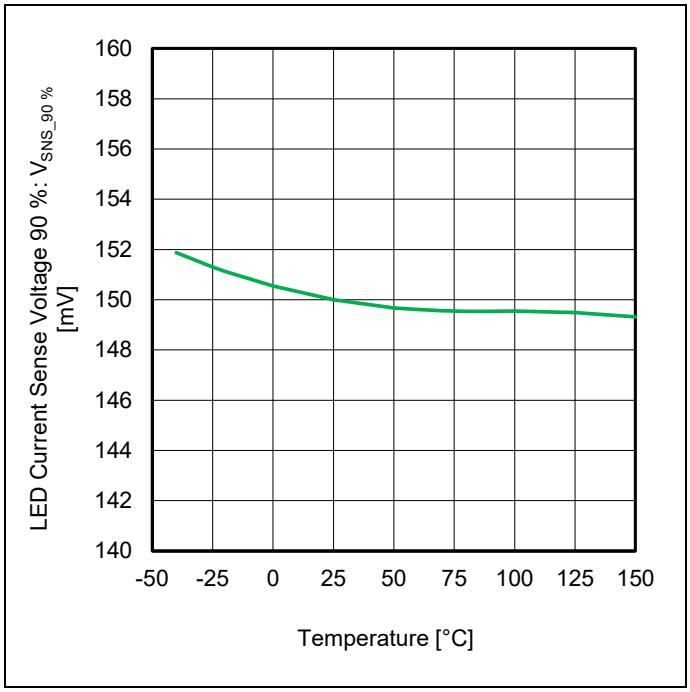

Figure 17. LED Current Sense Voltage 90 % vs Temperature
(V_{DCDIM1} = 2.0 V, V_{DCDIM2} = 2.5 V)

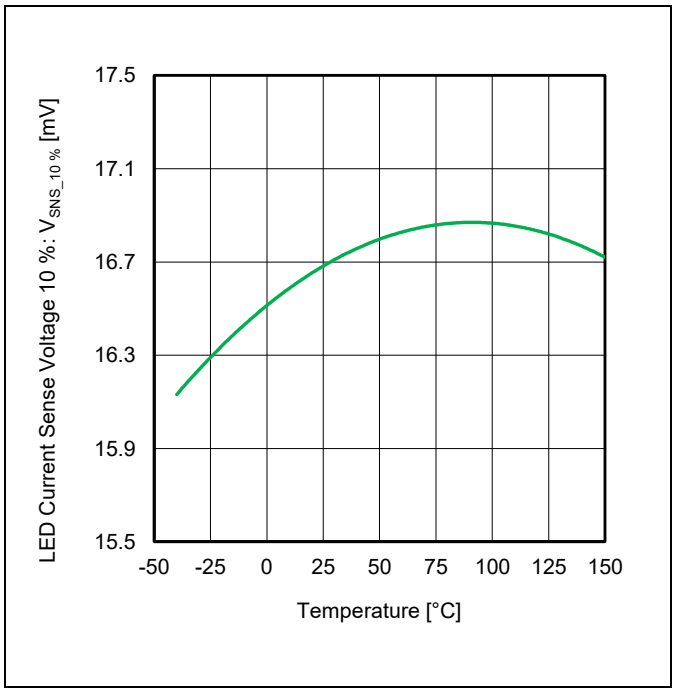

Figure 18. LED Current Sense Voltage 10 % vs Temperature
(V_{DCDIM1} = 0.4 V, V_{DCDIM2} = 2.5 V)

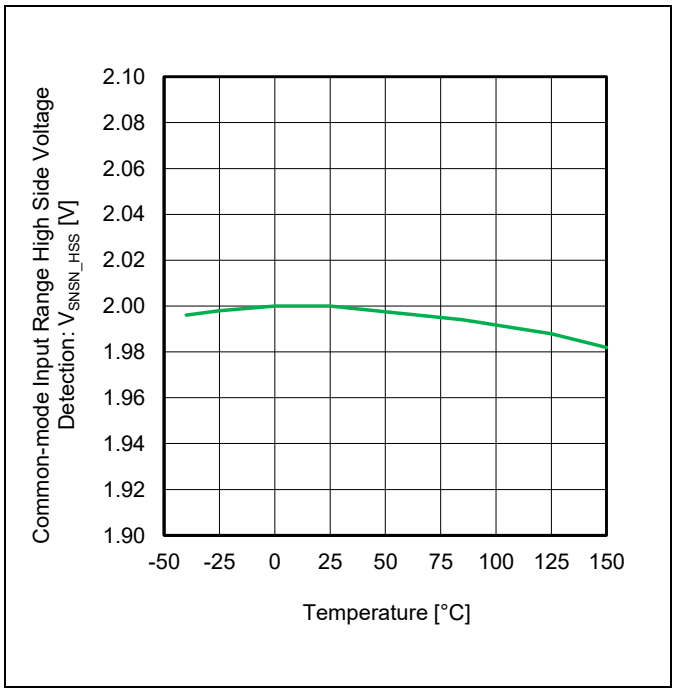

Figure 19. Common-mode Input Range High Side Voltage Detection vs Temperature

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = +25 °C)

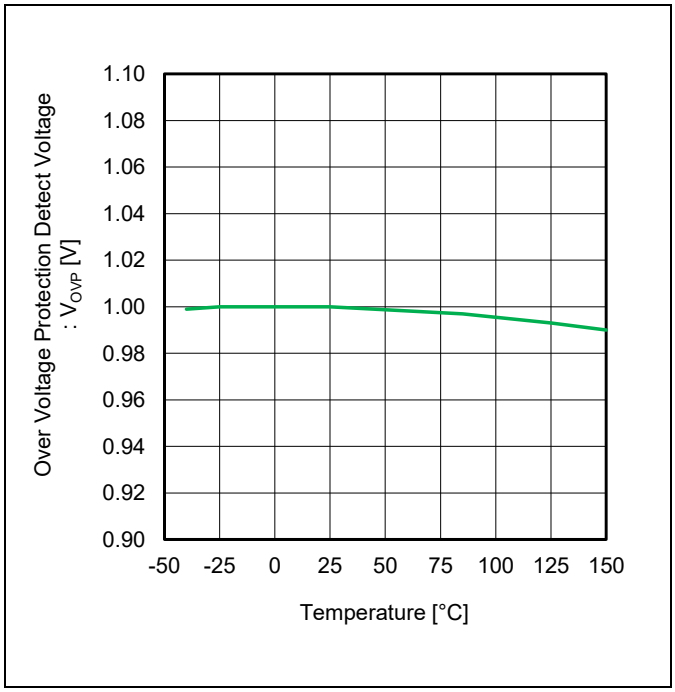

Figure 20. Over Voltage Protection Detect Voltage vs Temperature

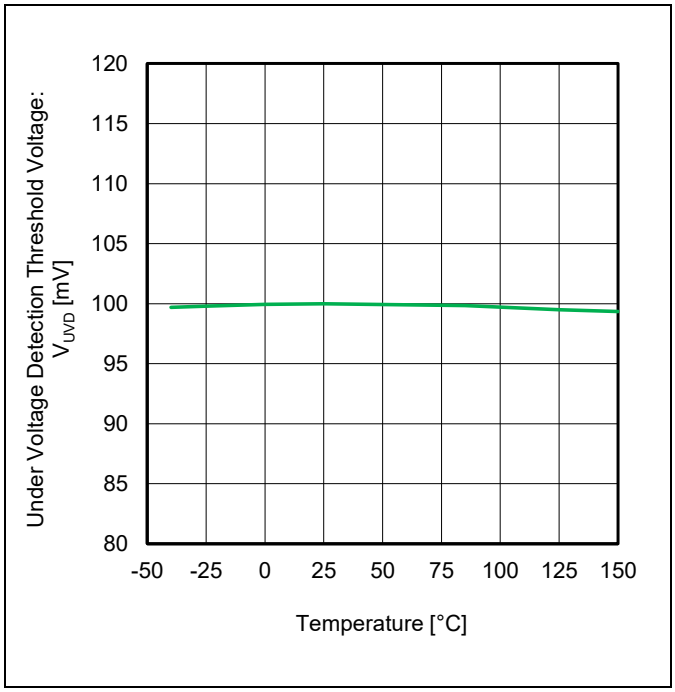

Figure 21. Under Voltage Detection Threshold Voltage vs Temperature

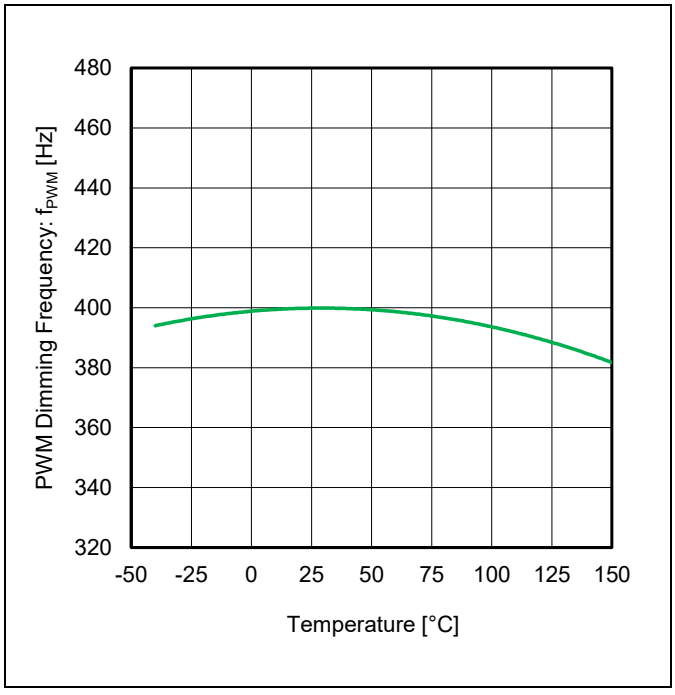

Figure 22. PWM Dimming Frequency vs Temperature

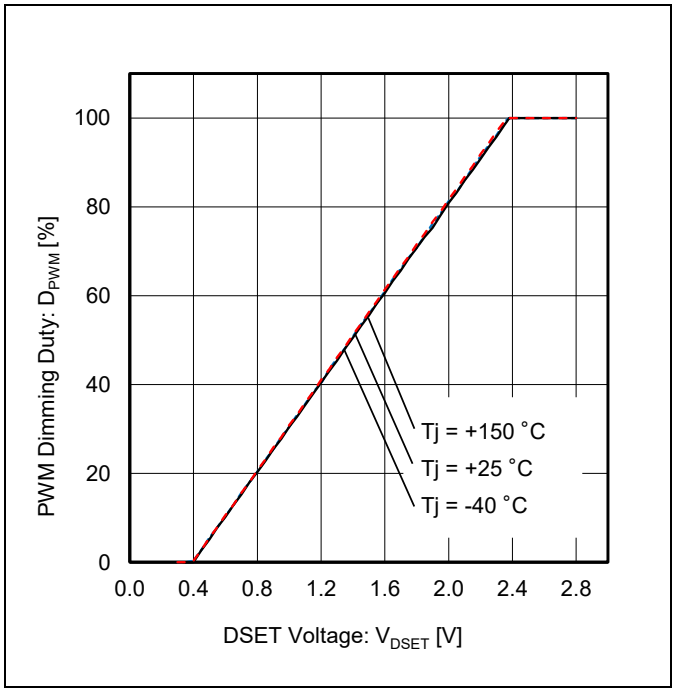

Figure 23. PWM Dimming Duty vs DSET Voltage

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Typical Performance Curves - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = +25 °C)

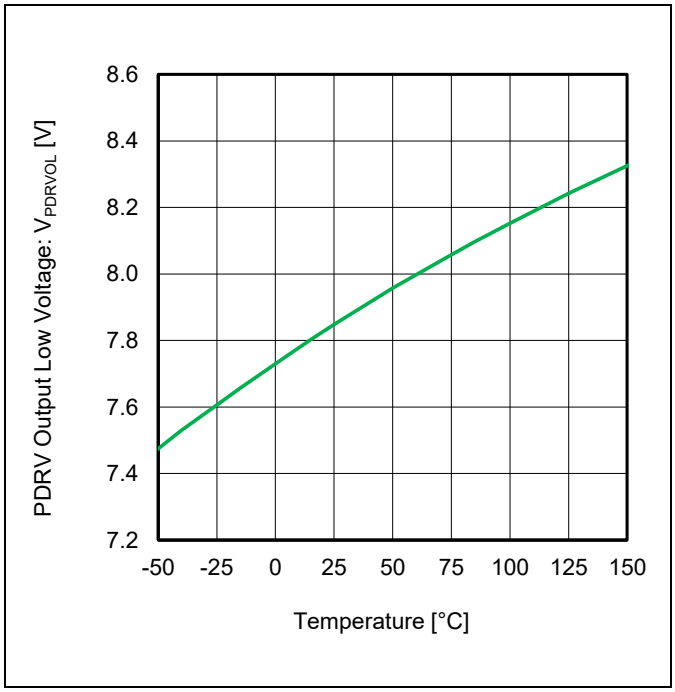

Figure 24. PDRV Output Low Voltage vs Temperature

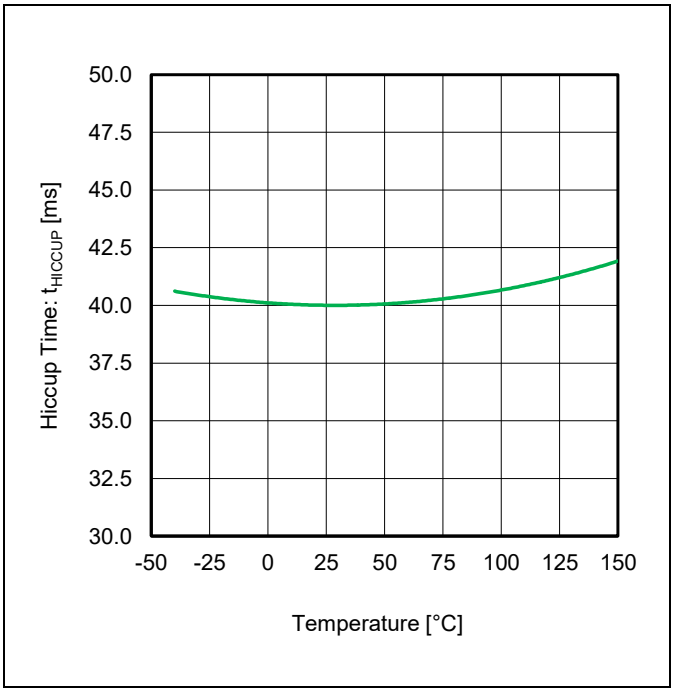

Figure 25. Hiccup Time vs Temperature

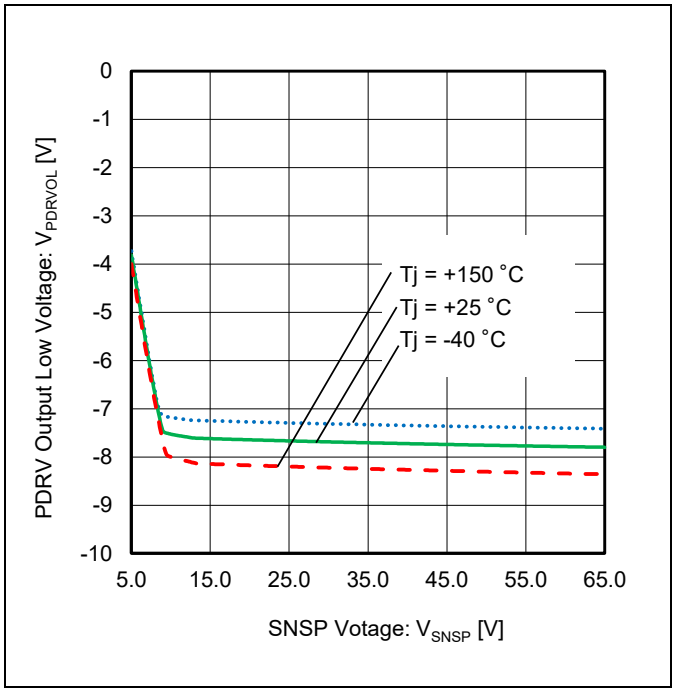

Figure 26. PDRV Output Low Voltage vs SNSP Voltage

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Typical Performance Curves - continued
(Application Examples 1 BOOST (Position Mode / DRL Mode))

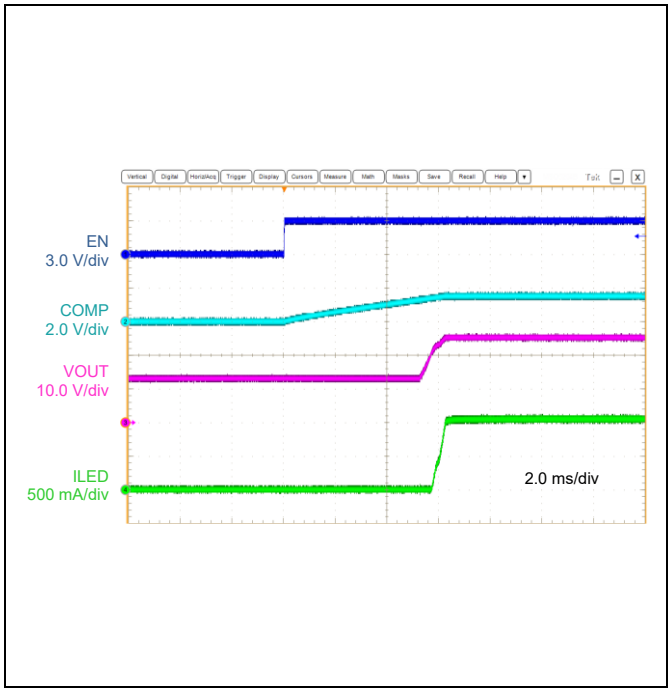

Figure 27. EN Power ON (DRL Mode)

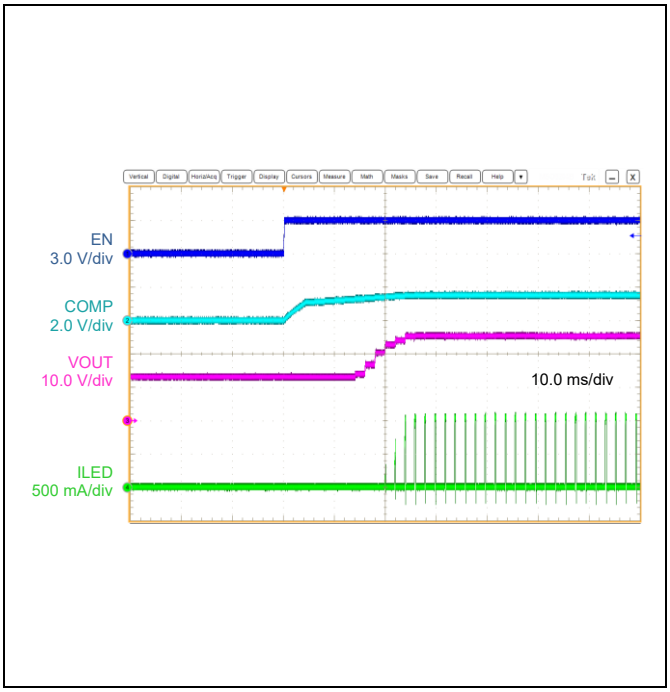

Figure 28. EN Power ON (PWM Mode)

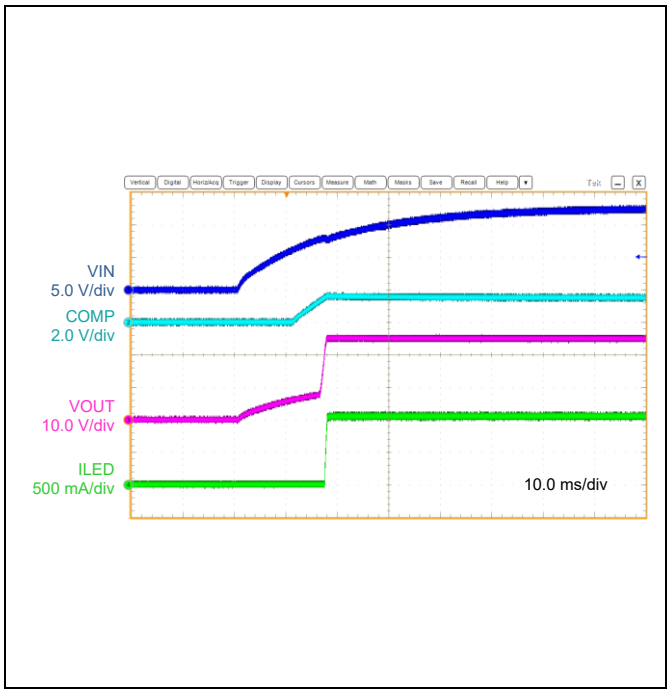

Figure 29. VIN Power ON (DRL Mode)

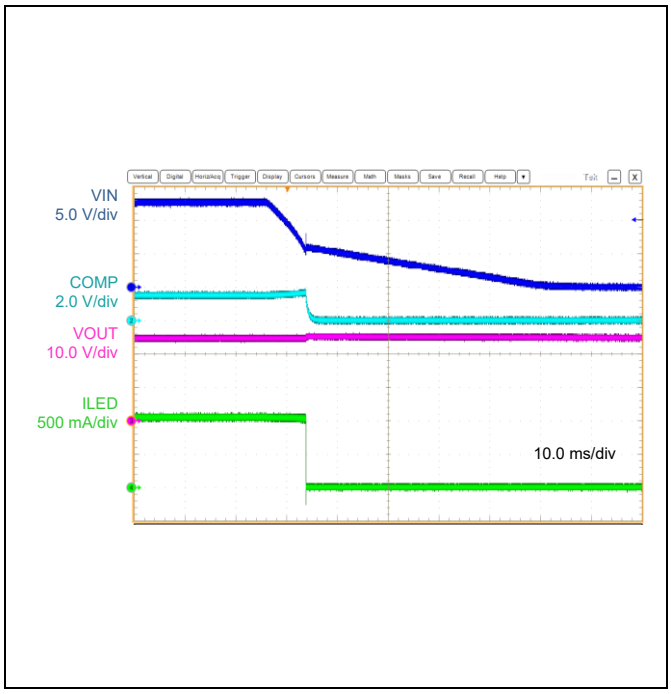

Figure 30. VIN Power OFF (DRL Mode)

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Typical Performance Curves - continued
(Application Examples 1 BOOST (Position Mode / DRL Mode))

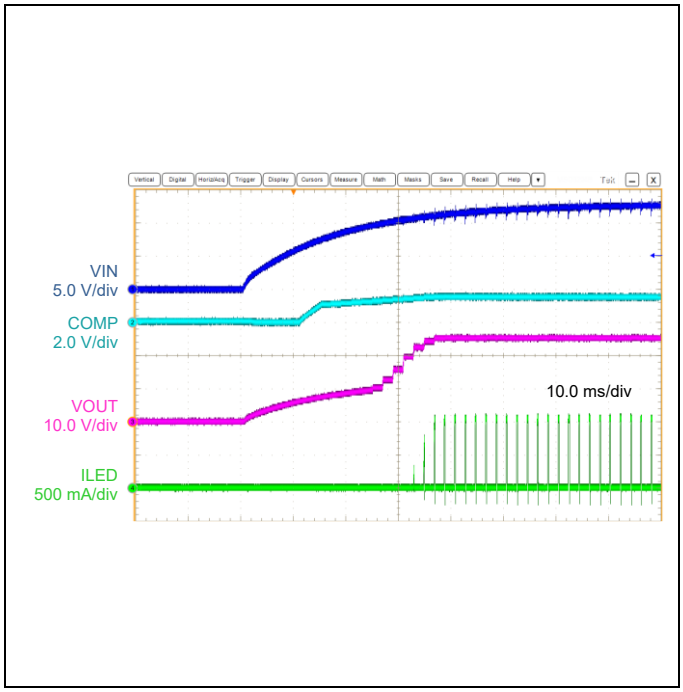

Figure 31. VIN Power ON (PWM Mode)

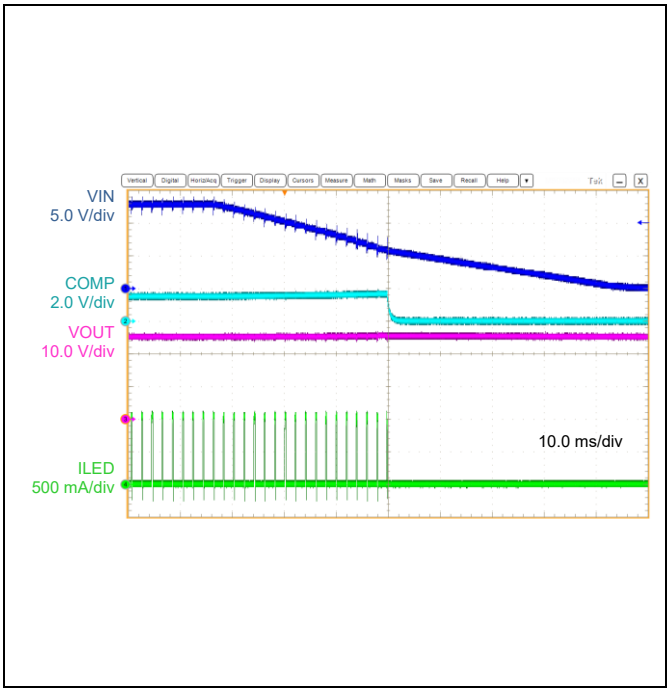

Figure 32. VIN Power OFF (PWM Mode)

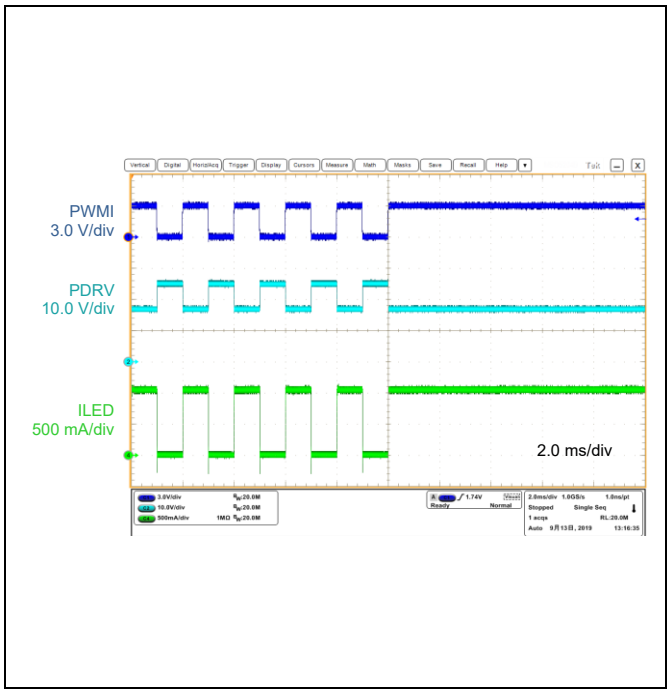

Figure 33. PWM Mode → DRL Mode

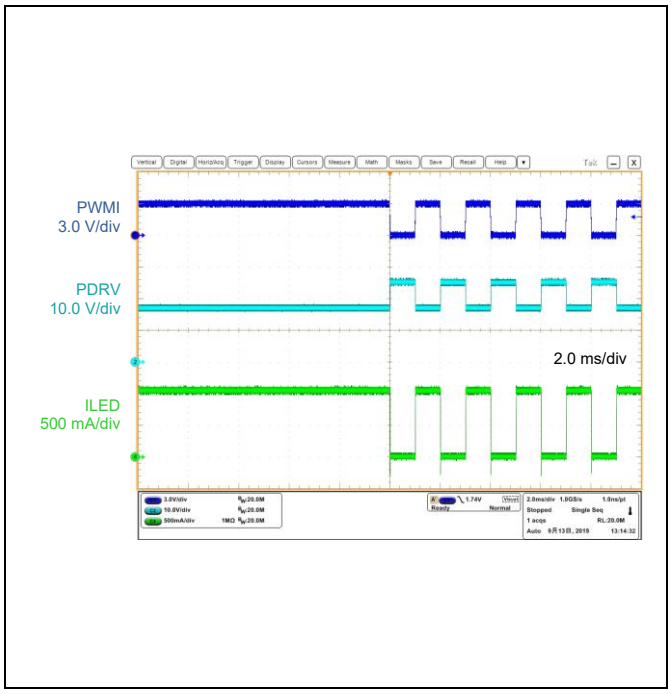

Figure 34. DRL Mode → PWM Mode

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Typical Performance Curves - continued
(Application Examples 1 BOOST (Position Mode / DRL Mode))

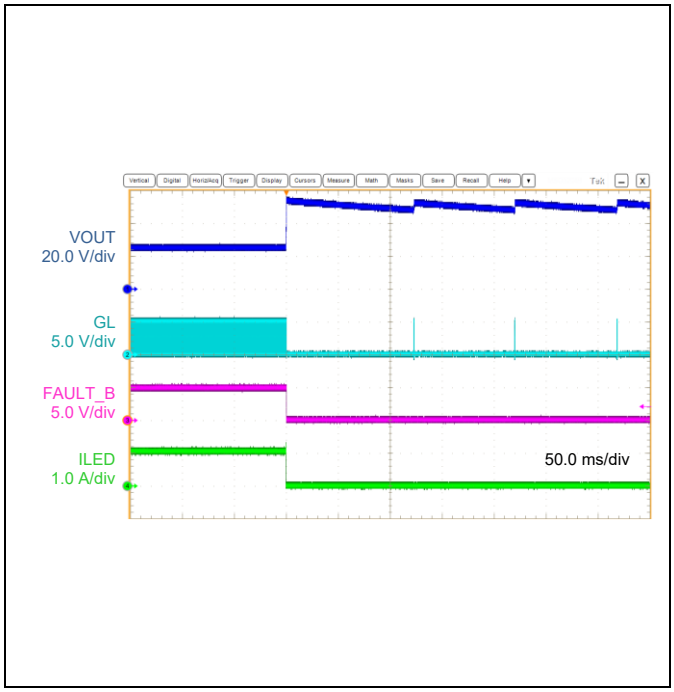

Figure 35. LED Open Operation (Normal → Open)
DRL Mode

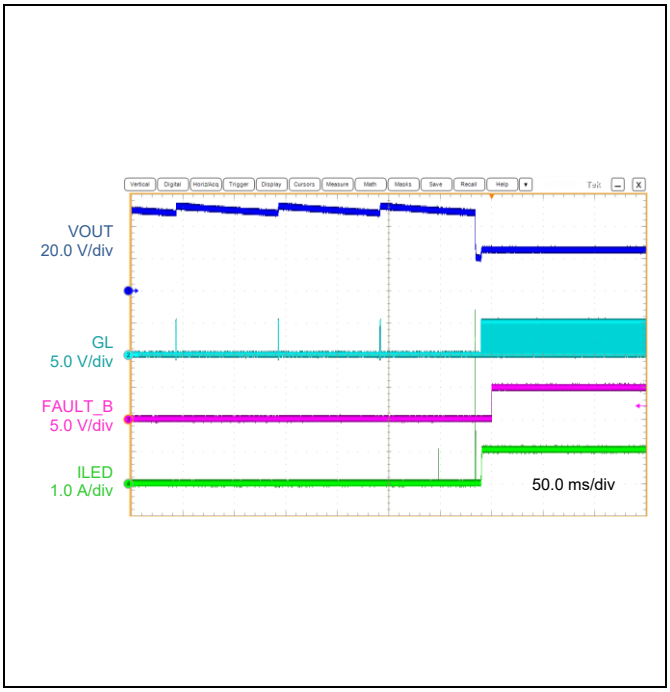

Figure 36. LED Open Operation (Open → Normal)
DRL Mode)

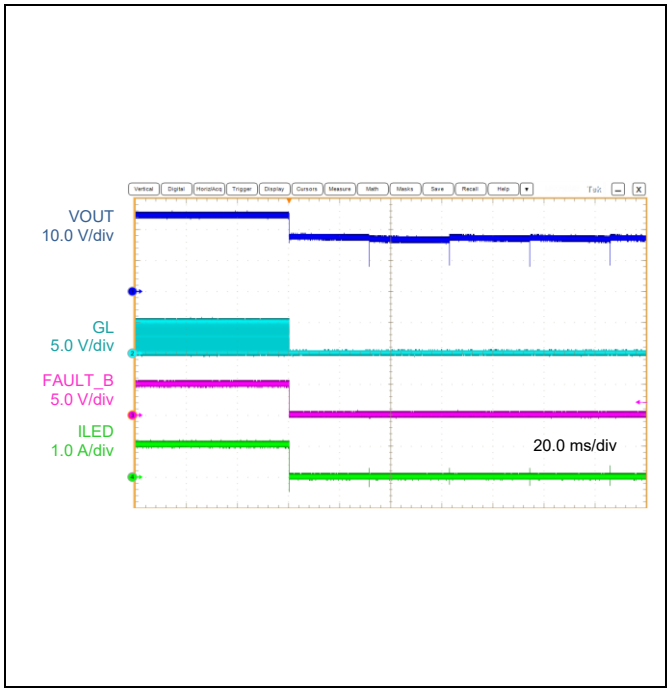

Figure 37. SCP Operation (Normal → Short)
DRL Mode

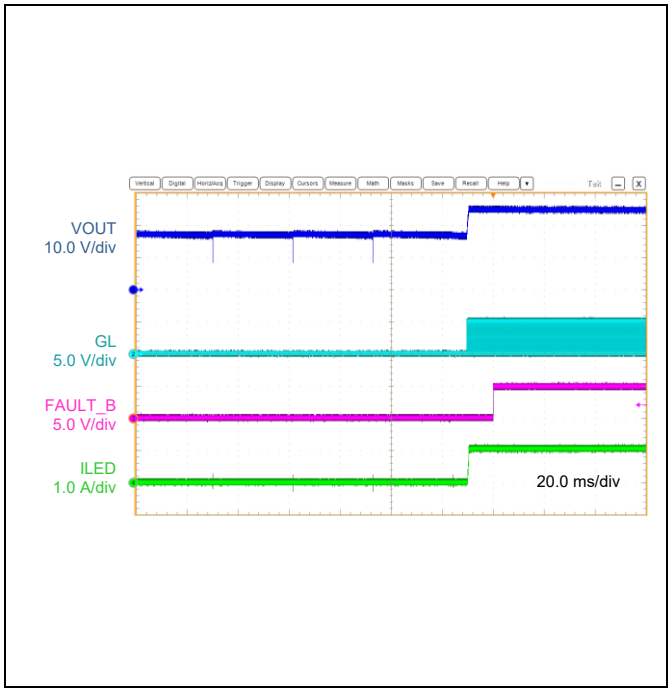

Figure 38. SCP Operation (Short → Normal)
DRL Mode

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Typical Performance Curves - continued
(Application Examples 1 BOOST (Position Mode / DRL Mode))

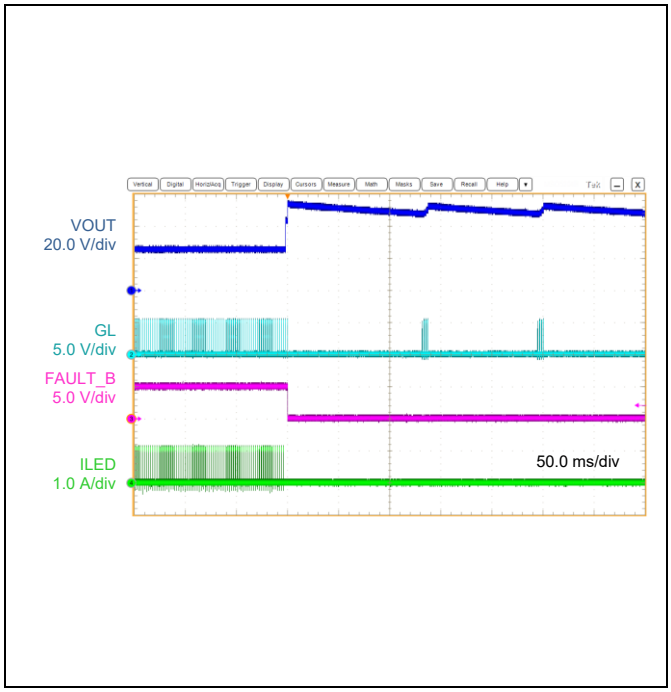

Figure 39. LED Open Operation (Normal → Open)
PWM Mode

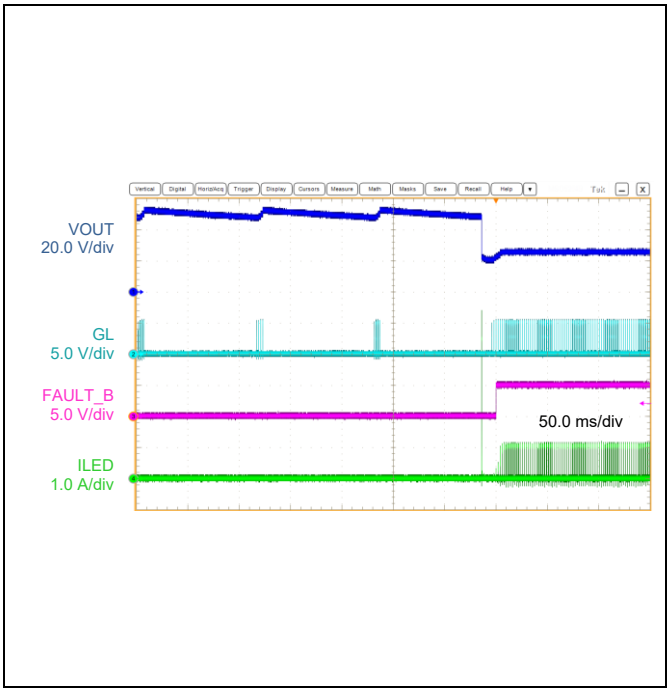

Figure 40. LED Open Operation (Open → Normal)
PWM Mode

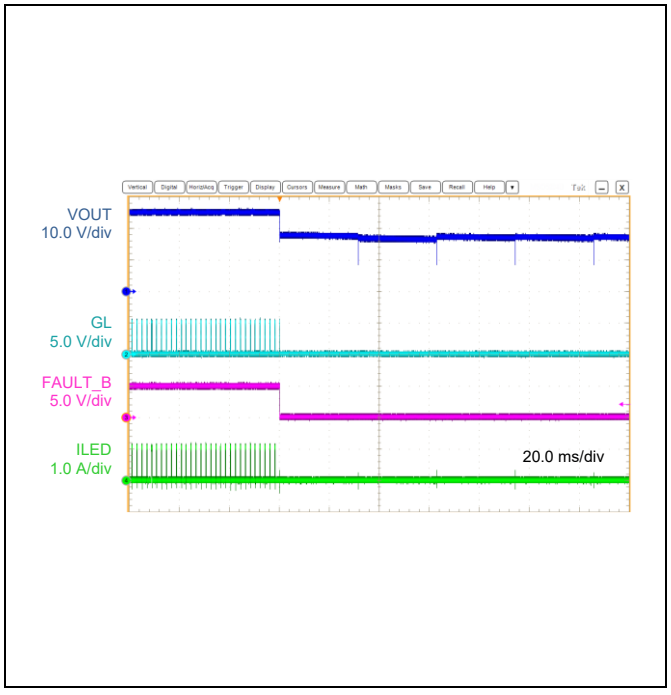

Figure 41. SCP Operation (Normal → Short)
PWM Mode

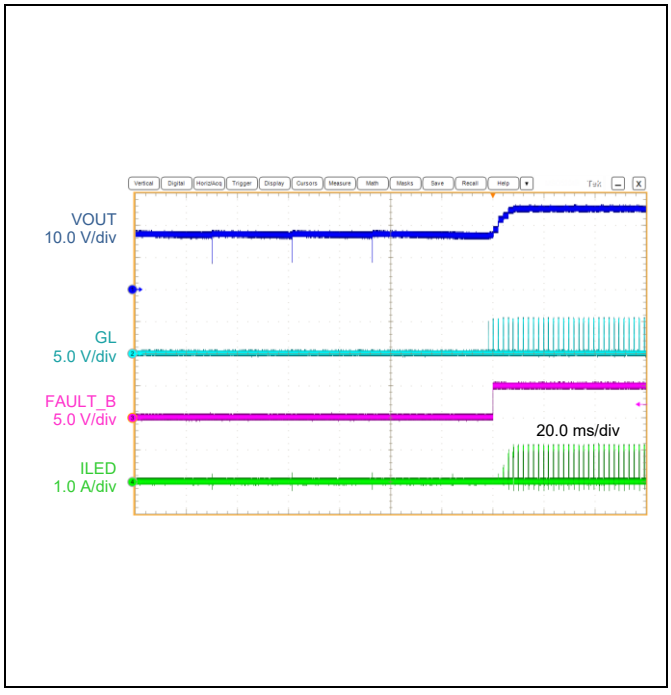

Figure 42. SCP Operation (Short → Normal)
PWM Mode

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Typical Performance Curves - continued
(Application Examples 1 BOOST (Position Mode / DRL Mode))

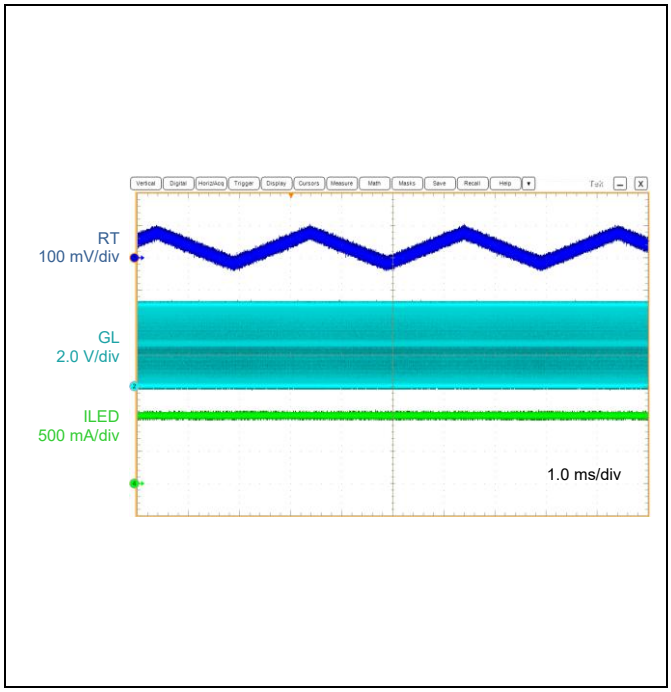

Figure 43. SSFM Operation (DRL Mode)

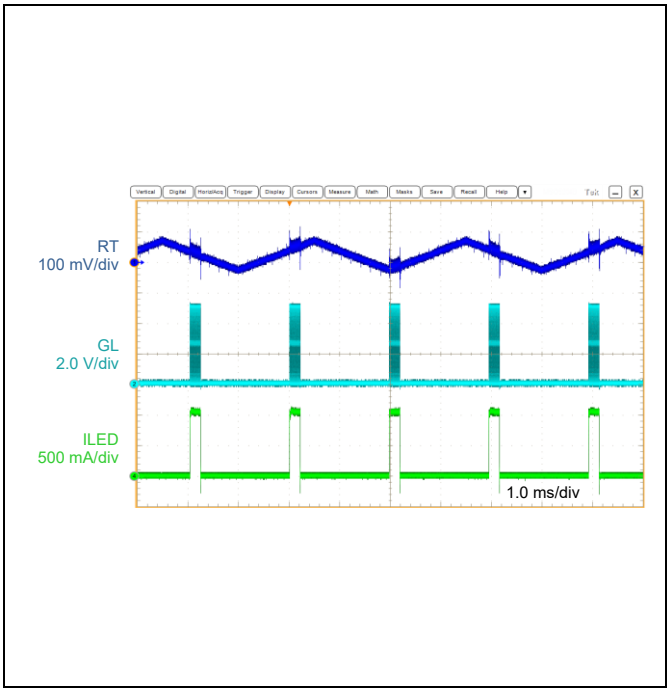

Figure 44. SSFM Operation (PWM Mode)

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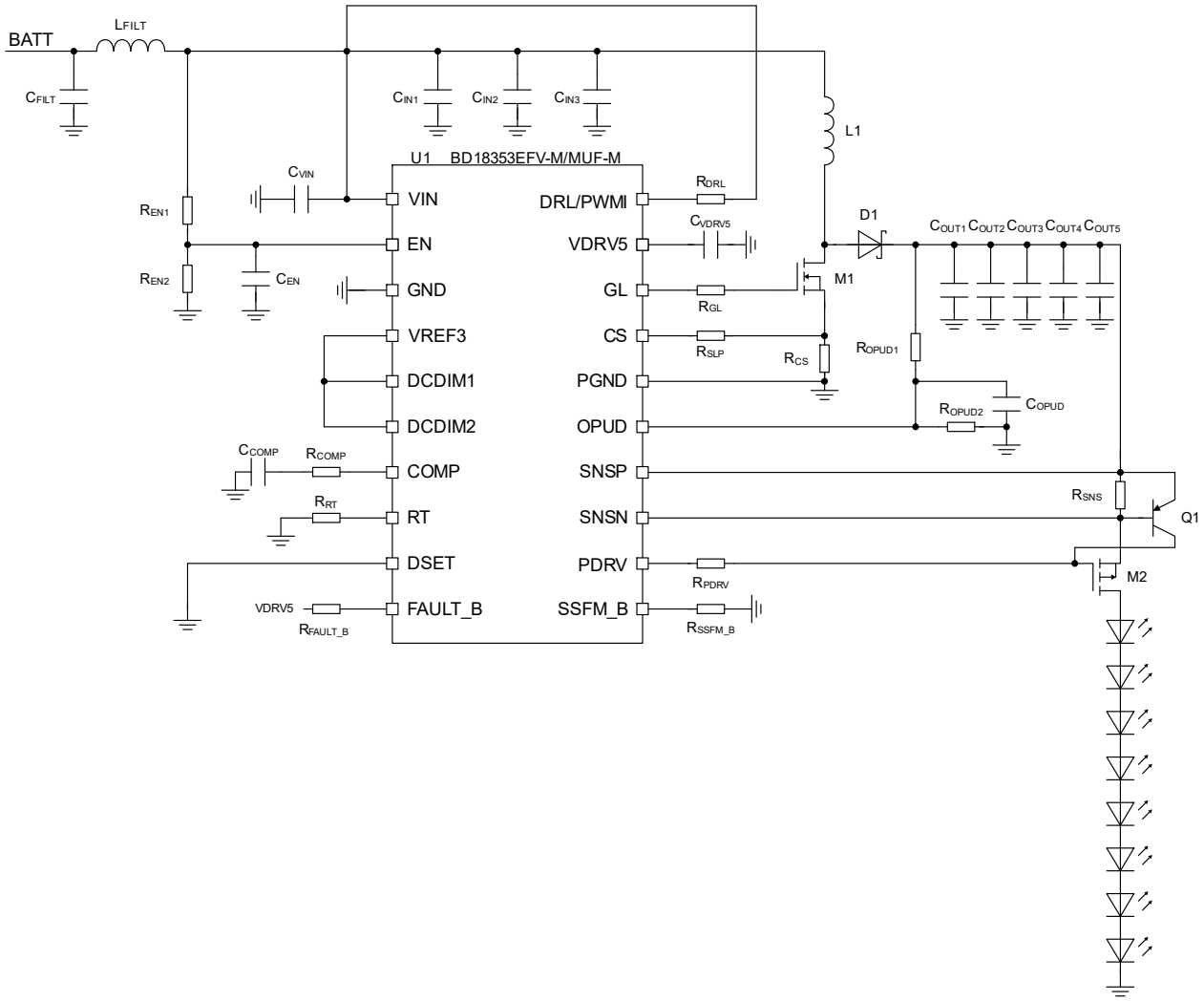
Application Examples

1 BOOST (Position Mode / DRL Mode)

BATT = 8 V to 18 V
LED = 8 series, Vf = 3.0 V (Typ), 3.5 V (Max)
LED Current = 1.04 A
VIN Enable Threshold = 6.1 V
OVP Setting Voltage = 51.9 V
DC/DC Switching Frequency = 300 kHz



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Application Examples - continued

1.1 Recommended Parts List

Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18353EFV-M/MUF-M	-	-	ROHM
Resistor	R_{EN1}	MCR03	51	kΩ	ROHM
	R_{EN2}	MCR03	10	kΩ	ROHM
	R_{DSET1}	MCR03	39	kΩ	ROHM
	R_{DSET2}	MCR03	10	kΩ	ROHM
	R_{COMP}	MCR03	33	Ω	ROHM
	R_{RT}	MCR03	33	kΩ	ROHM
	R_{FAULT_B}	MCR03	20	kΩ	ROHM
	R_{SSFM_B}	MCR03	100	kΩ	ROHM
	R_{PDRV}	MCR03	0	Ω	ROHM
	R_{SNS}	LTR18	0.16	Ω	ROHM
	R_{OPUD1}	MCR03	560	kΩ	ROHM
	R_{OPUD2}	MCR03	11	kΩ	ROHM
	R_{CS}	LTR18	0.024	Ω	ROHM
	R_{GL}	MCR03	10	Ω	ROHM
	R_{SLP}	MCR03	0	kΩ	ROHM
	R_{DRL}	MCR03	100	kΩ	ROHM
Capacitor	C_{FILT}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN1}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN2}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN3}	GCM32ER71H475KA	4.7	μF	murata
	C_{VIN}	GCM188L81H104KA	0.1	μF	murata
	C_{EN}	GCM155R71H103KA	0.01	μF	murata
	C_{COMP}	GCM21BR11E105KA	1	μF	murata
	C_{OPUD}	GCM155R72A102KA	1000	pF	murata
	C_{VDRV5}	GCM21BR71E225KA	2.2	μF	murata
	C_{OUT1}	GCJ188R72A104KA	0.1	μF	murata
	C_{OUT2}, C_{OUT3}, C_{OUT4}, C_{OUT5}	GCM32DC72A475KE	4.7	μF	murata
Inductor	L_{FILT}	CLF6045NIT-2R2N-D	2.2	μH	TDK
	L1	MSS1278-103MLB	10	μH	Coil Craft
Diode MOSFET	D1	RBQ10BM65AFHTL	-	-	ROHM
	M1	IRLR3110ZTRPBF	-	-	Infineon
MOSFET	M2	FDC3535	-	-	ON Semiconductor
Transistor	Q1	SST2907AHZG	-	-	ROHM

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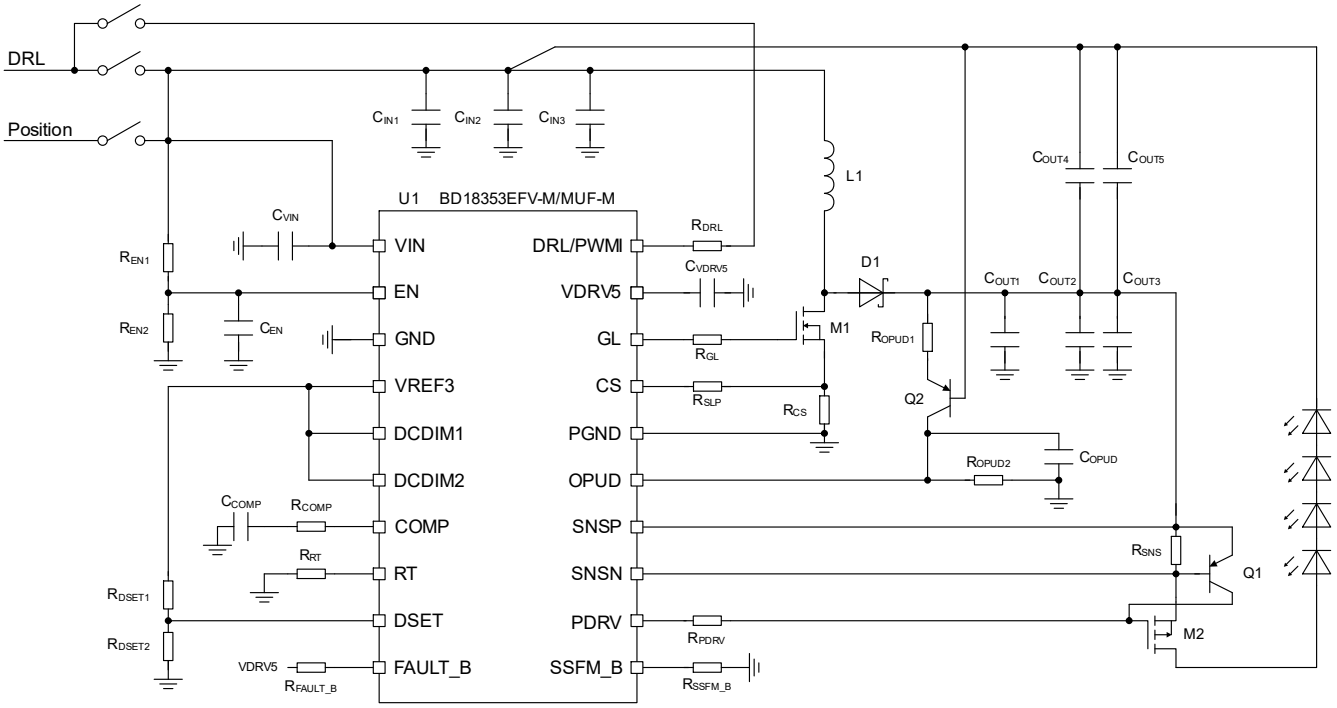
Application Examples - continued

2 BOOST to VIN (Position Mode / DRL Mode)

Position Mode
Position = 13 V
LED = 4 series, Vf = 3.0 V (Typ)
LED Current = 1.04 A
PWM Frequency = 400 Hz
PWM Dimming Duty = 10.6 %
VIN Enable Threshold = 6.1 V
OVP Setting Voltage = 51.9 V
DC/DC Switching Frequency = 412 kHz

DRL Mode
DRL = 13 V
LED = 4 series, Vf = 3.0 V (Typ)
LED Current = 1.04 A
PWM Dimming Duty = 100 %
VIN Enable Threshold = 6.1 V
OVP Setting Voltage = 51.9 V
DC/DC Switching Frequency = 412 kHz



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Application Examples - continued

2.1 Recommended Parts List

Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18353EFV-M/MUF-M	-	-	ROHM
Resistor	R_{EN1}	MCR03	51	kΩ	ROHM
	R_{EN2}	MCR03	10	kΩ	ROHM
	R_{DSET1}	MCR03	39	kΩ	ROHM
	R_{DSET2}	MCR03	10	kΩ	ROHM
	R_{COMP}	MCR03	33	Ω	ROHM
	R_{RT}	MCR03	24	kΩ	ROHM
	R_{FAULT_B}	MCR03	20	kΩ	ROHM
	R_{SSFM_B}	MCR03	100	kΩ	ROHM
	R_{PDRV}	MCR03	0	Ω	ROHM
	R_{SNS}	LTR18	0.16	Ω	ROHM
	R_{OPUD1}	MCR03	680	kΩ	ROHM
	R_{OPUD2}	MCR03	18	kΩ	ROHM
	R_{CS}	LTR18	0.024	Ω	ROHM
	R_{GL}	MCR03	10	Ω	ROHM
	R_{SLP}	MCR03	2.4	kΩ	ROHM
	R_{DRL}	MCR03	100	kΩ	ROHM
Capacitor	C_{FILT}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN1}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN2}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN3}	GCM32ER71H475KA	4.7	μF	murata
	C_{VIN}	GCM188L81H104KA	0.1	μF	murata
	C_{EN}	GCM155R71H103KA	0.01	μF	murata
	C_{COMP}	GCM21BR11E105KA	1	μF	murata
	C_{OPUD}	GCM155R72A102KA	1000	pF	murata
	C_{VDRV5}	GCM21BR71E225KA	2.2	μF	murata
	C_{OUT1}	GCJ188R72A104KA	0.1	μF	murata
	C_{OUT2}, C_{OUT3}, C_{OUT4}, C_{OUT5}	GCM32DC72A475KE	4.7	μF	murata
Inductor	L1	MSS1278-103MLB	10	μH	Coil Craft
Diode	D1	RBQ10BM65AFHTL	-	-	ROHM
MOSFET	M1	IRLR3110ZTRPBF	-	-	Infineon
	M2	FDC3535	-	-	ON Semiconductor
Transistor	Q1	SST2907AHZG	-	-	ROHM
	Q2	SST2907AHZG	-	-	ROHM

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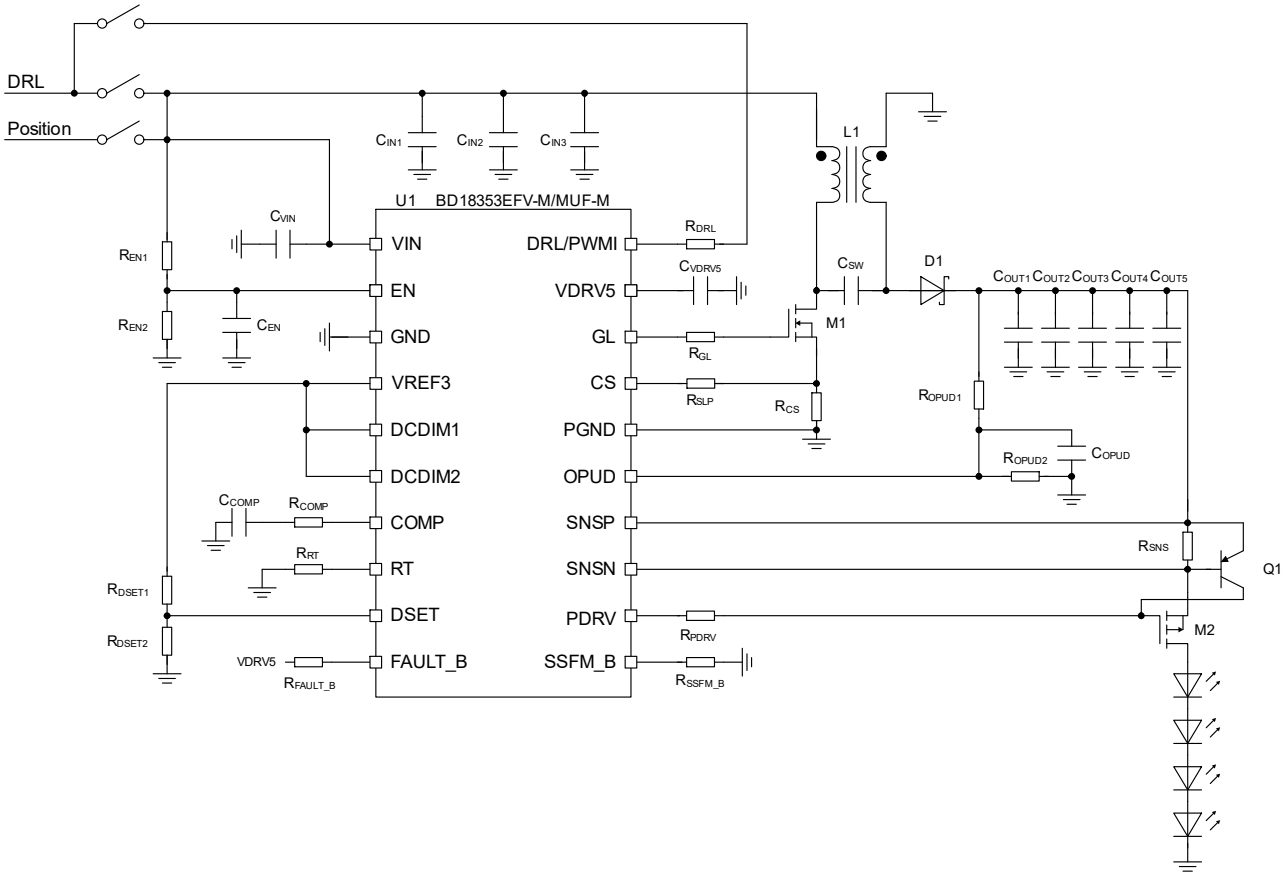
Application Examples - continued

3 SEPIC

Position Mode
Position = 13 V
LED = 4 series, Vf = 3.0 V (Typ)
LED Current = 1.04 A
PWM Frequency = 400 Hz
PWM Dimming Duty = 10.6 %
VIN Enable Threshold = 6.1 V
OVP Setting Voltage = 51.9 V
DC/DC Switching Frequency = 412 kHz

DRL Mode
DRL = 13 V
LED = 4 series, Vf = 3.0 V (Typ)
LED Current = 1.04 A
PWM Dimming Duty = 100 %
VIN Enable Threshold = 6.1 V
OVP Setting Voltage = 51.9 V
DC/DC Switching Frequency = 412 kHz



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Application Examples - continued

3.1 Recommended Parts List

Parts	Symbol	Parts Name	Value	Unit	Product Maker
IC	U1	BD18353EFV-M/MUF-M	-	-	ROHM
Resistor	R_{EN1}	MCR03	51	kΩ	ROHM
	R_{EN2}	MCR03	10	kΩ	ROHM
	R_{DSET1}	MCR03	39	kΩ	ROHM
	R_{DSET2}	MCR03	10	kΩ	ROHM
	R_{COMP}	MCR03	15	Ω	ROHM
	R_{RT}	MCR03	24	kΩ	ROHM
	R_{FAULT_B}	MCR03	20	kΩ	ROHM
	R_{SSFM_B}	MCR03	100	kΩ	ROHM
	R_{PDRV}	MCR03	0	Ω	ROHM
	R_{SNS}	LTR18	0.16	Ω	ROHM
	R_{OPUD1}	MCR03	470	kΩ	ROHM
	R_{OPUD2}	MCR03	11	kΩ	ROHM
	R_{CS}	LTR18	0.024	Ω	ROHM
	R_{GL}	MCR03	10	Ω	ROHM
	R_{SLP}	MCR03	2.4	kΩ	ROHM
	R_{DRL}	MCR03	100	kΩ	ROHM
Capacitor	C_{IN1}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN2}	GCM32ER71H475KA	4.7	μF	murata
	C_{IN3}	-	-	-	-
	C_{VIN}	-	-	-	-
	C_{EN}	GCM155R71H103KA	0.01	μF	murata
	C_{COMP}	GCM21BR11E105KA	1	μF	murata
	C_{OPUD}	GCM155R72A102KA	1000	pF	murata
	C_{VDRV5}	GCM21BR71E225KA	2.2	μF	murata
	C_{OUT1}	GCJ188R72A104KA	0.1	μF	murata
	C_{SW}	GCM32DC72A475KE	4.7 x 2	μF	murata
	C_{OUT2}, C_{OUT3}, C_{OUT4}, C_{OUT5}	GCM32DC72A475KE	4.7	μF	murata
Inductor	L1	MSD1278T-103MLB	10	μH	Coil Craft
Diode	D1	RBQ10BM65AFHTL	-	-	ROHM
MOSFET	M1	IRLR3110ZTRPBF	-	-	Infineon
	M2	FDC3535	-	-	ON Semiconductor
Transistor	Q1	SST2907AHZG	-	-	ROHM

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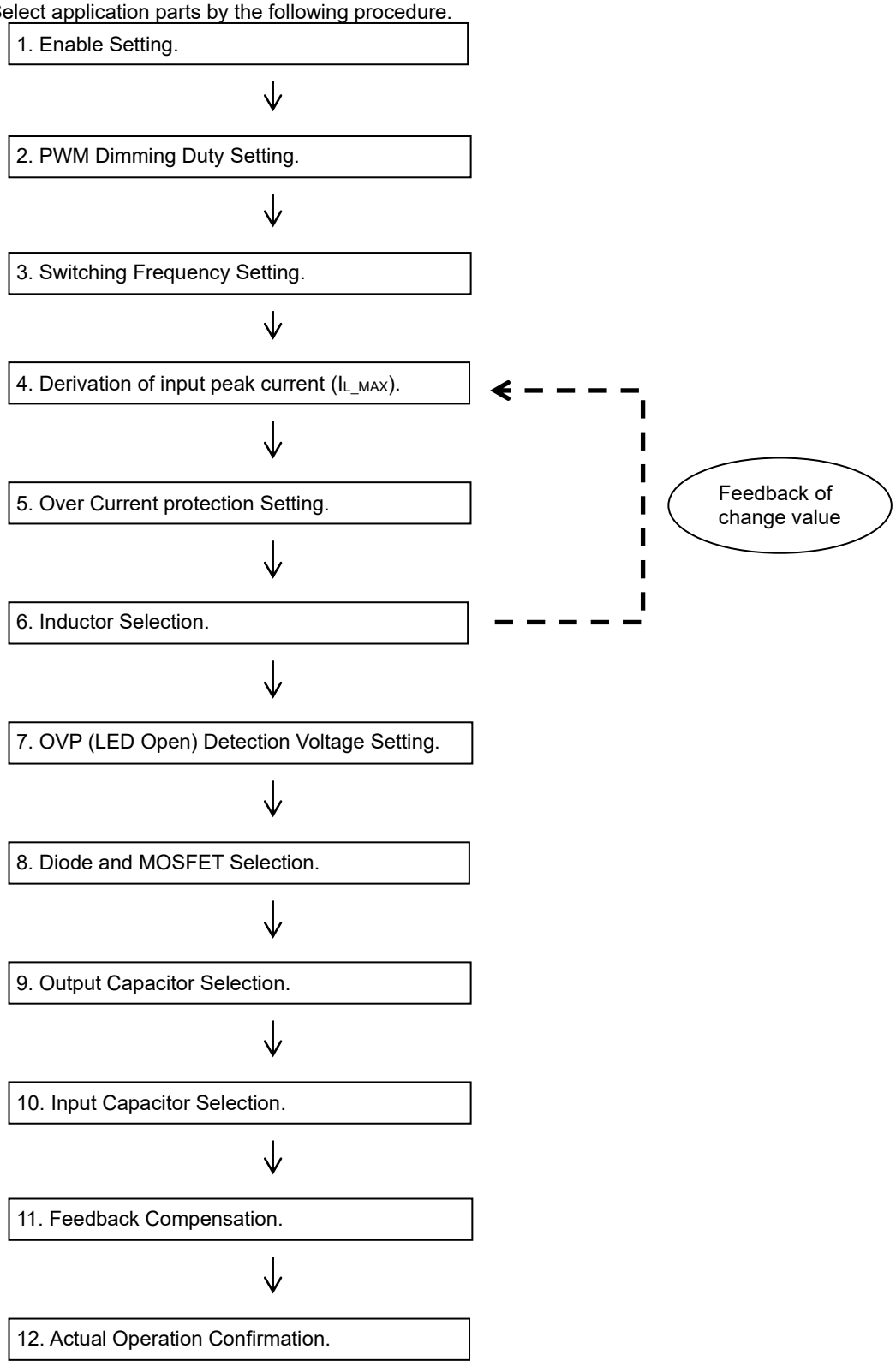
Application Parts Selection Method (Boost Mode Application)

Refer to Application Examples 1. BOOST (Position Mode / DRL Mode).

A constant setting sheet is available. Contact ROHM directly.

Select application parts by the following procedure.



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Application Parts Selection Method (Boost Mode Application) - continued

1 Enable Setting

The BD18353EFV-M/MUF-M can be ON/OFF controlled by the EN pin.
Design value: V_{INON} = 6.1 V, V_{INOFF} = 5.5 V

$$V_{INON} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times V_{ENIH} = \frac{(51\ k\Omega + 10\ k\Omega)}{10\ k\Omega} \times 1.0 = 6.1 \quad [V]$$

$$V_{INOFF} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times V_{ENIL} = \frac{(51\ k\Omega + 10\ k\Omega)}{10\ k\Omega} \times 0.9 = 5.49 \quad [V]$$

2 PWM Dimming Setting (Internal PWM Dimming Signal Generator)

The BD18353EFV-M/MUF-M has a built-in PWM dimming pulse generation circuit. Set the duty with the built-in ramp waveform and the voltage input to the DSET pin. The DSET pin voltage is set from the VREF3 pin by resistance voltage division.
Design value: PWM Dimming Duty (D_{PWM}) = 10.6 %

$$D_{PWM} = \frac{V_{REF3} \times \frac{R_{DSET2}}{R_{DSET1} + R_{DSET2}} - V_{RAMPB}}{V_{RAMPP} - V_{RAMPB}} \times 100$$

$$= \frac{3.00 \times \frac{10\ k\Omega}{39\ k\Omega + 10\ k\Omega} - 0.40}{2.40 - 0.40} \times 100 = 10.6 \quad [\%]$$

3 Switching Frequency Setting

The switching frequency of the DC/DC can be set by the resistor R_{RT} connected to the RT pin.
Design value: Switching Frequency = 300 kHz

$$f_{SW1} \fallingdotseq \frac{9900}{R_{RT}} \times 10^3 = \frac{9900}{33\ k\Omega} \times 10^3 = 300 \quad [kHz]$$

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Application Parts Selection Method (Boost Mode Application) - continued

4 Derivation of Input Peak Current I_{L_MAX} (V_{DCDIM1} > 2.5 V, V_{DCDIM2} > 2.5 V)

4.1 Calculation of Output Voltage (V_{OUT})

BOOST Setting:

$$V_{OUT} = V_{f_LED} \times N + V_{SNS_100\,\%} + R_{ON_PWMFET} \times I_{LED}$$

$$= 3 \times 8 + 0.1667 + 0.2 \times 1 \approx 24.4 \quad [V]$$

Where:

V_{f_LED}	is the Vf of LED (Typ: 3.0 V, Max: 3.5 V).
N	is the number of series LED.
R_{ON_PWMFET}	is the ON resistance of MOSFET for PWM Dimming. (M1)
I_{LED}	is the output LED current.

4.2 Calculation of DC/DC Switching Duty (D_{SW})

$$D_{SW} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} = \frac{24\,V - 13\,V}{24\,V} \approx 0.458$$

4.3 Calculation of Output Current (I_{LED})

$$I_{LED} = \frac{V_{SNS_100\,\%}}{R_{SNS}} = \frac{0.1667}{0.16} \approx 1.04 \quad [A]$$

4.4 Calculation of Input Peak Current (I_{L_MAX})

$$I_{L_MAX} = I_{L_AVE_MAX} + \frac{1}{2}\Delta I_{L_MAX} = 3.90 + 1.30 = 5.2 \quad [A]$$

$$I_{L_MIN} = I_{L_AVE_MIN} - \frac{1}{2}\Delta I_{L_{MAX}} = 1.48 - 1.30 = 0.18 \quad [A]$$

$$I_{L_AVE_MAX} = \frac{V_{OUT_MAX} \times I_{LED}}{\eta \times V_{IN_MIN}} = \frac{28\,V \times 1\,A}{0.9 \times 8} \approx 3.90 \quad [A]$$

$$I_{L_AVE_MIN} = \frac{V_{OUT_MIN} \times I_{LED}}{\eta \times V_{IN_MAX}} = \frac{24\,V \times 1\,A}{0.9 \times 18} \approx 1.48 \quad [A]$$

$$\Delta I_{L_MAX} = \frac{V_{IN}}{L} \times \frac{(V_{OUT} - V_{IN})}{V_{OUT}} \times \frac{1}{f_{SW_MIN}}$$

$$= \frac{14\,V}{10\,\mu H} \times \frac{(28\,V - 14\,V)}{28\,V} \times \frac{1}{270\,kHz} \approx 2.59 \quad [A]$$

Where:

I_{L_MAX}	is the maximum inductor current.
I_{L_MIN}	is the minimum inductor current.
I_{L_AVE}	is the mean inductor current.
$I_{L_AVE_MAX}$	is the maximum mean inductor current.
$I_{L_AVE_MIN}$	is the minimum mean inductor current.
ΔI_{L_AVE}	is the maximum inductor ripple current.
η	is the Efficiency.
f_{SW_MIN}	is the minimum switching frequency.

- Assign minimum input voltage for calculation.
- BD18353EFV-M/MUF-M adopts current mode DC/DC converter control. When I_{L_MIN} is positive, it becomes to be in the consecutive modes, and it will be in the discontinuity mode when I_{L_MIN} is negative. Feedback characteristics are easy to become insufficient in the discontinuous mode, and responsiveness turns worse, and a switching waveform pattern becomes irregular, and stability is easy to turn worse. Therefore it is sufficient validation of feedback characteristics are recommended.
- η (efficiency) is calculated as 90 %.
- In the case of V_{DCDIM1} ≤ 2.5 V or V_{DCDIM2} ≤ 2.5 V, calculate I_{LED} with reference to Description of Blocks 5 Analog Dimming (DCDIM).

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Application Parts Selection Method (Boost Mode Application) - continued

5 Over Current Protection Setting

Select R_{CS} (resistance for over current detection) to realize below.
Design value: Over current detection = 12.5 A

$$I_{OCP_MIN} = \frac{V_{CSOCP_MIN}}{R_{CS}} > I_{L_MAX} \quad [A]$$

$$I_{OCP_MIN} = \frac{V_{CSOCP_MIN}}{R_{CS}} = \frac{0.275}{0.024} \approx 11.46 > 5.2 \quad [A]$$

Where:
I_{OCP_MIN} is the minimum over current detection current.
V_{CSOCP_MIN} is the minimum over current detection voltage.

Set a sufficient margin in consideration of the variation of the inductor.

6 Inductor Selection

For the purpose of stabilizing current mode DC/DC converter operation, adjustment of L value within the following condition is recommended.
Design value: R_{SLP} = 0.0 kΩ

$$L > \frac{(V_{OUT} - V_{IN}) \times R_{CS} \times R_{RT} \times 1.5 \times 10^{-6}}{4\ k + R_{SLP}}$$

$$L > \frac{(28 - 8) \times 24.24\ m \times 33.33\ k \times 1.5 \times 10^{-6}}{4\ k} \approx 6 \quad [\mu H]$$

Design value: R_{SLP} = 1.2 kΩ

$$L > \frac{(28 - 8) \times 24.24\ m \times 33.33\ k \times 1.5 \times 10^{-6}}{4\ k + 1.2\ k} \approx 4.7 \quad [\mu H]$$

Reduction of calculated value will increase stability, but may reduce responsiveness such as power voltage variation. If the above formula is not satisfied, the switching becomes unstable due to sub-harmonic oscillation, and the LED may flicker. The condition can be eased by adding R_{SLP}. However, be aware that adding R_{SLP} will also change OCP detection (I_{OCP}) level. The formula for calculating the OCP detection level (I_{OCP}) when R_{SLP} is added is as follows.
Design value: R_{SLP} = 1.2 kΩ

$$I_{OCP_MIN} = \frac{\left(V_{CSOCP_MIN} - \frac{1.06}{R_{RT} \times 1.2 \times 10^{-6}} \times \frac{D_{SW_MAX}}{f_{SW_MIN}} \times R_{SLP}\right)}{R_{CS}} > I_{L_MAX} \quad [A]$$

$$I_{OCP_MIN} = \frac{\left(0.275 - \frac{1.06}{33\ k \times 1.2 \times 10^{-6}} \times \frac{0.72}{270\ k} \times 1.2\ k\right)}{0.024} \approx 7.89 > I_{L_MAX} \quad [A]$$

Where:
D_{SW_MAX} is the maximum DC/DC switching duty.
f_{SW_MIN} is the minimum switching frequency.
I_{L_MAX} is the maximum inductor current.

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Application Parts Selection Method (Boost Mode Application) - continued

7 OVP (LED Open) Detection Voltage Setting

LED open detection voltage needs higher voltage setting than overshoot of output voltage at start up to avoid start up failure. Further, output voltage at the time of LED open detection (V_{OUT_OVP}) is calculable as shown below by setting R_{OPUD1} and R_{OPUD2}.
Design value: Over voltage detection = 51.9 V

$$V_{OUT_OVP} = \frac{R_{OPUD1} + R_{OPUD2}}{R_{OPUD2}} \times V_{OVP}$$

$$= \frac{560\ k + 11\ k}{11\ k} \times 1.0\ V \approx 51.9\ (Typ) \quad [V]$$

Where:
V_{OUT_OVP} is the OVP (LED Open) Detection Voltage.

R_{OPUD1}, R_{OPUD2} resistor will be the current discharge path for the output capacitor when PWM = Low.
Improperly the resistor value can increase VOUT ripple and cause the LED to flicker. Therefore, R_{OPUD1} should be selected within the Recommended Setting Parts Range.
Sufficient verification for LED flickering is required with actual application as behavior differs by characteristic of output capacitor and LED. (V_{OUT} drop can be prevented by inserting bigger output capacitor or ODT resistance.)

8 Diode and MOSFET Selection

Selection of MOSFET M1
Select a MOSFET (M1) whose VDS rating is higher than the maximum voltage for OVP (LED open) detection.

$$M1\ V_{DS} > V_{OUT_OVP_MAX} = \frac{R_{OPUD1} + R_{OPUD2}}{R_{OPUD2}} \times V_{OVP_MAX}$$

$$= \frac{560\ k + 11\ k}{11\ k} \times 1.04\ V \approx 54\ (Max) \quad [V]$$

Where:
$M1\ V_{DS}$ is the maximum rating voltage between drain and source of M1.
$V_{OUT_OVP_MAX}$ is the maximum over voltage detection voltage.

The RMS current rating (I_{DS_RMS}) flowing between the drain - source of M1 can be calculated as follows.

$$I_{DS_RMS} = 1.3 \times \sqrt{(I_{L_AVE})\text{^}2 \times D_{SW}}$$

Where:
I_{L_AVE} is the mean inductor current.
D_{SW} is the Switching Duty.

A loss of M1 is calculated next. The loss of M1 has Switching loss P_{LOSS1} and M1 On resistance loss P_{LOSS2}. Switching loss P_{LOSS1} and M1 On resistance loss P_{LOSS2} can be calculated as follows.

$$P_{LOSS1} = \frac{(t_R + t_F)}{2} \times f_{SW} \times (V_{OUT} + V_{D1}) \times I_{L_AVE}$$

$$P_{LOSS2} = {I_{L_AVE}}^2 \times R_{ON} \times D_{SW}$$

Where:
t_R is the rise time of M1 drain-source.
t_F is the fall time of M1 drain-source.
V_{D1} is the forward voltage of D1.
R_{ON} is the ON resistance of M1.

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8 Diode and MOSFET Selection - continued

Selection of rectifier diode D1

For power consumption reduction, use a Schottky Barrier diode for rectification diode D1. The withstand voltage rating of the diode shall be higher than the OVP (LED Open) detection voltage. In addition, Schottky Barrier diode with low leakage current shall be selected if PWM dimming is used. Because the leakage current increases with higher temperature environment, the output capacitor can be discharged in PWM = Low which may result that LED current will be unstable. The current limit of D1 can be calculated in following formula.

$$I_{D1} = I_{L_AVE} \times (1 - D_{SW})$$

Where:
I_{L_AVE} is the mean inductor current.
D_{SW} is the DC/DC switching duty.

Selection of MOSFET M2

Consider margin and set the rated voltage rather higher than the actual usage condition for LED current and output voltage.

Selection of transistor Q1 for current clamp

It is recommended to insert Q1 to control the flow of excessive large current at the time of anode ground fault. By inserting Q1, the set current is clamped by the Vf of Q1, so the withstand current of M2 can be suppressed.
For example, when Vf = 0.5 V, the current is clamped at about 3 times the set current. Select the Vce of Q1 that satisfies the following formula.

$$V_{CE} > V_{OUT_OVP_MAX}$$

Also, select in consideration of hfe, speed and saturation voltage.

9 Output Capacitor Selection

Output capacity includes two purposes. The first is to reduce output ripple. The second is to supply current to LED when MOSFET (D1) is switched on. The output voltage ripple is influenced by both bulk capacity and ESR. (When a ceramic capacitor is used, most of the ripple caused by bulk capacity.) Bulk capacity and the ESR can be calculated in lower formula.

$$C_{OUT} \geq I_{LED} \times \frac{D_{SW_MAX}}{\Delta V_{COUT} \times f_{SW_MIN}}$$

$$R_{ESR} < \frac{\Delta V_{ESR}}{I_{L_MAX}}$$

Where:
ΔV_{COUT} is the influence with the capacitor among output ripple.
ΔV_{ESR} is the ripple which occurs in the ESR of the output capacitor.
f_{SW_MIN} is the minimum switching frequency.

The total output ripple permitted here can be expressed as product of LED current ripple and the equivalent resistance of the LED. This equivalent resistance is defined as "ΔV / ΔI of the LED current", and it is necessary to calculate from I-V properties in the data sheet of the selected LED. When the application condition is the number of the driven LED = 8 pcs (equivalent resistance 0.2 Ω / LED), LED current = 1 A (I_{L_MAX} = 5.2 A), switching duty = 72 %(V_{IN} = 8 V, V_{OUT} = 28 V) , switching frequency = 300 kHz, LED current ripple = 5%. Then the total output ripple can be calculated as follows.

$$V_{OUT_RIPPLE} = 1\,A \times 5\,\% \times (0.2\,\Omega \times 8) = 80 \quad \text{[mV]}$$

Where:
V_{OUT_RIPPLE} is the V_{OUT} ripple voltage.

If bulk capacity causes 95 % among total output ripple, the output capacitor is calculated as follows.

$$C_{OUT} \geq 1 \times \frac{0.72}{0.08 \times 0.95} \times \frac{1}{300\,kHz} \approx 31.6 \quad \text{[µF]}$$

$$R_{ESR} < \frac{V_{OUT_RIPPLE}}{I_{L_MAX}} = \frac{0.08}{5.2} \approx 15.38 \quad \text{[mΩ]}$$

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9 Output Capacitor Selection - continued

However the capacitance of output capacitor mentioned above is minimum capacitance. Therefore select parts considering the tolerance of the capacitor and DC bias properties. Furthermore, because small external part connected to output may lead to bigger ripple on output voltage, which may result in LED flickering, sufficient verification of the actual application is required. Increase output capacitors if judged to be required from the verification. In addition, an acoustic noise may be produced by the piezoelectric effect of the ceramic capacitor during PWM dimming. Low ESR electrolytic capacitor used together with a ceramic capacitor may reduce this noise. But capacitance may largely decrease with a change of the voltage with the ceramic capacitor and may not accord with the numerical value calculated from theory.

10 Input Capacitor Selection

In DC/DC converter, since peak current flows between input and output, a capacitor is also required in the input side. Therefore, low ESR capacitors with capacitor of 10 μF or more and ESR component of 100 mΩ or less are recommended as input capacitors. If a capacitor out of the range is selected, an excessive ripple voltage may be superimposed on the input voltage and the LSI may malfunction.

$$C_{IN} \geq \frac{\Delta I_L}{8 \times V_{IN_RIPPLE} \times f_{SW}}$$

Where:
V_{IN_RIPPLE} is the V_{IN} ripple voltage.

11 Feedback Compensation

- ●Concerning stability condition of application.
  Stability condition for system with negative feedback is as shown below.
  Phase-lag when gain is 1 (0 dB) is no more than 150 ° (namely, phase margin is 30 ° or more).
  Further, since DC/DC converter application is sampled by switching frequency, GBW of the entire system is set to be 1 / 10 or less of switching frequency. To wrap up, target characteristics of application are as shown below.
- ●Phase-lag when gain is 1 (0 dB) is 150 ° or less (namely, phase margin is 30 ° or more).
- ●GBW at the time (namely, frequency when gain is 0 dB) is 1/10 or less of switching frequency. Therefore, in order to raise responsiveness by limiting GBW, higher switching frequency is required.
- ●Phase margin: 60 ° or more
- ●GBW: 1/20 or less of switching frequency.
  is recommended.

The knack for securing stability feedback compensation is to insert phase-lead f_{Z1} near GBW. GBW is determined by C_{OUT} and phase-lag f_P due to output impedance R_L (= V_{OUT} / I_{LED}).
They are shown in the following formulae.

Phase-lead

$$f_{Z1} = \frac{1}{2\pi \times C_{COMP} \times R_{COMP}}$$

Phase-lag

$$f_P = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

$$R_L = \frac{V_{OUT}}{I_{LED}}$$

As described above, secure phase margin. For R_L value at max load should be inserted. In addition, with boost DC/DC, right half plane zero (RHP zero) is to be considered. This zero has a characteristic of zero as a gain and as the pole with phase. Because it causes an oscillation when this zero effects on a control loop, it is necessary to bring GBW just before RHP zero. RHP zero f_{Z2} can be calculated with an equation below and shows good characteristic by setting GBW to be lower than 1/10 of RHP zero or less.

$$f_{Z2} = \frac{R_L \times (\frac{V_{IN}}{V_{OUT}})^2}{2\pi \times L}$$

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11 Feedback Compensation - continued

Particularly when supply voltage rises and gets close to output voltage, the switching output becomes irregular and ripple of the output voltage increases. Ripple of the LED current may thereby get bigger.

Since this setting is obtained by simplified, not strict, calculation, adjustment by actual equipment may be required in some cases.
Further, since these characteristics will vary depending upon substrate layout, load condition, etc., confirm satisfactorily with actual equipment when planning mass production.

12 Actual Operation Confirmation

Select external parts based on verification with actual equipment since characteristics will vary depending on various factors such as load current, input voltage, output voltage, inductor value, load capacity, switching frequency and mounting pattern.

About the attention point at the time of the PCB layout

1. Locate the decoupling capacitor of C_{VIN}, C_{VDRV5} close to an LSI pin as much as possible.
2. R_{RT} locates it close to the RT pin, and prevent there from being capacity.
3. Because high current may flow in PGND, lower impedance.
4. Prevent noise to be applied to the EN, VREF3, COMP, RT, DCDIM1, DCDIM2, DSET, OPUD, SNSP and SNSN pins.
5. As the GL, CS, PDRV pins are switching, be careful not to affect the neighboring patterns.
6. There is EXP-PAD on the back side of the package.
7. For noise reduction, PGND of R_{CS} and PGND of C_{OUT} recommend to have one common grounds. In addition, consider the PCB layout so that the current path of M1 → R_{CS}, R_{CS} → PGND and the current path of M1 → D1 → C_{OUT} → PGND are the shortest and with the lowest impedance on the same surface without vias etc.

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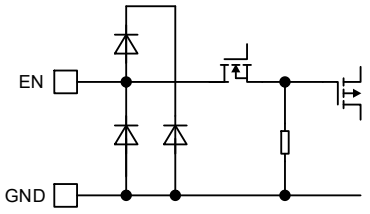
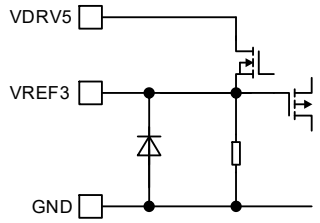
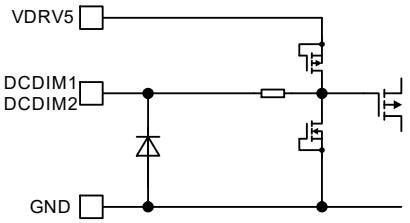
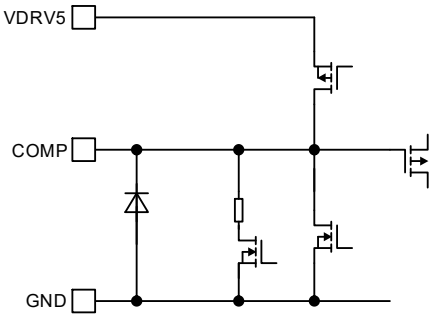
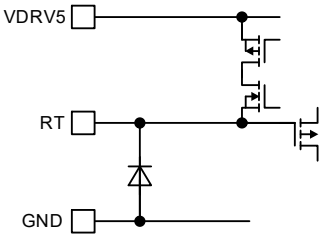
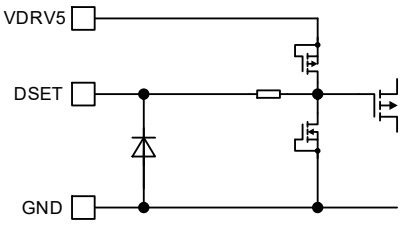
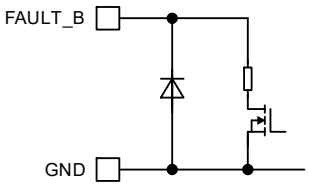
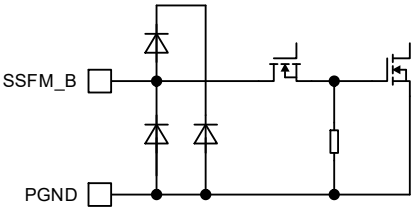
I/O Equivalence Circuits

Pin No.	Pin Name	I/O Equivalence Circuit	Pin No.	Pin Name	I/O Equivalence Circuit
2 (20)	EN		4 (2)	VREF3	
5 (3)	DCDIM1		7 (5)	COMP	
6 (4)	DCDIM2				
8 (6)	RT		9 (7)	DSET	
10 (8)	FAULT_ B		11 (9)	SSFM_B	

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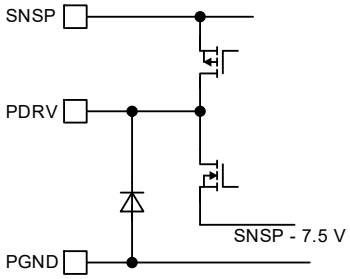
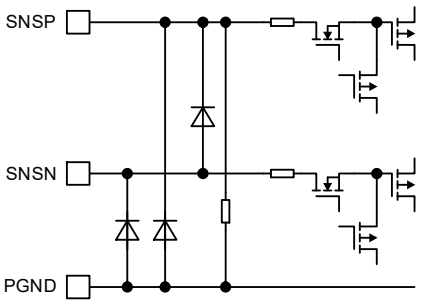
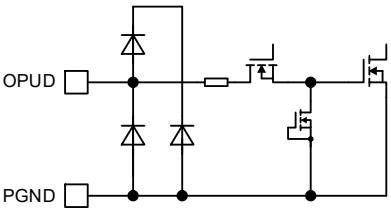
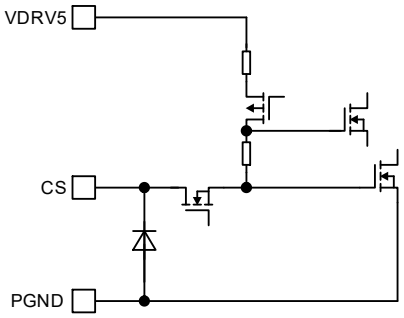
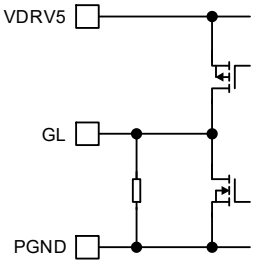
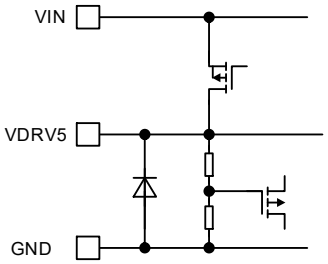
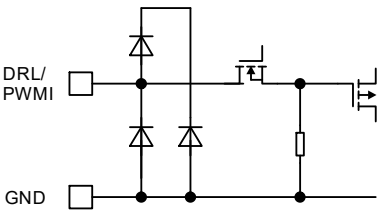
I/O Equivalence Circuits- continued

Pin No.	Pin Name	I/O Equivalence Circuit	Pin No.	Pin Name	I/O Equivalence Circuit
12 (10)	PDRV		13 (11)	SNSN	
			14 (12)	SNSP	
15 (13)	OPUD		17 (15)	CS	
18 (16)	GL		19 (17)	VDRV5	
20 (18)	DRL/ PWMI				

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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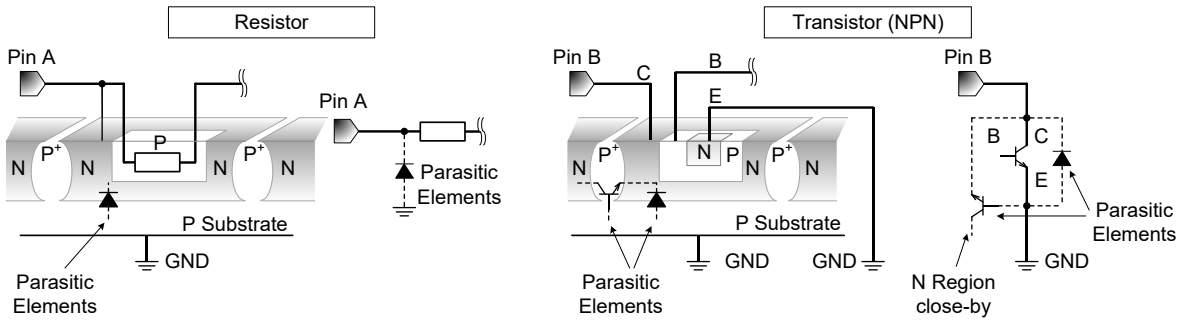
Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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Ordering Information

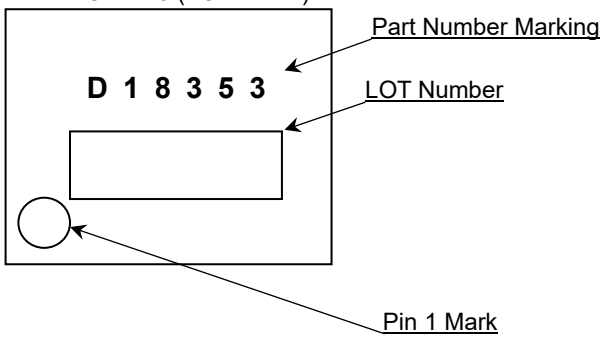
B	D	1	8	3	5	3	x	x	x	-	M E 2

Package
EFV: HTSSOP-B20
MUF: VQFN20FV3535

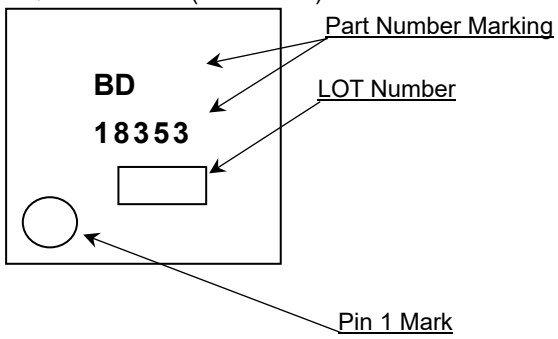
Product Rank
M: for Automotive
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagrams

HTSSOP-B20 (TOP VIEW)



VQFN20FV3535 (TOP VIEW)



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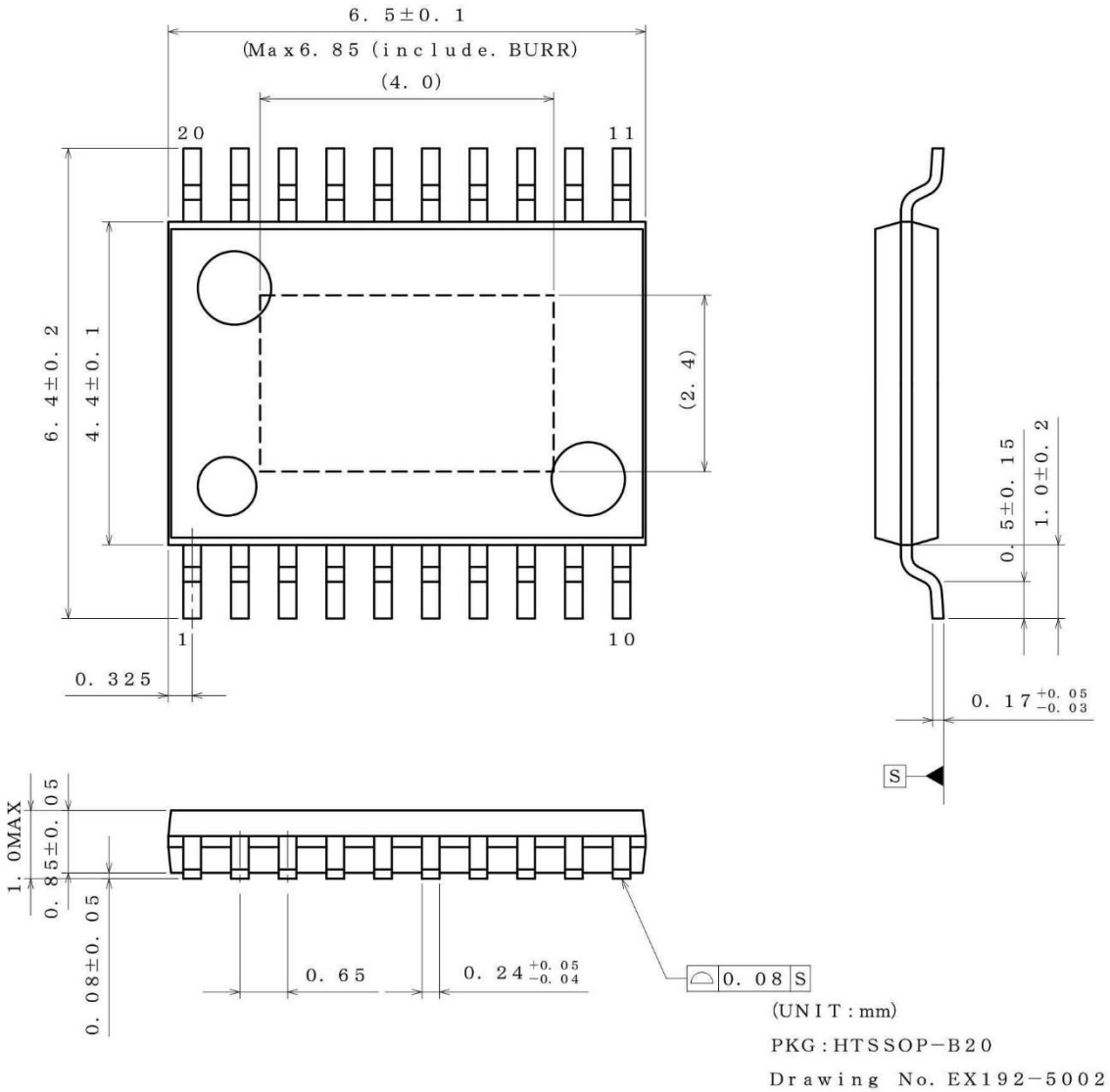
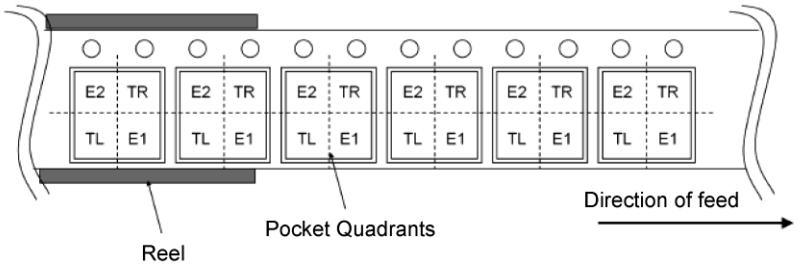
Physical Dimension and Packing Information

Package Name	HTSSOP-B20



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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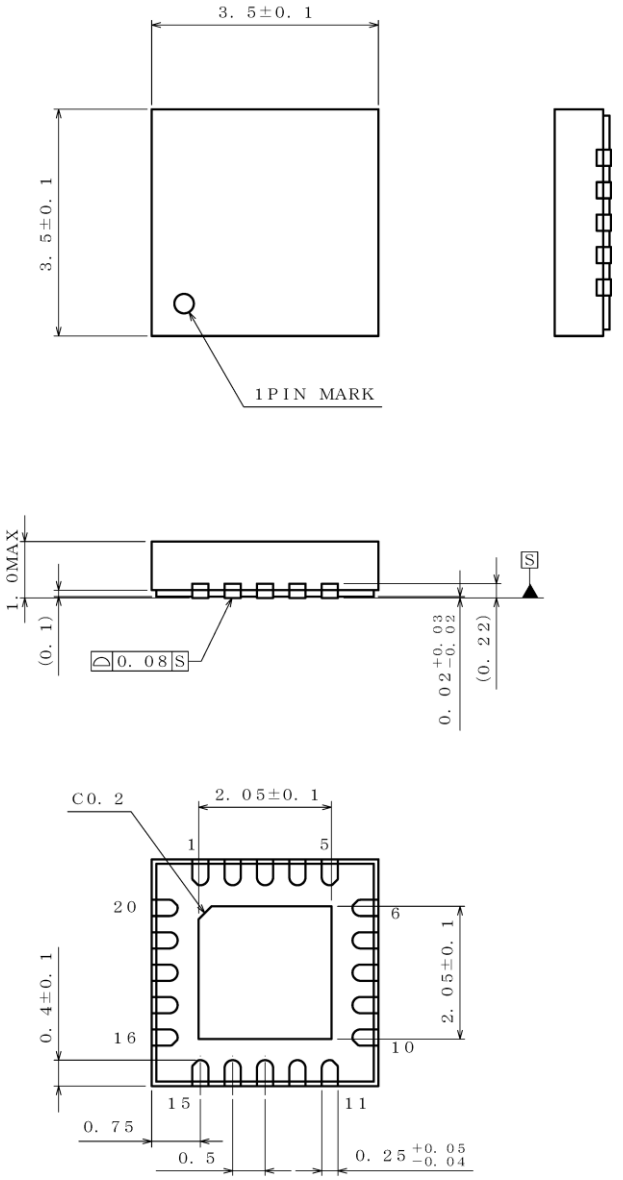
Physical Dimension and Packing Information

Package Name	VQFN20FV3535

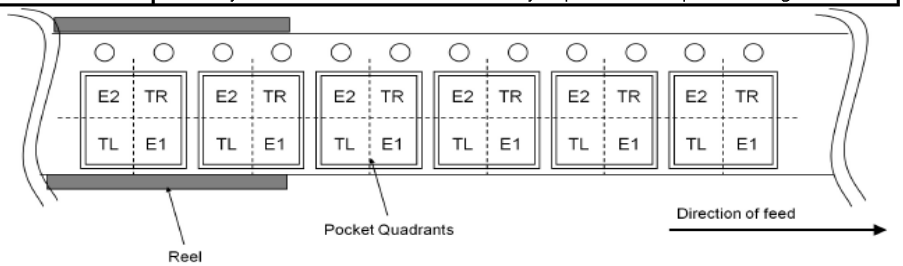


(UNIT:mm)
PKG:VQFN20FV3535
Drawing No. EX375-5001-4

NOTE: Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
16.Mar.2020	001	New Release
5.Feb.2021	002	Change Electrical Characteristics VDRV5 Reference Voltage Before: I_{VDRV5} = 0 mA to 10 mA After: I_{VDRV5} = 0 mA to 10 mA load VDRV5 Drop Voltage Before: I_{VDRV5} = 10 mA After: I_{VDRV5} = 10 mA load VREF3 Reference Voltage Before: I_{VREF3} = 0 mA to 2 mA After: I_{VREF3} = 0 mA to 2 mA load OSCILLATOR Circuit Before: Spread Spectrum Frequency Moduration Width After: Spread Spectrum Frequency Modulation Width GL ON Resistor High Before: I_{GL} = -10 mA After: I_{GL} = 10 mA load GL ON Resistor Low Before: I_{GL} = +10 mA After: I_{GL} = 10 mA input COMP Sink Current Before: V_{DCDIM} = 0 V After: V_{DCDIM1} = V_{DCDIM2} = 0 V Internal Ramp Bottom Voltage Before: (Min) 0.38 (Typ) 0.40 (Max) 0.42 After: (Min) V_{REF3} / 3 x 0.4 - 0.02 (Typ) V_{REF3} / 3 x 0.4 (Max) V_{REF3} / 3 x 0.4 + 0.02 Deletion: V_{REF3} = 3.0 V Internal Ramp Peak Voltage Before: (Min) 2.38 (Typ) 2.40 (Max) 2.42 After: (Min) V_{REF3} / 3 x 2.4 - 0.02 (Typ) V_{REF3} / 3 x 2.4 (Max) V_{REF3} / 3 x 2.4 + 0.02 Deletion: V_{REF3} = 3.0 V PDRV Pull Up ON Resistor Before: V_{SNSP_PDRV} = 7 V, V_{SNSP} = 30 V, V_{DSET} = 5 V, $V_{DRL/PWM}$ = 0 V After: I_{PDRV} = 10 mA load, V_{SNSP} = 30 V, V_{DSET} = 0 V, $V_{DRL/PWMI}$ = 0 V PDRV Pull Down Current Before: V_{DSET} = 0 V, $V_{DRL/PWM}$ = 0 V After: V_{DSET} = 5 V, $V_{DRL/PWMI}$ = 0 V FAULT_B Output Low Voltage Before: I_{FAULT_B} = 5 mA After: I_{FAULT_B} = 5 mA input Change Typical Performance Curves Before: VREF3 Reference Voltage vs Temperature (I_{VREF3} = 0 mA to 2 mA) After: VREF3 Reference Voltage vs Temperature (I_{VREF3} = 0 mA to 2 mA load) Change Application Examples SEPIC Recommended Parts List Inductor L1 Before: MSS1278T-103MLB After: MSD1278T-103MLB

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25.Jun.2026	003	page17 Recommended Setting Parts Range Deleted the maximum specification for the Capacitor Connecting to the VIN Pin. Added the maximum specification for the Resistor Connecting to the Upper Side of the OPUD Pin (transferred from P.42). page33, 35, 37 Recommended Parts List R_{FAULT_B}: Changed from 10 kΩ to 20 kΩ. R_{SSFM_B}: Changed from 47 kΩ to 100 kΩ. R_{DRL}: Changed from 10 kΩ to 100 kΩ. page42 7 OVP (LED Open) Detection Voltage Setting Changed the lower limit of the R_{OPUD1} setting range from 500 kΩ to 450 kΩ. Also transferred this specification to page17 Recommended Setting Parts Range. page43 9 Output Capacitor Selection Corrected an error in the R_{ESR} calculation formula by removing 0.05.

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application examples, their constants, software, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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