Automotive LED Driver Series

24CH Linear LED Driver Embedded Automotive Lamps LED Driver

BD18330EFV-M

General Description

BD18330EFV-M is 24CH constant current driver with a built-in hysteresis type 1CH buck controller and 8-bit PWM dimming and 8-bit local DC dimming for each channel individually. Communication with µ-Controller is available via UART.

Features

- Nano Cap™ Integrated
- AEC-Q100 Qualified*(Note 1)*
- Functional Safety Supportive Automotive Products
- Built-in Hysteresis Type 1CH Buck Controller
- Integrated 24CH LED Constant Current Driver
- UART Interface
- Independent 8-bit PWM Dimming Function
- Independent 8-bit Local DC Dimming Function
- Independent 4-bit Delay Function
- LSI Protection Function (UVLO, TSD)
- LED Abnormality Detection Function (Open/Short)
- LED Cathode Short Detection Function
- Integrated Abnormality Output the FAILB Pin

(Note 1) Grade 1

Application

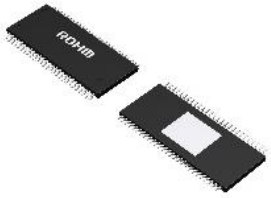
- Rear Lamps (+ Animation)
- Position/DRL (+ Animation)
- Turn (+ Animation)

Key Specification

- Operating Input Voltage Range : 4.5 V to 40.0 V
- LED Pin Maximum Output Current : 125 mA
- Operating Temperature Range : -40 °C to +125 °C

Package

	W (Typ) x D (Typ) x H (Max)
HTSSOP-B54	18.5 mm x 9.5 mm x 1.0 mm



Typical Application Circuit

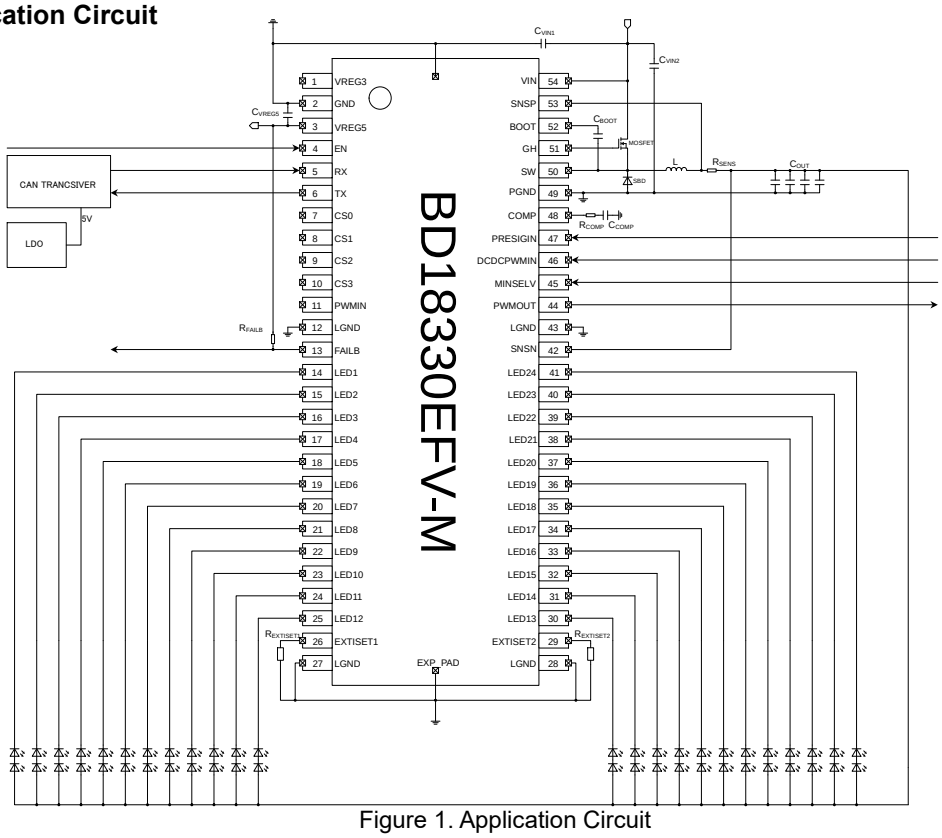


Figure 1. Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

HTSSOP-B54
(TOP VIEW)

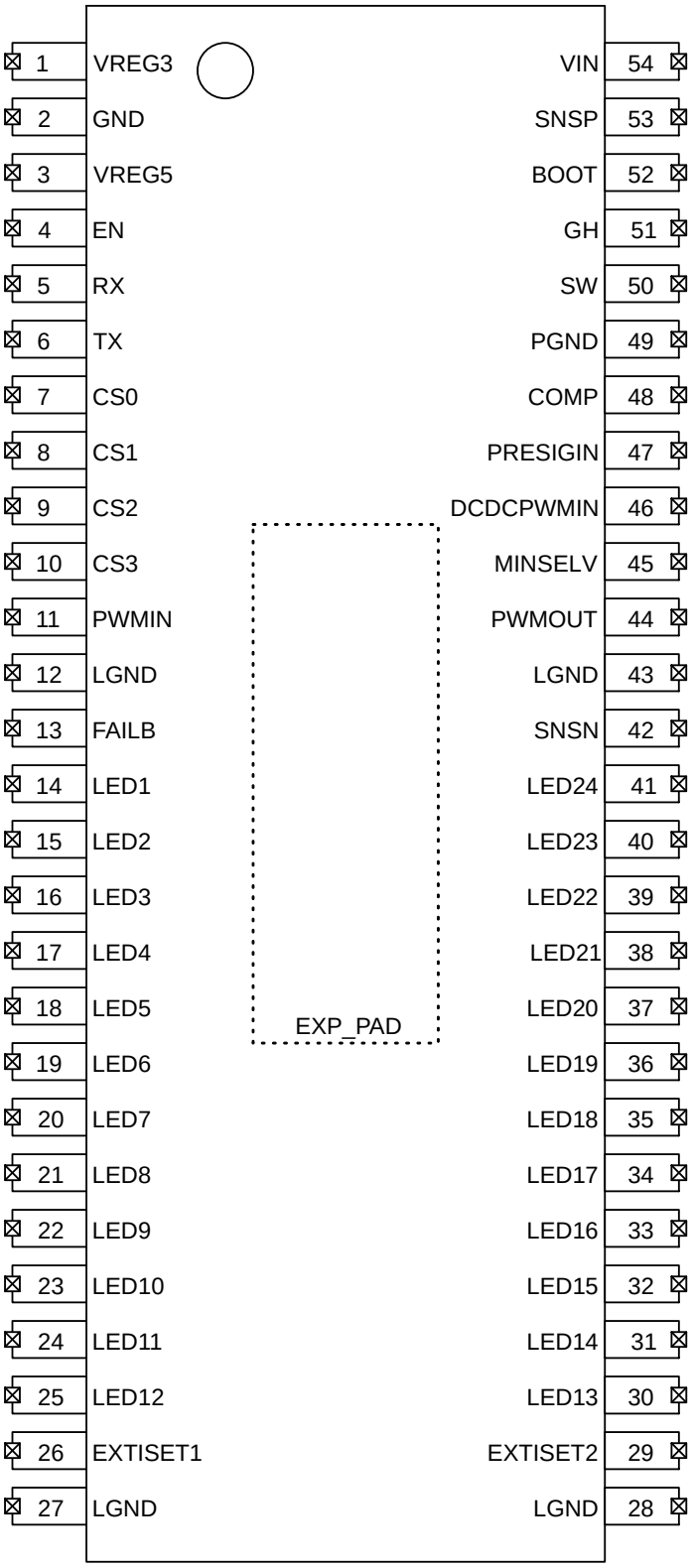


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	VREG3	3.3 V voltage output
2	GND	Ground
3	VREG5	5.0 V voltage output
4	EN	Chip enable
5	RX	UART signal receiver
6	TX	UART signal transmitter
7	CS0	Chip select pin
8	CS1	Chip select pin
9	CS2	Chip select pin
10	CS3	Chip select pin
11	PWMIN	PWM frequency input pin for PWM frequency synchronization
12	LGND	LED driver ground
13	FAILB	Error flag pin
14	LED1	LED output pin
15	LED2	LED output pin
16	LED3	LED output pin
17	LED4	LED output pin
18	LED5	LED output pin
19	LED6	LED output pin
20	LED7	LED output pin
21	LED8	LED output pin
22	LED9	LED output pin
23	LED10	LED output pin
24	LED11	LED output pin
25	LED12	LED output pin
26	EXTISET1	LED current setting pin
27	LGND	LED driver ground

Pin Description - continued

Pin No.	Pin Name	Function
28	LGND	LED driver ground
29	EXTISET2	LED current setting pin for LIMPHOME mode
30	LED13	LED output pin
31	LED14	LED output pin
32	LED15	LED output pin
33	LED16	LED output pin
34	LED17	LED output pin
35	LED18	LED output pin
36	LED19	LED output pin
37	LED20	LED output pin
38	LED21	LED output pin
39	LED22	LED output pin
40	LED23	LED output pin
41	LED24	LED output pin
42	SNSN	Output current sense N pin
43	LGND	LED driver ground
44	PWMOUT	PWM frequency output pin for PWM frequency synchronization
45	MINSELV	LED pins minimum voltage select input pin
46	DCDCPWMIN	DCDCPWM operation signal input pin
47	PRESIGIN	Pre FB setting signal input pin
48	COMP	Erramp output pin
49	PGND	DCDC control driver ground
50	SW	External high side FET source pin
51	GH	External high side FET gate control pin
52	BOOT	External high side FET driver supply pin
53	SNSP	Output current sense P pin
54	VIN	Power supply pin
-	EXP-PAD	Exposed Pad. Connect EXP-PAD to the internal PCB ground plane using multiple via, it will provide excellent heat dissipation characteristics.

Block Diagram

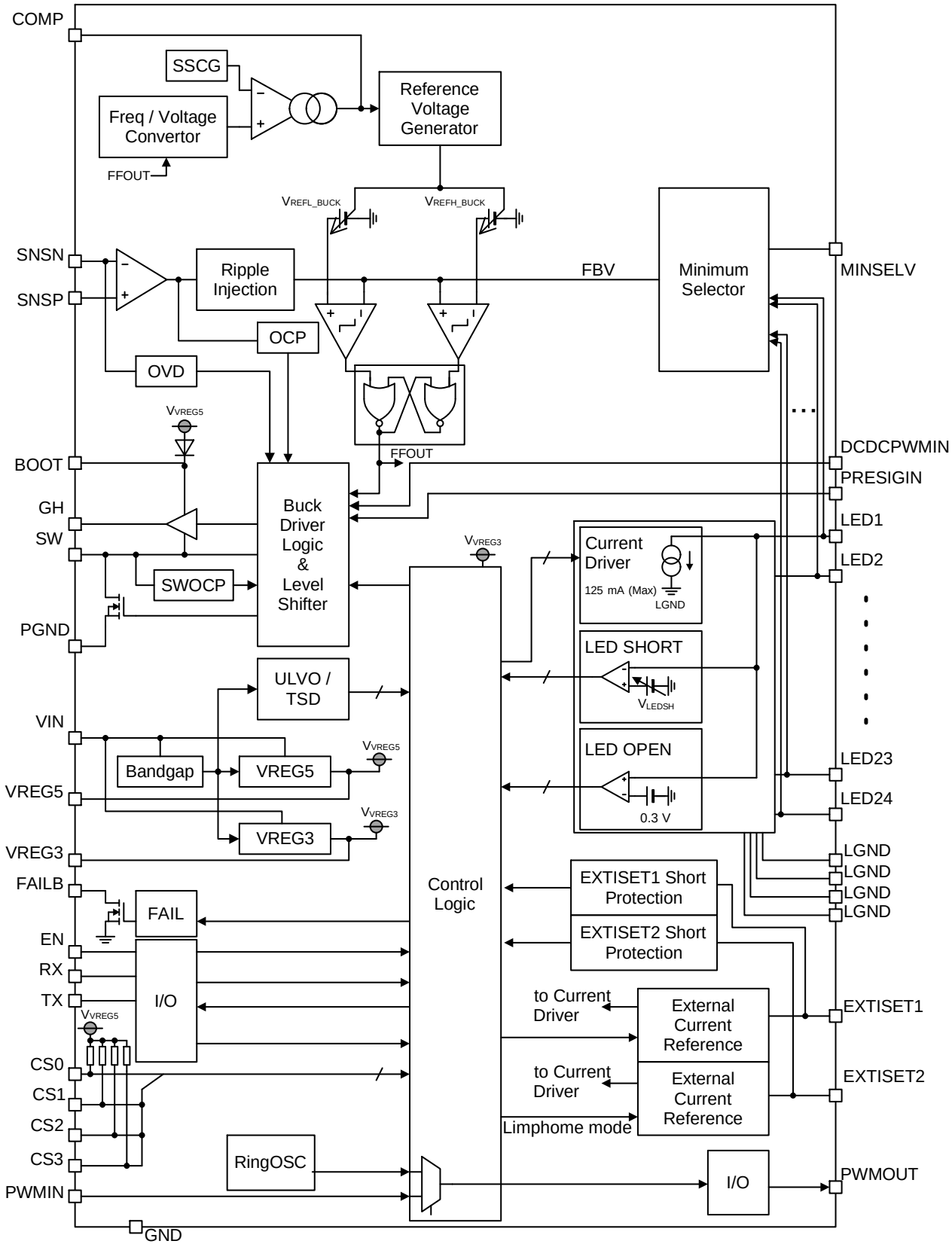


Figure 3. Block Diagram

Description of Block

1. Reference Voltage (VREG5, VREG3)

This IC generates 5.0 V (Typ) and 3.3 V (Typ) from the voltage input to VIN. These voltages are output on the VREG5 and the VREG3 pins. The output voltage of the VREG5 pin (V_{VREG5}) is used as the power supply for the internal circuit, and the output voltage of the VREG3 pin (V_{VREG3}) is used as the power supply for the internal digital circuit. To secure the phase compensation capacitance, it is necessary to connect 1.0 µF to 10 µF to the VREG5 pin and 0.0 µF (the VREG3 pin is able to set for capacitor less application with Nano Cap™ technology) to 0.1 µF to the VREG3 pin. If a capacitor is not connected to the VREG5 pin, circuit operation such as oscillation of the reference voltage will be very unstable. Do not use these pins voltages as a power source other than this LSI.
UVLO function is built-in to the VIN pin, the VREG5 pin and the VREG3 pin. When the conditions of VIN > 4.2 V (Typ), VREG5 > 4.2 V (Typ), VREG3 > 2.8 V (Typ) are satisfied, the IC starts operating. If any condition of VIN < 4.0 V (Typ), VREG5 < 4.0 V (Typ), VREG3 < 2.7 V (Typ) is satisfied, the IC will stop operating.

Nano Cap™ is a combination of technologies which allow stable operation even if output capacitance connected with the range of nF unit. And this IC achieve capacitor less technology with the Nano Cap™ .

2. Current Driver

This IC has a built-in 24CH constant current driver. The maximum output current of the constant current driver is 125 mA/CH when the EXTISET1 function is used. Built-in PWM dimming and DC dimming function for each CH. The resolution for each dimming mode depends on the register settings. Please refer to the detailed description of Address 0x00h, 0x24h to 0x2Fh, 0x30h to 0x32h, 0x33h to 0x4Ah for the setting of dimming mode and output current.

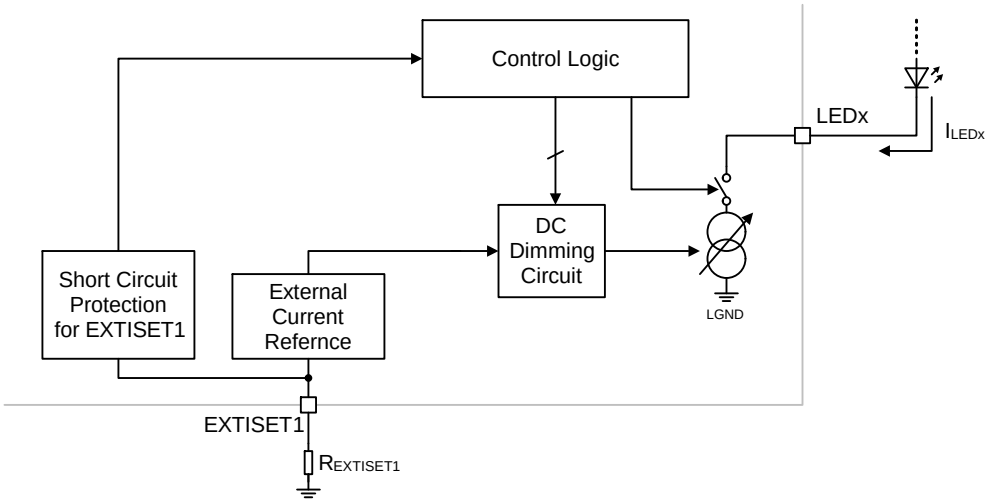


Figure 4. LED Current Setting

(1) Local PWM Dimming Control and LED Current Setting

This IC has a built-in 8-bit PWM dimming function. LED current PWM on duty of each channel can be controlled by UART input. To use 8-bit PWM dimming, set the DIMMODE register value to "0". When using PWM dimming, the LED current can be set by the built-in 4-bit DC dimming function.
LED current PWM on duty and LED current I_{LEDx} (x = 1 to 24) can be calculated by the following formula.

$$PWM\ ON\ duty\ = \frac{DIMSETx[7:0] + 1}{256} \times 100 \quad [\%]$$

where:
$DIMSETx[7:0]$ is the decimal number of DIMSETx[7:0]. (x = 01 to 24)

In case of using the EXTISET1 pin

$$I_{LEDx}\ = \frac{(DCDIMx[3:0] + 1)}{16} \times \left(\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000\right) \quad [A]$$

where:
$DCDIMx[3:0]$ is the decimal number of DCDIMx[3:0]. (x = 01 to 24)
$V_{EXTISET1}$ is the EXTISET1 pin voltage, 600 mV (Typ).
$R_{EXTISET1}$ is the Resistor for connecting the EXTISET1 pin.

2. Current Driver - continued

(2) Local PWM Delay Control

This IC can reduce the load fluctuation by controlling the rising timing of LED current for each CH. This setting is not required when using Local DC dimming described later.
Delay width (t_{DLY_LED}) can be calculated by the following formula.

$$t_{DLY\_LED} = 4bit\_DC\_PWMDLYx[3:0] \times 8 + 24 \quad [\mu s]$$

where:
$4bit\_DC\_PWMDLYx[3:0]$ is the decimal number of PWMDLYx[3:0]. (x = 01 to 24)
t_{LED_ONn} is LED current PWM on time. (n = 1 to 24)
f_{PWM} is PWM dimming frequency.

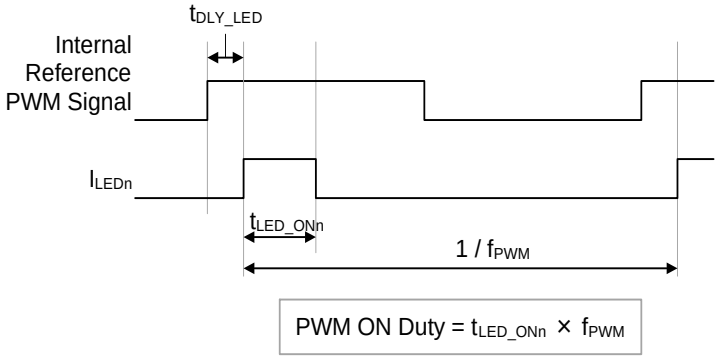


Figure 5. Local PWM Delay Control

(3) Local DC Dimming Control

This IC can switch the 8-bit PWM dimming register for Local DC dimming. To use 8-bit DC dimming, set the DIMMODE register value to "1". When using 8-bit DC dimming, PWM ON Duty is fixed at 100 %.
LED current I_{LEDn} (n = 1 to 24) can be calculated by the following formula.

In case of using the EXTISET1 pin

$$I_{LEDn} = \frac{(DIMSETx[7:0] + 1)}{256} \times \left(\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000\right) \quad [A]$$

where:
$DIMSETx[7:0]$ is the decimal number of DIMSETx[7:0].
$V_{EXTISET1}$ is the EXTISET1 pin voltage, 600 mV (Typ).
$R_{EXTISET1}$ is the Resitor for connecting the EXTISET1 pin.

(4) LED Current Output Enable (PWMOUT, LEDEN)

This IC can individually turn off the CH regardless of the PWM/DC dimming setting. It can be set by updating the register of Address 0x30h (PWMOUTL), 0x31h (PWMOUTM) and 0x32h (PWMOUTH). When this register is set, the output is kept on until the next PWM cycle and the output is turn off at the PWM rising timing. The LED current ON/OFF control can also be controlled using the Address 0x04h (LEDENL), 0x05h (LEDENM) and 0x06h (LEDENH) registers. For these registers, ON/OFF control is reflected immediately when written to the register.

Description of Blocks – continued

3. Buck DC/DC Control Signal Output

This IC has a built-in buck DC/DC controller that reduces the heat generation of the IC. This controller operates so that the lowest voltage of LED1 pin to LED24 pin voltage becomes a constant voltage. By using the hysteresis type, it is possible to respond to sudden load changes during animation. In addition, to suppress the ripple voltage of the LEDx (x = 1 to 24) pin voltage, a ripple injection circuit that adds information on the current flowing through the coil to the feedback voltage is built in. Built-in SSCG circuit and frequency stabilization circuit to prevent EMC noise.

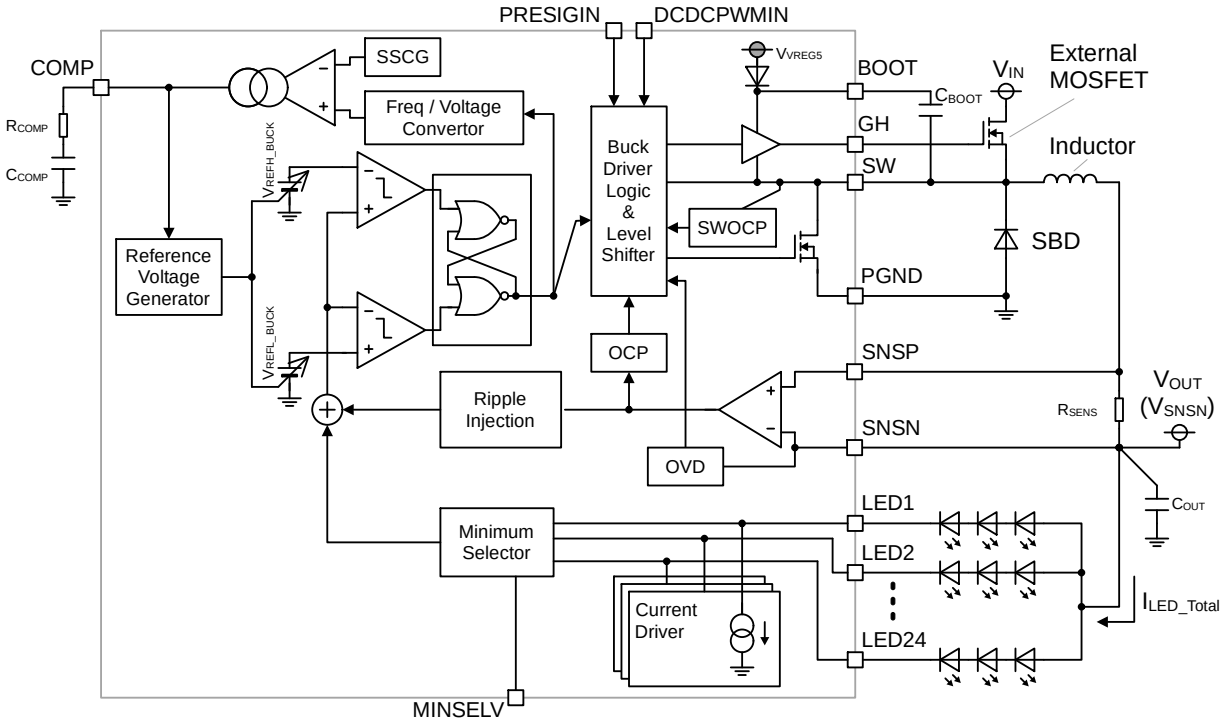


Figure 6. Buck DC/DC Controller Block Diagram

(1) Minimum Voltage Feedback Control

To reduce the power consumption of the IC, this IC operate with the minimum voltage from the LED1 pin to the LED24 pin and MINSELV pin input voltage from follower device as the feedback voltage for DC/DC control.

(2) PREBOOST Control

To prevents LED flicker due to load fluctuation during PWM/DC dimming, it has a built-in PREBOOST function that raises SNSN pin voltage immediately before load fluctuation. PREBOOST time is programmed by UART input. (Address 0x02: SYSSET2)

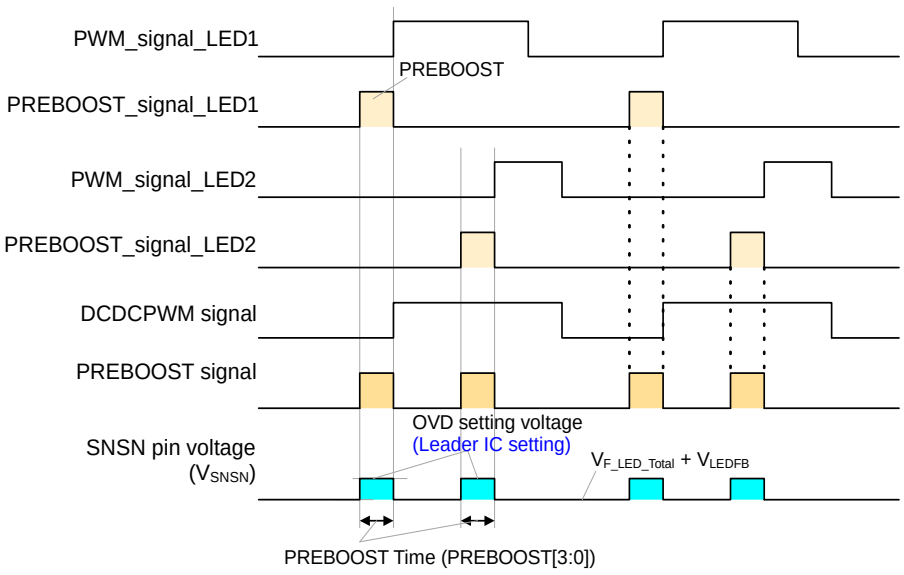


Figure 7. PREBOOST Function

3. Buck DC/DC Controller – continued

(3) Over Current Protection (OCP) and Selection of the Inductor and Resistor (R_{SENS})

This IC has a built-in the over current protection (OCP) to protect the inductor and MOSFET. When $V_{SNSP-SNSN}$ > V_{OCP} (over current protection threshold voltage), external MOSFET will be controlled to turn off.
OCP threshold current (I_{OCP}) can be calculated by the following formula.

$$I_{OCP} = \frac{V_{OCP}}{R_{SENS}} \quad [A]$$

V_{OCP} is the over current protection threshold voltage, 100 mV (Typ)
R_{SENS} is the resistor for monitor inductor current.

To prevent false detection of OCP during normal operation, select external components so that the following formula is satisfied.

$$V_{OCP} > \left(I_{LED\_Total} + \frac{I_{L\_RIPPLE}}{2}\right) \times R_{SENS} \quad [V]$$

$$I_{L\_RIPPLE} = \frac{(V_{IN} - V_{SNSN})}{L} \times t_{ON} \quad [A]$$

$$t_{ON} = \frac{V_{SNSN}}{V_{IN}} \times \frac{1}{f_{SW}} \quad [s]$$

I_{LED_Total} is the LED total current.
I_{L_RIPPLE} is the inductor ripple current.
V_{SNSN} is the SNSN pin voltage.
t_{ON} is the turn on time of external MOSFET.
f_{SW} is the DC/DC switching frequency, 400 kHz (Typ).

Also, to stably feedback the current information of the inductor, set so that the following formula is also satisfied.

$$V_{SNS\_RIPPLE} = I_{L\_RIPPLE} \times R_{SENS} > 10\,mV \quad [V]$$

V_{SNS_RIPPLE} is the ripple voltage between the SNSP pin and SNSN pin.

(4) Selection of the Capacitor for Connecting SNSN Pin (C_{OUT})

To ensure the stability of buck DC/DC controller, set the capacitor for connecting SNSN pin (C_{OUT}) so that it satisfies the following formula.

$$V_{OUT\_RIPPLE} \ll V_{SNS\_RIPPLE} \times G_{RIPPLE}$$

Recommendation is the following formula.

$$V_{OUT\_RIPPLE} < \frac{1}{2} \times V_{SNS\_RIPPLE} \times G_{RIPPLE}$$

$$V_{OUT\_RIPPLE} \approx \frac{I_{L\_RIPPLE} \times t_{ON}}{C_{OUT}}$$

V_{OUT_RIPPLE} is the DC/DC output ripple voltage.
G_{RIPPLE} is the GAIN of ripple injection, 10 (Typ).
C_{OUT} is the capacitor for connecting SNSN pin.

(5) External MOSFET Over Current Protection (SWOCP)

This IC has a built-in external MOSFET over current protection (SWOCP) to protect the external MOSFET. When SWOCP is detected, the external MOSFET is hiccup controlled (SWOCP hiccup time = 10 ms (Typ)) to prevent MOSFET destruction. SWOCP threshold voltage can be calculated by the following formula.

$$V_{IN} - V_{SW} > V_{SWOCP}$$

V_{IN} is the VIN pin voltage.
V_{SW} is the SW pin voltage.
V_{SWOCP} is the external MOSFET over current protection threshold voltage, 1.0 V (Typ).

Description of Blocks – continued

4. Diagnosis Enable (DEN)

When $V_{IN} < V_{IN\_DEN}$, the IC cannot detect LED Open Detection (LEDOP).
V_{IN_DEN} can be defined by setting register. (Address 0x17h)

5. LED Short Protection and Open Protection

This IC has LED short protection and open protection. LED short protection can be disabled, and LED short protection voltage can be controlled by UART input. (Disable setting: Address 0x09h, 0x0Ah, protection voltage setting: Address 0x0Bh to 0x16h) And also, LED open protection can be disabled by UART input. (Disable setting: Address 0x08h)
LED short and open error status of each channel can be read by UART input. (LED short: Address 0x4Bh to 0x4Dh, LED open: Address 0x4Dh to 0x50h)
The IC can detect LED short condition when IC meets the following condition:

$$V_{LEDx} > V_{LEDSH} \; and \; V_{IN} > V_{IN\_DEN}$$

Where:
V_{LEDx} is the LEDx pin voltage. (x = 1 to 24)
V_{LEDSH} is the LED short detecting voltage.
V_{IN_DEN} is the Diagnosis Enable VIN voltage.

The IC can also detect LED open condition when the IC meets the following condition:

$$V_{LEDx} < V_{LEDOP} \; and \; V_{IN} > V_{IN\_DEN}$$

Where:
V_{LEDx} is the LEDx pin voltage. (x = 1 to 24)
V_{LEDOP} is the LED open detecting voltage, 0.3 V (Typ).
V_{IN_DEN} is the Diagnosis Enable VIN voltage.

If the IC detects LED error (short or open) mode and set AUTOOFF register to “1” (Address 0x07h: SYSSET4), Current Driver of detected CH is turn off and the FAILB pin voltage is switched to “Low”. Other current driver CH are continuing to output.

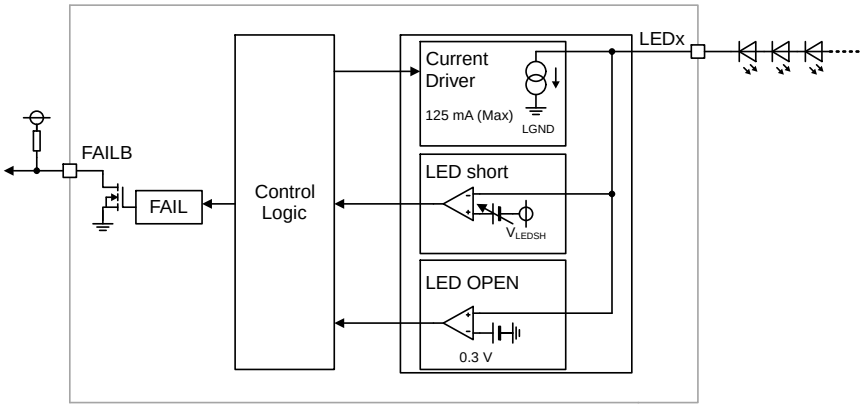


Figure 8. LED Open Detection

5.1 LED Error Output Mask Time Setting

The mask time for LED error detection can be controlled by UART input. (Address 0x03h: SYSSET3)
LED error detection is disabled until the mask time has elapsed.

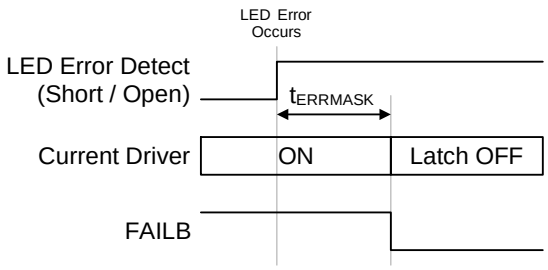


Figure 9. LED Error Output Mask Time Setting

Where:
$t_{ERRMASK}$ is the mask time for LED error detection.

Description of Blocks – continued

6. Protection Feature

Table 1. Protection Table 1

No.	Protection	Detect condition	Release condition	DC/DC	Current Driver	FAILB	Status register	LIMPHOME *(Note 2)*
1	VIN UVLO	VIN < 4.0 V (Typ)	VIN > 4.2 V (Typ)	OFF	OFF	Low	UVLOTSD ERR	O
2	VREG5 UVLO	VREG5 < 4.0 V (Typ)	VREG5 > 4.2 V (Typ)	OFF	OFF	Low	UVLOTSD ERR	O
3	VREG3 UVLO	VREG3 < 2.7 V (Typ)	VREG3 > 2.8 V (Typ)	OFF	OFF	Low	UVLOTSD ERR	O
4	TSD	Ta > 175 °C (Typ)	Ta < 150 °C (Typ)	OFF	OFF	Low	UVLOTSD ERR	O
5	TSD warning	Ta > 125 °C (Typ)	Ta < 110 °C (Typ)	operating	operating	Low	TSDW	O
6	LED open	V_{LEDx} < 0.3 V (Typ)	V_{LEDx} > 0.4 V (Typ)	operating	Selectable of auto turn off	Low	LOPERR	O
7	LED Short	V_{LEDx} > register setting & PWM “High”	V_{LEDx} < register setting & PWM “High”	operating	Selectable of auto turn off	Low	LSHERR	-
8	LED cathode short *(Note 1)*	V_{LEDx} < 0.3 V (Typ)	-	Should keep off *(Note 3)*	Should keep off *(Note 3)*	Low	CATHERR	-
9	CRC error	Error in data setent in UART Write/Read	No error in data sent in UART Write	operating	operating	Low	CRCERR	O
10	UART WDT	UART no access during 100 ms	-	operating	operating	Low	WDTERR	-
11	OCP	$V_{SNSP-SNSN}$ > 100 mV (Typ)	$V_{SNSP-SNSN}$ < 100 mV (Typ)	OFF	operating	Low	OCPERR	-
12	SWOCP	V_{IN} - V_{SW} > 1.0 V (Typ)	V_{IN} - V_{SW} < 1.0 V (Typ)	OFF	OFF	Low	SWOCP ERR	-
13	OVD	V_{SNSN} > register setting	V_{SNSN} < register setting	OFF	operating	-	-	-
14	ISETSH1	$R_{EXTISET1}$ < 30 kΩ (Typ)	$R_{EXTISET1}$ > 30 kΩ (Typ)	operating	operating	Low	ISETSH ERR	O
15	ISETSH2	$R_{EXTISET2}$ < 30 kΩ (Typ)	$R_{EXTISET2}$ > 30 kΩ (Typ)	operating	operating	Low	ISETSH ERR	O

When it detects “VINUVLO” or “VREG3UVLO” or “VREG5UVLO” or “TSD” or “EN = L”, it invokes system reset. It can’t detect other protection. (x = 1 to 24)

(Note 1) “LED open protection” is not available when set CATHEN register to “1”.
(Note 2) “O” this protection can be detected during LIMPHOME mode. “-” this protection cannot be detected during LIMPHOME mode. If any of “-” protection is detect before entering LIMPHOME mode, keep status register until mode returns to normal.
(Note 3) Please execute this function before the LED dimming. For details, refer to description of “LED Cathode Short”.

The FAILB pin is recommended to pull up to VREG5. Recommended value for pull up resistance is 20 kΩ to 100 kΩ. When above failure is detected, the FAILB pin voltage becomes “Low”. If the FAILB pin is not used pin shall be kept open.

6. Protection Feature – continued

Table 2. Protection Table 2

No.	Protection	SSMASK	ERRMASK	Protection enable	Status and FAILB output latch enable	AUTOOFF
1	VIN UVLO	-	-	-	O	-
2	VREG5 UVLO	-	-	-	O	-
3	VREG3 UVLO	-	-	-	O	-
4	TSD	-	-	-	O	-
5	TSD warning	-	-	TSDWEN	-	-
6	LED open	O	O	LOPEN	LOPLAT	O
7	LED short	O	O	LSHEN	LSHLAT	O
8	LED cathode short	-	-	CATHEN	O	-
9	CRC error	-	-	-	CRCERLAT	-
10	UART WDT	-	-	WDTEN	O	-
11	OCP	-	-	OCPEN	OCPLAT	-
12	SWOCP	-	-	SWOCPEN	-	-
13	OVD	O	-	-	-	-
14	ISETSH1	-	-	ISETSEL	ISETLAT	-
15	ISETSH2	-	-	ISETSEL	ISETLAT	-

O: It has this function by default.
-: It doesn't have this function.

7. PWM Synchronization for Each Device

This feature allows the BD18330EFV-M to synchronize its internal clock with Leader device. SYNCSET register can set this IC as Leader or Follower. As Leader device (BD18330EFV-M), it generates 488 Hz (Typ) reference signal (Duty = 50 %) in PWMOUT that other Follower devices (BD18332EUV-M) use to adjust internal clock. As Follower device, it enables PWMIN input to receive the reference signal to adjust internal clock and LED output timing.

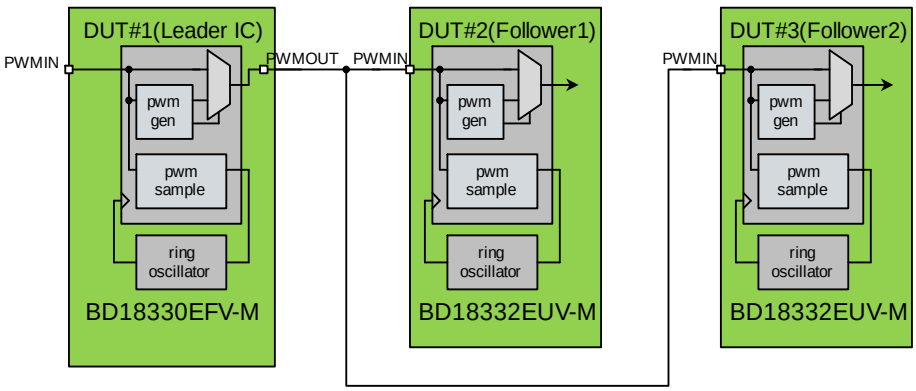


Figure 10. PWM Synchronization Setting

In this figure above, DUT#1 is a Leader device, it generates the reference signal via PWMOUT. On the other hand, DUT#2 receives the reference signal via PWMIN, it processes this signal to adjust the internal ring oscillator. Same process in DUT#2 occur in DUT#3 and so on. There is only a single Leader device.

Description of Blocks – continued

8. LIMPHOME Function

This IC has LIMPHOME function. This function is controlled by LIMPHEN register (Address 0x5Eh, initially enabled). If LIMPHEN is “1” and there is no UART access (no CRC OK) for over 1.0 s (Typ), device detects the error and operates LED dimming. In each state, LED dimming is according to the latest register value (DIMSET, DCDIM and LHDTY). The registers are updated at the timing described in the register description.

Note: Devices can be connected in parallel, refer to UART Protocol for more details. When a device is connected in parallel and is not being accessed while other devices are being accessed, it will not enter LIMPHOME mode.

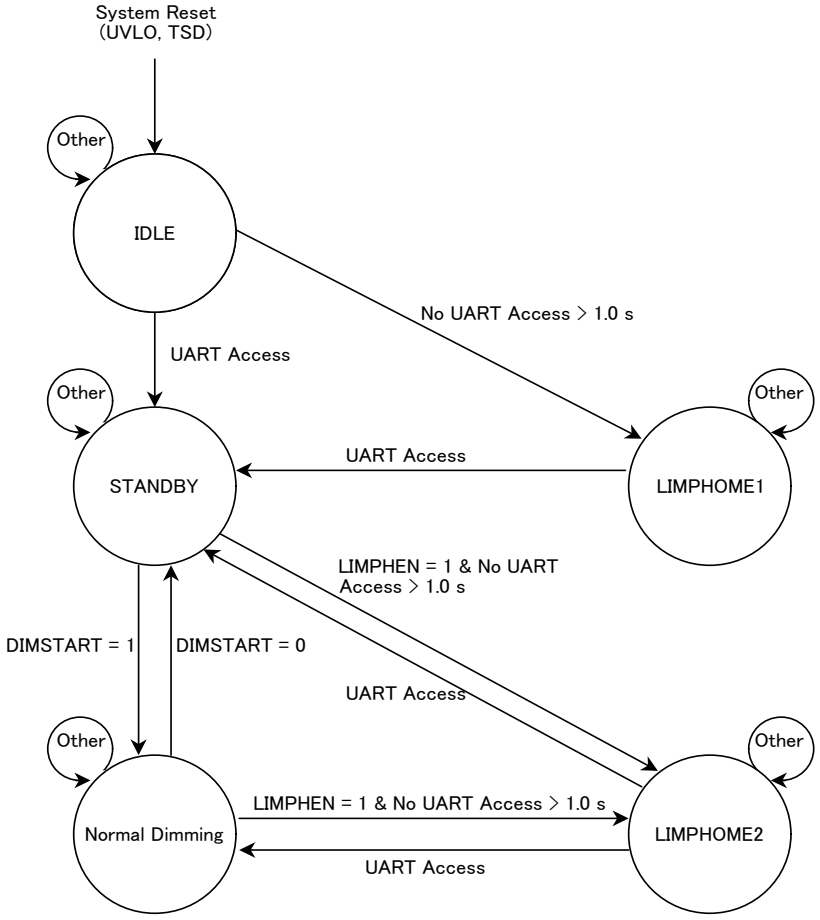


Figure 11. LIMPHOME Function

Table 3. LIMPHOME Dimming Settings (x = 1 to 24)

State	Description	Dimming setting		
		Current reference setting	DC current setting	PWM duty setting
IDLE	Reset condition, No lighting	-	-	-
STANDBY	During initial setting, No lighting	-	-	-
LIMPHOME1	lighting by EXTISET2 resistor (UART error condition)	EXTISET2	100 % (DCDIMx)	100 % (LHDTYx)
Normal Dimming	Normal dimming condition	ISETSEL = 0 (Internal ISET)*(Note 1)* ISETSEL = 1 (EXTISET1)	DIMMODE = 0 DCDIMx DIMMODE = 1 DIMSETx	DIMMODE = 0 DIMSETx DIMMODE = 1 100 %
LIMPHOME2	lighting by UART LIMPHOME setting (UART error condition)	LEXTISET2SEL = 1*(Note 1)* EXTISET1 + EXTISET2 LEXTISET2SEL = 0 ISETSEL = 0 (Internal ISET) ISETSEL = 1 (EXTISET1)	DIMMODE = 0 DCDIMx DIMMODE = 1 DIMSETx	LHDTYx

(Note 1) Not Recommended Setting

8. LIMPHOME Function – continued

At LIMPHOME1,

In case of the EXTIET2 pin set “OPEN”

$$I_{LEDn} = 0 \quad [A]$$

In case of the EXTISET2 pin set $R_{EXTISET2}$

$$I_{LEDn} = \frac{V_{EXTISET2}}{R_{EXTISET2}} \times 12000 \quad [A]$$

At LIMPHOME2,

$$PWM\ ON\ duty = \frac{LHDTYx[3:0] + 1}{16} \times 100 \quad [\%]$$

In case of using the EXTISET2 pin and the EXTISET2 pin set “OPEN”

$$I_{LEDn} = 0 \quad [A]$$

In case of using the EXTISET2 pin and DIMMODE = 0

$$I_{LEDn} = \frac{(DCDIMx[3:0] + 1)}{16} \times \left(\frac{V_{EXTISET1}}{R_{EXTISET1}} + \frac{V_{EXTISET2}}{R_{EXTISET2}}\right) \times 12000 \quad [A]$$

In case of using the EXTISET2 pin and DIMMODE = 1

$$I_{LEDn} = \frac{(DIMSETx[7:0] + 1)}{256} \times \left(\frac{V_{EXTISET1}}{R_{EXTISET1}} + \frac{V_{EXTISET2}}{R_{EXTISET2}}\right) \times 12000 \quad [A]$$

In case of using the Internal Current Set and DIMMODE = 0

$$I_{LEDn} = \frac{(DCDIMx[3:0] + 1)}{16} \times 0.060 \quad [A]$$

In case of using the Internal Current Set and DIMMODE = 1

$$I_{LEDn} = \frac{(DIMSETx[7:0] + 1)}{256} \times 0.060 \quad [A]$$

In case of using the EXTISET1 pin and DIMMODE = 0

$$I_{LEDn} = \frac{(DCDIMx[3:0] + 1)}{16} \times \left(\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000\right) \quad [A]$$

In case of using the EXTISET1 pin and DIMMODE = 1

$$I_{LEDn} = \frac{(DIMSETx[7:0] + 1)}{256} \times \left(\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000\right) \quad [A]$$

where: (n = 1 to 24, x = 01 to 24)
I_{LEDn} is each channel current.
$V_{EXTISET2}$ is the EXTISET2 pin voltage. It is 300 mV (Typ).
$R_{EXTISET2}$ is the Resistor for connecting the EXTISET2 pin.
$LHDTYx[3:0]$ is the decimal number of LHDTYx[3:0].
$DCDIMx[3:0]$ is the decimal number of DCDIMx[3:0].
$DIMSETx[7:0]$ is the decimal number of DIMSETx[7:0].
$V_{EXTISET1}$ is the EXTISET1 pin voltage, 600 mV (Typ).
$R_{EXTISET1}$ is the Resistor for connecting the EXTISET1 pin.

Absolute Maximum Ratings (Tj = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{IN}	-0.2 to +42.0	V
EN Pin Voltage	V_{EN}	-0.2 to VIN	V
SW Pin Voltage	V_{SW}	-0.2 to VIN	V
SNSP, SNSN Pin Voltage	V_{SNSP}, V_{SNSN}	-0.2 to +42.0	V
SNSP-SNSN Voltage	$V_{SNSP-SNSN}$	-0.3 to +0.3	V
BOOT, GH Pin Voltage	V_{BOOT}, V_{GH}	-0.2 to +49.0	V
BOOT-SW Voltage BOOT-GH Voltage GH-SW Voltage	$V_{BOOT-SW}$, $V_{BOOT-GH}$, V_{GH-SW}	-0.2 to +7.0	V
LED1 to LED24 Pin Voltage	V_{LED1} to V_{LED24}	-0.2 to +42.0	V
VREG3 Pin Voltage	V_{VREG3}	-0.2 to +4.5	V
VREG5, FAILB, RX, TX, PRESIGIN, MINSELV, DCDCPWMIN, COMP, CS0, CS1, CS2, CS3, PWMIN, PWMOUT, EXTISET1, EXTISET2 Pin Voltage	V_{VREG5}, V_{FAILB}, V_{RX}, V_{TX}, $V_{PRESIGIN}$, $V_{MINSELV}$, $V_{DCDCPWMIN}$, V_{COMP}, V_{CS0}, V_{CS1}, V_{CS2}, V_{CS3}, V_{PWMIN}, V_{PWMOUT}, $V_{EXTISET1}$, $V_{EXTISET2}$	-0.2 to +7.0 < V_{VREG5}	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
HTSSOP-B54				
Junction to Ambient	θ_{JA}	59.10	26.10	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	8.00	7.00	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD18330EFV-M Chip.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Power Supply Voltage*(Note 1)*	VIN	4.5	12.0	40.0	V	
Operating Temperature	Topr	-40	25	+125	°C	
The Capacitor for Connecting the VREG5 Pin	C_{VREG5}	1.0	4.7	10.0	µF	
The Capacitor for Connecting the VREG3 Pin*(Note 2)*	C_{VREG3}	0.0	-	0.1	µF	
The Capacitor for Connecting the BOOT Pin	C_{BOOT}	0.047	0.1	0.22	µF	
Coupling Output Capacitor	C_{OUT}	10	-	-	µF	
Current Sense Resistor for Connecting between the SNSP and SNSN Pin	R_{SENS}	10	-	-	mΩ	
The Resistor for Connecting the EXTISET1 Pin	$R_{EXTISET1}$	56	-	720	kΩ	
The Resistor for Connecting the EXTISET2 Pin	$R_{EXTISET2}$	56	-	720	kΩ	
The Resistor for Connecting the FAILB Pin	R_{FAILB}	56	100	220	kΩ	
PWMIN Frequency	f_{EXTCLK}	400	488	600	Hz	
PWMIN Duty	D_{EXTCLK}	-	50	-	%	Please connect to the PWMOUT pin of Leader device

Note: Above operation range is referring to IC independently. Thorough verification of the coefficient setting in actual application shall be practiced.

(Note 1) When IC is started, the voltage must be UVLO release voltage or more. Therefore, consider the power supply drop caused by the parasitic resistor. VIN (Min) = 4.5 V is the minimum value that can operate the IC independently after started. The minimum value of power supply voltage that can be set depends on the voltage drop due to the parasitic resistor of power line.

(Note 2) The VREG3 pin is designed to work with “Capacitor less” application for use Nano Cap™ technology. When adding capacitor, it may affect noise. So please kindly consider noise reduction such as using a 2s2p PCB board and etc.

Electrical Characteristic

(Unless otherwise specified: V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Device Overview]						
Circuit Current	I_{CC}	-	14.0	24.0	mA	V_{EN} = High, 24CH Current driver OFF
Standby Current	I_{STB}	-	7.5	18.0	μA	V_{EN} = Low
[VREG5 Block]						
VREG5 Pin Output Voltage	V_{VREG5}	4.5	5.0	5.5	V	I_{VREG5} = 0 mA
VREG5 Pin Load Regulation Voltage	ΔV_{VREG5}	-	-	50	mV	I_{VREG5} = 5 mA
VREG5 Pin Over Current Protection	$I_{VREG5OCP}$	60	-	-	mA	
[VREG3 Block]						
VREG3 Pin Output Voltage	V_{VREG3}	3.1	3.3	3.5	V	I_{VREG3} = 0 mA
VREG3 Pin Load Regulation Voltage	ΔV_{VREG3}	-	-	30	mV	I_{VREG3} = 5 mA
VREG3 Pin Over Current Protection	$I_{VREG3OCP}$	30	-	-	mA	
[Constant Current Driver Block]						
LED Pin ON Resistance	R_{LED1}	-	-	6.5	Ω	Tj = 25 °C
	R_{LED2}	-	-	9.5	Ω	Tj = -40 °C to +150 °C
LED Pin Output Current Absolute Error 1 ($I_{OUT\_AVE}/I_{OUT\_IDEAL}$ - 1)	ΔI_{OUTA1}	-3.5	-	+3.5	%	Tj = 25 °C, $R_{EXTISET1}$ = 120 kΩ, ISETSEL = 1, DCDIMx[3:0] = 0xFh, DIMSETx[7:0] = 0xFFh (x = 01 to 24)
		-5.5	-	+5.5	%	Tj = -40 °C to +150 °C, $R_{EXTISET1}$ = 120 kΩ, ISETSEL = 1, DCDIMx[3:0] = 0xFh, DIMSETx[7:0] = 0xFFh (x = 01 to 24)
LED Pin Output Current Relative Error 1 (I_{OUTx}/I_{OUT_AVE} - 1)	ΔI_{OUTR1}	-4	-	+4	%	Tj = 25 °C, $R_{EXTISET1}$ = 120 kΩ, ISETSEL = 1, DIMSETx[7:0] = 0xFFh (x = 01 to 24)
LED Pin Output Current DC Dimming Function Differential Nonlinearity*(Note 1)*	I_{INL}	-1.5	-	+1.5	LSB	Tj = 25 °C $R_{EXTISET1}$ = 120 kΩ, ISETSEL = 0, DIMMODE = 0, DCDIMx[3:0] = 0x0h to 0xFh DIMSETx[7:0] = 0xFFh, (x = 01 to 24)
	I_{DNL}	-1.5	-	+1.5	LSB	
PWM Frequency	f_{PWM}	440	488	535	Hz	
EXTISET1 Pin Short Circuit Protection Resistor	$R_{EXTISET1\_SCP}$	-	30	50	kΩ	
EXTISET2 Pin Short Circuit Protection Resistor	$R_{EXTISET2\_SCP}$	-	30	50	kΩ	

(Note 1) Guaranteed by design only.

Electrical Characteristic - continued
(Unless otherwise specified: V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[Buck DC/DC Converter Block]						
GH Pin High Side PMOS ON Resistance	R_{ONH_GH}	-	5.5	12.0	Ω	
GH Pin Low Side NMOS ON Resistance	R_{ONL_GH}	-	1.2	5.0	Ω	
SW Pin Low Side NMOS ON Resistance	R_{ONL_SW}	-	1.5	6.0	Ω	
Over Current Protection Threshold Voltage	V_{OCP}	60	100	140	mV	
External MOSFET Over Current Protection Threshold Voltage	V_{SWOCP}	0.8	1.0	1.2	V	
COMP Pin Source Current	I_{COMP_SO}	100	200	300	µA	
COMP Pin Sink Current	I_{COMP_SI}	-300	-200	-100	µA	
Switching Frequency	f_{SW}	376	400	424	kHz	
Spread Spectrum Frequency	f_{RAMP}	103.2	122.1	140.9	Hz	
Spread Spectrum Width	W_{SPREAD}	8	9	10	%	
GAIN of Ripple Injection	G_{RIPPLE}	-	10	-	-	
LED Terminal Feedback Voltage	V_{LEDFB}	0.9	1.0	1.1	V	
OVD Threshold Voltage	V_{OVD}	5.4	6.0	6.6	V	OVDVOLT[3:0] = 0x6h
SWOCP Hiccup Time	t_{HICCUP}	7.5	10.0	12.5	ms	
SNSP Pin Bias Current 1	I_{SNSP1}	-	40	55	µA	V_{SNSP} = 4.0 V, $V_{SNSP-SNSN}$ = 0 mV
SNSP Pin Bias Current 2	I_{SNSP2}	-	60	80	µA	V_{SNSP} = 4.0 V, $V_{SNSP-SNSN}$ = 50 mV
SNSN Pin Bias Current	I_{SNSN}	-	47	65	µA	V_{SNSP} = 4.0 V, $V_{SNSP-SNSN}$ = 0 mV
[PROTECT LOGIC Block]						
VREG5UVLO Detection Voltage	$V_{VREG5UVLO}$	3.8	4.0	4.2	V	V_{VREG5} falling detect threshold
VREG5UVLO Hysteresis Voltage	$V_{VREG5UVHYS}$	-	200	-	mV	
VREG3UVLO Detection Voltage	$V_{VREG3UVLO}$	2.5	2.7	2.9	V	V_{VREG3} falling detect threshold
VREG3UVLO Hysteresis Voltage	$V_{VREG3UVHYS}$	-	100	-	mV	
VINUVLO Detection Voltage	$V_{VINUVLO}$	3.8	4.0	4.2	V	V_{VIN} falling detect threshold
VINUVLO Hysteresis Voltage	$V_{VINUVHYS}$	-	200	-	mV	
[LED Abnormal Detection Block]						
LEDOPEN Detection Voltage	V_{LEDOP}	0.2	0.3	0.4	V	V_{LEDn} falling detect threshold (n = 1 to 24)
SHORT Detection Voltage	V_{LEDSH}	1.75	2.00	2.25	V	V_{LEDn} rising detect threshold (n = 1 to 24) LEDSHx[7:0] = 0x22h (x = 01 to 24)
Diagnosis Enable VIN Voltage	V_{IN_DEN}	6.3	7.0	7.7	V	DENVOLT[3:0] = 0x7h

Electrical Characteristic - continued
(Unless otherwise specified: V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
[EN Input Pin]						
EN Pin Input Current	I_{EN}	2.5	5.0	10.0	µA	V_{EN} = 5.0 V
EN Input Pin High Voltage	V_{ENH}	0.75 x V_{VREG5}	-	V_{IN}	V	
EN Input Pin Low Voltage	V_{ENL}	-0.2	-	0.2 x V_{VREG5}	V	
[LOGIC Input (CS0, CS1, CS2, CS3)]						
CSx Pin Output Current	I_{CSx}	-10	-5	-	µA	(x = 0,1,2,3) V_{CSx} = 0.0 V
CSx Pin Setting Voltage	V_{CSxSET}	-	-	2.5	V	
[LOGIC Input (PWMIN)]						
PWMIN Pin Input Current	I_{PWMIN}	20	50	100	µA	V_{PWMIN} = 5.0 V
PWMIN Input Pin High Voltage	V_{PWMINH}	0.75 x V_{VREG5}	-	V_{VREG5} + 0.2	V	
PWMIN Input Pin Low Voltage	V_{PWMINL}	-0.2	-	0.2 x V_{VREG5}	V	
[LOGIC Input (RX)]						
RX Input Pin High Voltage	V_{RXH}	0.75 x V_{VREG5}	-	V_{VREG5} + 0.2	V	
RX Input Pin Low Voltage	V_{RXL}	-0.2	-	0.2 x V_{VREG5}	V	
[LOGIC Output Block (PWMOUT)]						
Output High Voltage	V_{OUTH}	0.75 x V_{VREG5}	-	V_{VREG5} + 0.2	V	I_{PWMOUT} = -1 mA
Output Low Voltage	V_{OUTL}	-	-	0.2	V	I_{PWMOUT} = +1 mA
[LOGIC Output Block (TX) Block]						
Output High Voltage	V_{TXH}	0.75 x V_{VREG5}	-	V_{VREG5} + 0.2	V	I_{TX} = -1 mA
Output Low Voltage	V_{TXL}	-	-	0.2 x V_{VREG5}	V	I_{TX} = +1 mA
[FAILB Output Block]						
FAILB Pin ON Resistance	R_{FAILB}	0.30	0.65	1.00	kΩ	I_{FAILB} = +1 mA
FAILB Pin Leak Current	$I_{LEAKFAILB}$	-	-	10	µA	V_{FAILB} = 5.0 V
[MINSELV Input Pin]						
MINSELV Pin Input Current	$I_{MINSELV}$	-	-	10	µA	$V_{MINSELV}$ = 5.0 V
[PRESIGIN/DCDCPWMIN Input Pin]						
PRESIGIN Pin Input Current	$I_{PRESIGIN}$	20	50	100	µA	$V_{PRESIGIN}$ = 5.0 V
PRESIGIN Input Pin High Voltage	$V_{PRESIGINH}$	0.75 x V_{VREG5}	-	V_{VREG5} + 0.2	V	
PRESIGIN Input Pin Low Voltage	$V_{PRESIGINL}$	-0.2	-	0.2 x V_{VREG5}	V	
DCDCPWMIN Pin Input Current	$I_{DCDCPWMIN}$	20	50	100	µA	$V_{DCDCPWMIN}$ = 5.0 V
DCDCPWMIN Input Pin High Voltage	$V_{DCDCPWMINH}$	0.75 x V_{VREG5}	-	V_{VREG5} + 0.2	V	
DCDCPWMIN Input Pin Low Voltage	$V_{DCDCPWMINL}$	-0.2	-	0.2 x V_{VREG5}	V	

Typical Performance Curve

(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C, C_{VREG5} = 4.7 µF)

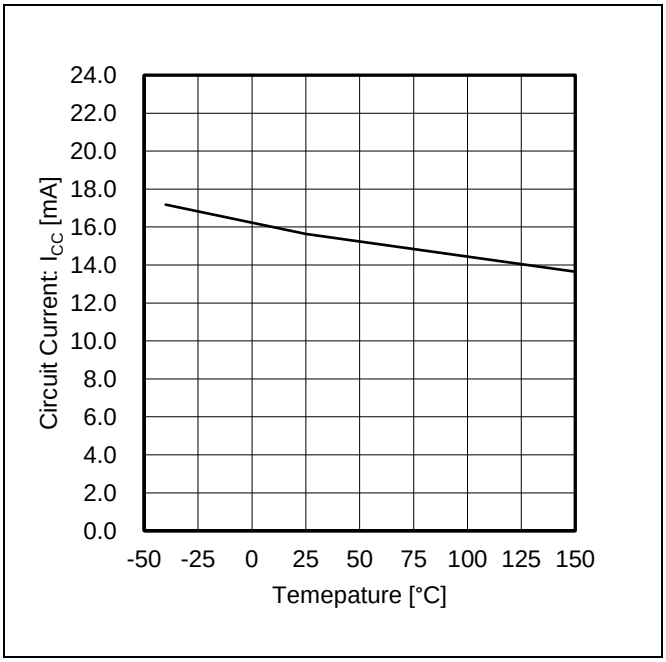


Figure 12. Circuit Current vs Temperature

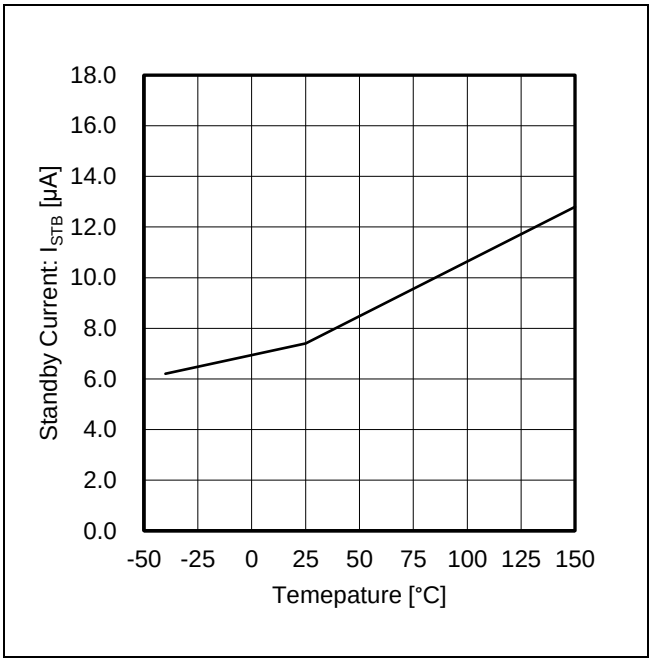
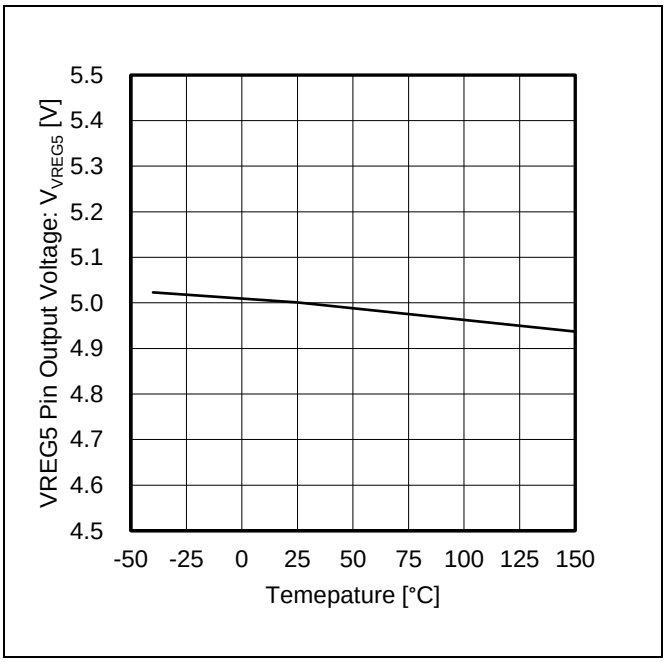


Figure 13. Standby Current vs Temperature



. Figure 14. VREG5 Pin Output Voltage vs Temperature

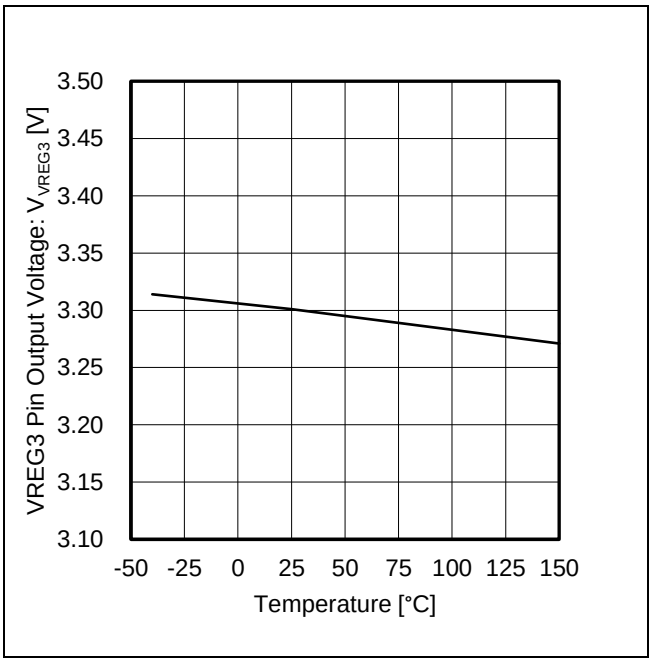


Figure 15. VREG3 Pin Output Voltage vs Temperature

Typical Performance Curve - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C, C_{VREG5} = 4.7 µF)

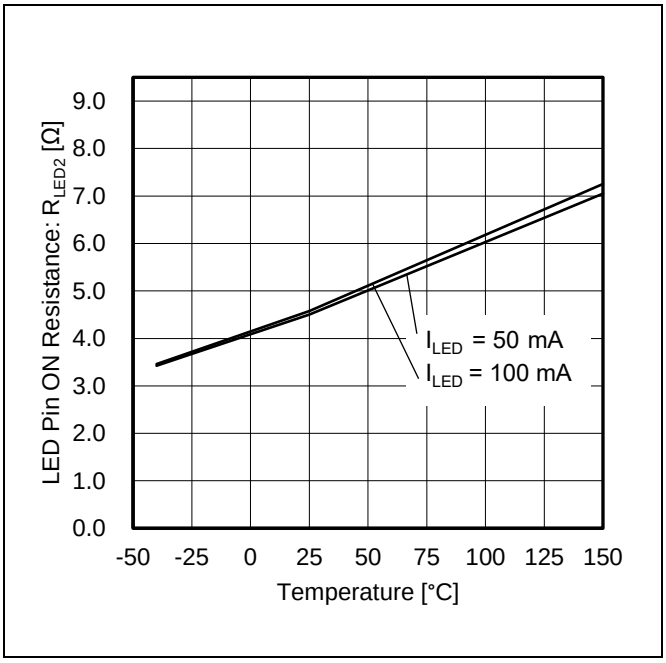


Figure 16. LED Pin ON Resistance vs Temperature

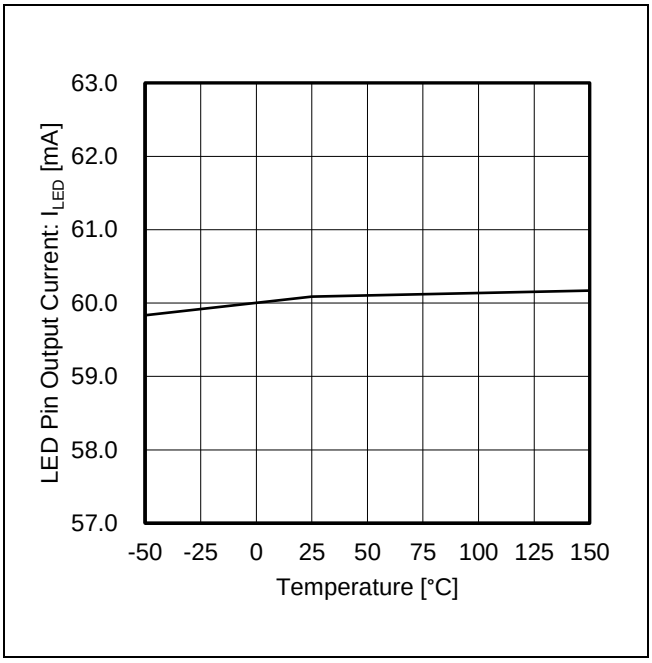


Figure 17. LED Pin Output Current vs Temperature

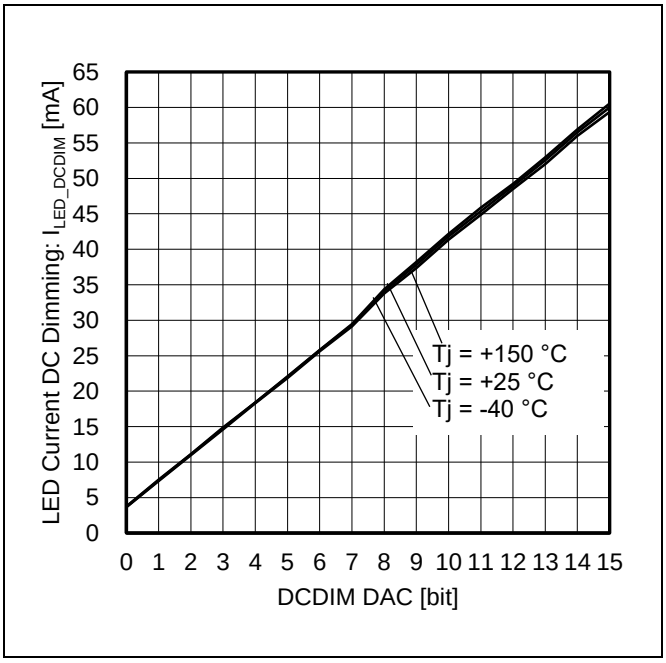


Figure 18. LED Current DC Dimming vs DCDIM DAC

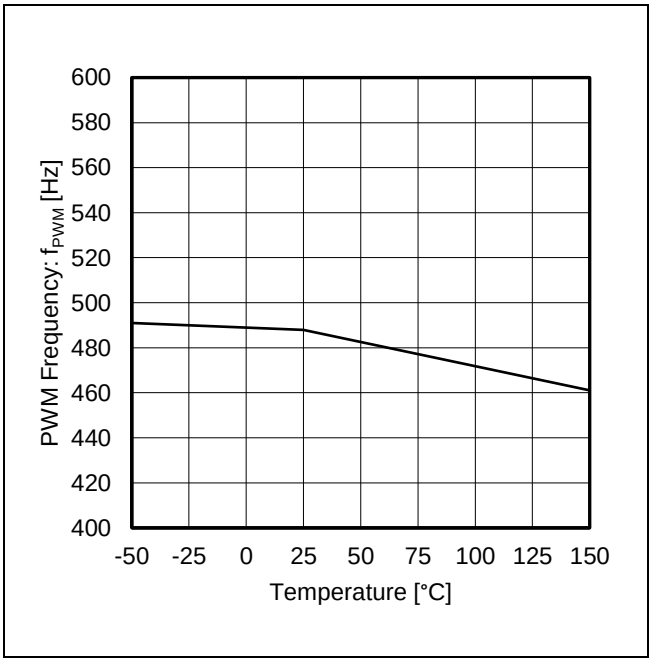


Figure 19. PWM Frequency vs Temperature

Typical Performance Curve - continued
(Unless otherwise specified V_{IN} = 13 V, Tj = -40 °C to +150 °C, C_{VREG5} = 4.7 µF)

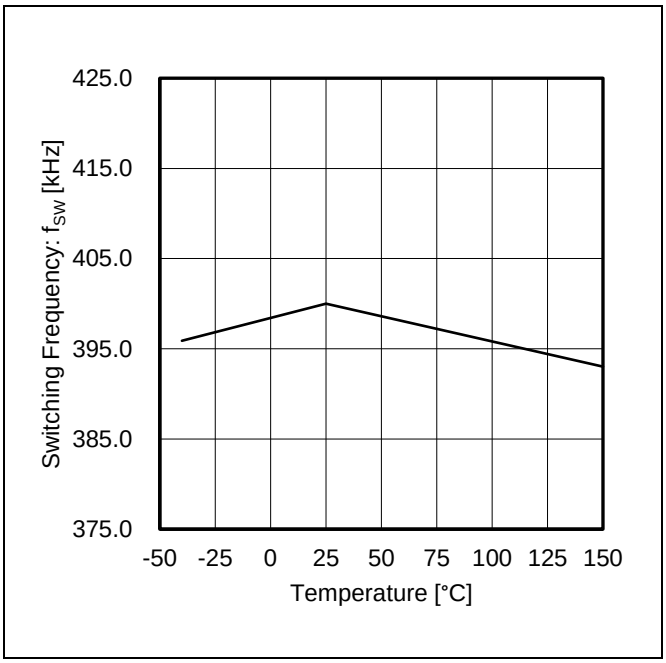


Figure 20. Switching Frequency vs Temperature

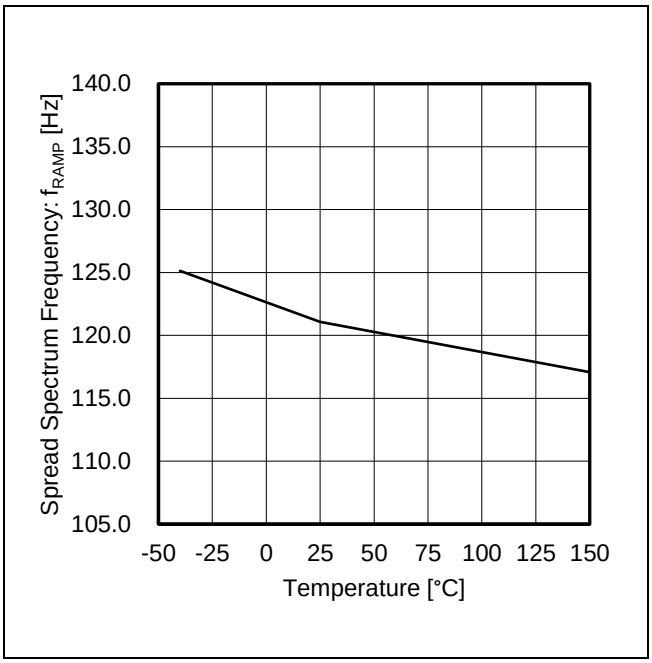


Figure 21. Spread Spectrum Frequency vs Temperature

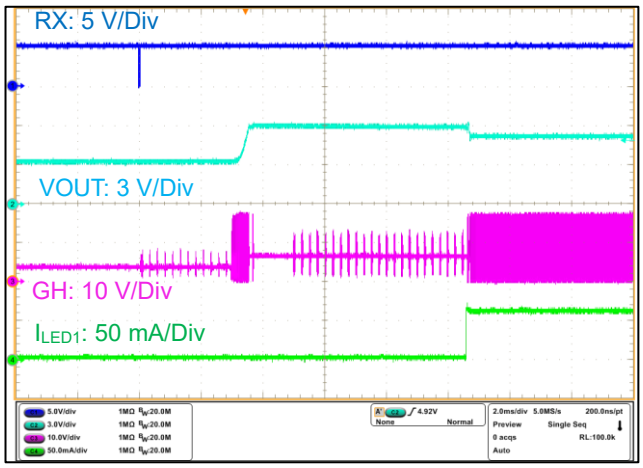


Figure 22. Start-up Function (PREBOOST)
(L = 10 µH, C_{OUT} = 40 µF, C_{BOOT} = 0.1 µF, R_{SENS} = 10 mΩ, R_{COMP} = 100 Ω, C_{COMP} = 15 nF, $R_{EXTISET1}$ = 120 kΩ)

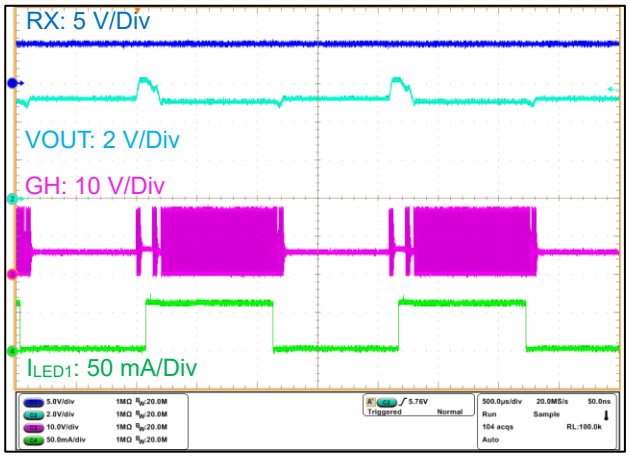


Figure 23. PWM Dimming Function (PREBOOST)
(L = 10 µH, C_{OUT} = 40 µF, C_{BOOT} = 0.1 µF, R_{SENS} = 10 mΩ, R_{COMP} = 100 Ω, C_{COMP} = 15 nF, $R_{EXTISET1}$ = 120 kΩ)

Functions of Logic Block

1. UART Protocol and AC Electrical Characteristics

This device has a UART Interface (Universal Asynchronous Receiver-Transmitter). This interface uses the RX (Receiver) and TX (Transmitter) pins for communication. The initial value of UART communication RX and TX is “High”. The format of a frame consists of 10-bit: start bit, 8-bit data and stop bit. Data is sent from LSB first to MSB last.

For read command, MCU must synchronize each frame of UART start bit and strobe data at 50 % to provide enough margin to ensure successful communication.

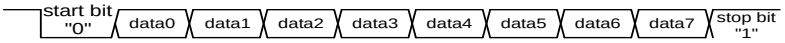


Figure 24. Data Format of a Frame

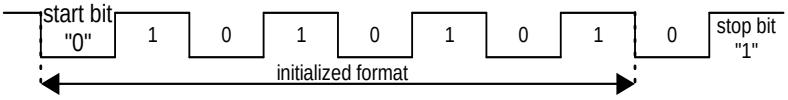


Figure 25. Clock Synchronization (SYNC)

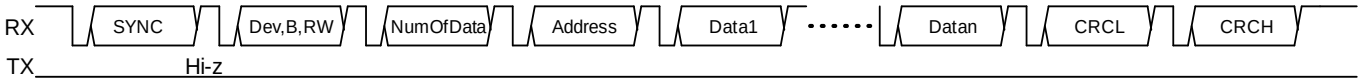


Figure 26. UART Protocol (WRITE)

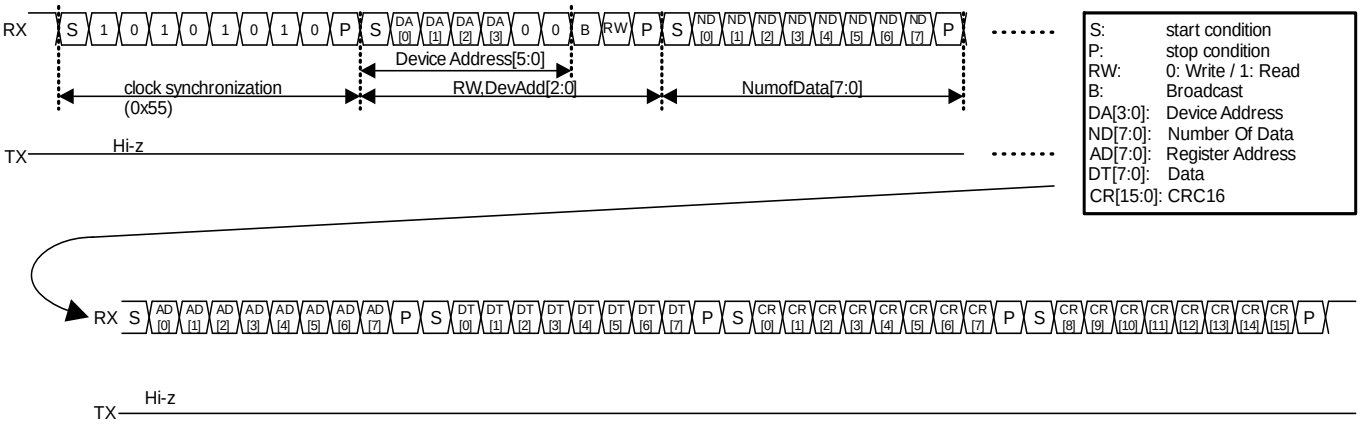


Figure 27. Detail of UART Protocol (WRITE)

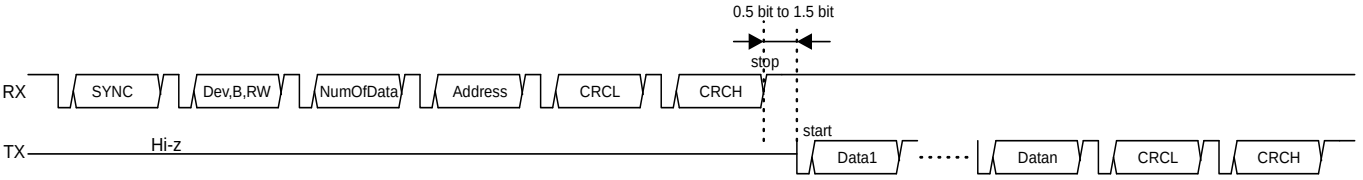


Figure 28. UART Protocol (READ)

Functions of Logic Block – continued

2. UART AC Timing

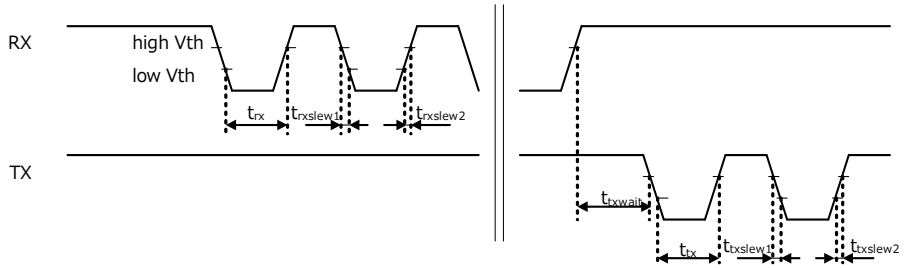


Figure 29. UART AC Timing

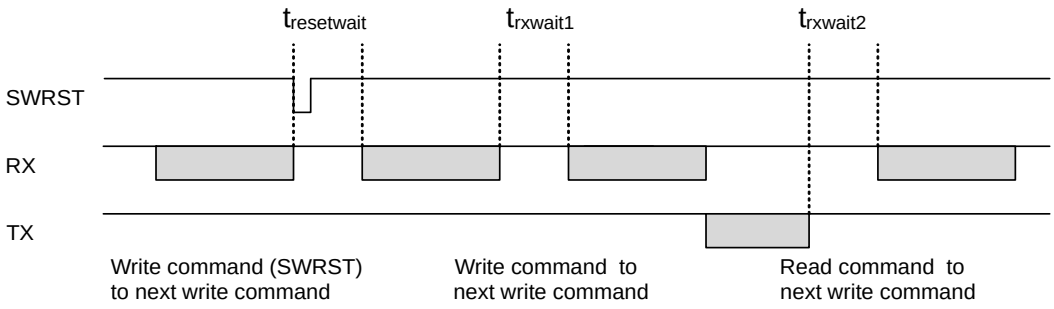


Figure 30. UART Inter-command Timing

Table 4. UART AC Characteristics
Recommended Operation Condition (Unless otherwise specified, V_{IN} =13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Rating			Unit	Comments
		Min	Typ	Max		
RX transfer time	t_{rx}	1.0	-	10.0	µs	
TX transfer time	t_{tx}	1.0	-	10.0	µs	
TX output delay time	t_{txwait}	0.5	1.0	1.5	bit	
RX slew rate High to Low	$t_{rxslew1}$	-	-	t_{rx} x 10 %	µs	
RX slew rate Low to High	$t_{rxslew2}$	-	-	t_{rx} x 10 %	µs	
TX slew rate High to Low	$t_{txslew1}$	-	-	t_{tx} x 10 %	µs	
TX slew rate Low to High	$t_{txslew2}$	-	-	t_{tx} x 10 %	µs	
RX to RX wait time	$t_{rxwait1}$	2.0	-	-	µs	The time interval between continuous write commands.
TX to RX wait time	$t_{rxwait2}$	2.0	-	-	µs	The time interval between read and write commands.
RX to RX wait after SWRST	$t_{resetwait}$	100	-	-	µs	The time required after the software reset write.

(Output load capacitance：15 pF)

Functions of Logic Block – continued

3 UART Protocol

3.1 Initialize Format

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	1	0	1	0	1	0	1

This interface receives SYNC frame 0x55h (0b01010101) to calculate the baudrate of the incoming UART command. It generates internal sampling time based on the computed baudrate (1-bit period / 2). After receiving the SYNC frame, this interface expects succeeding frames have the same baudrate as that of the SYNC frame. If incorrect input timing occurred, it may trigger communication error.

3.2 Device Address, Broadcast, Read/Write

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RW	B	DA[5:0]					

bit	Parameter	Function
DA[5:0]	Device Address	We can set from “0b000000” to “0b001111”. DA[0] = CS0 setting DA[1] = CS1 setting DA[2] = CS2 setting DA[3] = CS3 setting DA[4] = 0 DA[5] = 0

Note:
1. When the CSx (x = 0 to 3) pin are OPEN, DA[5:0] = 0b000000.
2. When the CSx pin short to GND, DA[n] is “High”, inverted operation. (n = 0 to 5)
3. When the CSx pin set to over 4.5 V (Typ), DA[n] is “Low”, inverted operation.

bit	Parameter	Function
B	Broadcast	0: Access the device that matched the device address 1: Access all devices connected to the UART line.

Note:
1. Broadcast is not possible for Read access.
2. If B = 1, device address setting is ignored.

bit	Parameter	Function
RW	Read/Write	0: Write access 1: Read access

3 UART Protocol – continued

3.3 Number of Data

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
NumOfData[7:0]							

bit	Parameter	Function
NumOfData [7:0]	Number of Data transferred	Available to use from 1 to 27.

Note:
1. Available data buffer for multiple write access is 27 data.
2. NumOfData = 0 is not valid.
3. NumOfData > 27 is not valid.

3.4 Register Address

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
RegAddr [7:0]							

bit	Parameter	Function
RegAddr [7:0]	Register Address	It is available to access from 0x00h to 0x5Eh.

3.5 Data

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Data [7:0]							

bit	Parameter	Value
Data [7:0]	Data	0x00h to 0xFFh.

3 UART Protocol – continued

3.6 CRC

16bit LSB First:
Cyclic Redundancy Check (CRC)
The CRC-16 is used to detect errors in the UART I/F Communication data.
The data included for CRC computation are the following: Device address, Number of Data, Address Data, Write or Read Data.

During write communication (both write and read command has write communication),
The last 2 frames received in a write communication is a 16-bit CRC data that will be compared to the computed CRC.
If CRC data is the same with the computed CRC, Register Map will be updated with all the written data.
Else, all written data will be disregarded, CRC Status Register becomes High and FAILB output becomes “Low”.

CRC Error is released after sending UART Write command with correct data (Matched CRC Calculation). UART Read command will not release CRC Error.

CRC Polynomial:
CRC Polynomial is expressed as
CRC16-IBM
$x^{16}+x^{15}+x^2+1$

Bit Order LSB First:
The CRC calculation starts with LSB and proceeds from bit[0] to bit[7] of each byte.

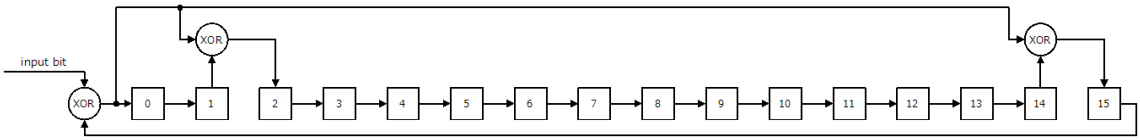


Figure 31. CRC Polynomial

CRC Initial Setting:
The initial value is “0x0000h”.
The CRC calculate registers are reset to the initial value of “0x0000h” prior to each CRC bytes calculation.

Example for

Figure 32. CRC Data Format

RW,B,DA[5:0]:	DA[7:0]	= 0x1Ah	to	DA[0:7] = 0x58h
NumOfData[7:0]:	ND[7:0]	= 0x02h	to	ND[0:7] = 0x40h
Address[7:0]:	AD[7:0]	= 0xA5h	to	AD[0:7] = 0xA5h
Data[7:0]:	DT[7:0]	= 0x5Ah	to	DT[0:7] = 0x5Ah
CRC Data[7:0]:	CR[7:0]	= 0xBAh	to	CR[0:7] = 0xB3h
CRC Data[15:8]:	CR[15:8]	= 0xCDh	to	CR[8:15] = 0x5Dh

3.6 CRC - continued

$X^{16} + X^{15} + X^2 + 1$
Initial Value: 0x0000
LSB First

Data MSB first	Data LSB first		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1A	58	[0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		[1]	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
		[2]	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1
		[3]	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
		[4]	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1
		[5]	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	1
		[6]	0	1	1	0	1	0	1	1	1	0	0	0	0	0	0	1
		[7]	0	1	1	0	0	1	0	1	1	1	0	0	0	0	0	1
				3				D				1				8		
02	40	[0]	0	1	1	0	0	0	1	0	1	1	1	0	0	0	0	1
		[1]	1	0	1	1	0	0	0	1	0	1	1	1	0	0	0	0
		[2]	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0	0
		[3]	0	0	0	0	1	1	0	0	0	1	0	1	1	1	0	0
		[4]	0	0	0	0	0	1	1	0	0	0	1	0	1	1	1	0
		[5]	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	0
		[6]	0	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1
		[7]	0	1	0	1	0	0	0	0	1	1	0	0	0	1	0	1
				5				8				1				5		
A5	A5	[0]	1	1	1	1	1	0	0	0	0	1	1	0	0	0	1	0
		[1]	0	0	1	1	1	1	0	0	0	0	1	1	0	0	0	1
		[2]	1	1	0	0	1	1	1	0	0	0	0	1	1	0	0	0
		[3]	0	0	1	0	0	1	1	1	0	0	0	0	1	1	0	0
		[4]	0	0	0	1	0	0	1	1	1	0	0	0	0	1	1	0
		[5]	1	1	0	1	1	0	0	1	1	1	0	0	0	0	1	1
		[6]	0	1	1	1	1	1	0	0	1	1	1	0	0	0	0	1
		[7]	1	1	1	0	1	1	1	0	0	1	1	1	0	0	0	0
				B				3				7				0		
5A	5A	[0]	0	0	1	1	0	1	1	1	0	0	1	1	1	0	0	0
		[1]	1	1	0	0	1	0	1	1	1	0	0	1	1	1	0	0
		[2]	0	1	1	1	0	1	0	1	1	1	0	0	1	1	1	0
		[3]	1	0	1	1	1	0	1	0	1	1	1	0	0	1	1	1
		[4]	1	1	0	0	1	1	0	1	0	1	1	1	0	0	1	1
		[5]	0	0	1	0	0	1	1	0	1	0	1	1	1	0	0	1
		[6]	1	0	0	1	0	0	1	1	0	1	0	1	1	1	0	0
		[7]	0	1	0	1	1	0	0	1	1	0	1	0	1	1	1	0
CRC:	BACD			D				C				A				B		

3. UART Protocol - continued

3.7 Example of UART Protocol

Single device, 1 byte Write (Write to Device #1)

(CS3, CS2, CS1, CS0) =	“0101”	
B =	0:	Target Device receives the data
DevAddr[5:0] =	0x05h:	Target Device Address
NumOfData[7:0] =	1:	1 byte Write mode
RW =	0:	Write
RegAddr[7:0] =	0x02h:	Address
Data[7:0] =	0xAAh:	Data

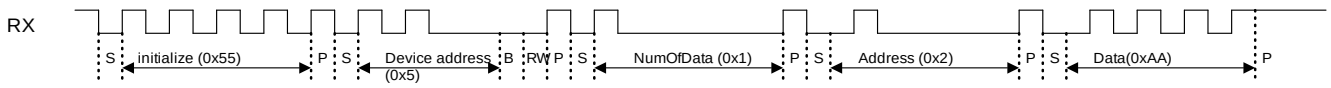


Figure 33. UART Protocol of the 1 byte Write to Device #1

4. Communication Reset

UART IF has a communication reset function. This function can be used to interrupt UART communication and return to idle condition. This function is triggered by setting RX to “High” for at least 2.75 ms (Typ). This feature can be used to recover from communication. If Communication Reset is executed, it will not affect LED Dimming. When UART is in IDLE condition it does not detect Communication Reset.

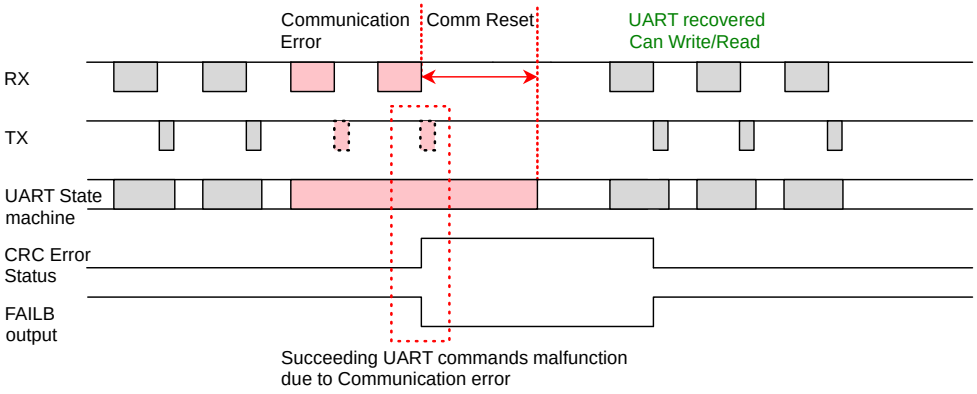


Figure 34. Communication Reset

5. Watchdog Timer (WDT)

UART IF has a watchdog timer function. This function monitors the RX line for no UART access for 100 ms (Typ) and notifies via status register and FAILB output. This no UART access means no successful UART command (no CRC OK). This function is enabled by WDTEN (initial is “Low”) and the status can be checked in WDTERR Status register and can be observed in the FAILB pin output. When detected, it returns the UART state to idle condition and does not affect LED Dimming. Details of the operation is further discussed in Error Control and Error Sequence.

When a device is connected in parallel and is not being accessed, it will not detect WDT.

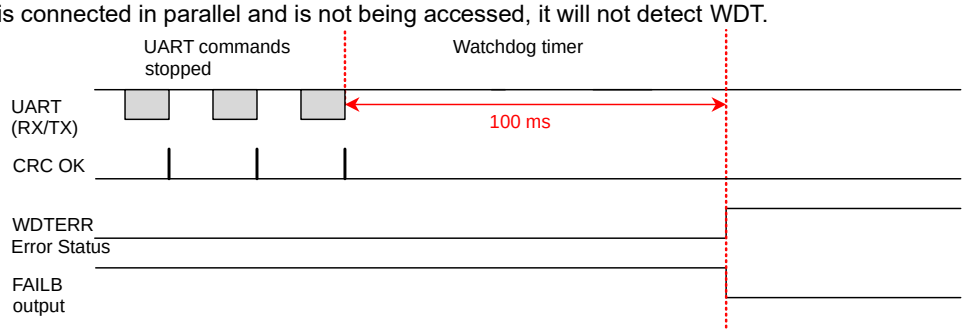


Figure 35. Watchdog Timer

Functions of Logic Block – continued

6. Register Map

Each register is updated at the 2 timings.
Reset Condition: “UVLO” condition = VREG3UVLO, VREG5UVLO, VINUVLO, TSD or EN is detected.
Register Update timing for control data:
A. Updated to the newest data immediately when the data is written.
B. Updated to the newest data when the next PWM (PWM is internal signal) timing after the data is written.

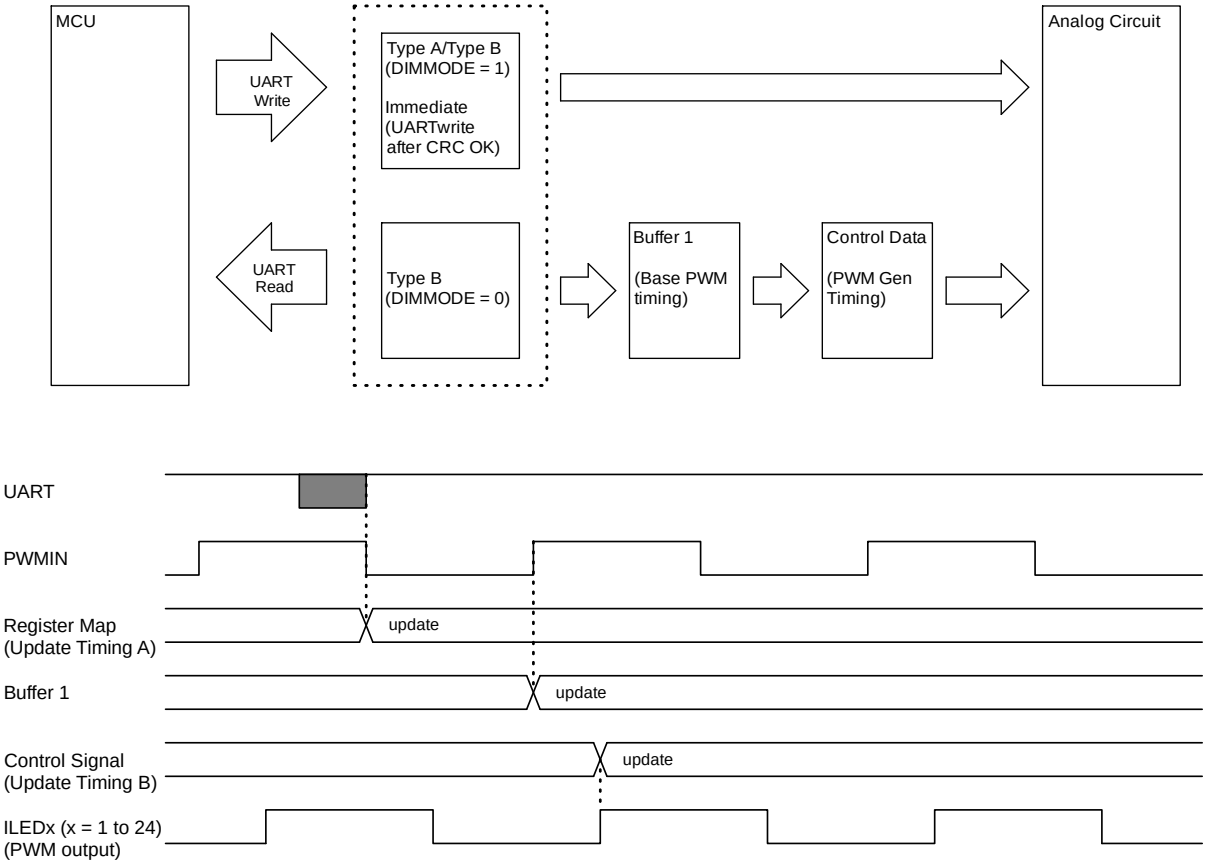


Figure 36. UART Data Flow

6. Register Map – continued

*Attention:
Please don't access (Write/Read) register except for following registers (0x00h to 0x5Eh) and write "0" in "-".
"RESERVED" Registers can be written/read. Do not update.

Address 0x00h to 0x23h (1/3)

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	initial	Reset Condition	update timing	comments
SYNC	0x00	DCDCSLSW	PWMTIM(Note 2)	ISETSEL	SLOPEEN	DIMMODE	PWMPSYNC(Note 1)	DIMSTART	SWRST(Note 1)	R/W	0x00	UVLO or SWRST	Type A	PWM phase syncronization and output
SYSSET1	0x01	FAILBCNT	FAILBEN	SSFM[2:0]			PWMFSYNC(Note 2)	SYNCSET[1:0]		R/W	0x00	UVLO or SWRST	Type A	PWM frequency synchronous setting and SSCG enable, FAILB control setting
SYSSET2	0x02	OVDVOLT[3:0]				PREBOOST[3:0]				R/W	0x00	UVLO or SWRST	Type A	Pre-Feedback voltage setting
SYSSET3	0x03	ERRMASK[3:0]				SSMASK[3:0]				R/W	0x00	UVLO or SWRST	Type A	Error mask for LED open/short, Error mask setting during softstart
LEDENL	0x04	LEDEN[7:0]								R/W	0x00	UVLO or SWRST	Type A	Channel enable for LED1 to LED8
LEDENM	0x05	LEDEN[15:8]								R/W	0x00	UVLO or SWRST	Type A	Channel enable for LED9 to LED16
LEDENH	0x06	LEDEN[23:16]								R/W	0x00	UVLO or SWRST	Type A	Channel enable for LED17 to LED24
SYSSET4	0x07	-	ISETLAT	AUTOOFF	ERRCLR(Note 1)	OCPLAT	CRCERLAT	LSHLAT	LOPLAT	R/W	0x00	UVLO or SWRST	Type A	Error status and flag latch setting
SYSSET5	0x08	-	-	SWOCPEN	OCPEN	CATHEN(Note 1)	TSDWEN	WDTEN	LOPEN	R/W	0x00	UVLO or SWRST	Type A	error enable CATHEN returns '0' automatically
LEDSHENL	0x09	LSHEN[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short enable
LEDSHENH	0x0A	-	-	ISETSHCNT[1:0]		LSHEN[11:8]				R/W	0x20	UVLO or SWRST	Type A	LED short enable, OCP current setting
LEDSHTH0102	0x0B	LEDSHTH0102[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED1 and LED2
LEDSHTH0304	0x0C	LEDSHTH0304[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED3 and LED4
LEDSHTH0506	0x0D	LEDSHTH0506[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED5 and LED6
LEDSHTH0708	0x0E	LEDSHTH0708[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED7 and LED8
LEDSHTH0910	0x0F	LEDSHTH0910[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED9 and LED10
LEDSHTH1112	0x10	LEDSHTH1112[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED11 and LED12
LEDSHTH1314	0x11	LEDSHTH1314[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED13 and LED14
LEDSHTH1516	0x12	LEDSHTH1516[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED15 and LED16
LEDSHTH1718	0x13	LEDSHTH1718[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED17 and LED18
LEDSHTH1920	0x14	LEDSHTH1920[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED19 and LED20
LEDSHTH2122	0x15	LEDSHTH2122[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED21 and LED22
LEDSHTH2324	0x16	LEDSHTH2324[7:0]								R/W	0x00	UVLO or SWRST	Type A	LED short detection voltage for LED23 and LED24
DENVOLT	0x17	LLSDAC[1:0]		PWMFREQ[1:0]		DENVOLT[3:0]				R/W	0x00	UVLO or SWRST	Type A	DEN threshold voltage
PWMDLY0102	0x18	PWMDLY02[3:0]				PWMDLY01[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED1 and LED2
PWMDLY0304	0x19	PWMDLY04[3:0]				PWMDLY03[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED3 and LED4
PWMDLY0506	0x1A	PWMDLY06[3:0]				PWMDLY05[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED5 and LED6
PWMDLY0708	0x1B	PWMDLY08[3:0]				PWMDLY07[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED7 and LED8
PWMDLY0910	0x1C	PWMDLY10[3:0]				PWMDLY09[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED9 and LED10
PWMDLY1112	0x1D	PWMDLY12[3:0]				PWMDLY11[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED11 and LED12
PWMDLY1314	0x1E	PWMDLY14[3:0]				PWMDLY13[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED13 and LED14
PWMDLY1516	0x1F	PWMDLY16[3:0]				PWMDLY15[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED15 and LED16
PWMDLY1718	0x20	PWMDLY18[3:0]				PWMDLY17[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED17 and LED18
PWMDLY1920	0x21	PWMDLY20[3:0]				PWMDLY19[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED19 and LED20
PWMDLY2122	0x22	PWMDLY22[3:0]				PWMDLY21[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED21 and LED22
PWMDLY2324	0x23	PWMDLY24[3:0]				PWMDLY23[3:0]				R/W	0x00	UVLO or SWRST	Type A	PWM delay setting for LED23 and LED24

WO: Write Only, RO: Read Only, R/W: Read and Write

(Note 1) PWMPSYNC, CATHEN, SWRST and ERRCLR are "write only", and reset condition of SWRST is only "UVLO/TSD."
(Note 2) PWMTIM and PWMFSYNC are read-only Registers.

6. Register Map – continued

Address 0x24h to 0x51h (2/3)

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	initial	Reset Condition	update timing	comments
DCDIM0102	0x24	DCDIM02[3:0]				DCDIM01[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED1 and LED2 in PWM mode
DCDIM0304	0x25	DCDIM04[3:0]				DCDIM03[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED3 and LED4 in PWM mode
DCDIM0506	0x26	DCDIM06[3:0]				DCDIM05[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED5 and LED6 in PWM mode
DCDIM0708	0x27	DCDIM08[3:0]				DCDIM07[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED7 and LED8 in PWM mode
DCDIM0910	0x28	DCDIM10[3:0]				DCDIM09[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED9 and LED10 in PWM mode
DCDIM1112	0x29	DCDIM12[3:0]				DCDIM11[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED11 and LED12 in PWM mode
DCDIM1314	0x2A	DCDIM14[3:0]				DCDIM13[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED13 and LED14 in PWM mode
DCDIM1516	0x2B	DCDIM16[3:0]				DCDIM15[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED15 and LED16 in PWM mode
DCDIM1718	0x2C	DCDIM18[3:0]				DCDIM17[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED17 and LED18 in PWM mode
DCDIM1920	0x2D	DCDIM20[3:0]				DCDIM19[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED19 and LED20 in PWM mode
DCDIM2122	0x2E	DCDIM22[3:0]				DCDIM21[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED21 and LED22 in PWM mode
DCDIM2324	0x2F	DCDIM24[3:0]				DCDIM23[3:0]				R/W	0xFF	UVLO or SWRST	Type A	DC Dimming setting for LED23 and LED24 in PWM mode
PWMOUTL	0x30	PWMOUTEN[7:0]								R/W	0x00	UVLO or SWRST	Type B	pwm output enable for LED1 to LED8 in PWM mode
PWMOUTM	0x31	PWMOUTEN[15:8]								R/W	0x00	UVLO or SWRST	Type B	pwm output enable for LED9 to LED16 in PWM mode
PWMOUTH	0x32	PWMOUTEN[23:16]								R/W	0x00	UVLO or SWRST	Type B	pwm output enable for LED17 to LED24 in PWM mode
PWMDTY01	0x33	DIMSET01[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED1
PWMDTY02	0x34	DIMSET02[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED2
PWMDTY03	0x35	DIMSET03[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED3
PWMDTY04	0x36	DIMSET04[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED4
PWMDTY05	0x37	DIMSET05[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED5
PWMDTY06	0x38	DIMSET06[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED6
PWMDTY07	0x39	DIMSET07[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED7
PWMDTY08	0x3A	DIMSET08[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED8
PWMDTY09	0x3B	DIMSET09[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED9
PWMDTY10	0x3C	DIMSET10[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED10
PWMDTY11	0x3D	DIMSET11[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED11
PWMDTY12	0x3E	DIMSET12[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED12
PWMDTY13	0x3F	DIMSET13[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED13
PWMDTY14	0x40	DIMSET14[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED14
PWMDTY15	0x41	DIMSET15[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED15
PWMDTY16	0x42	DIMSET16[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED16
PWMDTY17	0x43	DIMSET17[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED17
PWMDTY18	0x44	DIMSET18[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED18
PWMDTY19	0x45	DIMSET19[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED19
PWMDTY20	0x46	DIMSET20[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED20
PWMDTY21	0x47	DIMSET21[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED21
PWMDTY22	0x48	DIMSET22[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED22
PWMDTY23	0x49	DIMSET23[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED23
PWMDTY24	0x4A	DIMSET24[7:0]								R/W	0x00	UVLO or SWRST	Type B	PWM On Duty in PWM mode or DC Dimming setting in DC mode for LED24
LSHERRL	0x4B	LSHERR[7:0]								RO	0x00	UVLO or SWRST	Type A	status of "LED short error" for LED1 to LED8
LSHERRM	0x4C	LSHERR[15:8]								RO	0x00	UVLO or SWRST	Type A	status of "LED short error" for LED9 to LED16
LSHERRH	0x4D	LSHERR[23:16]								RO	0x00	UVLO or SWRST	Type A	status of "LED short error" for LED17 to LED24
LOPERRL	0x4E	LOPERR[7:0]								RO	0x00	UVLO or SWRST	Type A	status of "LED open error" for LED1 to LED8
LOPERRM	0x4F	LOPERR[15:8]								RO	0x00	UVLO or SWRST	Type A	status of "LED open error" for LED9 to LED16
LOPERRH	0x50	LOPERR[23:16]								RO	0x00	UVLO or SWRST	Type A	status of "LED open error" for LED17 to LED24
UVLOERR	0x51	ISETSHERR	SWOCPERR	OCPERR	CATHERR	TSDWERR	WDTERR	CRCERR	UVLOTSDERR	RO	0x01	UVLO or SWRST	Type A	UVLO or TSD Error, CRC Error, WDT Error. Cathode short error, OCP Error status

WO: Write Only, RO: Read Only, R/W: Read and Write

6. Register Map – continued

Address 0x52h to 0x5Eh (3/3)

Register Name	Address	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	Register Access	initial	Reset Condition	update timing	comments
LHDTY0102	0x52	LHDTY02[3:0]				LHDTY01[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED01 and LED02
LHDTY0304	0x53	LHDTY04[3:0]				LHDTY03[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED03 and LED04
LHDTY0506	0x54	LHDTY06[3:0]				LHDTY05[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED05 and LED06
LHDTY0708	0x55	LHDTY08[3:0]				LHDTY07[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED07 and LED08
LHDTY0910	0x56	LHDTY10[3:0]				LHDTY09[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED09 and LED10
LHDTY1112	0x57	LHDTY12[3:0]				LHDTY11[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED11 and LED12
LHDTY1314	0x58	LHDTY14[3:0]				LHDTY13[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED13 and LED14
LHDTY1516	0x59	LHDTY16[3:0]				LHDTY15[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED15 and LED16
LHDTY1718	0x5A	LHDTY18[3:0]				LHDTY17[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED17 and LED18
LHDTY1920	0x5B	LHDTY20[3:0]				LHDTY19[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED19 and LED20
LHDTY2122	0x5C	LHDTY22[3:0]				LHDTY21[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED21 and LED22
LHDTY2324	0x5D	LHDTY24[3:0]				LHDTY23[3:0]				R/W	0xFF	UVLO or SWRST	Type A	Duty Setting of PWM for Stand Alone Mode for LED23 and LED24
LIMPHOME	0x5E	-	-	-	-	-	-	LEXTISET2SEL	LIMPHEN	R/W	0x03	UVLO or SWRST	Type A	LIMP HOME setting

WO: Write Only, RO: Read Only, R/W: Read and Write

Description of Registers

Address 0x00h: SYNC Setting of PWM phase synchronized for all device[Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	DCDCSLSW	PWMTIM	ISETSEL	SLOPEEN	DIMMODE	PWMPSYNC	DIMSTART	SWRST
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.
PWMPSYNC and SWRST registers return to “0” automatically.

bit[7] DCDCSLSW
This register is control the DCDC operation mode.
Please set this register in initial setting.

Table 5. DCDCSLSW Setting

DCDCSLSW	DCDC operation
0	Diode Rectification Mode
1	Synchronous Rectification Mode

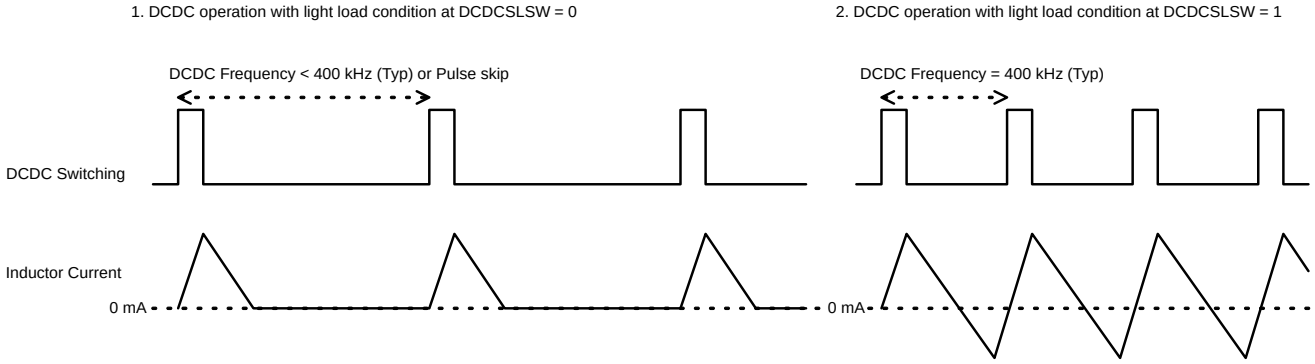


Figure 37. DCDCSLSW Function at Light Load Condition

bit[6] PWMTIM
This register is controlled as following figure. This register is read-only.

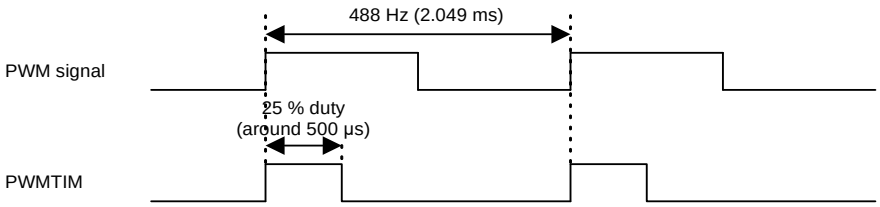


Figure 38. PWMTIM Image

This function can be used for synchronizing MCU (sending UART) and Device (LED Dimming).
MCU executes register polling to PWMTIM register continuously until PWMTIM is High is detected and then it will send succeeding UART commands for LED Dimming for maximum of 16 devices. The number of devices that can be updated per successful register poll is dependent on PWMFREQ register setting.

Consider the example in Figure 39 and Figure 40.

Address 0x00h: SYNC - continued

CASE1: PWMFREQ = 0h (488 Hz), Around 2000 µs period, UART Baudrate = 1 Mbps, Max data per UART transaction is 27. MCU wants to send data during 1 PWM cycle.

Total duration is 300 µs per UART transaction.
(2000 µs to 500 µs (polling time)) / 300 µs = 4 to 5 devices (considering tolerance)

For High Sampling,

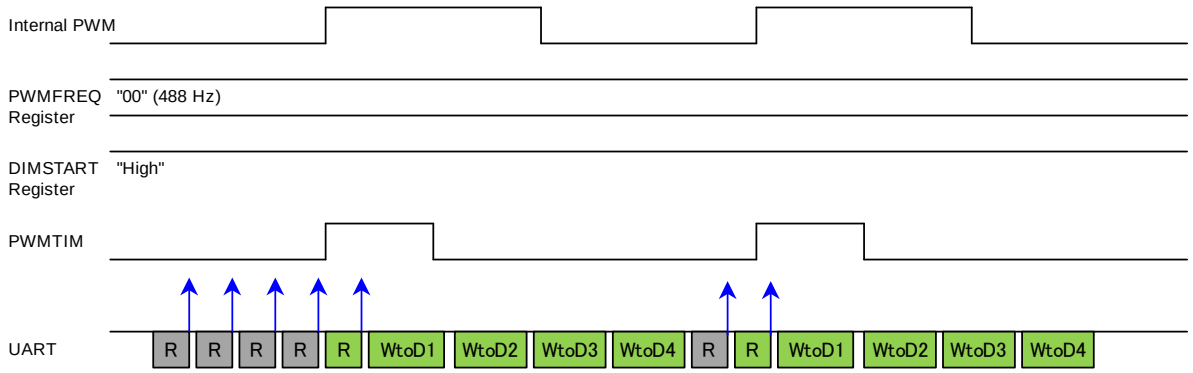


Figure 39. High Sampling UART Access Using PWMTIM Register

For Low Sampling,

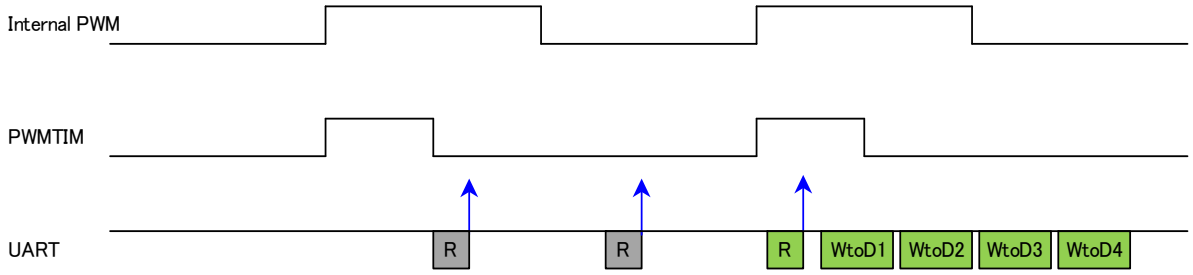


Figure 40. Low Sampling UART Access Using PWMTIM Register

Where:

R – Read Command for PWMTIM
WtoDn – Write to Device (n = device number)

For the number of devices that can be written based on the PWMFREQ setting, please refer to the table below.
This is considered at typical operating frequency 18 MHz (Typ) and 1 Mbps baudrate for UART.

Table 6. PWM Frequency Setting

PWMFREQ	PWM frequency (Hz)	Number of devices can be accessed
0	488	4 to 5
1	976	2 to 3
2	1952	1
3	3904	Cannot be used

Address 0x00h: SYNC - continued

bit[5] ISETSEL
Please set this register in initial setting.

Table 7. LED Current Setting

ISETSEL	LED Current setting
0	LED current is controlled by internal circuit. ISET Short (ISETSHERR) protection detection is disabled.
1	LED current is controlled by a resistor in the EXTISET1 pin. EXTISET1 Short (ISETSHERR) protection detection is enabled. This register setting does not release the protection status when it is already detected.

bit[4] SLOPEEN
Slope enable setting for DC Dimming Mode.
Please set this register in initial setting.

Table 8. SLOPE Setting for DC Dimming

SLOPEEN	Slope setting
0	Disabled
1	Enabled

SLOPEEN function is available only in DC Dimming mode (DIMMODE = 1).

For SLOPEEN = 0,

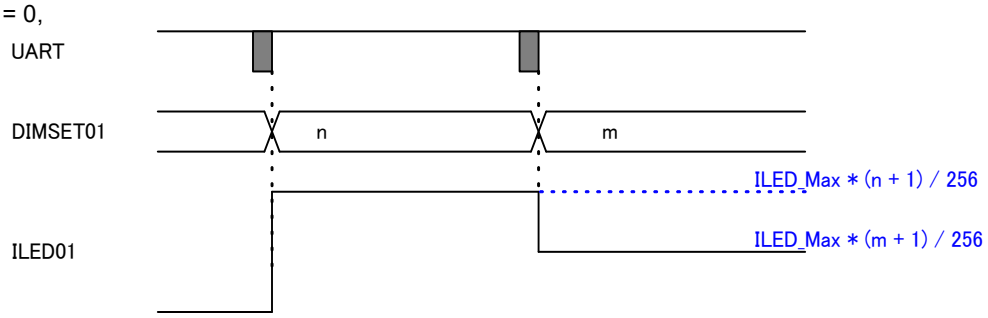


Figure 41. DC Dimming When SLOPEEN “Disabled”

For SLOPEEN = 1,

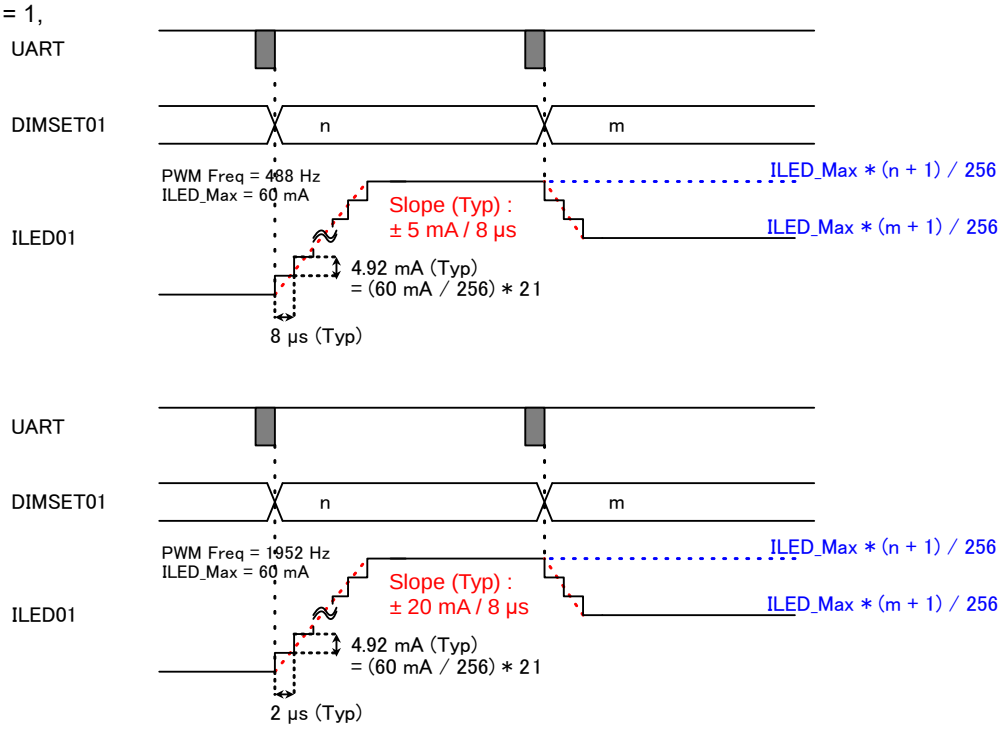


Figure 42. DC Dimming When SLOPEEN “Enabled”

Address 0x00h: SYNC - continued

bit[3] DIMMODE Dimming mode select setting

Table 9. DIMMODE Select Setting

DIMMODE	Dimming mode	Normal Dimming		LIMPHOME Mode	
		PWM duty for each channel	DC current for each channel	PWM duty for each channel	DC current for each channel
0	PWM dimming mode	DIMSETx register	DCDIMx register	LHDTYx register	DCDIMx register
1	DC dimming mode	100 % fixed	DIMSETx register	LHDTYx register	

Please refer to DCDIMx, DIMSETx and LHDTYx for description of register. (x = 01 to 24)

bit[2] PWMPSYNC PWM phase synchronous setting

Table 10. PWMPSYNC Setting

PWMPSYNC	Counter for PWM Generator
0	Not synchronize
1	Synchronize phase of PWM counter by this register setting

This function synchronizes the phase of the PWM output between multiple devices. When this function is used in a single device, it will initialize the phase of the PWM output based on the UART access time. Please send PWMPSYNC when clock is already synchronized (PWMFSYNC = 0).

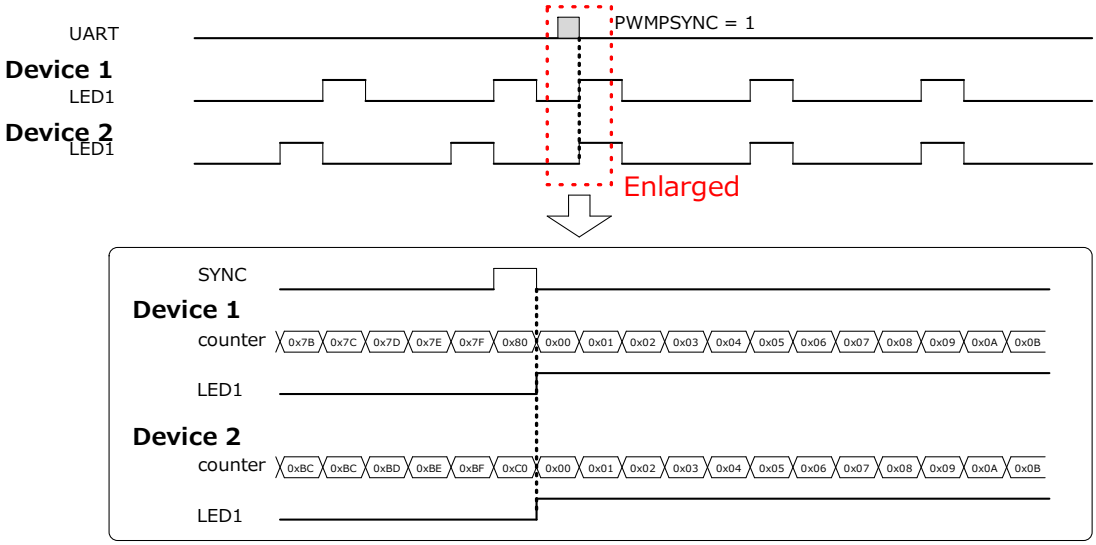


Figure 43. SYNC Register Setting Function

bit[1] DIMSTART Dimming start setting.

Table 11. DIMSTART Setting

DIMSTART	PWM Generator for LED dimming
0	OFF
1	Start the operation of DC/DC and Current Driver.

bit[0] SWRST Software reset setting.
Please set this register when you want to reset digital circuit.

Table 12. SWRST Description

SWRST	Reset
0	Normal
1	Synchronous reset for digital circuit (Automatically returns to “0”)

Description of Registers - continued

Address 0x01h: SYSSET1 system setting1 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	FAILBCNT	FAILBEN	SSFM[2:0]			PWMFSYNC	SYNCSET[1:0]	
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit[7] FAILBCNT
bit[6] FAILBEN

Please set this register in initial setting.

Table 13. FAILBEN and FAILBCNT Description

FAILBEN	Operation
0	FAILB output is controlled by error status.
1	FAILB output is controlled by FAILBCNT.

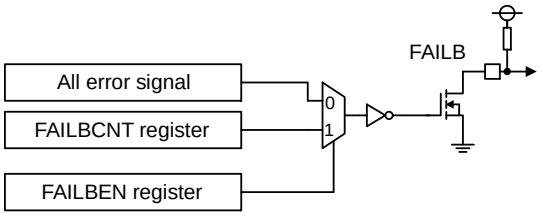


Figure 44. FAILB Controlled Circuit Image

bit[5:3] SSFM[2:0]
This register controls SSCG ON/OFF for DC/DC.

Table 14. SSFM Setting

SSFM[2:0]	CLK_SSM	SSCG modulation ratio
0	SSCG OFF (fixed frequency of DC/DC)	
1	15.625 kHz	122.1 Hz
2	17.578 kHz	137.3 Hz
3	20.089 kHz	156.9 Hz
4	23.438 kHz	183.1 Hz
5	28.125 kHz	219.7 Hz
6	35.156 kHz	274.7 Hz
7	46.875 kHz	366.2 Hz

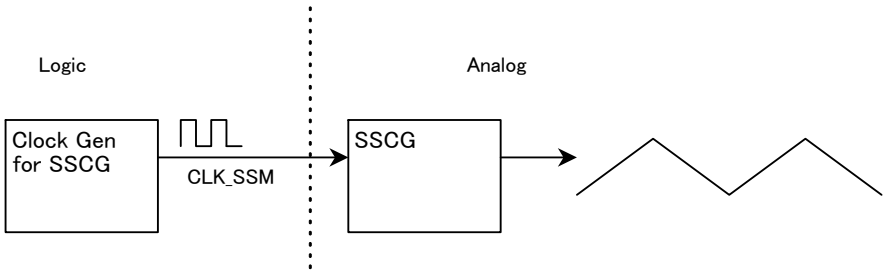


Figure 45. SSCG Structure

Address 0x01h: SYSSET1 - continued

bit[2] PWMFSYNC

This is a read-only register. When device is set as Follower (SYNCSET = 10b or 11b) it monitors if the internal clock of the Follower device is synchronized to the Leader device. It synchronizes internal clock using the PWMIN input from Leader device. When PWMIN input clock is stable and no UART communication during synchronization, Follower device can synchronize around 10 ms (Max) for PWMFSYNC = “Low” and 20 ms (Max) for PWMFSYNC = “High”. In the event that PWMIN frequency changes, PWMFSYNC becomes High until stable condition is achieved.

When device is set as Leader, this register is fixed to “0”. When device is set as Follower and there is no PWMIN input, this register is “High” until PWMIN input is present and clock is synchronized.

Table 15. PWMFSYNC Description

PWMFSYNC	Operation
0	Internal clock is stable
1	Internal clock is not stable

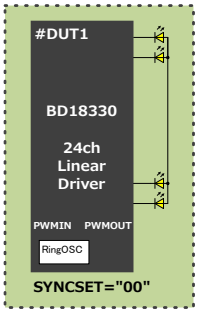


Figure 46. SYNCSET setting for Stand Alone

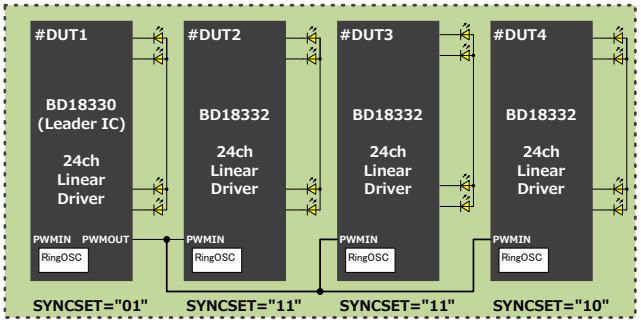


Figure 47. SYNCSET setting for multiple connection

bit[1:0] SYNCSET[1:0]

Use this register to select if device is Stand Alone, Leader or Follower.
Please set this register in initial setting.

Table 16. PWMIN/PWMOUT Setting

SYNCSET[1:0]	PWMIN Port	PWMOUT Port	PWM adjusting	Comment
00	Disable	Disable	Disable	Stand Alone
01	Disable	Enable (PWM output)	Disable	Leader device
10	Enable	Disable	Enable	Follower device
11	Enable	Enable (PWM output)	Enable	Follower device

Description of Registers - continued

Address 0x02h: SYSSET2 system setting2 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	OVDVOLT[3:0]				PREBOOST [3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: immediately

bit[7:4] OVDVOLT[3:0]
Control PREBOOST and OVD protection voltage register setting.

Table 17. OVDVOLT Setting

OVDVOLT[3:0]	PREBOOST and OVD protection voltage [V]
0x0	5.0
0x1	
0x2	
0x3	
0x4	
0x5	
0x6	6.0
0x7	7.0
0x8	8.0
0x9	9.0
0xA	10.0
0xB	11.0
0xC	12.0
0xD	13.0
0xE	14.0
0xF	15.0

bit[3:0] PREBOOST[3:0]
Control PREBOOST time register setting.

Table 18. PREBOOST Time Setting

PREBOOST[3:0]	Time [µs]
0x0h	8
0x1h	16
0x2h	24
0x3h	32
0x4h	40
0x5h	48
0x6h	56
0x7h	64
0x8h	72
0x9h	80
0xAh	88
0xBh	96
0xCh	104
0xDh	112
0xEh	120
0xFh	128

Address 0x02: SYSSET2 - continued

For PWM dimming (DIMMODE = “0”), generate PREBOOST signal based on PREBOOST register value. This signal is generated before DCDCPWM output timing. If PWM duty is 100 % generate only at 1st rising edge.

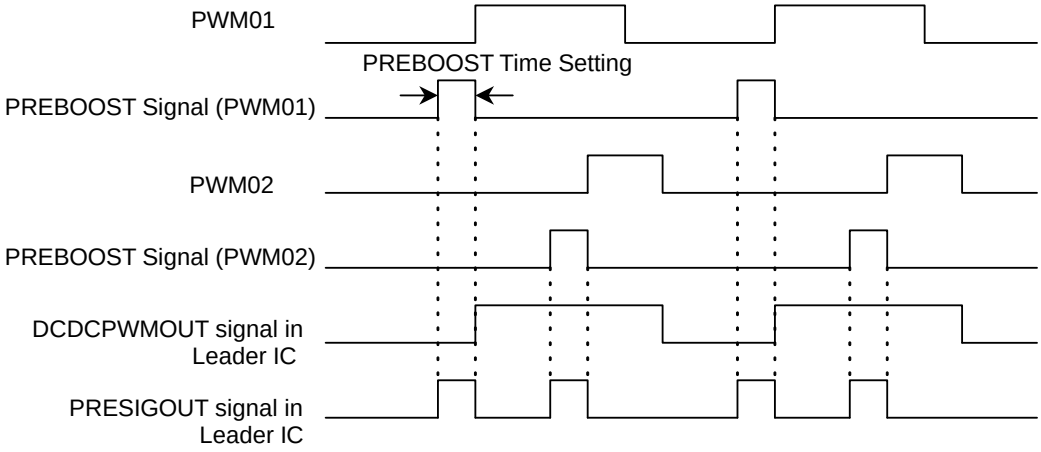


Figure 48. PREBOOST Operation for DIMMODE = 0

For DC dimming (DIMMODE = “1”), generate PREBOOST signal based on PREBOOST register value. This pulse is generated every DC Dimming update via UART(DIMSET) when next DC Dimming value is Higher than the previous value.

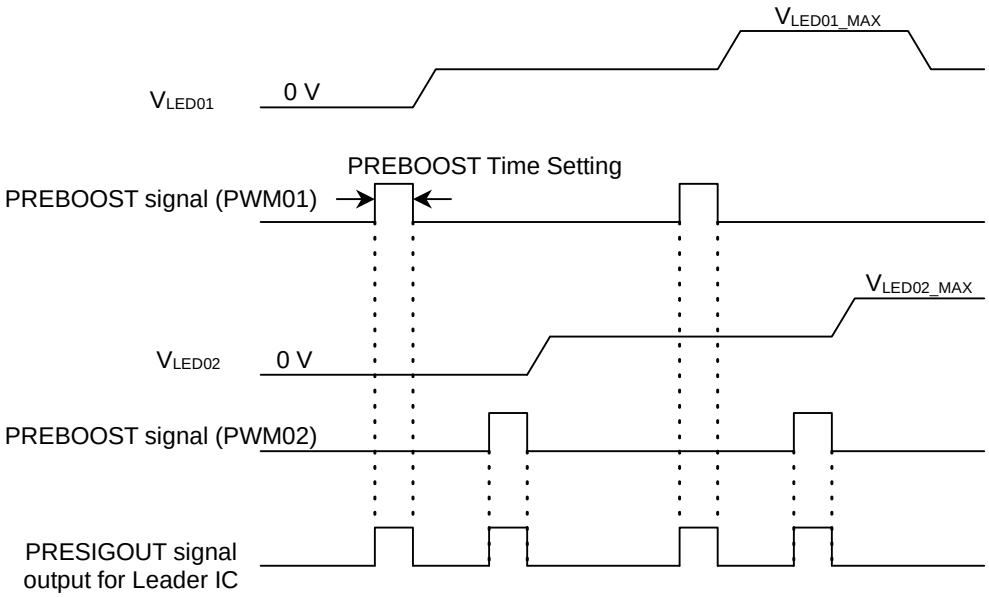


Figure 49. PREBOOST Operation for DIMMODE = 1

Description of Registers - continued

Address 0x03h: SYSSET3 system setting3 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ERRMASK[3:0]				SSMASK[3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

bit [7:4] ERRMASK[3:0]
Configurable mask time for “LED open protection”. If the protection detection time is more than this value, the corresponding protection is detected. Protection is detected in status register and FAILB output after 1 or 2 clock (1.125 MHz) cycles. Please set this register in initial setting.

Table 19. ERRMASK Setting

ERRMASK[3:0]	Mask time [µs]
0x0h to 0x1h	1.8
0x2h	3.6
0x3h	5.3
0x4h	7.1
0x5h	8.9
0x6h	10.7
0x7h	12.4
0x8h	14.2
0x9h	16.0
0xAh	17.8
0xBh	19.6
0xCh	21.3
0xDh	23.1
0xEh	24.9
0xFh	26.7

bit[3:0] SSMASK[3:0]
This setting mask “LED open protection” and “LED short protection” at start-up operation.
The mask time is based on the protection detection time. SSMASK indicates the Soft-start duration.
During soft start LED Open and LED Short Protection is masked. After soft-start protection detection will be available. Please refer timing chart of “Soft start masking function”.

Table 20. SSMASK Setting

SSMASK[3:0]	SSMASK time [ms]
0x0	-
0x1	0.68
0x2	1.36
0x3	1.81
0x4	2.49
0x5	3.17
0x6	3.85
0x7	4.31
0x8	4.99
0x9	5.67
0xA	6.12
0xB	6.80
0xC	7.48
0xD	8.16
0xE	8.61
0xF	9.29

Description of Registers – continued

Address 0x04h: LEDENL LED channel enable1 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LEDEN[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: immediately

Address 0x05h: LEDENM LED channel enable2 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LEDEN[15:8]							
Initial value	0	0	0	0	0	0	0	0

Update: immediately

Address 0x06h: LEDENH LED channel enable3 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LEDEN[23:16]							
Initial value	0	0	0	0	0	0	0	0

Update: immediately

These data in register are updated to the newest data immediately when the new data is written.

This registers control enable/disable each LED channel. For enable control, the LED Channel outputs according to the setting of PWM Duty Setting. For disabled control, LED Channel output is OFF regardless of the PWM Duty Setting, protection and DC/DC feedback is disabled for the controlled channel.

Table 21. LED Channel Enable Setting (x = 0 to 23)

LEDEN[x]	Operation
0	“LEDx+1” is disabled.
1	“LEDx+1” is enabled.

Description of Registers – continued

Address 0x07h: SYSSET4 system setting4 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	ISETLAT	AUTOOFF	ERRCLR	OCPLAT	CRCERLAT	LSHLAT	LOPLAT
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.

bit[6] ISETLAT
Please set this register in initial setting.

Table 22. ISETLAT Setting

ISETLAT	Operation
0	Normal (Auto-release)
1	Enable latch condition for the EXTISET1 pin and the EXTISET2 pin short detection. Outputs based on ISETSHCNT[1:0] setting are latched until writing ERRCLR = 1. Please refer detailed information on ISETCNT register description.

bit[5] AUTOOFF
Please set this register in initial setting.

Table 23. AUTOOFF Setting

AUTOOFF	Operation
0	Normal
1	Target channel is disabled automatically when “LED open error” is detected.

bit[4] ERRCLR

Table 24. ERRCLR Setting

ERRCLR	Operation
0	Normal
1	This register clears error status registers the EXTISET1 pin and the EXTISET2 pin short detection (ISETSHERR when ISETLAT = H), LED open protection (LOPERR when LOPLAT = H), UART CRC error (CRCERR when CRCERLAT = H), UVLO protection (UVLOTSDERR), Cathode short protection (CATHERR) and UART WDT protection (WDTERR). This register returns to “0” automatically.

bit[3] OCPLAT
Please set this register in initial setting.

Table 25. OCPLAT Setting

OCPLAT	Operation
0	Normal (Auto-release)
1	FAILB output (Low) and “OCP error” status registers (OCPERR) are latched until writing ‘1’ in ERRCLR register.

bit[2] CRCERLAT
Please set this register in initial setting.

Table 26. CRCERLAT Setting

CRCERLAT	Operation
0	Normal (Auto-release)
1	Enable latch condition for UART CRC detection. This setting latches detection in the FAILB pin output “Low” and “CRC error” status register (CRCERR) until writing “1” in ERRCLR register.

Address 0x07h: SYSSET4 – continued

bit[1] LSHLAT
Please set this register in initial setting.

Table 27. LSHLAT Setting

AUTOOFF	LSHLAT	LED Channel Control	Operation
0	0	Must set register LEDEN[x] = 0 via UART to disable target channel	FAILB output (Low) and “LED short error” status register (LSHERR[x]) returns to normal condition after error is released.
0	1		FAILB output (Low) and “LED short error” status register (LSHERR[x]) are latched until writing ‘1’ in ERRCLR register.
1	*	LEDEN[x] = 0 automatically after detection	

x: error channel number -1

bit[0] LOPLAT
Please set this register in initial setting.

Table 28. LOPLAT Setting

AUTOOFF	LOPLAT	LED Channel Control	Operation
0	0	Must set register LEDEN[x] = 0 via UART to disable target channel	Normal (auto-release)
0	1		Enable latch condition for LED Open detection. This setting latches the detection in the FAILB pin output “Low” and “LED open error” status register (LOPERR[x]) are latched until writing “1” in ERRCLR register.
1	*	LEDEN[x] = 0 automatically after detection	The FAILB pin output and LOPERR status register is released automatically with LED Channel disable.

x: error channel number -1

Description of Registers – continued

Address 0x08h: SYSSET5 ERROR output mask setting register [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	SWOCPEN	OCPEN	CATHEN	TSDWEN	WDTEN	LOPEN
Initial value	0	0	0	0	0	0	0	0

Update: immediately

These data in register are updated to the newest data immediately when the new data is written.
CATHEN returns “0” automatically.

Bit[5] SWOCPEN
Please set this register in initial setting.

Table 29. SWOCPEN Register

SWOCPEN	Operation
0	SWOCP protection is disabled.
1	SWOCP protection is enabled. If it detects, it controls SWOCPERR and the FAILB pin output “Low”. This only affect protection detection and will not release the protection when already detected.

Bit[4] OCPEN
Please set this register in initial setting.

Table 30. OCPEN Register

OCPEN	Operation
0	OCP protection is disabled
1	OCP protection is enabled. If it detects, it controls OCPERR and the FAILB pin output “Low”. This only affect protection detection and will not release the protection when already detected. This is for latched conditions.

Bit[3] CATHEN
Please set this register in initial setting.

Table 31. CATHEN Register

CATHEN	Operation
0	Cathode short protection is disabled.
1	Cathode short protection is enabled. Enable this function at initialization and the device monitors “Cathode short error” after 10 ms. If it detects the error, it sets CATHERR status register and the FAILB pin output “Low”. This register automatically returns “0” after monitoring. CATHERR status register is latched automatically. When CATHEN = 1, “LED open protection” is disabled.

Bit[2] TSDWEN
Please set this register in initial setting.

Table 32. TSDWEN Register

TSDWEN	Operation
0	TSD Warning protection is disabled.
1	TSD Warning protection is enabled. If it detects error, it sets TSDW status register and the FAILB pin output “Low”. This register setting does not release the protection status when it is already detected.

Address 0x08h: SYSSET5 – continued

bit[1] WDTEN
Please set this register in initial setting.

Table 33. WDTEN Register

WDTEN	Operation
0	Watch Dog Timer for UART is disabled.
1	Watch Dog Timer for UART is enabled. If it detects disconnection over 100 ms (Typ), it sets WDTERR status register and the FAILB pin output “Low”. This register setting does not release the protection status when it is already detected.

bit[0] LOPEN
Please set this register in initial setting.

Table 34. LOPEN Register

LOPEN	Operation
0	LED open protection is disabled.
1	LED open protection is enabled. If it detects error, it sets LOPERR status register and the FAILB pin output “Low”. This register setting does not release the protection status when it is already detected.

Description of Registers – continued

Address 0x09h: LEDSHENL ERROR output mask time setting register [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LSHEN[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: immediately

Address 0x0Ah: LEDSHENH ERROR output mask time setting register [Read/Write] initial value 0x20h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	ISETSHCNT[1:0]		LSHEN[11:8]			
Initial value	0	0	1	0	0	0	0	0

Update: immediately

These registers are updated to the newest data immediately when the new data is written.

Address 0x09h bit[7:0], Address 0x0Ah bit[3:0] LSHEN[11:0]

This register control “LED short error” protection. This register is assigned each 2 channels.
This only affect protection detection and will not release the protection when already detected. This is for latch conditions.

Table 35. LSHEN Enable Setting

LSHEN[n]	Operation
n = 0	LED1 and LED2 channel short protection enable
n = 1	LED3 and LED4 channel short protection enable
n = 2	LED5 and LED6 channel short protection enable
n = 3	LED7 and LED8 channel short protection enable
n = 4	LED9 and LED10 channel short protection enable
n = 5	LED11 and LED12 channel short protection enable
n = 6	LED13 and LED14 channel short protection enable
n = 7	LED15 and LED16 channel short protection enable
n = 8	LED17 and LED18 channel short protection enable
n = 9	LED19 and LED20 channel short protection enable
n = 10	LED21 and LED22 channel short protection enable
n = 11	LED23 and LED24 channel short protection enable

Table 36. LSHEN Register (n = 0 to 11)

LSHEN[n]	Operation
0	LED Short protection is disabled
1	LED Short protection is enabled

Address 0x0Ah bit[5:4] ISETSHCNT[1:0]

This register is the output control setting for ISETSH1 and ISETSH2 detection. Please set this register in initial setting.

Table 37. ISETSHCNT Register Setting

ISETSEL Register	ISETSHCNT Register	Status register	FAILB	LEDEN	EXTISET1 Selector (ISETSEL)	EXTISET2 Selector (LEXTISET2SEL)
0	-	Internal ISET				
1	0	H	L	-	-	-
1	1	H	L	L	-	-
1	2	H	L	-	L *(Note 1)*	L *(Note 2)*
1	3	Not used				

This table shows the state of the outputs when EXTISET1 and EXTISET 2 short is detected. "-" not affected.

(Note 1) When detected, output state is latched until ERRCLR is sent. This function is not dependent on ISETLAT setting.
For Latch function via ISETLAT setting, output conditions corresponding to ISETSHCNT setting are latched when protection is detected. Latched condition is cleared by system reset or sending ERRCLR.

(Note 2) When IC is at LIMPHOME mode and ISET Short is detected, change ISET selector from external (EXTISET1/EXTISET2) to internal. This function is not dependent on ISETLAT setting. Latched condition is cleared by system reset or sending ERRCLR.

Description of Registers – continued

Address 0x0B: LEDSHTH0102 LED Short Detection Voltage for LED1 and LED2 [Read / Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LEDSHTH0102[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: immediately

These register data in updated to the newest data immediately when the new data is written.
Please set this register in initial setting.

Table 38. LED Short Detection Voltage

LEDSHTH0102	Detection voltage (V_{LEDSH}) [V]
0 to 15	0.93
16	1.00
17	1.05
-	-
n	(15 / 256) x (n + 1)
-	-
251	14.77
252	14.82
253	14.88
254	14.94
255	15.00

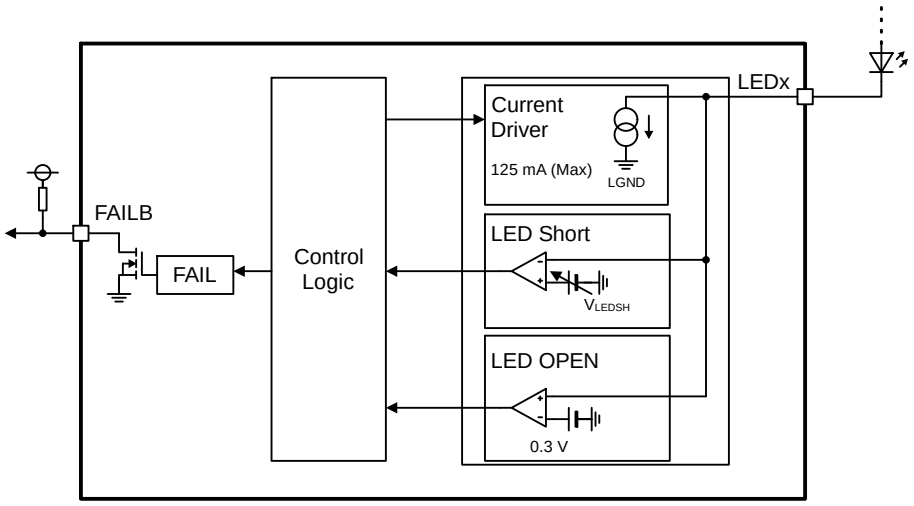


Figure 50. LED Pin Protection Circuit Image

Address 0x0C to 0x16: LEDSHTHx (x = 0304 to 2324)

This register is used to make LED Short detection voltage setting for LED3 to LED24. The setting procedure is the same as that for LED1 with Address set to 0x0B.

Description of Registers – continued

Address 0x17h: DENVOLT DEN Threshold voltage setting register [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LLSDAC[1:0]		PWMFREQ[1:0]		DENVOLT[3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: immediately

These data in register are updated to the newest data immediately when the new data is written.

bit[7:0] LLSDAC[1:0]
DCDC Low level reference selector for feedback voltage

Table 39. LLSDAC Register

LLSDAC[1:0]	DCDC Low level Refence Voltage [V]
0x0h	1.2
0x1h	1.0
0x2h	0.8
0x3h	0.6

bit[5:4] PWMFREQ[1:0]
This register setting determines the LED output frequency.
This setting is also applicable to PWMTIM.

Table 40. PWM Frequency Setting

PWMFREQ[1:0]	LED PWM Dimming Frequency*(Note 1)*
0x0h	488 Hz (Typ)
0x1h	976 Hz (Typ)
0x2h	1952 Hz (Typ)
0x3h	3904 Hz (Typ)

(Note 1) The frequency indicated above is based on 18 MHz (Typ) system clock. It may vary depending on internal clock frequency.

bit[3:0] DENVOLT[3:0]
When $V_{IN} < V_{IN\_DEN}$, IC cannot detect LED open detection (LEDOP).
V_{IN_DEN} can be defined by setting register and set by the following table.

Table 41. DENVOLT Register

DENVOLT[3:0]	V_{IN_DEN} detection voltage [V]
0x0h	4.5
0x1h	
0x2h	
0x3h	
0x4h	
0x5h	5.0
0x6h	6.0
0x7h	7.0
0x8h	8.0
0x9h	9.0
0xAh	10.0
0xBh	11.0
0xCh	12.0
0xDh	13.0
0xEh	14.0
0xFh	15.0

Description of Registers – continued

Address 0x18h: PWMDLY0102 PWM delay setting [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	PWMDLY02[3:0]				PWMDLY01[3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

The data in register is updated to the newest data immediately when the new data is written.
Please set this register in initial setting.

This register is used to set phase shift/delay width for PWM light modulation in a total of 4-bit.

Table 42. PWMDLY Register

PWMDLY01[3:0] PWMDLY02[3:0]	LED Delay Width [µs]
0x0h	24
0x1h	32
0x2h	40
0x3h	48
0x4h	56
0x5h	64
0x6h	72
0x7h	80
0x8h	88
0x9h	96
0xAh	104
0xBh	112
0xCh	120
0xDh	128
0xEh	136
0xFh	144

Address 0x19h to 0x23h: PWMDLYx (x = 0304 to 2324)
This register is used make setting for PWM delay width setting for LED3 to LED24. The setting procedure is the same as that for LED1 with Address set to 0x18h.

Description of Registers – continued

Address 0x24h: DCDIM0102 DC Current Setting for CH1,2 [Read/Write] initial value 0xFFh

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	DCDIM02[3:0]				DCDIM01[3:0]			
Initial value	1	1	1	1	1	1	1	1

Update: immediately

The data in register is updated to the newest data immediately when the new data is written.
Please set this register in initial setting.

Table 43. DCDIM Register

DCDIM01[3:0] DCDIM02[3:0]	LED current setting [mA]
0x0h	3.75
0x1h	7.50
0x2h	11.25
0x3h	15.00
0x4h	18.75
0x5h	22.50
0x6h	26.25
0x7h	30.00
0x8h	33.75
0x9h	37.50
0xAh	41.25
0xBh	45.00
0xCh	48.75
0xDh	52.50
0xEh	56.25
0xFh	60.00

Address 0x25h to 0x2Fh: DCDIMx (x = 0304 to 2324)
This register is used to make DC current setting for LED3 to LED24. The setting procedure is the same as that for LED1 with Address set to 0x24h.

The data in register is updated to the newest data immediately when the new data is written.

Description of Registers – continued

Address 0x30h: PWMOUTL PWM output enable setting 1 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	PWMOUTEN[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: PWM

Address 0x31h: PWMOUTM PWM output enable setting 2 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	PWMOUTEN[15:8]							
Initial value	0	0	0	0	0	0	0	0

Update: PWM

Address 0x32h: PWMOUTH PWM output enable setting 3 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	PWMOUTEN[23:16]							
Initial value	0	0	0	0	0	0	0	0

Update: PWM

Address 0x33h: DIMSET01 PWM duty or DC dimming setting for LED1 [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	DIMSET01[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: PWM

The register data is updated to the newest data when the next PWM signal rises up after the data is written.

This register is used to make setting of pulse duty for PWM light modulation in a total of 8-bits in PWM dimming mode.

Table 44. DIMSET Register

DIMMODE	PWMOUTEN[0]	DIMSET01[7:0]	PWM Duty	DC current
0	0	0x00h to 0xFFh	0.0 %	DCDIM01[3:0] register setting
	1	0x00h	0.4 %	
		0x01h	0.8 %	
		0x02h	1.2 %	
		0x03h	1.6 %	
		-	-	
		xx	(xx + 1) / 256	
		-	-	
		0xFEh	99.6 %	
		0xFFh	Normally set to High (Duty 100 %)	
1	0	0x00h to 0xFFh	0 %	0.23 mA
	1	0x00h	100 %	0.23 mA
		0x01h		0.47 mA
		0x02h		0.70 mA
		0x03h		0.94 mA
		-		-
		xx		(xx + 1) / 256 x 60 mA
		-		-
		0xFEh		59.77 mA
		0xFFh		60.00 mA

Address 0x34h to 0x4Ah: DIMSETx (x = 02 to 24)

This register is used to make setting of PWM pulse width for LED2 to LED24. The setting procedure is the same as that for LED1 with Address set to 0x33h.

Description of Registers – continued

Address 0x4Bh: LSHERRL LED1 to LED8 pin short error status [Read] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LSHERR[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: -

Address 0x4Ch: LSHERRM LED9 to LED16 pin short errors status [Read] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LSHERR[15:8]							
Initial value	0	0	0	0	0	0	0	0

Update: -

Address 0x4Dh: LSHERRH LED17 to LED24 pin short error status [Read] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LSHERR[23:16]							
Initial value	0	0	0	0	0	0	0	0

Update: -

The register data is updated to the newest data immediately when the data (“LED short error”) is detected.

Table 45. LED Short Error Status (n = 1 to 24)

LSHERR[n-1]	status
0	Normal
1	Detect error*(Note 1)*

(Note 1) How to return “0” for status register.

AUTOOFF = 0, LSHLAT = 0 : (n = 1 to 24)
Please set LEDEN[n-1] = 0 or PWMOUTEN[n-1] = 0 to release error channel and status register.

AUTOOFF = 0, LSHLAT = 1 : (n = 1 to 24)
Please set LEDEN[n-1] = 0 or PWMOUTEN[n-1] = 0 to release error channel.
Please set ERRCLR = 1 to clear status register

AUTOOFF = 1, LSHLAT = 0/1 : (n = 1 to 24)
Please set ERRCLR = 1 to clear status register
(Operates LEDEN[n-1] = 0 automatically)

Please refer timing chart of error control.

Description of Registers – continued

Address 0x4Eh: LOPERRL **LED1 to LED8 open error status** **[Read]** **initial value 0x00h**

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LOPERR[7:0]							
Initial value	0	0	0	0	0	0	0	0

Update: -

Address 0x4Fh: LOPERRM **LED9 to LED16 open error status** **[Read]** **initial value 0x00h**

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LOPERR[15:8]							
Initial value	0	0	0	0	0	0	0	0

Update: -

Address 0x50h: LOPERRH **LED17 to LED24 open error status** **[Read]** **initial value 0x00h**

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LOPERR[23:16]							
Initial value	0	0	0	0	0	0	0	0

Update: -

The register data is updated to the newest data immediately when the data (“LED open error”) is detected.

Table 46. LOPERR Register (n = 1 to 24)

LOPERR[n-1]	status
0	Normal
1	Detect error*(Note 1)*

(Note 1) How to return “0” for status register.

AUTOOFF = 0, LOPLAT = 0: (n = 1 to 24)
Set LEDEN[n-1] = 0 or PWMOUTEN[n-1] = 0 to release error channel and status register.

AUTOOFF = 0, LOPLAT = 1: (n = 1 to 24)
Set LEDEN[n-1] = 0 or PWMOUTEN[n-1] = 0 to release error channel.
Set ERRCLR = 1 to clear status register.

AUTOOFF = 1, LOPLAT = 0/1: (n = 1 to 24)
Set ERRCLR = 1 to clear status register.
(Operates LEDEN[n-1] = 0 automatically.)

Please refer timing chart of error control.

Description of Registers – continued

Address 0x51h: UVLOERR CRC and UVLO, TSD error status [Read] initial value 0x01h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ISETSHERR	SWOCP ERR	OCPERR	CATHERR	TSDWERR	WDTERR	CRCERR	UVLOTSDERR
Initial value	0	0	0	0	0	0	0	1

Update: -

bit[7] ISETSHERR
The register data is updated to the newest data immediately when the data (“ISET short Error”) is detected.

Table 47. ISETSHERR Register Setting

ISETSHERR	Status
0	Normal (or ISETSEL = 0)
1	Detect ISET Short Error (under 30 kΩ) when ISETSEL = 1

Table 48. EXTISET Pin Short Detection Setting

ISETSEL	ISETLAT	Release condition
0	*	Internal ISET setting. This protection is not available.
1	0	ISETSHERR error condition is released when protection is released. When “ISETSHCNT = 2”, status register is latched and can be released when “ERRCLR = 1” is set.
1	1	Status condition is released when “ERRCLR = 1” is set

bit[6] SWOCPERR
The register data is updated to the newest data immediately when the data (“SWOCP Error”) is detected.

Table 49. SWOCPERR Register Setting

SWOCPERR	Status
0	Normal
1	Detect SWOCP error

Table 50. SWOCP Detection Setting

SWOCPEN	Release condition
0	It is not available to control status and FAILB output
1	SWOCP error condition is released when protection is released

bit[5] OCPERR
The register data is updated to the newest data immediately when the data (“OCP Error”) is detected.

Table 51. OCPERR Register Setting

OCPERR	Status
0	Normal
1	Detect OCP error

Table 52. OCP Detection Setting

OCPEN	OCPLAT	Release condition
0	*	It is not available to control status and FAILB output
1	0	OCP error condition is released when protection is released
1	1	Status condition is released when “ERRCLR = 1” is set

bit[4] CATHERR
The register data is updated to the newest data immediately when the data (“Cathode Short Error ”) is detected.

Table 53. CATHERR Register

CATHERR	Status
0	Normal
1	Detect Cathode Short Error*(Note 1)*

(Note 1) Release “CATHERR” protection by ERRCLR = 1.
CATHEN automatically return “0” after monitoring “cathode short error”.

Address 0x51h: UVLOERR – continued

bit[3] TSDWERR
The register data is updated to the newest data immediately when the data (“TSD warning”) is detected.

Table 54. TSDWERR Register

TSDWERR	Status
0	Normal
1	Detect TSD warning

Table 55. TSD Warning Release Condition

TSDWEN	Status
0	It is not available to control status and FAILB output.
1	TSD warning protection is enabled.

bit[2] WDTERR
The register data is updated to the newest data immediately when the data (“UART WDT Error”) is detected.

Table 56. WDTERR Register

WDTERR	Status
0	Normal
1	Detect UART WDT*(Note 1)*

(Note 1) Release “WDTERR” protection by ERRCLR = 1.

bit[1] CRCERR
The register data is updated to the newest data immediately when the data (“CRC error”) is detected.

Table 57. CRCERR Register

CRCERR	Status
0	Normal
1	Detect CRC Error until CRC OK.

Table 58. CRC Error Release Condition

CRCERLAT	Release condition
0	CRC OK condition (for Write command) releases the status register and FAIL output.
1	Status Register is released when “ERRCLR = 1” is set.

bit[0] UVLOTSDERR
The register data is updated to the newest data immediately when the data (“UVLO or TSD error”) is detected.

Table 59. UVLOTSDERR Register

UVLOTSDERR	Status
0	Normal
1	Detect UVLO or TSD*(Note 2)*

(Note 2) When EN = L, this register is initialized to H. SWRST does not initialize this status register.
UVLOTSDERR is released if “ERRCLR = 1” is set.

Description of Registers – continued

Address 0x52h: LHDTY0102 LIMPHOME2 PWM duty setting for LED1 and LED2 [Read/Write] initial value 0xFFh

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LHDTY02[3:0]				LHDTY01[3:0]			
Initial value	1	1	1	1	1	1	1	1

Update: PWM

The register data is updated to the newest data when the next PWM signal rise up after the data is written.

This register is used to make setting of pulse duty for PWM light modulation in a total of 4-bits in PWM dimming mode.

Table 60. PWM Duty Setting at LIMPHOME2 (x = 01 to 02)

LHDTYx[3:0]	PWM Duty Setting for each CH	DC Dimming Setting for each CH
0x0h	OFF	DC Dimming is based on DCDIMx[3:0] register (DIMMODE = 0) or DIMSETx[7:0] register (DIMMODE = 1)
0x1h	5 %	
0x2h	10 %	
0x3h	15 %	
0x4h	20 %	
0x5h	25 %	
0x6h	30 %	
0x7h	40 %	
0x8h	45 %	
0x9h	50 %	
0xAh	55 %	
0xBh	60 %	
0xCh	70 %	
0xDh	80 %	
0xEh	90 %	
0xFh	100 %	

Address 0x53h to 0x5Dh: LHDTYx[3:0] (x = 0304 to 2324)
This register is used for PWM duty setting for LED3 to LED24 during LIMPHOME mode. The setting procedure is the same as LED1 and LED2 with address set to 0x52h.

Address 0x5Eh: LIMPHOME [Read/Write] initial value 0x03h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	-	-	-	-	LEXTISET2SEL	LIMPHEN
Initial value	0	0	0	0	0	0	1	1

Update: Immediate

bit[1] LEXTISET2SEL
This register is used to select the source for LED current setting operation during LIMPHOME.

Table 61. LED Current Setting Operation at LIMPHOME2

LEXTISET2SEL	Operation
0	LED current setting operation is based on ISETSEL register. It selects either internal current setting or using the EXTISET1 pin.
1	LED current setting operated using the EXTISET2 pin. This is operational only during LIMPHOME mode.

bit[0] LIMPHEN
This register is used to enable LIMPHOME Mode detection.

Table 62. LIMPHOME2 Enable Setting

LIMPHEN	Operation
0	LIMP HOME Detection is disabled
1	Enter LIMPHOME mode after 1.0 s of no UART access. Refer to LIMPHOME sequence.

Timing Chart

1. Dimming

1.1 PWM Delay Setting

Example of PWM behavior for LED1 is shown as follows.

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting (n = 01 to 24)
  - DIMSTART = 1
  - DIMMODE = 0
  - PWMDLYn[3:0]: refer to Figure 51.
  - DIMSETn[7:0] = 0x7Fh (50 % Duty)
  - Other: normal dimming setting
- Internal signal
  - CLKDIV144: internal clock (18 MHz / 144)
  - PWM base timing: base timing of PWM dimming

1.1.1 PWM Delay Setting

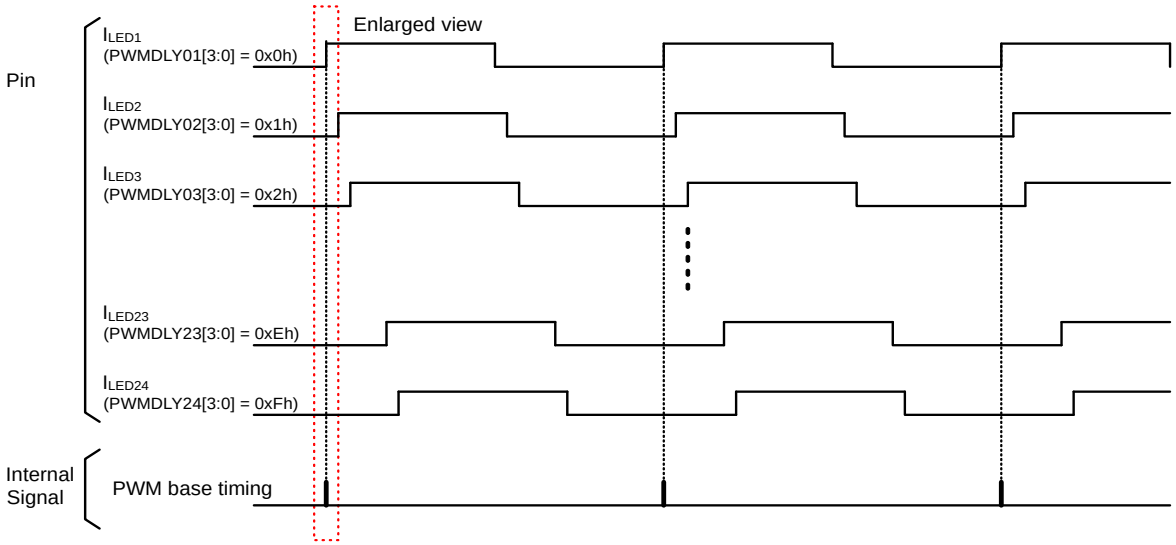
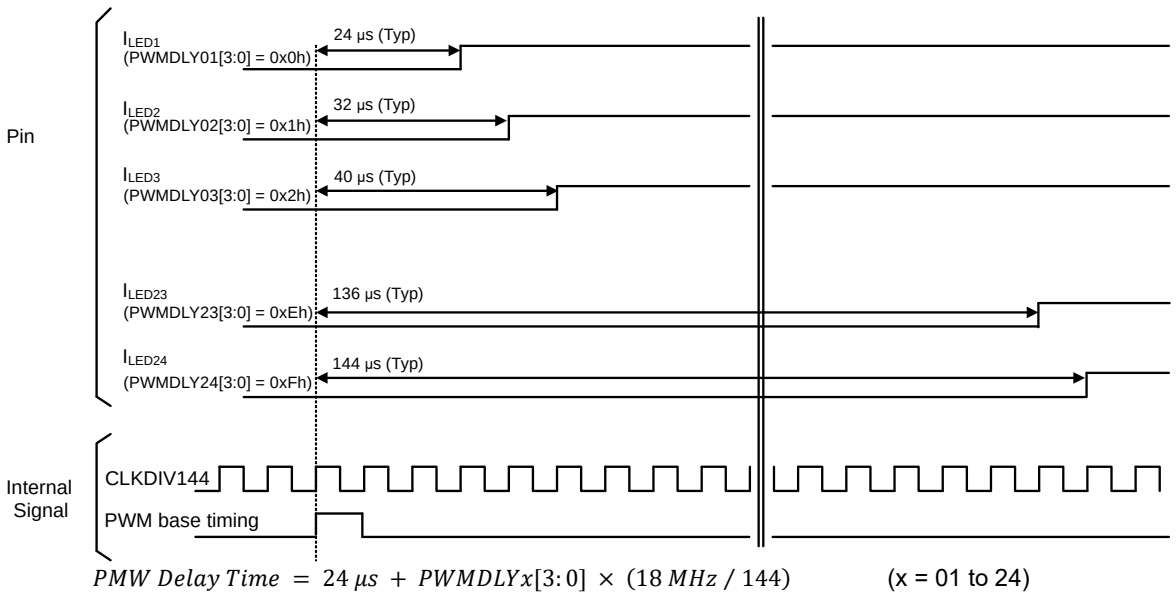


Figure 51. PWM Delay Setting

1.1.2 PWM Delay Setting (Enlarged View)



$$PMW\ Delay\ Time\ =\ 24\,\mu s\ +\ PWMDLYx[3:0]\ \times\ (18\,MHz\ /\ 144) \qquad (x = 01\ to\ 24)$$

Figure 52. PWM Delay Setting (Enlarged View)

1. Dimming – continued

1.2 PWM Diming

Example :

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting (n = 01 to 24)
  DIMSTART = 1
  DIMMODE = 0
  SYNCSET = 1
  PWMDLYn[3:0] = 0x0Fh
  PWMOUTEN[23:0] = 0x000000h
  DIMSETn[7:0] = 0x7Fh (50 % Duty)
  Other: normal dimming setting
- Internal signal
  pwmouten_buf: PWM output enable setting. This signal is updated at PWM base timing.
  dimset01_buf: PWM duty setting. This signal is updated at PWM base timing.
  pwmouten_cnt[0]: PWM output enable setting. This signal is updated with a delay of the PWMDLY01 setting from PWM base timing.
  dimset01_cont: PWM duty setting. This signal is updated with a delay of the PWMDLY01 setting from PWM base timing.

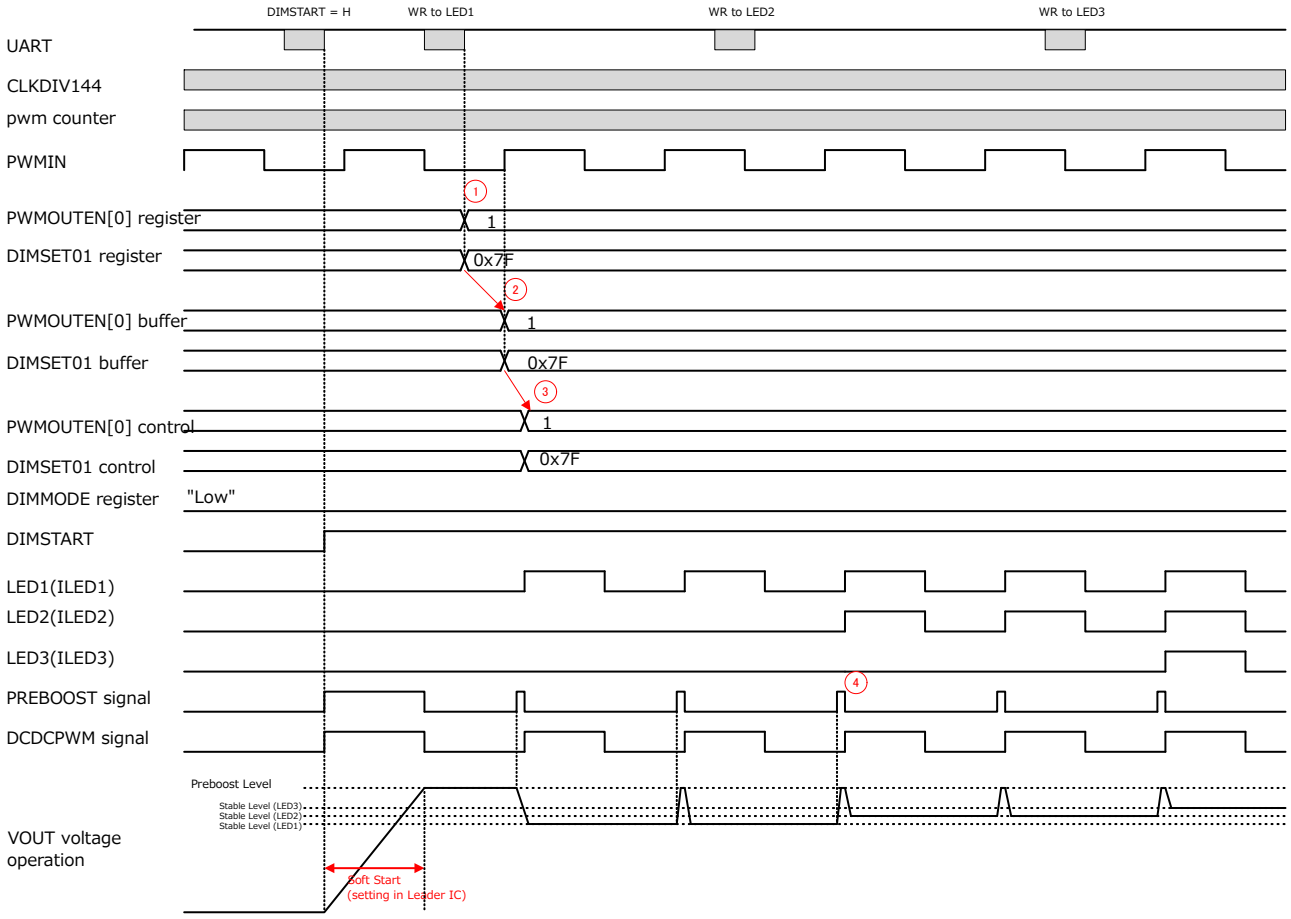


Figure 53. Dimming Setting in DIMMODE = 0

This example shows PWM Dimming control, DIMMODE = 0 (PWM Dimming).

① Send PWM settings (PWMOUTEN[0], DIMSET01[7:0], via UART) and other Settings like DIMMODE, PWMDLY01[3:0] and DCDIM01[3:0] are updated during initialization.

② At internal base PWM rising edge timing (for Leader) or PWMIN rising edge timing (for Follower), transfer data (PWMOUTEN, DIMSET) to buffer to prevent data from changing every base PWM cycles.

③ After PWMDLY01[3:0] setting, transfer data (PWMOUTEN[0], DIMSET01[7:0]) to start PWM output control. Control PWM duty based on DIMSET01[7:0] register value and DC dimming based on DCDIM01[3:0] register value.

④ Set LED2 = ON (PWMOUTEN[1], DIMSET02[7:0], via UART) and LED3 = ON (PWMOUTEN[2], DIMSET03[7:0], via UART) output at next PWMIN, after writing the corresponding settings.

1. **Dimming – continued**

1.3 PWM Dimming (Duty = 100 %)

Examples below show PWM Dimming control, DIMMODE = 0 (PWM Dimming) and duty setting is 100 % (DIMSET = 0xFFh) while having different Leader vs Follower frequency. The timing of the LED output generation is dependent on the timing of the rising edge of PWMIN input. The internal frequency of a Follower device is dependent on PWMIN input as reference signal. PWMIN input in this example is from a Leader device. Faster frequency of Leader device produces faster PWMIN input to Follower device and vice versa.

During PWM synchronization, the Follower device adjust internal clock to be the same as Leader device. In the example below, Leader device has equal frequency vs Follower Device.

Example :

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting: (n = 01 to 24)
  SYNCSET = 1 (Leader), SYNCSET = 2 (Follower)
  DIMSTART = 1
  DIMMODE = 0
  DIMSETn[7:0] = 0xFFh (100 % Duty)
- Internal signal
  PWM counter: this counter generates the PWM control for I_{LED} current.

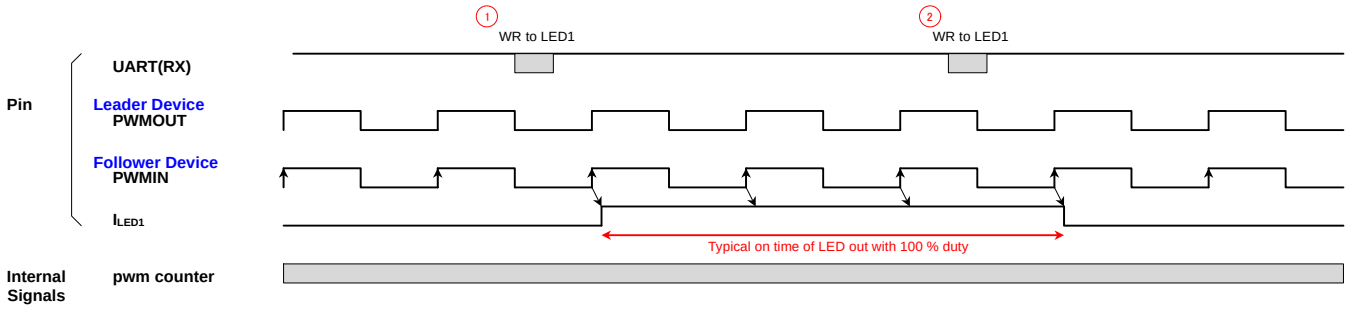


Figure 54. Dimming at 100 % Duty Setting and Leader Device and Follower Device has Typical Frequency

In the example below, Leader device has faster frequency vs Follower Device that resulted to faster PWMIN input. In the Follower device, the timing of LED output is dependent on a faster PWMIN input, the internal counter is restarted in each rising edge of PWMIN signal resulting to the total length of LED output that is shorter than typical.

Example :

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting: (n = 01 to 24)
  SYNCSET = 1 (Leader), SYNCSET = 2 (Follower)
  DIMSTART = 1
  DIMMODE = 0
  DIMSETn[7:0] = 0xFFh (100 % Duty)
- Internal signals:
  PWM counter: this counter generates the PWM control for I_{LED} current.

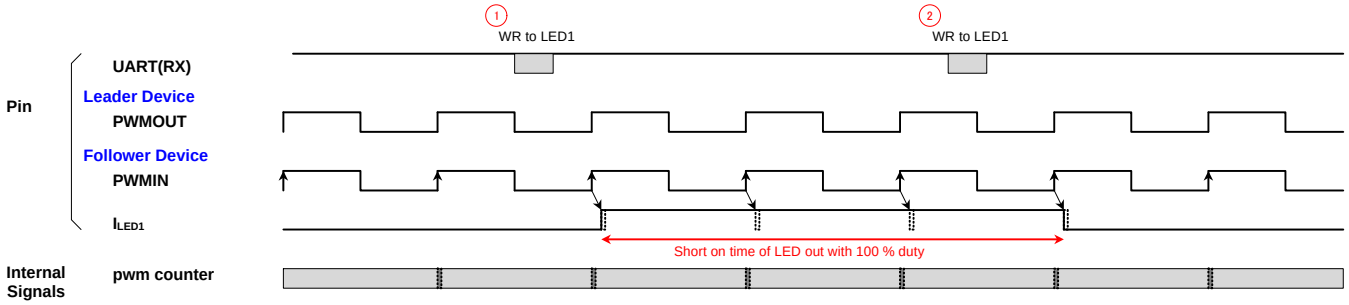


Figure 55. Dimming at 100 % Duty Setting and Leader Device has Higher Frequency vs Follower Device

1.3 PWM Dimming (Duty = 100 %) – continued

In the example below, Leader device has slower frequency vs Follower Device that resulted to slower PWMIN input. In the Follower device, the timing of LED output is dependent on a slower PWMIN input, internal counter for the 100 % duty finishes earlier then wait for PWMIN rising edge before restarting resulting to LED output turning off then the LED output continues after receiving PWMIN input.

Example :

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting: (n = 01 to 24)
  SYNCSET = 1 (Leader), SYNCSET = 2 (Follower)
  DIMSTART = 1
  DIMMODE = 0
  DIMSETn[7:0] = 0xFFh (100 % Duty)
- Internal signals:
  PWM counter: this counter generates the PWM control for I_{LED} current.

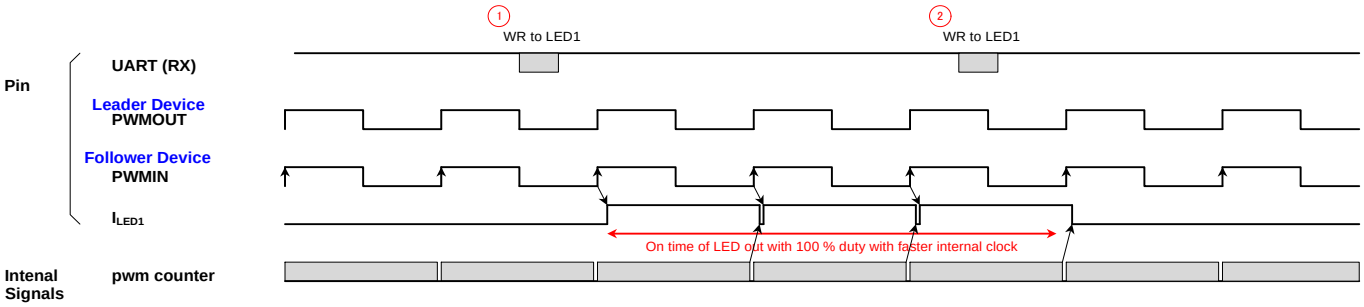


Figure 56. Dimming at 100 % Duty Setting and Leader Device has Lower Frequency vs Follower Device

All UART commands in the figures above are sent with the same timing to observe the length of the LED output. The sequence is as follows,

① Send DIMSETn[7:0] = 0xFFh (100 % Duty) via UART. At PWMIN rising edge timing for Follower device, Start LED output control based on DIMSETn[7:0] setting.

② Send DIMSETn[7:0] = 0x00h (0 % Duty) via UART. At PWMIN rising edge timing for Follower device, Start LED output control based on DIMSETn[7:0] setting.

1. Diming – continued

1.4 DC Dimming

Example :

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting (n = 01 to 24)
  DIMSTART = 1
  DIMMODE = 1
  SYNCSET = 1
  PWMOUTEN[23:0] = 0xFFFFFFh
  DIMSETn[7:0] = 0x7Fh (128/256 x ILED_MAX setting)
  Other: normal dimming setting

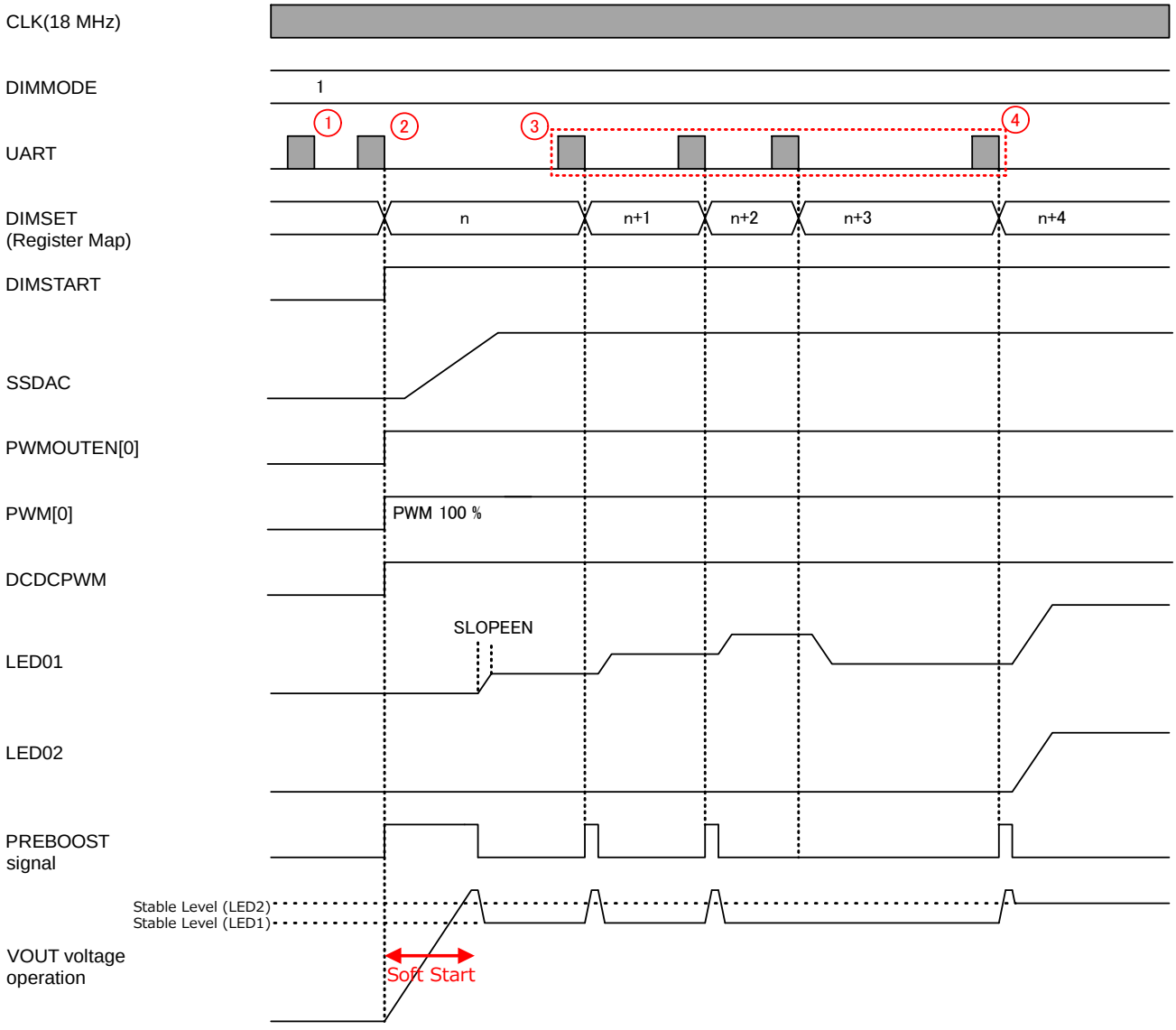


Figure 57. Dimming Setting in DIMMODE = 1

This example shows DC Dimming control, DIMMODE = 1 (DC Dimming)

① Send PWM settings DIMMODE via UART. PWMDLY and DCDIM don't have effect in DC Dimming.
② Send DIMSTART via UART to start with soft start function, Output 100 % PWM and DC Dimming start.
③ Adjust DC Dimming every update of DIMSET register. DC Dimming has slope function based on SLOPEEN register. Generate PREBOOST signal for DCDC when DC Dimming is adjusted from Lower to Higher value.
④ Set LED2 "ON", VOUT stable level increases based on active LED Channels.

1. **Diming – continued**

1.5 PWMFREQ Setting

Example: (n = 01 to 24)
Register setting
DIMMODE = 0
PWMOUTEN[23:0] = 0xFFFFFFh
DIMSETn[7:0] = 0x7Fh (50 % Duty)
Other: normal diming setting
I_{LEDx}: LEDx pin current (x = 1 to 24)

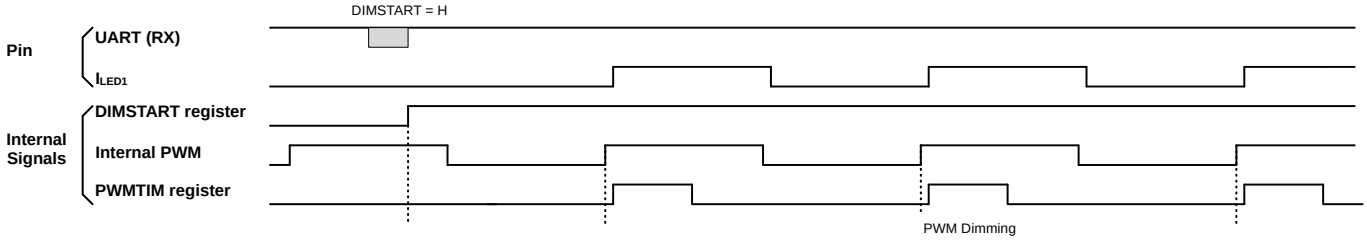


Figure 58. PWMFREQ = 0

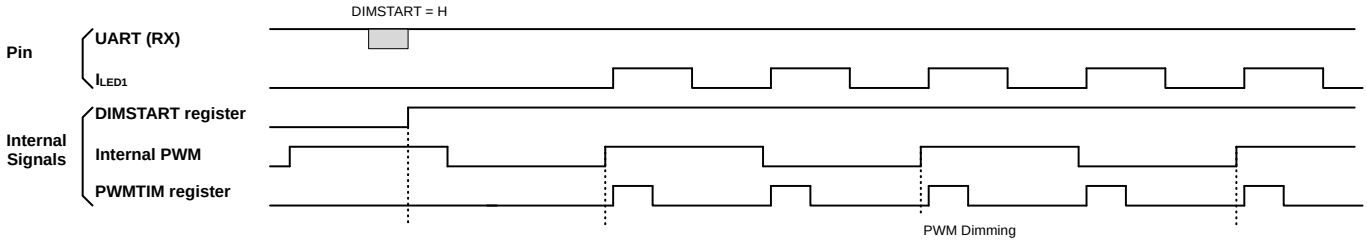


Figure 59. PWMFREQ = 1

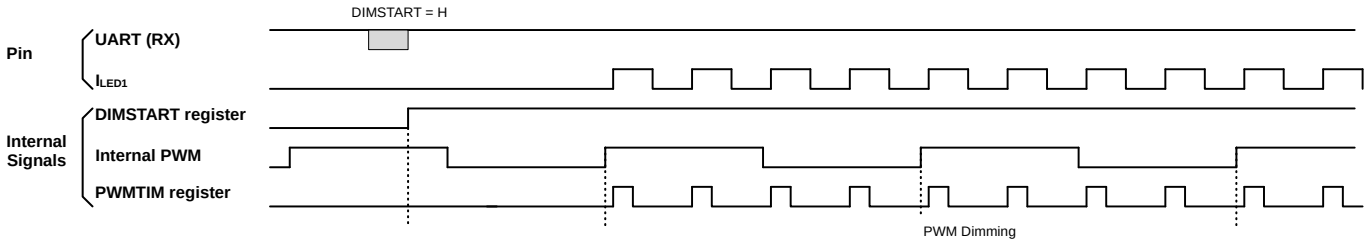


Figure 60. PWMFREQ = 2

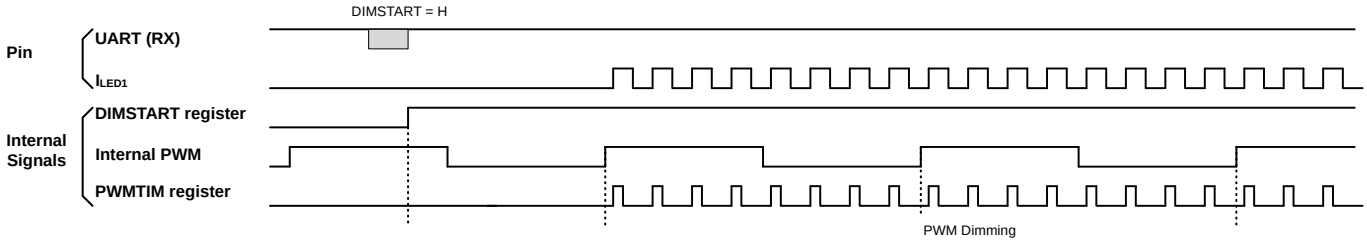


Figure 61. PWMFREQ = 3

This example shows PWM Dimming control using different PWMFREQ setting.
In the timing diagram above, PWMFREQ setting must be configured before DIMSTART = H.
After DIMSTART “L to H” will be soft start and dimming starts at succeeding internal PWM cycles.

(1) PWMFREQ = 0, PWM Dimming frequency is 488 Hz (Typ).
(2) PWMFREQ = 1, PWM Dimming frequency is 976 Hz (488 Hz x 2).
(3) PWMFREQ = 2, PWM Dimming frequency is 1952 Hz (488 Hz x 4).
(4) PWMFREQ = 3, PWM Dimming frequency is 3904 Hz (488 Hz x 8).

Timing Chart – continued

2. ERROR Control

There are the following internal signals on timing charts: (n = 1 to 24)

(1)	“PWM_OH[n-1]”	PWM signal for LEDn (High: LED ON, Low: LED OFF).
(2)	“CLKDIV16”	internal clock (divided by 16).
(3)	“CLKDIV144”	internal clock (divided by 144).
(4)	“TSD_IL”	TSD signal (Low: error)
(5)	“SSEND”	Soft start mask signal (Low: mask).
(6)	“WARTSD_IL”	TSD warning signal (Low: error).
(7)	“LOPDET_IL[n-1]”	LED open error signal (Low: error).
(8)	r_lopdet, r_lshdet, r_wartsd	retiming signal.
(9)	err_mskcnt	error mask counter.
(10)	ERRCLR	ERRCLR register.

Timing chart of each ERROR detection is as follows.

2.1 VINUVLO/VREG5UVLO/VREG3UVLO/TSD

If the device detects TSD, internal digital circuit is reset as shown in the figure. Other error (UVLO) is almost same as this. ERRMASK and SSMASK don’t have effect in this protection. During detection, other protections are masked. UVLOTSDERR register is reset to initial value “1”. ERRCLR is necessary to release UVLOTSDERR and the FAILB pin.

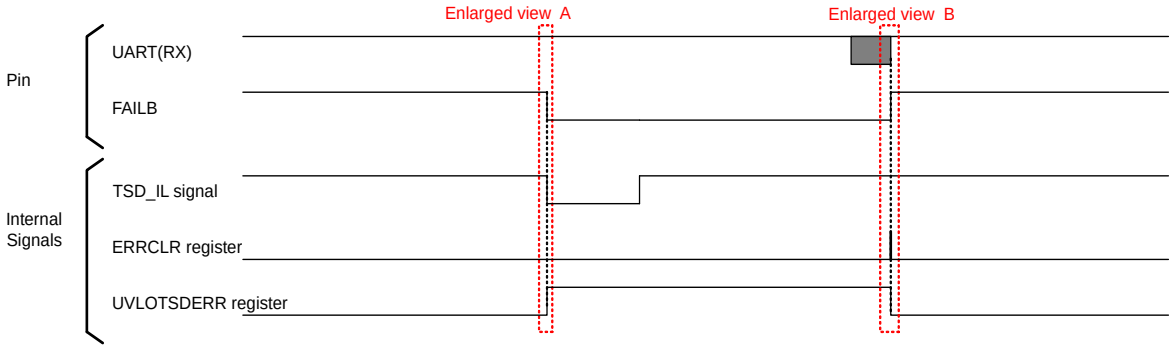


Figure 62. TSD Detection Function

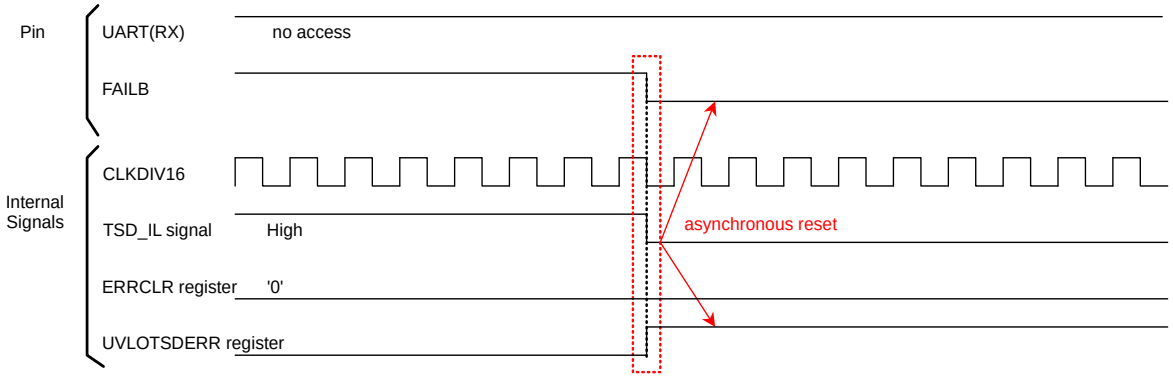


Figure 63. TSD Detected Function (Enlarged View A)

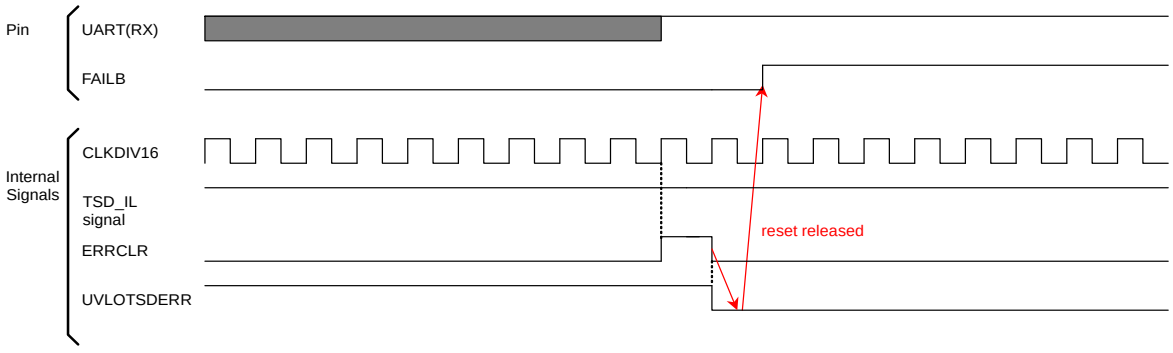


Figure 64. TSD Released Function (Enlarged View B)

2. ERROR Control – continued

2.2 TSD Warning

If temperature is over 125 °C, it can detect “WARTSD” (WARTSD_IL = Low). During detection, it updates FAILB = Low. At release, it updates FAILB = High after released. ERRMASK and SSMASK does not have effect in this protection.

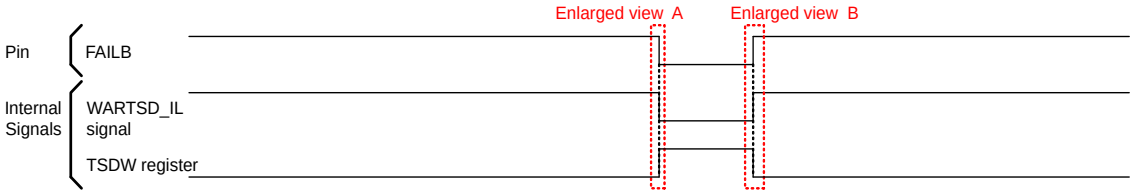


Figure 65. TSD Warning Function

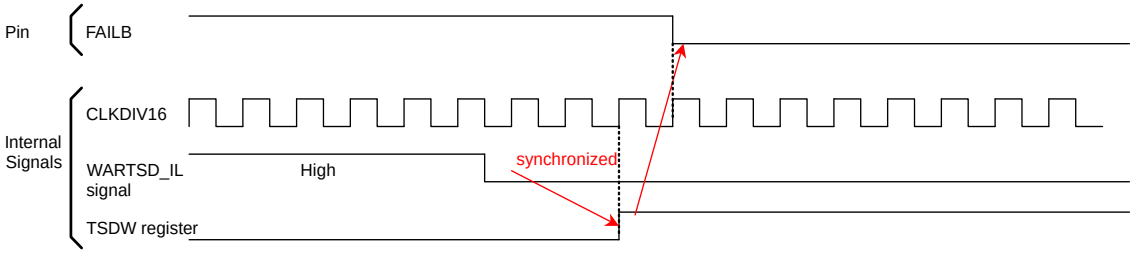


Figure 66. TSD Warning Detected Function (Enlarged View A)

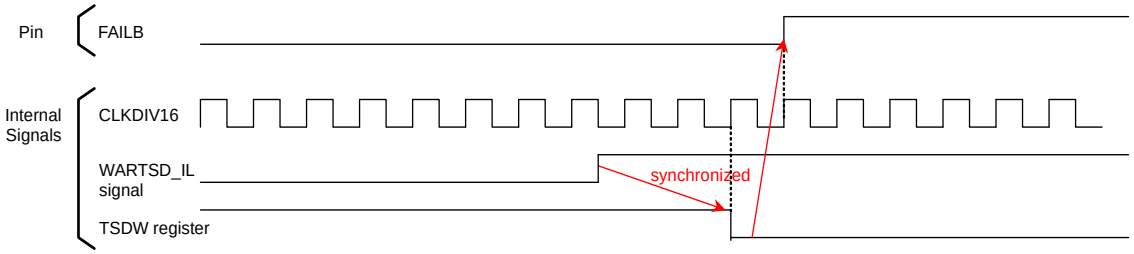


Figure 67. TSD Warning Released Function (Enlarged View B)

2. ERROR Control – continued

2.3 OCP Protection

If $V_{SNSP} - V_{SNSN} > V_{OCP}$ (Over Current Protection Threshold Voltage, 100 mV (Typ)), it can detect “OCP” (internal OCP_IL signal change to “Low”). During detection, status register OCPERR = H and FAILB = Low. At release, it updates status register OCPERR = H and FAILB = High. ERRMASK and SSMASK does not have effect in this protection.

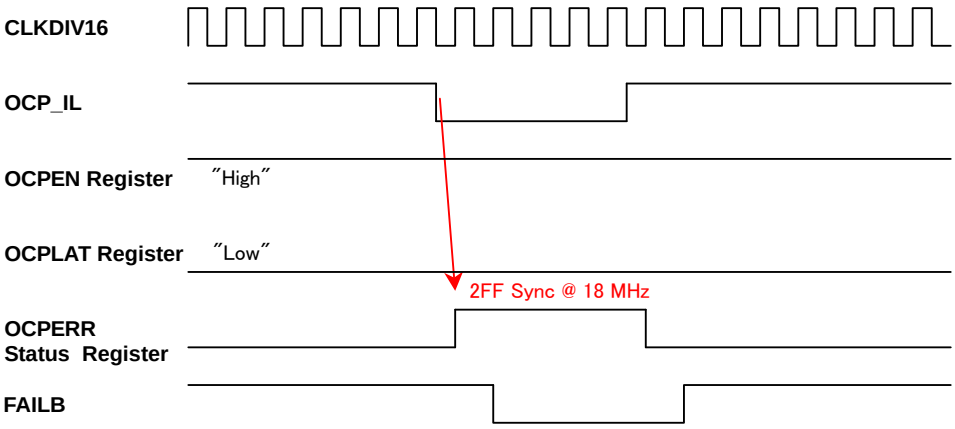


Figure 68. OCP Error Detection with OCPLAT “L”

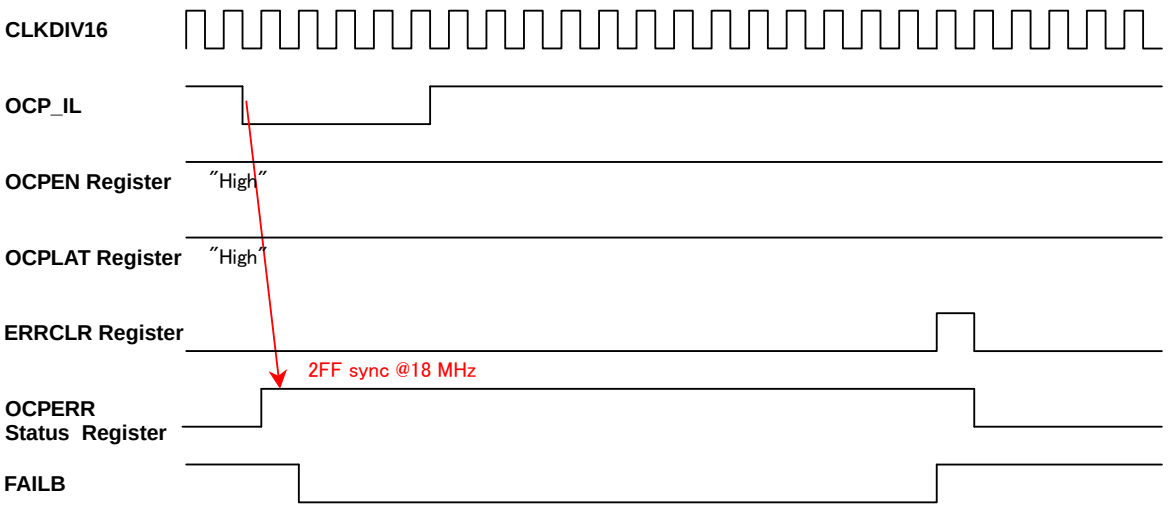


Figure 69. OCP Error Detection with OCPLAT “H”

2. ERROR Control – continued

2.4 LED Short Protection

When $V_{LEDx} > V_{LEDSH,}$ LED Short Protection is detected and when $V_{LEDx} < V_{LEDSH,}$ LED Short Protection is released. The detection and release of this protection is shown in Figure 70.

Example:

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting (n = 01 to 24)
  DIMSTART = 1
  DIMMODE = 0
  ERRMASK = 0x2h
  LSHLAT = 0
  DIMSETn[7:0] = 0x7Fh
  Other: normal diming setting internal signal
  CLKDIV16: internal clock (18 MHz / 16)
  PWM_OH[1]: Current Driver control signal (High: lighting) for LED2
  LSPDET_IL[1]: LED open error signal (low: error) for LED2
  err_mskcnt: error mask filter of detection and released for LED short protection

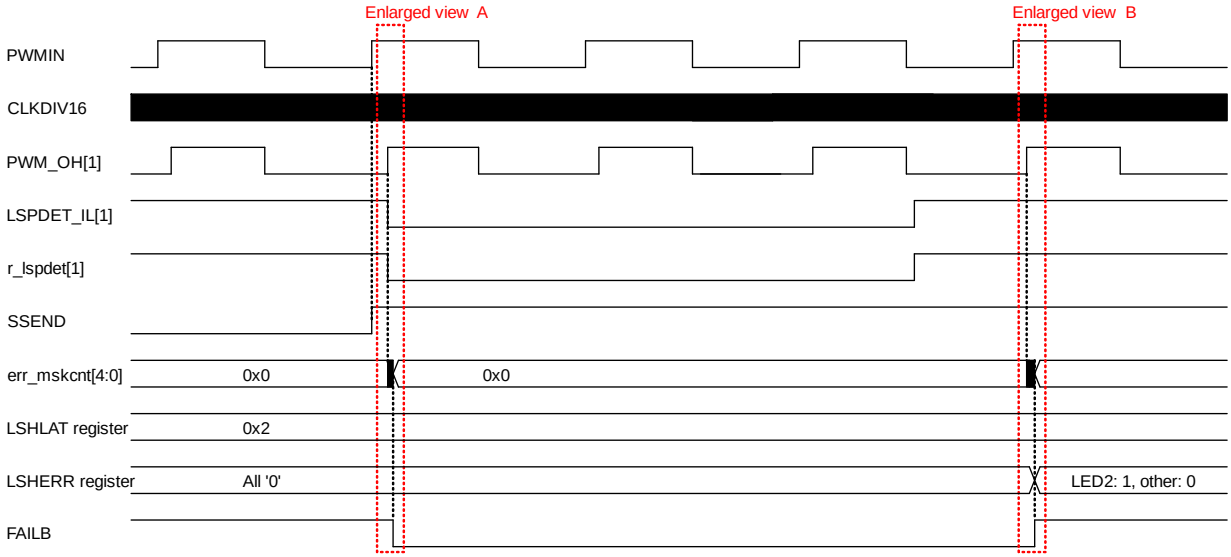


Figure 70. LED Short Protection Function

2.4. LED Short Protection – continued

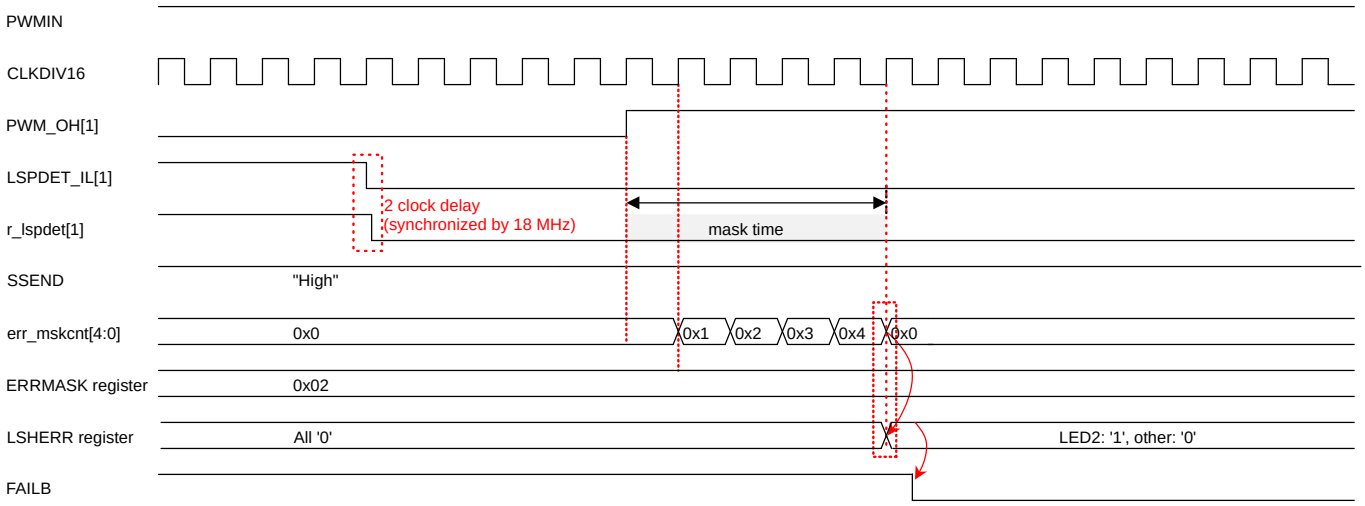


Figure 71. LED Short Protection Function (Enlarged View A)

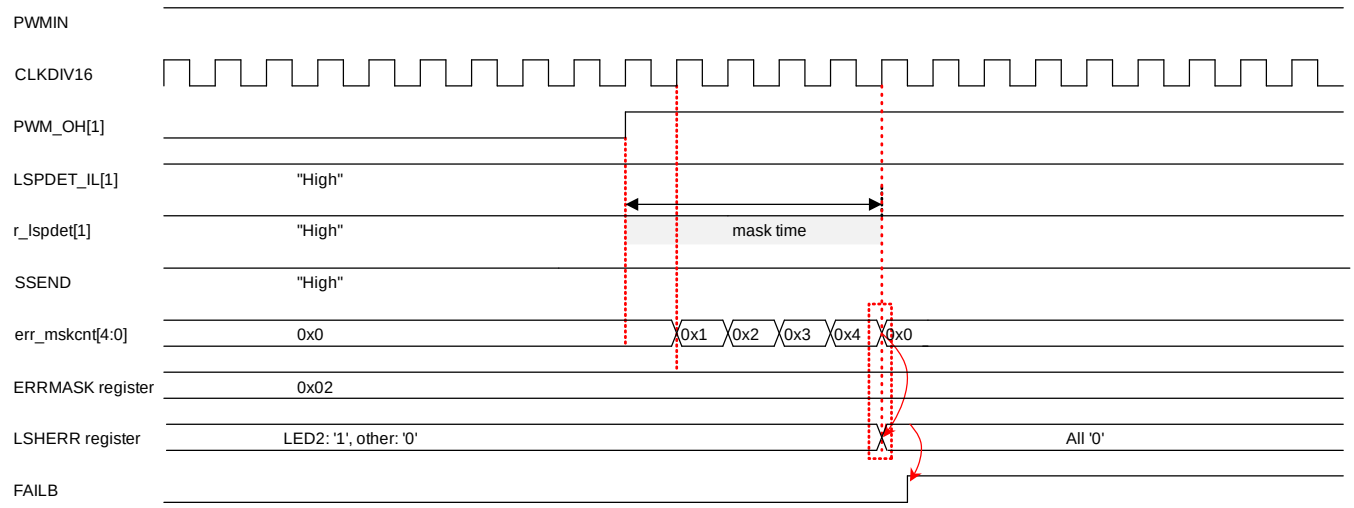


Figure 72. LED Short Protection (Enlarged View B)

Operation:

When SSEND = ‘High’ (Soft Start end), PWM_OH[1] = ‘High’ and LSPDET_IL[1] = ‘Low’ (LED short protection) is detected, ERRMASK starts counting with CLKDIV16 (err_mskcnt_r) from the rise-edge of PWM_OH[1]. When the set value (0x03h) is reached, FAIL is set to ‘Low’, i.e., ERROR is detected.

When ERROR is detected and PWM_OH[1] = ‘High’ and LSPDET_IL[1] = ’High’, ERRMASK starts counting with CLKDIV16 (err_mskcnt_r) from the rise-edge of PWM_OH[1]. When the set value (0x03h) is reached, FAILB is set to ‘High’, i.e. It releases the ERROR condition.

2. ERROR Control – continued

2.5 LED Open Protection

When V_{LEDx} < 0.3 V (Typ), LED Open protection is detected and when V_{LEDx} > 0.3 V (Typ), LED Open protection is released. The detection and release of this protection is shown in Figure 73.

Example:

- I_{LEDx}: LEDx pin current (x = 1 to 24)
- Register setting (n = 01 to 24)
  DIMSTART = 1
  DIMMODE = 0
  ERRMASK = 0x2h
  LOPLAT = 0
  DIMSETn[7:0] = 0x7Fh
  Other: normal diming setting internal signal
  CLKDIV16: internal clock (18 MHz / 16)
  PWM_OH[1]: Current Driver control signal (High: lighting) for LED2
  LOPDET_IL[1]: LED open error signal (low: error) for LED2
  err_mskcnt: error mask filter of detection and released for LED open detection

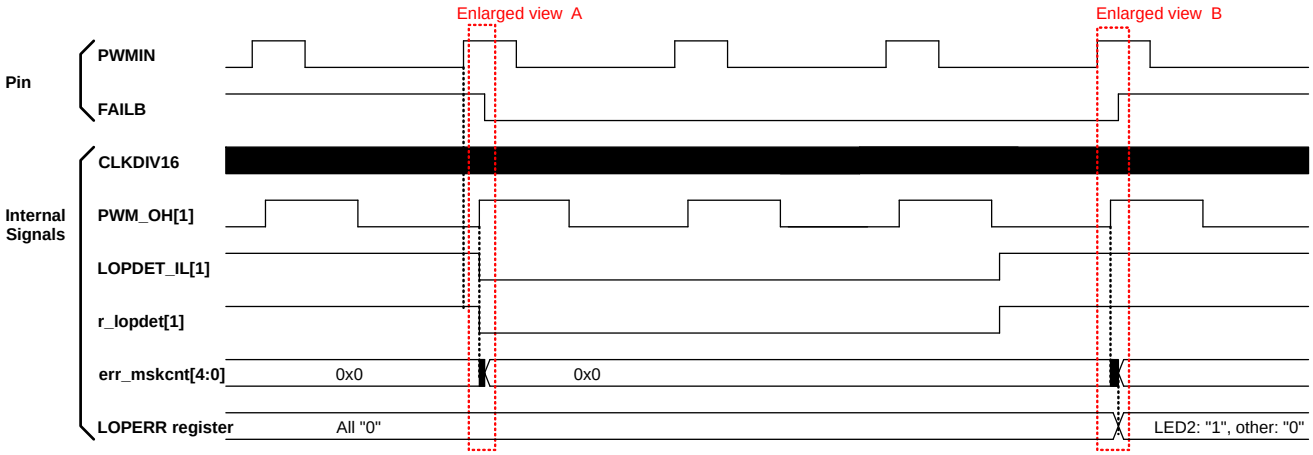


Figure 73. LED Open Protection Function

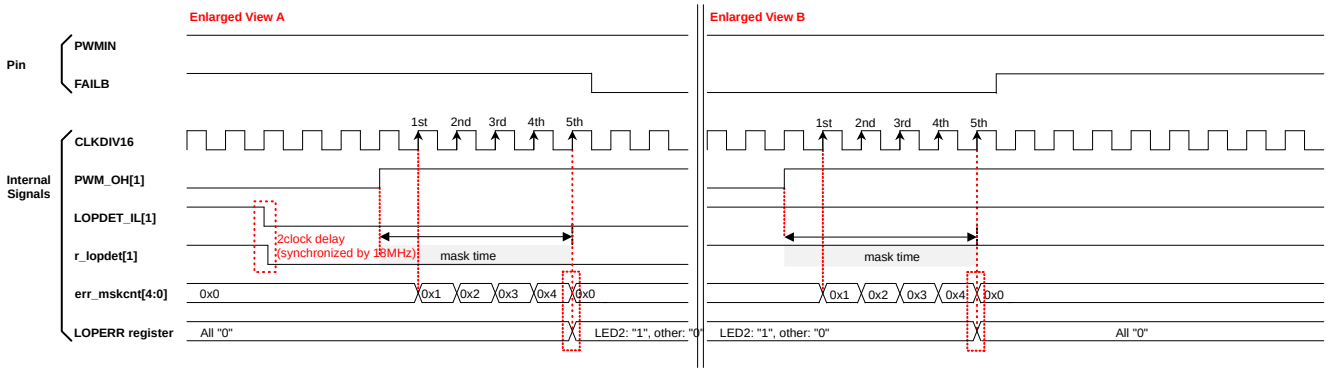


Figure 74. LED Open Protection Function (Enlarged View A)

Operation:

When SSEND = “High” (Soft Start end), PWM_OH[1] = “High” and LOPDET_IL[1] = “Low” (LED open protection) is detected, ERRMASK starts counting with CLKDIV16 (err_mskcnt) from the rise-edge of PWM_OH[1]. When the set value (0x03h) is reached, FAIL is set to “Low”, i.e., ERROR is detected.

When ERROR is detected and PWM_OH[1] = “High” and LOPDET_IL[1] = “High”, ERRMASK starts counting with CLKDIV16 (err_mskcnt) from the rise-edge of PWM_OH[1]. When the set value (0x03h) is reached, FAILB is set to “High”, i.e. It releases the ERROR condition.

2.5. LED Open Protection – continued

Example: Low width error case, Register setting: ERRMASK[3:0] = 0x02h, LOPLAT = 0

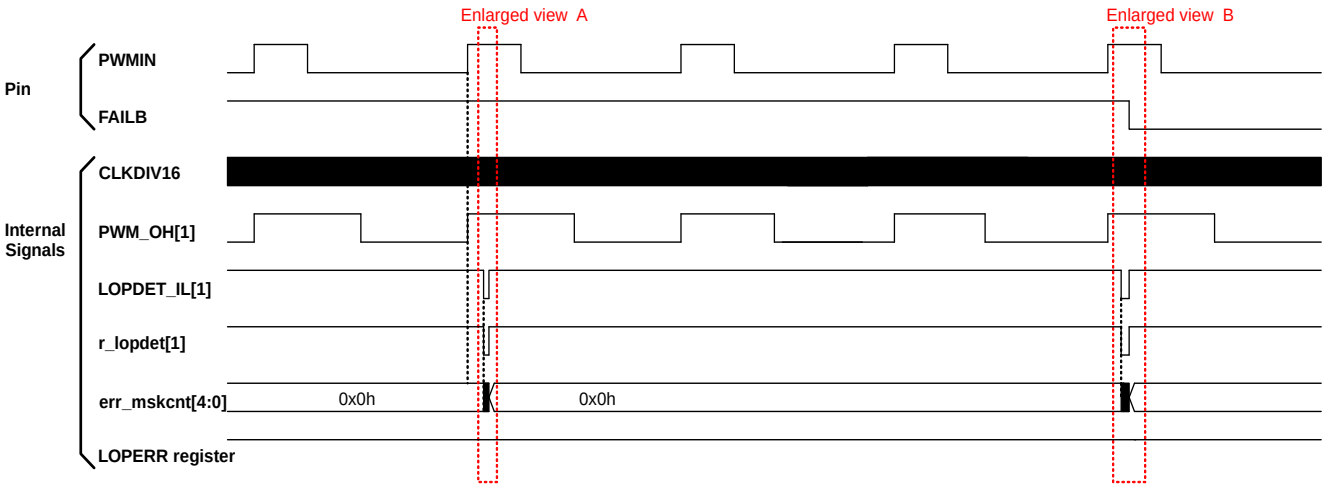


Figure 75. LED Open Protection Mask Function

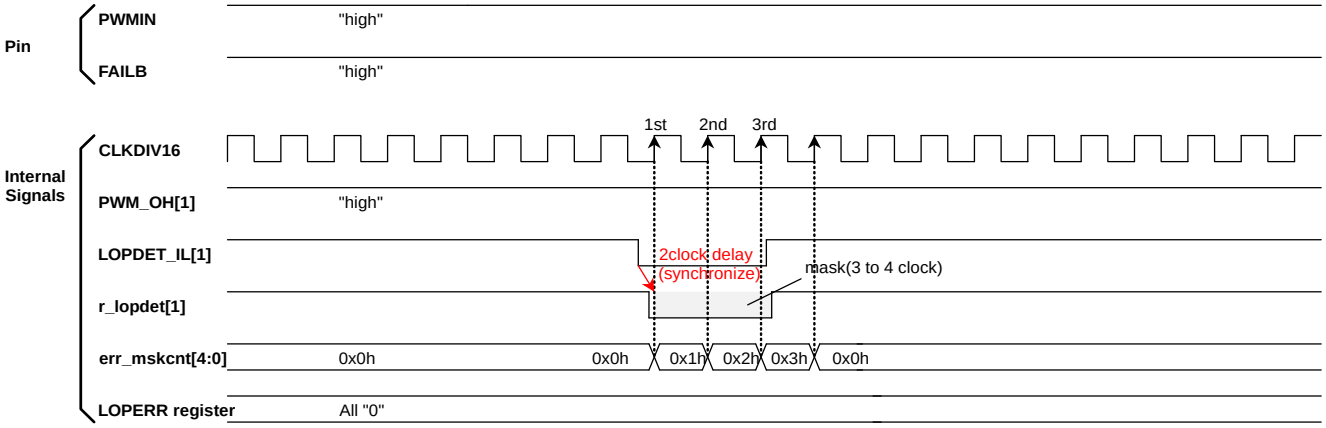


Figure 76. LED Open Protection Masked (Enlarged View A)

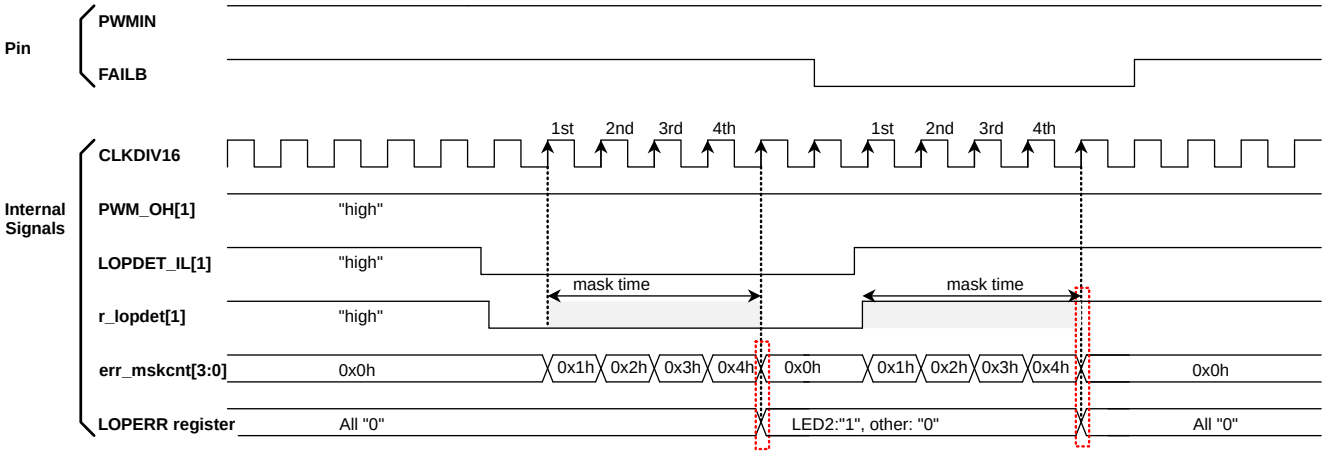


Figure 77. LED Open Protection (Enlarged View B)

2. ERROR Control – continued

2.6 LED Cathode Short Protection

Write CATHEN = 1 via UART to use cathode short protection.
It will monitor the LED pin voltage after 10 ms. If this voltage less than 0.3 V (Typ), it detects “cathode short error”. This condition is the same as LED Open detection, during the 10 ms counting, LED Open protection cannot be detected.

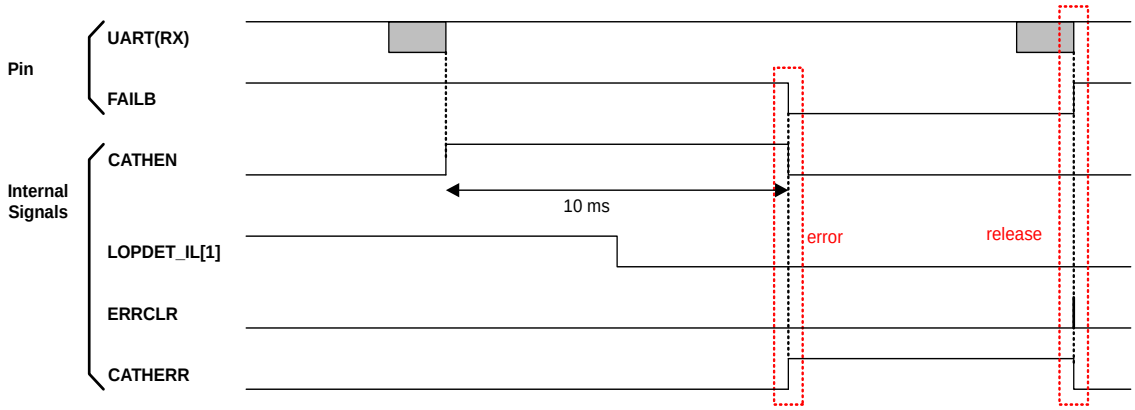


Figure 78. LED Cathode Short Protection (Error)

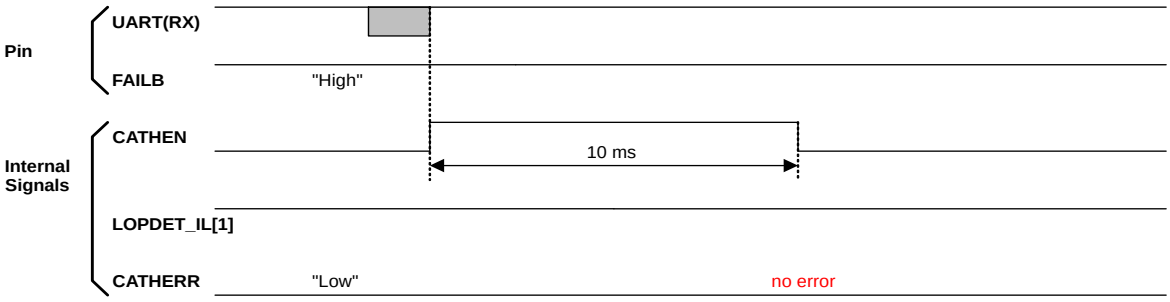


Figure 79. LED Cathode Short Protection (No Error)

2. ERROR Control – continued

2.7 UART WDT

This device has watch-dog timer (WDT) for UART communication when WDTEN register is set to "High".
It detects WDT Error when there is no activity for 100 ms in UART interface (RX line). When detected, this protection will set WDTERR Status register to "High" and FAILB output is latched to "Low". This condition is latched until "ERRCLR" is sent via UART to release this condition.

Example1: WDT protection detection

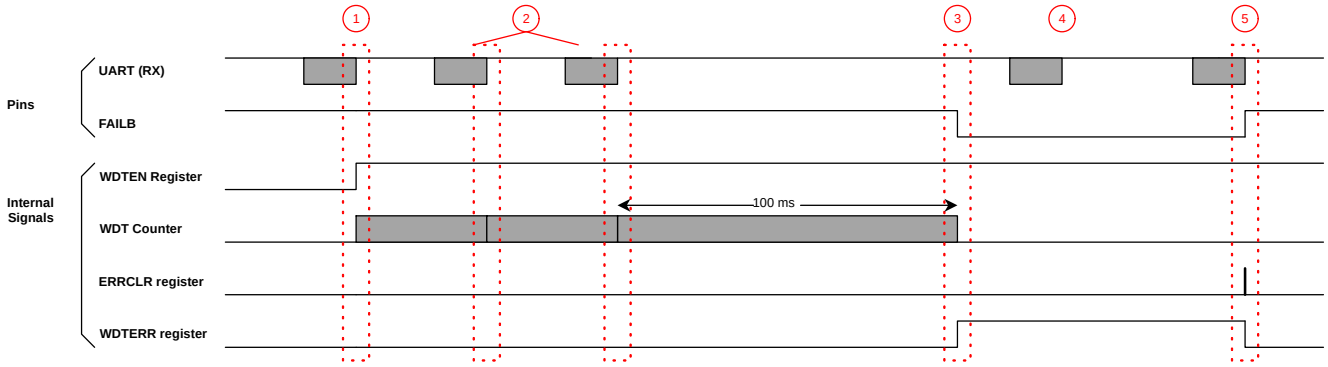


Figure 80. WDT Protection

① Set WDTEN = H, this setting enables WDT error detection.
② Any UART command with CRC OK resets the watch dog counter.
③ No CRC OK is received within 100 ms, WDT Error is detected. It sets WDTERR status register to “High” and the FAILB pin output to “Low”.
④ Send UART Read to Status registers.
⑤ WDTERR status register and FAILB are cleared when ERRCLR is received.

Register Settings:
WDTEN register = 1

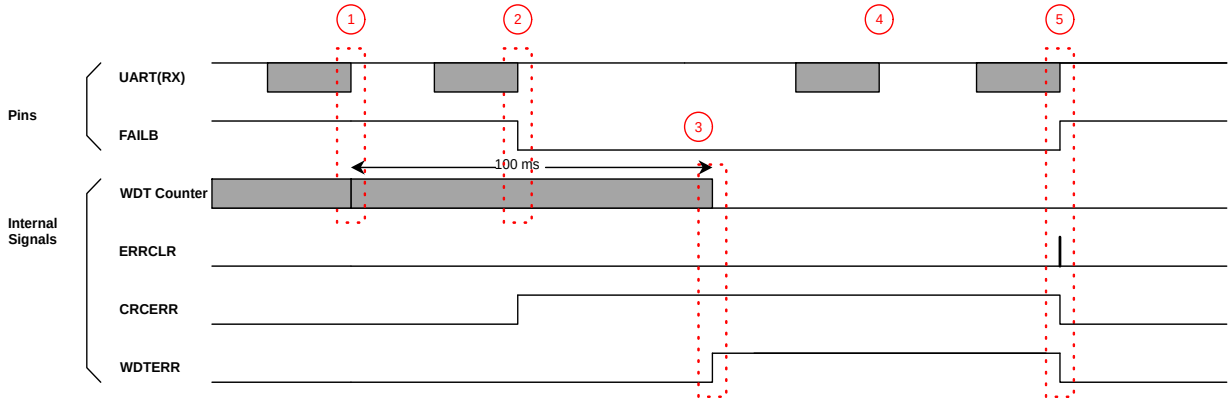


Figure 81. WDT Protection with CRC Error

① UART command received with CRC OK resets the watch dog counter.
② UART command with CRC error is detected, CRCERR status register is set to “High” and FAILB to “Low”.
③ No CRC OK is received within 100 ms, WDT Error is detected. It sets WDTERR status register to “High” and FAILB is already “low” since CRC Error is detected.
④ Send UART Read to Status registers.
⑤ WDTERR status register, CRC Error Register and the FAILB pin output are cleared when ERRCLR is received.

2. ERROR Control – continued

2.8 Soft Start Masking Function

The mask time of ERROR detection from initialization of IC is set by SSMASK register. This register value corresponds to an amount of mask time is shown in Table 63. The mask time is based on the protection detection time. If the protection detection time is more than this value. Protection is detected in FAILB after 1 or 2 clock (18 MHz / 16) cycles.

Table 63. Soft Start Mask time

SSMASK[3:0]	Soft Start Mask time [ms]
0x0	-
0x1	0.68 + PREBOOST time Setting
0x2	1.37 + PREBOOST time Setting
0x3	1.82 + PREBOOST time Setting
0x4	2.50 + PREBOOST time Setting
0x5	3.19 + PREBOOST time Setting
0x6	3.87 + PREBOOST time Setting
0x7	4.32 + PREBOOST time Setting
0x8	5.01 + PREBOOST time Setting
0x9	5.69 + PREBOOST time Setting
0xA	6.14 + PREBOOST time Setting
0xB	6.83 + PREBOOST time Setting
0xC	7.51 + PREBOOST time Setting
0xD	8.19 + PREBOOST time Setting
0xE	8.65 + PREBOOST time Setting
0xF	9.33 + PREBOOST time Setting

Example: Address = 0x03h (SSMASK), DATA = 0x02h:

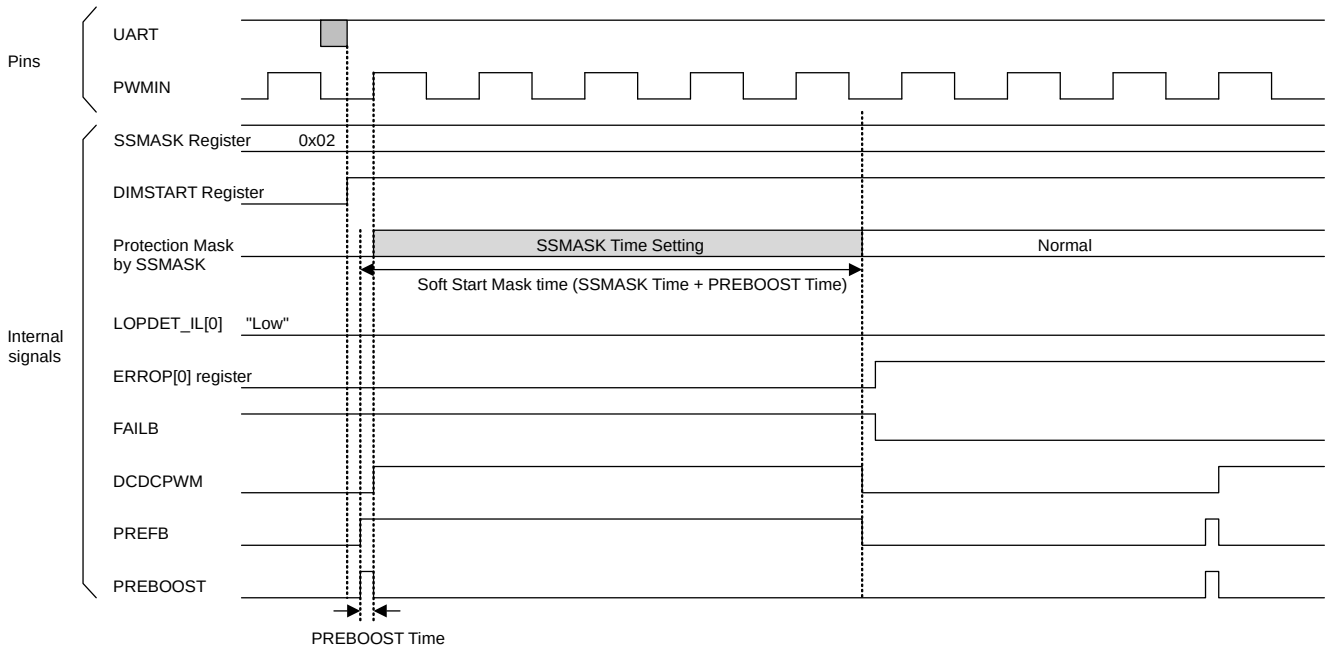


Figure 82. Setting for Soft Start Mask

2. ERROR Control – continued

2.9 SWOCP Protection

SWOCP (External MOSFET over current protection) is detected when V_{IN} - V_{SW} > 1.0 V (Typ). After the 1.5 µs filter, it can detect SWOCP, SWOCPERR status register is “High” and FAILB is “Low”. Release is delayed by 10 ms after detection.

After 10 ms,
if SWOCP protection is still active, filter for 1.5 µs and release after 10 ms.
if SWOCP protection is still not active, release SWOCPERR status register and FAILB output.

This protection is not affected by ERRCLR, ERRMASK and SSMASK.

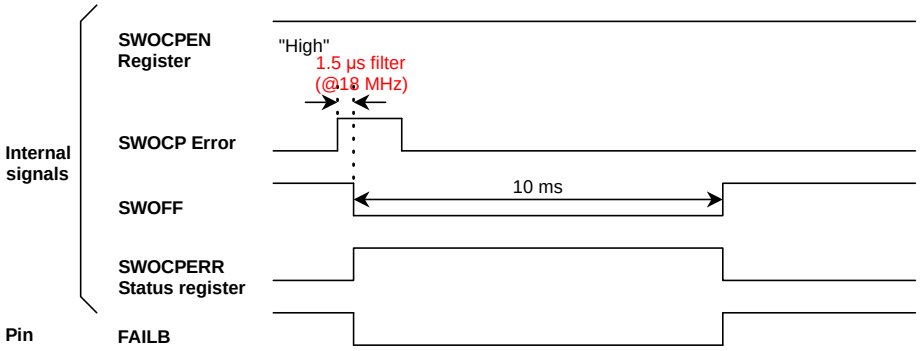


Figure 83. SWOCP Detection Protection

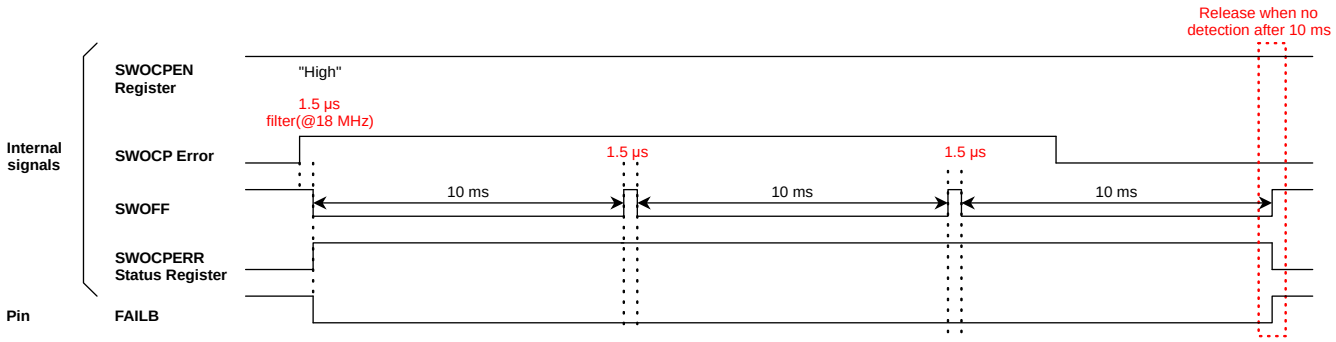


Figure 84. SWOCP Release Condition

2. ERROR Control – continued

2.10 ISET Short Protection

When ISETSEL is High, user can use external resistor to set the ISET current. ISET Short protection is detected when $R_{EXTISET1}$ < 30 kΩ (Typ). When protection is detected continuously for 56 µs (Typ), it sets ISETSHERR status register to High and FAILB output to Low. After released continuously for 56 µs (Typ), it clears status register (ISETSHERR = Low) and FAILB = High.

Depending on ISETSHCNT register setting, output LED or ISETSEL (internal/external selector) can be controlled when ISETSH Error is detected. When ISETSEL is “Low”, this function is not active.

This protection is not affected by ERRMASK and SSMASK.

Register Settings: (x = 01 to 24)
DIMSTART = 1
DIMMODE = 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)
ISETSEL register = 1
ISETSHCNT register = 0x0h or 0x3h
ISETLAT register = 0

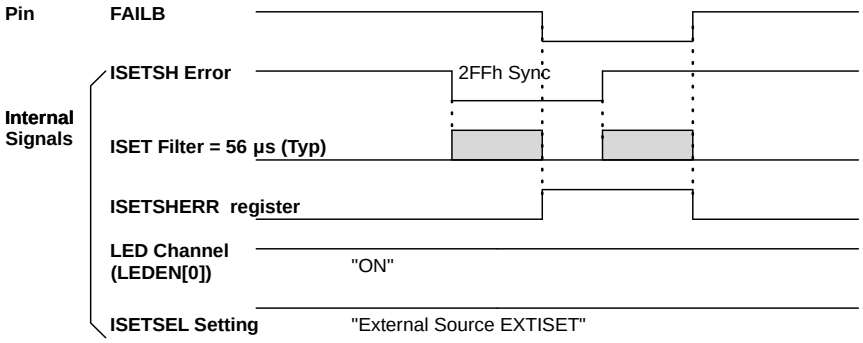


Figure 85. Operation when ISETLAT = 0 and ISETSHCNT = 0

The operation in the diagram above shows the default operation of ISETSH error detection with ISETSHCNT register = 0 and ISETLAT register = 0. Status register and the FAILB pin output can be monitored in this operation. When the protection is released, status register and the FAILB pin output are released.

Register Settings: (x = 01 to 24)
DIMSTART = 1
DIMMODE = 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)
ISETSEL register = 1
ISETSHCNT register = 0x1h
ISETLAT register = 1

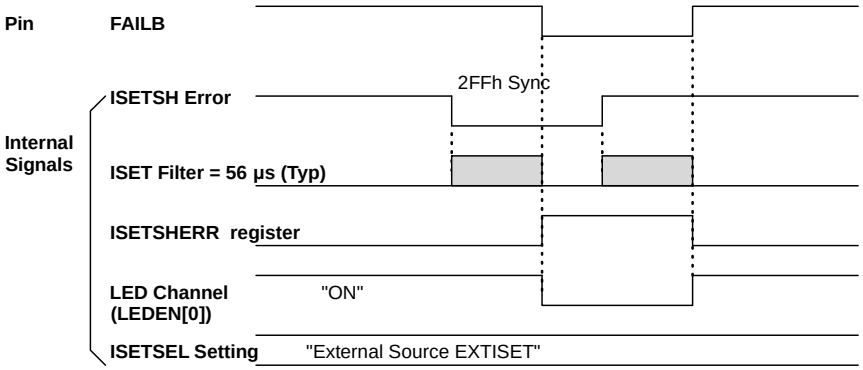


Figure 86. Operation when ISETLAT = 0 and ISETSHCNT = 1

The operation in the diagram above shows the default operation of ISETSH error detection with ISETSHCNT register = 1 and ISETLAT register = 0. Status register and the FAILB pin output can be monitored in this operation. When ISETSH error is detected, LED output turns off. When the protection is released, LED output turns on, status register and FAILB output is released.

2.10 ISET Short Protection – continued

Register Settings: (x = 01 to 24)
DIMSTART = 1
DIMMODE = 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)
ISETSEL register = 1
ISETSHCNT register = 0x2h
ISETLAT register = 0 or 1

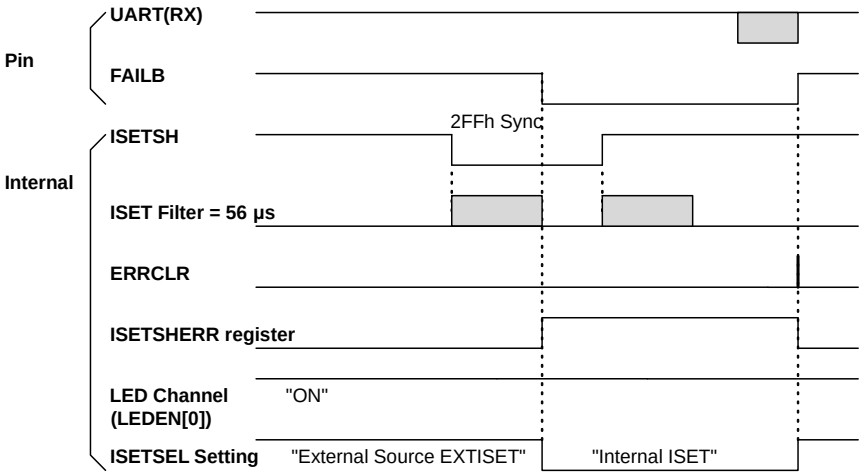


Figure 87. Operation when ISETLAT = 0 or 1 and ISETSHCNT = 2

The operation in the diagram above shows the default operation of ISETSH error detection with ISETSHCNT register = 2 and ISETLAT register = 0. Status register and the FAILB pin output can be monitored in this operation. When ISETSH error is detected, it changes the input selector for LED current setting (ISETSEL) from external to internal source. ERRCLR is necessary to clear this condition. Release condition for 56 µs (Typ) will not release the protection. Upon executing clear condition, input selector for ISET (ISETSEL) returns from internal to external.

Register Settings: (x = 01 to 24)
DIMSTART = 1
DIMMODE = 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)
ISETSEL register = 1
ISETSHCNT register = 0x0h o 0x3h
ISETLAT register = 1

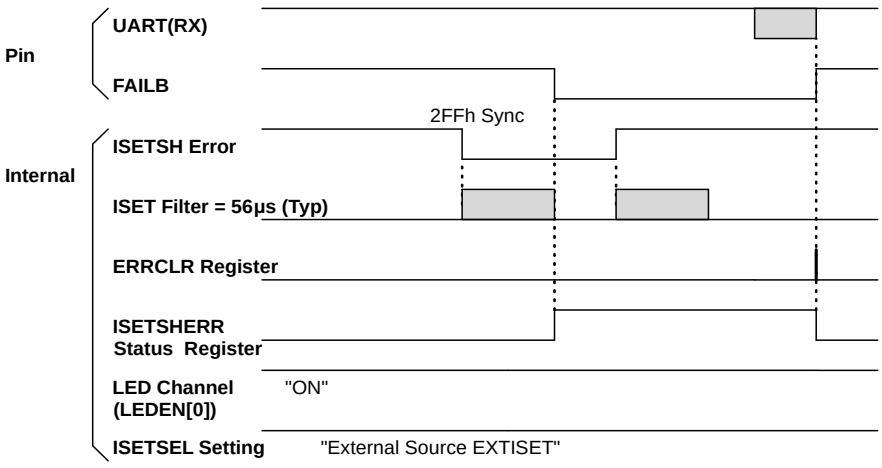


Figure 88. Operation when ISETLAT = 1 and ISETSHCNT = 0

The operation in the diagram above shows the operation of ISETSH error detection with ISETSHCNT register = 0 and ISETLAT register = 1. Status register and the FAILB pin output can be monitored in this operation. Sending ERRCLR is necessary to clear the status register and the FAILB pin output.

2.10 ISET Short Protection – continued

Register Settings: (x = 01 to 24)
DIMSTART = 1
DIMMODE = 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)
ISETSEL register = 1
ISETSHCNT register = 0x1h
ISETLAT register = 1

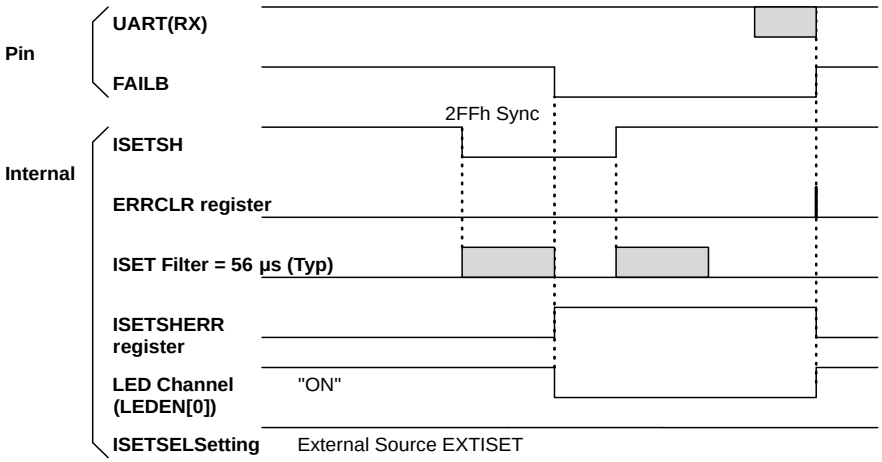


Figure 89. Operation when ISETLAT = 1 and ISETSHCNT = 1

The operation in the diagram above shows the default operation of ISETSH error detection with ISETSHCNT register = 1 and ISETLAT register = 1. Status register and the FAILB pin output can be monitored in this operation. When ISETSH error is detected, LED turns off. Sending ERRCLR is necessary to clear the LED output, status register and the FAILB pin output.

Sequence

1. Start-up Sequence

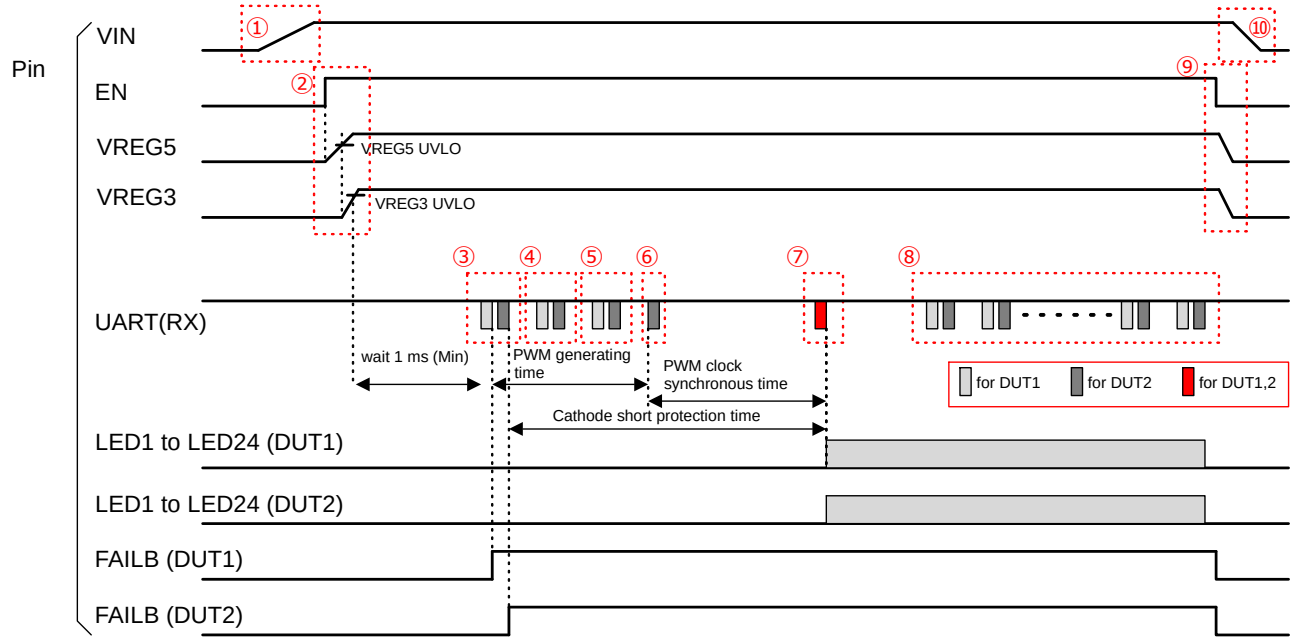


Figure 90. Starting Sequence for Normal Operation

When you light the LED by general UART control, please follow the below sequence.

① Input power supply in the VIN pin.
② Launch the EN pin from “Low” to “High”, the VREG5 and VREG3 pins are generated.
③ Write initial setting from address 0x01h to 0x17h.
Write ERRCLR, to release FAILB. If you write CATHEN, it starts to operate cathode short error.
④ Write initial setting from address 0x18h to 0x2Fh.
⑤ Write initial setting from address 0x30h to 0x4Ah.
⑥ Write SYNCSET register to 10b.
⑦ All device starts dimming at same timing.
⑧ Operate dimming control for each channel.
⑨ Dimming is stopped.
⑩ Stop input power supply in the VIN pin.

Sequence – continued

2. PWM Synchronization Sequence

Sequence (x = 01 to 24)
DUT1 (Leader):
SYNCSET register = 0x1h (Leader)
DIMSETx[7:0] = 0x7Fh (50 % Duty)

DUT2 (Follower):
SYNCSET register = 0x2h (Follower)
DIMSETx[7:0] = 0x7Fh (50 % Duty)

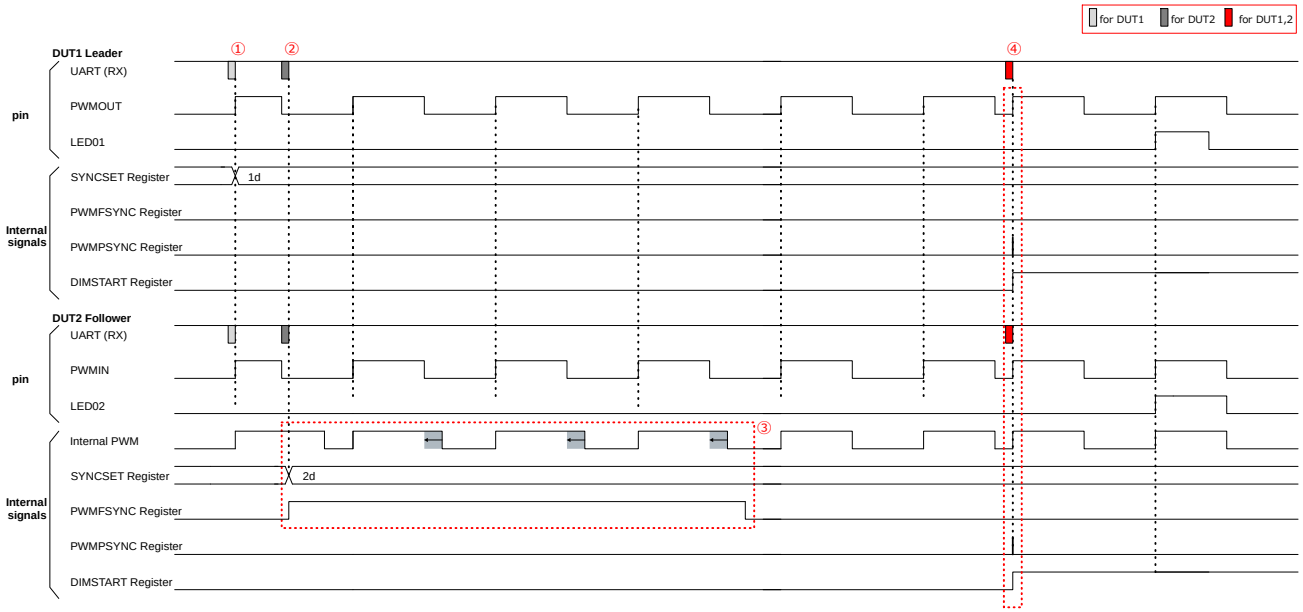


Figure 91. PWM Synchronization Operation

When it synchronizes PWM phase with other device, please follow the sequence below.

① Write SYNCSET register for Leader device. Leader starts to output reference signal from PWMOUT.
② Write SYNCSET register for Follower device. Follower devices start to monitor PWMIN to adjust internal oscillator.
③ When it detects unstable clock condition in Follower devices, PWMFSYNC register = 1. This meaning, internal clock of the Follower device is not yet synchronized to Leader clock. During this time, it is possible to send UART command to read the status of PWMFSYNC, however, internal frequency adjusting stops during UART communication.
④ Write PWMPSYNC and DIMSTART register after clock is already stable. PWMPSYNC command triggers all device to lock the phase of the PWM generation. DIMSTART command triggers all device to start LED output.

Sequence – continued

3. Error Sequence

3.1 Protection Sequence for “LED Open Error” without LOPLAT

Example: Register Settings (x = 01 to 24)
AUTOOFF register = 0
LOPLAT register = 0
LOPEN register = 1
DIMMODE= 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)

Detected “LED open error” in LED1: (n = 1 to 24)

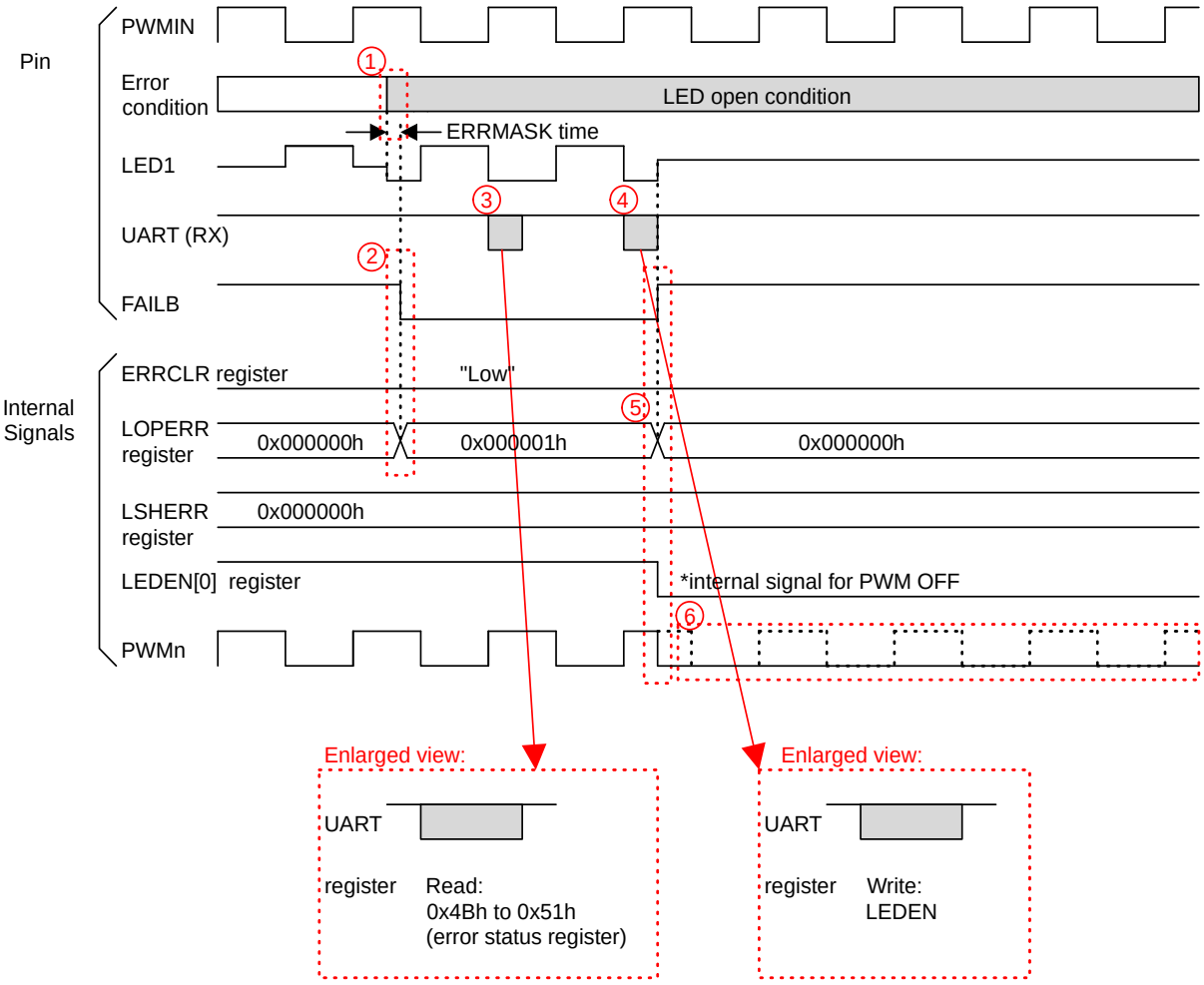


Figure 92. Error Sequence for “LED Open Error” without LOPLAT

① “LED Open Error” is detected after ERRASK time.
If Error condition is released before ERRMASK time setting is reached, Error condition is not detected in FAILB and status register.
② In error detection, corresponding status register (LOPERR) is updated and FAILB = Low.
③ MCU received FAILB = Low condition and issues a read command to status registers (0x4Bh to 0x51h).
④ After confirming status, MCU issues write command to set ”LEDEN[0] = 0” to affected “Error Channel” for protection.
⑤ “Error register” and FAILB return to normal condition.
⑥ Corresponding channel output PWMn = Low.

Note: MCU cannot detect Error condition if “error condition” is cleared before reading “error register”.

3 Error Sequence - continued

3.2 Protection Sequence for “LED Open Error” with LOPLAT

Example: Register Settings (x = 01 to 24)
AUTOOFF register = 0
LOPLAT register = 1
LOPEN register = 1
DIMMODE = 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)

Detected “LED open error” in LED1: (n = 1 to 24)

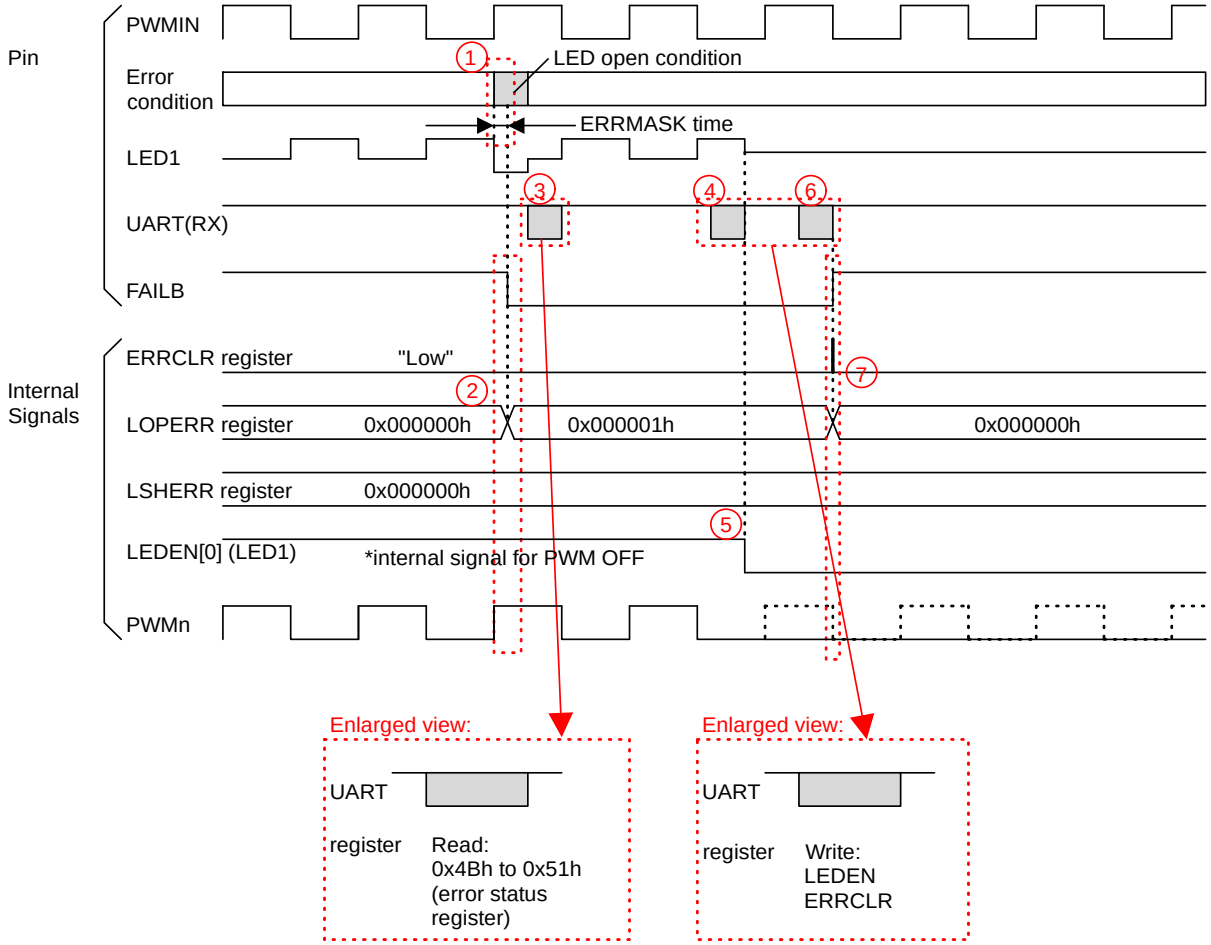


Figure 93. Error Sequence for “LED Open Protection” with LOPLAT

① “LED Open Error” is detected after ERRASK time.
If Error condition is released before ERRMASK time setting is reached, Error condition is not detected in FAILB and status register.
② In error detection, corresponding status register (LOPERR) is updated and FAILB = Low.
③ MCU received FAILB = Low condition and issues a read command to status registers (0x4Bh to 0x51h).
④ After confirming status, MCU issues write command to set ”LEDEN[0] = 0” to affected “Error Channel” for protection.
⑤ Corresponding channel outputs PWMn = Low.
⑥ MCU issues a write command to set ”ERRCLR = 1” to release “latch condition”.
⑦ “Error register” and the FAILB pin output return to normal condition after setting “ERRCLR = 1”.

3 Error Sequence - continued

3.3 Protection Sequence for “LED Open Error” with AUTOOFF

Example: Register Settings (x = 01 to 24)
AUTOOFF register = 1
LOPLAT register = 0
LOPEN register = 1
DIMMODE = 0
DIMSETx[7:0] = 0x7Fh (50 % Duty)

Detected “LED open error” in LED1: (n = 1 to 24)

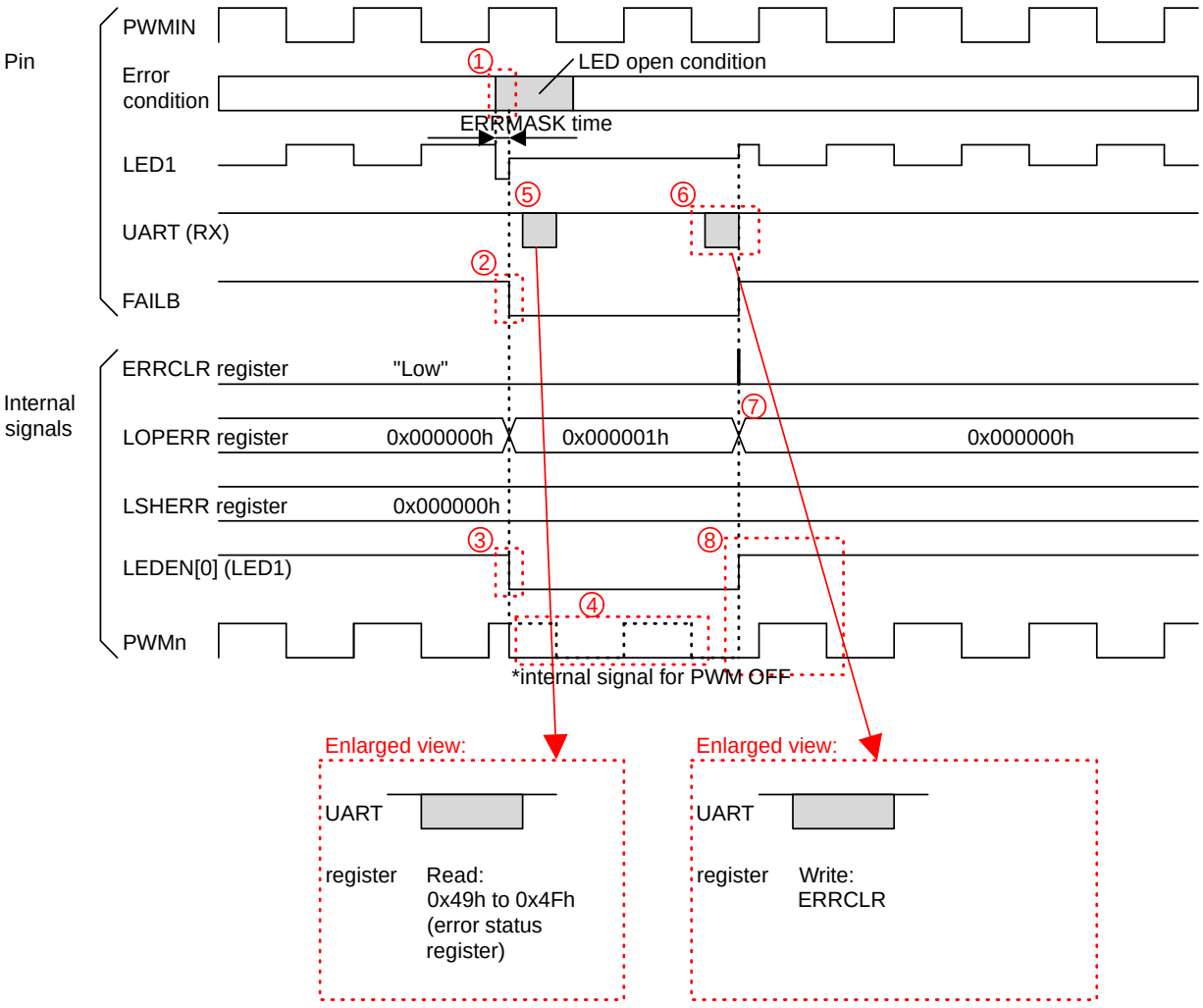


Figure 94. Error Sequence for “LED Open Protection” with AUTOOFF

① “LED Open Error” is detected after ERRMASK time. If Error condition is released before ERRMASK time setting is reached, Error condition is not detected in FAILB and status register.
② In error detection, corresponding status register (LOPERR) is updated and FAILB = Low.
③ Corresponding “LEDEN[0] = 0” of “Error channel” is released automatically due to AUTOOFF Setting.
④ Corresponding channel outputs PWMn = Low.
⑤ MCU reads “Error register” after MCU receives FAILB = Low condition.
⑥ MCU issues a write command to set “ERRCLR = 1” to release “Latch condition” and another write command to set “LEDEN[0] = 1”.
⑦ “Error register” and the FAILB pin output return to normal condition after “ERRCLR = 1”.
⑧ “LEDEN[0] = 1” and PWM output recovered after “ERRCLR = 1”.

3 Error Sequence - continued

3.4 Protection Sequence for “LED Short Error” without LSHLAT

Example: It detects “LED short error” in LED1.

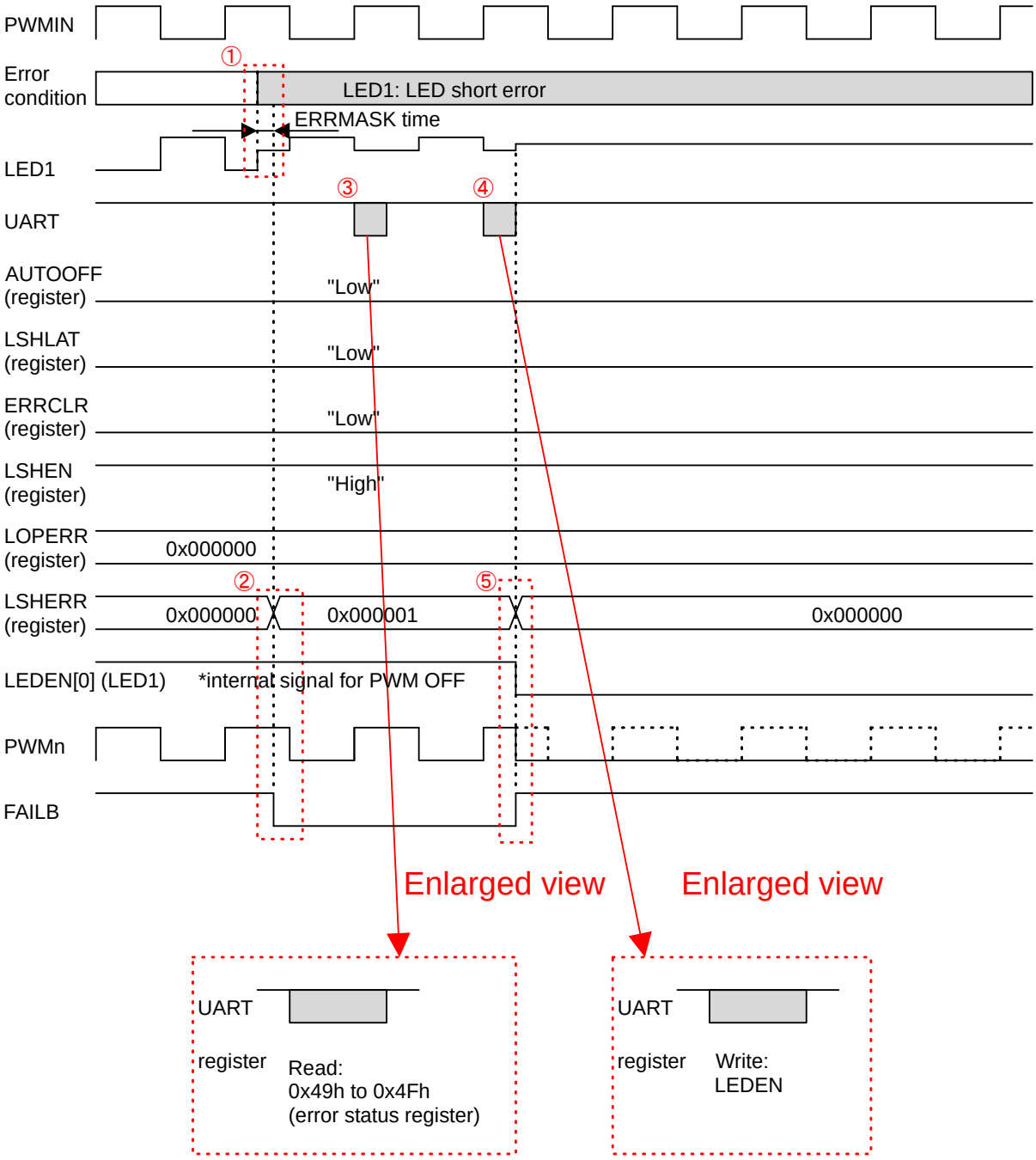


Figure 95. Error Sequence for “LED Short Protection” without LSHLAT

① It detecs “LED short error” after ERRMASK time.
If Error condition is released in this timing, it outputs High from FAILB after ERRMASK.
② it outputs Low from FAILB and update “error register”.
③ MCU reads “Error register” after MCU receives FAILB = Low condition.
④ MCU writes “LEDEN[0] = 0” to “Error Channel” for protection.
⑤ It doesn’t output PWM.
It releases “Error register” and FAILB.

MCU can’t detect Error condition if “error condition” is cleared before reading “error register”.

3 Error Sequence - continued

3.5 Protection Sequence for “LED Short Error” without AUTOOFF

Example: It detects “LED short Error” in LED1.

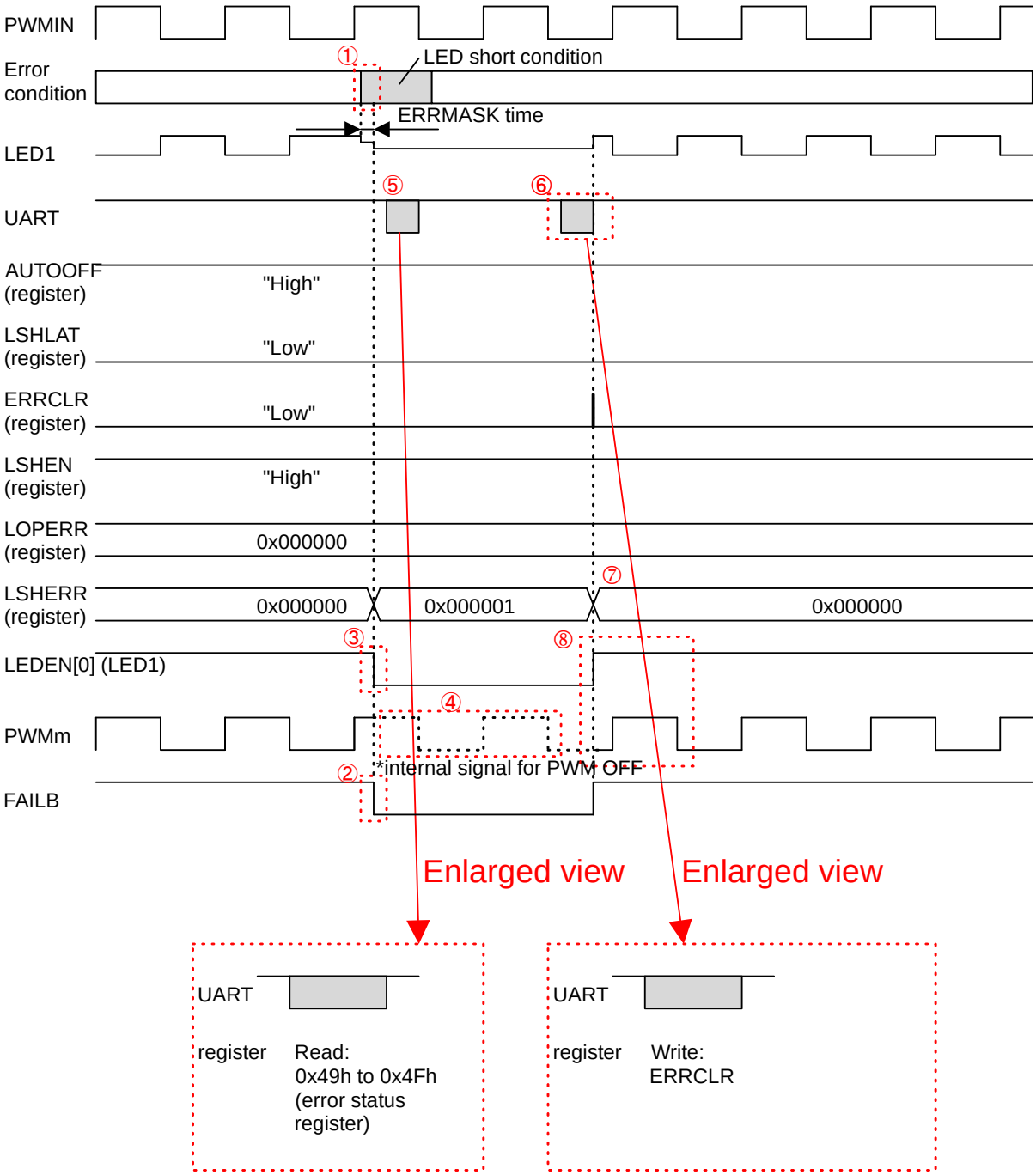


Figure 96. Error Sequence for “LED Short Protection” without ERRLAT

① It detects “LED short error” after ERRMASK time.
If Error condition is released in this timing, it keeps Low in FAILB and “Error register”.
② It outputs Low from FAILB and update “error register”.
③ “LEDEN[0] = 0” of “Error Channel” for protection condition released automatically.
④ It ouputs PWM = Low.
⑤ MCU reads “Error register” after MCU receives FAILB = Low condition.
⑥ MCU writes “ERRCLR = 1” for releasing “Latch condition”.
⑦ “Error register” and FAILB return normal condition after “ERRCLR = 1”.
⑧ “LEDEN[0] = 1” and PWM output recovered after “ERRCLR = 1”.

3 Error Sequence - continued

3.6 Protection Sequence for “CRC Error” without CRCERLAT

Example:
Register Setting
CRCERLAT register = 0
Detected “CRC Error”.

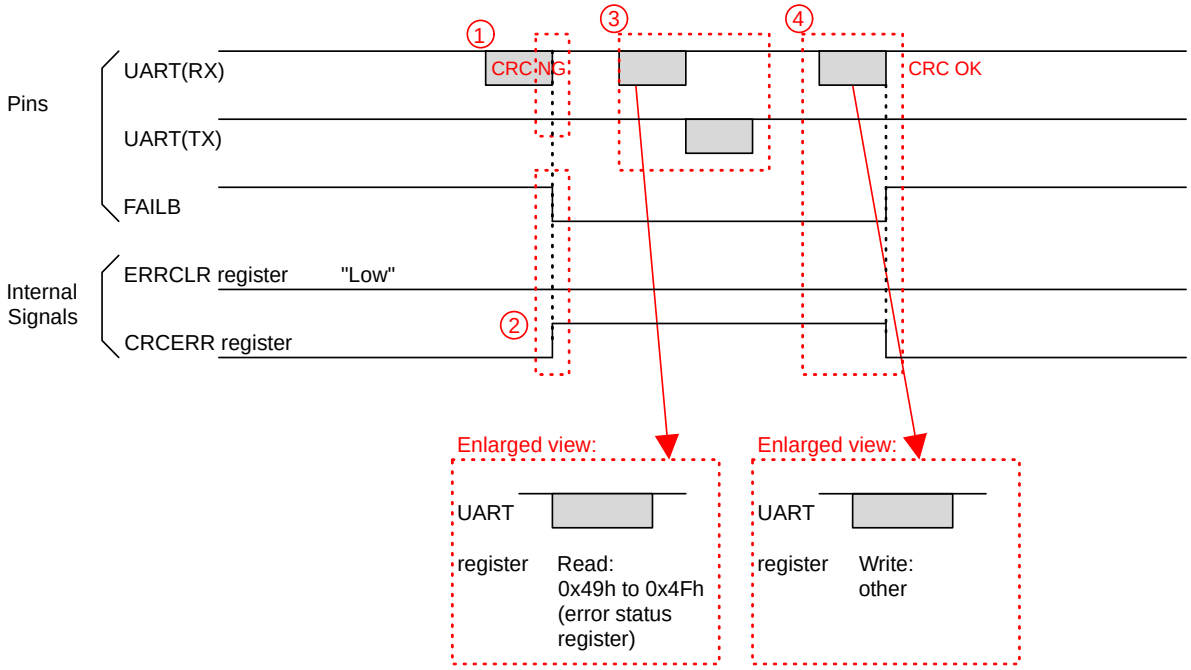


Figure 97. CRC Error Sequence for UART without CRCERLAT

① “CRC Error” is detected due to a communication error in the UART command.
② In error detection, status register (CRCERR) is updated and FAILB = Low.
③ MUC issues read “Error register” after MCU receiving FAILB = Low condition. Read Command does not clear CRC Error status.
④ If MCU write data of “CRC OK”, it outputs FAILB = High and update error register.

3 Error Sequence - continued

3.7 Protection Sequence for “CRC Error” with CRCERLAT

Example:
Register Setting
CRCERLAT register = 1
“CRC Error” is detected.

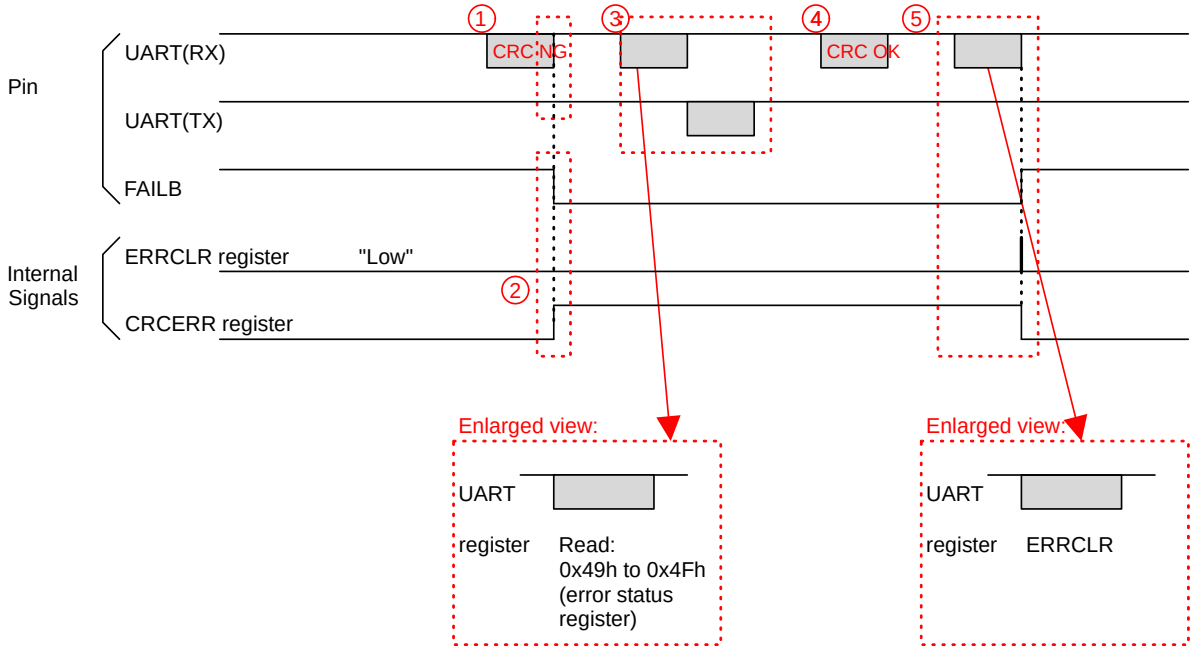


Figure 98. CRC Error Sequence with CRCERLAT

① “CRC Error” is detected due to a communication error in the UART command.
② In error detection, status register (CRCERR) is update and FAILB = Low.
③ MCU reads “Error register” after MCU receives FAILB = Low condition.
④ Read Command does not clear CRC Error status.
⑤ MCU writes “ERRCLR = 1” to release “Latch condition”.
“Error register” and the FAILB pin return normal condition after “ERRCLR = 1”.

3 Error Sequence - continued

3.8 Protection Sequence for “UART WDT Error”

Example:
Register Setting
WDTEN register = 1
It detects “UART WDT Error”.

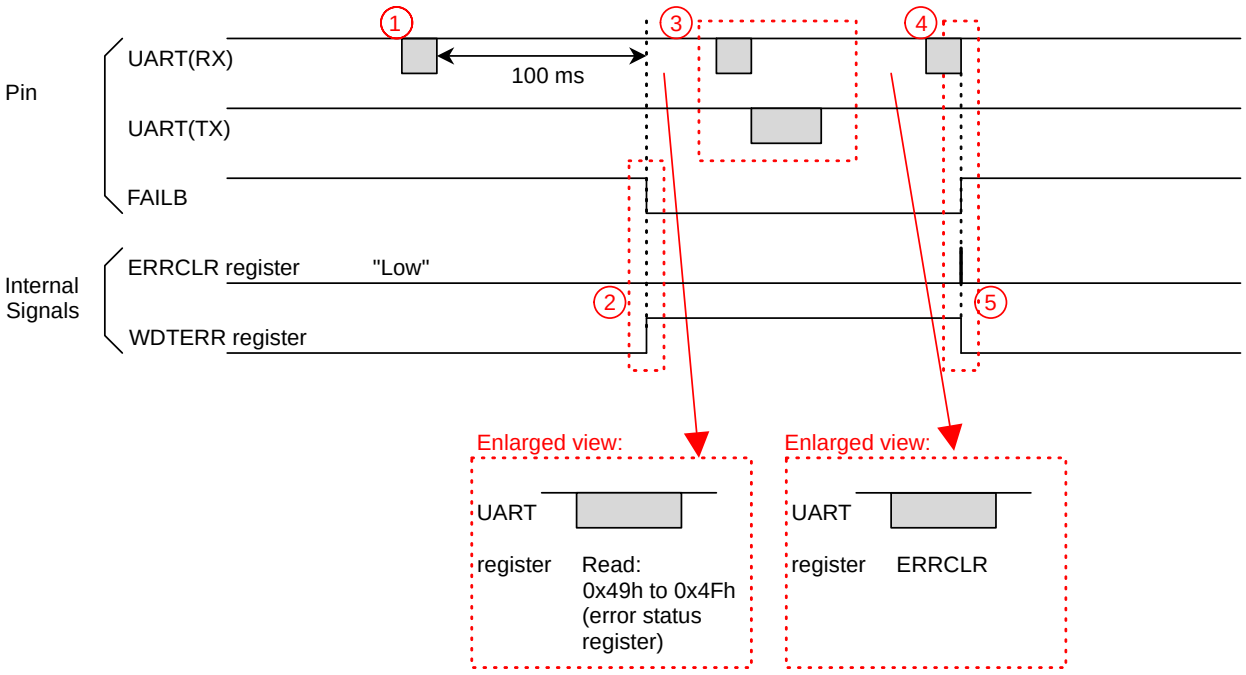


Figure 99. Error Sequence for WDT

① “UART WDT Error” is detected over 100 ms after last UART access.
② In error detection, Error register (WDTERR) and FAILB = Low.
③ MCU read “Error register” after MCU receiving FAILB = Low condition and is automatically latched.
④ MCU writes “ERRCLR = 1” to release “Latch condition”.
⑤ “Error register” and the FAILB pin return normal condition after “ERRCLR = 1”.

Note: MCU cannot detect Error condition if “error condition” is cleared before reading “error register”.

3 Error Sequence - continued

3.9 Protection Sequence for “Cathode Short Error”

Example: “Cathode short error” is detected during turn on.

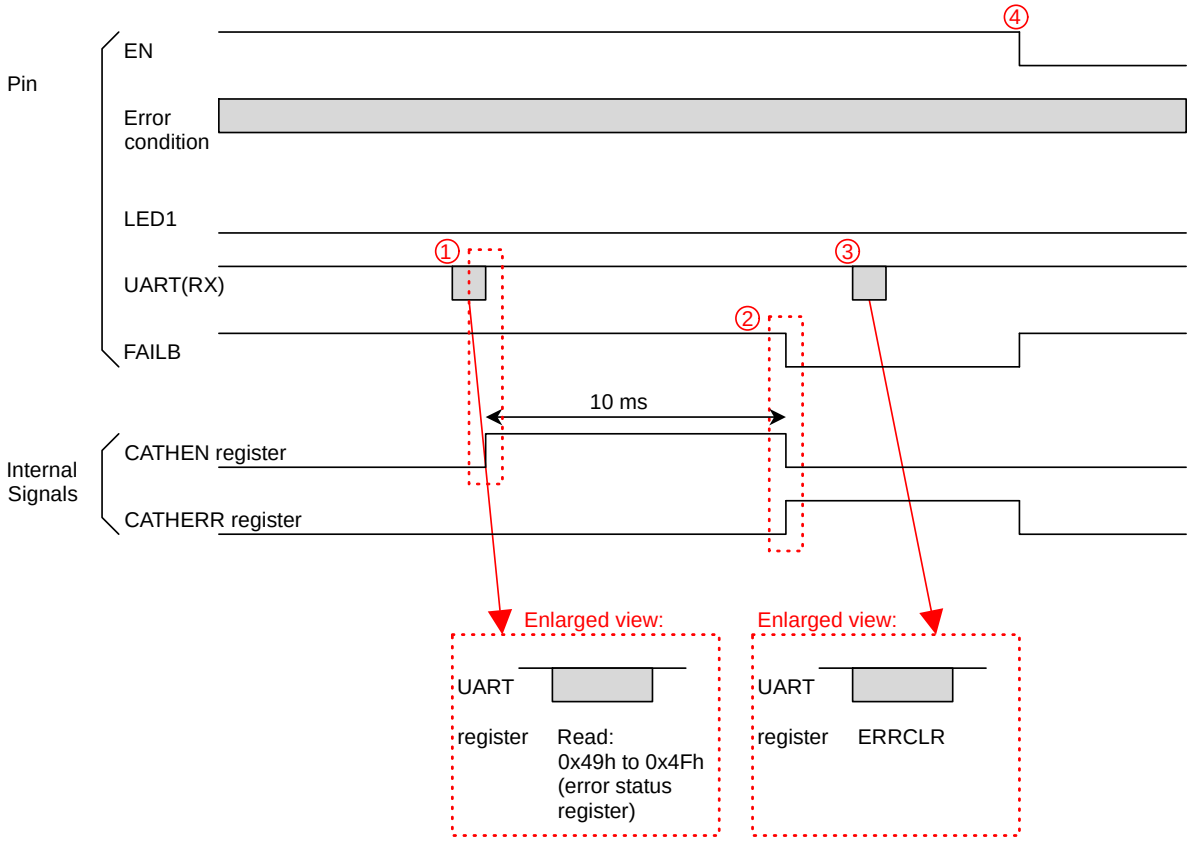


Figure 100. Error Sequence for “Cathode Short Error” without ERRLAT

① MCU writes to CATHEN register to start checking for “Cathode Short Error”.
② “Cathode Short Error” is detected after 10 ms.
Status register (CATHERR) is updated and FAILB = Low.
③ MCU read “Error register” after MCU receiving FAILB = Low condition.
④ Status register (CATHERR) and the FAILB pin return to normal after EN = Low.

Sequence – continued

4. FAILB Control Sequence

This IC can control FAILB output by register setting.

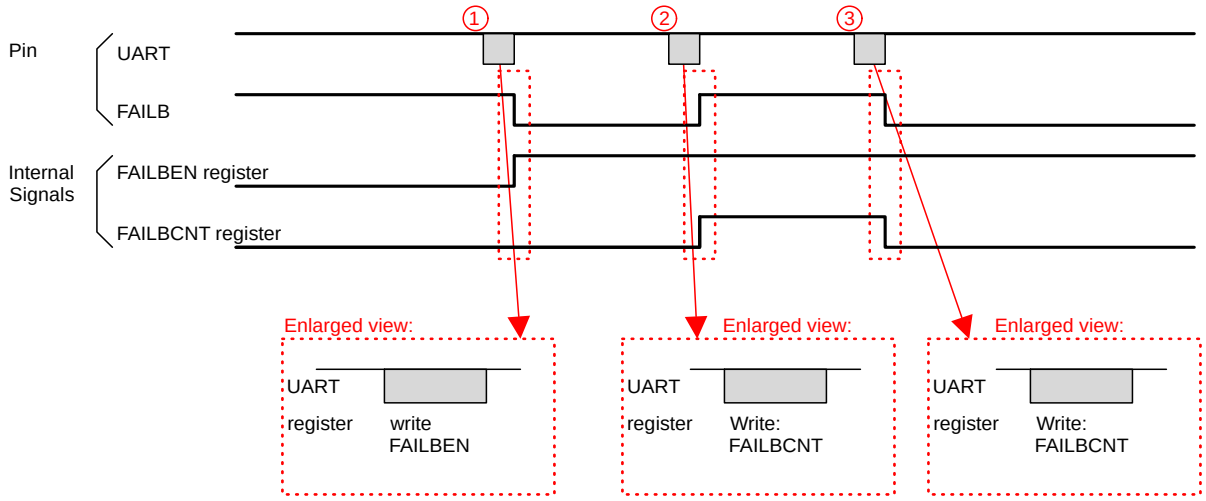


Figure 101. FAILB Control Sequence

① It is available to control FAILB output by FAILBEN = 1.
② FAILBCNT = High, so it outputs High from the FAILB pin.
③ FAILBCNT = Low, so it outputs Low from the FAILB pin.

5. Unused Pin Setting

Please kindly set unused pin following the table below.

Table 64. Unused Pin Setting

Pin Name	Setting	Unused Condition
FAILB	Open	Unused the FAIL Flag.
EXTISET2	Open	Unused the LIMPHOME1 Function.
PWMIN	Open	Unused the External PWM Frequency Synchronization Function.
PWMOUT	Open	Unused the Output PWM Frequency to next Follower device.
LEDx (x = 1 to 24)	Open	Unused the LED pin in application.
PRESIGIN	Open	Unused the Leader/Follower application (IC single use)
DCDCPWMIN	Open	Unused the Leader/Follower application (IC single use)
MINSELV	Open	Unused the Leader/Follower application (IC single use)

LIMPHOME Sequence

This IC can operate lighting in LIMPHOME.

1. CASE1: No Lighting in LIMPHOME

LIMPHOME1: OFF (EXTISET2 = OPEN)
Normal dimming: 120 mA ($R_{EXTISET1}$ = 60 kΩ)
LIMPHOME2: OFF (EXTISET2 = OPEN)

Example: Register Settings (x = 01 to 24)
LIMPEN register = 1
LEXTISET2SEL register = 1
ISETSEL register = 1
DIMMODE register = 0 or 1
LHDTYx[3:0] = 0xFh (100 % Duty)

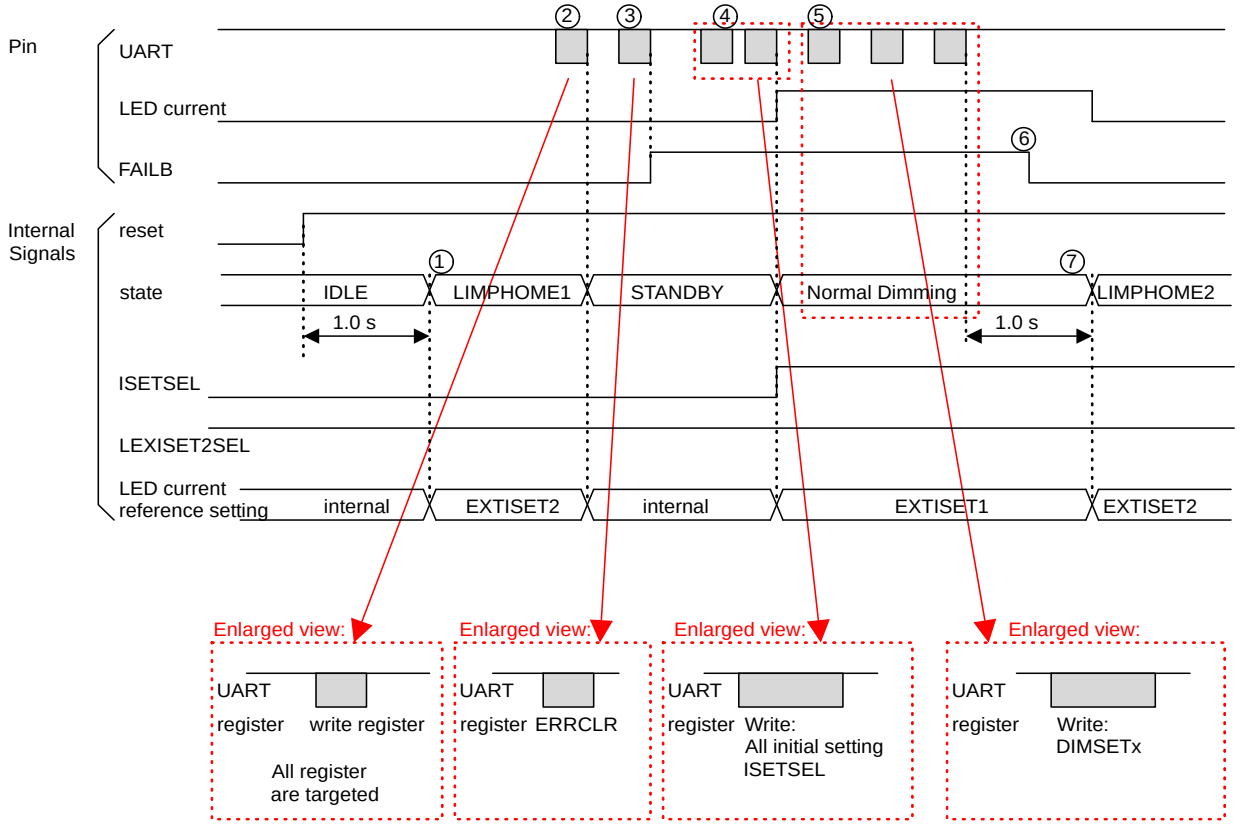


Figure 102. LIMPHOME Function Sequence (Case1)

① If UART are not accessed over 1.0 s from reset released, this IC operates “LIMPHOME1” with EXTISET2 resistor setting ($R_{EXTISET2}$). But, IC starts “No Lighting” in case of the EXTISET2 pin set to “OPEN”.
② If register is written and CRC OK, it operates change from “LIMPHOME1” to “STANDBY” state.
③ If ERRCLR is written, the FAILB pin returns to "High”.
④ All registers are updated for dimming, it starts lighting in DIMSETx[7:0] or DCDIMx[3:0] register setting after DIMSTART = 1. (x = 01 to 24)
⑤ Dimming data are updated.
⑥ If UART are not accessed over 100 ms (WDTEN = 1), it outputs FAILB = Low.
⑦ If UART are not accessed over 1.0 s from last signal, this IC operates “LIMPHOME2” with EXTISET2 resistor setting ($R_{EXTISET2}$). But, IC starts “No Lighting” in case of the EXTISET2 pin set to “OPEN” when Address 0x5Eh (LIMPHOME) set to initial.

LIMPHOME Sequence – continued

2. CASE2: 30 mA in LIMPHOME1 and LIMPHOME2

LIMPHOME1: 30 mA ($R_{EXTISET2}$ = 120 kΩ)
Normal Dimming: 120 mA ($R_{EXTISET1}$ = 60 kΩ)
LIMPHOME2: 150 mA ($R_{EXTISET1}$ = 60 kΩ + $R_{EXTISET2}$ = 120 kΩ)

Example: Register Settings (x = 01 to 24)
LIMPEN register = 1
LEXTISET2SEL register = 1
ISETSEL register = 1
DIMMODE register = 0 or 1
LHDTYx[3:0] = 0xFh (100 % Duty)

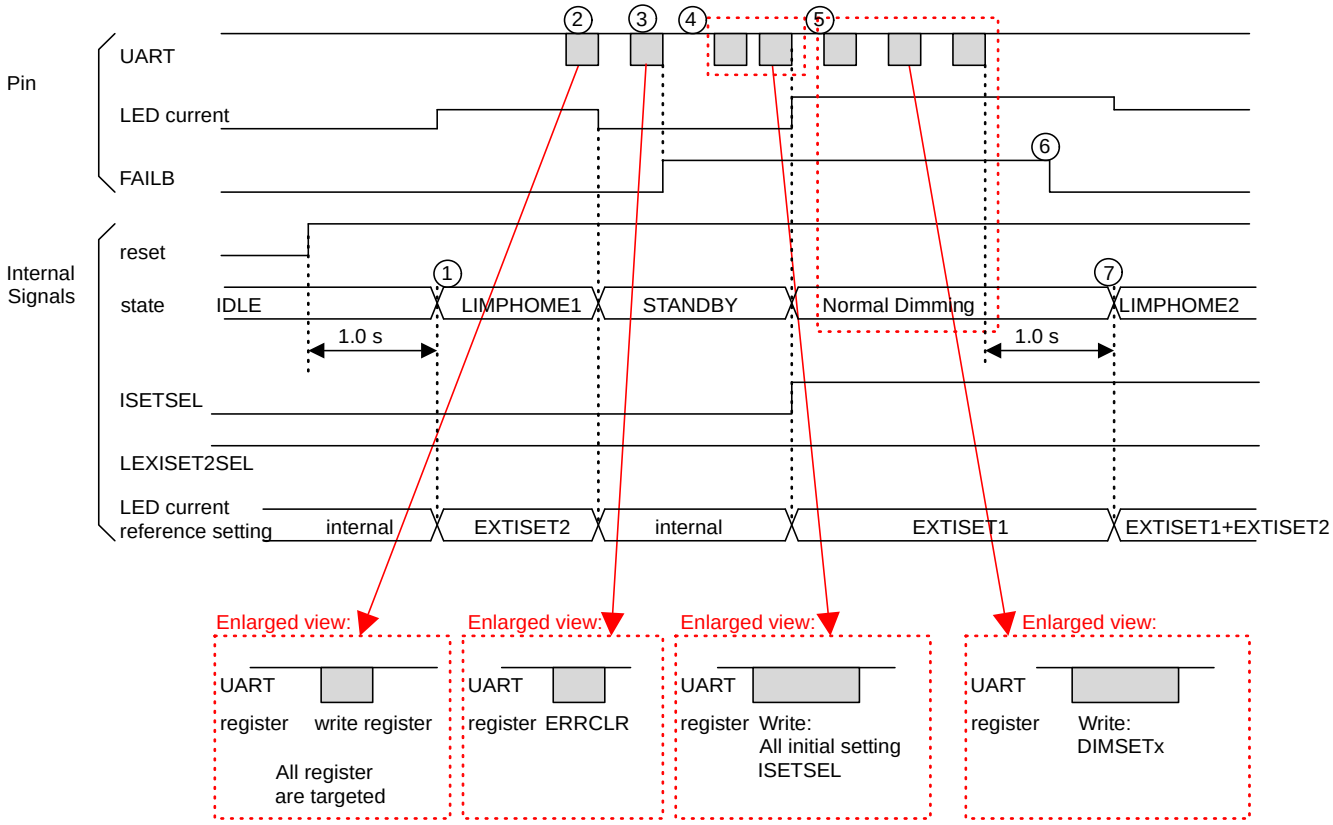


Figure 103. LIMPHOME Function Sequence (Case2)

① If UART are not accessed over 1.0 s from reset released, this IC operates “LIMPHOME1” with EXTISET2 resistor setting ($R_{EXTISET2}$).
② If register is written and CRC OK, it operates change from “LIMPHOME1” to “STANDBY” state.
③ If ERRCLR is written, the FAILB pin turns to “High”.
④ All registers are updated for dimming, it starts lighting in DIMSETx[7:0] or DCDIMx[3:0] register setting after DIMSTART = 1. (x = 01 to 24)
⑤ Dimming data are updated.
⑥ If UART are not accessed over 100 ms (WDTEN = 1), it outputs FAILB = Low.
⑦ If UART are not accessed over 1.0 s from last signal, this IC operates “LIMPHOME2” with EXTISET2 resistor setting ($R_{EXTISET2}$) when Address 0x5Eh (LIMPHOME) set to initial.
DC Dimming is changed from DIMSETx[7:0] (DIMMODE = 1) or DCDIMx[3:0] (DIMMODE = 0) at “LIMPHOME2” status. And, PWM Dimming is changed from LHDTYx[3:0] regiser setting.
(x = 01 to 24)

LIMPHOME Sequence – continued

3. CASE3: Mix Setting in LIMPHOME1 and LIMPHOME2

LIMPHOME1: 0 mA (EXTISET2 = OPEN)
Normal Dimming: 120 mA ($R_{EXTISET1}$ = 60 kΩ)
LIMPHOME2: 120 mA ($R_{EXTISET1}$ = 60 kΩ)

Example: Register Settings (x = 01 to 24)
LIMPEN register = 1
LEXTISET2SEL register = 0
ISETSEL register = 1
DIMMODE register = 0 or 1
LHDTYx[3:0] = 0xFh (100 % Duty)

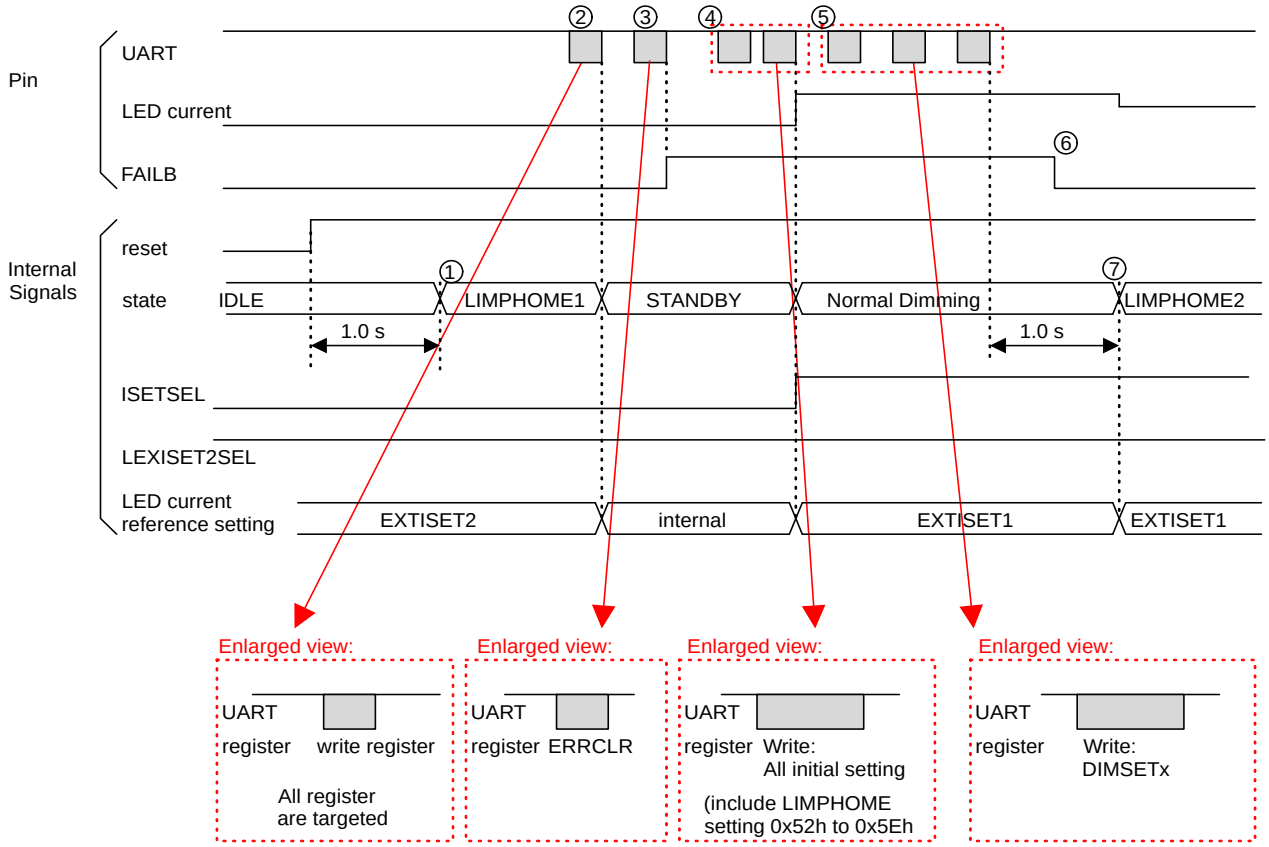


Figure 104. LIMPHOME Function Sequence (Case3)

① If UART are not accessed over 1.0 s from reset released, this IC operates “LIMPHOME1” with EXTISET2 resistor setting ($R_{EXTISET2}$). But, IC starts “No Lighting” in case of the EXTISET2 pin set to 1.0 V or “OPEN”.
② If register is written and CRC OK, it operates change from “LIMPHOME1” to “STANDBY” state.
③ If ERRCLR is written, the FAILB pin turns to "High”.
④ All registers are updated for dimming. we should use continuous writing when we write LIMPHOME register. LIMPHOME register don’t split “updated” and “not updated”. It starts lighting in DIMSETx[7:0] or DCDIMx[3:0] register setting after DIMSTART = 1. (x = 01 to 24)
⑤ Dimming data are updated.
⑥ If UART are not accessed over 100 ms (WDTEN = 1), it outputs FAILB = Low.
⑦ If UART are not accessed over 1.0 s from last signal, this IC operates “LIMPHOME2” with internal ISET setting (60 mA) when Address 0x5Eh (LIMPHOME) set to 0x01h (LEXTISETSEL = 0) and ISETSEL = 0.

Application Examples

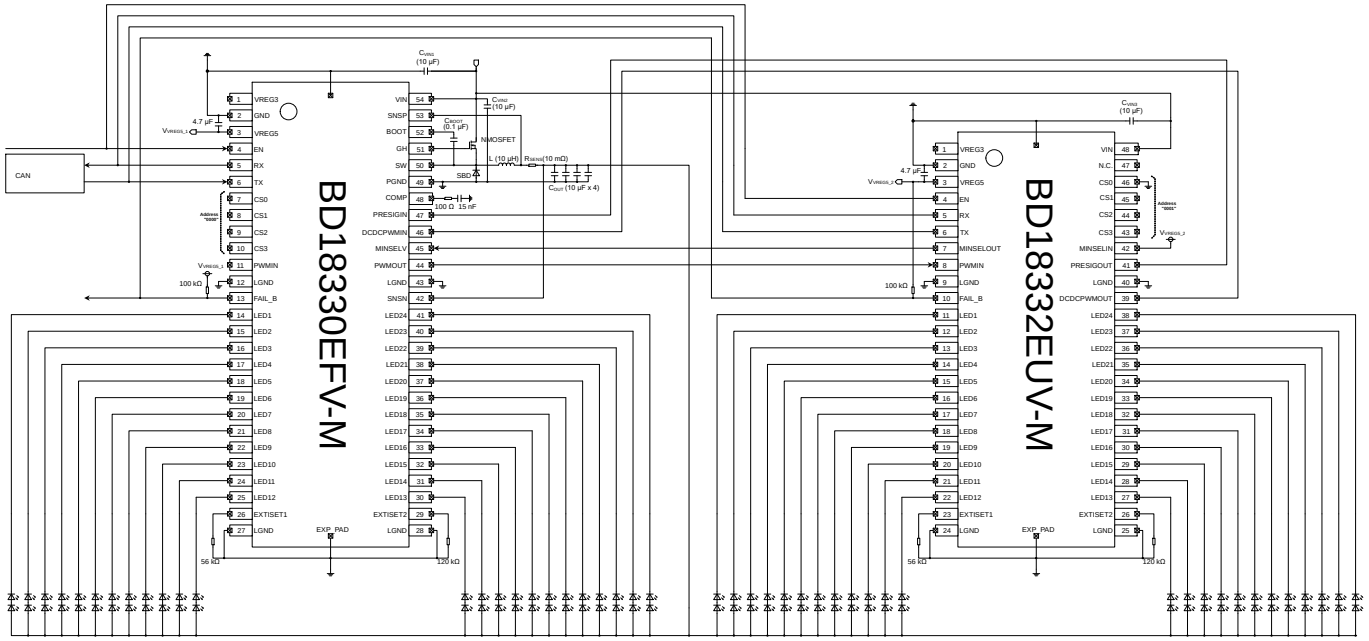
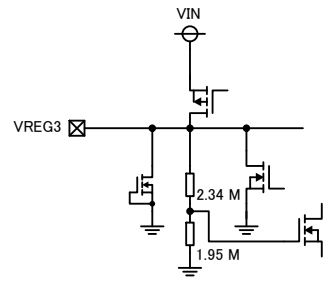
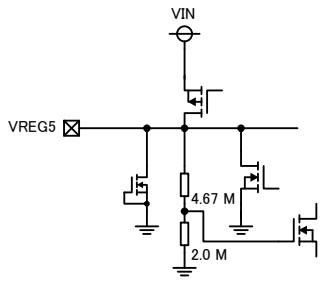
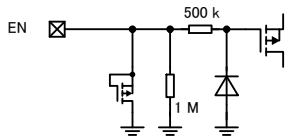
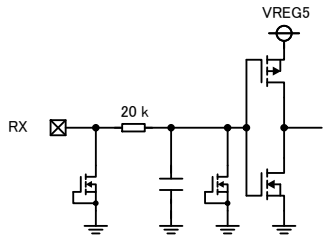
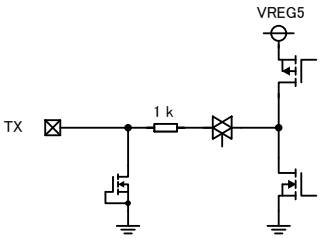
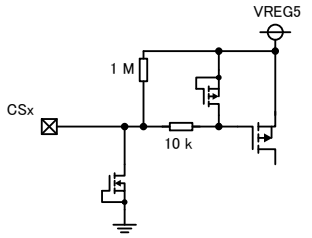
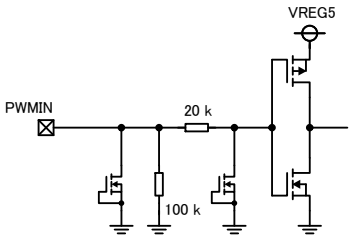
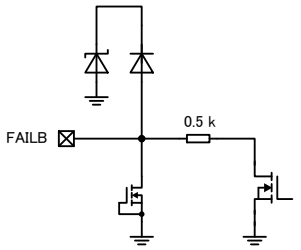
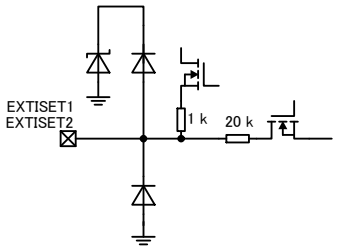
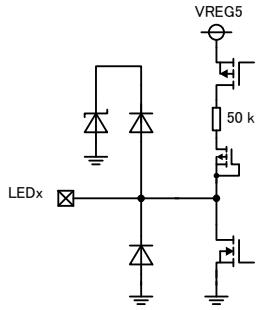
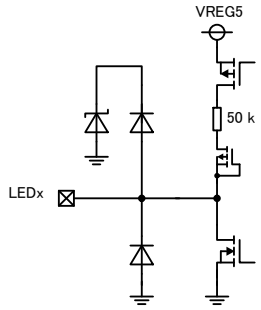
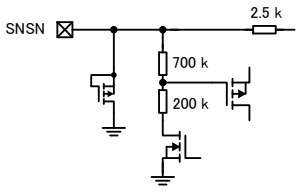
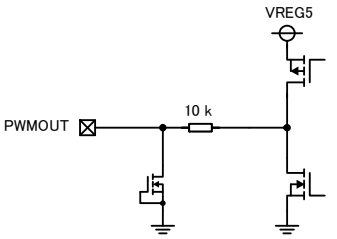
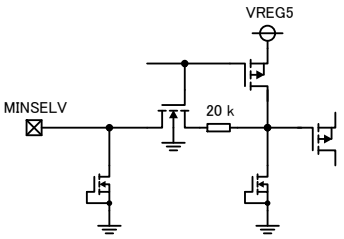
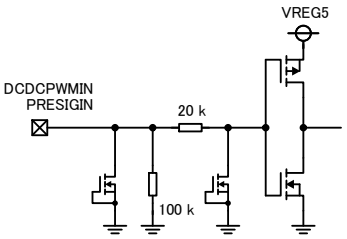
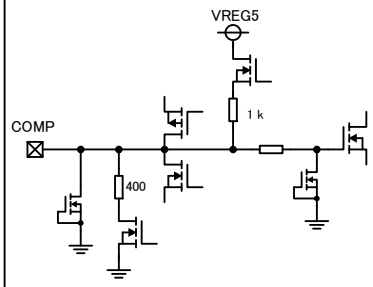
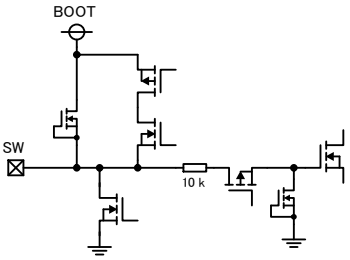
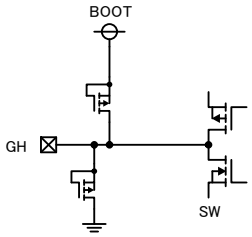
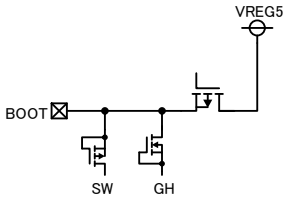
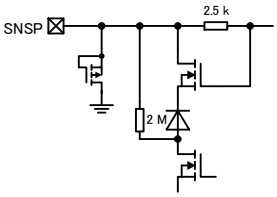


Figure 105. Leader (BD18330EFV-M) and Follower (BD18332EUV-M) Connection Application Example

I/O Equivalence Circuit

1. VREG3	3. VREG5	4. EN
		
5. RX	**6. TX**	**7. to 10. CSx (x = 0 to 3)**
		
11. PWMIN	**13. FAILB**	**26,29. EXTISET1, EXTISET2**
		
14 to 25. LEDx (x = 1 to 12)	**30 to 41. LEDx (x = 13 to 24)**	**42. SNSN**
		
44. PWMOUT	**45. MINSELV**	**46,47. DCDCPWMIN, PRESIGIN**
		

I/O Equivalence Circuit – continued

48. COMP	50. SW	51. GH
		
52. BOOT	**53. SNSP**	
		

Ordering Information

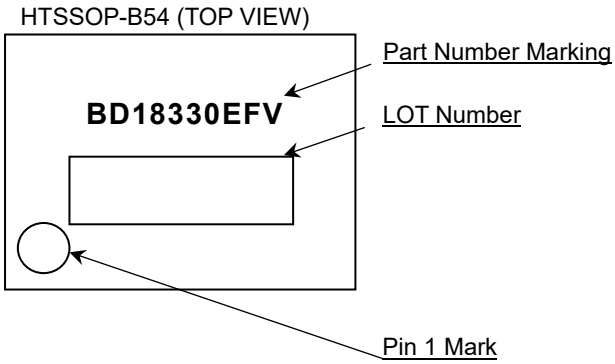
B	D	1	8	3	3	0	E	F	V	-	M	E2

Part Number

Package
EFV: HTSSOP-B54

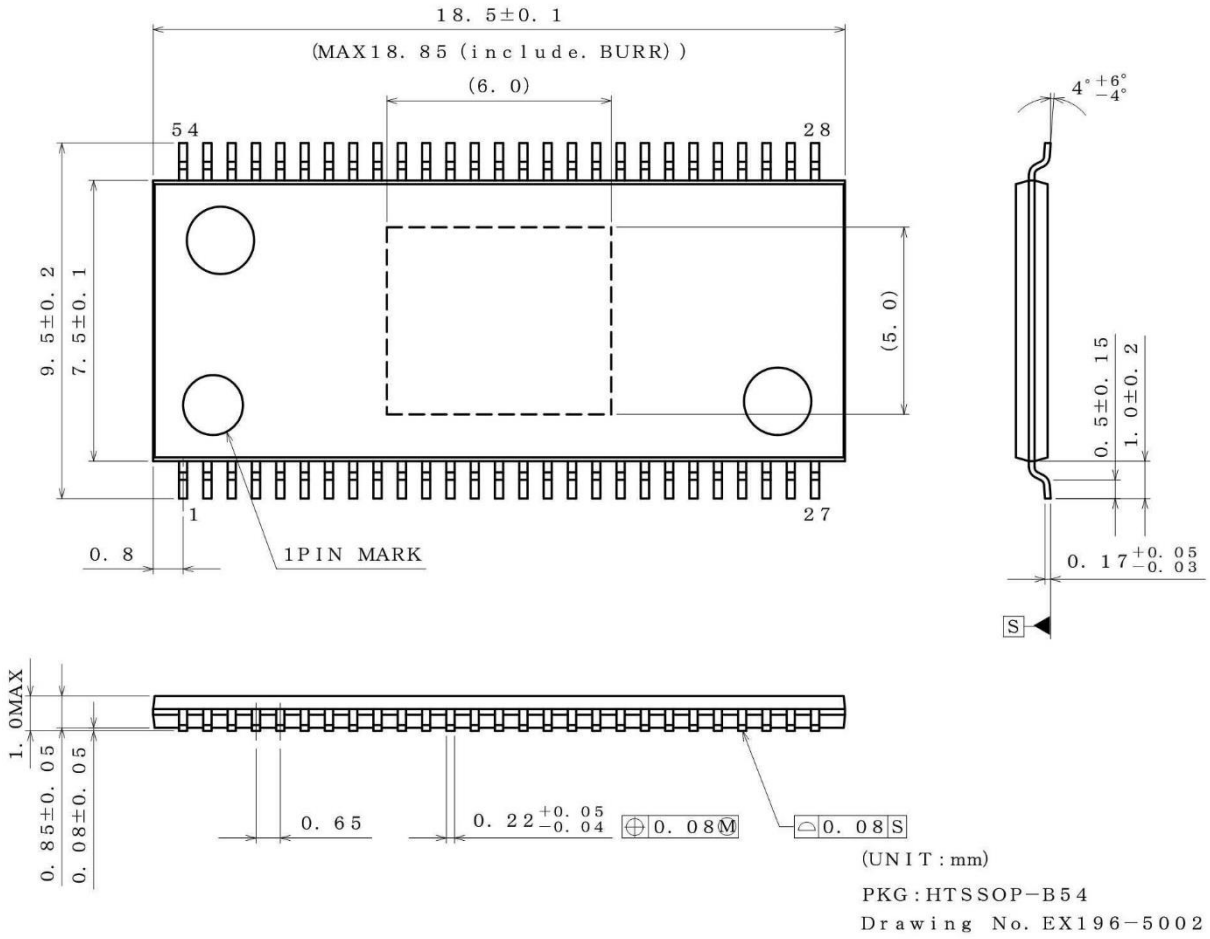
Packing and Forming Specification
M: For Automotive
E2: Embossed Tape and Reel

Marking Diagram



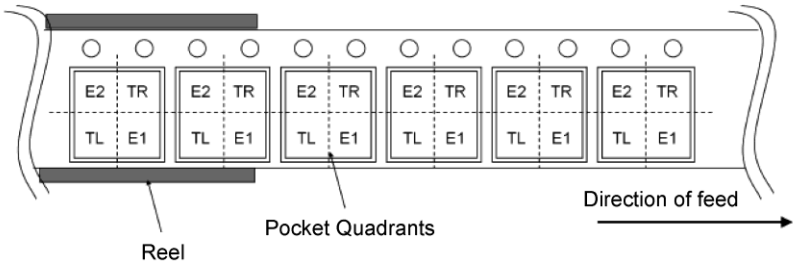
Physical Dimension and Packing Information

Package Name	HTSSOP-B54



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

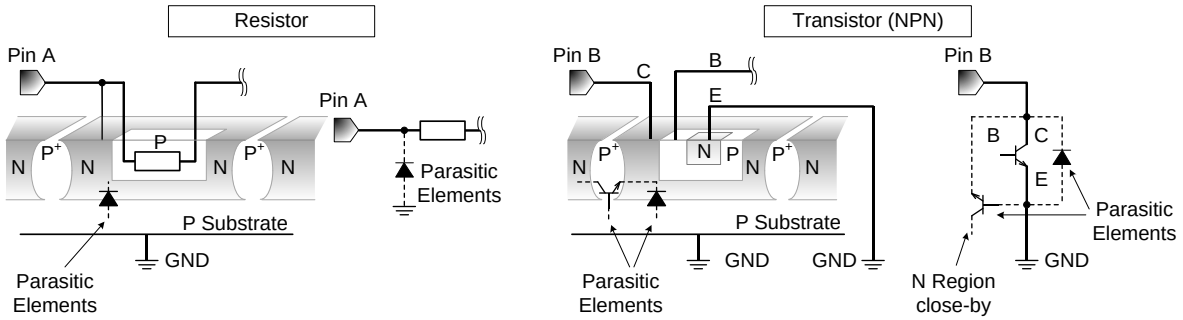


Figure 106. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Operational Notes – continued

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

14. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"

A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"

A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Revision History

Date	Revision	Changes
25.Apr.2023	001	1st released
20.Jun.2024	002	P1. Modify to Figure 1 (Application Circuit)

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.