Datasheet

AC/DC Converter IC

Primary Side Feedback Quasi Resonant Built-in 900 V MOSFET Flyback Converter IC

BM2QH0x13FS-Z

General Description

This series is a primary side feedback type AC/DC control IC. Built-in 900 V MOSFET, startup circuit, and resistors contribute to component reduction and low standby power consumption. The control method adopts Quasi Resonant to achieve low EMI and high efficiency. Optimized sampling timing during primary side feedback operation greatly improves load regulation characteristics. The SSOP-A20_16A high heat dissipation, surface mount type package is used to help reduce mounting costs.

Features

- Photocoupler Less by Primary Side Feedback
- Quasi Resonant Control / Current Mode
- Built-in 900 V Withstand Voltage Element / MOSFET / Startup Circuit / Resistor
- Frequency Reduction Function
- Brown IN / OUT Function (BR UVLO / BR OVP)
- VCC UVLO / VCC OVP
- FB Pin Resistance Open
- Timeout Function
- Overcurrent Limiter with AC Voltage Correction
- Overload Protection
- Dynamic Overcurrent Protection
- SOURCE Pin Open / Short Protection
- Soft Start Function
- TSD Function

Applications

- Air Conditioner, Smart Meter, Ceiling Fan, etc.

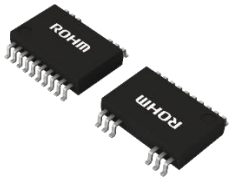
Key Specifications

- Operating Power Supply Voltage Range
  VCC: 8.6 to 30.0 V
  VH, DRAIN: 900 V (Max)
- Switching Operation Current: 0.9 mA (Typ)
- Operating Current: 0.80 mA (Typ)
- Max Frequency Limit: 120 kHz (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

W (Typ) x D (Typ) x H (Max)

SSOP-A20_16A 8.7 mm x 7.8 mm x 2.0 mm
pitch 0.8 mm

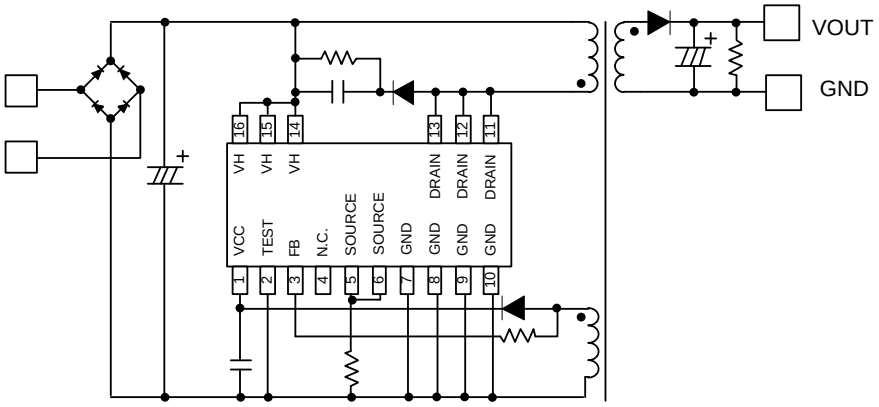


Lineup

Product Name	MOSFET R_{ON} (Typ)	BR UVLO V_{BRUVLO} (Typ)	BR OVP V_{BROVP} (Typ)
BM2QH0A13FS-Z	12.9 Ω	84.6 V	-
BM2QH0B13FS-Z	12.9 Ω	-	-
BM2QH0C13FS-Z	12.9 Ω	98.7 V	705 V
BM2QH0D13FS-Z	12.9 Ω	84.6 V	705 V

B, D series are under development

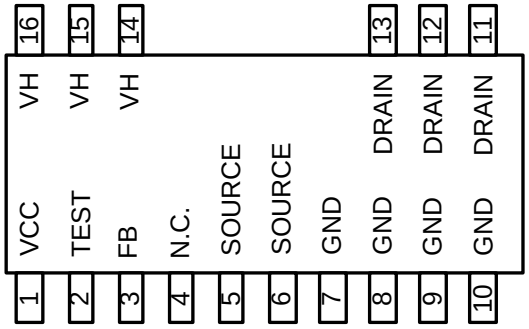
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

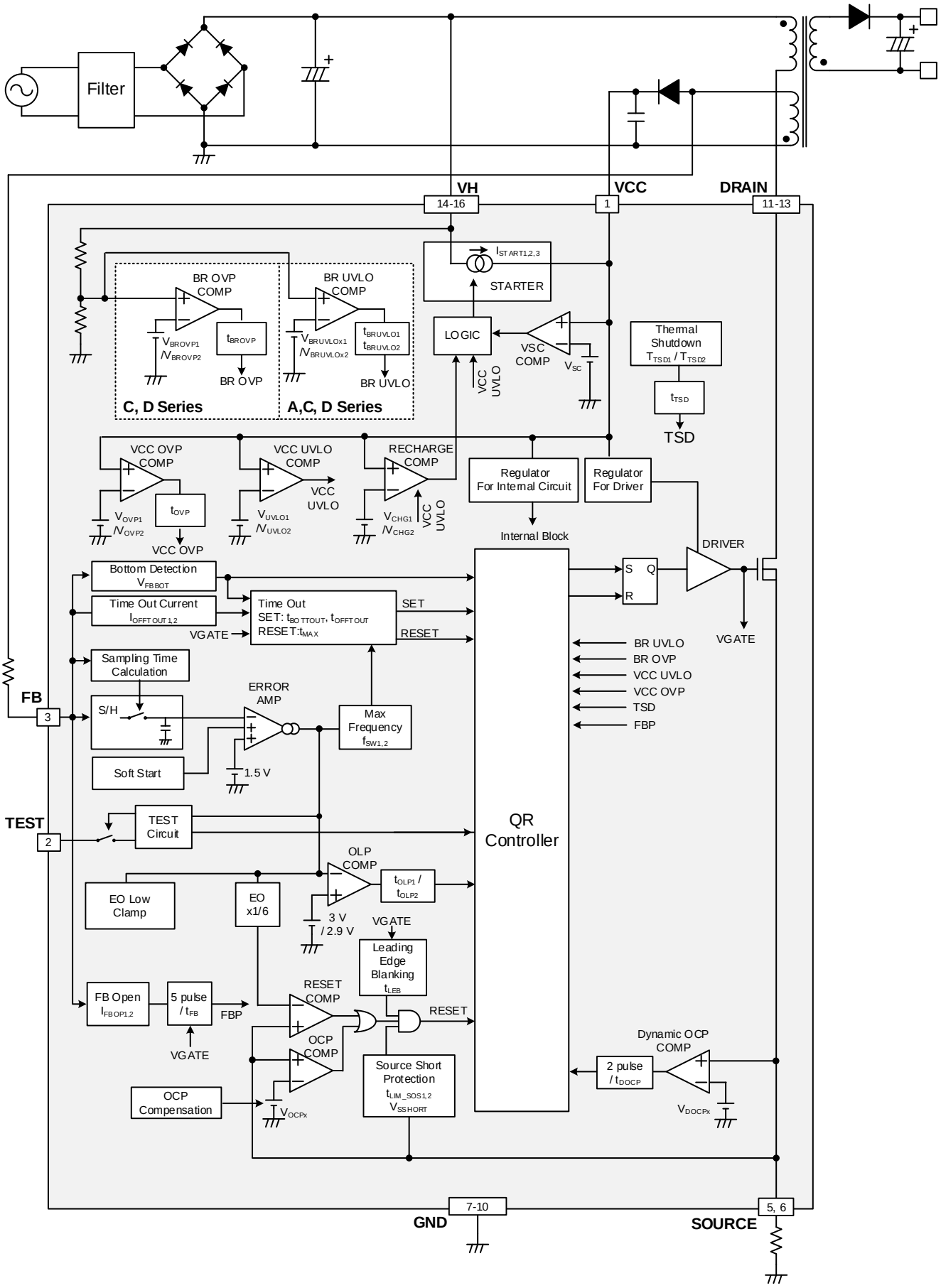
[TOP VIEW]



Pin Description

No	Pin	I/O	Function	ESD Diode	
				VCC	GND
1	VCC	I	VCC Input	-	○
2	TEST	-	TEST Pin. Connect to GND	-	○
3	FB	I	Feed Back / Bottom Voltage Detection	-	○
4	N.C.	-	No Connection	-	-
5	SOURCE	I	MOSFET SOURCE	-	○
6	SOURCE	I	MOSFET SOURCE	-	○
7	GND	I/O	GND	○	-
8	GND	I/O	GND	○	-
9	GND	I/O	GND	○	-
10	GND	I/O	GND	○	-
11	DRAIN	I/O	MOSFET DRAIN	-	○
12	DRAIN	I/O	MOSFET DRAIN	-	○
13	DRAIN	I/O	MOSFET DRAIN	-	○
14	VH	I	High Voltage Input	-	○
15	VH	I	High Voltage Input	-	○
16	VH	I	High Voltage Input	-	○

Block Diagram



Description of Blocks

1. Startup, Shutdown

Timing charts for startup and shutdown are shown. Details are provided in each chapter.

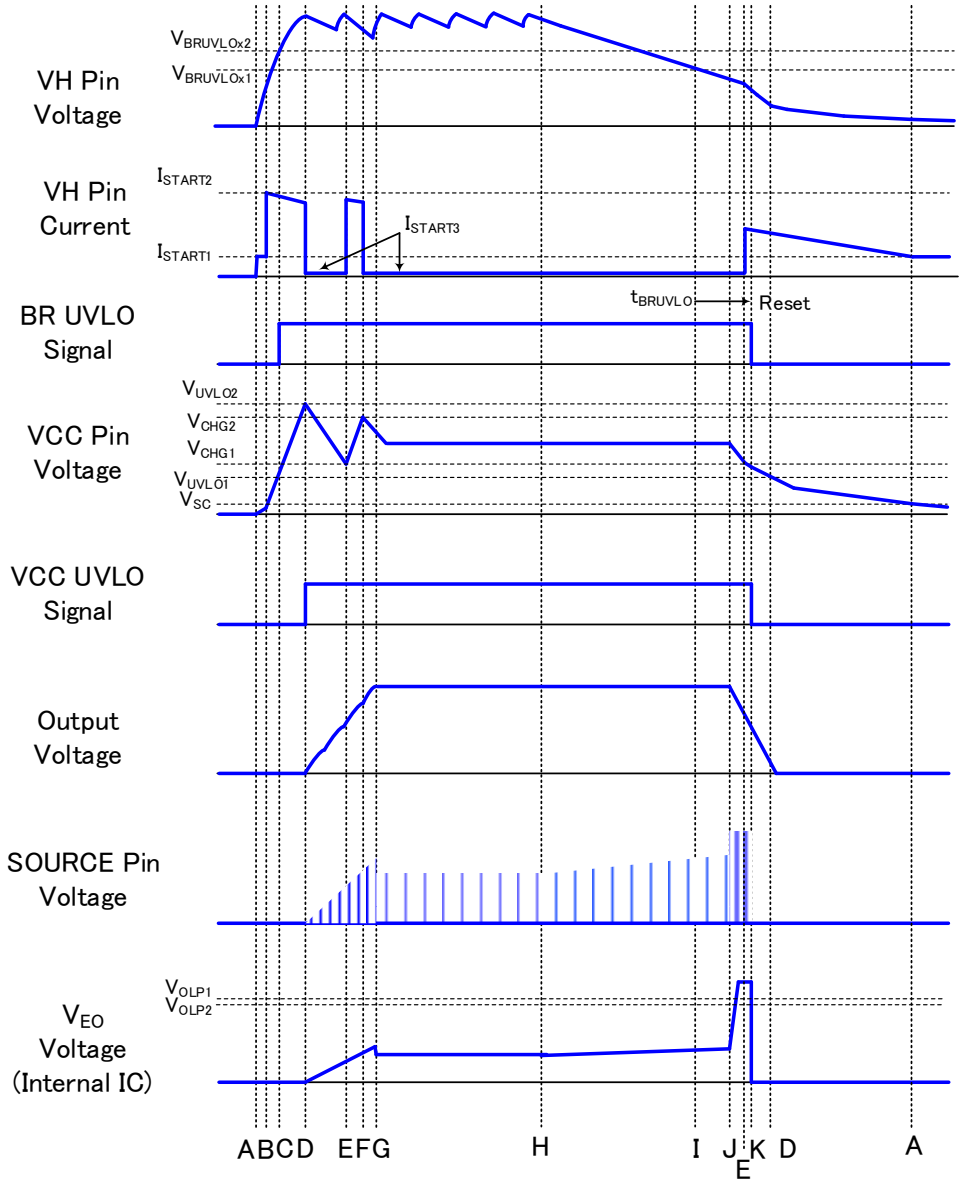


Figure 1. Startup and Shutdown Timing Chart

A: AC voltage input is applied and the VH pin voltage rises. I_{START1} current is charged from VH pin to VCC pin. (Refer 1.1 Startup Circuit about detail of I_{START1} current)
B: VCC voltage > V_{SC}, VCC charging current is switched to I_{START2}. (Refer 1.1 Startup Circuit about detail of I_{START2} current)
C: VH voltage > $V_{BRUVLOx2}$, BR UVLO releases.
D: VCC voltage > V_{UVLO2}, VCC UVLO releases, and soft start function activates. And VCC charging current is switched to I_{START3}. (Refer 1.1 Startup Circuit about detail of I_{START3} current)
E: VCC voltage < V_{CHG1}, charging to the VCC pin starts.
F: VCC voltage > V_{CHG2}, charging to the VCC pin stops.
G: The output voltage reaches the set value.
H: As AC voltage input stops, VH voltage starts to discharge.
I: When VH voltage < $V_{BRUVLOx1}$, BR UVLO is detected. Timer count starts.
J: As the VH voltage drops, the output voltage and VCC voltage also start to drop.
K: When VCC voltage < V_{UVLO1}, VCC UVLO is detected, and operation stops. BR UVLO timer count is reset.

1. Startup, Shutdown - continued

1.1 Startup Circuit

This IC has various built-in functions to enhance the speed and safety of startup.

Starter Circuit

This circuit enables high speed startup by supplying current from VH pin to VCC at startup. The charge current is controlled by VCC voltage level.

VCC UVLO (Under Voltage Lockout) Circuit

When VCC pin voltage < V_{UVLO1}, IC stops operation and resets it. When the VCC pin voltage > V_{UVLO2}, it resumes operation.

Recharge Function

When the VCC pin voltage > V_{UVLO1}, the recharge function is activated. When VCC pin voltage < V_{CHG1}, VCC recharge function operates to charge the VCC pin with I_{START2} current from the VH pin through the startup circuit. When the VCC pin voltage > V_{CHG2}, the recharge is terminated by switching to I_{START3} current.

The operation is shown in the timing chart.

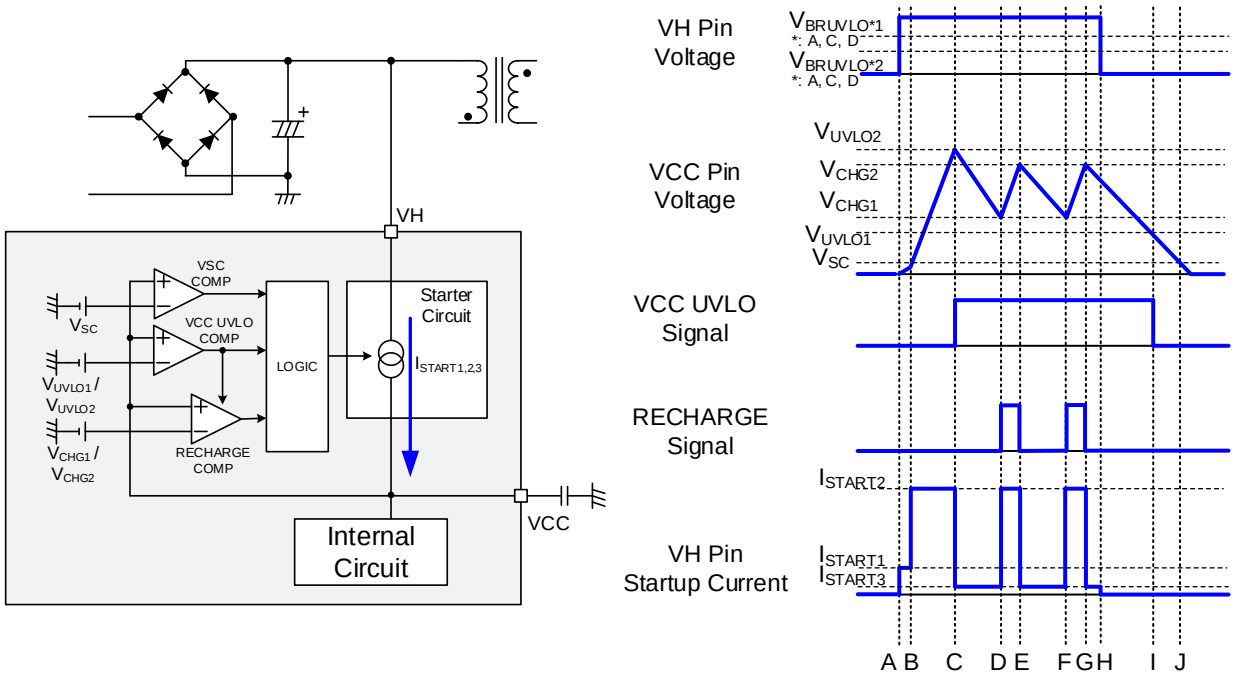


Figure 2. Start Up Block Diagram and Timing Chart

A: AC voltage is applied and the VH pin voltage rises. I_{START1} current is charged to VCC.
B: VCC voltage > V_{SC}, VCC charge current is switched to I_{START2}.
C: VCC voltage > V_{UVLO2}, VCC UVLO releases, and the operation starts.
D: VCC voltage < V_{CHG1}, charging to the VCC pin starts.
E: VCC voltage > V_{CHG2}, charging to the VCC pin stops.
F: VCC voltage < V_{CHG1}, charging to the VCC pin restarts.
G: VCC voltage > V_{CHG2}, charging to the VCC pin stops.
H: Low voltage level at VH pin stops the current from VH.
I: VCC voltage < V_{UVLO1}, VCC UVLO is detected, and IC operation stops, and reset.
J: VCC voltage < V_{SC} and VCC charge current is switched to I_{START1}.
(However, in this case, due to low VH voltage, there is no supply current from VH pin)

The VH startup circuit is a startup-only circuit. If the IC continues to operate using the charge current from VH after startup, the IC will consume power equal to the circuit current x VH voltage and generate heat. In that case, configure the circuit so that power is not always supplied to VCC from the VH startup circuit, such as by using an auxiliary winding to supply power to VCC.
Also, do not connect a pull-down or other load to the VCC pin. The power supply to the IC may be insufficient, causing startup failure.

1.1 Startup Circuit - continued

Soft Start Function

It has a built-in soft start function to prevent FET rush current at startup.
By changing the input voltage V_{SS} of the IC internal ERROR AMP at a slew rate of 0.1 V/ms, startup is completed in approximately 15 ms.

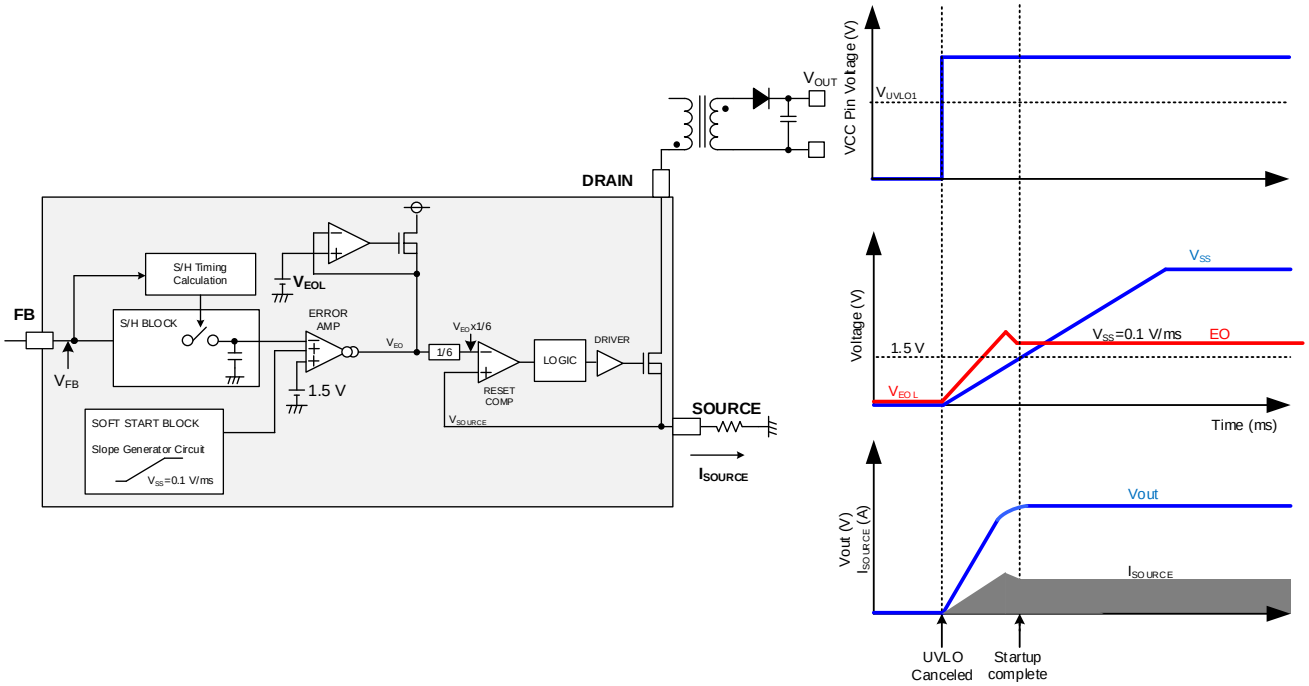


Figure 3. Soft Start Block Diagram and Timing Chart

BR UVLO (A, C, D series)

Since this IC has a built-in high withstand voltage resistor, it can monitor the voltage after diode bridge for voltage reduction protection, BR UVLO, and overvoltage protection, BR OVP.
The VH pin voltage < $V_{BRUVLOx1}$, then, after $t_{BRUVLO1}$ elapses, IC stops operating and resets. In addition, The VH pin voltage > $V_{BRUVLOx2}$ and after $t_{BRUVLO2}$ elapses, it restarts with a soft start.

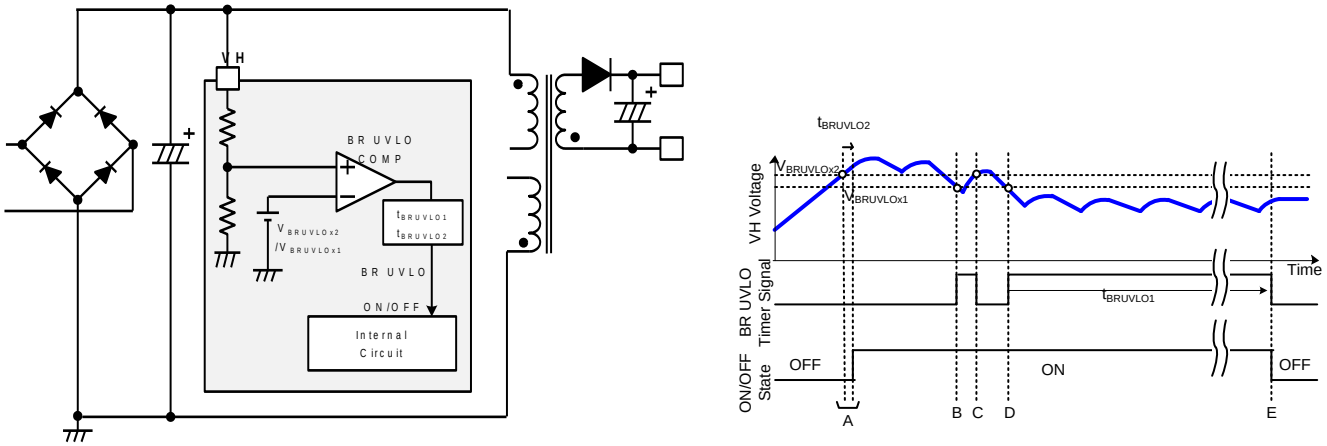


Figure 4. BR UVLO Block Diagram and Timing Chart

A: VH voltage > $V_{BRUVLOx2}$, BR UVLO is canceled. Startup starts after $t_{BRUVLO2}$ elapses.
B: VH voltage < $V_{BRUVLOx1}$, BR UVLO is detected. Timer count starts.
C: VH voltage > $V_{BRUVLOx2}$, BR UVLO is canceled. Timer count resets.
D: VH voltage < $V_{BRUVLOx1}$, BR UVLO is detected. Timer count starts.
E: VH voltage < $V_{BRUVLOx1}$, BR UVLO is detected and stopped after $t_{BRUVLO1}$ has elapsed.

Description of Blocks - continued

2. Feedback Control

This IC adopts a primary side feedback method that monitors the voltage of the auxiliary winding on the primary side and controls the output voltage. By doing so, feedback components such as shunt regulators and photocouplers on the secondary side can be greatly reduced. In addition, a unique monitoring system monitors the auxiliary winding voltage near the end of the secondary DIODE current flow, which minimizes the effects of VF voltage fluctuation of rectifier DIODE and surge voltage. As a result, stable voltage can be supplied.

2.1 Output Voltage Setting

FB Pin

In this IC, the output voltage can be set using a resistor R_{FB} connected between the auxiliary winding and FB pin.

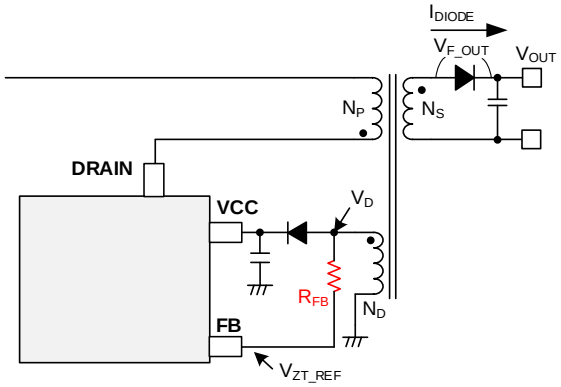


Figure 5. Output Control

The relation between the output voltage setting resistor R_{FB} and the secondary output voltage V_{OUT} is expressed by the following equation.

$$R_{FB} = \left\{ \left(V_{OUT} + V_{F\_OUT} \right) \times \frac{N_D}{N_S} - V_{ZTREF} \right\} \times 0.1 \quad [\text{M}\Omega]$$

The parameters are as follows.

R_{FB}:	The FB pin resistor
V_{OUT}:	Secondary output voltage
V_{F_OUT}:	Secondary DIODE V_F voltage
N_D:	Number of primary auxiliary windings
N_S:	Number of secondary windings
V_{ZTREF}:	FB pin voltage at feed back

Calculation Example

$V_{OUT} = 15[V]$, $V_{F\_OUT} = 0.6[\,V]$, $N_D = 12\ [turn]$, $N_S = 15\ [turn]$, $V_{ZTREF} = 0.48\ [V]$

It becomes

$$R_{FB} = \left\{ (15\ [V] + 0.6\ [V]) \times \frac{12\ [turn]}{15\ [turn]} - 0.48[V] \right\} \times 0.1 = 1.2 \quad [\text{M}\Omega]$$

FB pin is a controlled high impedance line so that 10 µA current flows. Therefore, it is susceptible to noise from DRAIN lines, auxiliary winding lines, etc. Place the setting resistor as close as possible to the FB pin. Consider wiring crosstalk as well.
Also, since the FB pin monitors the sampling timing of the auxiliary winding output, connecting a capacitor will hinder accurate sampling and will cause malfunction. Therefore, do not connect a capacitor to the FB pin.

Description of Blocks - continued

3. Drive Control

3.1 Quasi Resonant Control

This IC contributes to high efficiency and low noise through quasi resonant control. The ON timing is controlled by the bottom voltage of the auxiliary winding during resonance operation. Off timing is controlled by ERROR AMP output VEO and SOURCE pin voltage. A detailed explanation of the control method is given below.

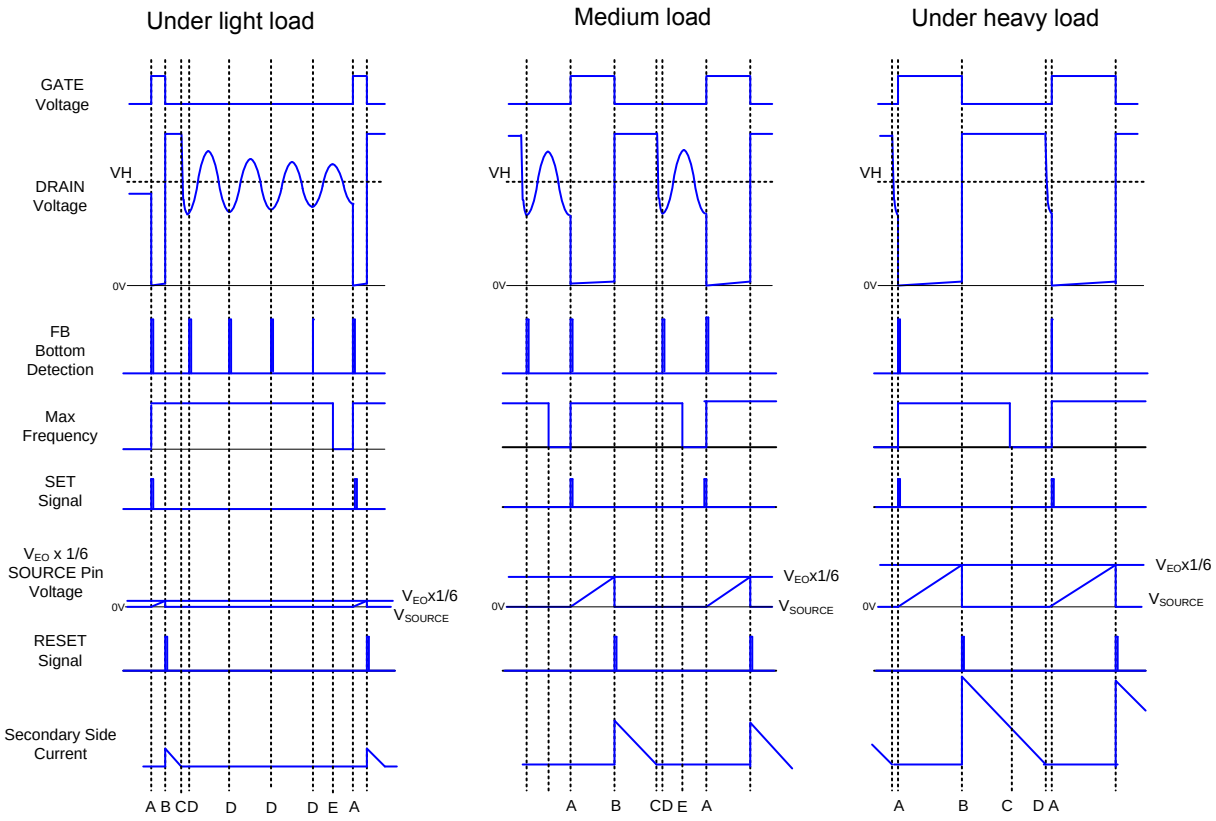


Figure 6. QR Control Timing Chart

Operation under light load and medium load

Maximum frequency limit depends on V_{EO} (frequency reduction function). At light loads, the V_{EO} voltage becomes low, which slows down the maximum frequency limit.

A: The FET is turned ON by detecting the bottom of the DRAIN pin with the FB pin.
Maximum frequency limit count starts.
B: When V_{SOURCE} > V_{EO} x 1/6 occurs, a RESET pulse signal is outputted FET is turned OFF.
Secondary current conduction starts.
C: The secondary side current stops and a resonance signal is generated at the DRAIN pin.
D: The bottom of the DRAIN pin is detected by the FB pin, but it is masked due to frequency limitations.
E: Maximum frequency limit count is complete.
A: The FET is turned ON by detecting the bottom of the DRAIN pin with the FB pin.
Maximum frequency limit count starts.

Operation under heavy load

In heavy load operation, the V_{EO} voltage increases, so the maximum frequency limit becomes faster and turns on at the first bottom. At this time, the maximum ON time of the FET is limited by t_{MAX}.

A: The FET is turned ON by detecting the bottom of the DRAIN pin with the FB pin.
Maximum frequency limit count starts.
B: When V_{SOURCE} > V_{EO} x 1/6 occurs, a RESET pulse signal is outputted, and FET is turned OFF.
Secondary current conduction starts.
C: Maximum frequency limit count is complete.
D: The secondary side current stops and a resonance signal is generated at the DRAIN pin.
A: The FET is turned ON by detecting the bottom of the DRAIN pin with the FB pin.
Maximum frequency limit count starts.

3. Drive Control - continued

3.2 Timeout Feature

In the Quasi Resonant control method, the bottom is detected, and FET is turned ON. However, the bottom may not be detected at the time of startup or during light load operation. Therefore, if the bottom is not detected for a certain period, a timeout function that forcibly turns ON FET is required.

OFF Timeout Function

When the output voltage is low, such as when starting up or when the output voltage is shorted, the voltage generated in the auxiliary winding becomes small, and if the bottom voltage cannot be detected, the FET is forcibly turned ON.

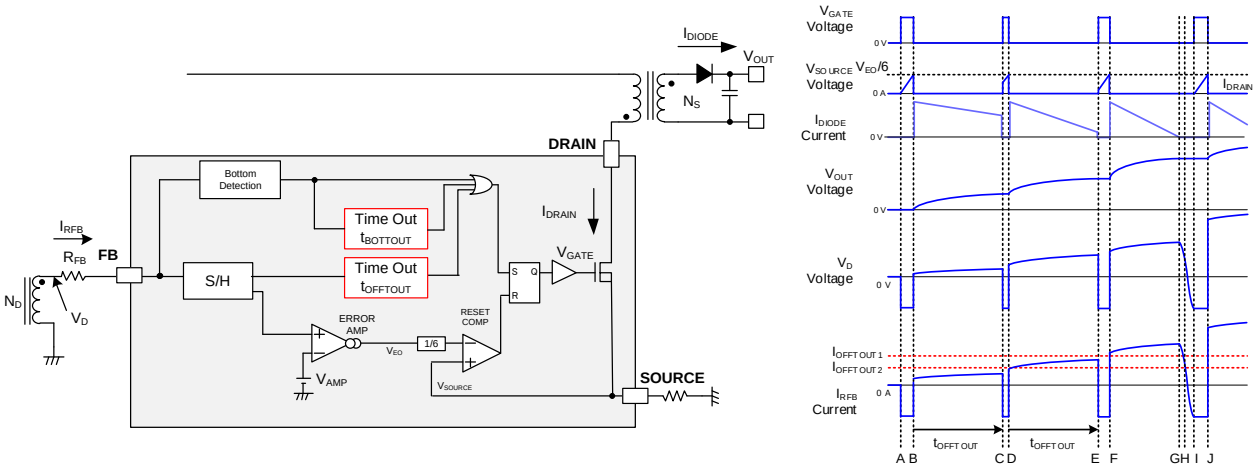


Figure 7. Time Out Block Diagram and Timing Chart

A: Switching starts.
B: SOURCE pin voltage V_{SOURCE} reaches $V_{EO}/6$, and FET is OFF.
Timeout starts due to $I_{RFB} < I_{OFFTOUT1}$ at this point of time.
C: $t_{OFFTOUT}$ has elapsed and forcibly FET is ON.
D: SOURCE pin voltage V_{SOURCE} reaches $V_{EO}/6$, and FET is OFF.
Timeout starts due to $I_{RFB} < I_{OFFTOUT1}$ at this point of time.
E: $t_{OFFTOUT}$ has elapsed and forcibly FET is ON.
F: SOURCE pin voltage V_{SOURCE} reaches $V_{EO}/6$, and FET is OFF.
The timeout is stopped due to $I_{RFB} > I_{OFFTOUT1}$ at this point of time.
G: Secondary transformer current discharge complete.
H: $I_{RFB} < I_{OFFTOUT2}$ condition occurs.
I: FET is turned ON by bottom detection.
J: SOURCE pin voltage V_{SOURCE} reaches $V_{EO}/6$, and FET turns OFF.

Bottom Timeout Function

When the resonant signal is attenuated and the bottom signal cannot be detected, such as when the load is light, FET is forcibly turned ON.

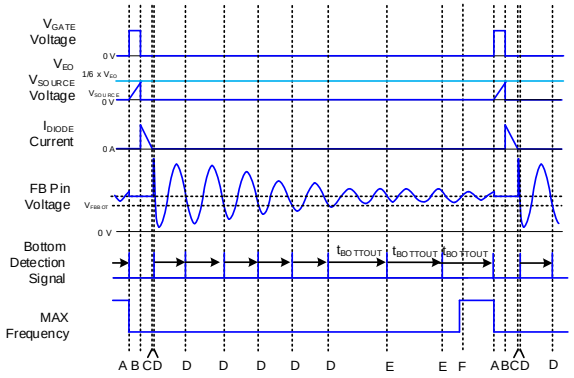


Figure 8. Bottom Time Out Timing Chart

Condition: Assume a condition where one cycle is long at light load.
A: Bottom timeout $t_{BOTTOUT}$ has elapsed. FET is ON.
B: $V_{SOURCE} > V_{EO}$ x 1/6 occurs, and FET is OFF.
C: Secondary current conduction ends, and the FB pin voltage resonance starts.
D: When FB pin voltage < V_{FBBOT}, bottom is detected, and bottom timeout is re-counted.
E: When FB pin voltage > V_{FBBOT}, bottom timeout $t_{BOTTOUT}$ has elapsed.
However, the set signal is masked by MAX Frequency.
F: MAX Frequency is demasked.
A: Bottom timeout $t_{BOTTOUT}$ has elapsed and FET is turned ON.

3. Drive Control - continued

3.3 Leading Edge Blanking (LEB) Function

When the built-in FET is ON, surge voltage may be generated at the SOURCE pin and the pin may turn OFF. Therefore, masking SOURCE voltage during t_{LEB} prevents immediate OFF operation due to surging.

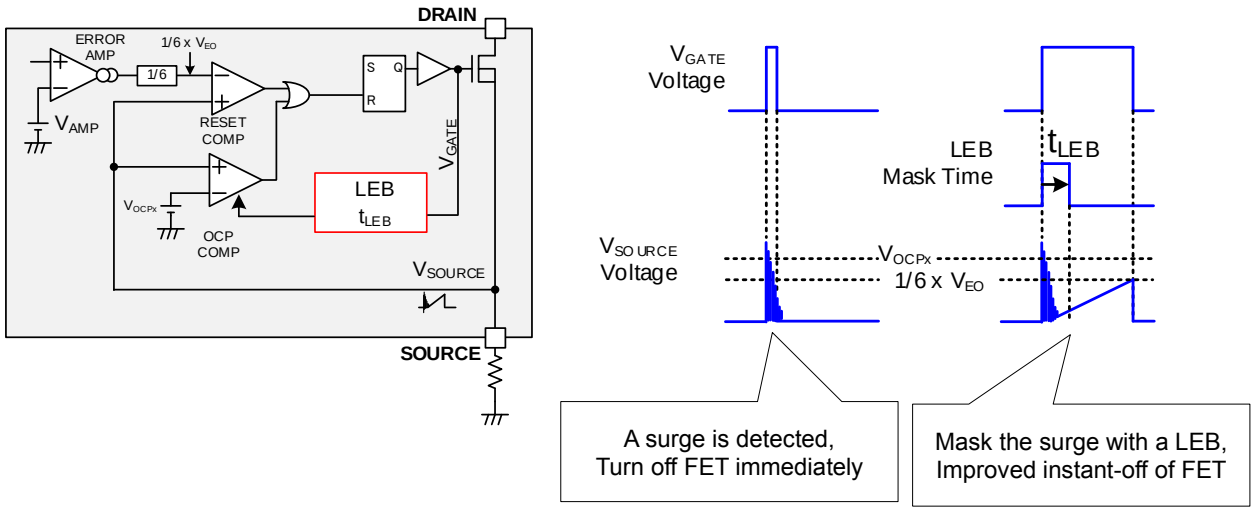


Figure 9. LEB Block Diagram and Timing Chart

3.4 EMI Reduction Function

This IC has a built-in function to reduce radiation noise.

3.5 Frequency Reduction Function

This IC has a built-in frequency reduction function. The maximum frequency limit varies from fsw2 to fsw1 depending on output power.

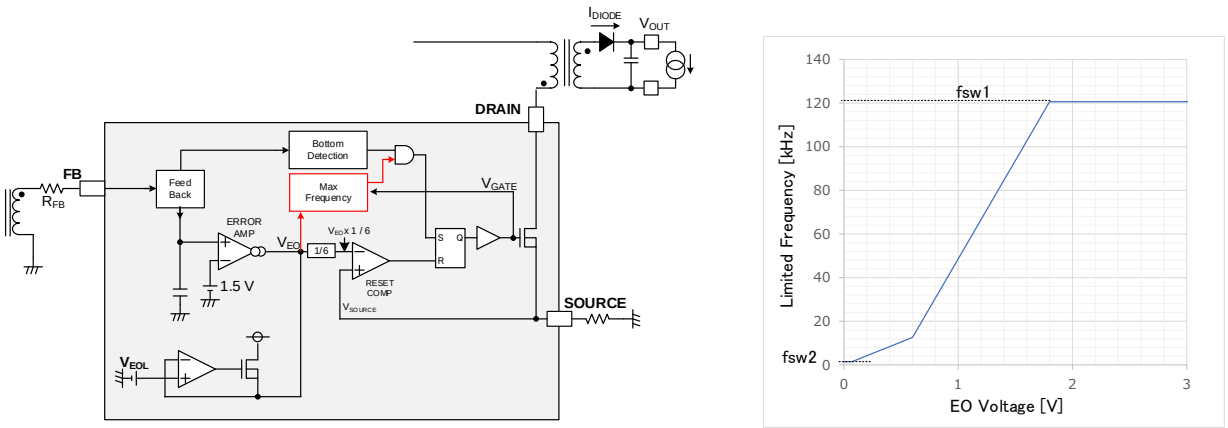


Figure 10. QR Frequency and Burst Control

Description of Blocks – continued

4. Protection Function

This IC detects various abnormal conditions and provides safe protection.

Table 1. Protect Function List (numerical value is entered as Typ)

Power Protection Temperature Protection

Function	VCC Under Voltage Lock Out (VCC UVLO)	BR Under Voltage Lock Out (BR UVLO)	VCC Over Voltage Protection (VCC OVP)	BR Over Voltage Protection (BR OVP)	Thermal Shutdown (TSD)
Detection condition	VCC < 7.5 V	VH < 84.6 V (A, D series) VH < 98.7 V (C series)	VCC > 33.0 V	VH > 705 V (C, D series)	175 °C
Cancel Conditions	VCC > 9.5 V	VH > 98.7 V (A, D series) VH > 112.8 V (C series)	VCC < 30.0 V	VH < 634.5 V (C, D series)	100 °C
Detection timer	-	128 ms	120 µs	120 µs	120 µs
Release timer	-	120 µs	-	-	-
Mode	Automatic reset	Automatic reset	Automatic reset	Automatic reset	Automatic reset
Operation at detection	Stop driving	Stop driving	Stop driving	Stop driving	Stop driving

SOURCE pin protective

Function	Over Current Protection (OCP)	Overload Protection (OLP)	Dynamic Over Current Protection (DOCP)	SOURCE Short Protection (SSP)
Detection condition	V_{SOURCE} > 0.325 V at V_H = 140 V V_{SOURCE} > 0.240 V at V_H = 400 V	SOURCE pin output setting power or more	V_{SOURCE} > 0.375 V at V_H = 140 V V_{SOURCE} > 0.290 V at V_H = 400 V	V_{SOURCE} < 50 mV
Cancel Conditions	V_{SOURCE} < 0.325 V at V_H = 140 V V_{SOURCE} < 0.240 V at V_H = 400 V	SOURCE pin output setting power or less	V_{SOURCE} < 0.375 V at V_H = 140 V V_{SOURCE} < 0.290 V at V_H = 400 V	V_{SOURCE} > 50 mV
Detection timer	-	28 ms	2 Pulse continuity	4.0 µs at V_H = 140 V 1.6 µs at V_H = 400 V
Release timer	-	200 ms	120 µs	-
Mode	Pulse by pulse	Automatic reset	Automatic reset	Pulse by pulse
Operation at detection	FET forced OFF	Stop driving	FET forced OFF	FET forced OFF

4. Protection Function - continued

4.1 VCC OVP (VCC Over Voltage Protection)

IC operation stops when VCC OVP has detected for t_{OVP}, when VCC pin voltage > V_{OVP1}. If VCC pin voltage < V_{OVP2}, operation restarts.

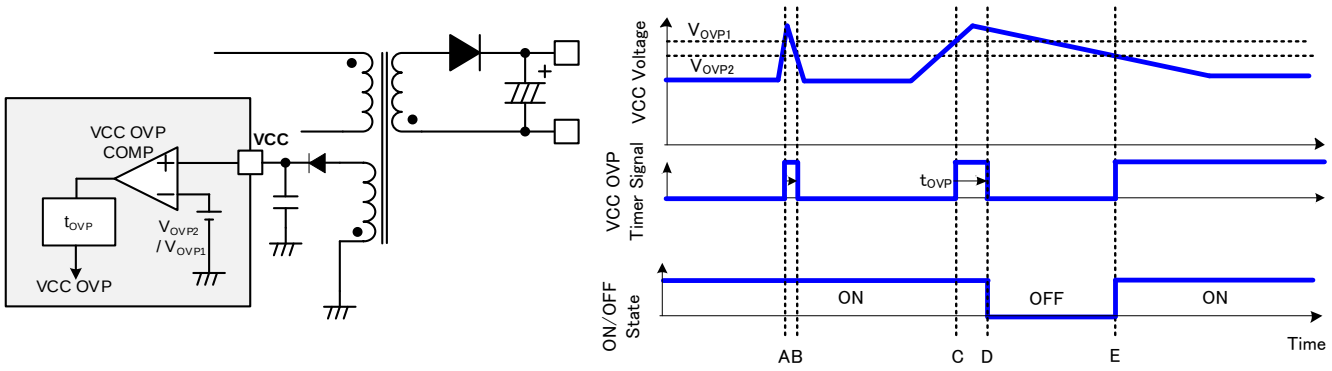


Figure 11. VCC OVP Block Diagram and Timing Chart

A: VCC voltage > V_{OVP1} and VCC OVP timer count starts.
B: VCC voltage < V_{OVP2} and VCC OVP timer count resets.
C: VCC voltage > V_{OVP1} and VCC OVP timer count starts.
D: VCC voltage > V_{OVP1}, t_{OVP} has elapsed and VCC OVP is detected. IC shutdowns.
E: VCC voltage < V_{OVP2} and VCC OVP is released. Operation starts.

4.2 BR OVP (BR Over Voltage Protection)

IC operation stops when BR OVP has detected for t_{BROVP} when VH pin voltage > V_{BROVP1}. If the VH pin voltage < V_{BROVP2}, operation restarts.

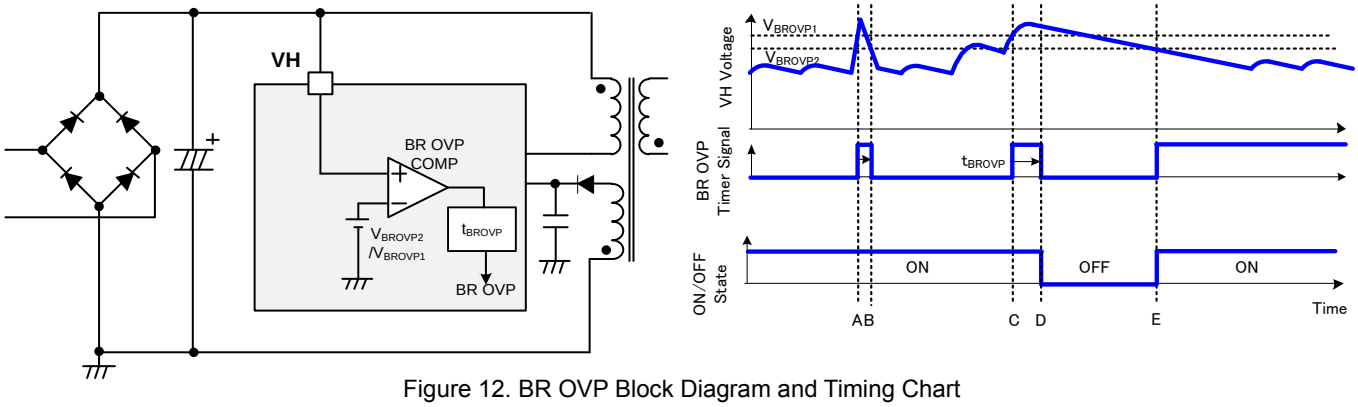


Figure 12. BR OVP Block Diagram and Timing Chart

A: VH voltage > V_{BROVP1} and BR OVP timer count starts.
B: VH voltage < V_{BROVP2} and BR OVP timer count resets.
C: VH voltage > V_{BROVP1} and BR OVP timer count starts.
D: VH voltage > V_{BROVP1}, t_{BROVP} has elapsed and BR OVP is detected. IC shutdowns.
E: VH voltage < V_{BROVP2} and BR OVP is released. Restart from slow start state

4.3 TSD (Thermal Shutdown)

This IC has a built-in overheat protective function. When the junction temperature becomes T_{TSD1} and t_{TSD} elapses, it is detected, and the driver stops. IC restarts from the slow start state when it is less than T_{TSD2}.

4. Protection Function - continued

4.4 OCP (Over Current Protection)

OCP will deactivate FET when the SOURCE pin voltage > V_{OCPx}.
Corrects OCP detect voltage according to the input AC voltage to improve the power supply voltage dependency.

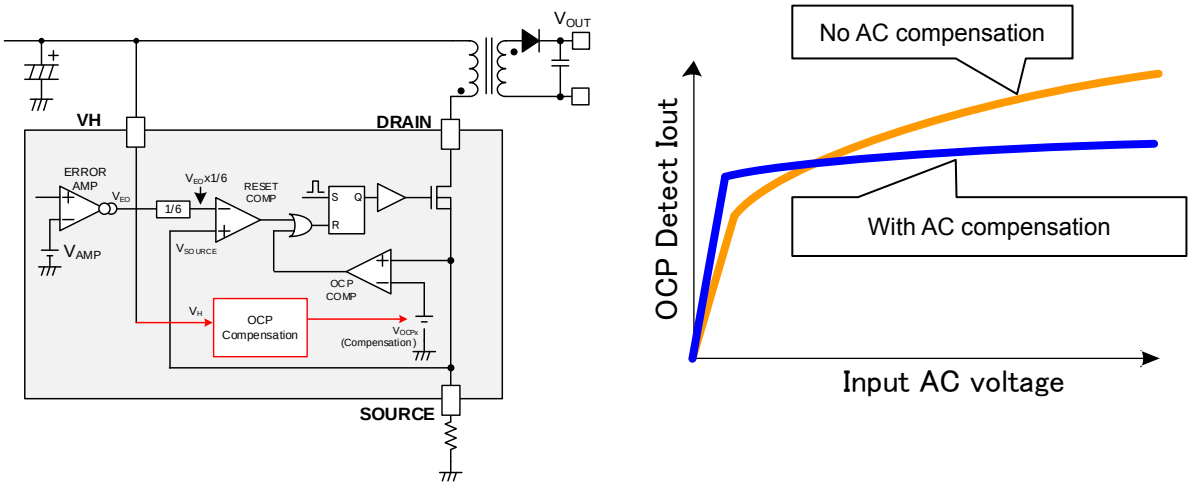


Figure 13. OCP Block Diagram and Timing Chart

The OCP detection voltage can be calculated using the approximate formula below.
However, the compensation value is for V_{OCP1} (VH = 140 V) and V_{OCP2} (VH = 400 V).

$$V_{OCPx} = -0.075 \times ln(VH) + 0.689 \quad [V]$$

Each parameter is as follows.

V_{OCPx} : OCP Detection Voltage
VH: DC Voltage after Diode Bridge

Calculation Example

The OCP detection voltage value V_{OCP} at $VH = 310\ [V]$ is below.

$$V_{OCPx} = -0.075 \times ln(310\ V) + 0.689 = 0.259 \quad [V]$$

4. Protection Function – continued

4.5 OLP (Overload Protection)

OLP will stop driving when t_{OLP1} has elapsed with the power set at the SOURCE pin or higher. Then, after t_{OLP2} has passed, it will automatically return and restart with a slow start.

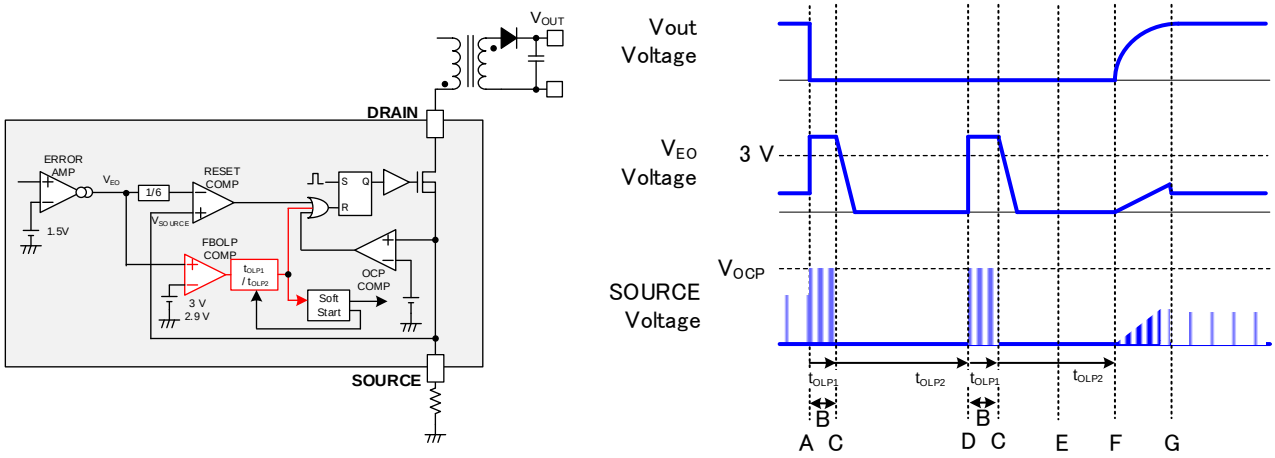


Figure 14. OLP Block Diagram and Timing Chart

A: Output voltage V_{OUT} is shorted to GND, becomes overload protection state, and timer count starts.
B: Drive with timeout operation because V_{OUT} voltage is GND.
C: t_{OLP1} elapsed and operation stopped.
D: Restart after t_{OLP2}. The timer count starts because the output voltage V_{OUT} continues to be shorted to GND.
B: Drive with timeout operation because V_{OUT} voltage is GND.
C: t_{OLP1} elapsed and operation stopped.
E: Release V_{OUT} GND short.
F: Restart with soft start.
G: Reboot completed.

4. Protection Function - continued

4.6 DOCP (Dynamic Over Current Protection)

This IC has a built-in DOCP function. When SOURCE pin voltage exceeds V_{DOCPx} twice consecutively, the pulse operation between t_{DOCP} is stopped. DOCP detection voltage depends on VH pin voltage.

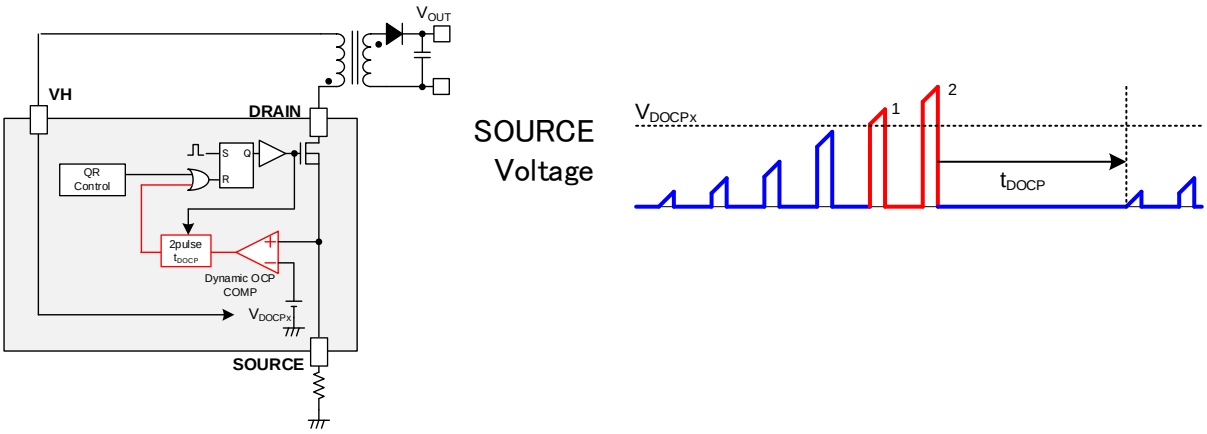


Figure 15. DOCP Block Diagram and Timing Chart

4.7 SSP (SOURCE Short Protection)

After the FET is turned ON, if the SOURCE voltage does not reach the V_{SSHORT} voltage when the timer time t_{LIM_SOSx} has elapsed, the FET will be forced OFF. Detection is performed by pulse by pulse.

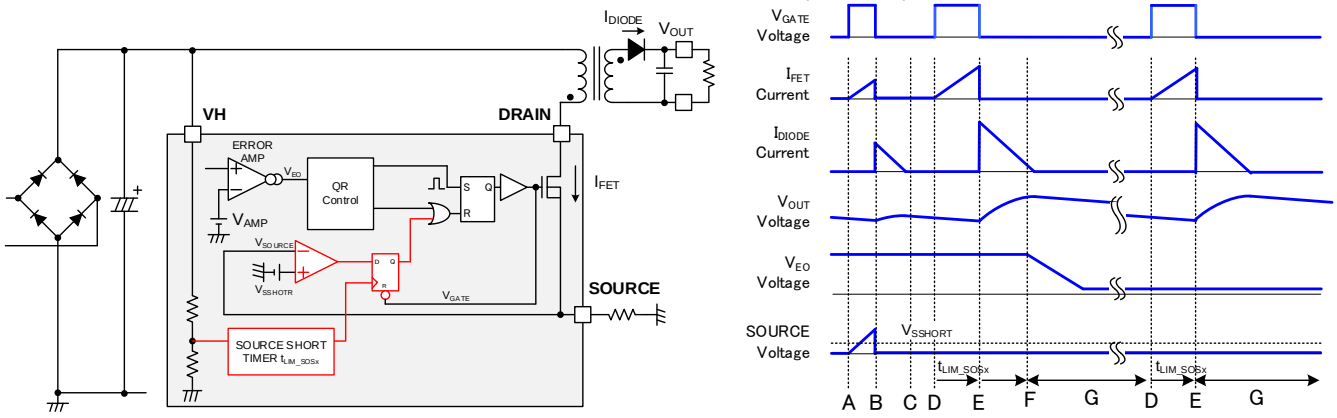


Figure 16. SOURCE Short Protection Block Diagram and Timing Chart

A: FET is turn ON by Quasi Resonant control.
B: FET is turn OFF by Quasi Resonant control.
C: SOURCE pin GND shorted.
D: FET is turn ON by Quasi Resonant control.
E: Because SOURCE pin GND is shorted, FET is turn OFF after the maximum ON time, t_{LIM_SOSx}, elapses.
F: Excessive power is supplied between D and E, causing the output to rise and the V_{EO} voltage to drop at the sampling timing.
G: Control with frequency reduced due to V_{EO} voltage drop.

During this protection operation, the ON time is determined by t_{LIM_SOSx}, and the output voltage is controlled by varying the frequency. Therefore, the output voltage may be over-boosted at light load. In this case.
Reduce the bleeder resistance.
Connect a Zener diode to the output.
Measures can be taken, for example.

However, Note that depending on the transformer specifications, the coil may become saturated at the maximum ON-time t_{LIM_SOSx}.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Condition
Maximum Applied Voltage 1	V_{MAX1}	-0.3 to +900	V	DRAIN, VH
Maximum Applied Voltage 2	V_{MAX2}	-0.3 to +6.5	V	SOURCE, FB
Maximum Applied Voltage 3	V_{MAX3}	-0.3 to +40.0	V	VCC
DRAIN Current (1 Pulse)	I_{DP}	1.0	A	P_w = 10 µs, Duty cycle = 10 % Drain Voltage < 600 Vdc
Maximum Junction Temperature	Tjmax	150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Recommended External Component Condition (Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
VCC Pin Capacitor	C_{VCC}	4.7	10	-	µF	

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSOP-A20_16A				
Junction to Ambient	θ_{JA}	123.1	65.7	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	8	5	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
VCC Pin Power Supply Voltage Range	V_{CC}	8.6 *(Note 1)*	-	30.0	V
VH Pin Power Supply Voltage Range	V_H	-	-	900	V
Operating Temperature	Topr	-40	-	+125	°C

(Note 1) VCC pin voltage is less than 9.0 V, VCC Recharge function operates. (Refer to P-5 VCC Recharge function.)

Electrical Characteristics MOSFET (Unless otherwise specified Tj = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
DRAIN Voltage	V_{DS}	900	-	-	V	I_D = 1 mA, V_{GS} = 0 V
DRAIN Leakage Current	I_{DSS}	-	-	100	μA	V_{DS} = 900 V, V_{GS} = 0 V
ON Resistance	R_{ON}	-	12.9	16.2	Ω	I_D = 0.1 A, V_{GS} = 10 V

Electrical Characteristics Starting VH (Unless otherwise specified Tj = -40 to +125 °C, V_{CC} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Starting Current 1 *(Note 3)*	I_{START1}	0.15	0.30	0.50	mA	V_H = 100 V, V_{CC} = 0 V
Starting Current 2 *(Note 3)*	I_{START2}	2.5	4.7	8.0	mA	V_H = 100 V, V_{CC} = 5 V
VH Pin OFF Current *(Note 3)*	I_{START3}	10	22	50	μA	V_H = 100 V, V_{CC} = 12 V
Starting Current Switching VH Voltage *(Note 3)*	V_{SC}	0.5	1.1	2.5	V	VCC rising
BR UVLO Detection Voltage A *(Note 2) (Note 3)*	$V_{BRUVLOA1}$	76.1	84.6	93.1	V	VH Voltage falling (A, D Series)
BR UVLO Release Voltage A *(Note 2) (Note 3)*	$V_{BRUVLOA2}$	88.8	98.7	108.6	V	VH Voltage Rising (A, D Series)
BR UVLO Detection Voltage C *(Note 2) (Note 3)*	$V_{BRUVLOC1}$	88.8	98.7	108.6	V	VH Voltage falling (C Series)
BR UVLO Release Voltage C *(Note 2) (Note 3)*	$V_{BRUVLOC2}$	101.5	112.8	124.1	V	VH Voltage Rising (C Series)
BR UVLO Detection Timer	$t_{BRUVLO1}$	94	128	173	ms	(A, C, D Series)
BR UVLO Release Timer	$t_{BRUVLO2}$	80	120	180	μs	(A, C, D Series)
BR OVP Detection Voltage *(Note 2) (Note 3)*	V_{BROVP1}	634.5	705.0	775.5	V	VH Voltage Rising (C, D Series)
BR OVP Release Voltage *(Note 2) (Note 3)*	V_{BROVP2}	571.1	634.5	698.0	V	VH Voltage falling (C, D Series)
BR OVP Detection Timer	t_{BROVP}	80	120	180	μs	(C, D Series)

(Note 2) This is a linkage item.
(Note 3) Tj = 25 °C warranty

Electrical Characteristics control IC (Unless otherwise specified Tj = -40 °C to +125 °C, V_{CC} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VCC Block						
Circuit Current at Drive Stop	I_{CC}	0.5	0.8	1.1	mA	Driving Is Stopped
Circuit Current at Operation *(Note 1)*	I_{CC13}	0.6	0.9	1.2	mA	
VCC UVLO Detection Voltage *(Note 2)*	V_{UVLO1}	6.5	7.5	8.5	V	VCC Falling
VCC UVLO Release Voltage *(Note 2)*	V_{UVLO2}	8.5	9.5	10.5	V	VCC Rising
VCC UVLO Hysteresis *(Note 2)*	V_{UVLO3}	-	2	-	V	$V_{UVLO3} = V_{UVLO2} – V_{UVLO1}$
VCC Recharge Initiation Voltage *(Note 2)*	V_{CHG1}	7	8	9	V	
VCC Recharge Shutdown Voltage *(Note 2)*	V_{CHG2}	8	9	10	V	
VCC OVP Detection Voltage *(Note 2)*	V_{OVP1}	31	33	35	V	VCC Rising
VCC OVP Release Voltage *(Note 2)*	V_{OVP2}	28	30	33	V	VCC Falling
VCC OVP Detect Times	t_{OVP}	80	120	180	µs	
Driver Block						
Maximum Switching Frequency *(Note 1)*	f_{SW1}	100	120	132	kHz	
Minimum Switching Frequency *(Note 1)*	f_{SW2}	0.8	1.2	2.0	kHz	
Leading Edge Blanking Time *(Note 4)*	t_{LEB}	-	0.3	-	µs	
FET Minimum ON Time *(Note 4)*	t_{MIN}	-	0.35	-	µs	
FET Maximum ON Time	t_{MAX}	29	40	54	µs	
Feedback Block						
Feedback Voltage at 12 V Output Setting *(Note 1) (Note 3)*	V_{FB1}	12.191	12.440	12.689	V	R_{FB} = 1.2 MΩ
Output Voltage Temperature Compensation *(Note 3) (Note 4)*	V_{FB2}	-	-2.5	-	mV/°C	R_{FB} = 1.2 MΩ, Ta = 25 °C to 125 °C
FB Pin Voltage *(Note 3)*	V_{ZTREF}	-	0.48	-	V	At Sampling Timing
Bottom Detection Voltage	V_{FBBOT}	0.20	0.38	0.55	V	
OLP Detect Times *(Note 1) (Note 2)*	t_{OLP1}	20	28	40	ms	
OLP Release Times *(Note 1) (Note 2)*	t_{OLP2}	140	200	280	ms	
Timeout Detected Current *(Note 1) (Note 2)*	$I_{OFFTOUT1}$	3.0	4.5	6.5	µA	FB Pin Current
Timeout Release Current *(Note 1) (Note 2)*	$I_{OFFTOUT2}$	3.5	5.0	7.0	µA	FB Pin Current
Timeout at FET OFF	$t_{OFFTOUT}$	50	70	90	µs	
Bottom Timeout Time	$t_{BOTTOUT}$	3.0	5.5	8.0	µs	Count From Final Bottom
Maximum Output Current of FB Pin at FET ON *(Note 1)*	I_{FB_MAX}	-1700	-900	-550	µA	FB = -0.2 V
Forced ON Timer	t_{FORCE}	80	120	180	µs	

(Note 1) Tj = 25 °C warranty
(Note 2) This is a linkage item.
(Note 3) Refer to the Measuring Circuit Diagram Figure 17.
(Note 4) Measurements are not made.

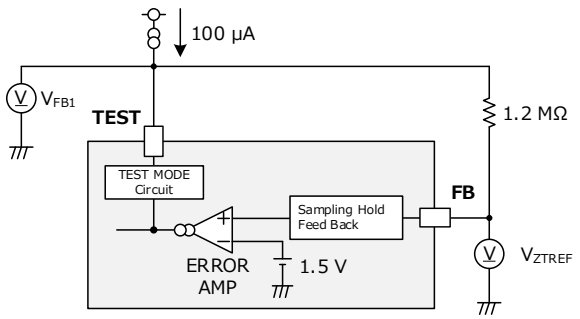


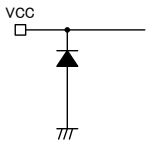
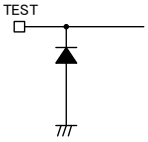
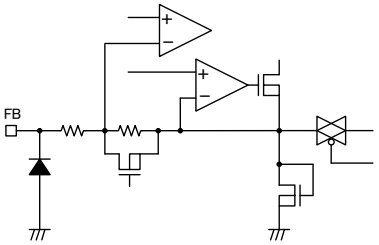
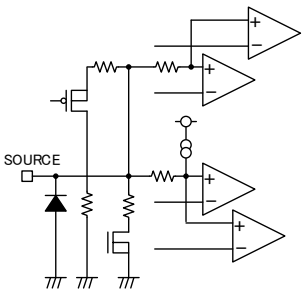
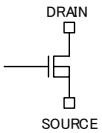
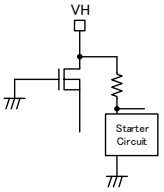
Figure 17. Feedback Voltage Measurement Circuit at Switching Stop Condition.

Electrical Characteristic - continued (Unless otherwise specified Tj = -40 °C to +125 °C, V_{CC} = 12 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Current Sense Block						
SOURCE Pin Over Current Protection Detection Voltage 1 *(Note 1)*	V_{OCP1}	300	325	350	mV	V_H = 140 V
SOURCE Pin Over Current Protection Detection Voltage 2 *(Note 1)*	V_{OCP2}	225	250	275	mV	V_H = 400 V
Dynamic Over Current Protection Detection Voltage 1 *(Note 1)*	V_{DOCP1}	340	375	410	mV	V_H = 140 V
Dynamic Over Current Protection Detection Voltage 2 *(Note 1)*	V_{DOCP2}	275	300	325	mV	V_H = 400 V
Dynamic Overcurrent Protection Stop Time	t_{DOCP}	80	120	180	µs	
SOURCE Pin Short Detection Voltage	V_{SSHORT}	0.03	0.05	0.08	V	
Timeout at SOURCE Pin Short 1	t_{LIM_SOS1}	2.5	4.0	6.5	µs	V_H = 140 V
Timeout at SOURCE Pin Short 2	t_{LIM_SOS2}	1.0	1.6	2.3	µs	V_H = 400 V
Temperature Protection						
Thermal Shutdown Temperature 1	T_{TSD1}	150	175	-	°C	At Temperature Rises
Thermal Shutdown Temperature 2	T_{TSD2}	-	100	-	°C	At Temperature Falling
Thermal Shutdown Time	t_{TSD}	80	120	180	µs	

(Note 2) This is a linkage item.

I/O Equivalence Circuits

1 VCC	2 TEST	3 FB	4 N.C.
			—
5, 6 SOURCE	**7, 8, 9, 10 GND**	**11, 12,13 DRAIN**	**14, 15, 16 VH**
			

Application Examples

Examples of flyback circuits and buck converter circuits are shown below.
The resistor connected to the FB pin is high impedance, so be sure to place it close to the FB pin and keep the wiring as short as possible. Also, since the FB pin is a feedback pin, do not connect a capacitor to it. This may cause malfunction.
Also, connect a bleeder resistor, Zener diode, or both to the output to reduce voltage rise during light loads.
A buck converter requires a peak hold circuit at the VH pin.

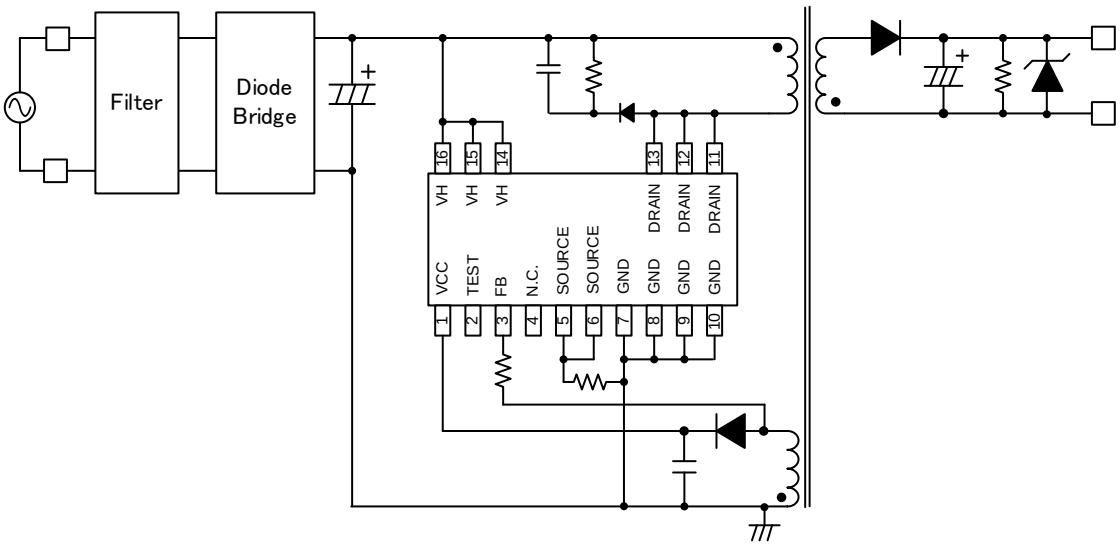


Figure 18. Flyback Convertor Application Diagram

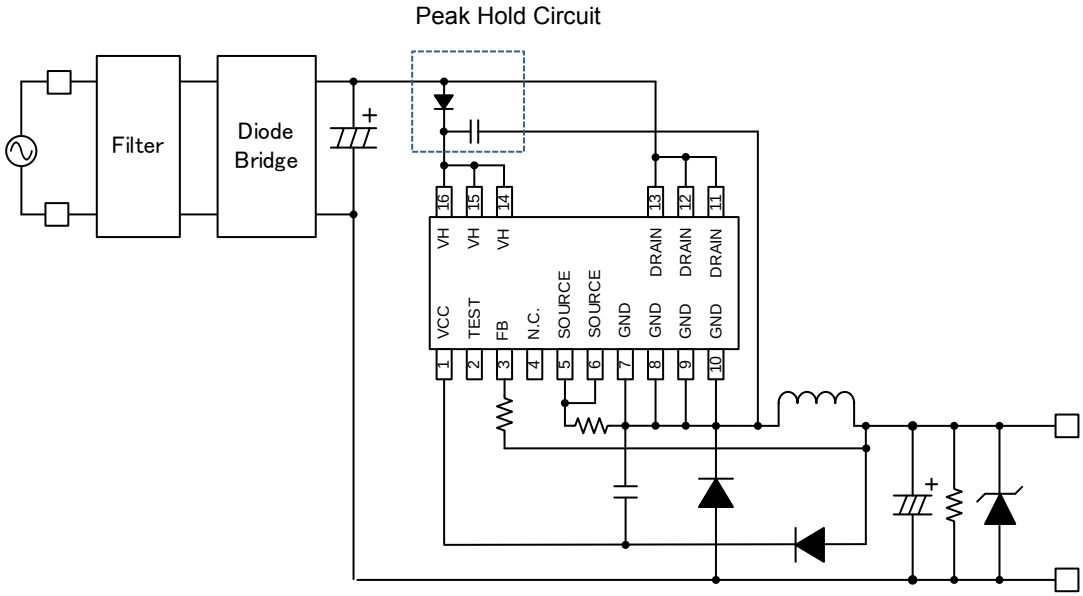


Figure 19. Buck Convertor Application Diagram

Typical Performance Curves
(Reference Data)

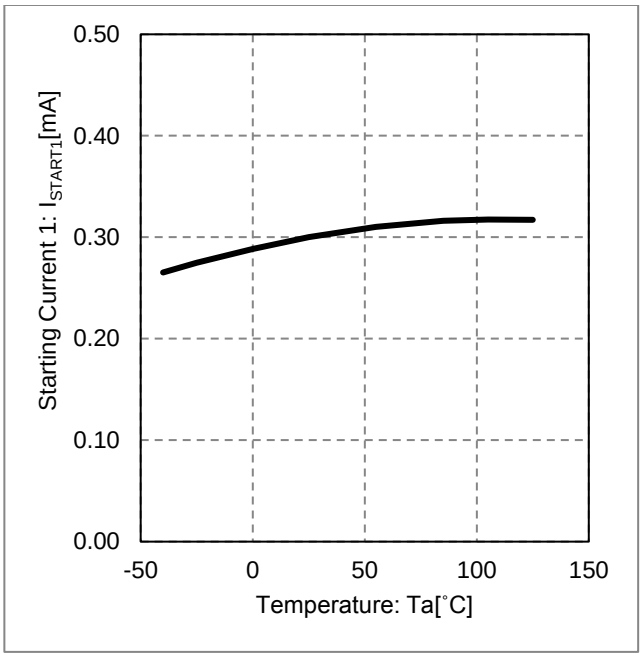


Figure 20. Starting Current 1 vs Temperature

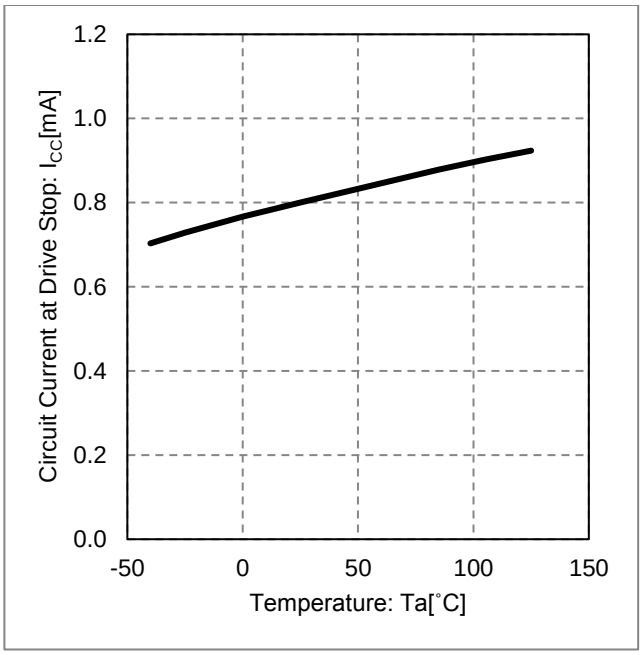


Figure 21. Circuit Current at Drive Stop vs Temperature

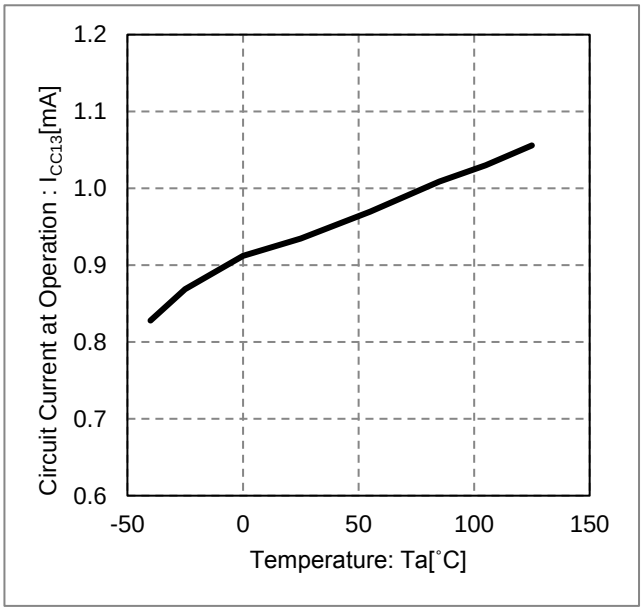


Figure 22. Circuit Current at Operation vs Temperature

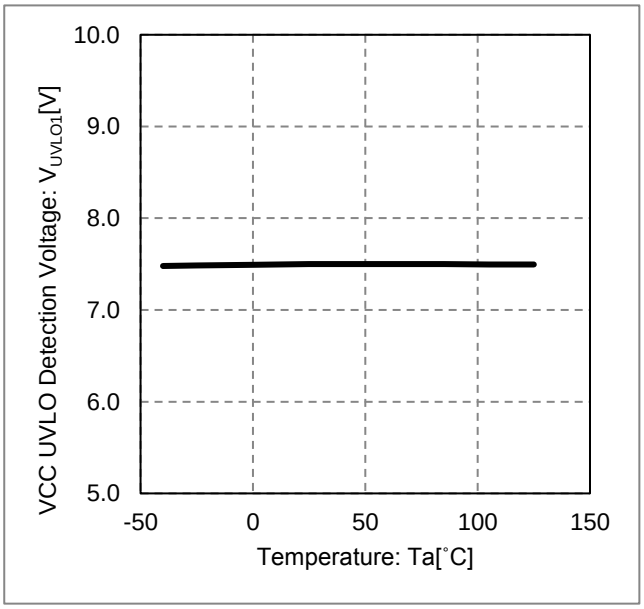


Figure 23. VCC UVLO Detection Voltage vs Temperature

Typical Performance Curves - continued
(Reference Data)

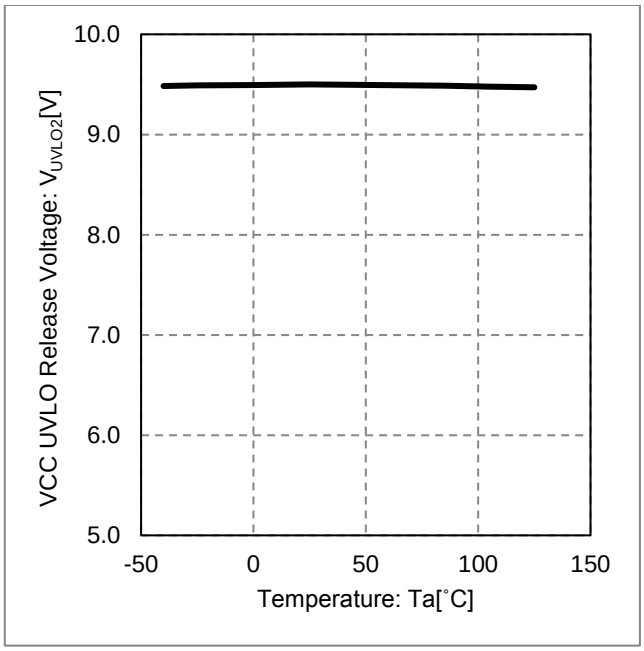


Figure 24. VCC UVLO Release Voltage vs Temperature

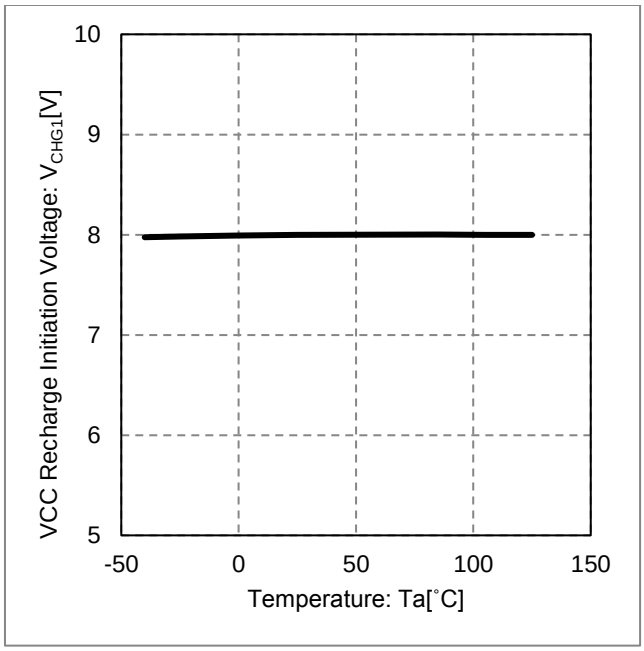


Figure 25. VCC Recharge Initiation Voltage vs Temperature

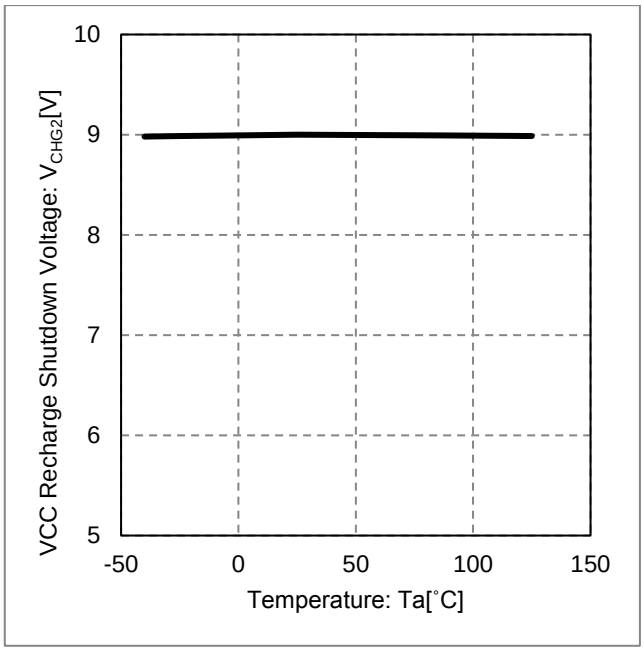


Figure 26. VCC Recharge Shutdown Voltage vs Temperature

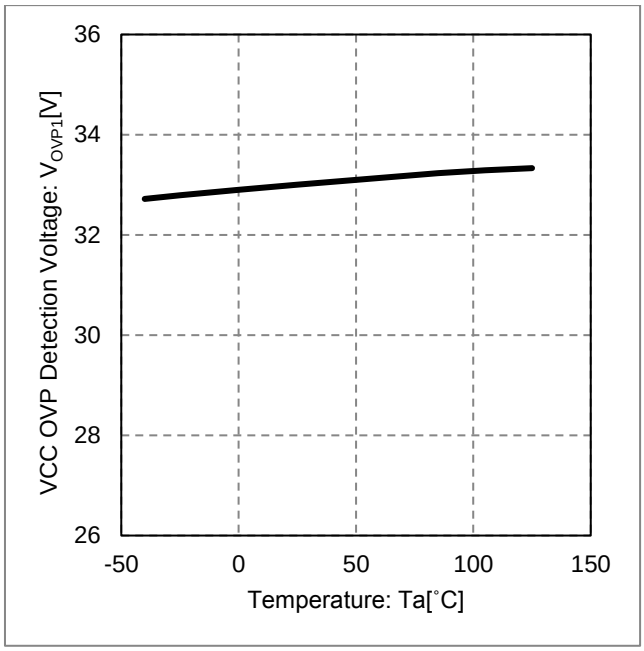


Figure 27. VCC OVP Detection Voltage vs Temperature

Typical Performance Curves - continued
(Reference Data)

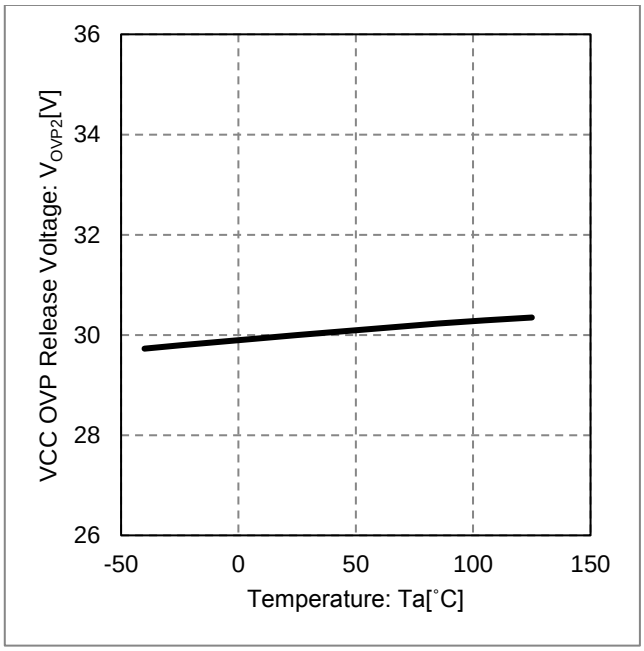


Figure 28. VCC OVP Release Voltage vs Temperature

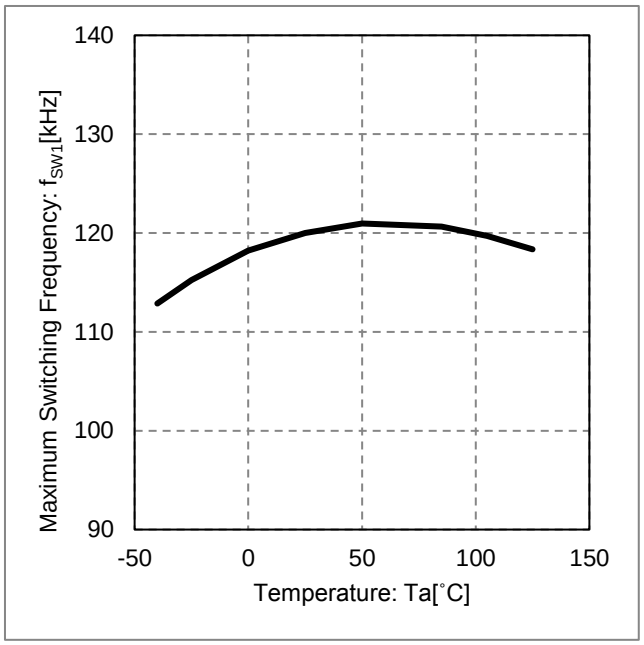


Figure 29. Maximum Switching Frequency vs Temperature

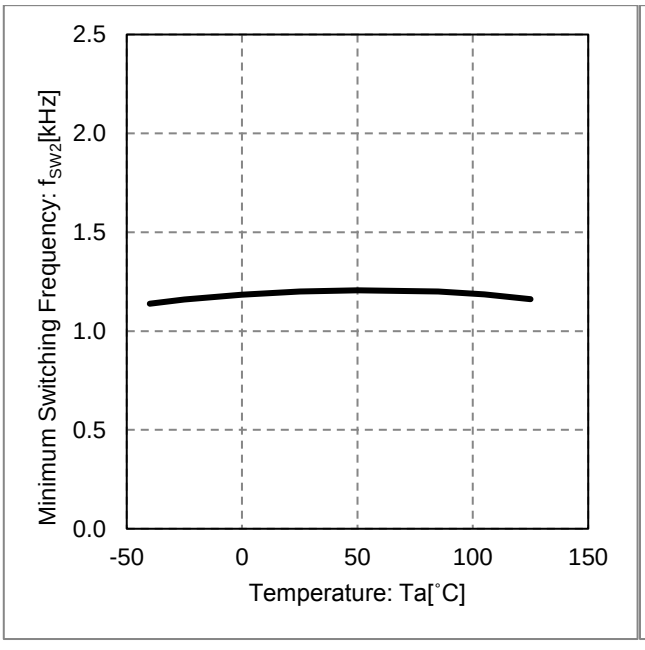


Figure 30. Minimum Switching Frequency vs Temperature

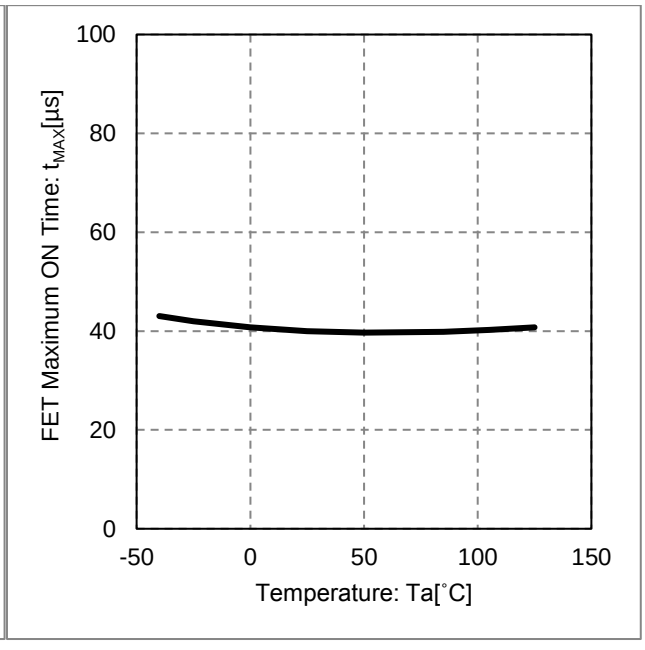


Figure 31. FET Maximum ON Time vs Temperature

Typical Performance Curves - continued
(Reference Data)

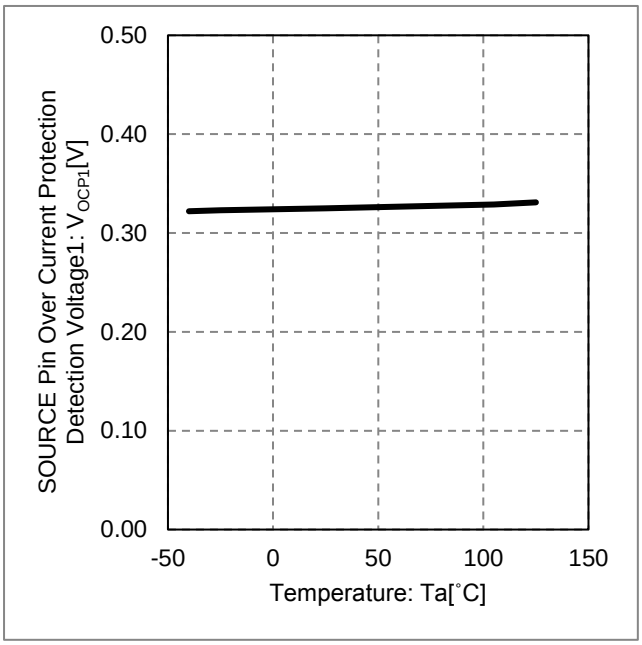


Figure 32. SOURCE Pin Over Current Protection Detection Voltage 1 vs Temperature

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turn off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

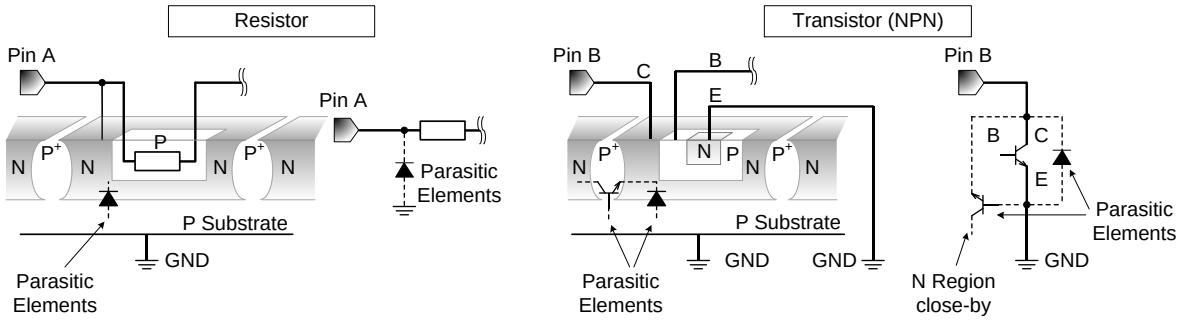


Figure 33. Example of IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B M 2 Q H 0 x 1 3 F S - ZE2

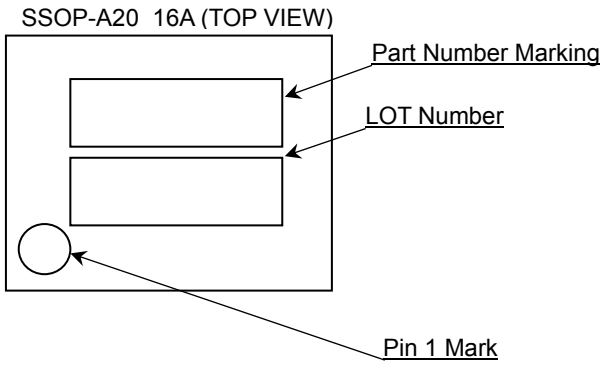
BR Protection Series A to D Refer below table	MOSFET Ron 12.9 Ω	Package SSOP-A20_16A	Packaging and forming specification Z: Outsourced package E2: Embossed tape and reel

Lineup

Part Number Marking	MOSFET Ron	BR UVLO (Typ)	BR OVP (Typ)	Package	Orderable Part Number
BM2QH0A13	12.9 Ω	84.6 V	-	SSOP-A20_16A	BM2QH0A13FS-ZE2
BM2QH0B13	12.9 Ω	-	-		BM2QH0B13FS-ZE2
BM2QH0C13	12.9 Ω	98.7 V	705 V		BM2QH0C13FS-ZE2
BM2QH0D13	12.9 Ω	84.6 V	705 V		BM2QH0D13FS-ZE2

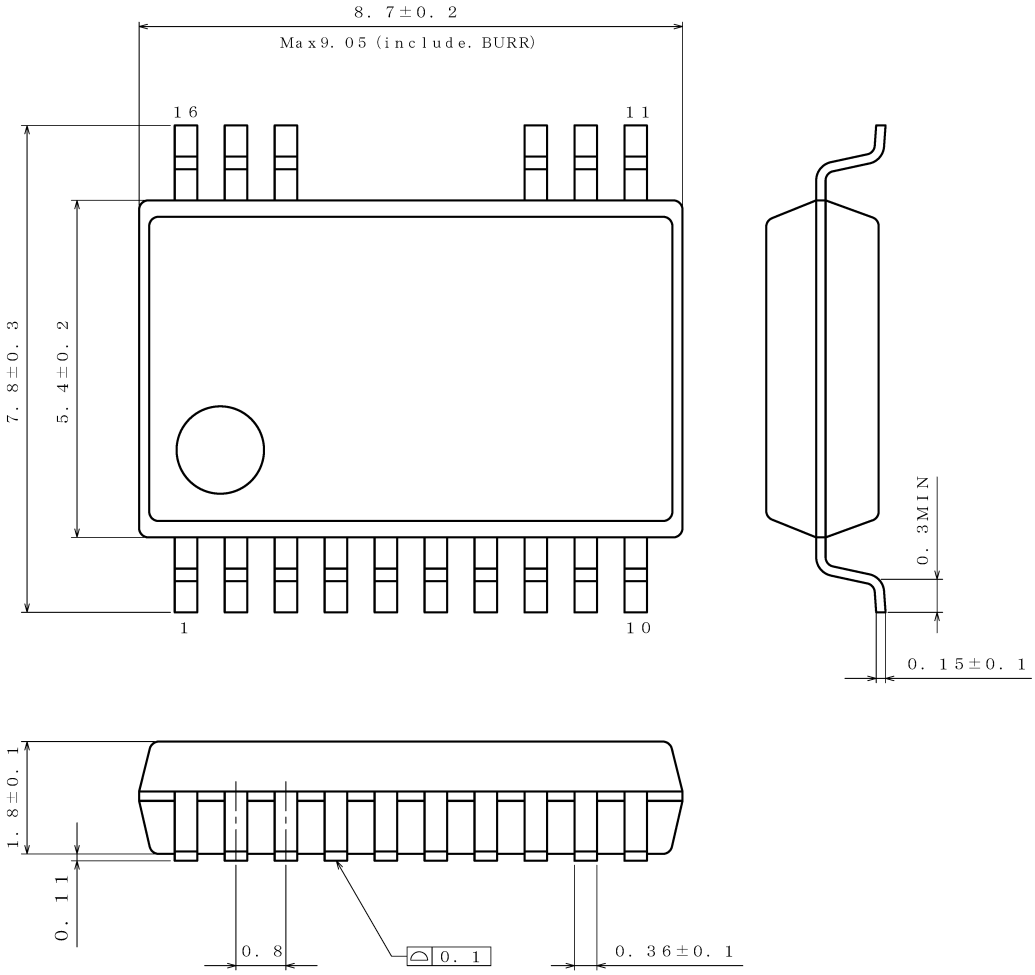
B, D series are under development

Marking Diagram



Physical Dimension and Packing Information

Package Name	SSOP-A20_16A

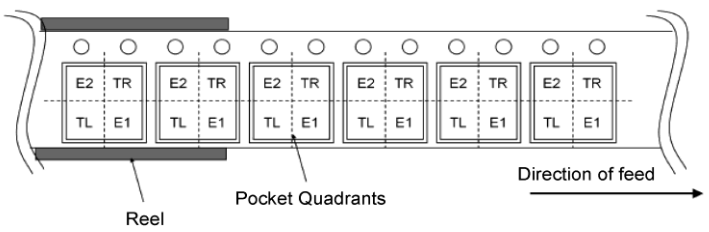


(UNIT:mm)

PKG:SSOP-A20_16A
Drawing No. EX001-0135

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
19.Jun.2024	001	New Release

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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