

# Automotive Intelligent Power Device Single Channel 40 mΩ High Side Switch

## BV1HB040EFJ-C

### General Description

The BV1HB040EFJ-C single channel 40 mΩ Intelligent High Side Power Device integrates an Overcurrent load protection, a dual Temperature Shutdown mechanism which limits the internal thermal transients and reduces the mechanical stress of the IC, and a smart Active-Clamp circuit to dissipate the magnetic energy while switching off inductive loads and to protect internal circuits from overvoltage surges. Embedded Current Sense and Diagnostic features provide real time load current information and open or short circuit feedback in both on and off state. A 3 V and 5 V CMOS compatible input pin offers direct microcontroller connection without special interfaces or level shifters. These in conjunction with a wide input voltage range make the High Side IPD a high-performance component suitable for 12 V battery connected automotive applications.

### Key Specifications

■ Supply Nominal Voltage Range:	6 V to 28 V
■ Low Operating Voltage (cranking):	4 V (Max)
■ Overvoltage Protection:	41 V (Min)
■ ON Resistance:	40 mΩ (Typ)
■ Overcurrent Limit:	30 A (Typ)
■ Sleep Current:	0.5 μA (Max)
■ Operating Current:	3 mA (Typ)
■ Junction Temperature Range (Tj):	-40 °C to +150 °C

### Package

HTSOP-J8

W (Typ) x D (Typ) x H (Max)  
4.9 mm x 6.0 mm x 1.0 mm

### Features

- AEC-Q100 Qualified<sup>(Note 1)</sup>
- Short Circuit Load Protection
- Overcurrent Limitation
- Active Clamp and Overvoltage Protection
- Dual Temperature Shutdown
- Undervoltage Lock Out
- Integrated Current SENSE Circuit
- Loss of Ground Protection
- Open Load and Short to Battery Diagnostics

(Note 1) Grade 1

### Applications

- Driver for Resistive, Inductive and Capacitive Loads
- MOSFET, Relay and Fuse Replacement
- Intelligent Power Device for 12 V Automotive Applications

- Thermally Enhanced Thin Small-Outline 8 pin package with 1.27 mm Pin Pitch
- Exposed Pad for improved thermal performance



### Typical Application Circuit

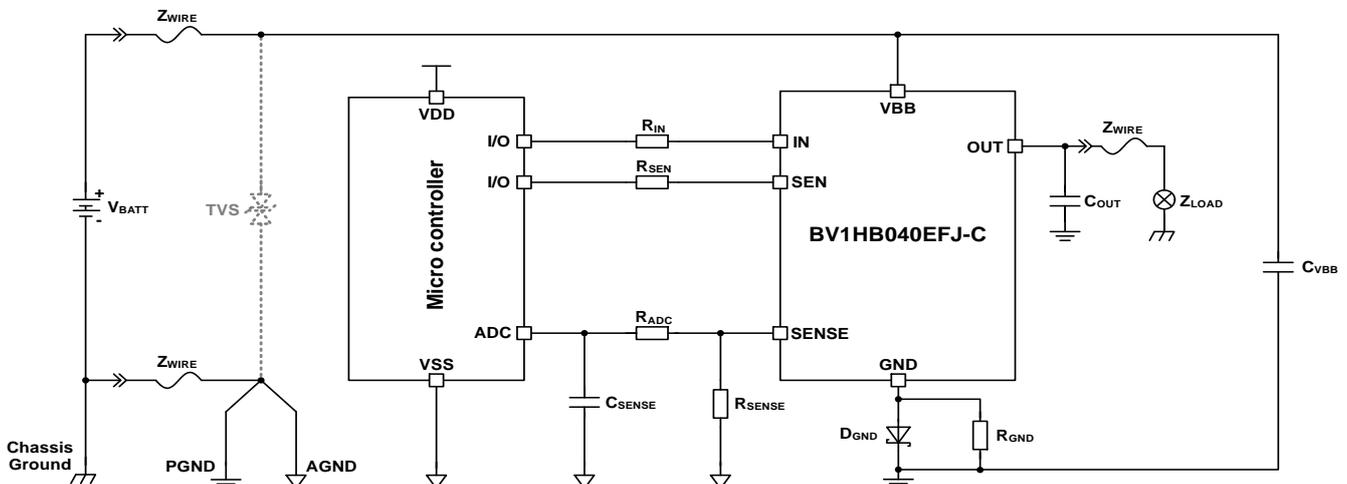


Figure 1. Typical Application Diagram

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

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Pin Configuration

HTSOP-J8  
(Top View)

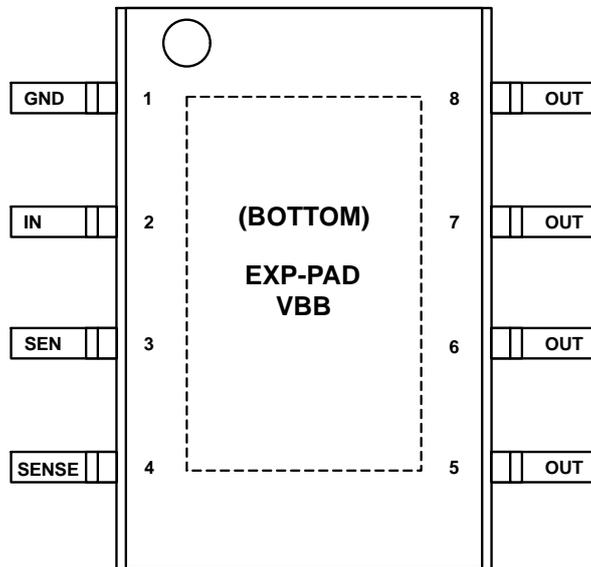


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	GND	Device Ground pin
2	IN	Input Pin. Turns on the Switch. Active "High"
3	SEN	Current Sense and diagnostic enable. Active "High"
4	SENSE	Current Sense analog output pin
5 to 8	OUT	High Side Switch Power Output <sup>(Note 1)</sup>
EXP-PAD	VBB	Exposed-Pad. Power Supply Voltage Line Input

*(Note 1)* Output pins are internally shorted. Please connect the respective pins together on the PCB such as the metal traces can withstand the desired maximum current.

Definitions

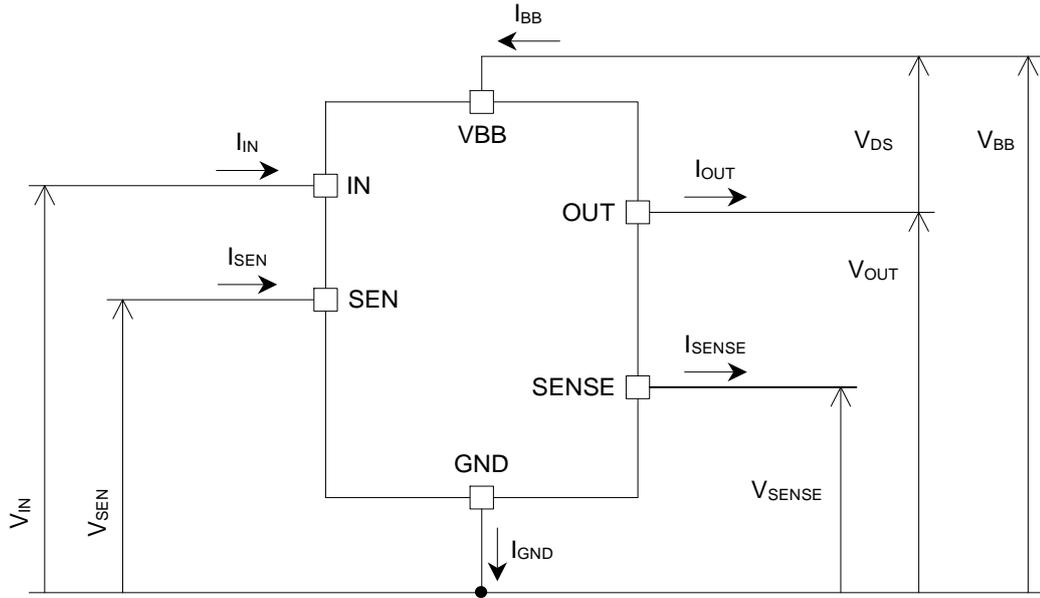


Figure 3. Voltage and Current Definitions

## Absolute Maximum Ratings

Parameters	Symbol	Ratings	Unit	Conditions
[Power Supply / GND pin]				
DC Supply Voltage	$V_{BB}$	-0.3 to +36	V	
Supply Voltage at load dump	$V_{BB\_LD}$	40	V	ISO16750-2, $R_i = 2 \Omega$
Supply Voltage (Output to GND short) (Note 4)	$V_{BB\_SC}$	-0.3 to +24	V	AEC-Q100-012
Supply Voltage (When battery is connected in reverse direction)	$V_{BB\_REV}$	-16	V	less than 2 minutes, $T_j = 25^\circ\text{C}$ , $R_L > 4 \Omega$ , $D_{GND}$ , $R_{GND}$ connected
GND Pin Current	$I_{GND}$	-50 to +30	mA	less than 2 minutes, $T_j = 25^\circ\text{C}$ , $D_{GND}$ , $R_{GND}$ connected
[Input Pin]				
Input Voltage	$V_{IN}$ , $V_{SEN}$	-0.3 to +7	V	
Input Current	$I_{IN}$ , $I_{SEN}$	-2 to +2	mA	
Input Current (When battery is connected in reverse direction)	$I_{IN\_REV}$ , $I_{SEN\_REV}$	-5	mA	less than 2 minutes, $T_j = 25^\circ\text{C}$ , $R_{IN}$ , $R_{SEN} \geq 4.7 \text{ k}\Omega$
[SENSE pin]				
SENSE Voltage	$V_{SENSE\_ON}$	-0.3 to internal limitation (Note 1)	V	$V_{SEN} = \text{"high"}$
	$V_{SENSE\_OFF}$	-0.3 to +7	V	$V_{IN} = V_{SEN} = \text{"low"}$
SENSE Current	$I_{SENSE}$	-20 to internal limitation (Note 1)	mA	$R_{SENSE} = 1 \text{ k}\Omega$
[OUT pin]				
Power Supply to Output Voltage	$V_{DS}$	-0.3 to internal limitation (Note 2)	V	
Maximum Output Current	$I_{OUT}$	internal limitation (Note 3)	A	Maximum $V_{BB} = 28 \text{ V}$
Single Pulse Energy Rating (Note 4)	$E_{AS\_25^\circ\text{C}}$	130	mJ	$T_j = 25^\circ\text{C}$ , $V_{BB} = 14 \text{ V}$ , $I_{OUT(START)} = 2 \text{ A}$
	$E_{AS\_150^\circ\text{C}}$	45	mJ	$T_j = 150^\circ\text{C}$ , $V_{BB} = 14 \text{ V}$ , $I_{OUT(START)} = 2 \text{ A}$
[Temperature]				
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ\text{C}$	
Junction Temperature Range	$T_j$	-40 to +150	$^\circ\text{C}$	
Maximum Junction Temperature	$T_{jmax}$	150	$^\circ\text{C}$	
[ESD] (Note 5)				
Electrostatic-Discharge Capability Human Body Model - HBM	VBB, OUT pins	$\pm 4$	KV	
	IN, SEN, SENSE pins	$\pm 2$	KV	
Electrostatic-Discharge Capability Charged Device Model - CDM	All pins	$\pm 750$	V	

(Note 1) Internal limitation by SENSE voltage clamp and current-limitation protection. Please see the "Electrical Characteristics" section for more details.

(Note 2) Internal limitation by output active-clamp overvoltage protection. Please see the "Electrical Characteristics" section for more details.

(Note 3) Internal limitation by output overcurrent protection. Please see the "Electrical Characteristics" section for more details.

(Note 4) Specified by design and/or statistical analysis of correlated parameters tested in production.

(Note 5) Measured as per EIA/JEDEC and AEC-Q100 Standard. HBM-Measured as per JESD22-A114D and AEC-Q100-002.

CDM-Measured as per JESD22-C101C and AEC-Q100-011.

**Caution 1:** Exposure to the absolute maximum ratings may cause permanent damage to the IC, may affect the device reliability and lifetime. Therefore, operation at or above the absolute maximum ratings is not recommended. The above-described values represent stress ratings and functional operation is not implied. In addition, no destructive conditions such as short or open can be assumed.

**Caution 2:** If the IC is used in a manner that exceeds the maximum junction temperature the original characteristics of the IC will be degraded. If the junction temperature exceeds the maximum specified temperature, increase the board size, increase the area of copper foil for heat dissipation, or use a heat sink. Consider reducing the thermal resistance so that the maximum junction temperature is not exceeded.

**Caution 3:** When an inductive load is turned off, the  $V_{OUT}$  voltage drops below ground level. An integrated active-clamp (overvoltage) protection limits the maximum  $V_{DS}$  across the power transistor and the inductive energy is dissipated internally. The energy can be calculated using the following simplified equation:

**Absolute Maximum Ratings – continued**

$$E_L = V_{DSCLP} \times \left[ \frac{V_{BB} - V_{DSCLP}}{R_L} \times \ln \left( 1 - \frac{R_L \times I_{OUT(START)}}{V_{BB} - V_{DSCLP}} \right) + I_{OUT(START)} \right] \times \frac{L}{R_L}$$

Where:

$L$  is the inductance value of the inductive load.

$R_L$  is the resistance value of the load.

$V_{BB}$  is the supply voltage.

$V_{DSCLP}$  is the clamping voltage.

$I_{OUT(START)}$  is the current flowing through the inductive load at the instance the inductive load is turned off.

In simplified form, if  $R_L$  is neglected.

$$E_L = \frac{1}{2} \times L \times I_{OUT(START)}^2 \times \left( 1 - \frac{V_{BB}}{V_{BB} - V_{DSCLP}} \right)$$

**Caution 4:** The maximum  $E_L$  energy the device can dissipate for a given  $I_{OUT(START)}$  is limited by the maximum thermal transient the power transistor can handle, hence the maximum inductance  $L$  must be selected with respect to the maximum given  $I_{OUT(START)}$ .

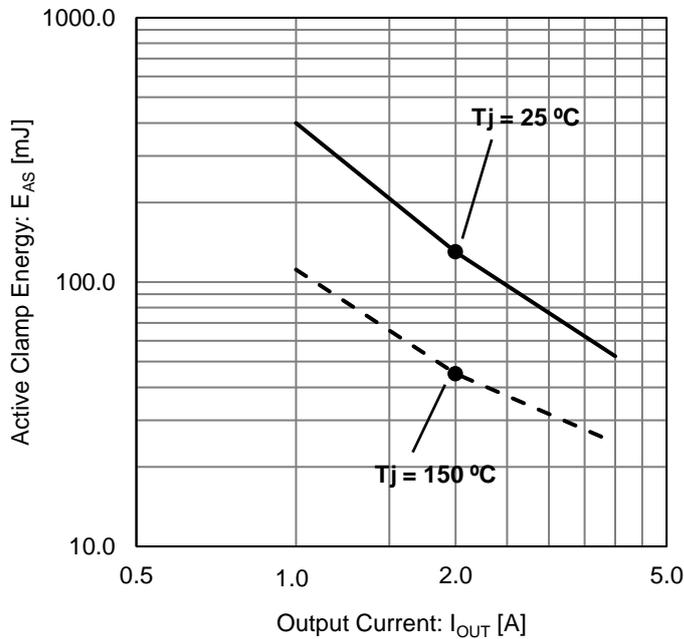


Figure 4. Active Clamp Energy vs Output Current

**Recommended Operating Conditions**

Parameters	Symbol	MIN	TYP	MAX	Unit
Supply Nominal Voltage Range <i>(Note 1)</i>	$V_{BB}$	6	14	28	V
Input Voltage	$V_{IN}, V_{SEN}$	0	-	5.5	V
Operating Junction Temperature	$T_j$	-40	+25	+150	$^\circ\text{C}$
Input Frequency	$f_{IN}$	-	-	1	kHz

*(Note 1)* An extended supply operating voltage range from 4.0 V up to 28 V is possible after start-up; protections are operational. The device is functional up to 36 V and protections are active, however parameter deviations are possible. Please refer to the "Electrical Characteristics" section and the "Features Description" section.

Thermal Resistance (Note 1)

Parameters	Symbol	TYP	Unit	Conditions	
HTSOP-J8					
Thermal Resistance between junction and ambient temperature	$\theta_{JA}$	132.3	°C/W	1s	(Note 2)
		40.7	°C/W	2s	(Note 3)
		29.0	°C/W	2s2p	(Note 4)
Thermal characterization parameter between junction and top center of the outside surface of the component package	$\Psi_{JT}$	12.6	°C/W	1s	(Note 2)
		6.1	°C/W	2s	(Note 3)
		4.8	°C/W	2s2p	(Note 4)

(Note 1) Based on JESD51-2A(Still-Air). Specified by design.

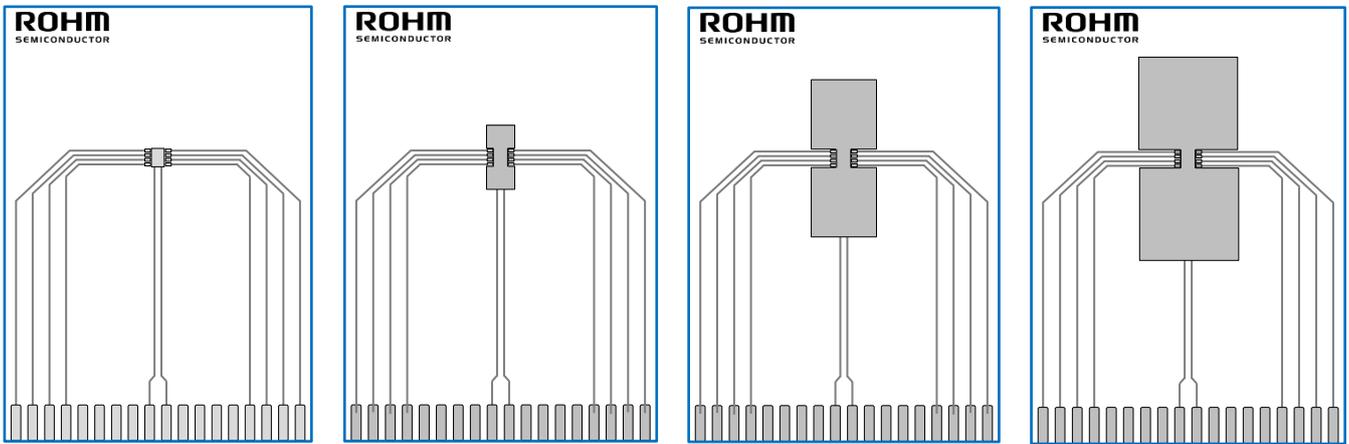
(Note 2) Using a PCB board based on JESD51-3.

(Note 3) Using a PCB board based on JESD51-5.

(Note 4) Using a PCB board based on JESD51-5, 7.

**Caution:** The values presented here were measured/simulated under a specific set of conditions and should be regarded only as a guideline on how to estimate the thermal behavior of the application and should not be used as design parameters. A careful evaluation of the actual application values should be done to confirm the estimated results

■ PCB Layout 1 Layer (1s)



Footprint

100 mm<sup>2</sup>

600 mm<sup>2</sup>

1200 mm<sup>2</sup>

Figure 5. PCB Layout 1 Layer (1s)

Dimension	Value
Board Finish Thickness	1.57 mm
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness	0.070 mm (Cu: 2 oz)
Copper Foil Area	Footprint / 100 mm <sup>2</sup> / 600 mm <sup>2</sup> / 1200 mm <sup>2</sup>

Thermal Resistance – continued

■ PCB Layout 2 Layers (2s)

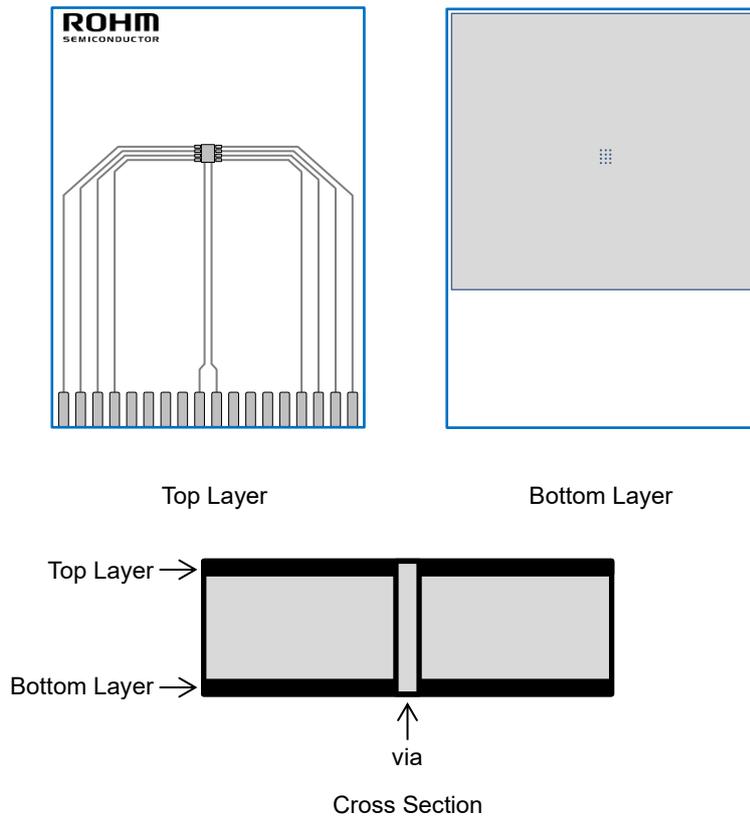


Figure 6. PCB Layout 2 Layers (2s)

Dimension	Value
Board Finish Thickness	1.60 mm
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top / Bottom Layers)	0.070 mm (Cu: 1 oz + plating)
Thermal Vias Separation / Diameter	1.2 mm / 0.3 mm

Thermal Resistance – continued

■ PCB Layout 4 Layers (2s2p)

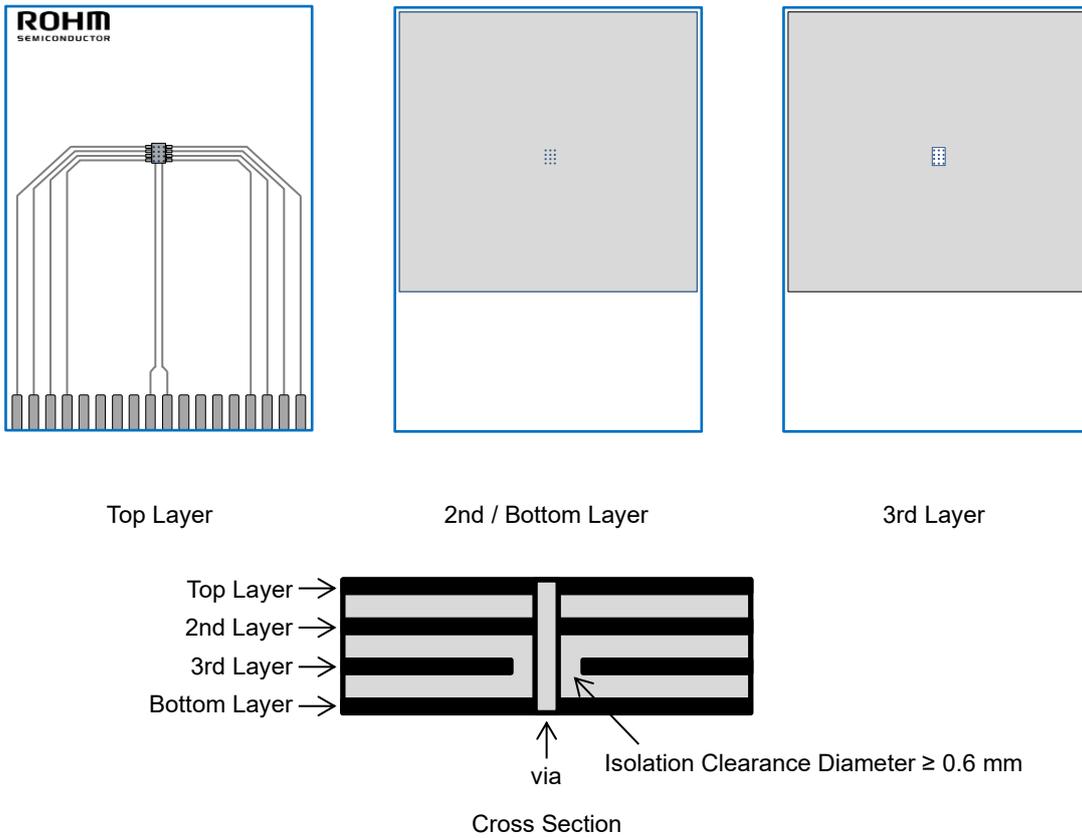


Figure 7. PCB Layout 4 Layers (2s2p)

Dimension	Value
Board Finish Thickness	1.60 mm
Board Dimension	76.2 mm x 114.3 mm
Board Material	FR4
Copper Thickness (Top / Bottom Layers)	0.070 mm (Cu: 1 oz + plating)
Copper Thickness (Inner Layers)	0.035 mm
Thermal Vias Separation / Diameter	1.2 mm / 0.3 mm

Thermal Resistance – continued

■ Thermal Resistance Graphs

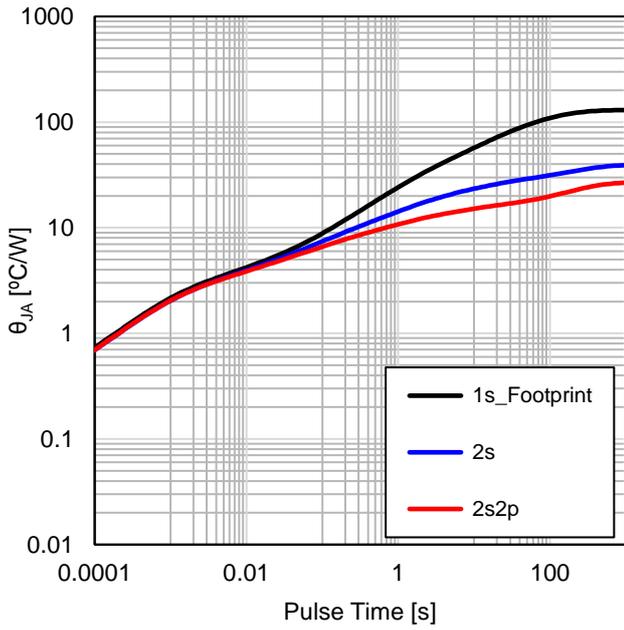


Figure 8. Transient Thermal Resistance

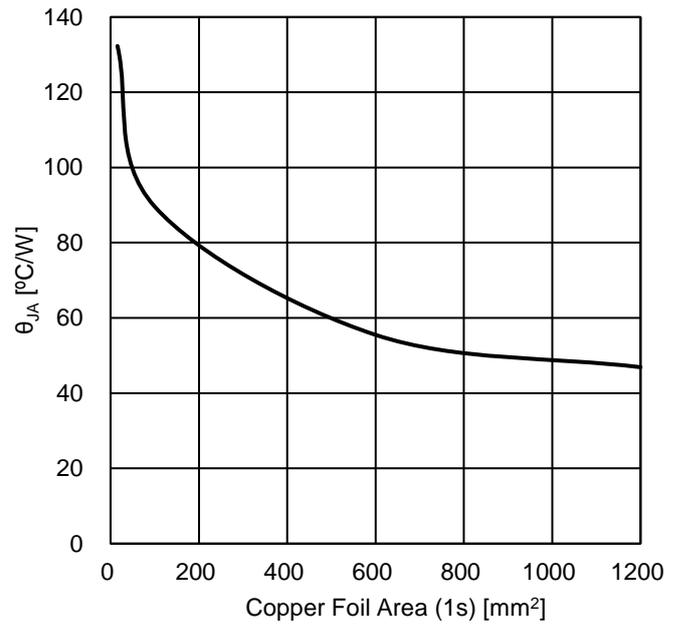


Figure 9. Thermal Resistance

**Electrical Characteristics**(Unless otherwise specified  $V_{BB} = 6\text{ V}$  to  $28\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ )

Parameters	Symbol	Ratings			Unit	Conditions
		MIN	TYP	MAX		
[Power Supply Section]						
Sleep Mode Current	$I_{BBL1}$	-	-	0.5	$\mu\text{A}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$
	$I_{BBL2}$ (Note 1)	-	-	1.0	$\mu\text{A}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 85\text{ }^\circ\text{C}$
	$I_{BBL3}$	-	-	10	$\mu\text{A}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$
Standby Mode Current (Diagnostic Function ON)	$I_{GN DL}$	-	1.0	2.0	$\text{mA}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 5\text{ V}$
Operating Mode Current	$I_{GN DH}$	-	3.0	5.0	$\text{mA}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 5\text{ V}$
UVLO Threshold Voltage	$V_{UV LOH}$	4.7	5.1	5.5	$\text{V}$	$V_{BB}$ : sweep-up, $V_{IN} = 5\text{ V}$ , $V_{OUT}$ reaches more than $V_{BB} - 1\text{ V}$
	$V_{UV LOL}$	3.0	3.5	4.0	$\text{V}$	$V_{BB}$ : sweep-down, $V_{IN} = 5\text{ V}$ , $V_{OUT}$ reaches less than $1\text{ V}$
UVLO Hysteresis Voltage	$V_{UV HYS}$	-	1.6	-	$\text{V}$	$V_{UV HYS} = V_{UV LOH} - V_{UV LOL}$
$V_{BB}$ Overvoltage Protection	$V_{BB CLP}$	41	45	49	$\text{V}$	$I_{BB} = 10\text{ mA}$
[Input Section (IN / SEN pin)]						
High Level Input Voltage	$V_{IH}$	2.1	-	-	$\text{V}$	
Low Level Input Voltage	$V_{IL}$	-	-	0.9	$\text{V}$	
Input Hysteresis Voltage	$V_{IHYS}$	-	0.25	-	$\text{V}$	
High Level Input Current	$I_{IH}$	-	50	100	$\mu\text{A}$	$V_{IN}$ , $V_{SEN} = 5\text{ V}$
Low Level Input Current	$I_{IL}$	-	5	10	$\mu\text{A}$	$V_{IN}$ , $V_{SEN} = 0.5\text{ V}$
[Output Section]						
Output ON Resistance	$R_{ON1}$	-	40	60	$\text{m}\Omega$	$V_{BB} \geq 8\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$ , $I_{OUT} = 1\text{ A}$
	$R_{ON2}$	-	-	90	$\text{m}\Omega$	$V_{BB} \geq 8\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ , $I_{OUT} = 1\text{ A}$
	$R_{ON3}$	-	-	75	$\text{m}\Omega$	$V_{BB} = 6\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$ , $I_{OUT} = 0.5\text{ A}$
Output Leakage Current	$I_{OUTL1}$	-	-	0.5	$\mu\text{A}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$
	$I_{OUTL2}$ (Note 1)	-	-	1.0	$\mu\text{A}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 85\text{ }^\circ\text{C}$
	$I_{OUTL3}$	-	-	10	$\mu\text{A}$	$V_{BB} = 18\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$
$V_{DS}$ Voltage at Light Load	$V_{DSSL}$	-	10	24	$\text{mV}$	$V_{IN} = 5\text{ V}$ , $I_{OUT} = 50\text{ mA}$
Output Slew Rate when ON	$SR_{ON}$	-	0.3	0.7	$\text{V}/\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\text{ }\Omega$ , $T_j = 25\text{ }^\circ\text{C}$ , $V_{OUT} = 30\%$ to $70\%$ of $V_{BB}$
Output Slew Rate when OFF	$-SR_{OFF}$	-	0.3	0.7	$\text{V}/\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\text{ }\Omega$ , $T_j = 25\text{ }^\circ\text{C}$ , $V_{OUT} = 70\%$ to $30\%$ of $V_{BB}$
Output Propagation Time Delay when Turning ON	$t_{OD\_ON}$	-	50	100	$\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\text{ }\Omega$ , $T_j = 25\text{ }^\circ\text{C}$ , $V_{OUT}$ rises at $20\%$ of $V_{BB}$
Output Propagation Time Delay when Turning OFF	$t_{OD\_OFF}$	-	30	100	$\mu\text{s}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\text{ }\Omega$ , $T_j = 25\text{ }^\circ\text{C}$ , $V_{OUT}$ drops at $80\%$ of $V_{BB}$
Switch ON Energy	$E_{ON}$	-	0.23	-	$\text{mJ}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\text{ }\Omega$ , $T_j = 25\text{ }^\circ\text{C}$
Switch OFF Energy	$E_{OFF}$	-	0.23	-	$\text{mJ}$	$V_{BB} = 14\text{ V}$ , $R_L = 6.5\text{ }\Omega$ , $T_j = 25\text{ }^\circ\text{C}$
Reverse Current (Note 1)	$I_{REVC}$	-	-2	-	$\text{A}$	$V_{IN} = 5\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$
Body Diode Voltage	$V_{DSDI}$	-	0.5	0.9	$\text{V}$	$I_{OUT} = -10\text{ mA}$ , $T_j = 150\text{ }^\circ\text{C}$
$V_{DS}$ Active Clamping Voltage	$V_{DSCLP}$	41	45	49	$\text{V}$	$I_{OUT} = 10\text{ mA}$

## Electrical Characteristics – continued

(Unless otherwise specified  $V_{BB} = 6\text{ V}$  to  $28\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ )

Parameters	Symbol	Ratings			Unit	Conditions
		MIN	TYP	MAX		
[Output Protection Section]						
Overcurrent Detection Value (Note 1) (Note 2)	$I_{OCD\_5V}$	21	30	40	A	$V_{DS} = 5\text{ V}$
	$I_{OCD\_5V\_TSD}$	-	26	-	A	$V_{DS} = 5\text{ V}$ , during thermal toggling
	$I_{OCD\_28V}$	-	16	-	A	$V_{DS} = 28\text{ V}$
Temperature Shutdown Detection Threshold (Note 1) (Note 2)	$T_{TSD}$	150	175	200	$^\circ\text{C}$	
Temperature Shutdown Detection Hysteresis (Note 1)	$T_{TSDHYS}$	-	15	-	$^\circ\text{C}$	
Dynamic Temperature Protection Threshold (Note 1) (Note 2)	$T_{DTJ}$	-	90	-	K	Differential temperature
[Diagnostic / SENSE Section]						
Output Pull Up Current	$I_{OLD}$	50	100	200	$\mu\text{A}$	$V_{BB} = 14\text{ V}$ , $V_{IN} = 0\text{ V}$ , $V_{SEN} = 5\text{ V}$ , $V_{OUT} = 5\text{ V}$
Open Load at OFF $V_{DS}$ Threshold	$V_{DSOL}$	1.0	2.0	3.0	V	$V_{IN} = 0\text{ V}$ , $V_{SEN} = 5\text{ V}$
Output Pull Down Resistor	$R_{PD}$	-	500	-	$\text{k}\Omega$	
SENSE Leakage Current	$I_{SENSEL}$	-	-	0.5	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ , $V_{SEN} = 0\text{ V}$ , $V_{SENSE} = 0\text{ V}$
	$I_{SENSELD}$	-	-	0.5	$\mu\text{A}$	$V_{IN} = 0\text{ V}$ , $V_{SEN} = 5\text{ V}$ , $V_{SENSE} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$
Diagnostic Error Flag Current	$I_{SENSEH}$	7	15	23	mA	$V_{BB} \geq 8\text{ V}$ , $V_{SENSE} = 0\text{ V}$
Diagnostic Error Flag Voltage	$V_{SENSEH}$	4.0	5.8	6.6	V	$V_{BB} \geq 8\text{ V}$ , $R_{SENSE} = 1\text{ k}\Omega$
SENSE Output Delay Time when the Device Turns ON	$t_{DS\_ON}$	-	90	200	$\mu\text{s}$	$R_L = 6.5\text{ }\Omega$ , $V_{SEN} = V_{IN} = 0\text{ to }5\text{ V}$ , $R_{SENSE} = 1\text{ k}\Omega$
SENSE Output Delay Time when Diagnostic Turns ON	$t_{DS\_DON}$	-	10	50	$\mu\text{s}$	$R_L = 6.5\text{ }\Omega$ , $V_{IN} = 5\text{ V}$ , $V_{SEN} = 0\text{ V to }5\text{ V}$ , $R_{SENSE} = 1\text{ k}\Omega$
SENSE Output Delay Time when Diagnostic Turns OFF	$t_{DS\_DOFF}$	-	10	50	$\mu\text{s}$	$R_L = 6.5\text{ }\Omega$ , $V_{IN} = 5\text{ V}$ , $V_{SEN} = 5\text{ V to }0\text{ V}$ , $R_{SENSE} = 1\text{ k}\Omega$
SENSE Settling Time during Load Current Switching	$t_{DS\_CHG\_H}$	-	-	20	$\mu\text{s}$	$V_{IN} = V_{SEN} = 5\text{ V}$ , $I_{OUT} = 1\text{ A to }2\text{ A}$ , $R_{SENSE} = 1\text{ k}\Omega$
	$t_{DS\_CHG\_L}$	-	0.4	1.0	ms	$V_{IN} = V_{SEN} = 5\text{ V}$ , $I_{OUT} = 1\text{ A to }50\text{ mA}$ , $R_{SENSE} = 1\text{ k}\Omega$
Open Load at OFF Detection Mask Time (Note 1) (Note 2)	$t_{OLDMSK}$	-	150	400	$\mu\text{s}$	$V_{DS} = 0\text{ V}$ , $V_{SEN} = 5\text{ V}$ , $V_{IN} = 5\text{ V to }0\text{ V}$
Diagnostic Error Flag Release Delay Time (Note 1) (Note 2)	$t_{ERRFD}$	-	500	900	$\mu\text{s}$	$V_{IN} = 0\text{ V}$ , $V_{SEN} = 5\text{ V}$ , $V_{DS} = 0\text{ V to }5\text{ V}$
Current Sense Ratio 1	$K_1$	-50 %	1600	+50 %	-	$V_{BB} = 14\text{ V}$ , $I_{OUT} = 0.05\text{ A}$ , $V_{IN} = V_{SEN} = 5\text{ V}$
Current Sense Ratio 2	$K_2$	-30 %	1550	+30 %	-	$V_{BB} = 14\text{ V}$ , $I_{OUT} = 0.25\text{ A}$ , $V_{IN} = V_{SEN} = 5\text{ V}$
Current Sense Ratio 3	$K_3$	-20 %	1550	+20 %	-	$V_{BB} = 14\text{ V}$ , $I_{OUT} = 0.5\text{ A}$ , $V_{IN} = V_{SEN} = 5\text{ V}$
Current Sense Ratio 4	$K_4$	-10 %	1550	+10 %	-	$V_{BB} = 14\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $V_{IN} = V_{SEN} = 5\text{ V}$
Current Sense Ratio 5	$K_5$	-7 %	1550	+7 %	-	$V_{BB} = 14\text{ V}$ , $I_{OUT} = 2\text{ A}$ , $V_{IN} = V_{SEN} = 5\text{ V}$
Current Sense Ratio 6	$K_6$	-5 %	1550	+5 %	-	$V_{BB} = 14\text{ V}$ , $I_{OUT} = 4\text{ A}$ , $V_{IN} = V_{SEN} = 5\text{ V}$
Current Sense Derating (Note 1)	$\Delta K_1$	-30	-	+30	%	$K_1$ vs $K_2$ , $T_j = 25\text{ }^\circ\text{C}$
	$\Delta K_2$	-5	-	+5	%	$K_4$ vs $K_5$ , $T_j = 25\text{ }^\circ\text{C}$
Output Load Open Detection ON	$I_{OUT\_ONOLD}$	7	16	32	mA	$I_{SENSE} = 10\text{ }\mu\text{A} = (16\text{ mA} / 1600)$

(Note 1) Specified by design and/or statistical analysis of correlated parameters tested in production.

(Note 2) Functional test only.

Typical Performance Curves

(Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

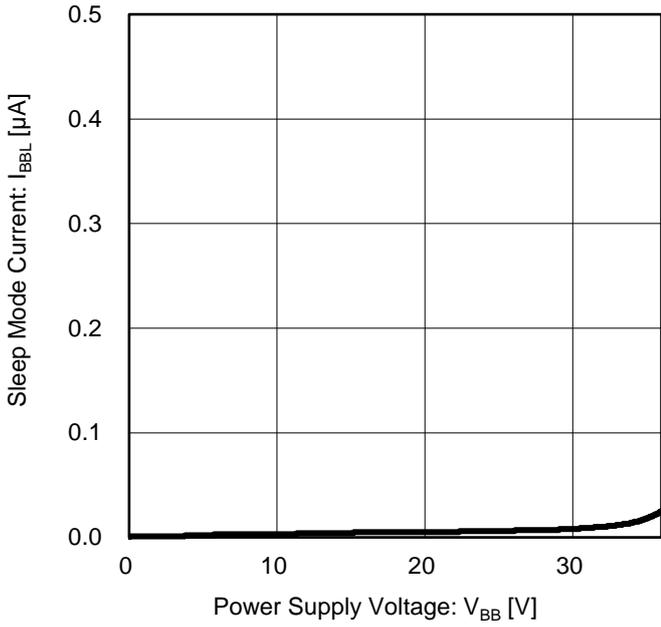


Figure 10. Sleep Mode Current vs Power Supply Voltage

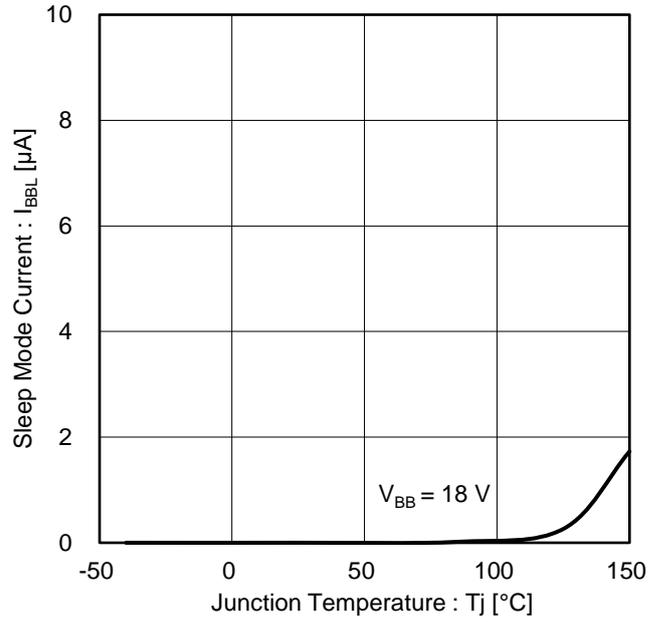


Figure 11. Sleep Mode Current vs Junction Temperature

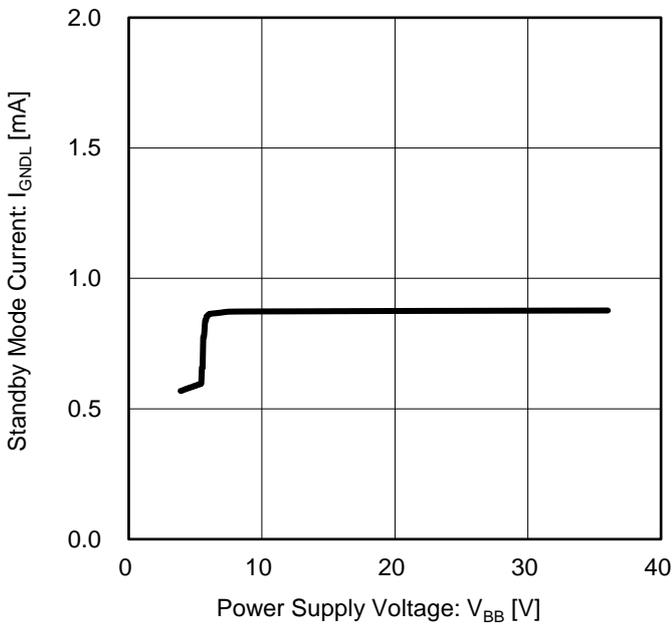


Figure 12. Standby Mode Current vs Power Supply Voltage

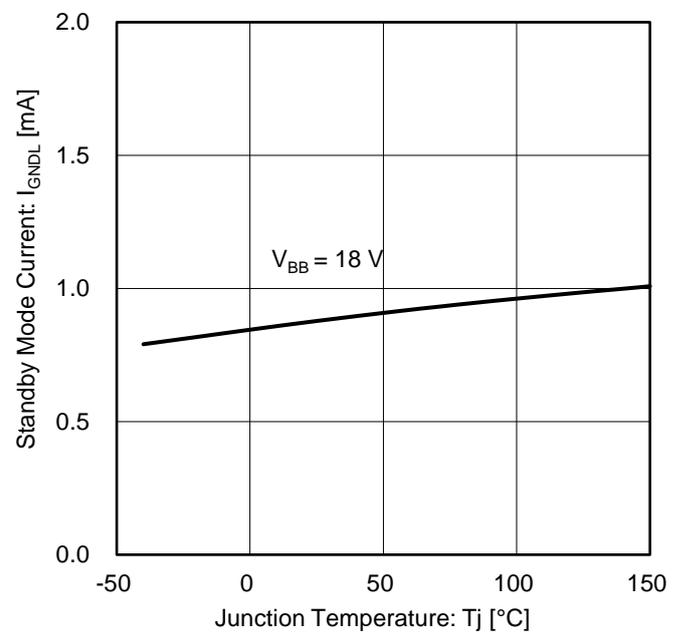


Figure 13. Standby Mode Current vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

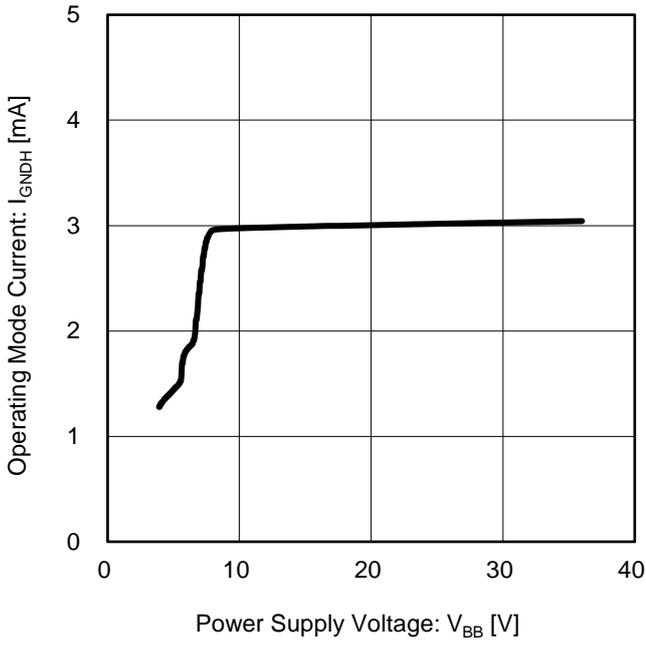


Figure 14. Operating Mode Current vs Power Supply Voltage

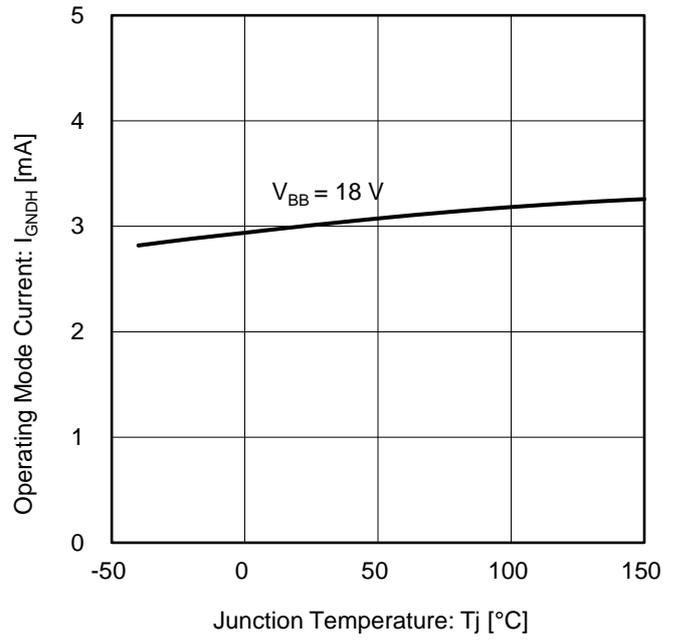


Figure 15. Operating Mode Current vs Junction Temperature

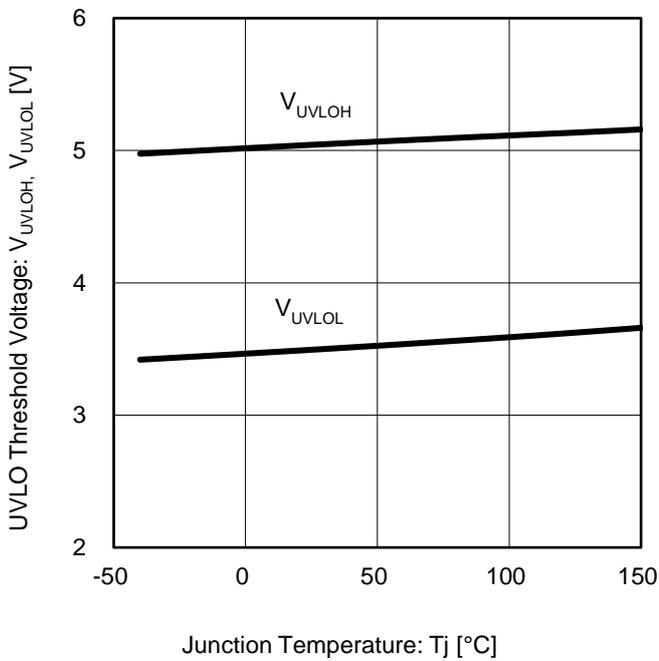


Figure 16. UVLO Threshold Voltage vs Junction Temperature

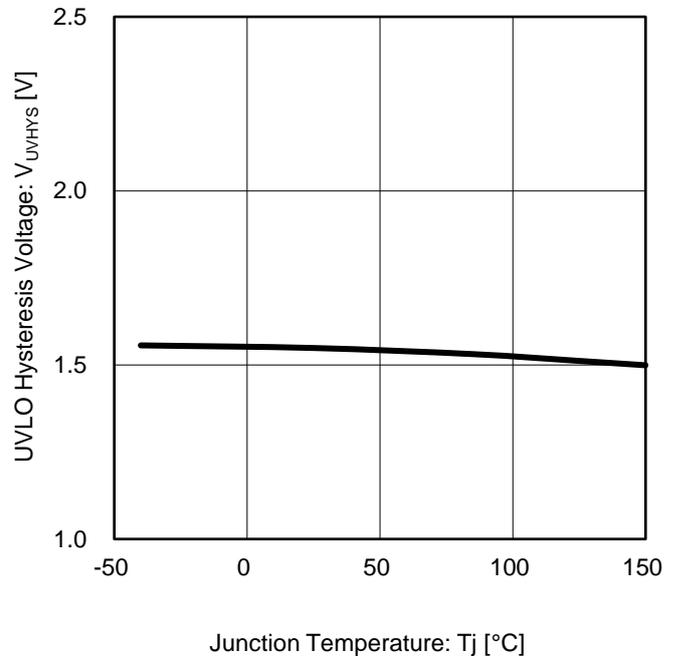


Figure 17. UVLO Hysteresis Voltage vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

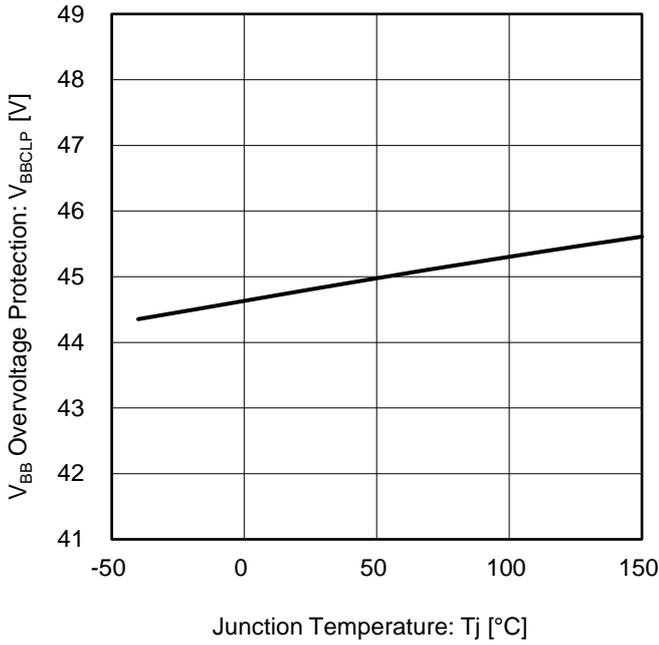


Figure 18.  $V_{BB}$  Overvoltage Protection vs Junction Temperature

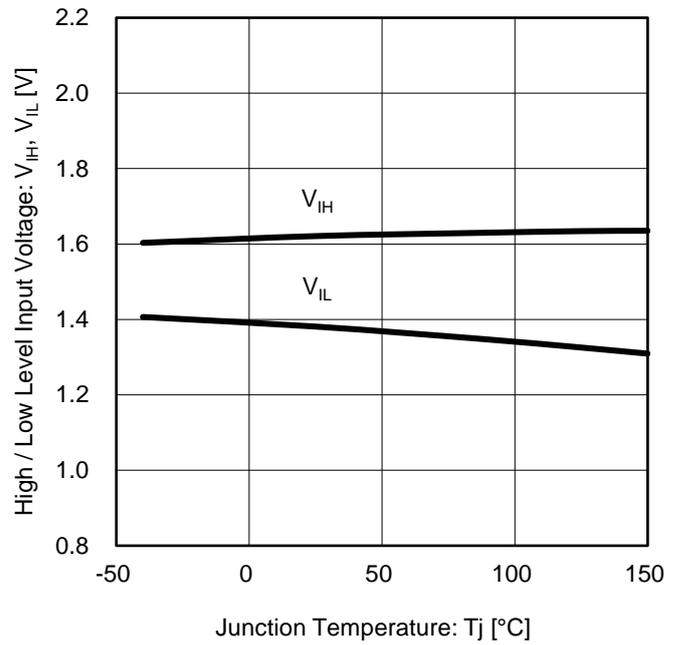


Figure 19. High / Low Level Input Voltage vs Junction Temperature

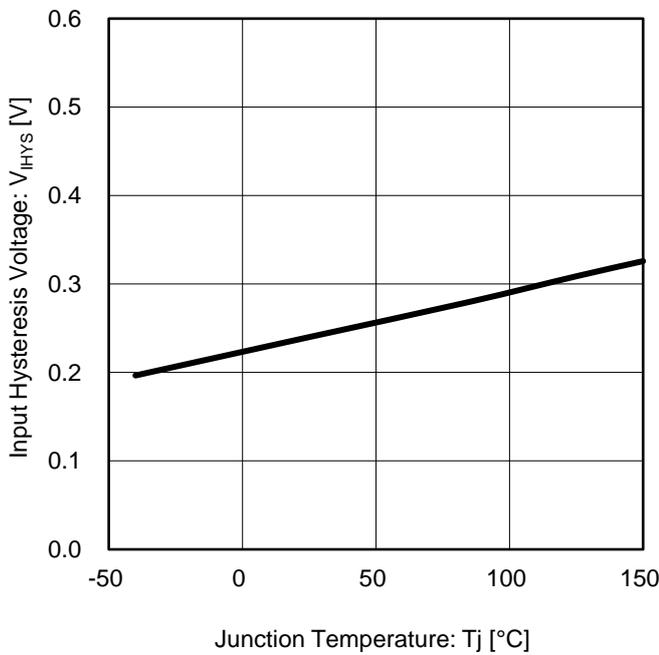


Figure 20. Input Hysteresis Voltage vs Junction Temperature

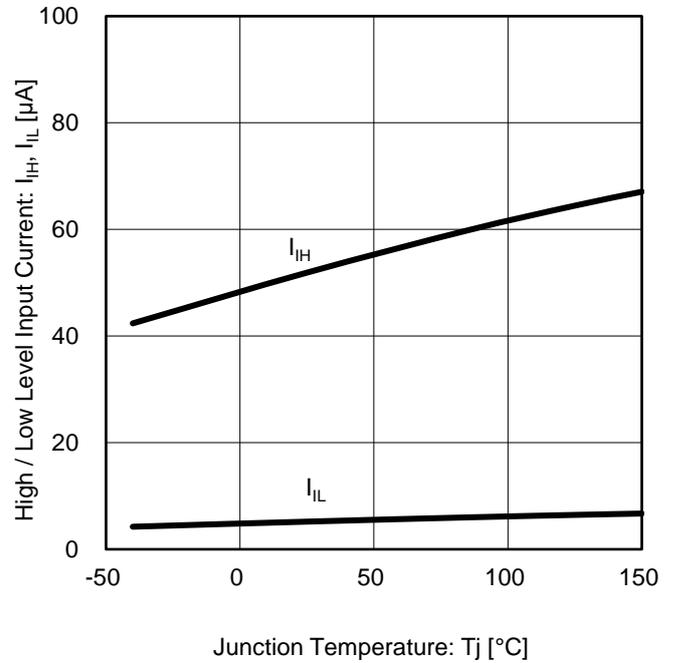


Figure 21. High / Low Level Input Current vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

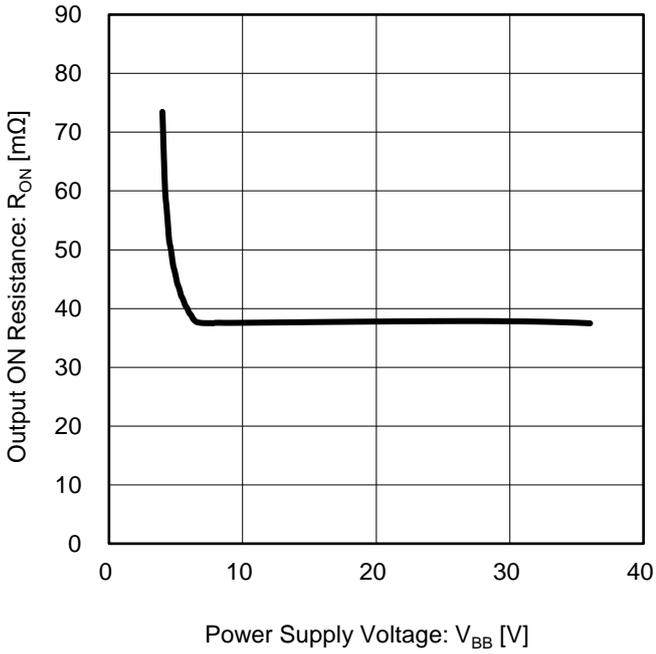


Figure 22. Output ON Resistance vs Power Supply Voltage

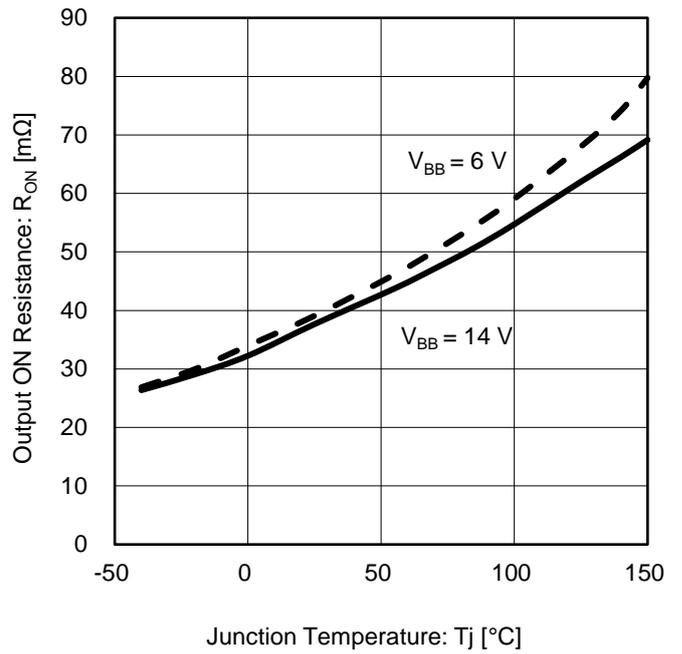


Figure 23. Output ON Resistance vs Junction Temperature

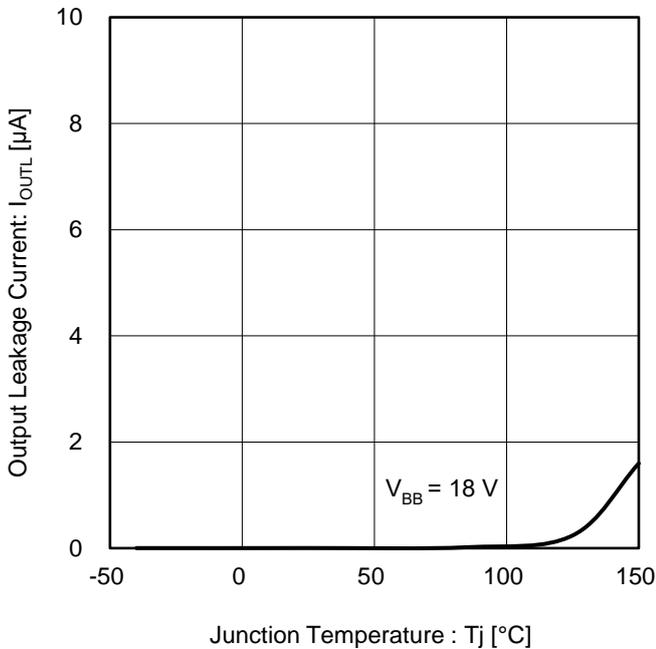


Figure 24. Output Leakage Current vs Junction Temperature

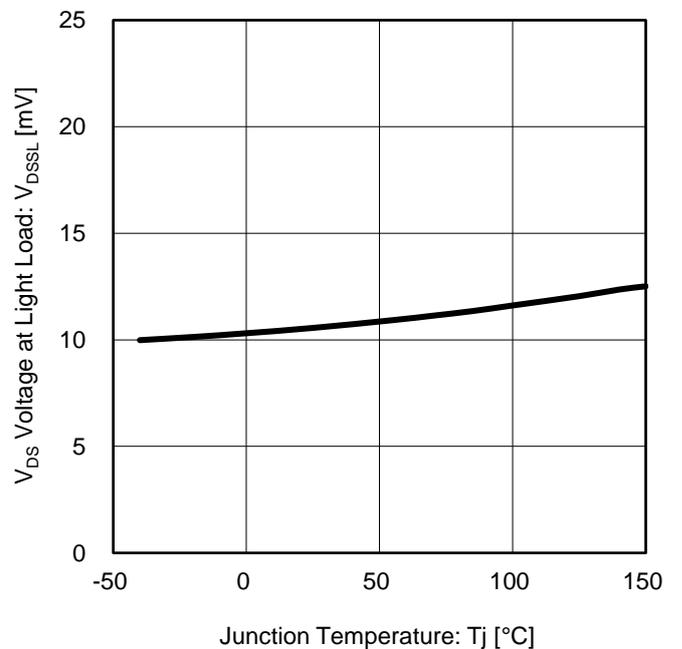


Figure 25.  $V_{DS}$  Voltage at Light Load vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

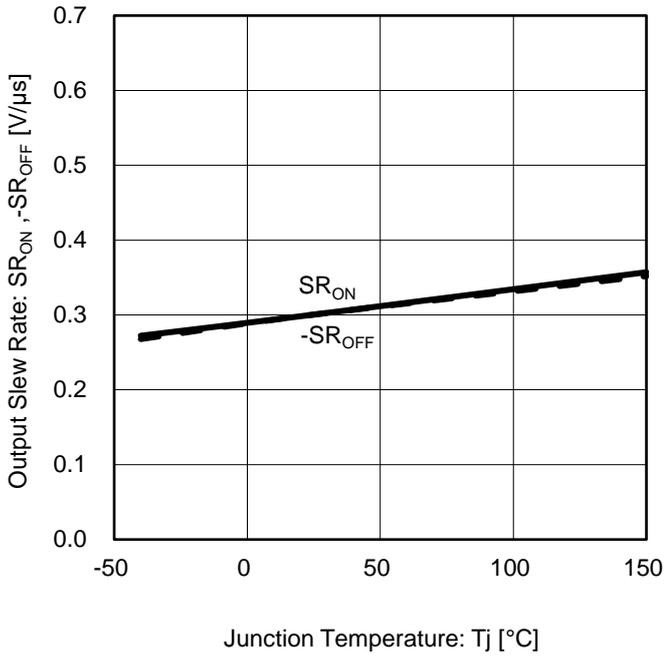


Figure 26. Output Slew Rate vs Junction Temperature

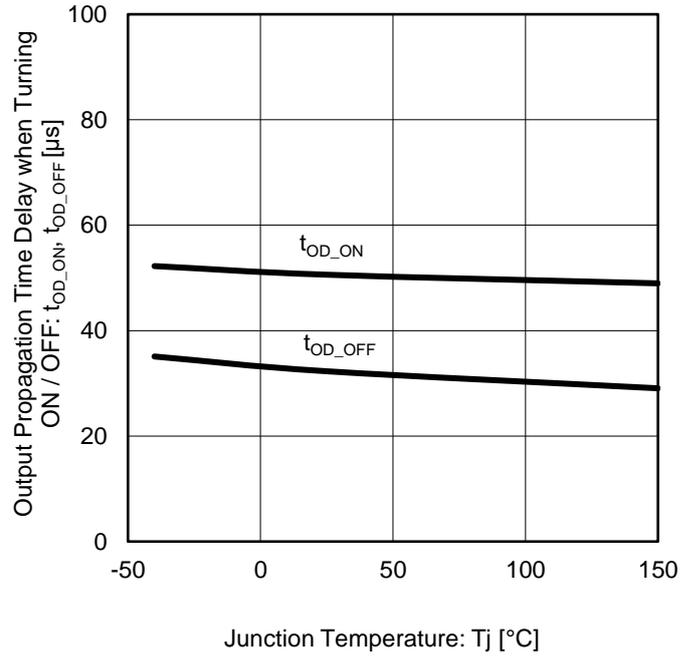


Figure 27. Output Propagation Time Delay when Turning ON / OFF vs Junction Temperature

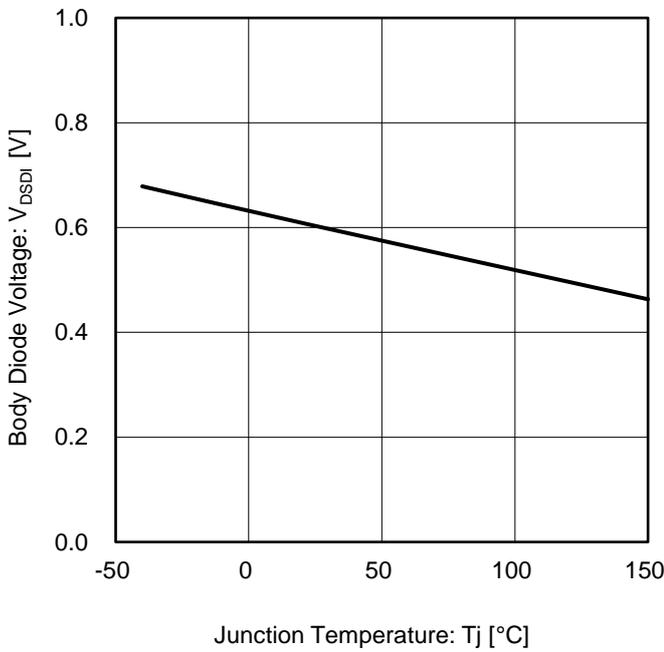


Figure 28. Body Diode Voltage vs Junction Temperature

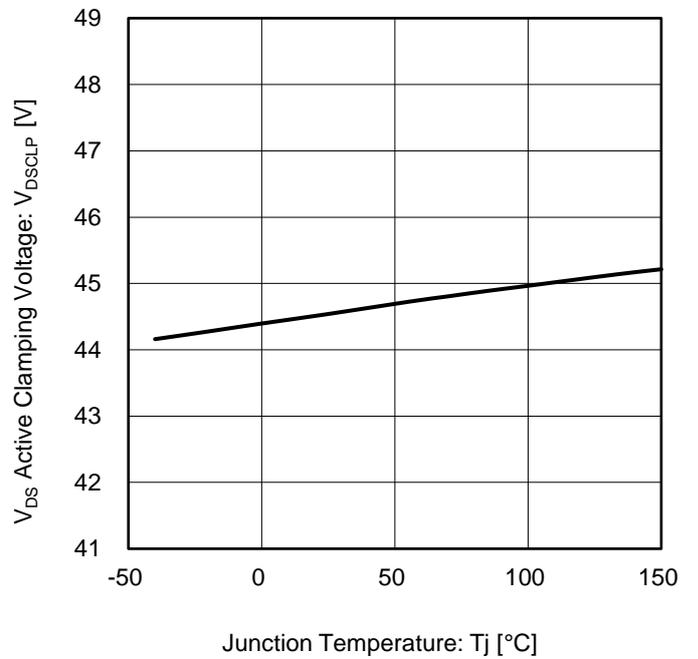


Figure 29.  $V_{DS}$  Active Clamping Voltage vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

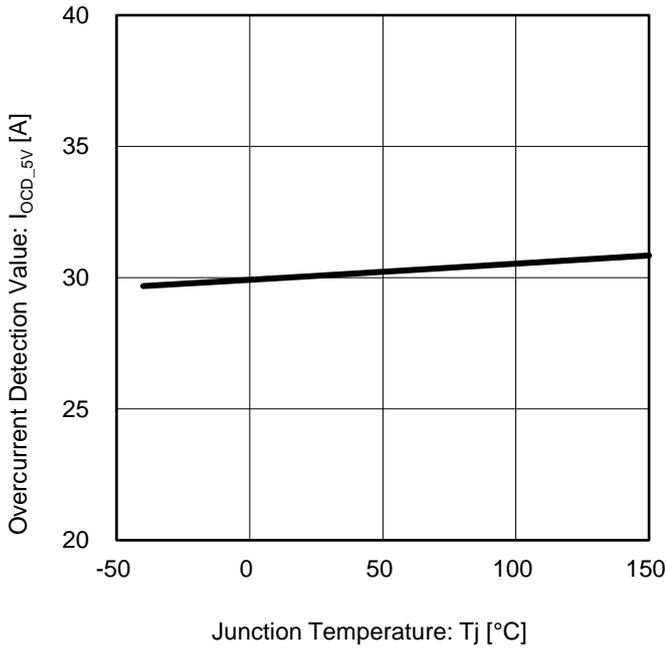


Figure 30. Overcurrent Detection Value vs Junction Temperature

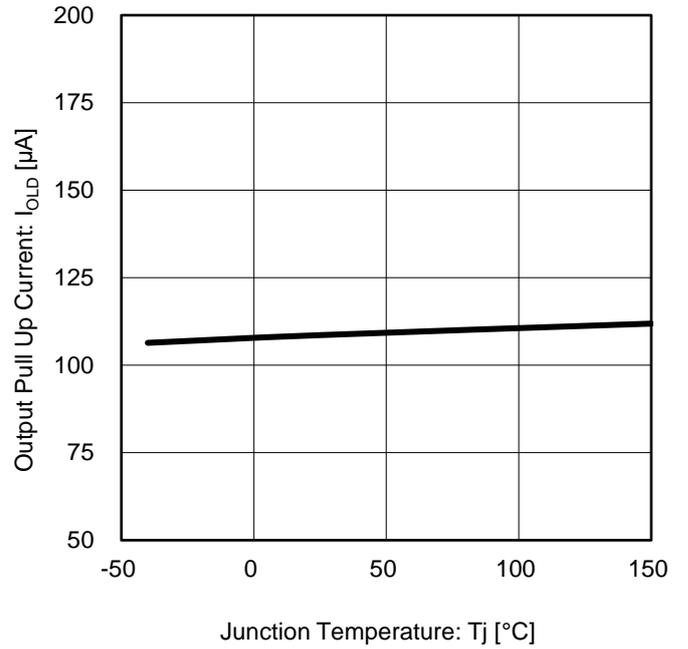


Figure 31. Output Pull Up Current vs Junction Temperature

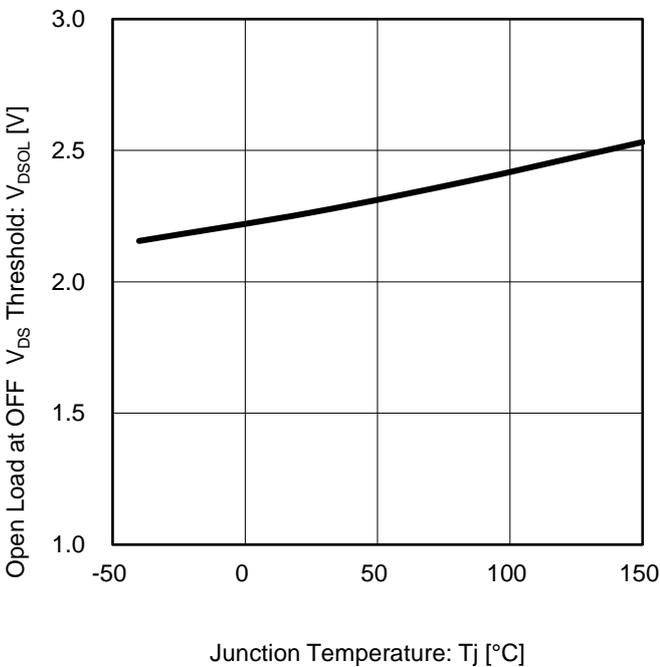


Figure 32. Open Load at OFF  $V_{DS}$  Threshold vs Junction Temperature

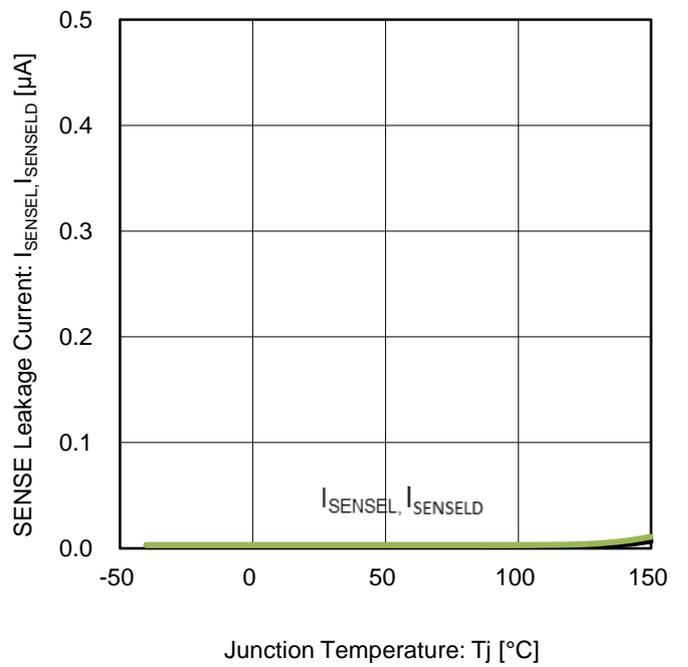


Figure 33. SENSE Leakage Current vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

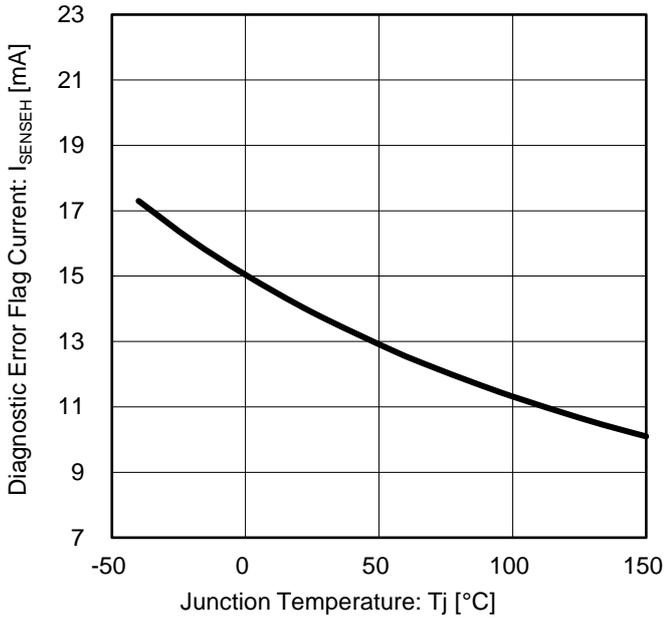


Figure 34. Diagnostic Error Flag Current vs Junction Temperature

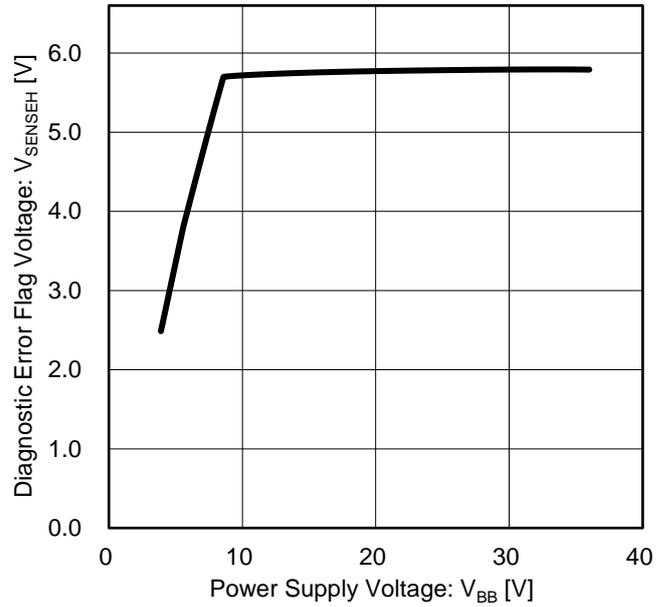


Figure 35. Diagnostic Error Flag Voltage vs Power Supply Voltage

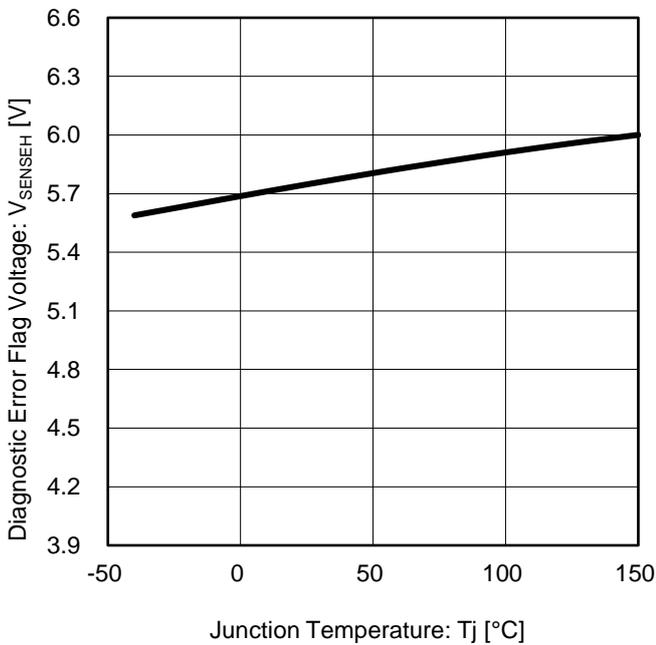


Figure 36. Diagnostic Error Flag Voltage vs Junction Temperature

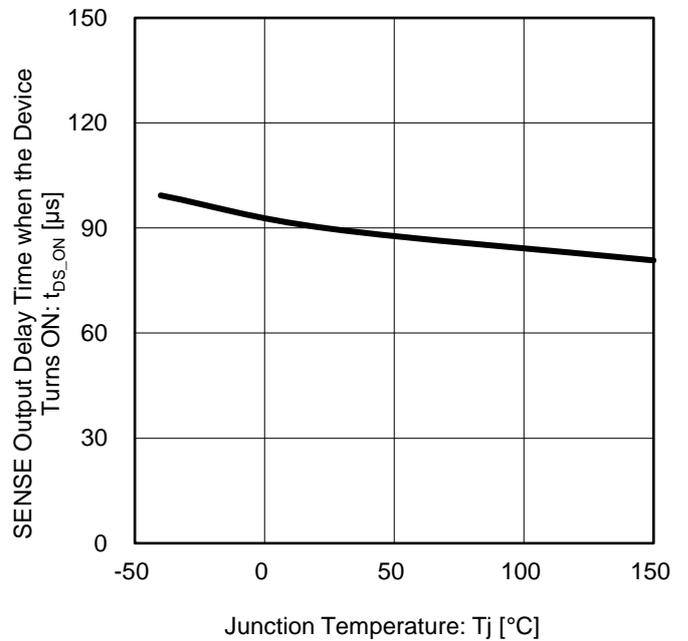


Figure 37. SENSE Output Delay Time when the Device Turns ON vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

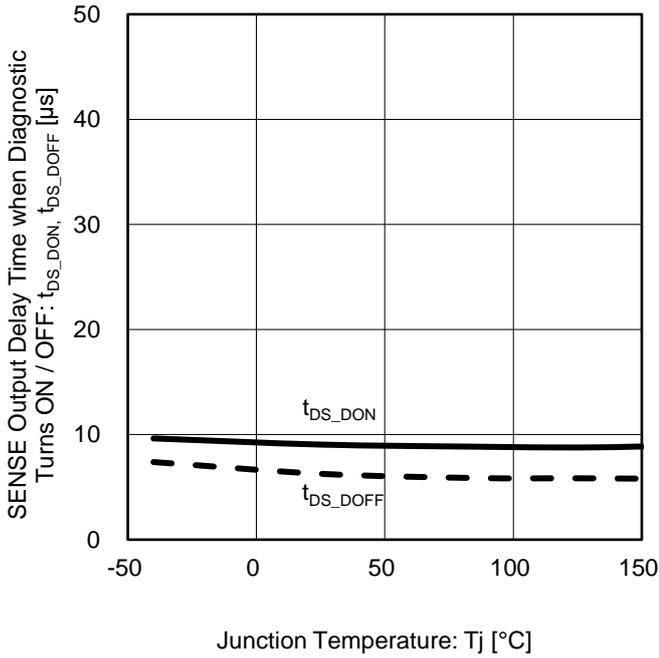


Figure 38. SENSE Output Delay Time when Diagnostic Turns ON / OFF vs Junction Temperature

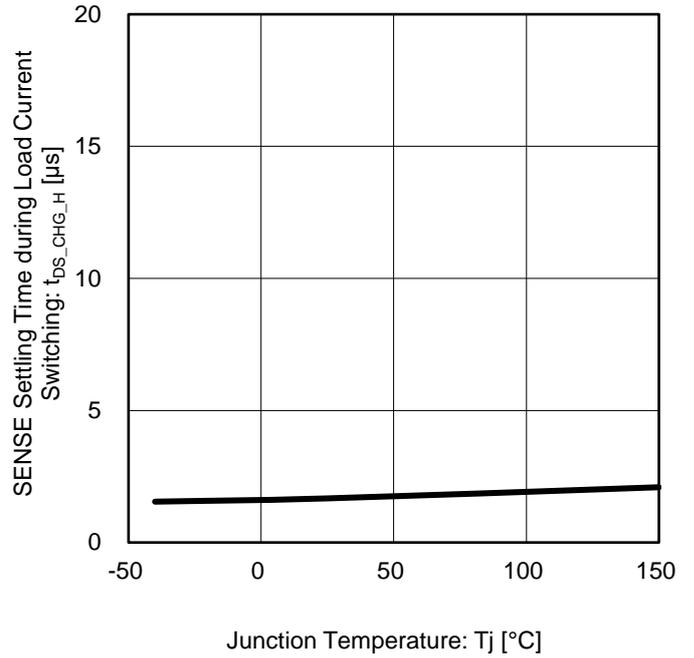


Figure 39. SENSE Settling Time during Load Current Switching vs Junction Temperature

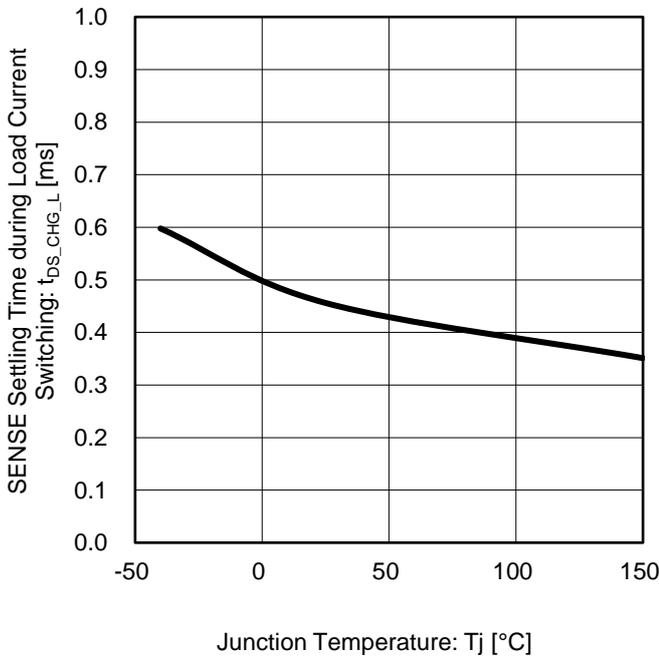


Figure 40. SENSE Settling Time during Load Current Switching vs Junction Temperature

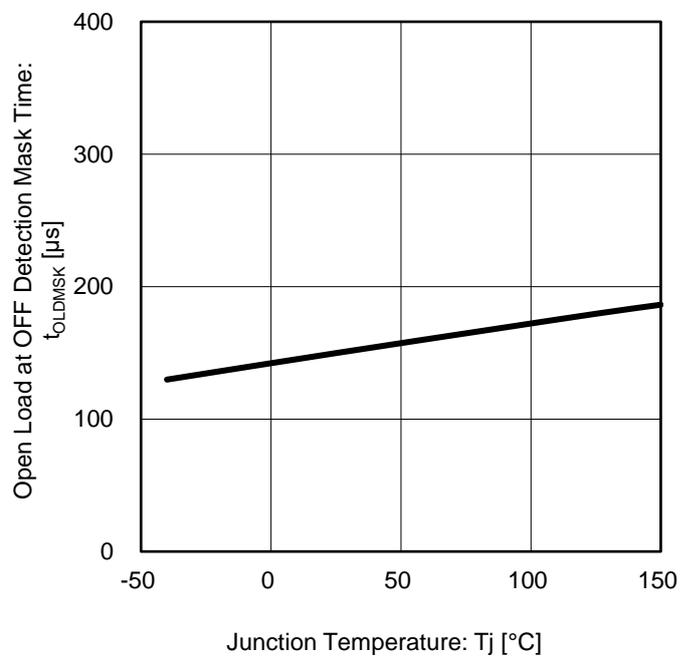


Figure 41. Open Load at OFF Detection Mask Time vs Junction Temperature

**Typical Performance Curves – continued**  
 (Unless otherwise specified  $V_{BB} = 14\text{ V}$ ,  $T_j = 25\text{ }^\circ\text{C}$ )

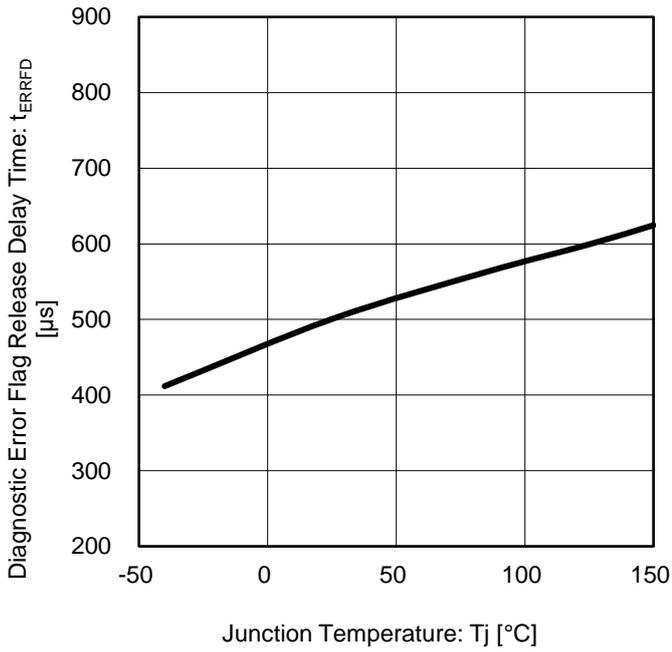


Figure 42. Diagnostic Error Flag Release Delay Time vs Junction Temperature

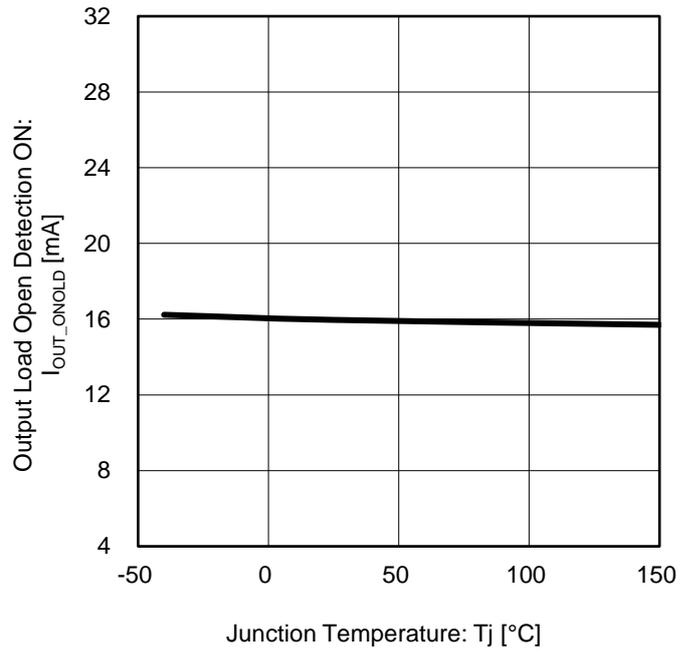


Figure 43. Output Load Open Detection ON vs Junction Temperature

Measurement Circuit Diagram

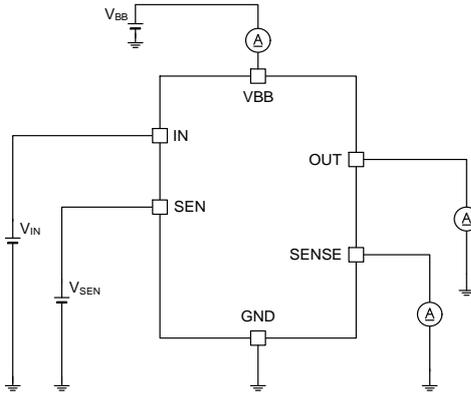


Figure 44. Sleep Mode Current  
OUT Leakage Current  
SENSE Leakage Current

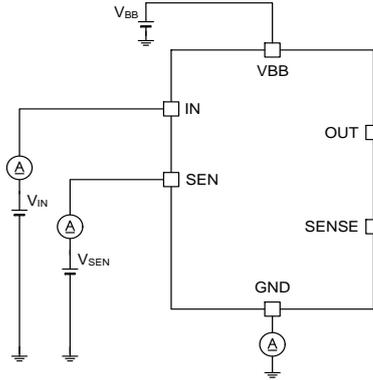


Figure 45. Standby Mode Current  
Operating Mode Current

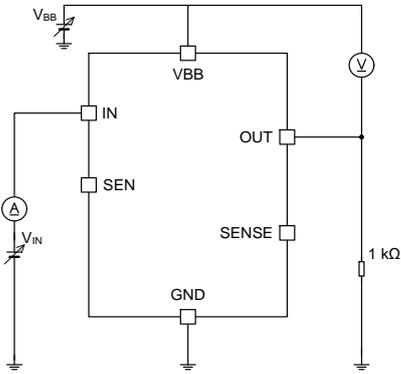


Figure 46. UVLO Threshold / Hysteresis Voltage  
High / Low Level Input Voltage (IN)  
Input Hysteresis Voltage (IN)  
High / Low Level Input Current (IN)

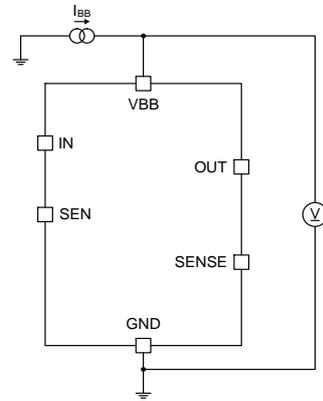


Figure 47.  $V_{BB}$  Overvoltage Protection

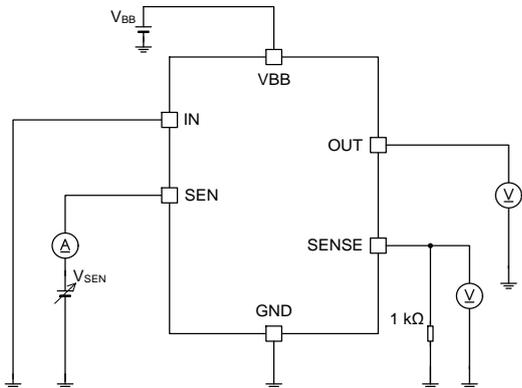


Figure 48. High / Low Level Input Voltage (SEN)  
Input Hysteresis Voltage (SEN)  
High / Low Level Input Current (SEN)

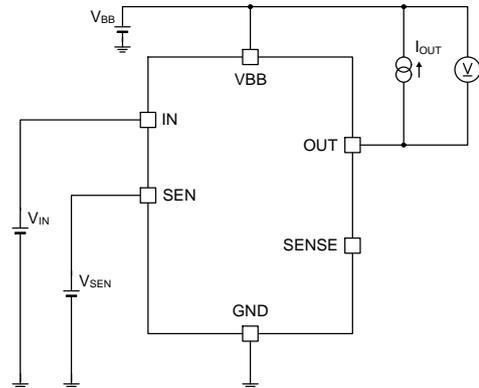


Figure 49. Output ON Resistance  
 $V_{DS}$  Voltage at Light Load  
Body Diode Voltage  
 $V_{DS}$  Active Clamping Voltage

Measurement Circuit Diagram – continued

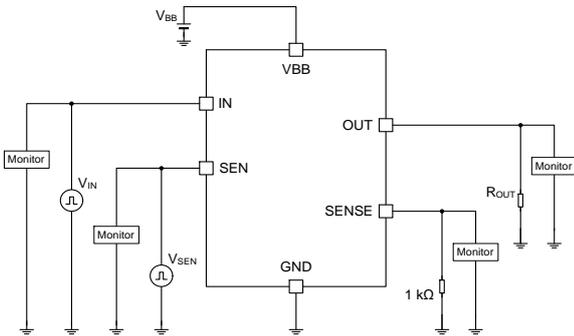


Figure 50. Output Slew Rate when ON / OFF  
Output Propagation Delay Time when Turning ON / OFF  
SENSE Output Delay Time when the Device Turns ON  
SENSE Output Delay Time when Diagnostic Turns ON / OFF

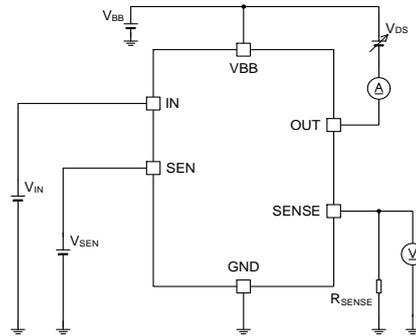


Figure 51. Open Load at OFF  $V_{DS}$  Threshold  
Output Pull Up Current  
Diagnostic Error Flag Voltage

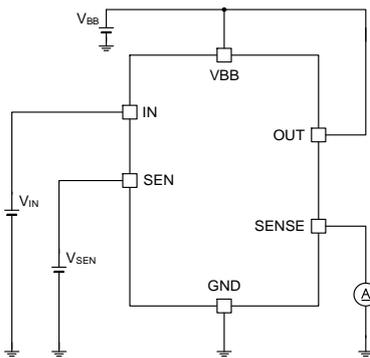


Figure 52. SENSE Leak Current  
Diagnostic Error Flag Current

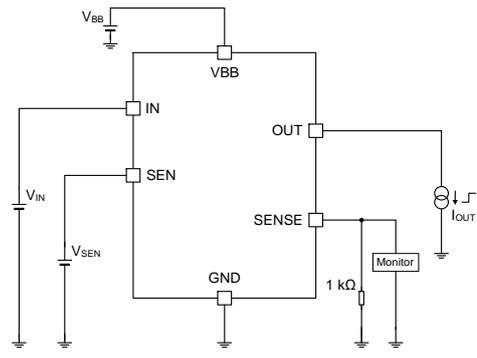


Figure 53. SENSE Settling Time During Load Current Switching

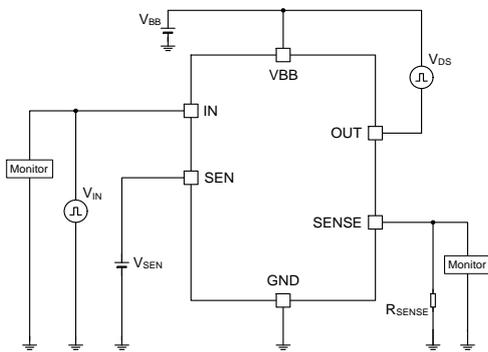


Figure 54. Open Load at OFF Detection Mask Time  
Diagnostic Error Flag Release Delay Time

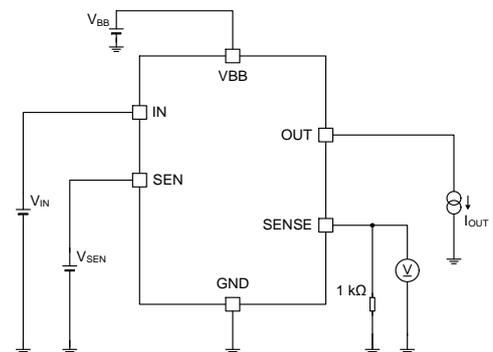


Figure 55. Current Sense Ratio

Block Diagram

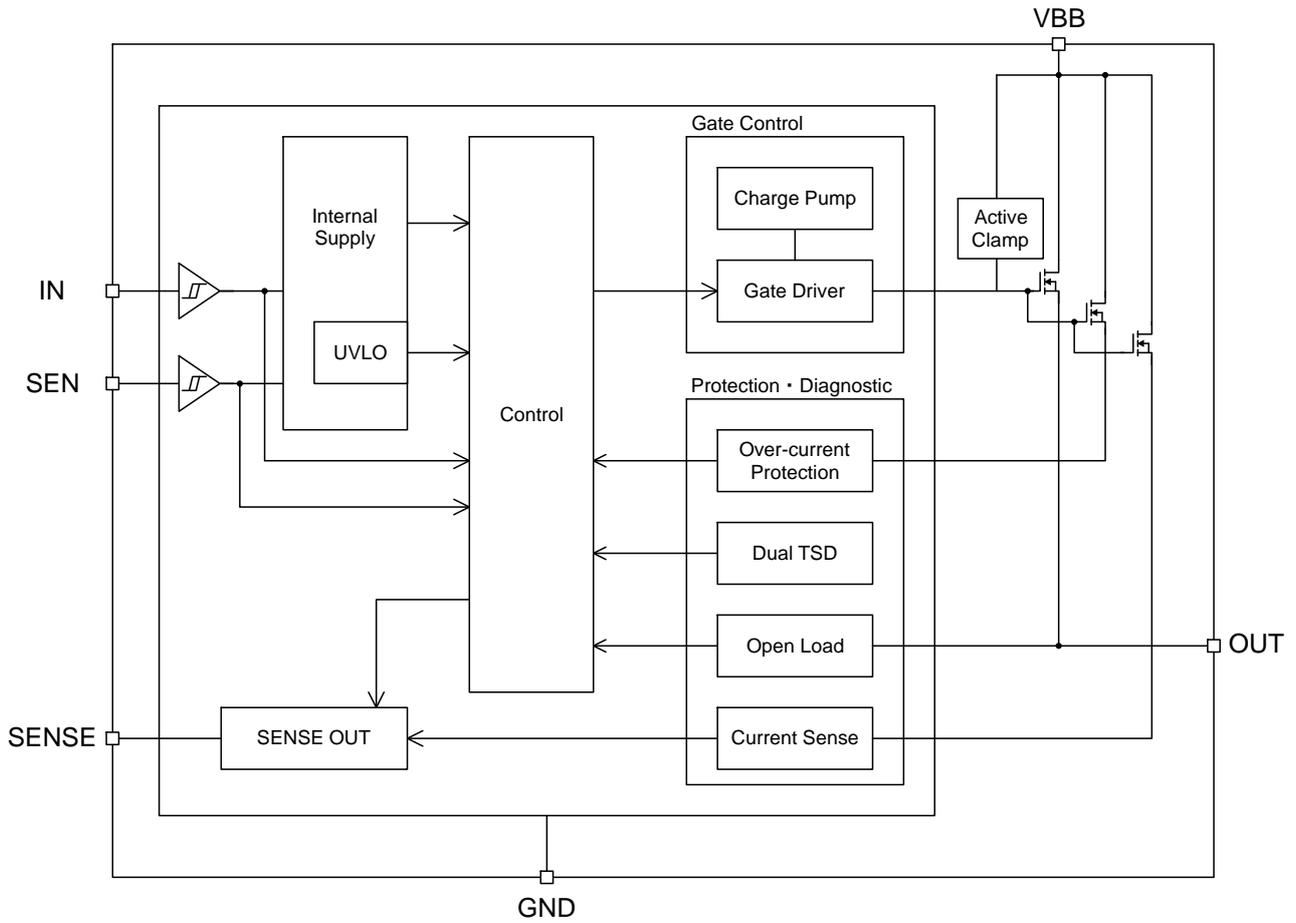


Figure 56. Block Diagram

Features Description

Input Pins

The input circuitry is compatible with 3.3 V and 5 V microcontrollers. The IN and SEN pins must be connected to the microcontroller via 4.7 kΩ resistors. In case not used, the pins shall be connected to ground via resistors; 4.7 kΩ or more is recommended.

The input circuitry reacts to voltage thresholds and avoids undefined states by use of internal hysteresis. Setting the IN pin voltage above 2.1 V the High Side Power Switch output turns on. The device is in Operating mode. Setting the SEN pin voltage above 2.1 V the diagnostic functions are activated. Setting the IN pin voltage below 0.9 V the output is turned off. Setting the SEN pin voltage below 0.9 V the diagnostic functions are deactivated.

With IN and SEN input pins “low” the device enters Sleep mode; all internal circuits are switched off to prevent current consumption from the power supply, output is turned off and no protection is active. In case the IN pin is de-asserted i.e., IN is “low” and the SEN pin is kept “high” then the device enters in a Standby mode with diagnostic functions activated. In this scenario the current consumption is reduced, but not stopped.

In case the connection is interrupted, the input pins are pulled down internally; only in case all input pins are low the Sleep mode is activated. The internal pull-down is implemented with a resistance. Furthermore, internal de-bounce filters make sure the circuits are not activated or deactivated by high frequency noise or other voltage spikes at the pins.

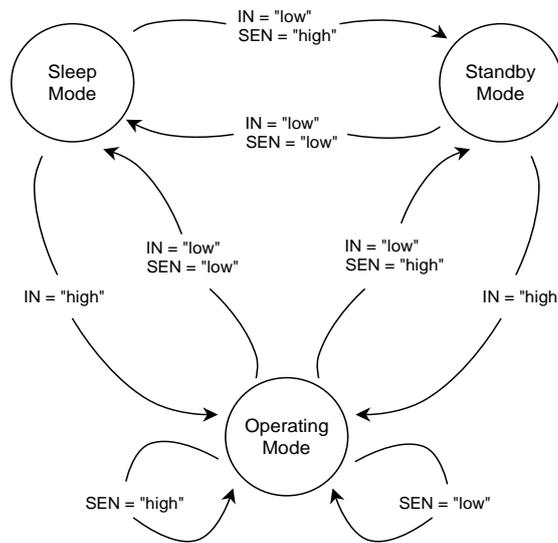


Figure 57. State Diagram

Internal Supply and Under Voltage Lock Out (UVLO)

The Power Supply Line Input  $V_{BB}$  is used to energize and supply internal circuitry and generate internal voltage references. The Intelligent High Side Power Device is designed to operate down to very low battery cranking voltages. However, as with any battery powered device it still needs a certain minimum voltage to operate. An under voltage protection circuit with hysteresis makes sure the device does nothing until the supply voltage is high enough and a predictable behavior can be maintained. The UVLO circuit prevents an undefined output state and/or unintended diagnostic functions turn on when the  $V_{BB}$  voltage is below the specified threshold.

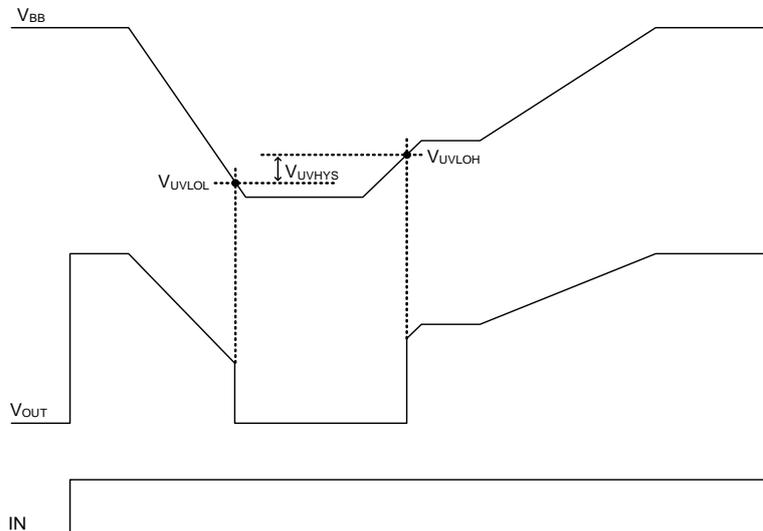


Figure 58. UVLO Functionality

Features Description – continued

Control Circuitry

The device integrates logic circuits that control the operation of the Intelligent High Side Power Switch. Based on the state of the protection circuits and given inputs the control logic performs state transitions and produces outputs as such.

Gate Control Circuitry

The device integrates a gate driving circuit that acts as interface between the control logic and the N-channel power transistor. A charge pump acts as internal supply allowing to turn on the MOSFET and drive it in the deep triode operation region. The integrated charge pump operates at a fixed frequency improving the EMI performance of the IC. Moreover, the switching behavior of the power transistor is regulated via the gate-driver hence the on and off switching times and slew rates are current-controlled to further improve the EMC.

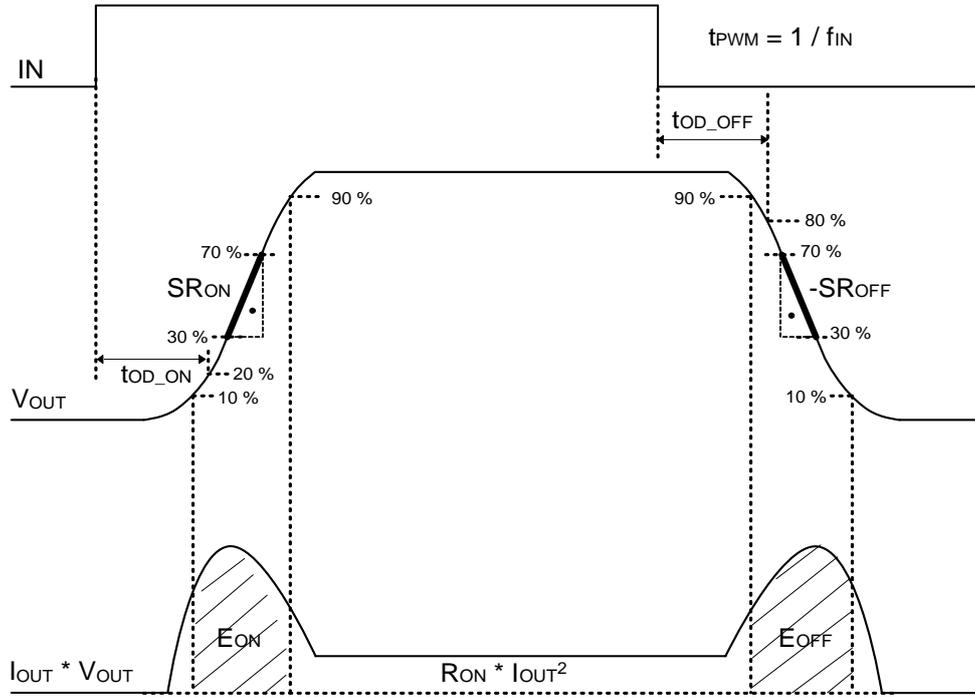


Figure 59. Switching Resistive Loads

Active Clamp Protection

An intelligent integrated active clamp protection limits the maximum  $V_{DS}$  across the power transistor when switching inductive loads at the output pin and the inductive energy is dissipated internally. Moreover, a  $V_{BB}$  to GND internal clamp circuit protects the internal circuits from overvoltage surges.

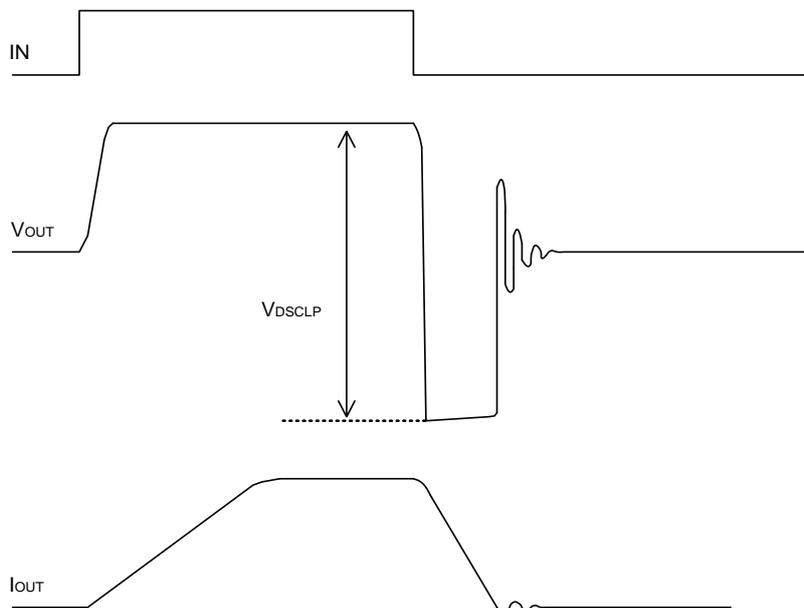


Figure 60. Switching Inductive Loads

Features Description – continued

Loss of Ground Protection

When the module's ground becomes open, the output switches off. However, it is recommended to add resistors connected between the input pins and the microcontroller. Furthermore, it is recommended to keep all the digital inputs pulled either all high or all low to avoid creating parasitic ground paths and prevent the outputs from switching off. If the GND pin is open when an inductive load is driven, the active clamp protection safeguards the IC.

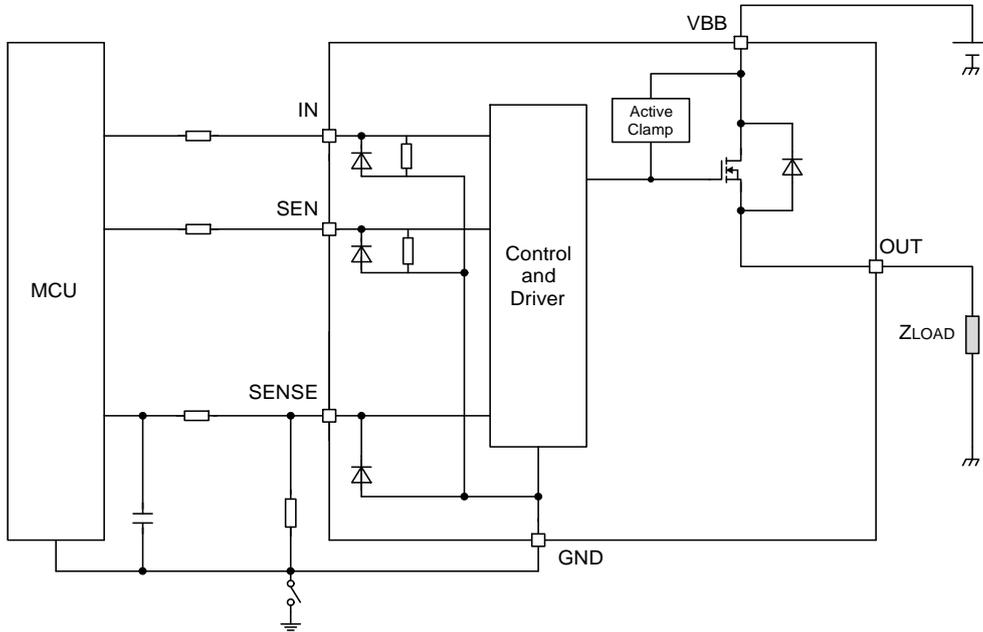


Figure 61. Loss of Ground Protection Diagram

Load Dump and Overvoltage Protection

The integrated VBB to GND overvoltage protection will safeguard the internal circuits from overvoltage transients. In order for the overvoltage protection to work a ground resistance  $R_{GND}$  is necessary. However, a ground shift needs to be considered versus the microcontroller ground when looking at the input voltage threshold levels while in normal operation. Furthermore, the active clamp protection limits the maximum  $V_{DS}$  across the power transistor. Moreover, in case the  $V_{BB}$  voltage exceeds the  $V_{BBCLP}$  level the input pins can start to conduct as well, hence input resistors are mandatory as per the above explanations.

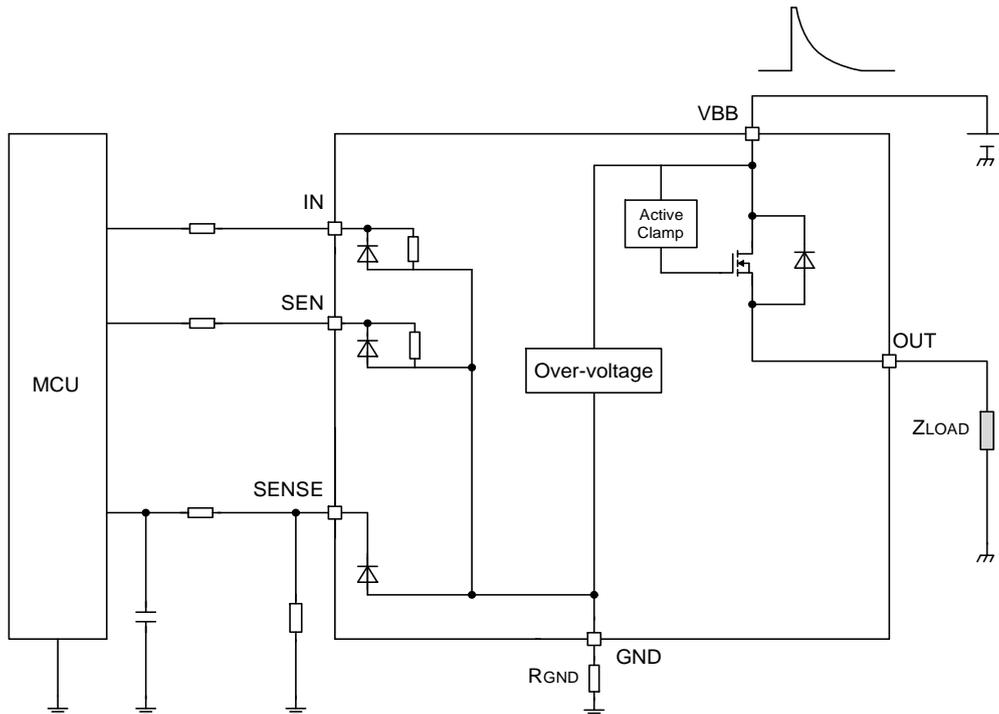


Figure 62. Load Dump Protection Diagram

Features Description – continued

Loss of Battery Protection

When the connection to the battery becomes open the device can dissipate the energy of the wire harness for inductivities up to 10  $\mu$ H without degrading its robustness. The integrated VBB to GND overvoltage protection will act as a freewheeling path and the active clamp at the output will close the path for the current to flow safeguarding the IC. In applications where the nominal load currents are exceeded, and more load inductivity is expected, an external load freewheeling diode is necessary and/or a transient voltage suppressor must be present on the battery line.

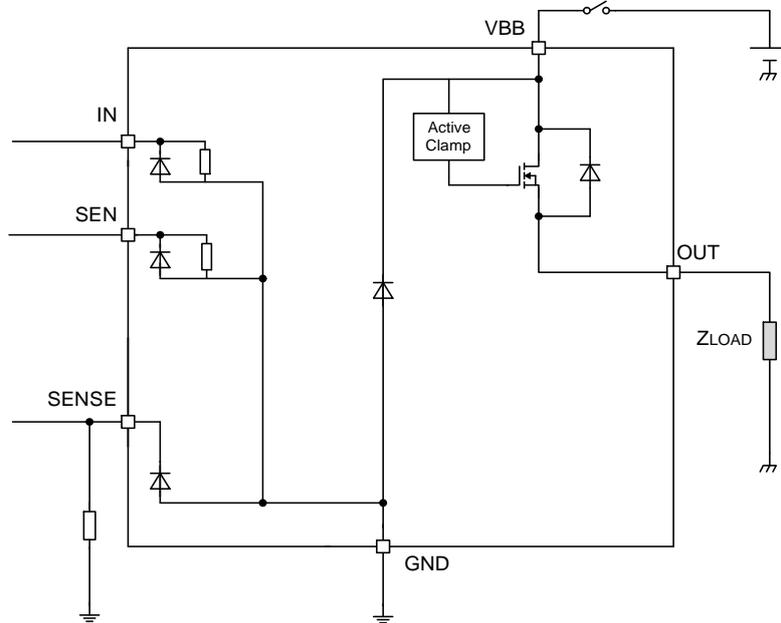


Figure 63. Loss of Battery Diagram

Reverse Battery Protection

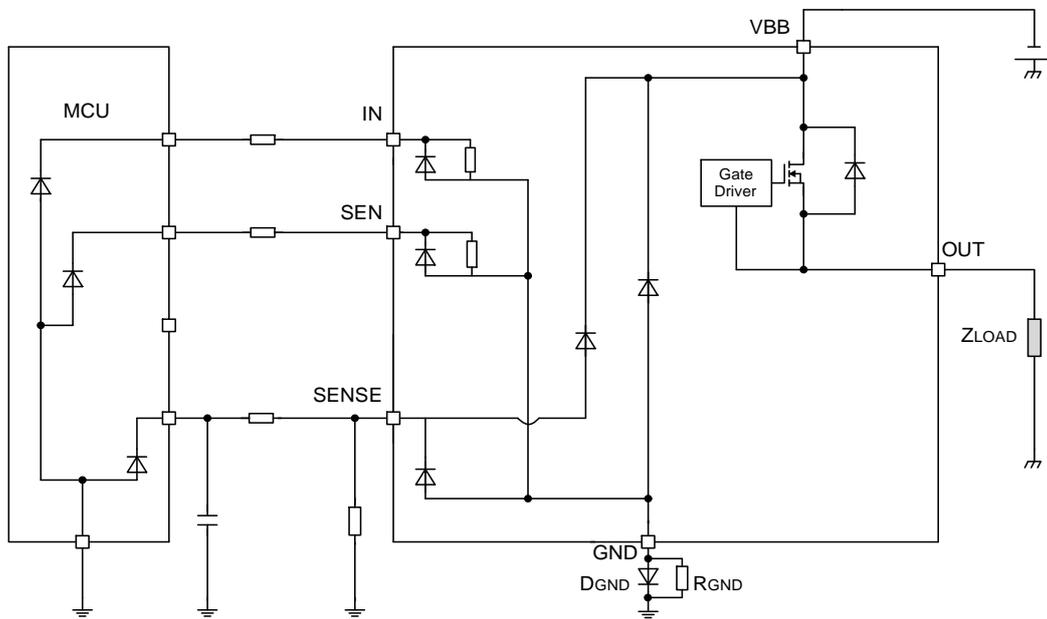


Figure 64. Reverse Battery Diagram

To limit the current through the input pins and the SENSE pin in case of reverse battery connection and negative or positive ISO transients on the battery line, the device's interface pins must be protected with resistors connected between the micro controller and the IC. Furthermore, a ground protection Schottky diode D<sub>GND</sub> is recommended to help improve the robustness of the IC in such scenarios.

A ground resistor at the IC GND pin will protect the IC in reverse battery and in case of negative or positive ISO transients on the battery line. Moreover, the ground resistor safeguards the IC during load dump or over voltage. However, a ground shift needs to be considered versus the micro controller ground when looking at the input voltage threshold levels due to the chip's current consumption in normal operation. Resistor power dissipation needs to be considered during reverse battery conditions.

Features Description – continued

A diode at the IC GND pin will increase the protection level in both reverse battery and negative ISO pulse transients, however it will reduce the positive ISO pulse robustness of the IC and it will diminish the load dump and over voltage protection ability of the IC. Furthermore, it will lessen the loss of battery protection in case of wire harness inductivity; a parallel resistor to the diode is recommended in this case. If a diode is used the load dump, over voltage and loss of battery scenarios need careful examination and external transient voltage suppressors or/and load freewheeling diodes need to be considered. Moreover, a ground shift will be present versus the microcontroller ground. However, the diode could be shared between multiple devices.

During reverse battery the device allows the load current to flow through the body diode of the power MOSFET; the current must be limited by the resistance of the load. However, in case the load is inductive, special care must be taken to ensure safe operation. A reverse polarity diode on the battery line would be a possible solution.

A compromise between the above options must be found depending on the specific application requirements and the targeted loads.

Dual Temperature Shutdown Protection

A dual temperature shutdown (Dual TSD) mechanism limits the internal thermal transients and reduces the mechanical stress of the IC increasing its cyclic short-circuit robustness. The device integrates an absolute and dynamic overtemperature protection circuit. When the chip’s junction temperature rises above either the  $T_{DTJ}$  or the  $T_{TSD}$  threshold, the output turns off. A thermal hysteresis restart mechanism is implemented. When the chip’s temperature falls below a predefined threshold, the output automatically restarts, and operation is resumed accordingly. Moreover, the TSD circuits safeguard the IC in case of overload operation (high inrush current) with the output current below the  $I_{OCD}$  thresholds i.e., before the overcurrent protection activates. When the TSD protection is triggered, the SENSE pin acts as an error flag and signals the fault to the microcontroller. The voltage at the SENSE pin is forced to be  $V_{SENSEH}$ .

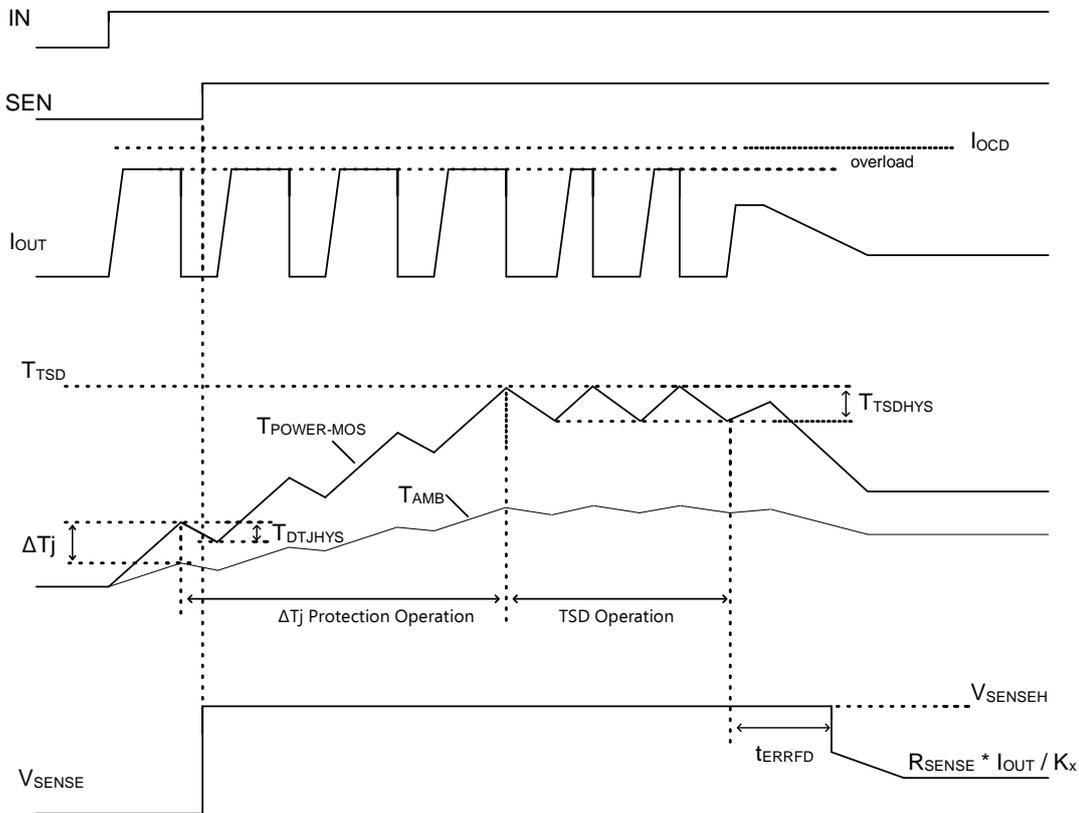


Figure 65. Overtemperature Protection

Features Description – continued

Over Current Protection

The IC has a built-in overcurrent protection feature. If an excessive current flows at the output of the High Side Power Switch, a current limitation aims to protect the IC and peripheral components. Given that a fault is present (short-circuit to ground), or high inrush current at start-up occurs, then the output current is limited to safe operating levels. Moreover, the output current limit is designed to have  $V_{DS}$  voltage dependency in favor of an increased robustness of the device. When the load current is above the  $I_{OCD}$  threshold the SENSE pin acts as an error flag and signals the fault to the microcontroller. The voltage at the SENSE pin is forced to be  $V_{SENSEH}$ . Furthermore, the overtemperature - dual temperature shutdown (TSD) protection - circuits complement the overcurrent protection. In case the overtemperature protection is triggered during current limitation the power MOSFET is turned off, hence the output current will toggle accordingly - a restart happens when the chip has cooled down sufficiently.

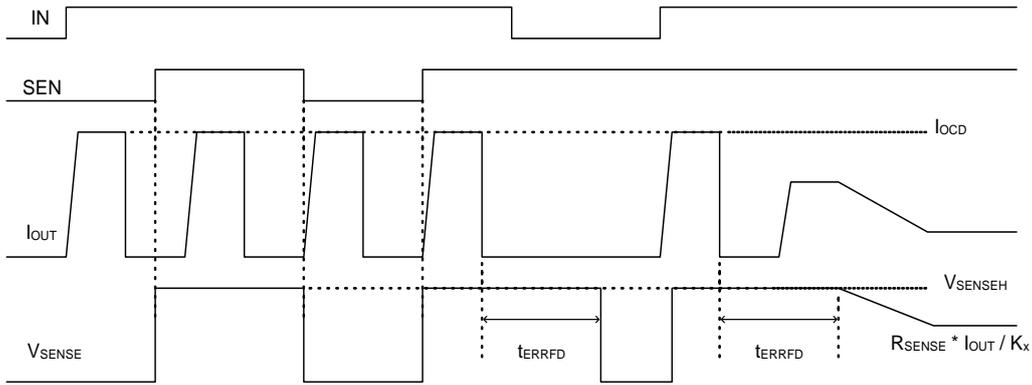


Figure 66. Overcurrent Protection

Reverse Current Protection

The IC allows reverse current to flow through the power MOSFET when the  $V_{OUT}$  voltage level is higher than  $V_{BB}$ . Furthermore, as long as the current is maintained within the nominal range and the package's thermal limitations are not exceeded the IC can maintain its operating state or can switch from off to on and vice versa.

Features Description – continued

Diagnostic / SENSE Functions

Diagnosis / SENSE Output<sup>(Note 1)</sup>

Mode	IN	SEN	SENSE	OUT
Normal Operation	Low	High	Hi-Z	Low
Open Load	Low	High	Hi-Z	$< V_{BB} - V_{DSOL}$
	Low	High	$V_{SENSEH}$	$\geq V_{BB} - V_{DSOL}$
Short to Battery	Low	High	$V_{SENSEH}$	High
Thermal Shutdown	Low	High	Hi-Z	Low
Short to Ground	Low	High	Hi-Z	Low
Reverse Current	Low	High	$V_{SENSEH}$	High
Normal Operation	High	High	$I_{OUT} / K_x$	High
Open Load	High	High	$I_{OUT\_ONOLD} / K_x$	High
Short to Battery	High	High	$< I_{OUT} / K_x$	High
Thermal Shutdown	High	High	$V_{SENSEH}$	Low
Short to Ground	High	High	$V_{SENSEH}$	Low
Reverse Current	High	High	Hi-Z	High
All modes	-	Low	Hi-Z	-

(Note 1) All values in the above table are Typ values and SENSE is considered Hi-Z looking into the pin i.e.,  $R_{SENSE}$  is ignored.

The current sense and diagnostic functions are enabled by setting the voltage  $V_{SEN} = \text{High}$ . The operation is as per the above table. However, an external resistor  $R_{SENSE}$  must be connected between SENSE and GND pins. The simplified implementation is described in the below diagram.

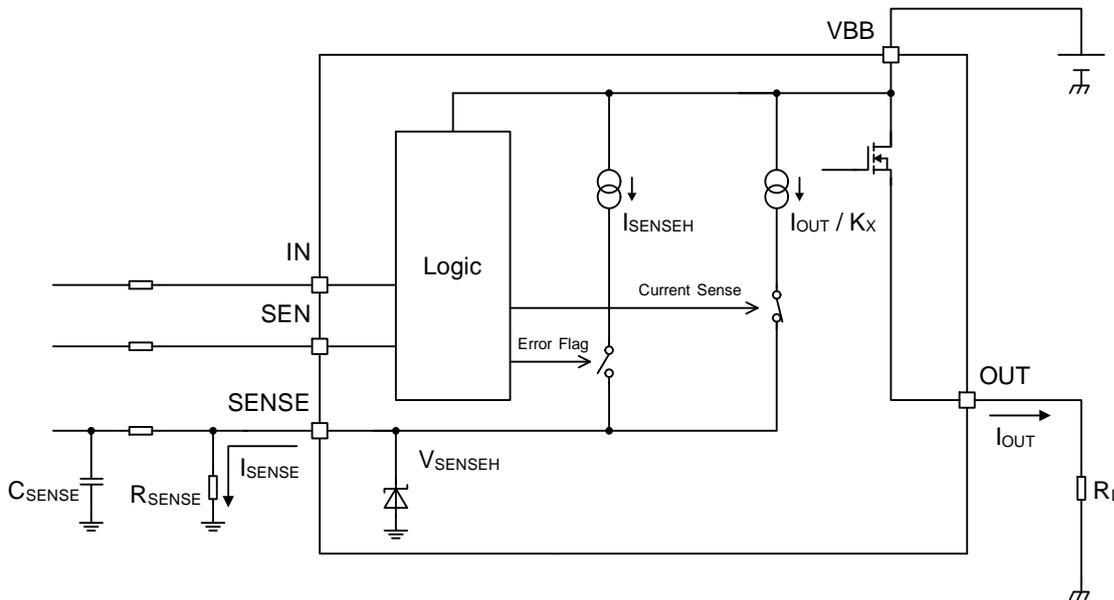


Figure 67. Diagnostic Output Block Diagram

Features Description – continued

Current Sense

When the diagnostic is enabled, and the high side power switch is turned on, a current proportional to the load current is flowing through the SENSE pin. The current  $I_{SENSE}$  becomes equal to  $I_{OUT} / K_X$ , ( $K_X$ : Current sense ratio). An external resistor  $R_{SENSE}$  is recommended, hence for example the voltage at the SENSE pin is equal to:

$$V_{SENSE} = \frac{R_{SENSE} \times I_{OUT}}{K_X}$$

Current Sense Ratio Accuracy

The below diagram shows the load current sense ratio dependency vs. the output current through the power MOSFET. The accuracy of the current sense ratio depends on the load current, technological process, voltage and temperature. A higher-precision current sense ratio could be obtained with additional calibration on the application side. The device allows derating at a specific point ( $\Delta K_X$ ,  $T_j = 25^\circ C$ ). Moreover, to reduce signal ripple at the microcontroller side, it is recommended to insert an external RC filter between the SENSE pin and the ADC input pin.

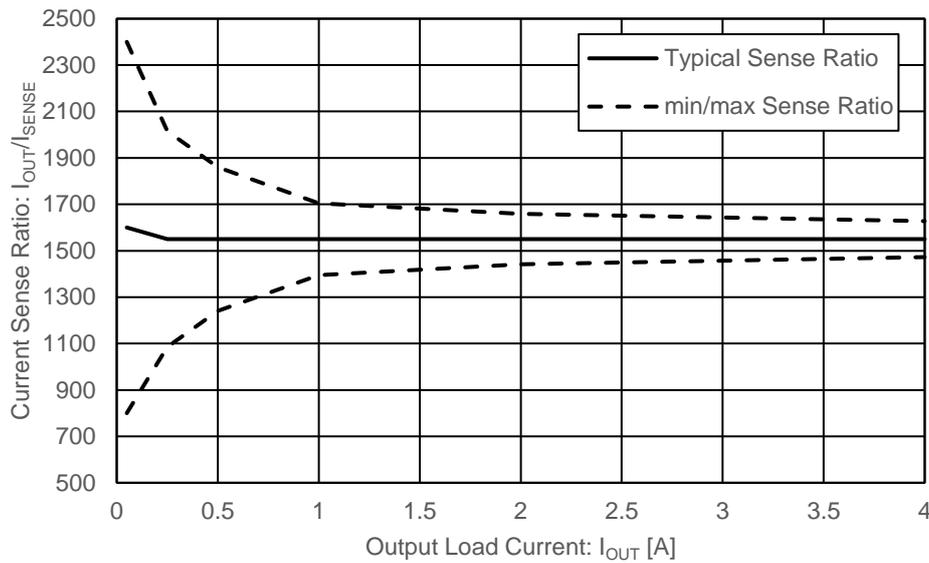


Figure 68. Current Sense Ratio vs Output Load Current

Furthermore, an open load at ON condition can be recognized via the sense ratio if the load current falls below a certain threshold. This is given by the  $I_{OUT\_ONOLD}$  parameter.

Open Load Detection

Open load at off can be detected by connecting an external resistance  $R_{OLD}$  between power supply  $V_{BB}$  and OUT.

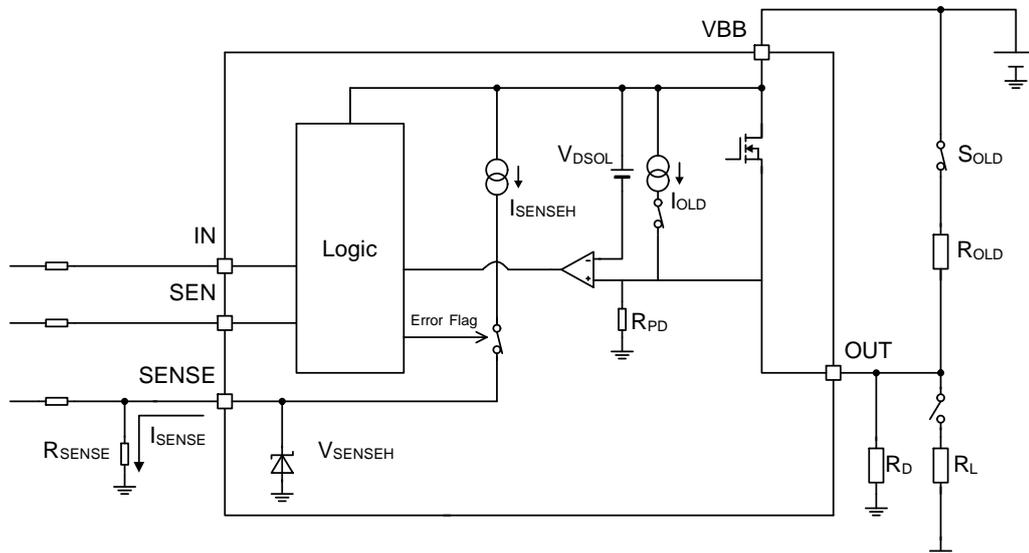


Figure 69. Open Load Detection Block Diagram

Features Description – continued

When the output load is disconnected, input pin IN is low and SEN is high, and open load will be flagged at the SENSE pin by the  $V_{SENSEH}$  voltage if the load is missing or the output is shorted to the VBB battery line. To reduce the standby current of the system, an open load switch  $S_{OLD}$  is recommended.  $R_D$  represents the minimum parasitic resistance at the output pin. In case  $R_D$  is not considered the device integrates a 500 kΩ  $R_{PD}$  resistance.

The value of external resistance  $R_{OLD}$  is decided based on the minimum power supply voltage ( $V_{BB}$ ), parasitic resistance  $R_{PD}$  and open detection threshold  $V_{DSOL}$ . The equation for calculating the  $R_{OLD}$  value is shown below.

$$R_{OLD} < \frac{R_D \times R_{PD}}{R_D + R_{PD}} \times \left( \frac{V_{DSOL}}{V_{BB(min)} - V_{DSOL}} \right)$$

Moreover, in case a high ohmic open load can be considered, an integrated 100 μA  $I_{OLD}$  pull up current could help detect an open load at off without the need for any external components.

Open Load Masking Time

The IC diagnoses open load detection after the mask time  $t_{OLDMSK}$  after the IN pin is de-asserted to allow for the output voltage to drop while in normal operation (load connected).

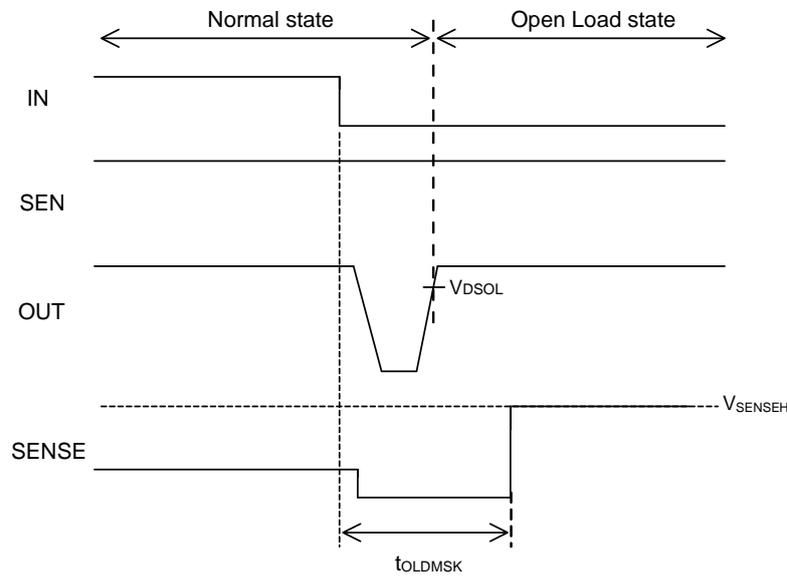


Figure 70. Open Load Masking Timing Chart

Diagnostic Timings

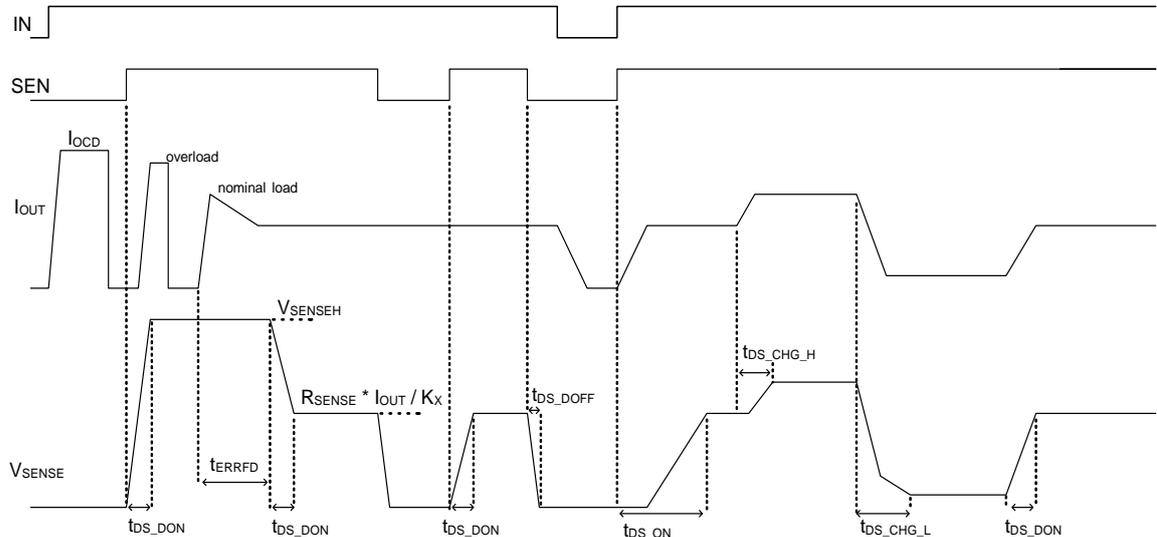


Figure 71. Diagnostics Timing Diagram

Application Circuit Example

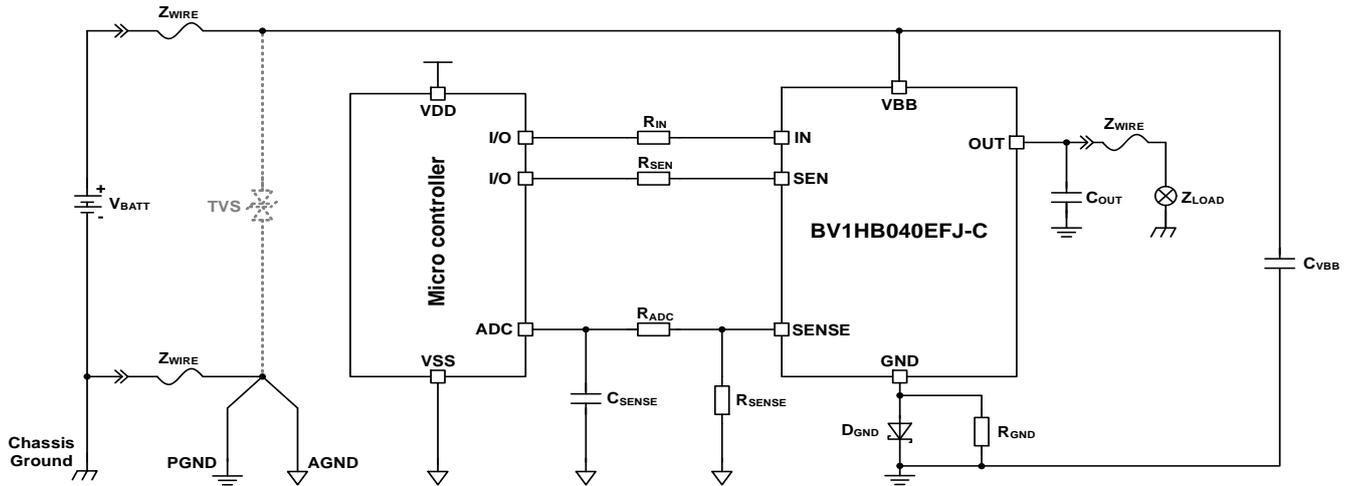


Figure 72. Application Schematic

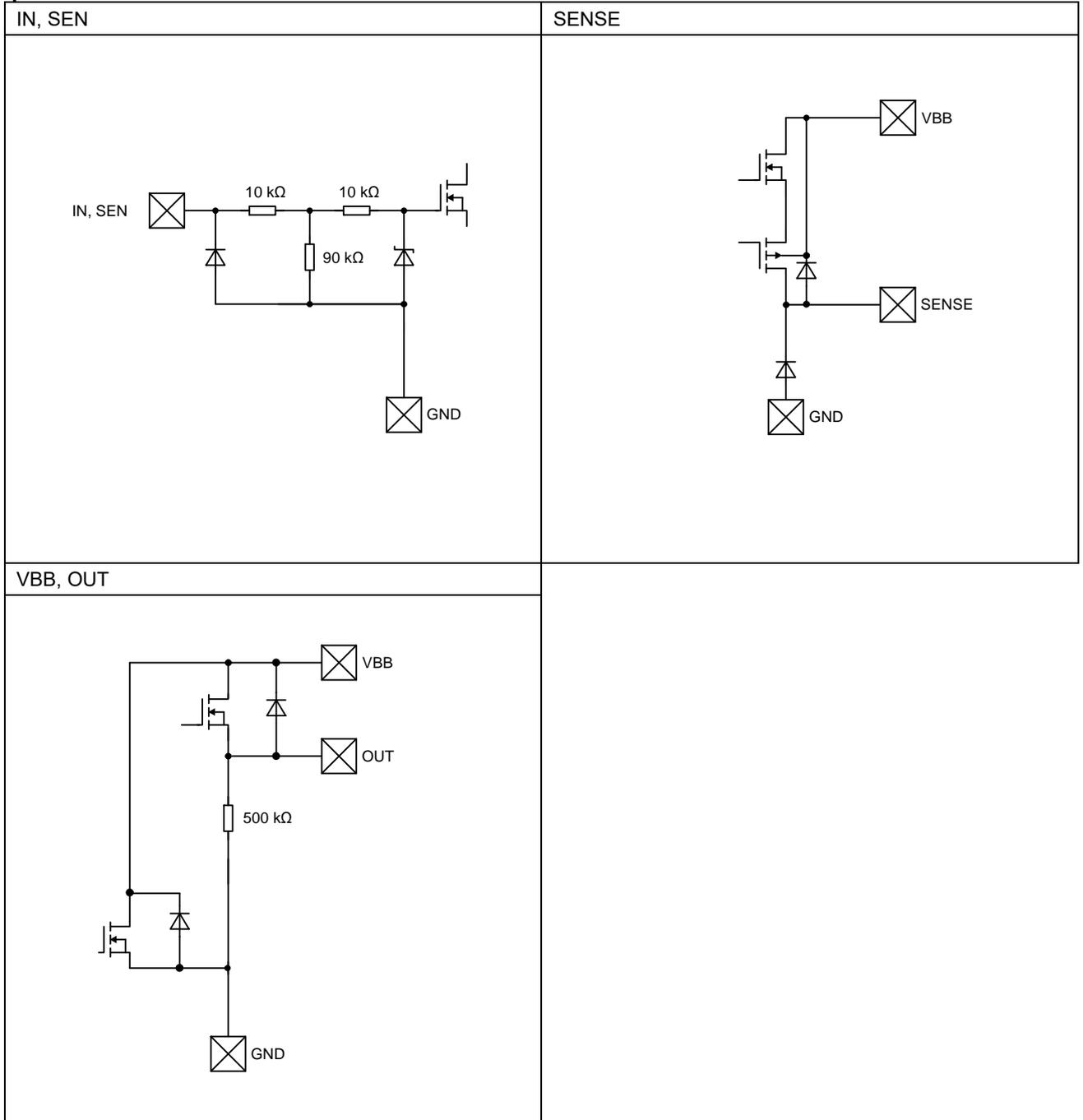
Recommended External Components Example

Item	Symbol	Standard Value			Unit	
		MIN	TYP	MAX		
Input Pin Resistance	$R_{IN}$	4.7	-	-	k $\Omega$	
Diagnostic Input Pin Resistance	$R_{SEN}$	4.7	-	-	k $\Omega$	
Microcontroller SENSE Pin Resistance	$R_{ADC}$	4.7	-	-	k $\Omega$	
SENSE Pin Resistance	$R_{SENSE}$	-	1	-	k $\Omega$	
SENSE Filter Capacitance	$C_{SENSE}$	-	100	-	pF	
Output EMC Capacitance	$C_{OUT}$	-	10	-	nF	
Battery Line Filter Capacitance	$C_{VBB}$	100	-	-	nF	
Chip Ground Protection Impedance Network <sup>(Note 1)</sup>	$R_{GND}$	-	4.7	-	k $\Omega$	
	$D_{GND}$	$V_F$ <sup>(Note 2)</sup>	-	0.3	-	V
		$V_R$	40	-	-	V
Transient Voltage Suppressor Diode	TVS	-	36	-	V	

(Note 1)  $R_{GND}$  in parallel with the Ground protection diode is optional.  $R_{GND}$  is needed in case of loss of  $V_{BB}$  with wire harness inductivity or inductive load.  $V_F$  of  $D_{GND}$  is forward bias voltage,  $V_R$  of  $D_{GND}$  is reverse bias voltage.

(Note 2)  $V_F$  depends on forward current of  $D_{GND}$ . When decide forward current value, please refer to Operating Mode Current ( $I_{GNDH}$ ) of the "Electrical Characteristics" section.

I/O Equivalence Circuits



## Operational Notes

### 1. Recommended Operating Conditions

The IC is designed to operate in 12 V automotive boar net applications. The functions and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions specified by the electrical characteristics. The IC can withstand transient voltages beyond the recommended operating conditions; however, parameter deviations are possible when used outside of the supply nominal voltage range. Exposure to the absolute maximum ratings may cause permanent damage to the IC.

### 2. Inrush Current

When a load is being activated by the IC inrush currents may flow. The IC is designed to drive high inrush current loads; however, careful consideration must be completed when pairing the IC with the load. In case special recommendations are not available in the Datasheet the minimum overcurrent protection level of the IC should be higher than the maximum expected inrush current for proper load driving.

### 3. Testing on Application Boards

When testing the IC on an application board, it is recommended to always discharge capacitors completely after each evaluation step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 4. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 5. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

### 6. Thermal Shutdown Function (TSD)

This IC has a built-in thermal shutdown function that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD function that will turn OFF power output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD function operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD function be used in a set design or for any purpose other than protecting the IC from heat damage.

### 7. Over Current Protection Function (OCP)

This IC integrates an overcurrent limitation protection function that is activated when the load is shorted towards ground. This protection function is effective in preventing damage due to sudden and unexpected fault events. However, the IC should not be used in applications characterized by continuous operation of the protection function.

### 8. Active Clamp Operation

The IC integrates the active clamp function to internally absorb the reverse energy  $E_L$  which is generated when the inductive load is turned off. When the active clamp operates, the thermal shutdown function does not work. Decide a load so that the reverse energy  $E_L$  is active clamp energy (Single Pulse)  $E_{AS}$  (refer to Figure 4. Active Clamp Energy vs Output Current) or under when inductive load is used.

### 9. Reverse Battery Connection

Connecting the power supply i.e., the battery with a reversed polarity can damage the IC. Precautions must be taken against reverse polarity when connecting the power supply, such as mounting an external diode between the battery feed and the IC's power supply, blocking all current paths. Alternatively, inserting a blocking diode or resistance in series with the IC's GND pin will prevent or limit the current from flowing into the control circuits of the high side switch respectively. However, current thorough the body diode of the integrated power FET must be limited by the resistive component of the load. The current through the Digital inputs and SENSE pins must be limited too with protection resistors.

### 10. Power Supply and PCB Layout

Design the PCB layout in order to provide sufficient cooling to the IC. Connect the exposed pad with sufficient thermal vias to power supply copper plane to dissipate as much as possible thermal energy to the environment. Furthermore, connect as close as possible to the IC a capacitor between power supply and ground pins. Minimize the input capacitance of the digital input pins by placing the protection resistors as close as possible to the IC. Place the ground network as close as possible to the IC. Place the sense pin resistance as close as possible to the IC and the R-C filtering network close to the microcontroller. Place the output capacitors as close as possible to the IC. Short all output pins of the respective channel on the PCB to ensure equal current distribution. It is usually recommended to use a PCB with an internal copper layer as a power supply plane and another internal copper layer as a ground plane for thermal and EMC considerations respectively.

**Operational Note – continued****11. Ground Shift and Ground Wiring Pattern**

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. The IC is robust against small ground shift, however, ensure that the ground traces of external components do not cause big variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance. Big ground shifts could cause additional switching losses and electromagnetic emissions.

**12. Reverse Current**

A capacitive or inductive type of load can cause the output of the IC to rise above the input power supply level. The IC is designed to accept reverse current and normal operation is maintained as long as the reverse current is below the specified levels. Therefore, give special consideration to the maximum amount of reverse current that can flow through the device.

**13. Undervoltage or Loss of Battery**

The IC is designed to automatically switch off in case of loss of battery/power supply or undervoltage events. The IC will restart once the battery exceeds the specified operation threshold. In case the load is inductive a resistor on the ground network is recommended if loss of battery is foreseen at the same time in the application.

**14. Loss of Ground**

The IC cannot operate without the appropriate ground connection; nonetheless, the IC will automatically switch off in case of loss of ground. However, careful consideration of the external state of the inputs must be considered in order to avoid creating parasitic paths to another ground in the application via the external circuitry.

**15. Load Dump and Overvoltage Protection**

The IC is designed with integrated overvoltage protection to safeguard its internal circuits. For the overvoltage protection to work a ground resistance  $R_{GND}$  is necessary. Furthermore, input pins' protection resistors are mandatory. In case of Load dump external TVS protection diodes must be connected to safeguard the system.

**16. Open Load or Short to Battery**

An open load event is not considered dangerous to the IC; moreover, the IC can detect such failure and signal the fault to the microcontroller. In case a short to battery is present the load is turned on independent of the state of the IC. The device can be used to detect such a failure and signal the fault to the microcontroller.

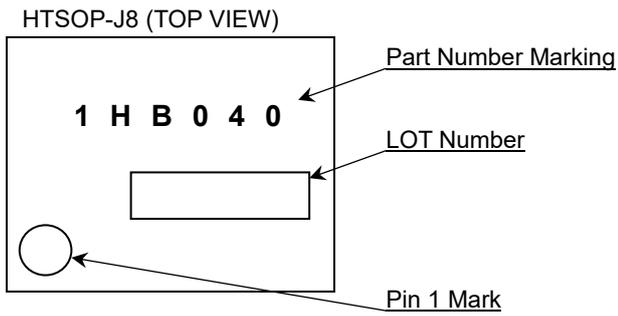
**17. Internally Not Connected (N.C.) Pins**

Pins that are specified as internally not connected have no physical connection to the IC. For mechanical reasons it is recommended to solder them on the PCB. Electrically they can remain not connected in the circuit or may be connected to different signals especially when using high current outputs.

Ordering Information

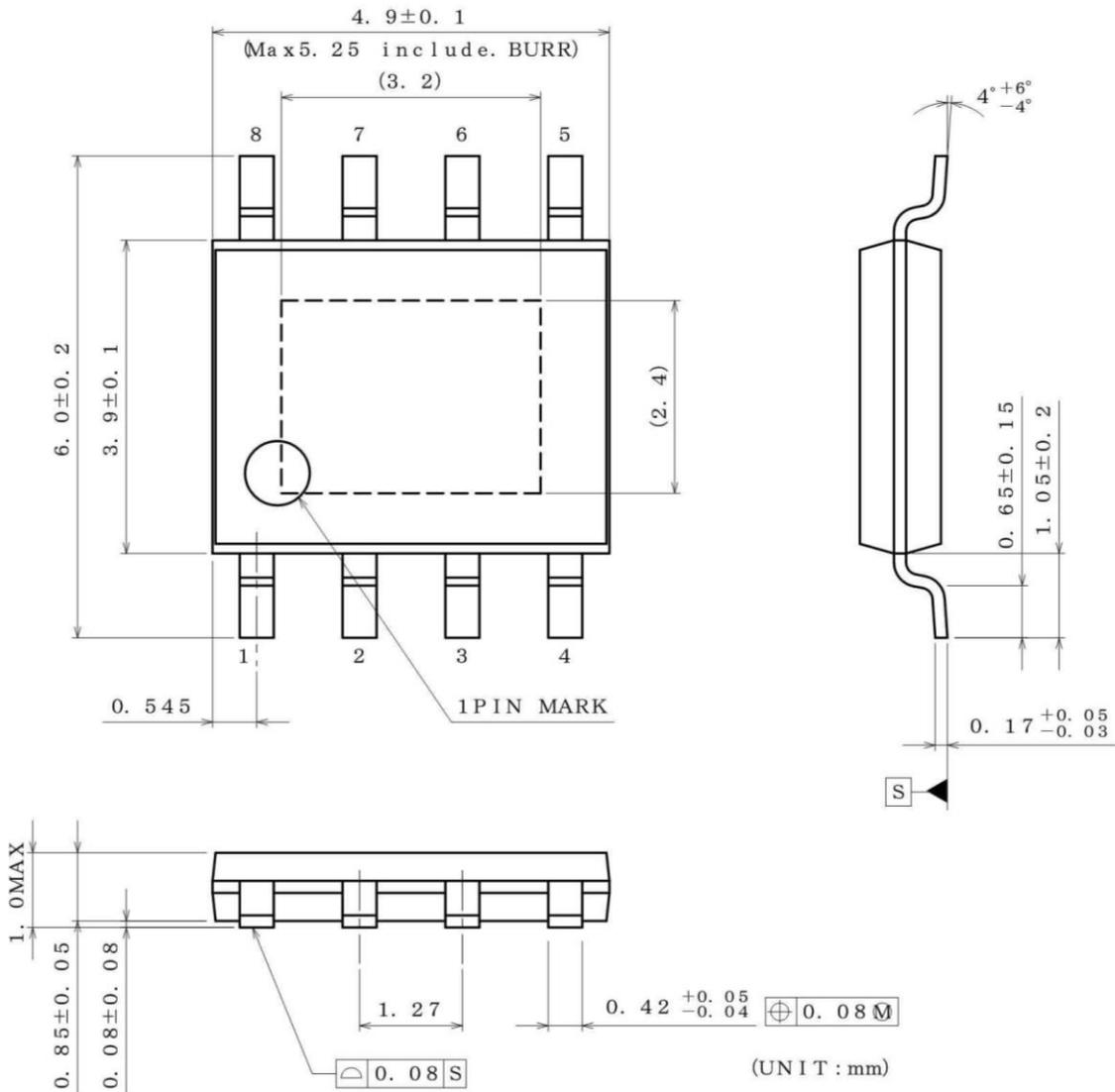


Marking Diagram



Physical Dimension and Packaging Information

Package Name	HTSOP-J8
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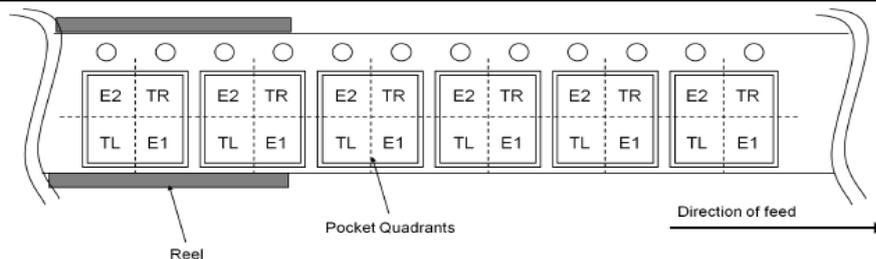
(UNIT : mm)

PKG : HTSOP-J8

Drawing No. EX169-5002-2

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



**Revision History**

Date	Ver.	Contents
20.Sep.2023	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
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  - [d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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