Datasheet

Gate Driver Providing Galvanic Isolation Series

Isolation Voltage 3750 Vrms
1ch Gate Driver Providing Galvanic Isolation

BM60068FU-C

General Description

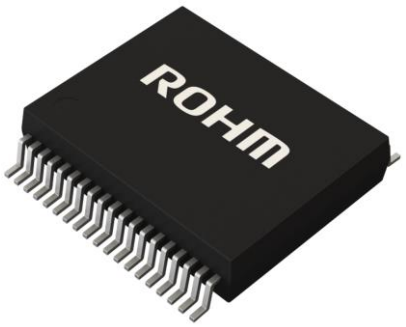
BM60068FU-C is a gate driver with isolation voltage of 3750 Vrms, I/O delay time of 150 ns, and have functions such as fault signal output function, ready signal output function, Under Voltage Lock Out (UVLO) function, Over Voltage Lock Out (OVLO) function, Short Circuit Protection (SCP) function, active miller clamping function, output state feedback function and Built In Self Test (BIST) function.

Key Specifications

- Isolation Voltage: 3750 Vrms
- Maximum Gate Drive Voltage: 20 V
- I/O Delay Time: 150 ns (Max)
- Minimum Input Pulse Width: 90 ns (Max)

Package

	W (Typ) x D (Typ) x H (Max)
SSOP-C38W	10.0 mm x 10.4 mm x 2.4 mm



Features

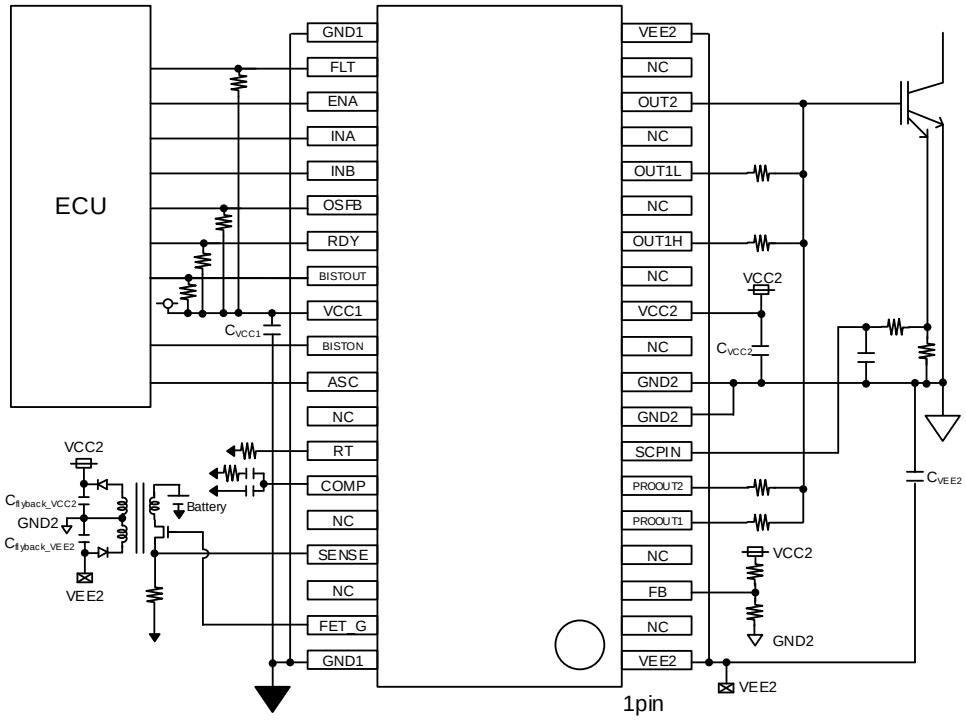
- AEC-Q100 Qualified *(Note 1)*
- Fault Signal Output Function
- Ready Signal Output Function
- Under Voltage Lock Out Function
- Over Voltage Lock Out Function
- Short Circuit Protection Function
- Active Miller Clamping Function
- Output State Feedback Function
- Built in Self Test Function
- Designed for UL1577

(Note 1) Grade1

Applications

- Automotive Inverter
- Automotive DC-DC Converter

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

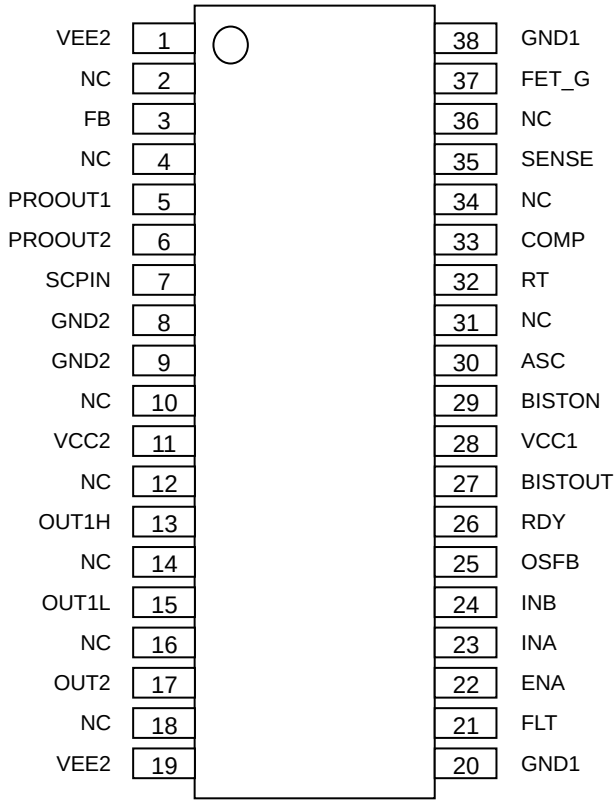
Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
RT	R_{RT}	24	-	150	kΩ
SENSE	R_{SENSE}	34	68	136	mΩ
VCC1	C_{VCC1}	0.1	-	-	µF
VCC2	C_{VCC2}	0.2	-	-	µF
VCC2	$C_{flyback\_VCC2}$	10	-	-	µF
VEE2	C_{VEE2}	0.2	-	-	µF
VEE2	$C_{flyback\_VEE2}$	10	-	-	µF

Caution:
Recommended Value of R_{SENSE} is set for stable operation, considering Phase Compensation.
Confirm separately that start up operation have finished within Soft Start Time, t_{SS}.
In case using switching controller, select the value of $C_{flyback\_VCC2}$ and $C_{flyback\_VEE2}$ properly, considering voltage ripple.

Pin Configuration

(TOP VIEW)

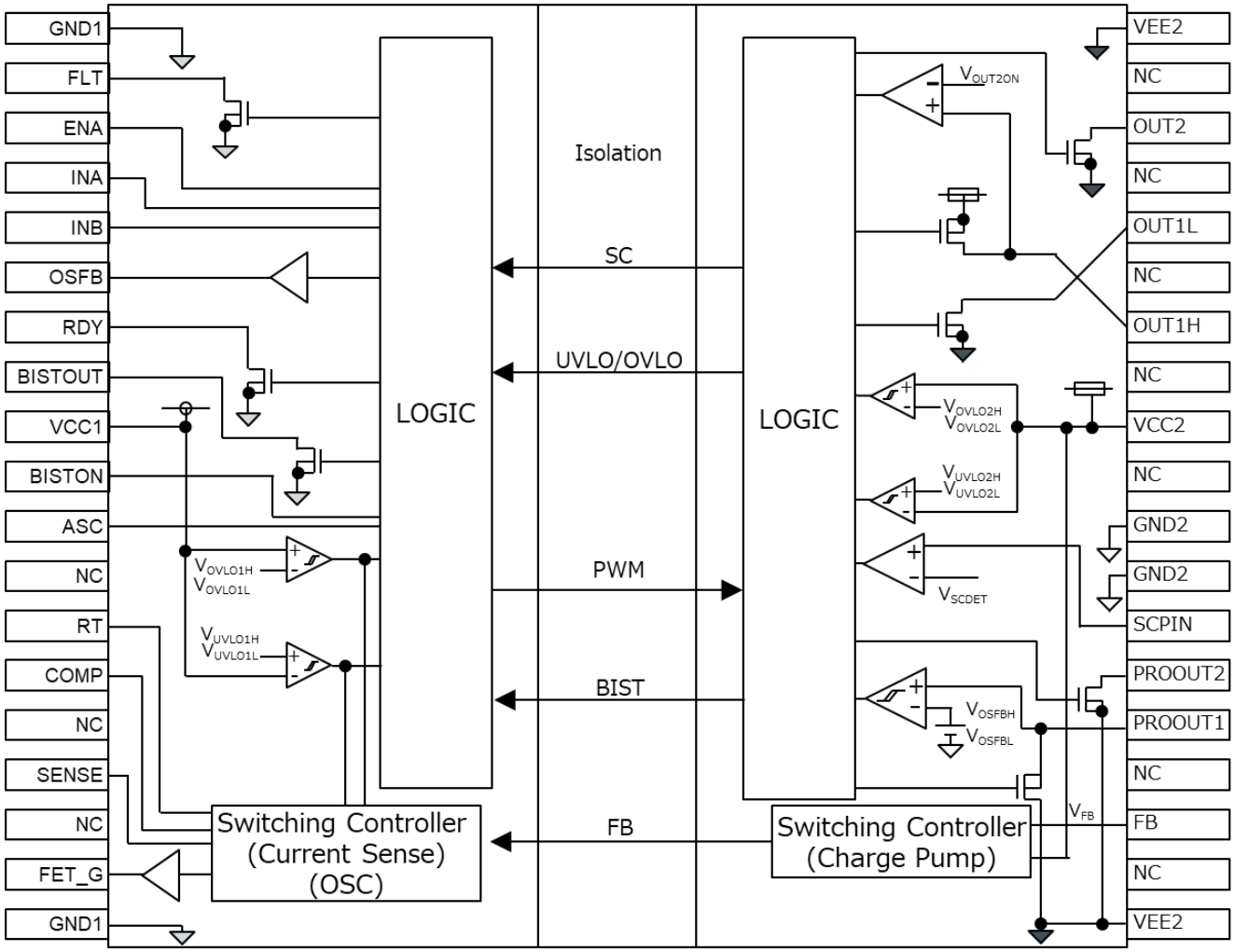


Pin Description

No.	Pin Name	Function	No.	Pin Name	Function
1	VEE2	Output side negative power supply	20	GND1	Input side ground
2	NC	No connection*(Note 2)*	21	FLT	Fault output
3	FB	Output side voltage feedback	22	ENA	Gate drive control enable input
4	NC	No connection	23	INA	Gate drive control input A
5	PROOUT1	Soft turn off output 1 / Gate voltage monitor	24	INB	Gate drive control input B
6	PROOUT2	Soft turn off output 2	25	OSFB	Output state feedback
7	SCPIN	Short circuit current detection input	26	RDY	Ready output
8	GND2	Output side ground	27	BISTOUT	BIST result output
9	GND2	Output side ground	28	VCC1	Input side power supply
10	NC	No connection	29	BISTON	Input for checking BIST result
11	VCC2	Output side positive power supply	30	ASC	Active Short Circuit input
12	NC	No connection	31	NC	Non connection
13	OUT1H	Source side output	32	RT	Switching frequency setting
14	NC	No connection	33	COMP	Charge Pump output
15	OUT1L	Sink side output	34	NC	No connection
16	NC	No connection	35	SENSE	Current Sense input
17	OUT2	Active Miller Clamping output	36	NC	No connection
18	NC	No connection	37	FET_G	Output for control external MOSFET driving trans
19	VEE2	Output side negative power supply	38	GND1	Input side ground

(Note 2) Use with No Connection pins are open.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input side Supply Voltage	V_{CC1MAX}	-0.3 to V_{GND1}+7.0	V
Output side Positive Supply Voltage	V_{CC2MAX}	V_{EE2}-0.3 to V_{GND2}+24.0	V
Output side Negative Supply Voltage	V_{EE2MAX}	-15.0 to V_{GND2}+0.3	V
Maximum Difference between Output side Positive and Negative Supply Voltages	V_{MAX1}	30.0	V
INA, INB, ENA, ASC, BISTON COMP, SENSE, RT, FLT, RDY, OSFB BISTOUT, FET_G Pin Input Voltage	V_{INMAX}	-0.3 to V_{CC1}	V
FLT, RDY, BISTOUT, OSFB Pin Output Current	I_{OUTMAX}	10	mA
SCPIN Pin Input Voltage	$V_{SCPINMAX}$	V_{EE2}-0.3 to V_{CC2}+0.3	V
FB Pin Input Voltage	$V_{FBINMAX}$	V_{GND2}-0.3 to V_{CC2}+0.3	V
OUT1H, OUT1L Pin Voltage	V_{OUT1H}, V_{OUT1L}	V_{EE2}-0.3 to V_{CC2}+0.3	V
OUT2 Pin Voltage	V_{OUT2}	V_{EE2}-0.3 to V_{CC2}+0.3	V
PROOUT1 Pin Voltage	$V_{PROOUT1}$	V_{EE2}-0.3 to V_{CC2}+0.3	V
PROOUT2 Pin Voltage	$V_{PROOUT2}$	V_{EE2}-0.3 to V_{CC2}+0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
SSOP-C38W				
Junction to Ambient	θ_{JA}	81.3	48.7	°C/W
Junction to Top Characterization Parameter*(Note 4)*	Ψ_{JT}	28	22	°C/W

(Note 3) Based on JESD51-2A(Still-Air)
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.
(Note 6) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input side Supply Voltage	V_{CC1}*(Note 7)*	4.5	5.5	V
Output side Positive Supply Voltage	V_{CC2}*(Note 8)*	14	20	V
Output side Negative Supply Voltage	V_{EE2}*(Note 8)*	-12	0	V
Maximum Difference between Output side Positive and Negative Supply Voltages	V_{MAX2}	-	28	V
Switching Frequency	f_{SW}	100	500	kHz
Operating Temperature	Topr	-40	+125	°C

(Note 7) Relative to GND1
(Note 8) Relative to GND2

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO} = 500 V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1 min	V_{ISO}	3750	Vrms
Insulation Test Voltage / 1 s	V_{ISO}	4500	Vrms

Electrical Characteristics

(Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC1} = 4.5 V to 5.5 V, V_{CC2} = 14 V to 20 V, V_{EE2} = -12 V to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input side Circuit Current 1	I_{CC11}	-	2.0	4.0	mA	OUT1L = L
Input side Circuit Current 2	I_{CC12}	-	2.0	4.0	mA	OUT1H = H
Input side Circuit Current 3	I_{CC13}	-	2.05	4.10	mA	INA = 10 kHz, Duty = 50 %
Input side Circuit Current 4	I_{CC14}	-	2.1	4.2	mA	INA = 20 kHz, Duty = 50 %
Output side Circuit Current	I_{CC2}	-	3.7	6.3	mA	
Logic Block						
Logic High Level Input Voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB, ENA, BISTON, ASC
Logic Low Level Input Voltage	V_{INL}	0	-	0.8	V	INA, INB, ENA, BISTON, ASC
Logic Pull-down Resistance	R_{IND}	25	50	100	kΩ	INA, ENA, BISTON, ASC
Logic Pull-up Resistance	R_{INU}	25	50	100	kΩ	INB
Logic Input Filtering Time	t_{INFIL}	30	-	90	ns	INA, INB, ENA, ASC
Output						
OUT1H ON Resistance	R_{OUT1H}	0.20	0.45	1.01	Ω	I_{OUT1H} = -40 mA
OUT1L ON Resistance	R_{OUT1L}	0.13	0.30	0.67	Ω	I_{OUT1L} = 40 mA
OUT1H, OUT1L Maximum Current	$I_{OUT1MAX}$	6	-	-	A	V_{CC2} = 15 V Guaranteed by design
PROOUT1 ON Resistance	R_{PRO1}	0.16	0.37	0.83	Ω	$I_{PROOUT1}$ = 40 mA
PROOUT1 Maximum Current	$I_{PRO1MAX}$	3	-	-	A	V_{CC2} = 15 V Guaranteed by design
PROOUT2 ON Resistance	R_{PRO2}	0.15	0.33	0.75	Ω	$I_{PROOUT2}$ = 40 mA Guaranteed by design
PROOUT2 Maximum Current	$I_{PRO2MAX}$	5	-	-	A	V_{CC2} = 15 V Guaranteed by design
Turn ON Time	t_{ON}	40	90	150	ns	INA/INB/ASC
Turn OFF Time	t_{OFF}	40	90	150	ns	INA/INB/ASC
Propagation Distortion	t_{PDIST}	-30	0	+30	ns	t_{OFF} - t_{ON}
Rise Time	t_{RISE}	-	30	-	ns	Load = 10 nF Guaranteed by design
Fall Time	t_{FALL}	-	30	-	ns	Load = 10 nF Guaranteed by design

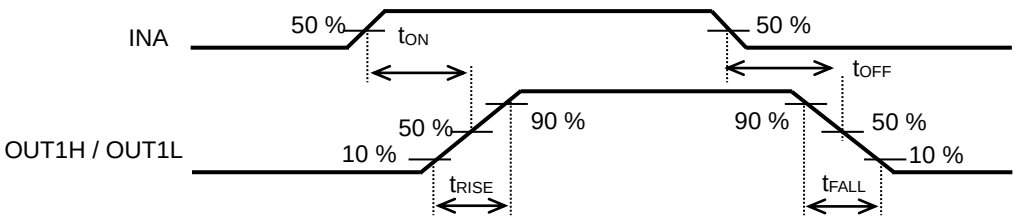


Figure 1. INA - OUT1H / OUT1L Timing Chart in Gate Drive

Electrical Characteristics - continued
(Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC1} = 4.5 V to 5.5 V, V_{CC2} = 14 V to 20 V, V_{EE2} = -12 V to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
OUT2 ON Resistance	R_{OUT2L}	0.12	0.27	0.61	Ω	I_{OUT2} = 40 mA
OUT2 Maximum Current	$I_{OUT2MAX}$	5	-	-	A	Guaranteed by design
OUT2 ON Threshold Voltage	V_{OUT2ON}	1.8	2.0	2.2	V	Relative to GND2
OUT2 Output Delay Time	t_{OUT2ON}	-	50	195	ns	
Common Mode Transient Immunity	CMTI	100	-	-	kV/μs	Guaranteed by design
Protection Functions						
Input side UVLO OFF Voltage	V_{UVLO1H}	4.05	4.25	4.45	V	
Input side UVLO ON Voltage	V_{UVLO1L}	3.95	4.15	4.35	V	
Input side UVLO Filtering Time	$t_{UVLO1FIL}$	4	10	45	μs	
Input side UVLO Delay Time (OUT1H, OUT1L)	$t_{UVLO1OUT1}$	4	-	46	μs	
Input side UVLO Delay Time (RDY)	$t_{UVLO1RDY}$	4	-	46	μs	
Input side OVLO ON Voltage	V_{OVLO1H}	6.1	6.5	6.9	V	
Input side OVLO OFF Voltage	V_{OVLO1L}	6.0	6.4	6.8	V	
Input side OVLO Filtering Time	$t_{OVLO1FIL}$	4.5	10	25	μs	
Input side OVLO Delay Time (OUT1H, OUT1L)	$t_{OVLO1OUT1}$	4.5	-	26	μs	
Input side OVLO Delay Time (RDY)	$t_{OVLO1RDY}$	4.5	-	26	μs	
Output side UVLO OFF Voltage	V_{UVLO2H}	11.9	12.5	13.1	V	Relative to GND2
Output side UVLO ON Voltage	V_{UVLO2L}	10.9	11.5	12.1	V	Relative to GND2
Output side UVLO Filtering Time	$t_{UVLO2FIL}$	5	10	19	μs	
Output side UVLO Delay Time (OUT1H, OUT1L)	$t_{UVLO2OUT1}$	5	10	20	μs	
Output side UVLO Delay Time (RDY)	$t_{UVLO2RDY}$	6	-	55	μs	
Output side OVLO ON Voltage	V_{OVLO2H}	21.2	22.5	23.8	V	Relative to GND2
Output side OVLO OFF Voltage	V_{OVLO2L}	20.2	21.5	22.8	V	Relative to GND2
Output side OVLO Filtering Time	$t_{OVLO2FIL}$	5	10	19	μs	
Output side OVLO Delay Time (OUT1H, OUT1L)	$t_{OVLO2OUT1}$	5	10	20	μs	
Output side OVLO Delay Time (RDY)	$t_{OVLO2RDY}$	6	-	55	μs	
RDY Output ON Resistance	R_{RDYL}	-	30	80	Ω	I_{RDY} = 5 mA
FLT Output ON Resistance	R_{FLTL}	-	30	80	Ω	I_{FLT} = 5 mA

Electrical Characteristics - continued

(Unless otherwise specified, Ta = -40 °C to +125 °C, V_{CC1} = 4.5 V to 5.5 V, V_{CC2} = 14 V to 20 V, V_{EE2} = -12 V to 0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Protection Functions						
SCPIN Input Voltage	V_{SCPIN}	-	0.10	0.22	V	I_{SCPIN} = 1 mA OUT1L = L Relative to GND2
SCPIN Output Current	I_{SCPIN}	0.5	1.0	1.5	µA	
SCPIN Leading Edge Blanking Time	$t_{SCPINLEB}$	0.10	0.20	0.30	µs	Guaranteed by Design
Short Circuit Detection Voltage	V_{SCDET}	0.67	0.70	0.73	V	Relative to GND2
Short Circuit Detection Filtering Time	t_{SCPFIL}	0.05	0.15	0.30	µs	
Short Circuit Detection Delay Time (PROOUT1, PROOUT2)	t_{SCPPRO}	0.10	0.25	0.50	µs	
Short Circuit Detection Delay Time (FLT)	t_{SCPFLT}	0.05	0.35	0.75	µs	
PROOUT2 ON Time	t_{PRO2ON}	100	160	220	ns	
PROOUT1 H Detection Voltage	V_{OSFBH}	-	5.0	-	V	Relative to GND2
PROOUT1 L Detection Voltage	V_{OSFBL}	-	4.5	-	V	Relative to GND2
OSFB ON Resistance (Source-side)	R_{OSFBH}	-	60	160	Ω	I_{OSFB} = -5 mA
OSFB ON Resistance (Sink-side)	R_{OSFBL}	-	60	160	Ω	I_{OSFB} = 5 mA
OSFB Output Delay Time H	t_{OSFBH}	0.10	0.33	0.50	µs	PROOUT1 Minimum Input Pulse Width = 0.5 µs
OSFB Output Delay Time L	t_{OSFBL}	0.05	0.20	0.40	µs	
OC BIST Time	t_{BISTOC}	-	-	150	µs	
BIST Time	$t_{BISTSTRDY}$	-	-	150	µs	
BIST OFF Time	$t_{RDYBISTOFF}$	-	-	250	µs	
BISTOUT Delay Time	$t_{BISTONOUT}$	-	-	1	µs	
BISTOUT Output ON Resistance	$R_{BISTOUTL}$	-	30	80	Ω	$I_{BISTOUT}$ = 5 mA
Switching Controller						
Switching Frequency	f_{SW}	f_{SW_EQ} x 0.87	f_{SW_EQ} *(Note 9)*	f_{SW_EQ} x 1.18	kHz	R_{RT} = 24 kΩ to 100 kΩ
Soft Start Time	t_{SS}	9.4	12.5	15.6	ms	
FB Output Voltage	V_{FB}	1.47	1.50	1.53	V	Relative to GND2
FB Input Current	I_{FB}	-0.8	0	+0.8	µA	
FET_G ON Resistance (Source Side)	R_{ONGH}	-	-	12	Ω	Source Current = 10 mA
FET_G ON Resistance (Sink Side)	R_{ONGL}	-	-	1.3	Ω	Sink Current = 10 mA
COMP Output Sink Current	$I_{COMPSINK}$	-15	-10	-5	µA	
COMP Output Source Current	$I_{COMPSOURCE}$	5	10	15	µA	
SENSE Over Current Detection Voltage	$V_{SENSEOC}$	170	200	230	mV	
Maximum ON Duty	D_{ONMAX}	75	85	95	%	
Protection Holding Time	$t_{DCDCHOLD}$	20	40	60	ms	
SENSE Over Current Detection Time	$t_{SENSEOCDET}$	0.1	-	0.5	µs	Guaranteed by design Rise Slew Rate of the SENSE pin = 0.127 V/µs

(Note 9) In detail about f_{SW_EQ}, refer P26.

Typical Performance Curves

(Reference data)

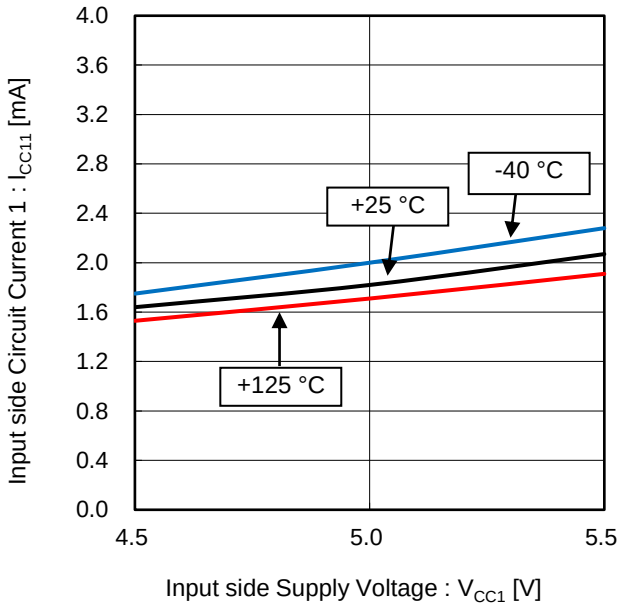


Figure 2. Input side Circuit Current 1 vs Input side Supply Voltage

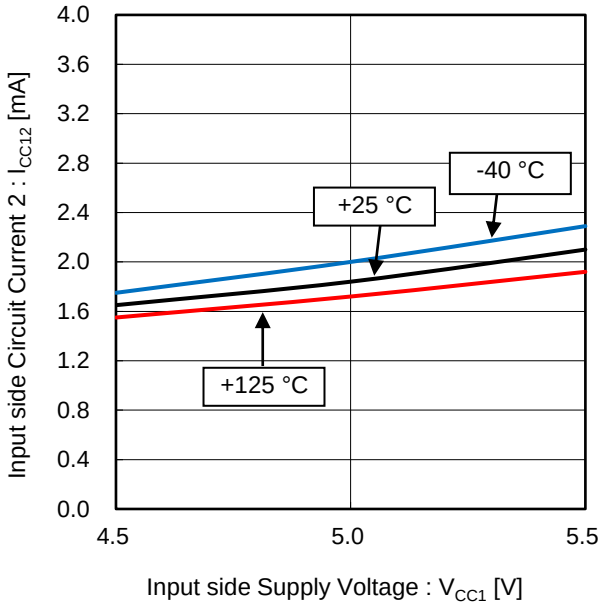


Figure 3. Input side Circuit Current 2 vs Input side Supply Voltage

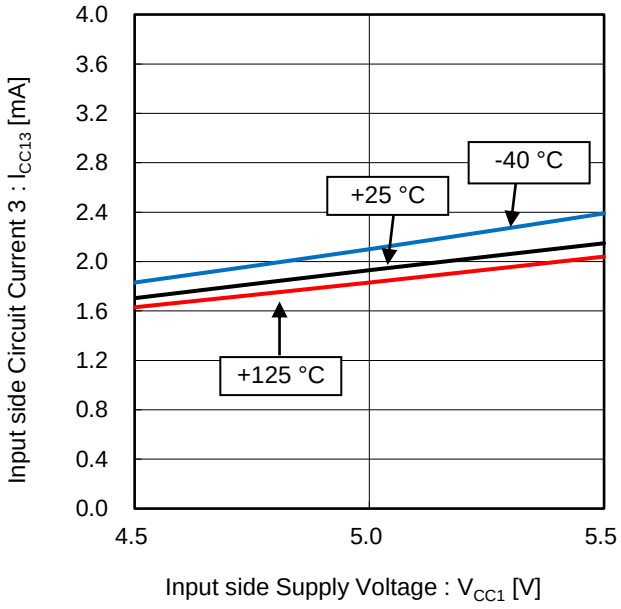


Figure 4. Input side Circuit Current 3 vs Input side Supply Voltage

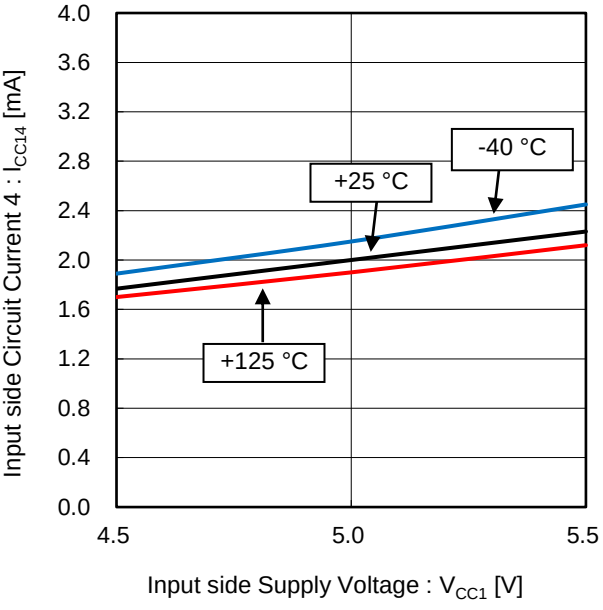


Figure 5. Input side Circuit Current 4 vs Input side Supply Voltage

Typical Performance Curves – continued
(Reference data)

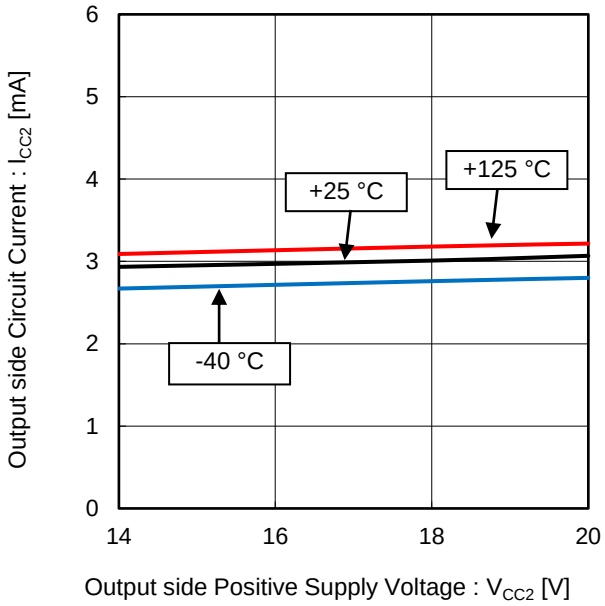


Figure 6. Output side Circuit Current vs Output side Positive Supply Voltage

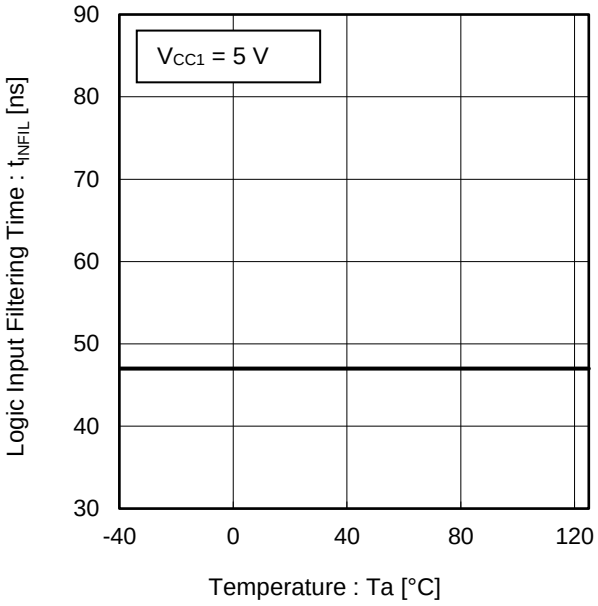


Figure 7. Logic Input Filtering Time vs Temperature

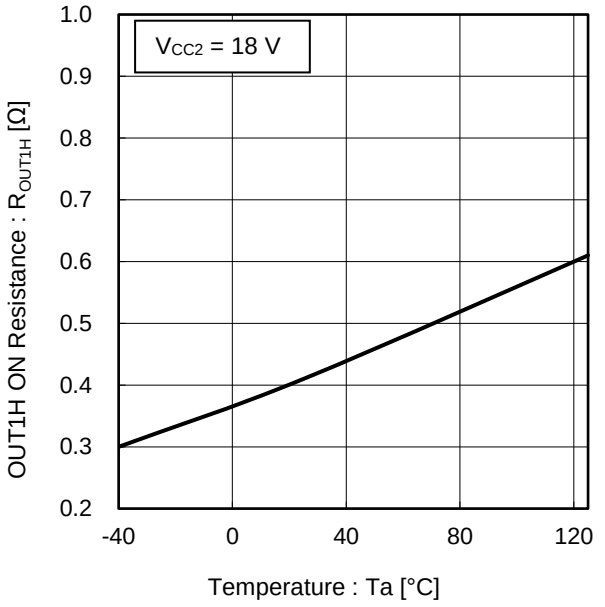


Figure 8. OUT1H ON Resistance vs Temperature

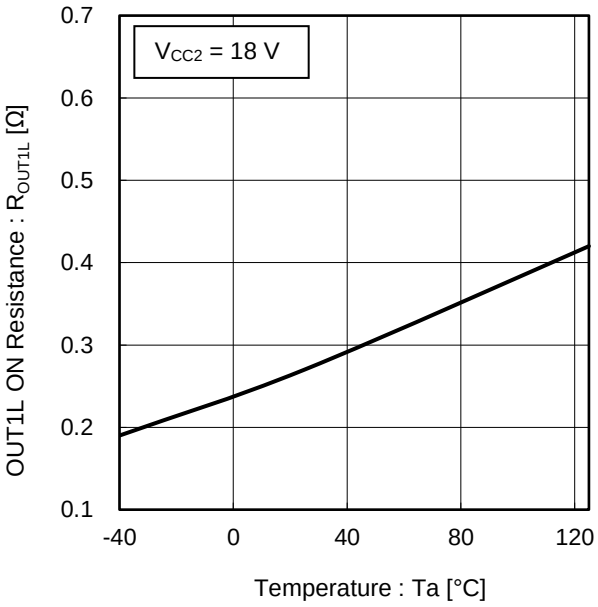


Figure 9. OUT1L ON Resistance vs Temperature

Typical Performance Curves – continued
(Reference data)

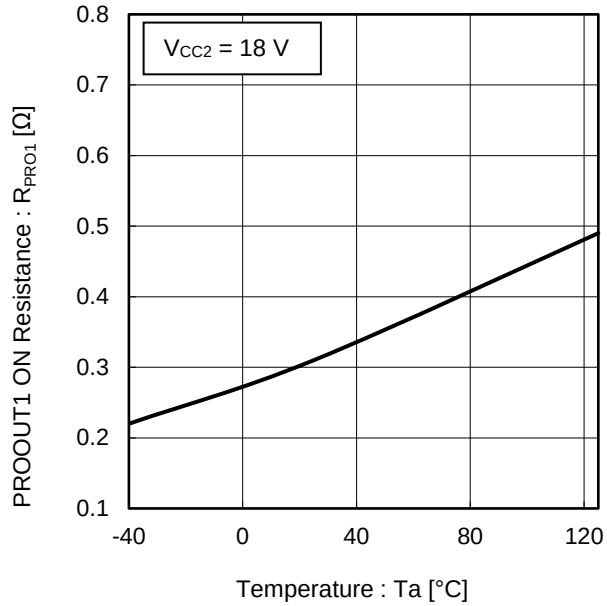


Figure 10. PROOUT1 ON Resistance vs Temperature

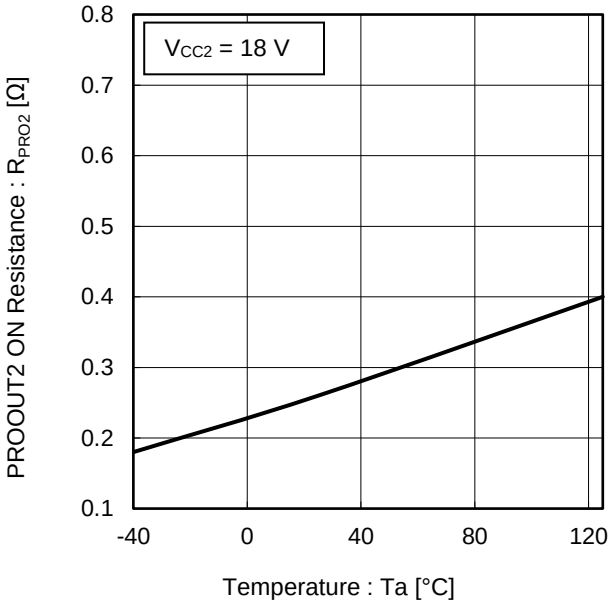


Figure 11. PROOUT2 ON Resistance vs Temperature

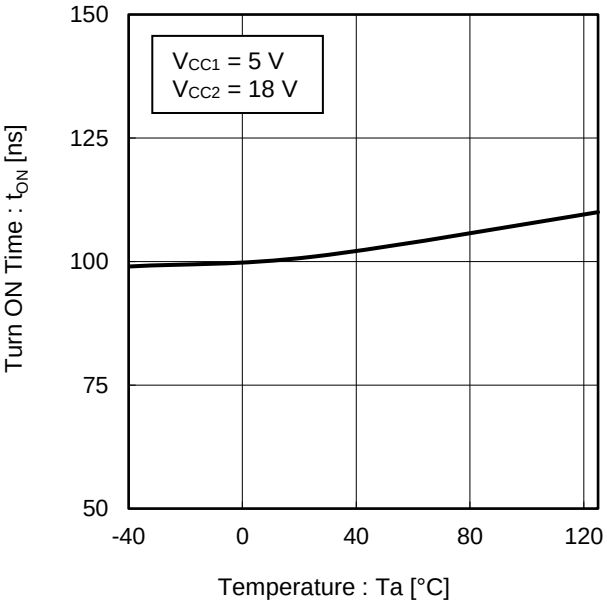


Figure 12. Turn ON Time vs Temperature

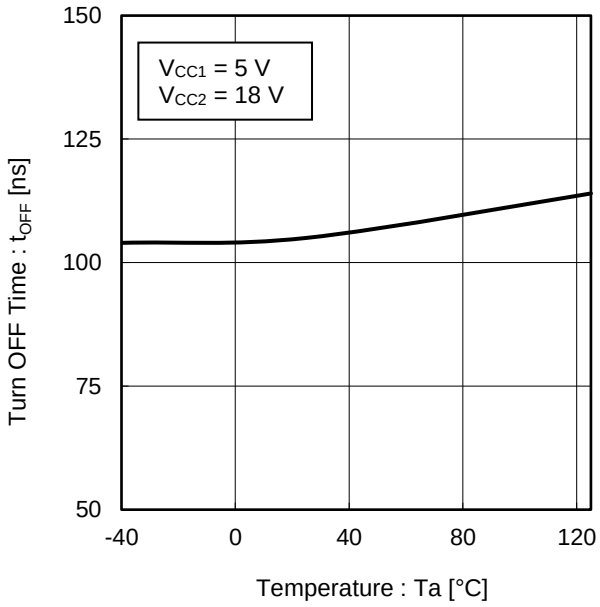


Figure 13. Turn OFF Time vs Temperature

Typical Performance Curves – continued
(Reference data)

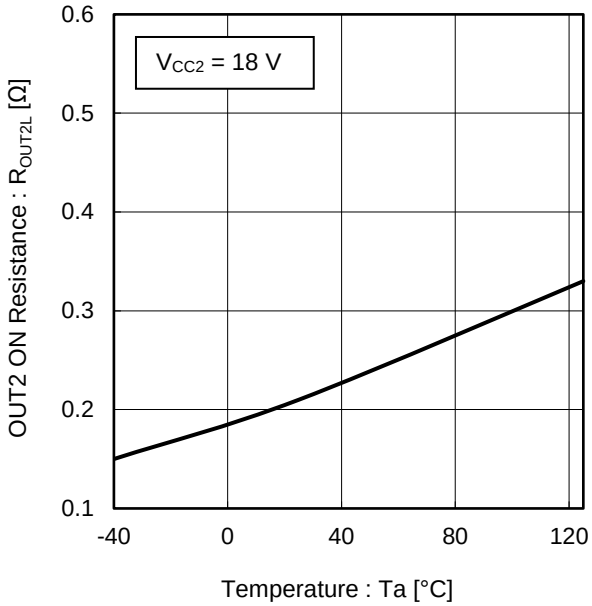


Figure 14. OUT2 ON Resistance vs Temperature

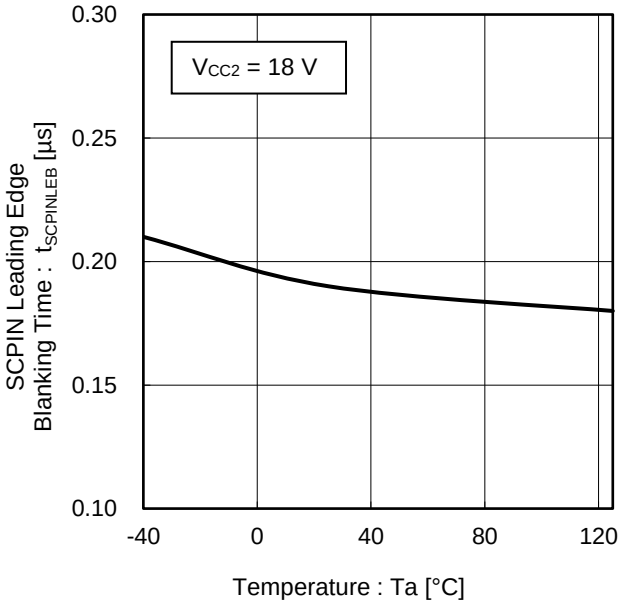


Figure 15. SCPIN Leading Edge Blanking Time vs Temperature

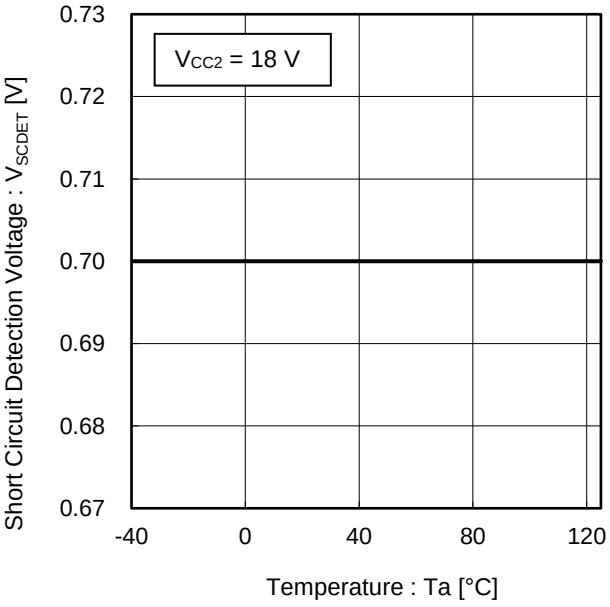


Figure 16. Short Circuit Detection Voltage vs Temperature

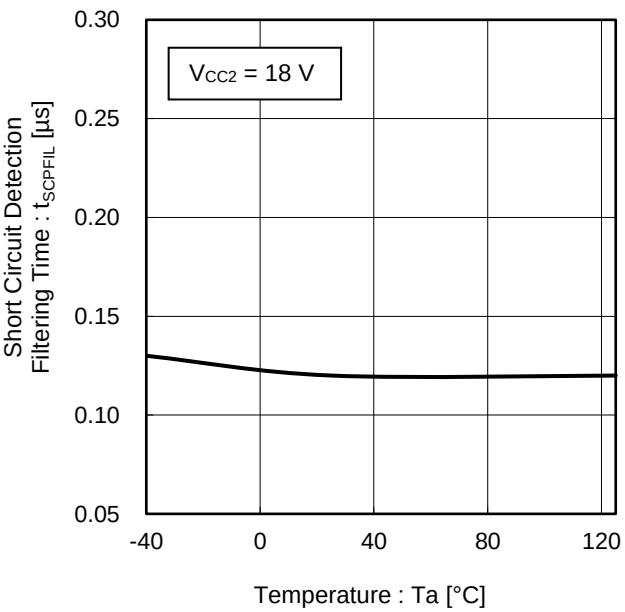


Figure 17. Short Circuit Detection Filtering Time vs Temperature

Typical Performance Curves – continued
(Reference data)

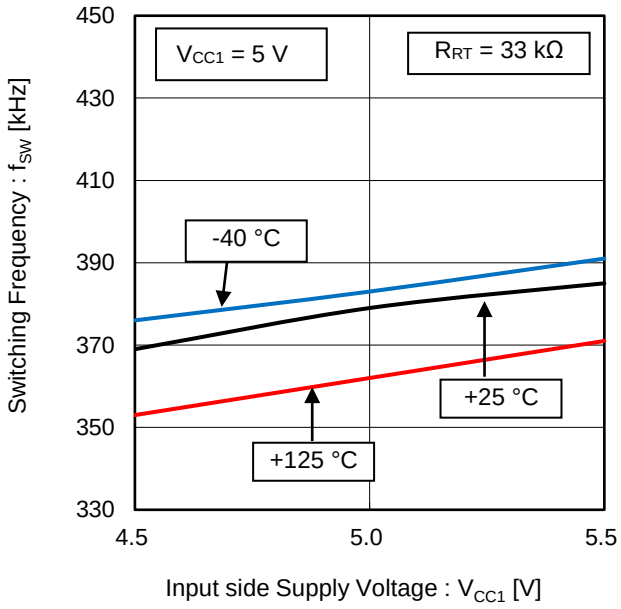


Figure 18. Switching Frequency vs Input side Supply Voltage

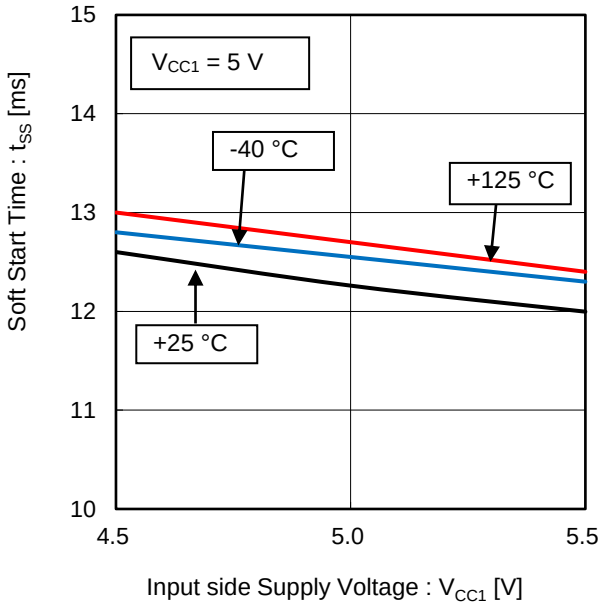


Figure 19. Soft Start Time vs Input side Supply Voltage

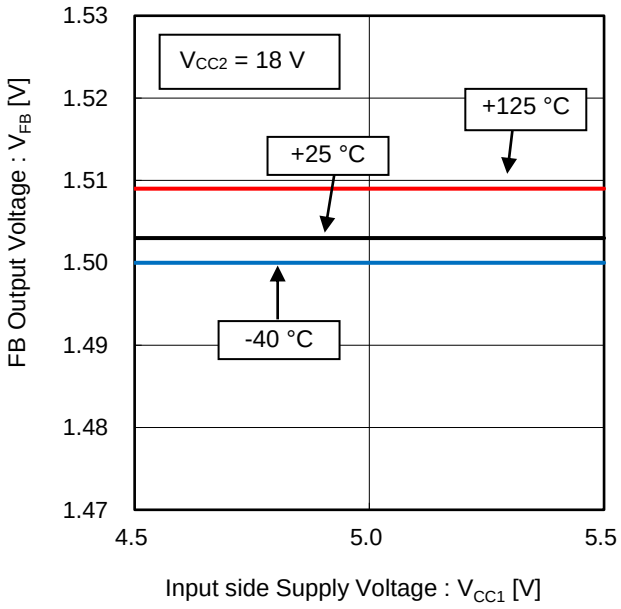


Figure 20. FB Output Voltage vs Input side Supply Voltage

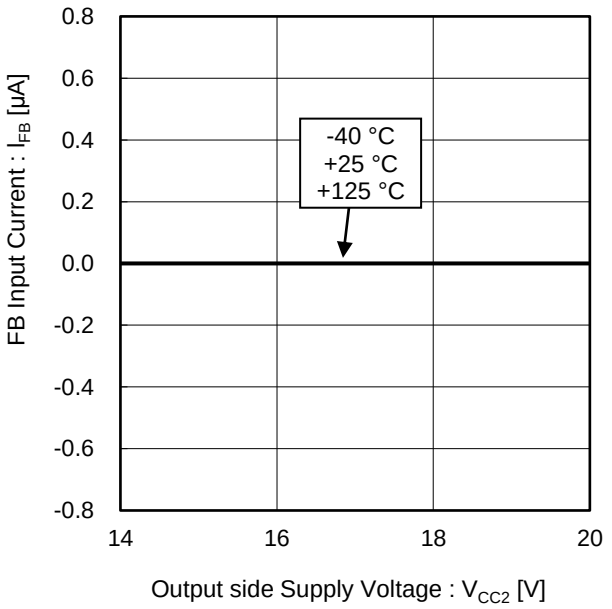


Figure 21. FB Input Current vs Output side Supply Voltage

Typical Performance Curves – continued
(Reference data)

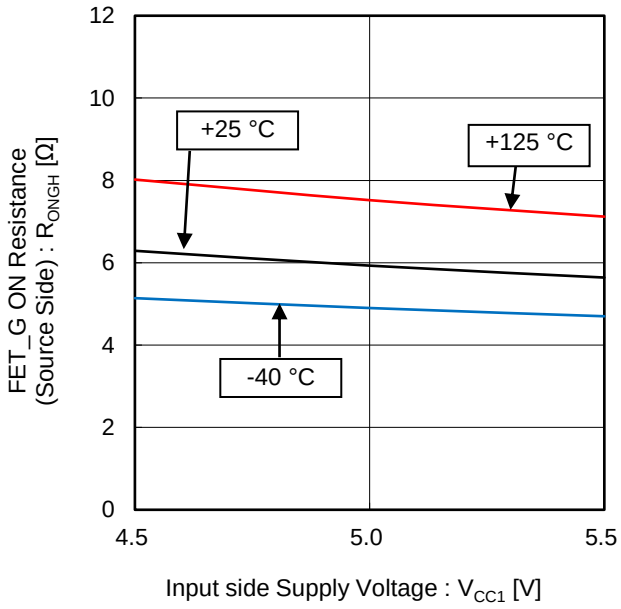


Figure 22. FET_G ON Resistance (Source Side) vs Input side Supply Voltage

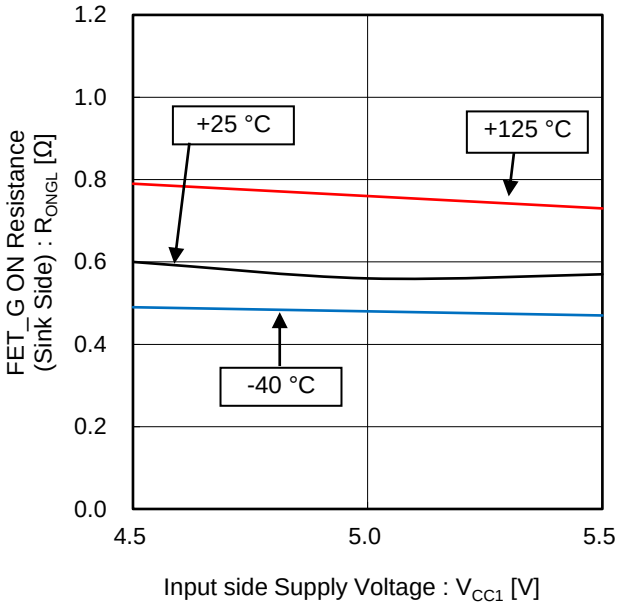


Figure 23. FET_G ON Resistance (Sink Side) vs Input side Supply Voltage

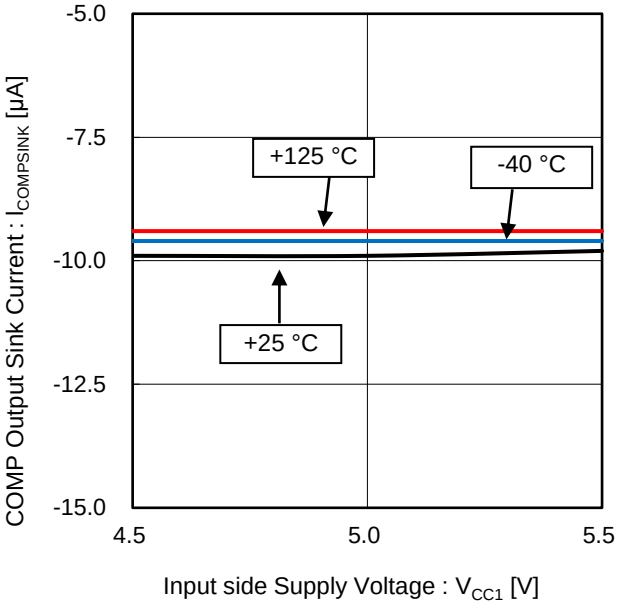


Figure 24. COMP Output Sink Current vs Input side Supply Voltage

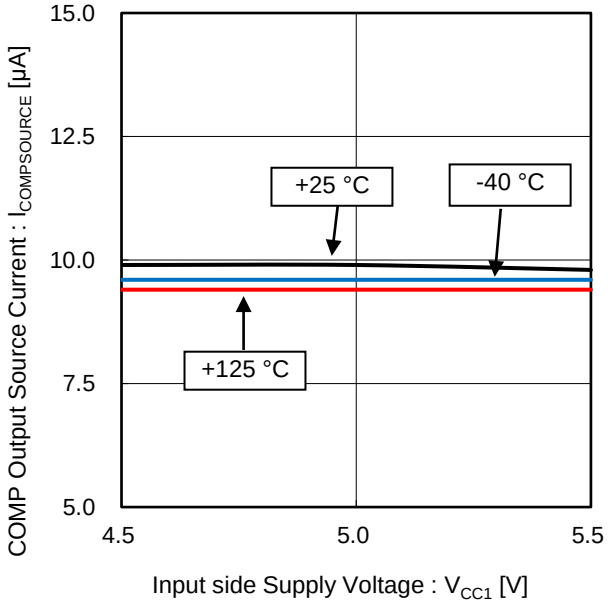


Figure 25. COMP Output Source Current vs Input side Supply Voltage

Typical Performance Curves – continued
(Reference data)

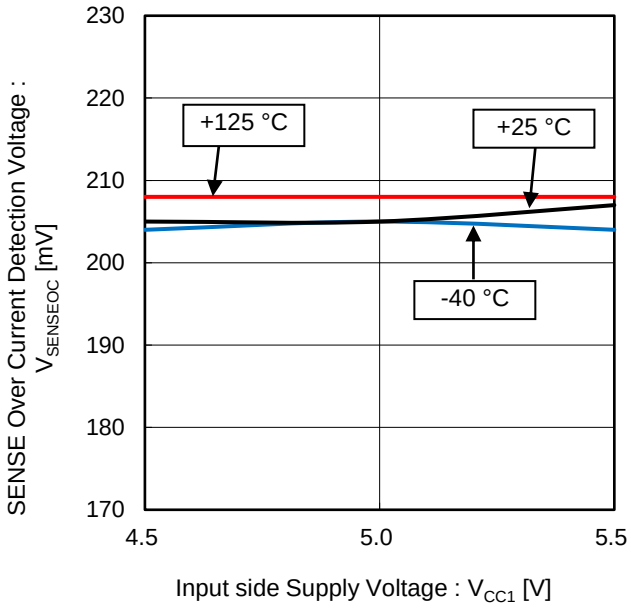


Figure 26. SENSE Over Current Detection Voltage vs Input side Supply Voltage

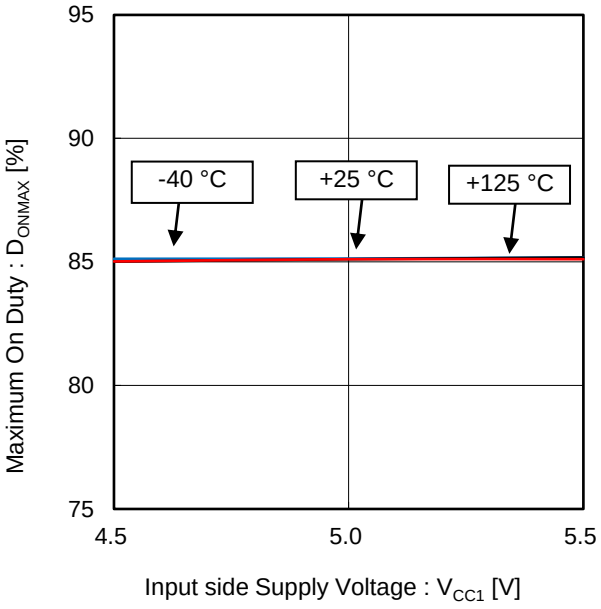


Figure 27. Maximum On Duty vs Input side Supply Voltage

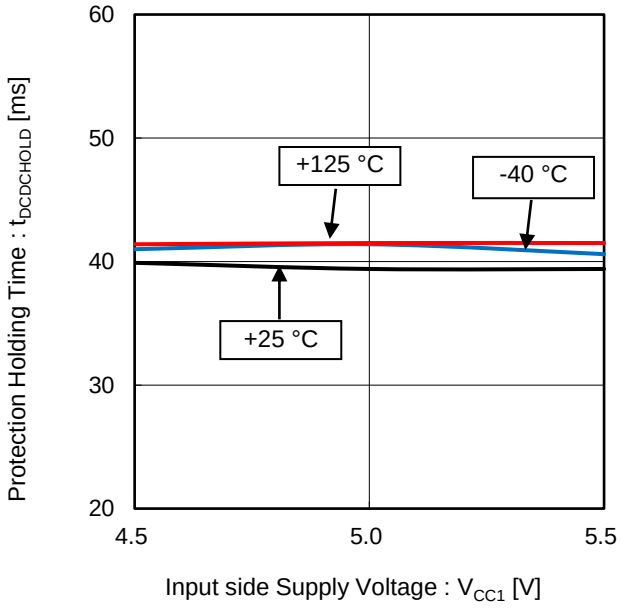


Figure 28. Protection Holding Time vs Input side Supply Voltage

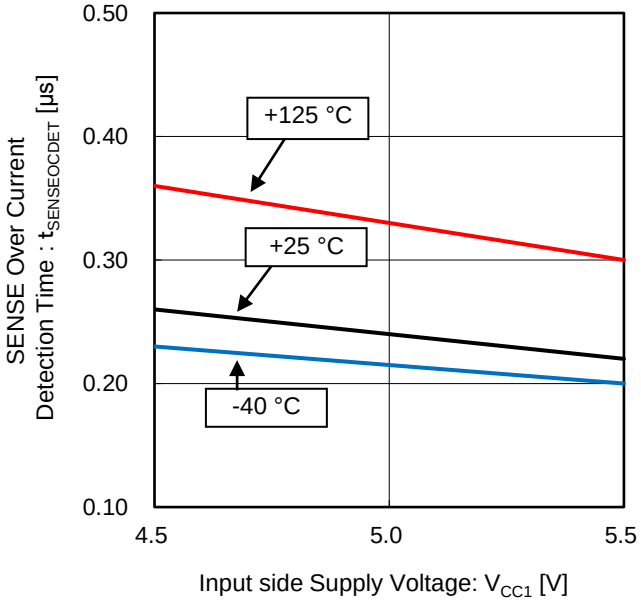


Figure 29. SENSE Over Current Detection Time vs Input side Supply Voltage

Typical Performance Curves – continued
(Reference data)

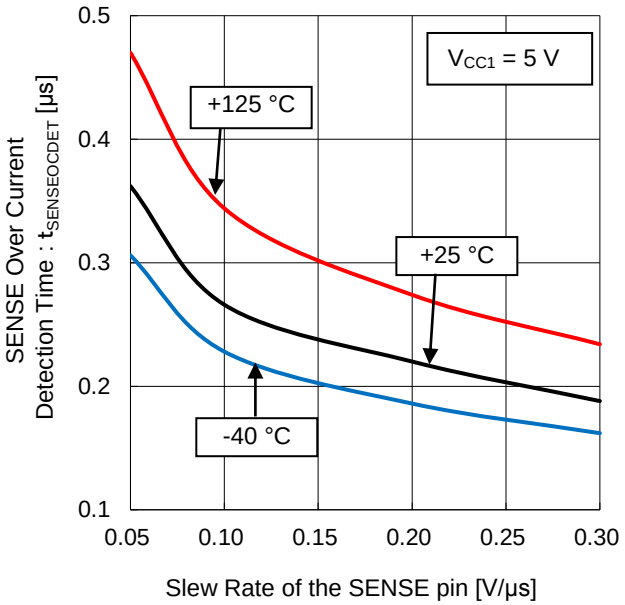


Figure 30. SENSE Over Current Detection Time vs Slew Rate of the SENSE pin

Application Information

1. Description of Pins and Cautions on Layout of Board

(1) VCC1 (Input side power supply)
The VCC1 pin is the power supply on the input side. To suppress voltage fluctuations due to the driving current of the internal transformer, connect a bypass capacitor between the VCC1 pin and the GND1 pins.

(2) GND1 (Input side ground)
The GND1 pin is a ground pin on the input side.

(3) VCC2 (Output side positive power supply)
The VCC2 pin is the positive power supply on the output side. To suppress voltage fluctuations due to the output current of the OUT1H pin and the OUT1L pin and the driving current of the internal transformer, connect a bypass capacitor between the VCC2 pin and the GND2 pins.

(4) VEE2 (Output side negative power supply)
The VEE2 pin is the negative power supply on the output side. To suppress voltage fluctuations due to the output current of the OUT1H pin and the OUT1L pin and the driving current of the internal transformer, connect a bypass capacitor between the VEE2 pin and the GND2 pins. In case no negative power supply is used, connect the VEE2 pin to the GND2 pin.

(5) GND2 (Output side ground)
The GND2 pin is the ground on the output side. Connect the GND2 pin to the emitter or source of the power device.

(6) ENA, ASC, INB, INA (Gate drive control input)
The ENA, INB and INA pins are used to control gate drive.
The ASC pin is used to control Active Short Circuit. In case Active Short Circuit is not used, connect the ASC pin to the GND1 pin.
The truth table about these pins and Gate output, the OUT1H pin and the OUT1L pin are shown as below.
In detail about Active Short Circuit function, refer P32.

ENA	ASC	INB	INA	OUT1H	OUT1L	Gate output
L	Don't care	Don't care	Don't care	Hi-Z	L	L
H	L	H	Don't care	Hi-Z	L	L
H	L	L	L	Hi-Z	L	L
H	L	L	H	H	Hi-Z	H
H	H	Don't care	Don't care	H	Hi-Z	H

(7) FLT (Fault output)
The FLT pin is an open drain pin which outputs a fault state when Short Circuit Protection function operates. The state in which the FLT pin is Low is released at the rising edge of the ENA pin. Also, in case the state of the RDY pin become L, the state in which the FLT pin is Low is released.

States	State of the FLT pin
Normal operation	Hi-Z
Short Circuit Protection operates	L

(8) RDY (Ready output)
The RDY pin is an open drain pin which outputs the state of operations of protection functions for power supply, VCC1 UVLO / VCC1 OVLO / VCC2 UVLO / VCC2 OVLO.

Status	State of the RDY pin
Normal operation	Hi-Z
Either VCC1 UVLO / VCC1 OVLO / VCC2 UVLO / VCC2 OVLO operates	L

(9) OSFB (Output state feedback)
The OSFB pin outputs the state of gate of the power device.

Status	State of the OSFB pin
The voltage of the PROOUT1 pin > V_{OSFBH} (5.0 V(Typ))	H
The voltage of the PROOUT1 pin < V_{OSFBL} (4.5 V(Typ))	L

(10) BISTON (Input for checking Built In Self Test result)
The BISTON pin is used to output BIST result from the BISTOUT pin.
While the BIST is running, the input of the BISTON pin is invalid.

1. Description of Pins and Cautions on Layout of Board – continued

(11) BISTOUT (Built In Self Test result output)
The BISTOUT pin shows the result of BIST function by BISTON rising edge.

Status	State of the BISTOUT pin
Built In Self Test Pass	Hi-Z
Built In Self Test Fail	L

(12) OUT1H, OUT1L (Source side, Sink side output)
The OUT1H pin is a source side pin which drive the gate of a power device. The OUT1L pin is a sink side pin which drive the gate of a power device. The OUT1H pin also monitors the gate voltage for miller clamp.

(13) OUT2 (Active Miller Clamping)
The OUT2 pin is for Miller Clamping which means preventing a rise of gate voltage due to miller current of a power device. When the OUT1H pin voltage falls down to V_{OUT2ON}, Miller Clamping function operates. In case Miller Clamping function is not used, connect the OUT2 pin to the VEE2 pin.

(14) PROOUT1, PROOUT2 (Soft turn off pin 1 / Gate voltage monitor, Soft turn off pin 2)
The PROOUT1 pin and the PROOUT2 pin are for soft turn off of the gate of the power device in case short circuit protection operates. Both the PROOUT1 pin and the PROOUT2 pin become low for the time of t_{PRO2ON} (160 ns(Typ)) from short circuit detection. After t_{PRO2ON} have passed, only the PROOUT1 pin continues L state. The PROOUT1 pin also monitor the gate voltage for output state feedback function.

(15) SCPIN (Short circuit current detection)
The SCPIN pin is used detect excessive current for short circuit protection. In case the SCPIN pin voltage exceeds V_{SCDET} (0.7 V(Typ)), SCP function operates. In case the SCPIN is open, short circuit protection function may operate unexpectedly. To avoid such trouble, connect the SCPIN pin to the GND2 pin in case short circuit protection function is not used. In order to prevent the such unexpected detection due to noise, the noise mask time t_{SCPFIL} (0.15 µs(Typ)) is set. Pin output current I_{SCPIN} (1.0 µA(Typ)) is built in for detection of open state of the SCPIN pin.

(16) FB (Voltage feedback in Switching Controller)
The FB pin is for voltage feedback in Switching Controller. In case Switching Controller is not used, connect to the GND2 pin.

(17) COMP (Charge Pump output in Switching Controller)
The COMP pin is output of Charge Pump in Switching Controller. Charge and discharge operation is done by the constant current of $I_{COMPSOURCE}$ (10 µA(Typ)), $I_{COMPSINK}$ (-10 µA(Typ)), at the duty determined by the result of comparation between the voltage of the FB pin and V_{FB} (1.5 V(Typ)). Connect capacitors and resisters for phase compensation. In case Switching Controller is not used, connect to the GND1 pin.

(18) RT (Switching Frequency setting)
The RT pin is for setting Switching Frequency. By connect resister between the RT pin and the GND1 pin, the oscillation frequency of Switching Controller can be set following the equation descripted in P26. In case Switching Controller is not used, connect to the VCC1 pin.

(19) FET_G (Control external MOSFET driving trans)
The FET_G pin is for control external MOSFET which drives external trans. In case Switching Controller is not used, set the FET_G pin open.

(20) SENSE (Current Sense input in Switching Controller)
The SENSE pin is input of Current Sense in Switching Controller. Connect R_{SENSE} to GND1. In case Switching Controller is not used, connect to the GND1 pin.

Application Information – continued

2. Description of Functions and Examples of Constant Setting

(1) Active Miller Clamping

In case OUT1H = Hi-Z and the voltage of the OUT1H pin become V_{OUT2ON} (2.0 V(Typ)) or less, internal MOSFET at the OUT2 pin is latched to L and Miller Clamping function operates. After Miller Clamping function operates, the OUT2 pin keeps L state until the OUT1H pin become H again. In case any protection functions as below operates, Miller Clamping function operates also as long as the voltage of the OUT1H pin become V_{OUT2ON} or less.

State	Input logic	Voltage of the OUT1H pin	State of the OUT2 pin
Normal operation	L	V_{OUT2ON} or more	Hi-Z
		V_{OUT2ON} or less	L
	H	Don't care	Hi-Z
Either VCC1 UVLO, VCC1 OVLO, VCC2 UVLO, VCC2 OVLO, SCP, OC operates	X	V_{OUT2ON} or more	Hi-Z
		V_{OUT2ON} or less	L

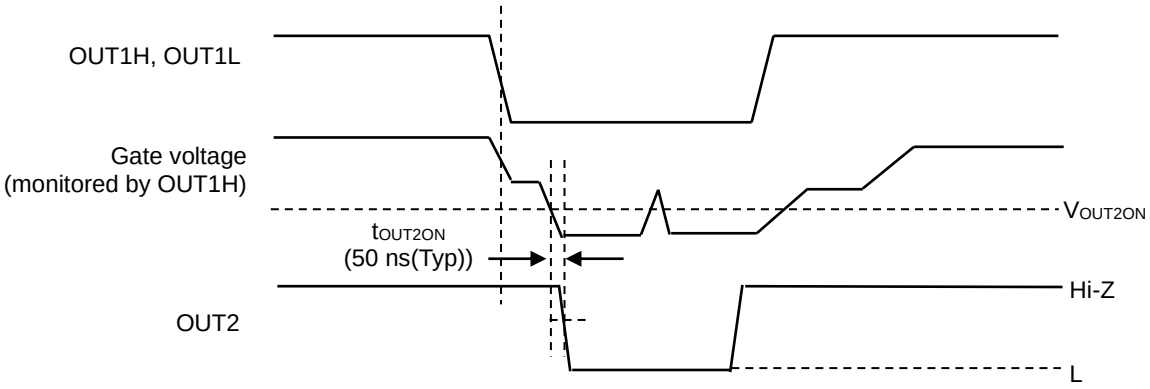


Figure 31. Timing Chart of Active Miller Clamping

2. Description of Functions and Examples of Constant Setting – continued

(2) Fault Status Output
In case Short Circuit Protection operates, the FLT pin is latched to L and released by rising edge from L to H of the ENA pin.

(3) Under Voltage Lock Out (UVLO)
Under Voltage Lock Out (UVLO) function is built in to both input side and output side. In case the voltage of the VCC1 pin or the VCC2 pin drops to UVLO ON voltage V_{UVLO1L} (4.15 V(Typ)) and V_{UVLO2L} (11.5 V(Typ)) or less, the OUT1L pin and the RDY pin become to L, if input logic is H, the OUT1H pin turns from H to Hi-Z. And, in case these voltage rise to UVLO OFF voltage V_{UVLO1H} (4.25 V(Typ)) and V_{UVLO2H} (12.5 V(Typ)) or more, the RDY pin and the OUT1H pin become to Hi-Z, and the OUT1H pin returns from Hi-Z to H if input logic is H. In order to prevent malfunctions due to noise, the noise mask time $t_{UVLO1FIL}$ and $t_{UVLO2FIL}$ are built in to both input side and output side.

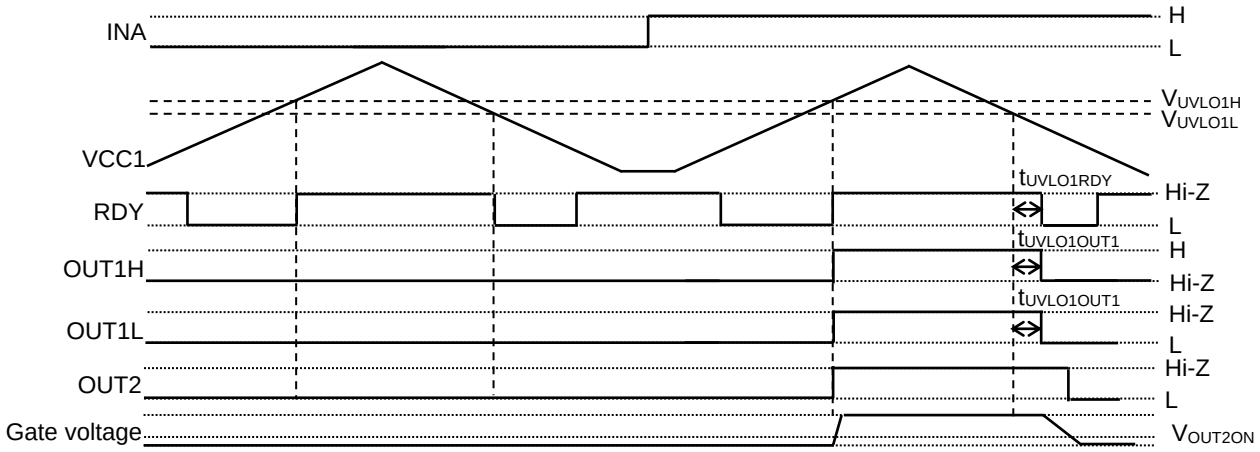


Figure 32. Timing Chart of input side UVLO operation

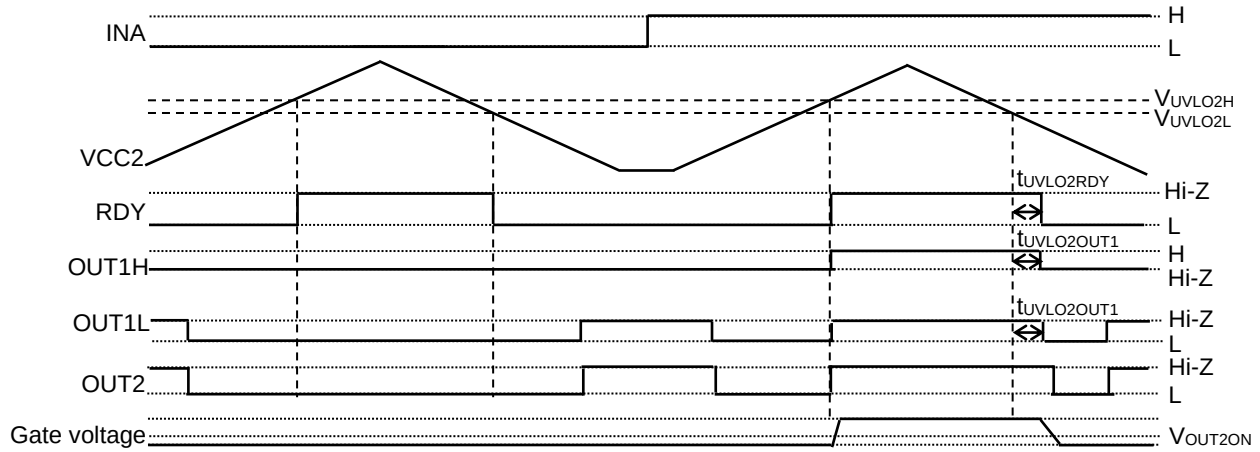


Figure 33. Timing Chart of output side UVLO operation

2. Description of Functions and Examples of Constant Setting – continued

(4) Over Voltage Lock Out (OVLO)

Over Voltage Lock Out (OVLO) function is built in to both input side and output side. In case the voltage of the VCC1 pin or the VCC2 pin rises to OVLO ON voltage V_{OVLO1H} (6.5 V(Typ)) and V_{OVLO2H} (22.5 V(Typ)) or more, the OUT1L pin and the RDY pin become to L, if input logic is H, the OUT1H pin turns from H to Hi-Z. And, in case these voltage drops to OVLO OFF voltage V_{OVLO1L} (6.4 V(Typ)) and V_{OVLO2L} (21.5 V(Typ)) or less, the RDY pin and the OUT1H pin become to Hi-Z and the OUT1H pin returns from Hi-Z to H if input logic is H. In order to prevent malfunctions due to noise, the noise mask time $t_{OVLO1FIL}$ and $t_{OVLO2FIL}$ are built in to both input side and output side.

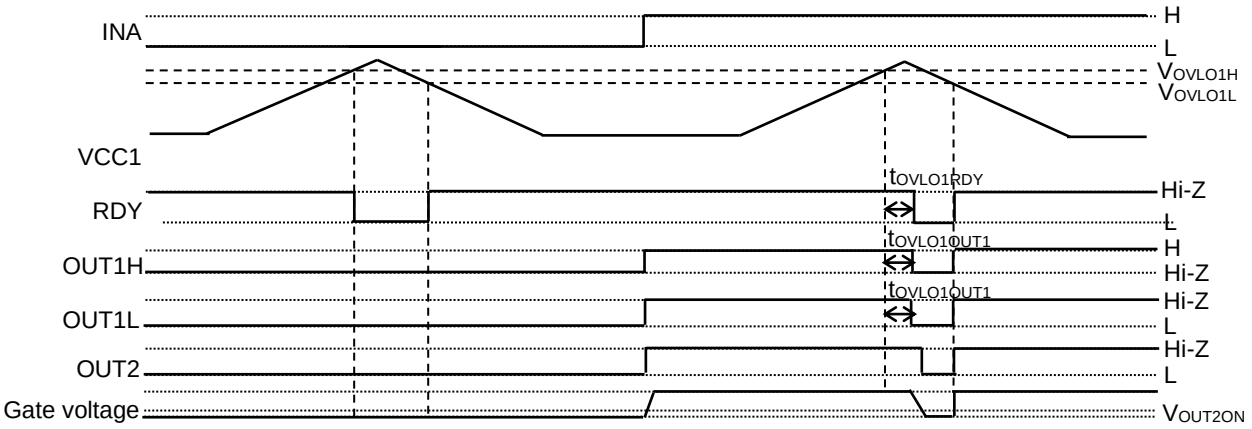


Figure 34. Timing Chart of input side OVLO operation

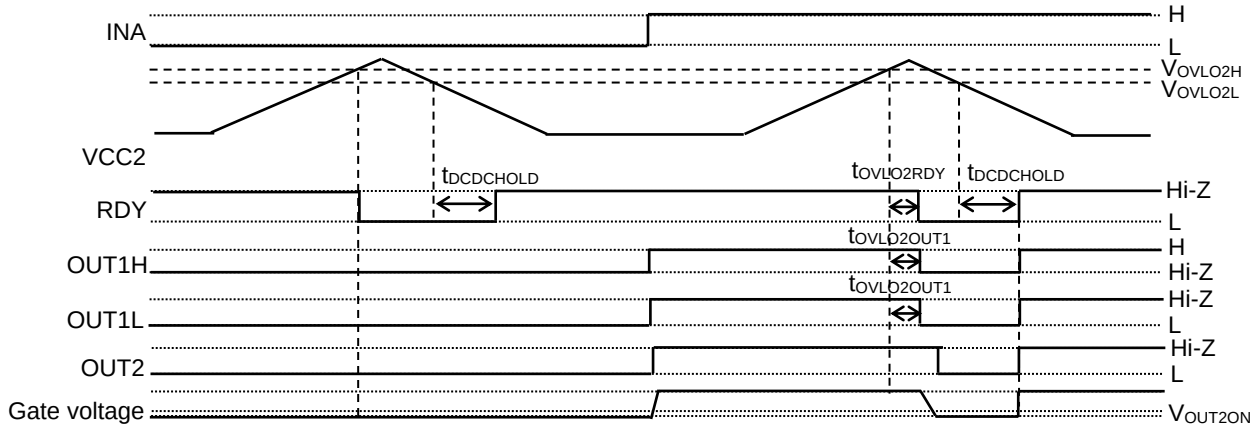


Figure 35. Timing Chart of output side OVLO operation

2. Description of Functions and Examples of Constant Setting – continued

(5) Short Circuit Protection (SCP)

In case the voltage of the SCPIN pin exceeds V_{SCDET} (0.7 V(Typ)), Short Circuit Protection operates, states of the OUT1H pin and the OUT1L pin voltages are latched to Hi-Z, and both the PROOUT1 pin and the PROOUT2 pin become L for the time of t_{PRO2ON} (160 ns(Typ)) from short circuit detection. After t_{PRO2ON} have passed, the PROOUT2 pin become Hi-Z and only the PROOUT1 pin continues L state. After that, the voltage of the OUT2 pin drops to V_{OUT2ON} (2 V(Typ)), and the OUT1L pin become L and the PROOUT1 pin become Hi-Z. After that, Short Circuit Protection is released by rising edge of L to H of the ENA pin.

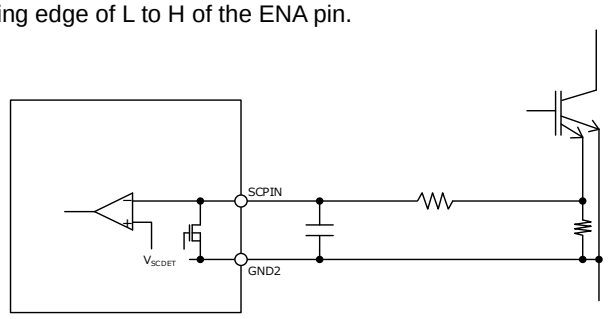


Figure 36. Application example of Short Circuit Protection

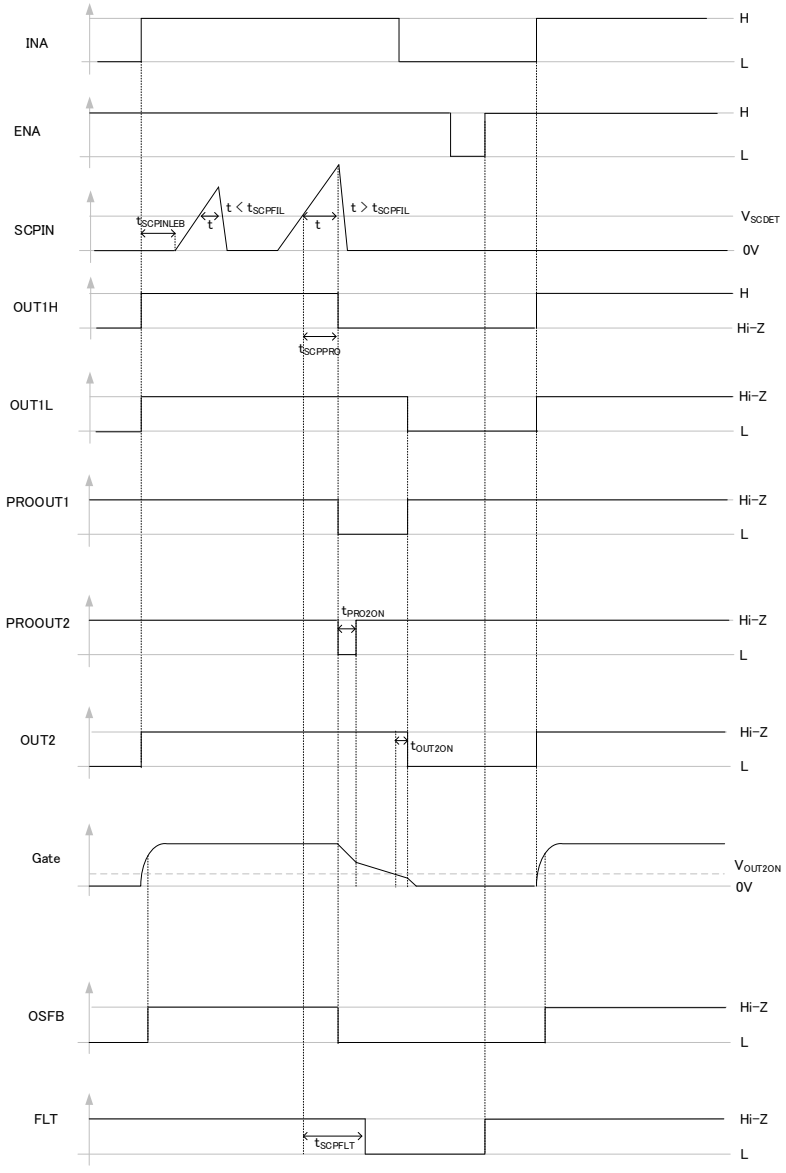


Figure 37. Timing Chart of Short Circuit Protection

(5) Short Circuit Protection (SCP) – continued

Short Circuit Protection can be used as DESAT function. Collector or drain voltage (V_{DESAT}) of power device can be detected by setting external components as below.

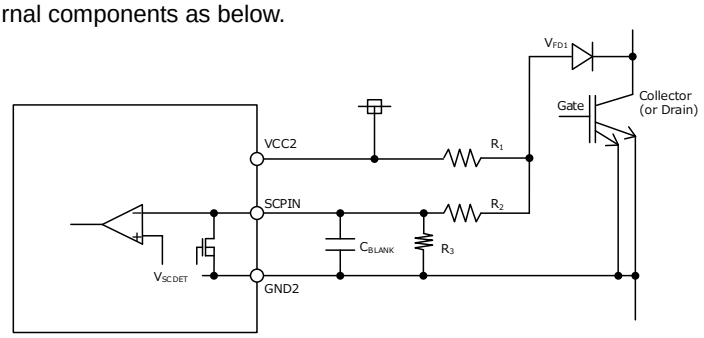


Figure 38. Block Diagram of DESAT function

Timing Chart of DESAT function operation is shown as below.

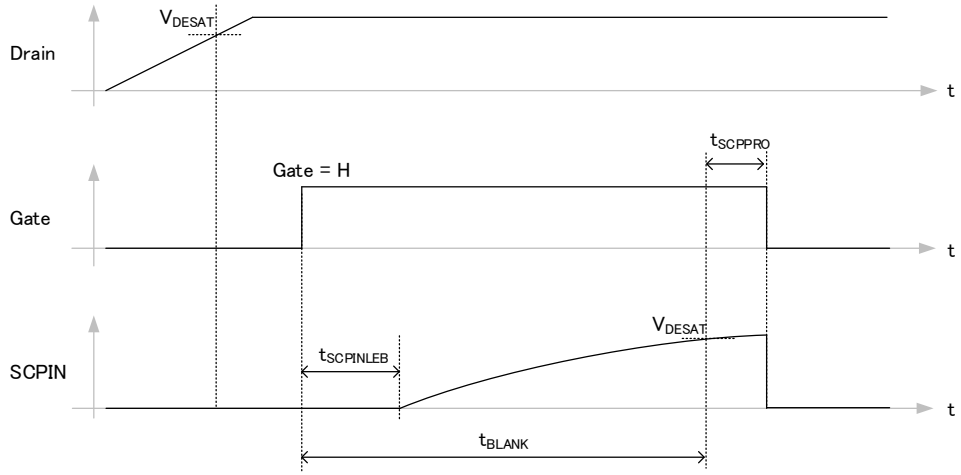


Figure 39. Timing Chart of DESAT function operation

Each parameter in DESAT function, detection threshold voltage V_{DESAT} and blanking time t_{BLANK} and minimum value of V_{CC2} at which DESAT function is valid $V_{VCC2MIN}$ can be determined as the formula below.

$$V_{DESAT} = V_{SCDET} \times \frac{R_2 + R_3}{R_3} - V_{FD1} - R_2 \times I_{SCPIN} \text{ [V]}$$

$$t_{BLANK} = -\frac{R_1 + R_2}{R_1 + R_2 + R_3} \times R_3 \times (C_{BLANK} + 5.5 \times 10^{-12}) \times \ln\left(1 - \frac{(R_1 + R_2 + R_3) \times V_{SCDET}}{R_3 \times V_{CC2} + R_3 \times (R_1 + R_2) \times I_{SCPIN}}\right) + t_{SCPINLEB} \text{ [s]}$$

$$V_{VCC2MIN} > V_{SCDET} \times \frac{R_1 + R_2 + R_3}{R_3} \text{ [V]}$$

V_{DESAT} : DESAT detection threshold voltage of power device
t_{BLANK} : Blanking time
$V_{VCC2MIN}$: Minimum value of V_{CC2} at which DESAT function is valid
V_{SCDET} : Short Circuit Detection Voltage
V_{FD1} : Forward voltage of external diode
I_{SCPIN} : SCPIN Output Current
R_1, R_2, R_3 : The value of external resisters
C_{BLANK} : The value of external capacitor

(5) Short Circuit Protection (SCP) – continued

An example in which each value of V_{DESAT} is determined by setting value of resistance R_1, R_2, R_3 is shown as below table.

V_{DESAT}	Setting Value		
	R_1	R_2	R_3
4.0 V	15 kΩ	39 kΩ	6.8 kΩ
4.5 V	15 kΩ	43 kΩ	6.8 kΩ
5.0 V	15 kΩ	36 kΩ	5.1 kΩ
5.5 V	15 kΩ	39 kΩ	5.1 kΩ
6.0 V	15 kΩ	43 kΩ	5.1 kΩ
6.5 V	15 kΩ	62 kΩ	6.8 kΩ
7.0 V	15 kΩ	68 kΩ	6.8 kΩ
7.5 V	15 kΩ	82 kΩ	7.5 kΩ
8.0 V	15 kΩ	91 kΩ	8.2 kΩ
8.5 V	15 kΩ	82 kΩ	6.8 kΩ
9.0 V	15 kΩ	130 kΩ	10 kΩ
9.5 V	15 kΩ	91 kΩ	6.8 kΩ
10.0 V	15 kΩ	130 kΩ	9.1 kΩ

(6) Output State Feedback

The gate logic is monitored by the PROOUT1 pin, and outputted to the logic of the OSFB pin.
The voltage of the PROOUT1 pin rises to V_{OSFBH} or more, and the OSFB pin become H. The voltage of the PROOUT1 pin drops to V_{OSFBL} or less, the OSFB pin become L.

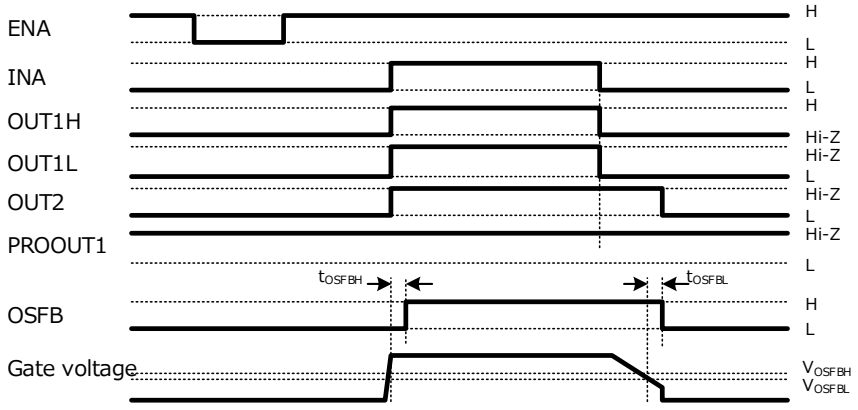


Figure 40. Timing Chart of Output State Feedback

2. Description of Functions and Examples of Constant Setting – continued

(7) Switching Controller

(a) Basic Operation

Switching Controller Circuit which repeats ON and OFF synchronizing to the internal oscillator is built in to this IC. When V_{CC1} power on and $V_{CC1} > V_{UVLO1H}$, the FET_G pin starts Soft Start switching. Output Voltage V_{OUT} is determined by V_{FB} (= 1.5 V(Typ)), resister R_1 and R_2, as the formula below.

$$V_{OUT} = V_{FB} \times \{(R_{FB1} + R_{FB2})/R_{FB2}\} \text{ [V]}$$

(b) Setting Switching Frequency

Switching Frequency f_{SW_EQ} is determined by resister R_T which is connected between the RT pin and the GND1 pin, as the formula below.

$$f_{SW\_EQ} = 1 \,/\, (6.68 \times 10^{-8} \times R_{RT} + 4.68 \times 10^{-4}) \text{ [kHz]}$$

(c) Soft Start

After power on, for a definite period of time, by limiting the volage of the SENSE pin to limit ON duty, and rising that limited voltage gradually, Soft Start is realized in which output voltage starts with charge current limited and rised gradually. When V_{CC1} power on and after $V_{CC1} > V_{UVLO1H}$, in each period as the table below, when the voltage of the SENSE pin reaches to the limited voltage for each period, the FET_G pin is forced to be L.

The period from power on	From 0 ms To 2.5 ms	From 2.5 ms To 5.0 ms	From 5.0 ms To 7.5 ms	From 7.5 ms To 10.0 ms	From 10.0 ms To 12.5 ms	After 12.5 ms
Limited voltage at the SENSE pin	40 mV	60 mV	80 mV	100 mV	100 mV	$V_{SENSEOC}$ = 200 mV (Over Current Protection)

Caution in start up:
After power on, during the voltage of the VCC1 pin is from 0 V to 2.54 V (Max), the voltage of the FET_G pin may be indefinite, so it may be possible that external MOSFET operates.

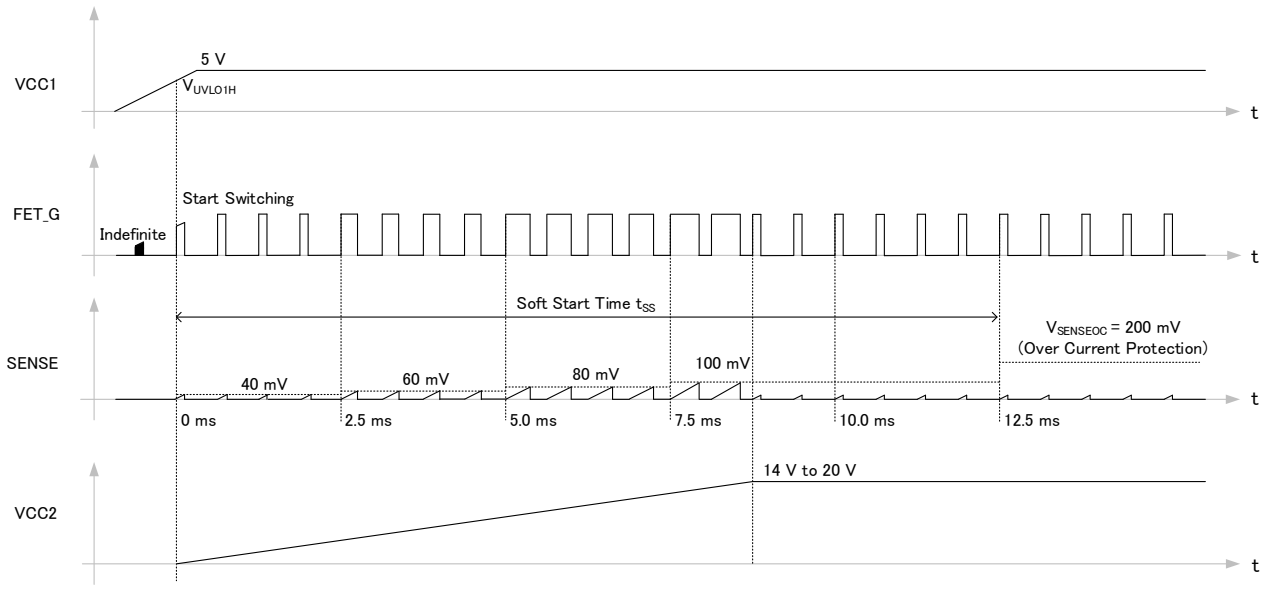


Figure 41. Timing Chart of Soft Start of Switching Controller

(7) Switching Controller – continued

(d) MAX DUTY

In case such as the value of flyback trans is abnormally high and therefore ON duty is abnormally high, MAX DUTY (D_{ONMAX}) operates and the FET_G pin is forced to be L.

(e) Pin setting in case Switching Controller is not used

In case Switching Controller is not used, set each pin as the table below.

Pin No.	Pin name	Pin setting
3	FB	Connect to the GND2 pin
32	RT	Connect to the VCC1 pin
33	COMP	Connect to the GND1 pin
35	SENSE	Connect to the GND1 pin
37	FET_G	Open

(f) Application for using tertiary winding trans

In application of using tertiary winding trans, recommended external parts list is shown as the table below.

In case using these parameters of external components, V_{OUT} value is 16.5 V (Typ) and V_{OUT} value is 16.5 V (Typ) and f_{SW_EQ} is 380 kHz (Typ).

Parts	Parts Symbol	Value	Manufacture	Product No.
Trans	T_1	-	SUMIDA	CEEH1011B (17357-T014)
Diode	D_1, D_2, $D_{SNUBBER}$	-	ROHM	RB168MM150TF
Nch MOS	M_{FET_G}	-	ROHM	RSR025N05HZG
Resister	$R_{SNUBBER}$	2.2 kΩ	ROHM	MCR03EZPD2201
Resister	R_{RT}	33 kΩ	ROHM	MCR03EZPD3302
Resister	R_{SENSE}	68 mΩ	ROHM	LTR18EZPFSR068
Resister	R_{FB1}	22 kΩ	ROHM	MCR03EZPD2202
Resister	R_{FB2}	2 kΩ	ROHM	MCR03EZPD2001

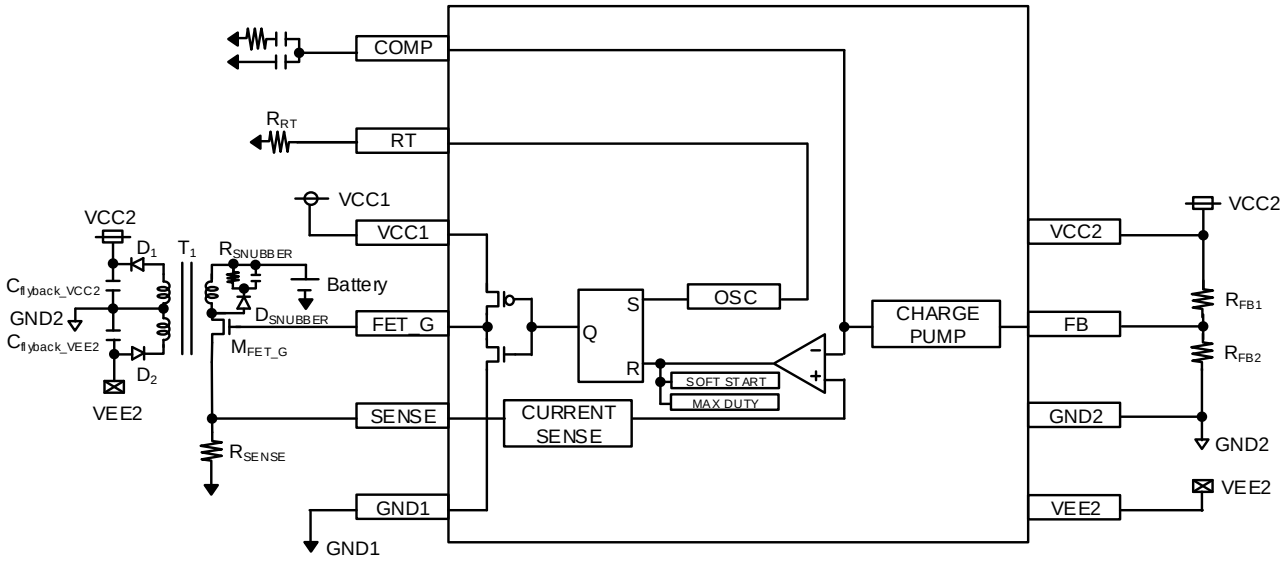


Figure 42. Block Diagram of Switching Controller using tertiary winding trans

(7) Switching Controller – continued

(g) Application for using secondary winding trans

In application of using secondary winding trans , recommended external parts list is shown as the table below.

Parts	Parts Symbol	Value	Manufacture	Product No.
Trans	T_2	-	SUMIDA	CEEH911 (17365-T006)
Diode	D_1, D_2, $D_{SNUBBER}$	-	ROHM	RB168MM150TF
Nch MOS	M_{FET_G}	-	ROHM	RSR025N05HZG
Resister	$R_{SNUBBER}$	2.2 kΩ	ROHM	MCR03EZPD2201
Resister	R_{RT}	33 kΩ	ROHM	MCR03EZPD3302
Resister	R_{SENSE}	68 mΩ	ROHM	LTR18EZPFSR068
Resister	R_{FB1}	22 kΩ	ROHM	MCR03EZPD2202
Resister	R_{FB2}	2 kΩ	ROHM	MCR03EZPD2001
Zener Diode	ZD_1	-	ROHM	BZX84C2V4LYFH
Resister	R_{ZD}	3 kΩ	ROHM	MCR03EZPD3001

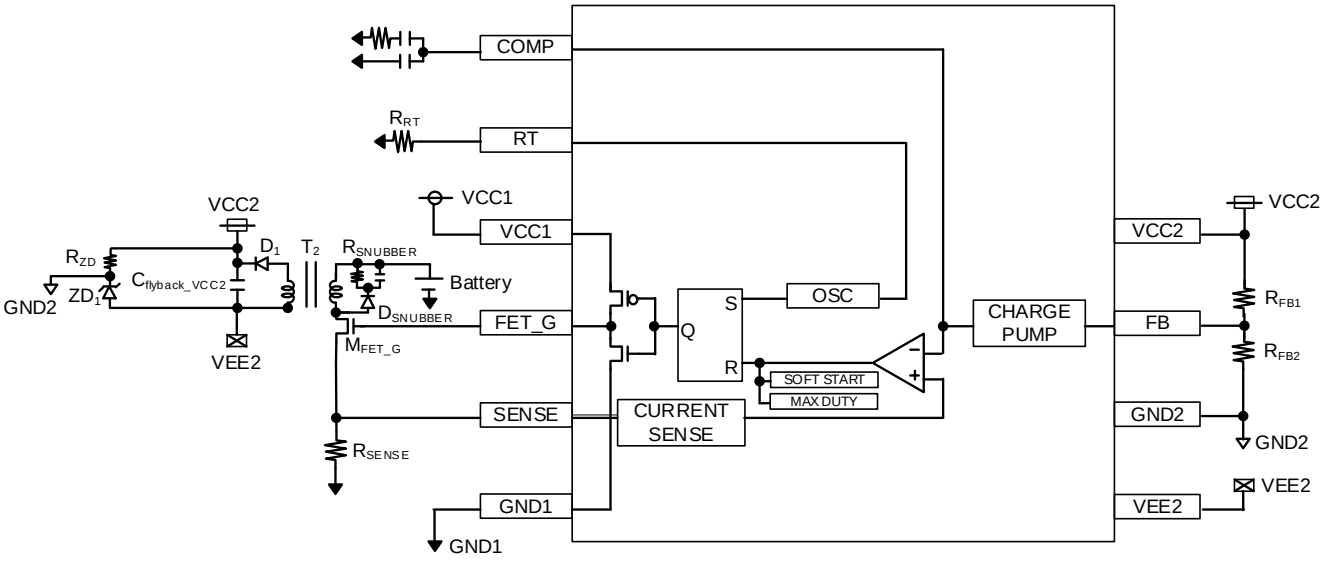


Figure 43. Block Diagram of Switching Controller using secondary trans

2. Description of Functions and Examples of Constant Setting – continued

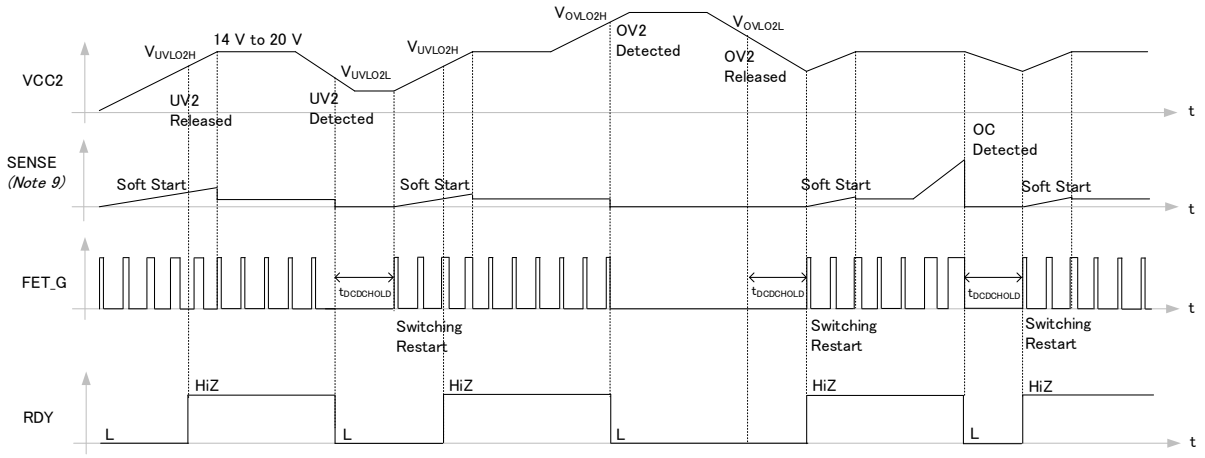
(8) Operation of Switching Controller under each protection function (VCC2 UVLO, VCC2 OVLO, OC)
In case each protection function (VCC2 UVLO, VCC2 OVLO, OC) operates, switching operation is forced to stopped for protection of MOSFET at the FET_G pin.
OC is Over Current Protection. When abnormal current is occurred at MOSFET at the FET_G pin, over current is detected and switching operation is forced to stopped.

Operation in detail under each protection function is as below.

VCC2 UVLO: In case VCC2 UVLO is detected, switching is stopped and the FET_G pin is forced to be L.
And after $t_{DCDCHOLD}$ (40 ms (Typ)) have passed, switching is started again by Soft Start operation.
During Soft Start operation, the operation in which switching is stopped is invalid.
And after Soft Start operation has been finished, VCC2 UVLO function becomes enable.

VCC2 OVLO: In case VCC2 OVLO is detected, switching is stopped and the FET_G pin is forced to be L.
And after $t_{DCDCHOLD}$ have passed only after VCC2 OVLO is released, switching is started again by Soft Start operation.

OC: In case OC is detected, switching is stopped and the FET_G pin is forced to be L.
And after $t_{DCDCHOLD}$ have passed, switching is started again by Soft Start operation.



(Note 9) About the voltage of the SENSE pin, averaged value is described.

Figure 44. Timing Chart of Operation of Switching Controller under each protection function

2. Description of Functions and Examples of Constant Setting – continued

(9) BIST function

Built In Self Test (BIST) of protection functions (VCC1 UVLO, VCC2 UVLO, VCC1 OVLO, VCC2 OVLO, Short Circuit Protection, Over Current Protection) is built in.

When V_{CC1} power on and $V_{CC1} > V_{UVLO1H}$, BIST of OC starts at first. After that, the FET_G pin starts switching. And when V_{CC2} rises and $V_{CC2} > V_{UVLO2H}$, the RDY pin is released from L to Hi-Z, and BIST of other protection function starts. After BIST have been finished, the result of BIST is outputted to the BISTOUT pin by input signal to the BISTON pin. After BIST have been completed means both period $t_{BISTSTRDY}$ and $t_{RDYBISTOFF}$ have passed from the RDY pin is released from L to Hi-Z, the input signal to the ENA, INA, INB pins for gate drive control and input signal to the BISTON pin for the checking of the result of BIST become enable.

Notice that BIST function is operated only when VCC1 UVLO is released and not operated when VCC2 UVLO is released.

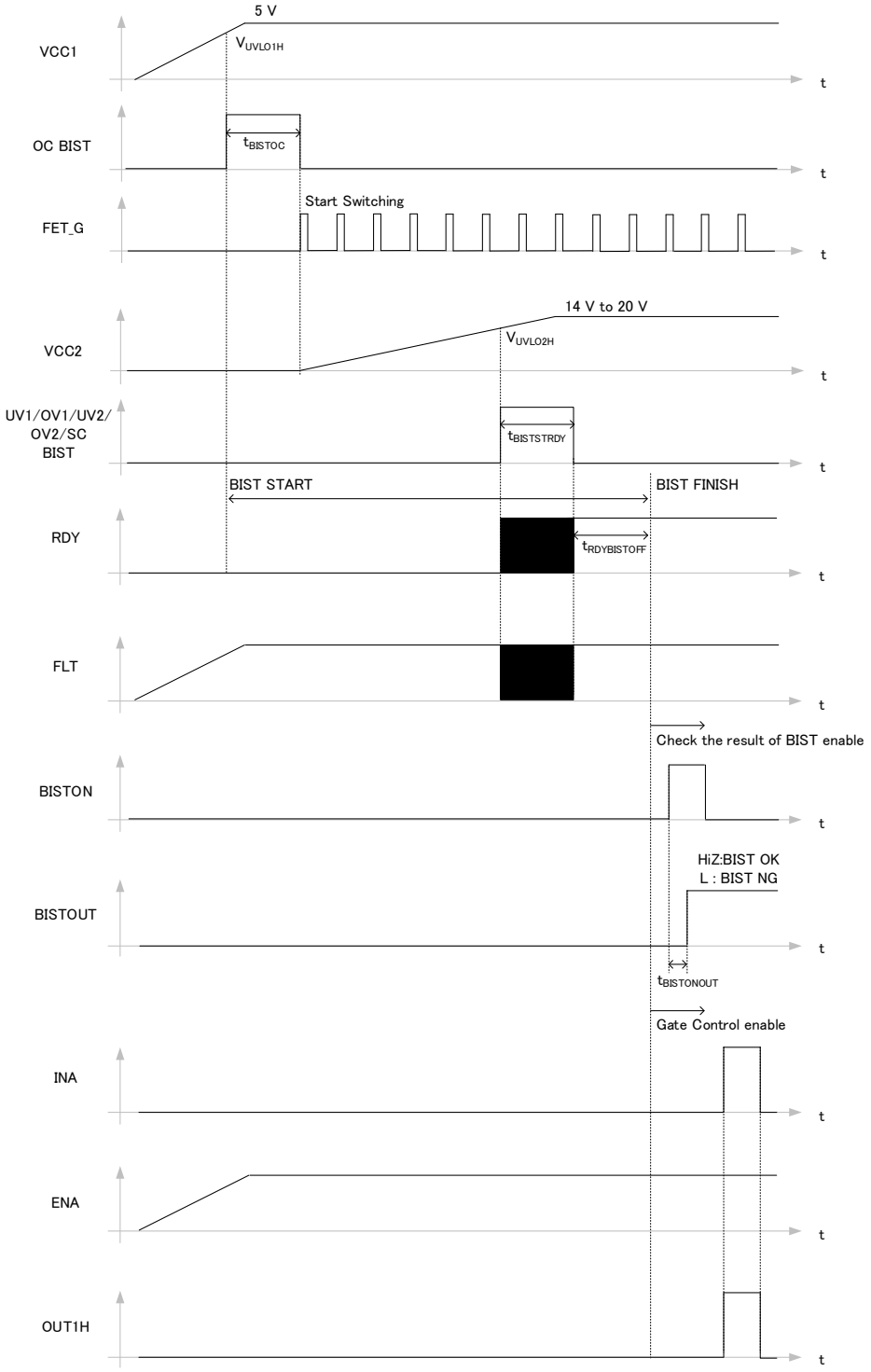


Figure 45. Timing Chart of BIST operation
(V_{CC1} power on at first)

(9) BIST function – continued

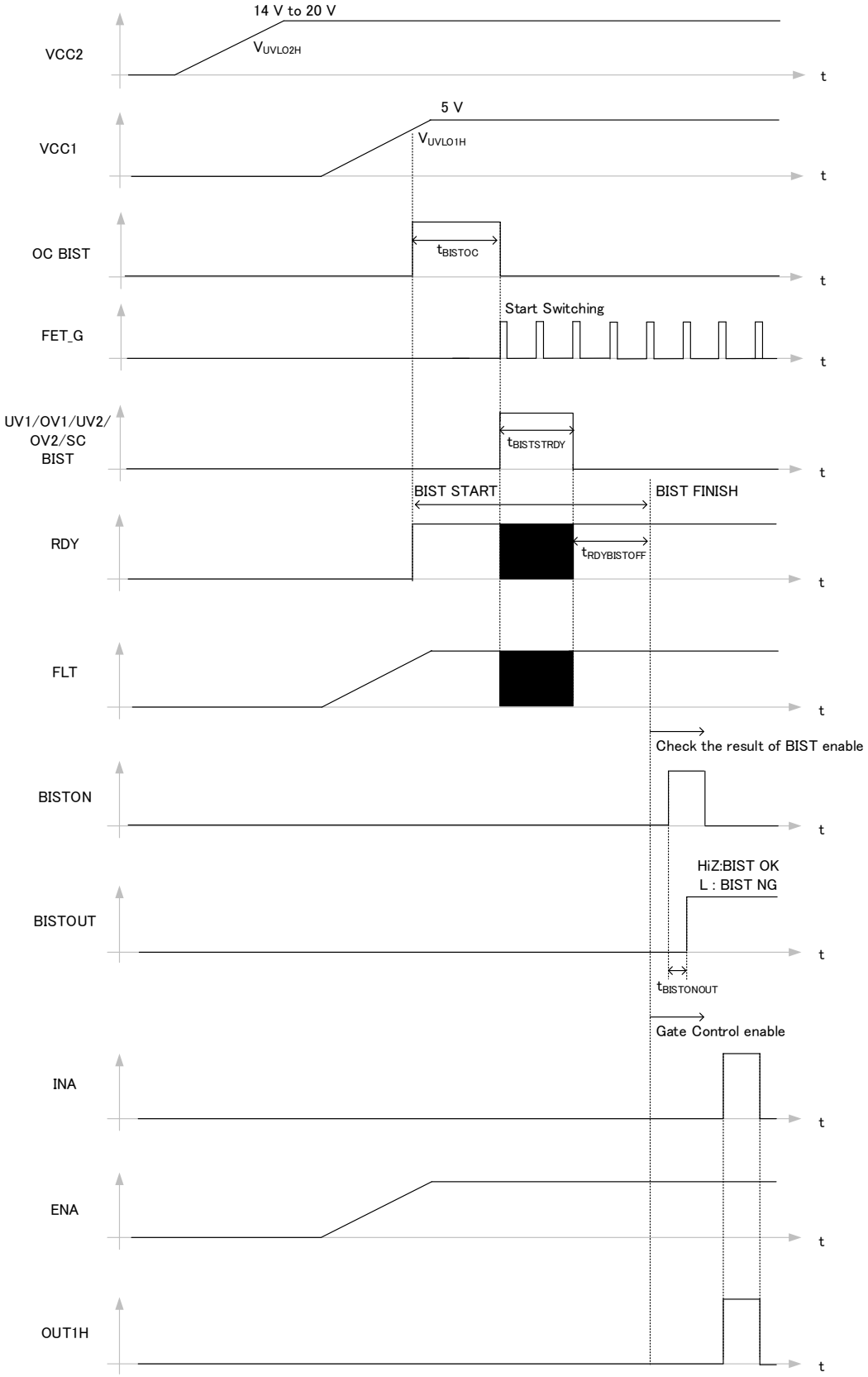


Figure 46. Timing Chart of BIST operation
(External V_{CC2} power on at first)

2. Description of Functions and Examples of Constant Setting – continued

(10) Active Short Circuit

For protection of power device, Active Short Circuit function is built in.
The priority of the logic of the ASC pin is higher than that of the INA pin and the INB pin as the table below.

ENA	ASC	INB	INA	Gate Output
L	Don't care	Don't care	Don't care	L
H	L	H	Don't care	L
H	L	L	L	L
H	L	L	H	H
H	H	Don't care	Don't care	H

In Active Short Circuit operation, protection functions VCC1 UVLO, VCC2 UVLO, VCC1 OVLO, VCC2 OVLO, Short Circuit Protection, Over Current are enable also.
The Timing Chart of Active Short Circuit is shown as below.

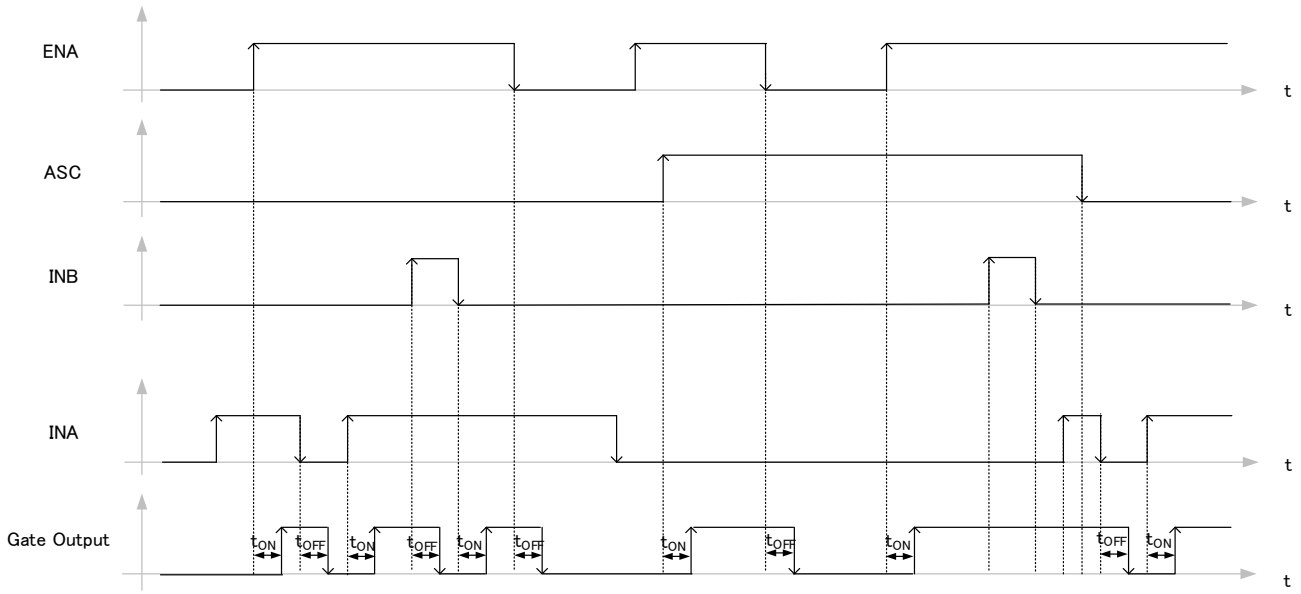
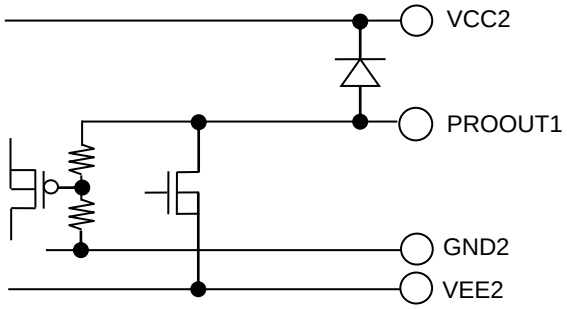
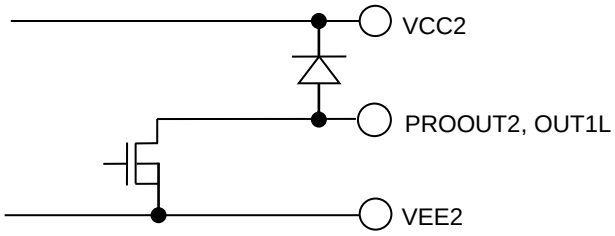
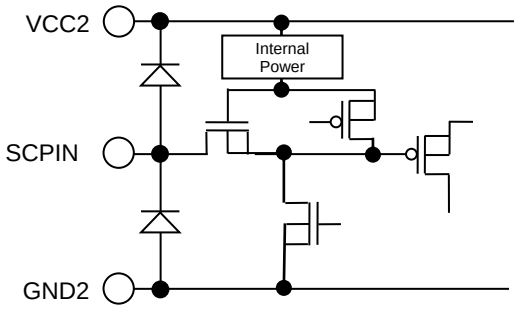
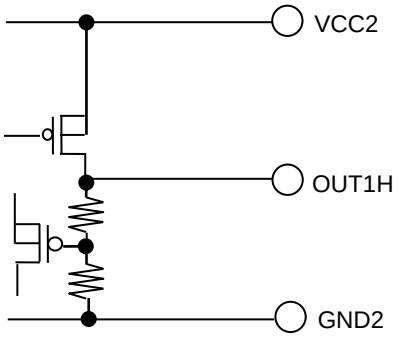
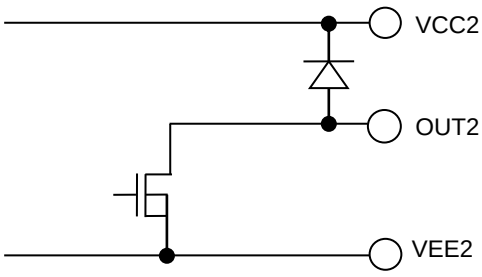
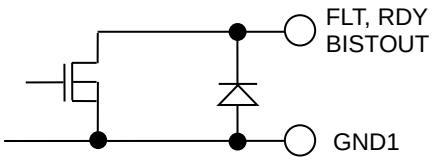
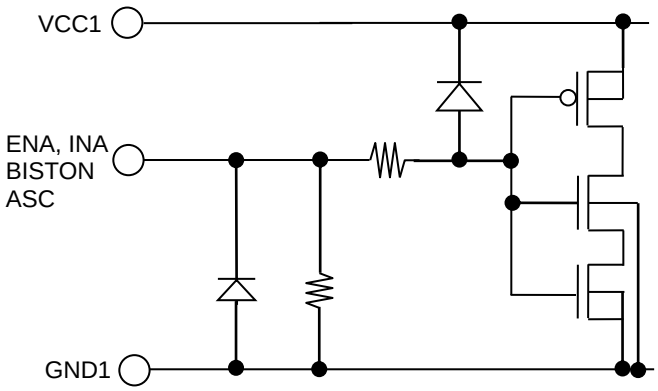


Figure 47. Timing Chart of Active Short Circuit operation

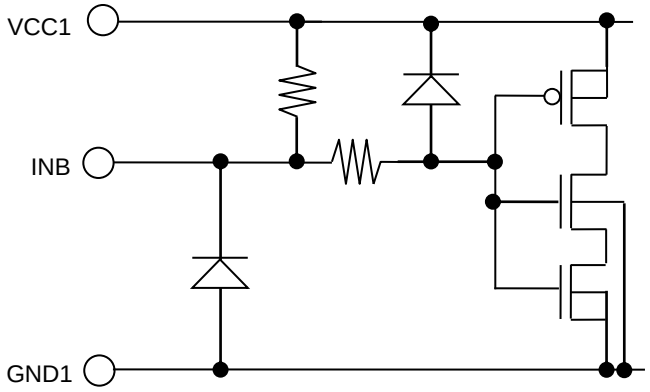
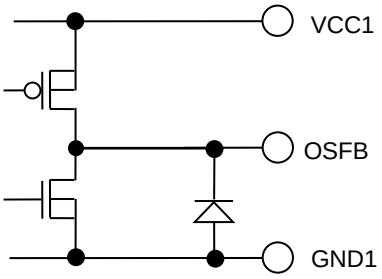
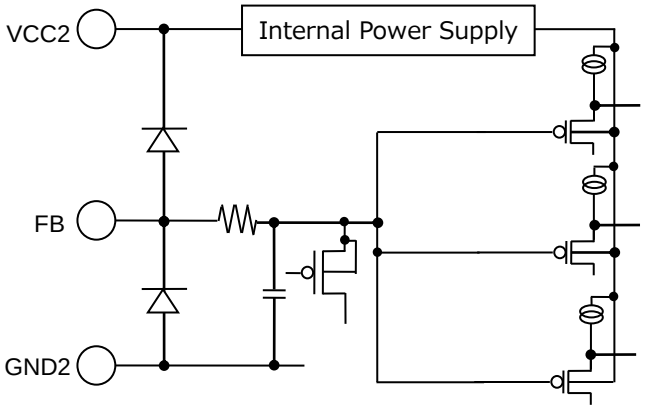
I/O Equivalence Circuit

Pin No.	Pin Name / Pin Function	Input Output Equivalence Circuit Diagram
5	PROOUT1 Soft turn off output 1 / Gate voltage monitor	
6 15	PROOUT2 Soft turn off output 2 OUT1L Sink side output	
7	SCPIN Short circuit current detection input	
13	OUT1H Source side output	
17	OUT2 Active Miller Clamping output	

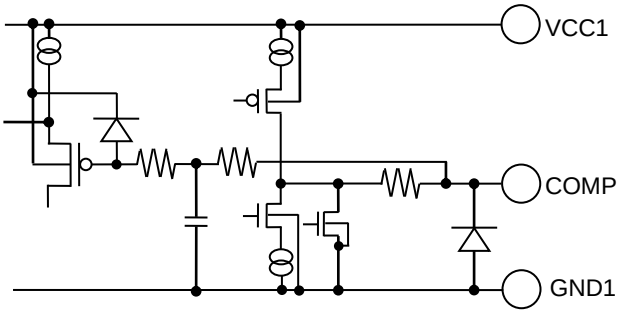
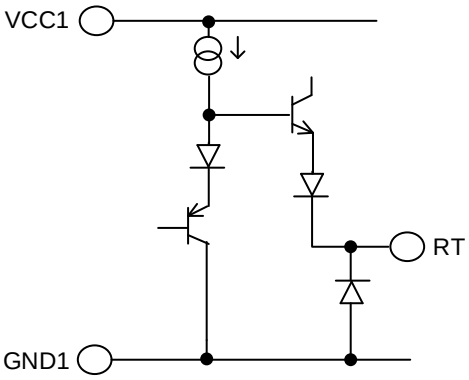
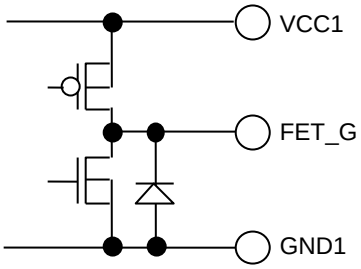
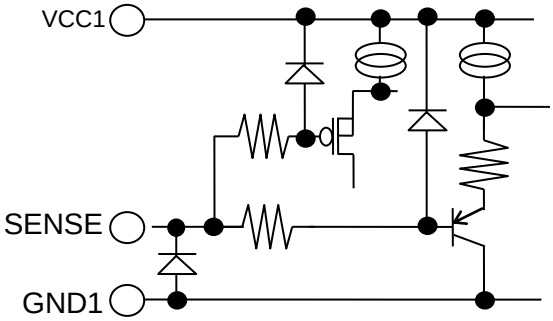
I/O Equivalence Circuit - continued

Pin No.	Pin Name / Pin Function	Input Output Equivalence Circuit Diagram
21	FLT Fault output	
26	RDY Ready output	
27	BISTOUT BIST result output	
22	ENA Gate drive control enable input	
23	INA Gate drive control input A	
29	BISTON Input for checking BIST result	
30	ASC Active Short Circuit input	

I/O Equivalence Circuit - continued

Pin No.	Pin Name / Pin Function	Input Output Equivalence Circuit Diagram
24	INB Gate drive control input B	
25	OSFB Output state feedback	
3	FB Output side voltage feedback	

I/O Equivalence Circuit - continued

Pin No.	Pin Name / Pin Function	Input Output Equivalence Circuit Diagram
33	COMP Charge Pump output	
32	RT Switching frequency setting	
37	FET_G Output for control external MOSFET driving trans	
35	SENSE Current Sense input	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

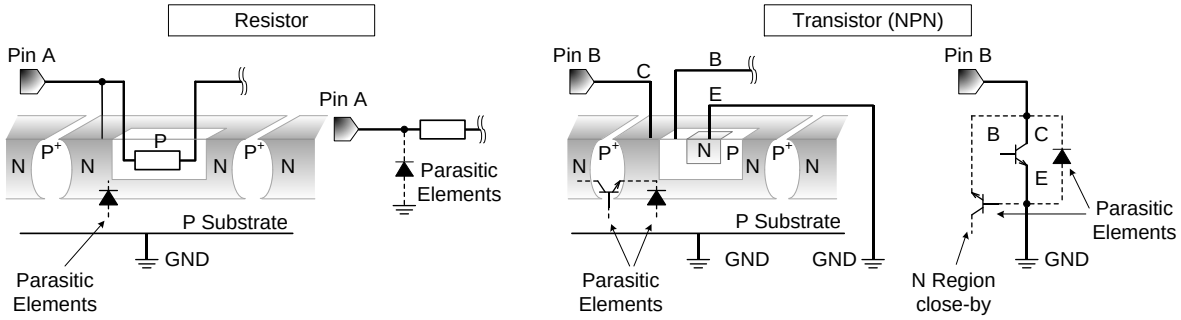


Figure 48. Example of IC Structure

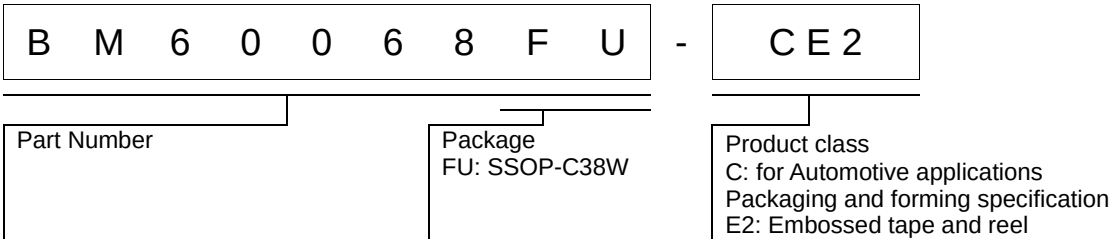
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

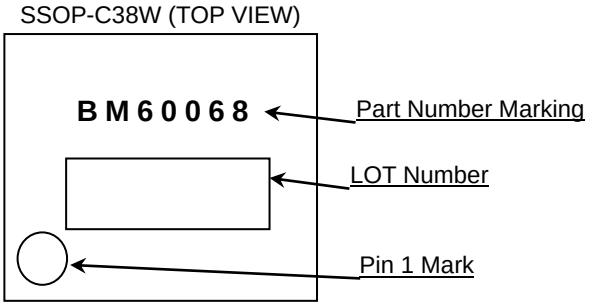
12. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

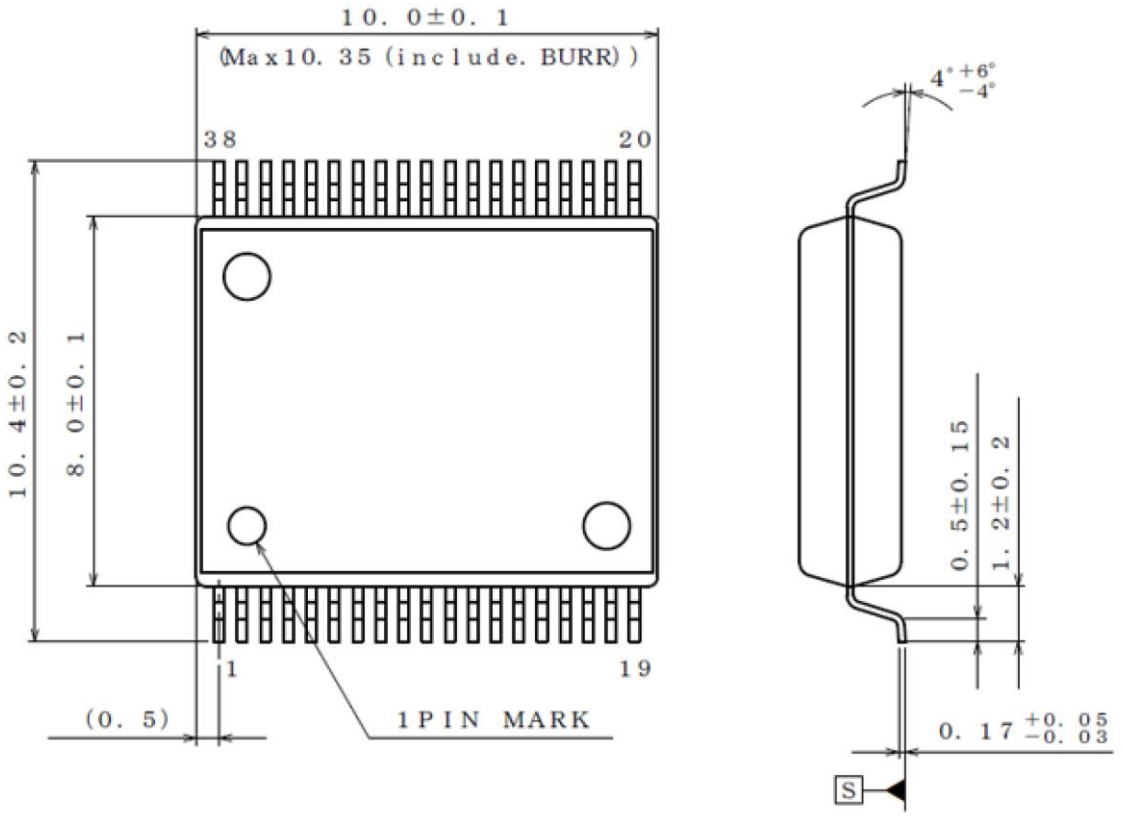


Marking Diagram



Physical Dimension and Packing Information

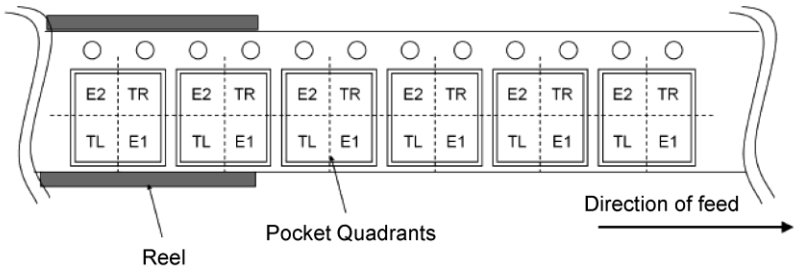
Package Name	SSOP-C38W



(UNIT : mm)

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
12.Apr.2024	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.