Target Spec

Single-Channel Ultra-Fast Gate Driver

BD2312GWL-LB

General Description

This product is a rank product for the industrial equipment market. This is the best product for use in these applications.

BD2312GWL-LB is a single gate driver capable of driving GaN HEMTs at Ultra-Fast with narrow pulses, which can contribute to the long-range and high accuracy of LiDAR. It can supply 7 A output current in a small 6-pin WLCSP package. As a protection function, the driver includes an Undervoltage Lockout (UVLO) between VCC and GND.

Features

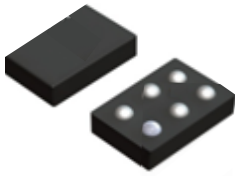
- Gate Driver Voltage Range 4.5 V to 5.5 V
- Minimum Input Pulse Width 1.25 ns (220 pF load)
- Typical Rise Time 0.65 ns (220 pF load)
- Typical Fall Time 0.70 ns (220 pF load)
- Built-in Undervoltage Lockout (UVLO) between VCC and GND
- Inverting and Non-inverting Inputs
- CSP Package UCSP50L1C (6Pin)

Key Specifications

- Gate Driver Voltage Range: 4.5 V to 5.5 V
- Output Current I_{OH} / I_{OL}: 7 A / 5 A (Typ)
- Turn-on / Turn-off Delay Time: 3.4 ns / 3.0 ns (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

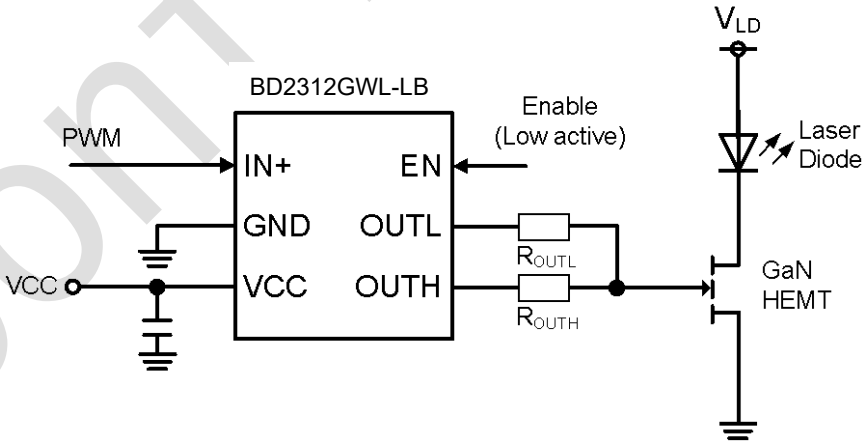
	W (Typ) x D (Typ) x H (Max)
UCSP501L1C(6pin)	0.8 mm x 1.2 mm x 0.57 mm



Applications

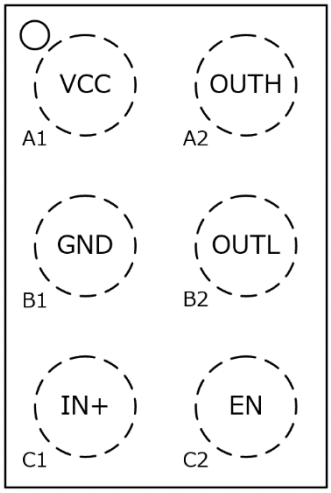
- Industrial Equipment
- Industrial LiDAR
- DC / DC Converters
- Industrial Detection Sensor
- Augmented Reality

Typical Application Circuit



Pin Configuration

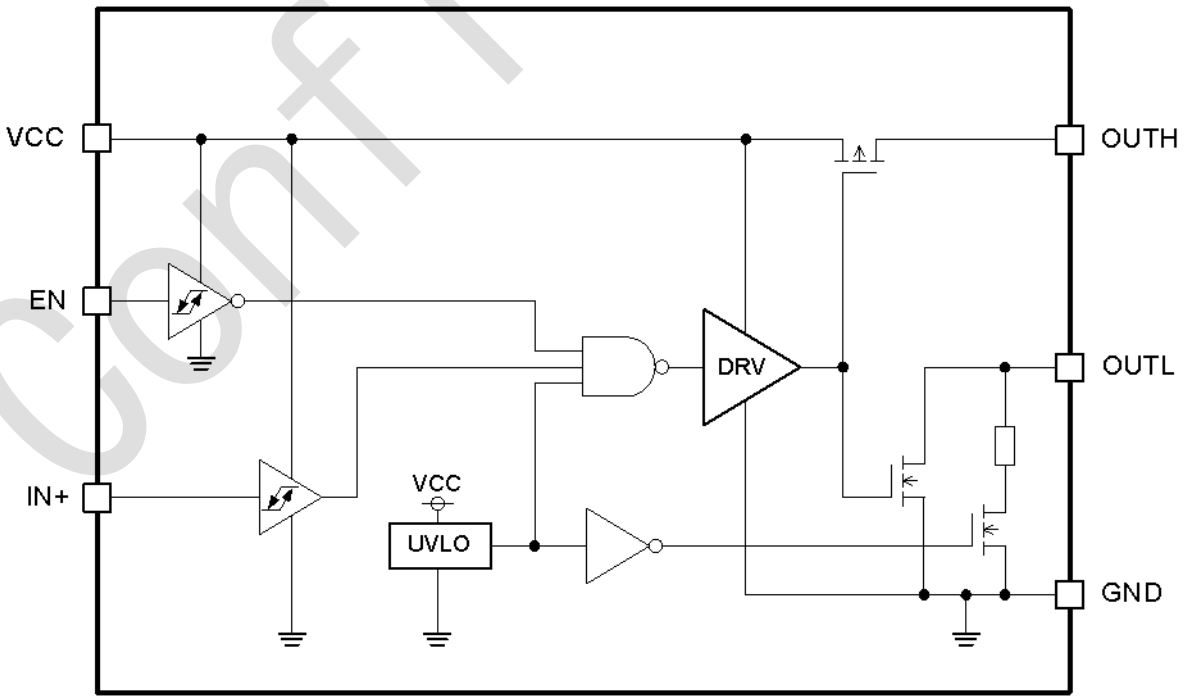
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
A1	VCC	Power supply.
A2	OUTH	Pull-up gate drive output.
B1	GND	Ground.
B2	OUTL	Pull-down gate drive output.
C1	IN+	Logic input pin.
C2	EN	Enable pin. (Low active)

Block Diagram



Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	-0.3 to +6.5	V
Input Voltage (IN+)	V_{IN+}	-5.0 to +7.0	V
Input Voltage (EN)	V_{EN}	-5.0 to +7.0	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 3)*	
UCSP50L1C				
Junction to Ambient	θ_{JA}	T.B.D.	T.B.D.	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	T.B.D.	T.B.D.	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-9.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.5 mm x 101.5 mm x 1.6 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	52.5 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.5 mm x 101.5 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	52.5 µm	99.5 mm x 99.5 mm	35 µm	99.5 mm x 99.5 mm	52.5 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Input Voltage (IN+)	V_{IN+}	-0.3	-	VCC	V
Input Voltage (EN)	V_{EN}	-0.3	-	VCC	V
Operating Temperature	Topr	-40	+25	+125	°C

Electrical Characteristics (Unless otherwise specified VCC = 5 V, Tj = -40 °C to +125 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current						
VCC Operating Current	I_{CC}	-	38.7	46.0	mA	30 MHz (50 % duty), 2 Ω as R_{OUTH} and R_{OUTL}, 100 pF load
VCC Shutdown Current	I_{CCSHD}	-	0.61	1.00	mA	V_{IN+} = V_{EN} = 0 V
Undervoltage Lockout (UVLO)						
UVLO Detect Threshold Voltage	V_{UVDOWN}	2.9	3.6	4.3	V	VCC falling
UVLO Reset Threshold Voltage	V_{UVUP}	3.1	3.9	4.5	V	VCC rising
UVLO Hysteresis Voltage	V_{UV_HYS}	-	0.3	-	V	
Input						
IN+, EN Pin High Threshold Voltage	V_{IH}	1.7	2.1	-	V	
IN+, EN Pin Low Threshold Voltage	V_{IL}	-	1.3	1.8	V	
Hysteresis Voltage	V_{HYS}	-	0.8	1.0	V	
Output						
Peak Source Current	I_{OH}	-	7	-	A	
Peak Sink Current	I_{OL}	-	5	-	A	
Turn-on Propagation Delay Time	t_{ON}	-	3.4	5.0	ns	100 pF load
Turn-off Propagation Delay Time	t_{OFF}	-	3.0	4.6	ns	100 pF load
Output Rise Time	t_R	-	0.65	-	ns	0 Ω series 220 pF load
Output Fall Time	t_F	-	0.70	-	ns	0 Ω series 220 pF load
Minimum Input Pulse Width	t_{INMIN}	-	1.25	-	ns	0 Ω series 220 pF load

Typical Performance Curves

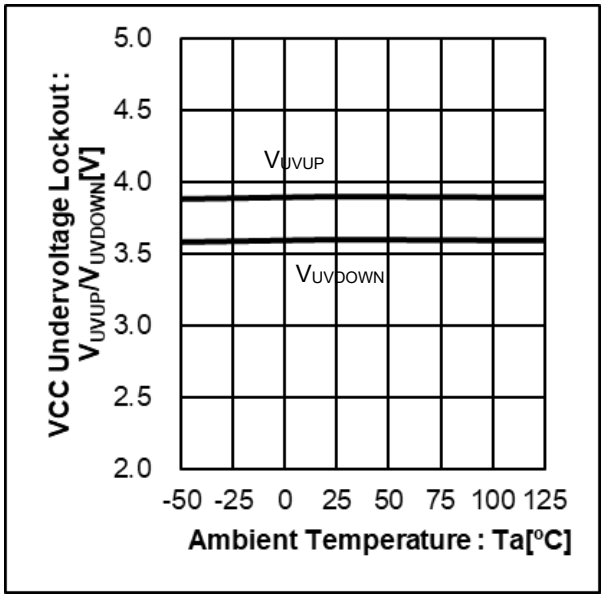


Figure 1. VCC Undervoltage Lockout vs Ambient Temperature
(VCC = 5 V, 2 Ω as ROUTH and ROUTL, 100 pF load)

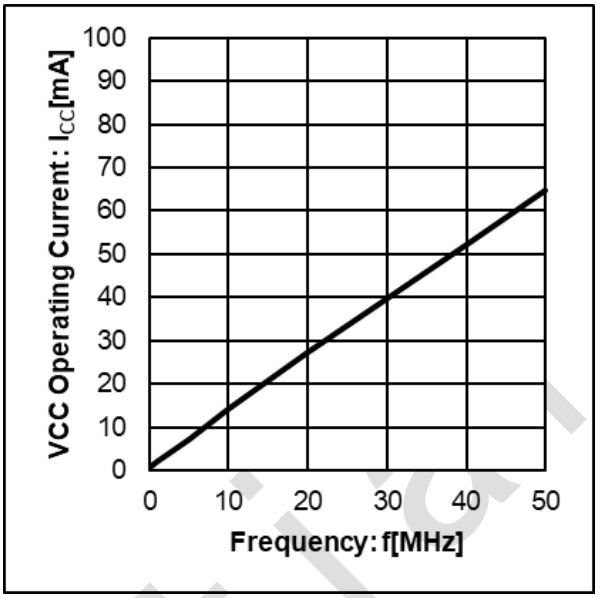


Figure 2. VCC Operating Current vs Frequency
(VCC = 5 V, 2 Ω as ROUTH and ROUTL, 100 pF load)

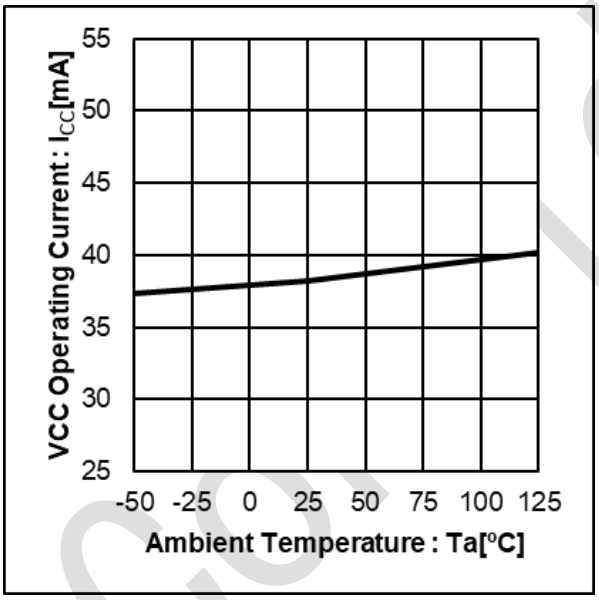


Figure 3. VCC Operating Current vs Ambient Temperature
(VCC = 5 V, 2 Ω as ROUTH and ROUTL, 100 pF load)

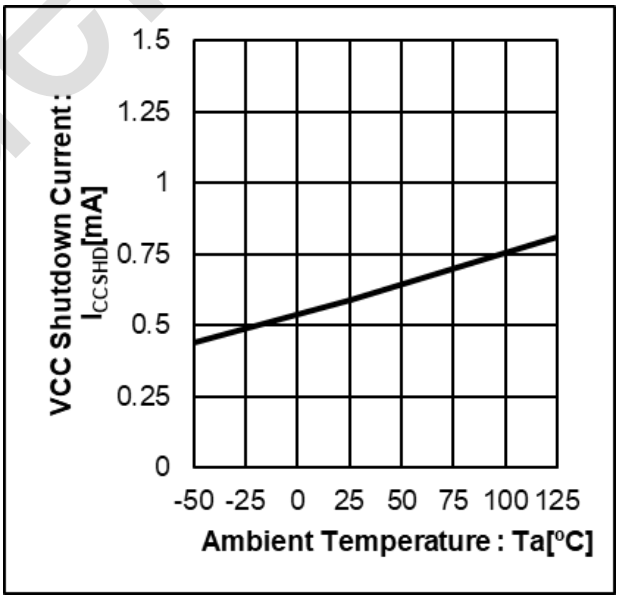


Figure 4. VCC Shutdown Current vs Ambient Temperature
(VCC = 5 V, VIN+ = VEN = 0 V)

Typical Performance Curves – continued

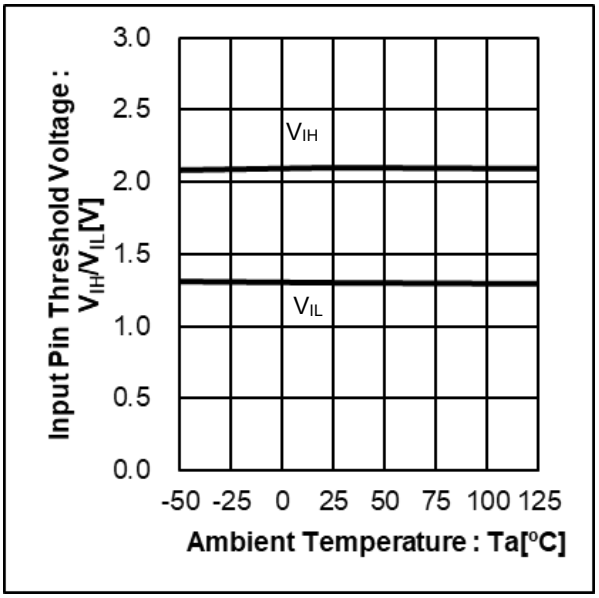


Figure 5. Input Pin Threshold Voltage vs Ambient Temperature

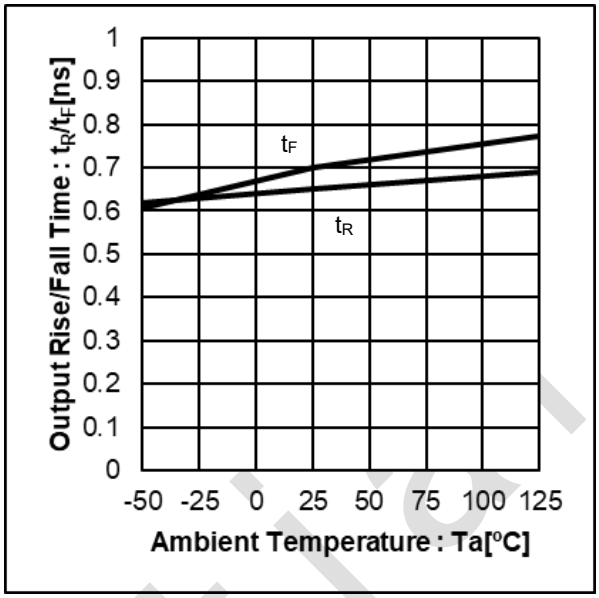


Figure 6. Output Rise/Fall Time vs Ambient Temperature
(VCC = 5 V, 0 Ω as R_{OUTH} and R_{OUTL}, 220 pF load)

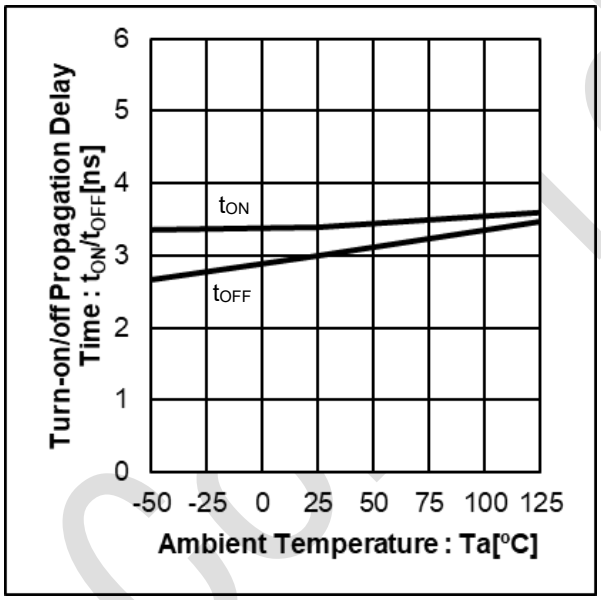


Figure 7. Turn-on/off Propagation Delay Time vs Ambient Temperature
(VCC = 5 V, 0 Ω as R_{OUTH} and R_{OUTL}, 100 pF load)

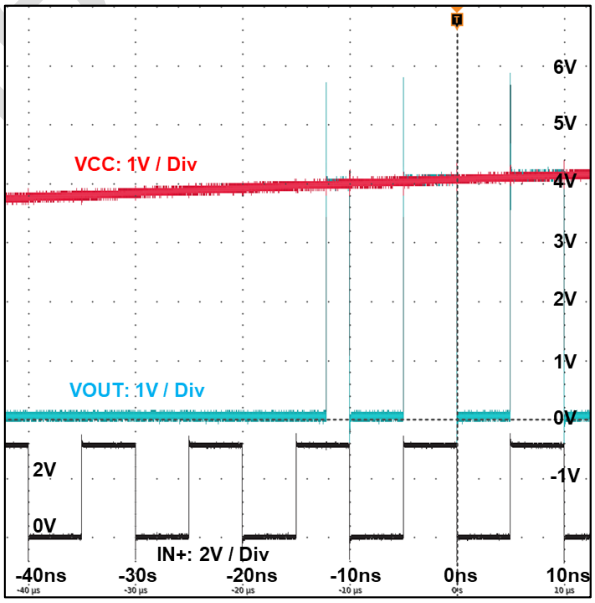


Figure 8. Startup Time
(0 Ω as R_{OUTH} and R_{OUTL}, 220 pF load)

Typical Performance Curves – continued

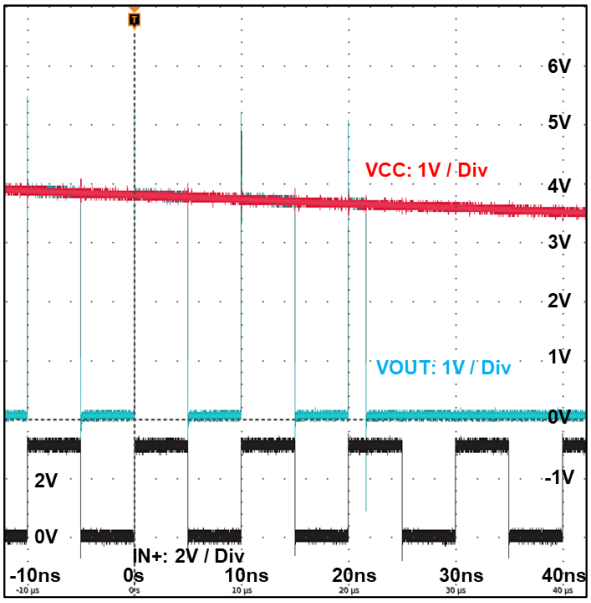


Figure 9. Shutdown Time
(0 Ω as R_{OUTH} and R_{OUTL}, 220 pF load)

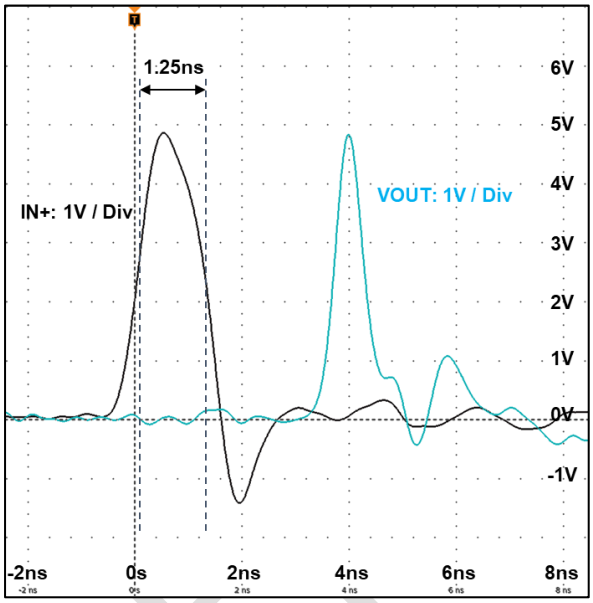


Figure 10. Minimum Input Pulse Width
(VCC = 5 V, 0 Ω as R_{OUTH} and R_{OUTL}, GNE1040TB)

Timing Chart

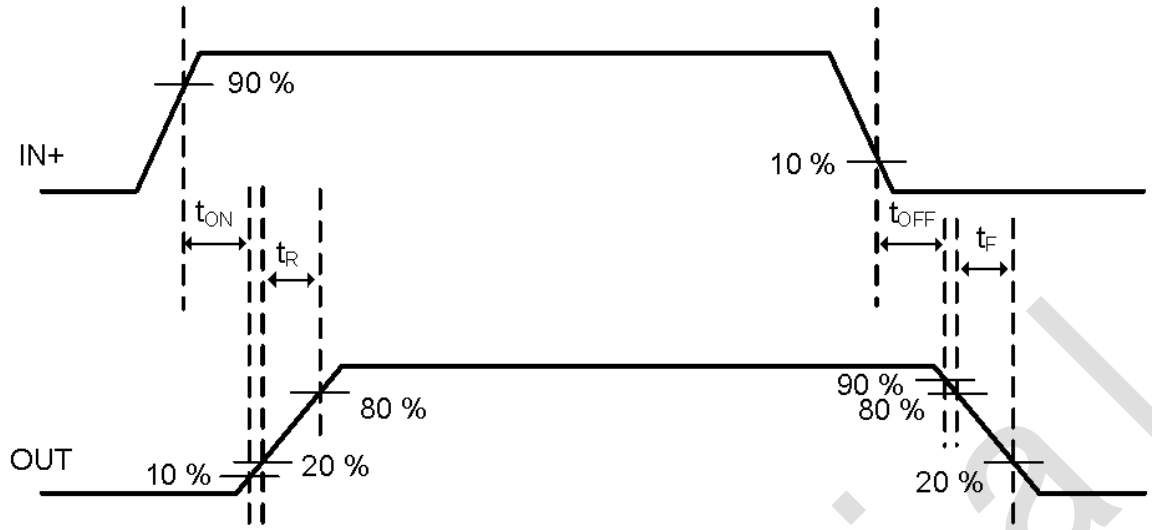


Figure 11. Timing Chart

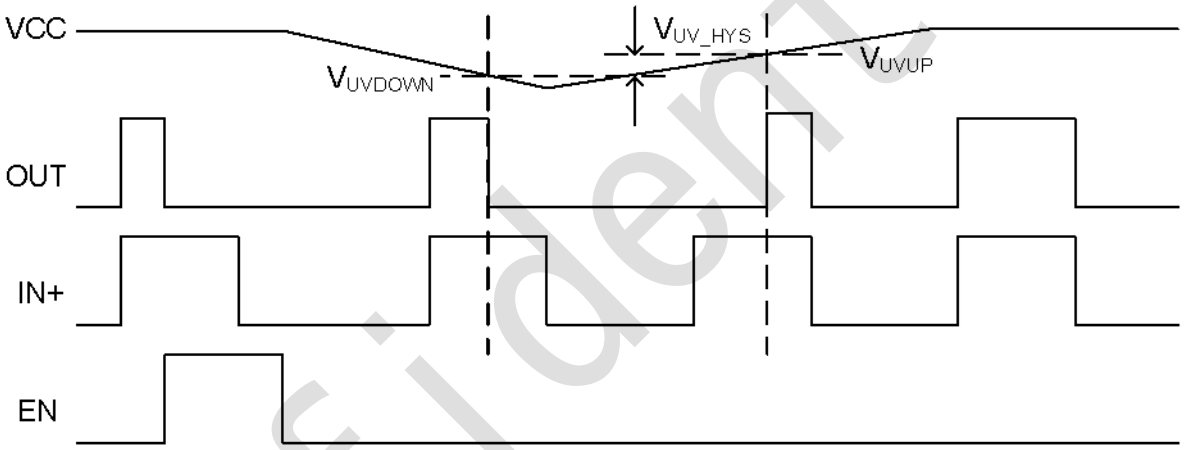


Figure 12. UVLO Timing Chart

Function Table

Table 1. The device will operate in following mode when in UVLO state.

IN+	EN	OUTH	OUTL
X(Note 6)	X(Note 6)	OPEN	L

(*Note 6*) X is not dependent on the value.

Table 2. The device will operate in following mode when not in UVLO state.

IN+	EN	OUTH	OUTL
L	L	OPEN	L
H	L	H	OPEN
L	H	OPEN	L
H	H	OPEN	L

Application Components Selection Method

(1) Gate Resistor

The gate resistor $R_{G(ON/OFF)}$ is selected to the switching speed of the power device. The switching time (t_{SW}) is defined as the time spent to reach the end of the plateau voltage, so the turn-on gate resistor $R_{G(ON)}$ can be calculated using the following formulas.

$$I_G = \frac{Q_{gs}+Q_{gd}}{t_{SW}} \quad [1]$$

$$R_{TOTAL(ON)} = R_{PON} + R_{G(ON)} = \frac{VCC-V_{GS(TH)}}{I_G} \quad [2]$$

$$t_{SW} = \frac{Q_{gs}+Q_{gd}}{I_G} = \frac{(Q_{gs}+Q_{gd})(R_{PON}+R_{G(ON)})}{(VCC-V_{GS(TH)})} \quad [3]$$

Where:

I_G is the gate current of the power device.

Q_{gs} is the charge between gate and source of the power device.

Q_{gd} is the charge between gate and drain of the power device.

$V_{GS(TH)}$ is the threshold voltage of the power device.

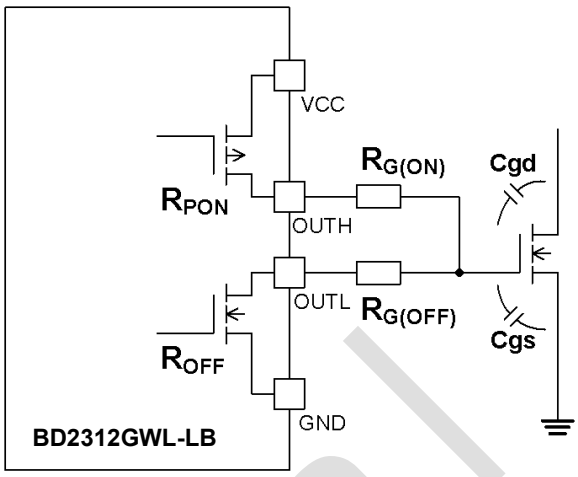


Figure 13. Gate Driver Equivalent Circuit

The turn-on gate resistance can be changed to control output slew rate (dV_D/dt). The slew rate of the power device is determined by the following equation.

$$\frac{dV_D}{dt} = \frac{I_G}{C_{rss}} \quad [4]$$

where:

C_{rss} is the feedback capacitance.

The gate resistance is determined as follows by substituting equation [4] into equation [2].

$$R_{TOTAL(ON)} = R_{PON} + R_{G(ON)} = \frac{VCC-V_{GS(TH)}}{C_{rss}\times\frac{dV_D}{dt}} \quad [5]$$

$$R_{G(ON)} = \frac{VCC-V_{GS(TH)}}{C_{rss}\times\frac{dV_D}{dt}} - R_{PON} \quad [6]$$

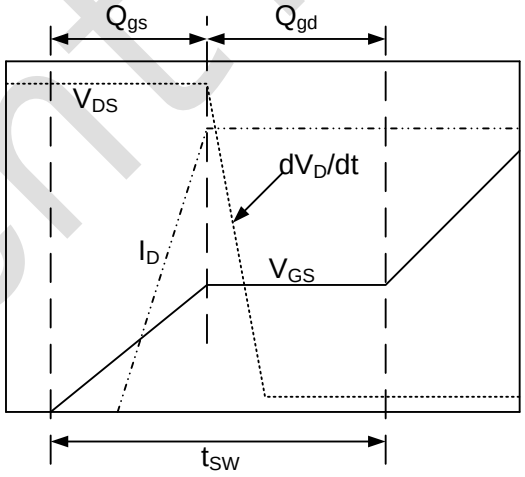


Figure 14. Gate Charge Transfer Characteristics

When other power devices are turned on, current flows in the power device which is off through Cgd. At this point, the gate resistance ($R_{G(OFF)}$) should be set so that the gate voltage does not exceed the threshold of the power device and turn on the power device itself.

$$V_{GS(TH)} \geq \left(R_{NOFF} + R_{G(OFF)}\right) \times I_G = \left(R_{NOFF} + R_{G(OFF)}\right) \times C_{gd} \times \frac{dV_D}{dt} \quad [7]$$

$$R_{G(OFF)} \leq \frac{V_{GS(TH)}}{C_{gd}\times\frac{dV_D}{dt}} - R_{NOFF} \quad [8]$$

Application Components Selection Method – continued

(2) Input Capacitor

A low-ESR ceramic capacitor should be used near the VCC pin to reduce input ripple voltage. In considering of the DC bias characteristic, it is recommended 0.5 µF or more between VCC and GND.

PCB Layout

The voltage of VCC pin may be risen by the parasitic inductance of the PCB and the internal interconnection in the IC.
The mechanism by which VCC voltage rises is Figure 15.

(1) When the signal with short pulse width is input as an input signal, it is turned off in the state that Pch-FET of the final stage is turned on and flows current.
(2) When Pch-FET is turned off while current is flowing, VCC voltage is risen by the parasitic inductance.

When VCC voltage is risen and over absolute maximum ratings, it can damage the IC.
To reduce the rising of VCC voltage, please locate a ceramic capacitor which is low-ESR near the VCC pin and the GND pin, and connect it so that parasitic inductance L_{VCC} and L_{GND} in the PCB becomes small. It is recommended 1 nH or less each L_{VCC} and L_{GND}.

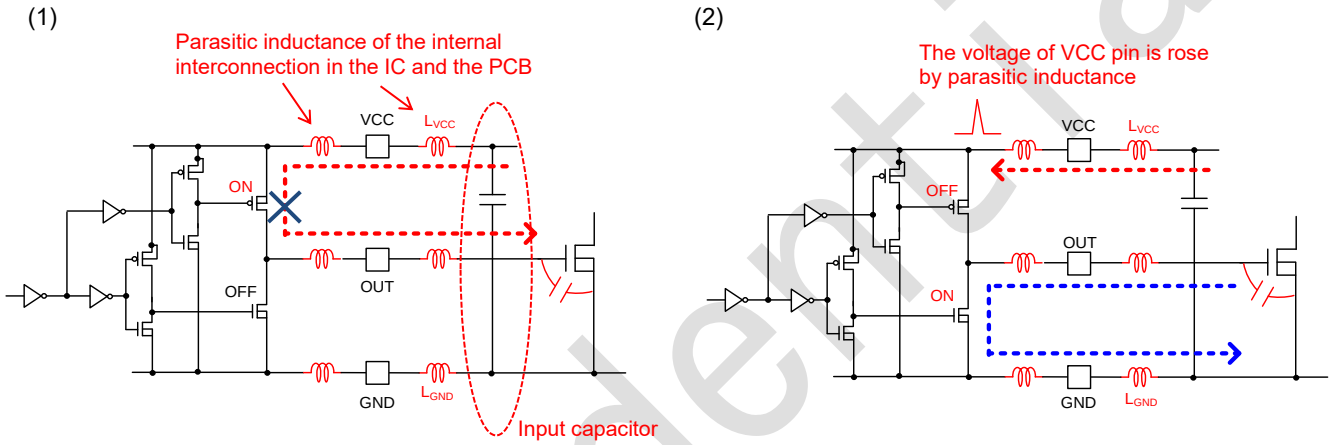
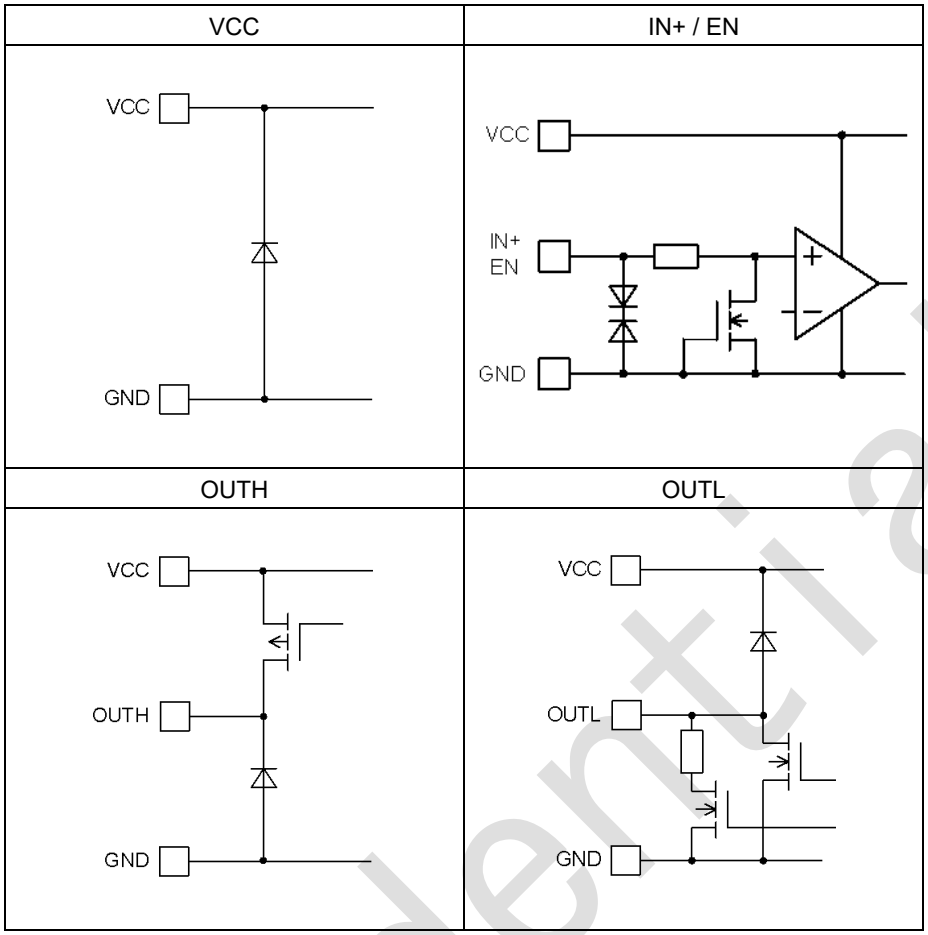


Figure 15. Mechanism of Overshoot

I/O Equivalence Circuits



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

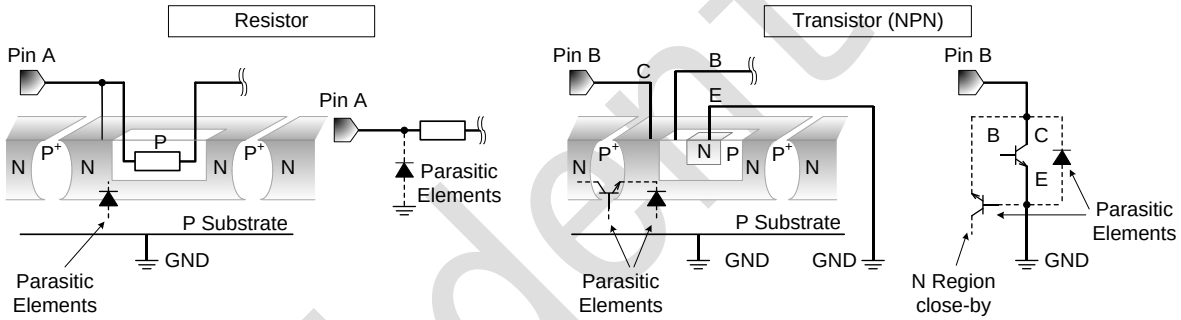


Figure 16. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

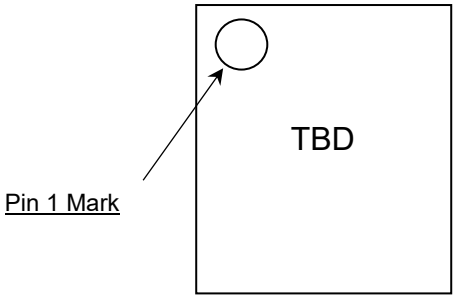
B	D	2	3	1	2	G	W	L	-	LB TR

Package
NVX: UCSP501L1C

Product Class
LB: for Industrial Applications
Packaging and Forming Specification
TR: Embossed Tape and Reel

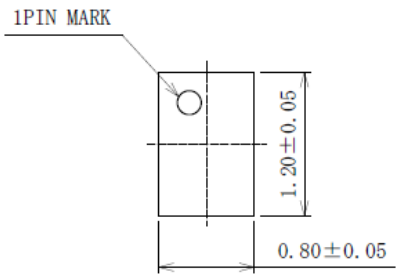
Marking Diagram

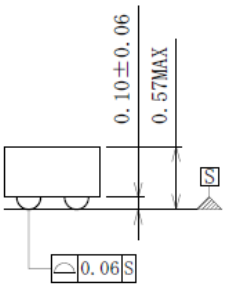
UCSP501L1C (TOP VIEW)

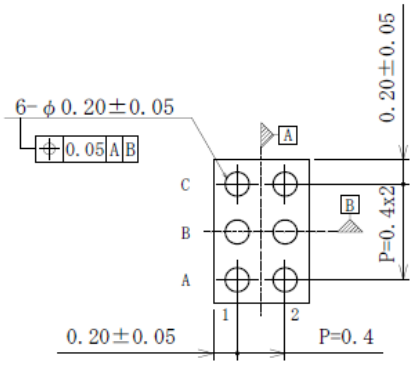


Physical Dimension and Packing Information

Package Name	UCSP501L1C







Revision History

Date	Revision	Changes
16.Nov.2023	001	New Release
5.Dec.2023	002	Changed pkg size on P.1
22.Dec.2023	003	Change the packaging and forming specification from E2 to TR on P.14 Change the marking diagram to TBD on P.14

General Precaution

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