High-efficiency 36 V Withstand Voltage Stepping Motor Drive

BD65520MUV

General Description

BD65520MUV is a 36 V power supply rated, 2.0 A output current rated, low-consumption bipolar PWM constant current driven High-efficiency Driver. The input interface adopts the CLK-IN drive system, and the excitation mode supports FULL STEP to 1/32 STEP mode via a built-in DAC. FAST / SLOW DECAY of current decay mode ratio linear variable freely. Pin settings and detailed settings by SPI are set to make an optimum current control possible according to the load of every motor for a High-efficiency Drive. In addition, the power supply may also be driven by a single system, contributing to a simple set design.

Features

- Built-in High-efficiency Drive Mode (Drive Current Value Output Function, High-efficiency Drive Setting Function)
- Motor Load Status Output Function
- Pin Setting Mode / SPI Setting Mode
- Detailed Setting Function by SPI Input
- Output Current Rating (DC) 2.0 A
- Low ON Resistance DMOS Output
- CLK-IN Drive System
- PWM Constant Current Control (Other Oscillation)
- Built-in Spike Noise Blanking Function (No external Noise Filter required)
- FULL STEP to 1/32 STEP Compatible
- Excitation Mode Switching Free Timing
- Current Decay Mode Switching Function (FAST DECAY / SLOW DECAY Ratio Linear Variable (MIX DECAY))
- Current Decay Mode Optimization Function (AUTO DECAY)
- Forward / Reverse Switching Function
- Power Save Function
- Built-in Logic Input Pull-down Resistor
- Power ON Reset Function
- Temperature Protection Circuit (TSD)
- Overcurrent Protection Circuit (OCP)
- Low Voltage Malfunction Prevention Function (UVLO)
- Overvoltage Output OFF Function (OVLO)
- Malfunction Prevention Function if no power applied (“Ghost Supply Prevention” function)
- Protection Status Output Function
- Adjacent Pin Short Protection
- Ultra-compact, Ultra-thin, High Heat Dissipation (Backside Heat Dissipation) Package

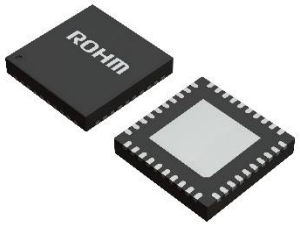
Application

- PPC, Multifunction Printer, Laser Beam Printer, Inkjet Printer, Surveillance Camera, WEB Camera, Sewing Machine, Photo Printer, Fax, Scanner, Mini Printer, Toy, Robot

Key Specifications

- Power Supply Voltage Range: 8 V to 28 V
- Rated Output Current (Continuous): 2.0 A/Phase
- Rated Output Current (Peak value): 2.5 A/Phase
- Operating Temperature Range: -25 °C to +85 °C
- Output ON Resistance (Total upper and lower) : 0.55 Ω (Typ)

Package	W (Typ) x D (Typ) x H (Max)
VQFN040V6060	6.0 mm x 6.0 mm x 1.0 mm



Typical Application Circuit

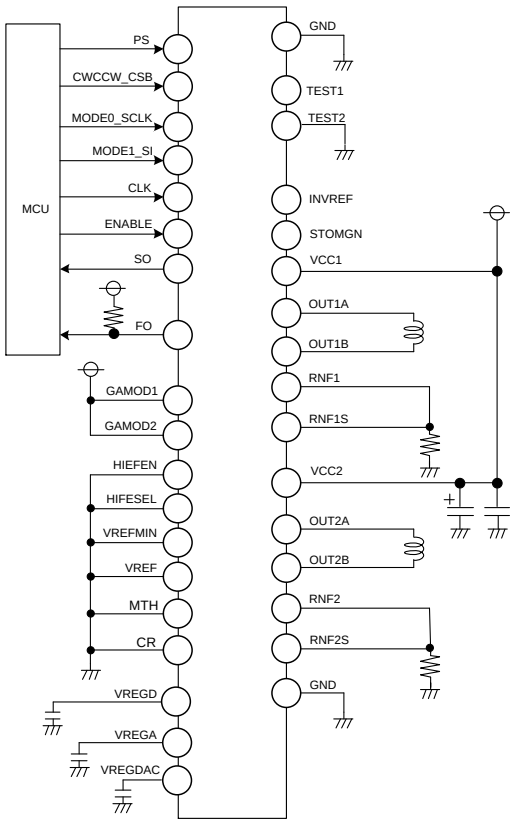


Figure 1. Application Circuit Diagram (SPI Setting Mode)

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Pin Configuration

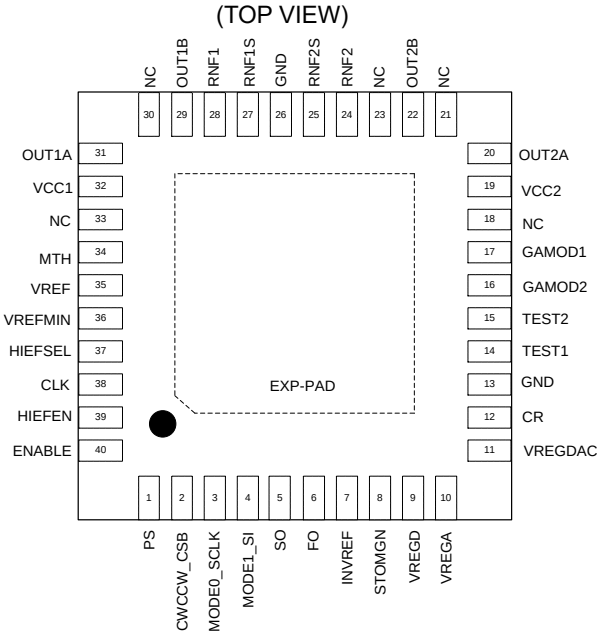


Figure 2. Pin Layout Diagram

Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	PS	Power save pin	21	NC	No connection
2	CWCCW_ CSB	Motor rotation direction setting pin *(Note 1)* Chip select input pin *(Note 2)*	22	OUT2B	H bridge output pin
3	MODE0_ SCLK	Motor excitation mode setting pin *(Note 1)* Serial clock input pin *(Note 2)*	23	NC	No connection
4	MODE1_SI	Motor excitation mode setting pin *(Note 1)* Serial data input pin *(Note 2)*	24	RNF2	Output current detection resistor connection pin
5	SO	Serial data output pin	25	RNF2S	Current detection comparator input pin
6	FO	Protect status output pin	26	GND	Ground pin
7	INVREF	Internal VREF output pin	27	RNF1S	Current detection comparator input pin
8	STOMGN	Step-out margin output pin	28	RNF1	Output current detection resistor connection pin
9	VREGD	1.5 V Regulator output pin	29	OUT1B	H bridge output pin
10	VREGA	5 V Regulator output pin	30	NC	No connection
11	VREGDAC	DAC 5 V Regulator output pin	31	OUT1A	H bridge output pin
12	CR	Chopping frequency setting pin *(Note 3)*	32	VCC1	Power pin
13	GND	Ground pin	33	NC	No connection
14	TEST1	Test pin (Set OPEN)	34	MTH	Current decay mode setting pin *(Note 3)*
15	TEST2	Test pin (Use while connected with GND)	35	VREF	Output current value setting pin *(Note 3)*
16	GAMOD2	High-efficiency Drive gain setting pin	36	VREFMIN	Output current value lower limit setting pin *Note 3)*
17	GAMOD1	High-efficiency Drive gain setting pin	37	HIEFSEL	High-efficiency Drive setting pin *(Note 3)*
18	NC	No connection	38	CLK	Phase-advancing clock input pin
19	VCC2	Power supply pin	39	HIEFEN	High-efficiency Drive enable pin *(Note 4)*
20	OUT2A	H bridge output pin	40	ENABLE	Output enable pin
-	EXP-PAD	Connect the EXP-PAD to GND			

(Note 1) Function in pin setting mode.
(Note 2) Function in SPI setting mode.
(Note 3) Not used in SPI setting mode. Connect with GND.
(Note 4) Not used in SPI setting mode. Open or connect to GND.

Block Diagram

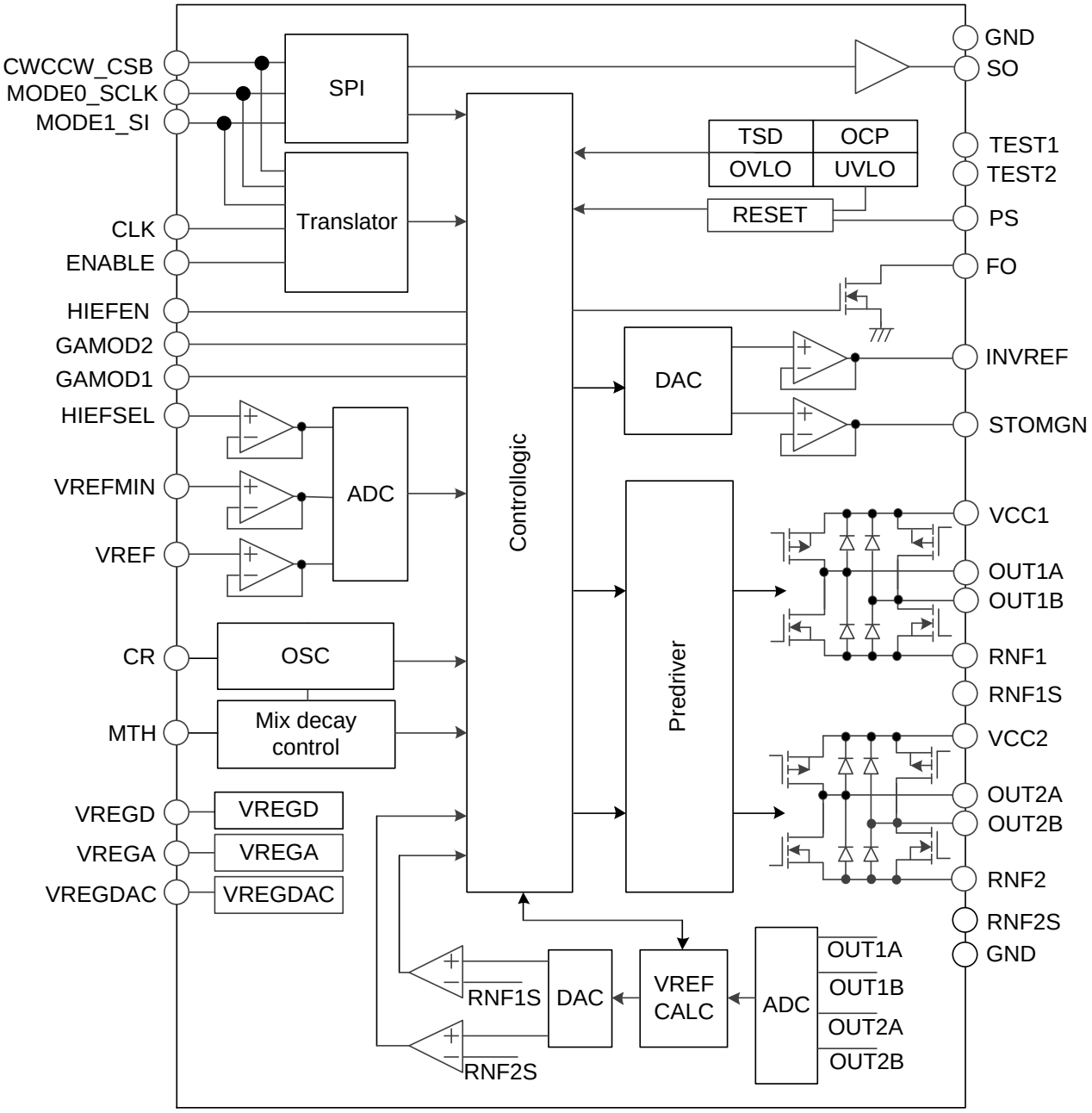


Figure 3. BD65520MUV Block Diagram

Absolute Maximum Rating (Ta = 25 °C)

Parameters	Symbol	Rating	Unit
Supply Voltage	V_{CC1}, V_{CC2}	-0.2 to +36.0	V
Input Voltage for Control Pin	V_{IN}	-0.2 to +5.5	V
RNF Maximum Voltage	V_{RNF}	0.7	V
Output Current (Continuous)	I_{OUT}	2.0*(Note 1)*	A/Phase
Output Current (Peak) *(Note 2)*	$I_{OUTPEAK}$	2.5*(Note 1)*	A/Phase
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Do not exceed Tjmax = 150 °C.
(Note 2) Pulse width tw ≤ 2 ms, duty 20 %.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded, the rise in temperature of chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Recommended Operating Condition

Parameters	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-25	+25	+85	°C
Supply Voltage	V_{CC1}, V_{CC2}	8	24	28	V
Maximum Output Current (Continuous)	I_{OUT}	0*(Note 3)*	1.0*(Note 3)*	2.0*(Note3)*	A/Phase

(Note 3) Must not exceed Tjmax = 150 °C.

Thermal Resistance *(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 6)*	2s2p*(Note 7)*	
VQFN040V6060				
Junction to Ambient	θ_{JA}	85.2	30.5	°C/W
Junction to Top Characterization Parameter*(Note 5)*	Ψ_{JT}	8	5	°C/W

(Note 4) Based on JESD51-2A (Still-Air), using a BD65520MUV Chip.
(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 6) Using a PCB board based on JESD51-3.
(Note 7) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 8)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 8) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, V_{CC1}, V_{CC2} = 24 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
[General]						
Circuit Current at Standby	I_{CCST}	-	-	10	μA	PS = L
Circuit Current	I_{CC}	-	10	25	mA	PS = H, VREF = 2.5 V
[Control Input] (PS, ENABLE, CLK, CWCCW_CSB, MODE0_SCLK, MODE1_SI, GAMOD1, GAMOD2, HIEFEN)						
H Level Input Voltage	V_{INH}	2.0	-	-	V	
L Level Input Voltage	V_{INL}	-	-	0.8	V	
H Level Input Current	I_{INH}	35	50	100	μA	V_{IN} = 5 V
L Level Input Current	I_{INL}	-10	0	-	μA	V_{IN} = 0 V
[Output] (OUT1A, OUT1B, OUT2A, OUT2B)						
Output ON Resistor	R_{ON}	-	0.55	0.85	Ω	I_{OUT} = ±1.0 A (Top/Bottom Total)
Output MOS Leak	I_{LEAK}	-	-	10	μA	V_{OUT} = 24 V
Output Inflow Current	I_{OUTR}	-	120	200	μA	V_{OUT} = 24 V
[Current Control Unit]						
RNF_XS Inflow Current*(Note1)*	I_{RNFS}	-2.0	-0.1	-	μA	RNF_XS = 0 V
RNF_X Inflow Current*(Note1)*	I_{RNF}	-80	-40	-	μA	RNF_X = 0 V
VREF Inflow Current	I_{VREF}	-2.0	-0.1	-	μA	VREF = 0 V
VREF Input Voltage Range	V_{VREF}	0	-	3.0	V	
MTH Inflow Current	I_{MTH}	-2.0	-0.1	-	μA	MTH = 0 V
MTH Input Voltage Range	V_{MTH}	0	-	3.5	V	
Minimum ON Time (Blank Time)	t_{ONMIN}	0.5	1.2	1.7	μs	C = 1000 pF, R = 39 kΩ
Comparator Threshold	V_{CTH}	0.573	0.600	0.627	V	VREF = 3.0 V
Comparator Threshold 1phase/2phase difference	V_{dcTH}	-0.27	0	+0.27	V	VREF = 3.0 V, OUT1 comparator Threshold - OUT2 comparator Threshold
[Regulator Output]						
VREGA Output Voltage	V_A	-	5.0	-	V	
VREGD Output Voltage	V_D	-	1.5	-	V	
VREGDAC Output Voltage	V_{DAC}	-	5.0	-	V	

(Note 1) x = 1, 2

Electrical Characteristics – Continued

(Unless otherwise specified, Ta = 25 °C, V_{CC1}, V_{CC2} = 24 V)

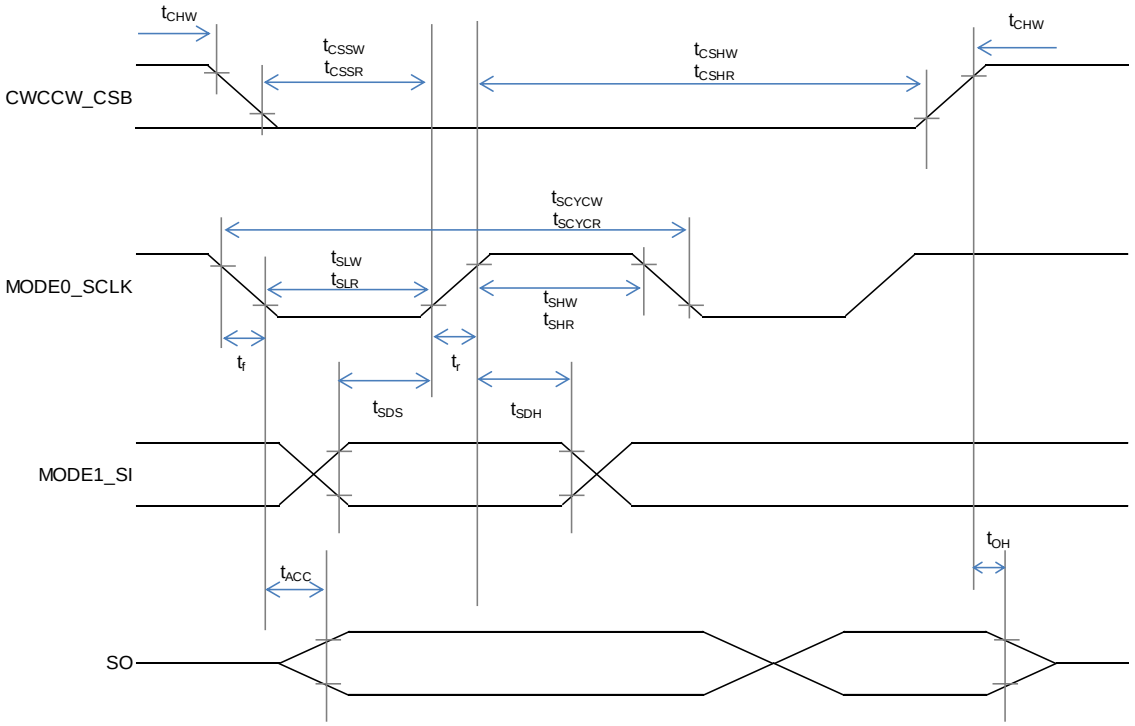
Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
[High-efficiency Drive Setting]						
VREFMIN Inflow Current	$I_{VREFMIN}$	-2.0	-0.1	-	µA	VREFMIN = 0 V
VREFMIN Input Voltage Range	$V_{VREFMIN}$	0	-	3.0	V	
HIEFSEL Inflow Current	$I_{HIEFSEL}$	-2.0	-0.1	-	µA	HIEFSEL = 0 V
HIEFSEL Input Voltage Range	$V_{HIEFSEL}$	0	-	3.99	V	
[Analog Output]						
INVREF Output Voltage	V_{INVREF}	0.95	1.00	1.05	V	I_{LOAD} = 0 mA, VREGDAC = 5 V, GAMOD1 = 5 V, GAMOD2 = 5 V VREFSET = 1.00
STOMGN Output Voltage	V_{STOMGN}	3.90	4.00	4.10	V	I_{LOAD} = 0 mA, VREGDAC = 5 V, OUT1A = 4 V, OUT1B = 0 V, (When OUT1-side is OPEN)
[FO Output]						
Output L Voltage	V_{OLF}	-	0.05	0.10	V	I_{LOAD} = -1 mA
Output Leak Current	I_{FO_LEAK}	-	-	10	µA	
[SO Output]						
Output H Voltage	V_{OHS}	V_A-0.2	V_A-0.1	-	V	I_{LOAD} = +1 mA
Output L Voltage	V_{OLS}	-	0.1	0.2	V	I_{LOAD} = -1 mA
Output Leak Current	I_{OS}	-	-	10	µA	

Electrical Characteristics - Continued

(Unless otherwise specified, Ta = 25 °C, V_{CC1}, V_{CC2} = 24 V)

Signal	Symbol	Parameter	Min	Typ	Max	Unit	Comment
CWCCW_CSB	t_{CHW}	CSX "H" Pulse Width	400	-	-	ns	
	t_{CSSW}	CSX-SCL Time (Write)	200	-	-	ns	
	t_{CSHW}		200	-	-	ns	
	t_{CSSR}	CSX-SCL Time (Read)	600	-	-	ns	
	t_{CSHR}		600	-	-	ns	
MODE0_SCLK (Write)	t_{SCYCW}	Serial Clock Cycle	1000	-	-	ns	
	t_{SHW}	SCL "H" Pulse Width	500	-	-	ns	
	t_{SLW}	SCL "L" Pulse Width	500	-	-	ns	
MODE0_SCLK (Read)	t_{SCYCR}	Serial Clock Cycle	2000	-	-	ns	
	t_{SHR}	SCL "H" Pulse Width	1000	-	-	ns	
	t_{SLR}	SCL "L" Pulse Width	1000	-	-	ns	
MODE1_SI	t_{SDS}	Data Setup Time	200	-	-	ns	
	t_{SDH}	Data Hold Time	200	-	-	ns	
SO	t_{ACC}	Access Time	-	-	1000	ns	Max Condition: CL = 30 pF Min Condition: CL = 8 pF
	t_{OH}	Output Disable Time	100	-	-	ns	

Caution 1: t_r and t_f (signal rise/fall) should be at 15 ns or less.



Pin Function Description

1 CLK / Phase Advance Clock Input Pin

This pin operates at rising edge. The Electrical angle advances by one for each CLK input. Motor misstep will occur if noise mixed in the CLK pin so, design the pattern in such a way that there is no noise mixing in.

2 ENABLE / Output Enable Pin

This pin forcibly turns off all output transistors (motor output OPEN). During ENABLE = L, CLK input is cut off so the phase advance operation of the internal translator circuit will stop. However, if the excitation mode (MODE0, MODE1) is switched in the ENABLE = L interval, the excitation mode when ENABLE pin returns from Low to High becomes enabled in the switched mode. Also, in the SPI setting mode, if the register setting is MODESET D5 = 1 even if at ENABLE = L, the phase advance operation will operate.

ENABLE	Motor Output
L	OPEN (electrical angle maintained)
H	ACTIVE

3 PS / Power Saving Pin

Standby mode can be set and motor output can be OPEN. When entering a standby state, the translator circuit will RESET (initialized) and the electrical angle will be initialized. Notice that after returning from standby state to normal state when PS = L becomes H, there will a delay of 1 ms (Max) until the motor output returns to the ACTIVE state.

PS	Status
L	Standby State (RESET)
H	ACTIVE

The electrical angle (initial electrical angle) for each excitation mode right after RESET shall be as follows.

Excitation Mode	Initial Electrical Angle
FULL STEP A	45°
HALF STEP A	45°
HALF STEP B	45°
QUARTER STEP A	45°
FULL STEP B	45°
HALF STEP C	45°
QUARTER STEP B	45°
1/8 STEP	45°
1/16 STEP	45°
1/32 STEP	45°

4 GAMOD1 and GAMOD2 / High-efficiency Drive Setting Select Pin and Interface Mode Setting Pin

This pin performs settings for pin setting mode and SPI setting mode.
This pin performs a High-efficiency Drive setting when in pin setting mode.

GAMOD1	GAMOD2	Interface	High-efficiency Drive Setting
L	L	Pin Setting Mode	Preset 1 (GAIN1_SET, GAIN4_SET)
H	L		Preset 2 (GAIN2_SET, GAIN5_SET)
L	H		Preset 3 (GAIN3_SET, GAIN6_SET)
H	H	SPI Setting Mode	GAIN1_SET, GAIN4_SET

This pin selects preset when in pin setting mode by GAMOD1 and GAMOD2 pin logic, and the circuit initial values of the corresponding register settings are used. Select the optimum High-efficiency Drive setting depending on the motor and load conditions.

This pin performs High-efficiency Drive setting in SPI setting mode by register setting of GAIN1_SET and GAIN4_SET.

Pin Function Description - Continued

5 MODE0_SCLK, MODE1_SI Motor Excitation Mode Setting Pin and SPI Setting Mode Input Pin

This pin sets the motor excitation mode when at pin setting mode.

MODE0_SCLK	MODE1_SI	Excitation Mode
L	L	FULL STEP
H	L	HALF STEP A
L	H	HALF SETP B
H	H	QUARTER STEP A

MODE0_SCLK pin becomes SPI clock input pin and MODE1_SI pin becomes SPI data input pin when in SPI setting mode.

For each excitation mode, refer to the timing chart and motor torque vector diagram.
This pin forcibly reflects the setting change regardless of CLK.

This pin carries out the motor excitation mode setting in the register setting when in the SPI setting mode.

6 CWCCW_CSB / Motor Rotation Direction Setting Pin and SPI Chip Select Input Pin

This pin sets the motor rotation direction when pin setting mode, and reflects the rising edge of CLK immediately after setting change.

CWCCW_CSB	Rotating Direction
L	Clockwise (CH2 current output is delay by 90° phase with respect to CH1 current)
H	Counter Clockwise (CH2 current output is advance by 90° phase with respect to CH1 current)

CWCCW_CSB is the SPI chip select input pin when in the SPI setting mode.

This pin carries out the motor rotating direction setting in the register setting when in SPI setting mode.

7 SO / SPI Setting Mode Output Pin

This is the serial data output pin when in the SPI setting mode. H Level is VA level(5 V Typ).

Open is recommended when you don't use SPI read.
SO pin is Hi-z without Read condition. So, it is recommended to attach 5 kΩ or more Pulldown resistance or Pullup resistance.

8 FO / Protection Status Output Pin

This pin outputs the status of protection with TSD, OCP, and OVLO.
The FO pin outputs L level when detects each protection function.
It is recommended to attach 5 kΩ or more Pullup resistance.

When SPI setting mode
FO pin is L level output after IC power on until READ_DIAGNOSTIC command sent.
When IC is receipt READ_DIAGNOSTIC command and TSD, OCP or OVLO are not detected, FO output is H level.

9 HIEFSEL / High-efficiency Drive Setting Pin

This pin sets the current decay ratio during High-efficiency driving in the pin setting mode.
This pin divides the values of the preset registers HIEFSELMAX (Page 58) and HIEFSELMIN (Page 59) into 16 as shown in the
following formula and the values are determined by the voltage setting of HIEFSEL.

Current Decay Ratio = HIEFSELMIN + (HIEFSELMAX – HIEFSELMIN) / 16 * n

[Relationship between n and HIEFSEL voltage setting]
n = 0: HIEFSEL = 4/16/2 = 0.125 V
n = 1: HIEFSEL = 4/16/2 + 4/16 = 0.375 V
n = 2: HIEFSEL = 4/16/2 + 4/16*2 = 0.625 V

n = 15: HIEFSEL = 4/16/2 + 4/16*15 = 3.875 V

Not used in SPI setting mode.

10 HIEFEN / High-efficiency Drive Enable Pin

This pin enables the High-efficiency Drive operation in pin setting mode.

This pin performs a High-efficiency Drive enable setting in SPI setting mode by register setting.

Pin Function Description - Continued

11 VCC1, VCC2 / Power Supply Pin

Motor drive current is flowing in this pin so wire in such a way that the wire is thick, short and has low impedance. Voltage VCC may have great fluctuation, so place a bypass capacitor (100 µF to 470 µF) as close to the pin as possible and adjust in such a way that the voltage VCC is stable. Increase the capacity if needed especially when a large current is used or those motors that have great back electromotive force are used. In addition, to lower the impedance of the power supply in a wide band, it is recommended that a multilayer ceramic capacitor of about 0.01 µF to 0.1 µF to be placed in parallel. Be careful not to exceed the rating even if the VCC voltage is instantaneous. Although VCC1 and VCC2 are shorted inside the IC, be sure to short externally VCC1 and VCC2 before using. If not shorted, the current path may be concentrated resulting in malfunction or destruction. The power supply pin has a built-in clamp element to prevent electrostatic damage. If a steep pulse signal or voltage such as a surge that exceeds the absolute maximum rating is applied, this clamp element may operate and cause damage. Therefore, never exceed the absolute maximum rating. It is also effective to attach a zener diode with an absolute maximum rating. Also, note that a diode for preventing static electricity destruction is inserted between the VCC pin and the GND pin, and if a reverse voltage is applied to the VCC pin and the GND pin, the IC may be destroyed.

12 GND / Ground Pin

In order to reduce noise due to switching current and stabilize the reference voltage inside the IC, make the impedance of the wiring from this pin as low as possible so that it has the lowest potential under any operating conditions. Also, design the pattern so that it does not have a common impedance with other GND patterns.

13 OUT1A, OUT1B, OUT2A, OUT2B / H Bridge Output Pin

Motor drive current is flowing in this pin so wire in such a way that the wire is thick, short and has low impedance. It is also effective to add a schottky diode when the output fluctuates greatly positively or negatively when using a large current such as a back electromotive force. The output pin has a built-in clamp element to prevent electrostatic breakdown. If a steep pulse signal or voltage such as a surge that exceeds the absolute maximum rating is applied, this clamp element may operate and cause damage, so never exceed the absolute maximum rating.

14 RNF1, RNF2 / Output Current Detection Resistance connection pin

Connect the resistor of 0.1 Ω to 0.3 Ω for current detection between this pin and GND. In view of the power consumption of the current-detecting resistor, determine the resistor in such a way that $W = I_{OUT}^2 \cdot R$ [W] does not exceed the power dissipation of the resistor. In addition, Wire in such a way that it has a low impedance and does not have impedance in common with other GND patterns because motor's drive current flows in the pattern through RNF pin to current-detecting resistor to GND. Do not exceed the rating because there is the possibility of circuit malfunction etc. if RNF voltage exceeds the maximum rating (0.7 V). Moreover, be careful because if RNF pin is shorted to GND, a large current will flow without normal PWM constant current control, then there is the danger that OCP or TSD will operate. Even if RNF pin is open, there is the possibility of malfunction such as no output current flowing, so do not put it in such as state.

15 RNF1S, RNF2S / Current Detection Comparator Input Pin

The RNFS pin, which is the input pin of the current detection comparator, is provided independently to reduce the decrease in current detection accuracy due to the wire impedance inside the IC of the RNF pin. Therefore, when controlling PWM constant current, be sure to connect the RNF pin and RNFS pin. Furthermore, when connecting, the decrease in current detection accuracy due to impedance in board pattern between the RNF pin and the current detection resistor can be reduced by connecting the wiring from the RNFS pin to the immediate vicinity of the current detection resistor. Also, design the pattern in consideration of wiring with less noise. Take note that if the RNF1S and RNF2S pins are short-circuited to GND, a large current may flow without normal PWM constant current control, and OCP or TSD may operate.

16 VREF / Output Current Value Setting Pin

This is the pin for setting the output current value to pin setting mode. Output current value can be set base on VREF voltage and current detection resistor (RNF resistor).

$$I_{OUT} = \frac{VREF}{5} / RNF \qquad [A]$$

Where:
I_{OUT} is the Output Current
VREF is the Output Current Value Set Voltage
RNF is the Resistor for Current Detection

If the VREF pin is open, the input becomes indefinite, the VREF voltage rises, the set current increases, and a large current may flow. Therefore, avoid using the VREF pin when it is open. If a voltage is applied to the VREF pin so that the calculated value of I_{OUT} exceeds 2 A, a current exceeding the rating will flow to the output, and OCP or TSD may operate or may even be destroyed.
Also, when inputting by divided resistance, select the resistance value in consideration of the outflow current (Max 2 µA). The minimum current that may be controlled from VREF voltage has a minimum ON time for PWM drive therefore, it is decided based on inductance and resistance values of motor coil and minimum ON time.

In SPI setting mode, the register set value is reflected, so the pin input is invalid. It is recommended that VREF connects GND in SPI setting mode.

Pin Function Description - Continued

17 VREFMIN / Output Current Value Lower Limit Setting Pin

This pin is for setting the lower limit of the output current during High-efficiency driving in pin setting mode. The lower limit of output current can be set base on VREF voltage and current detection resistor (RNF resistor).

$$I_{OUTMIN} = \frac{VREFMIN}{5} / RNF \qquad [A]$$

Where:
I_{OUTMIN} is the Output Lower Limit Current
VREFMIN is the Output Current Value Lower Limit Set Voltage
RNF is the Resistor for Current Detection

If VREFMIN voltage greater or equal VREF voltage, VREFMIN equals zero in IC internal.

In SPI setting mode, the register set value is reflected so the pin input is disabled. It is recommended that VREFMIN connects GND in SPI setting mode.

18 CR / Chopping Frequency Setting Pin

This is the pin for setting the chopping frequency of output using pin setting mode.
Connect external capacitor (470 pF to 1500 pF) and Resistance (10 kΩ to 200 kΩ) to GND.
Make sure that the wiring from the external to GND does not have a common impedance with other GND patterns. Also, keep away from the wiring of steep pulses such as square waves, and design the pattern so that the wiring is less likely to cause noise. If the CR pin is open or biased from the outside, normal PWM constant current control will not be possible. Therefore, be sure to attach both capacitor and resistance parts when using with PWM constant current control.

In SPI setting mode, register setting is used. so the pin input is invalid. It is recommended that CR connects GND in SPI setting mode.

19 MTH / Current Decay Mode Setting Pin

This is the pin for setting the current decay mode using pin setting mode. Current decay mode can be optionally set according to input voltage.

MTH Pin Input Voltage [V]	Current Decay Mode
0 to 0.3	SLOW DECAY
0.4 to 1.0	MIX DECAY
1.5 to 3.5	FAST DECAY

Connect to GND when using at SLOW DECAY mode. Don't use missing setting in above table.
If the MTH pin is open, the input will be unsettled and the PWM operation may become unstable. Therefore, avoid using the MTH pin when it is open. Also, when divided resistance is input, select the resistance value in consideration of the outflow current (Max 2 μA).
In SPI setting mode, register setting is used. so the pin input is invalid. It is recommended that MTH connects GND in SPI setting mode.

20 INVREF / Internal VREF Output Pin

This is the pin for the output of internal VREF voltage.

21 STOMGN / Step-out Margin Output Pin

This pin is for output a voltage corresponding to the back electromotive voltage of the connected motor.
This pin acquires counter electromotive voltage during the motor output OPEN period.
Therefore, using it in FULL STEP mode without an OPEN period is not possible. STOMGN voltage hold previous voltage in FULL STEP mode without an OPEN period. And, STOMGN voltage is 0 V when ENABLE = L.

22 VREGD / 1.5 V Regulator Output Pin

This is the regulator output pin for logic power supply. Place a multilayer ceramic capacitor of about 0.01 μF to 0.1 μF to stabilize the operation of the IC internal circuit.

23 VREGA / 5 V Regulator Output Pin

Regulator output pin for analog power supply. Place a multilayer ceramic capacitor of about 0.01 μF to 0.1 μF to stabilize the operation of the IC internal circuit.

24 VREGDAC / IC Internal ADC and DAC 5 V Regulator Output Pin

Regulator output pin for ADC and DAC inside the IC. Place a multilayer ceramic capacitor of about 0.01 μF to 0.1 μF to stabilize the operation of the IC internal circuit.

25 TEST1 / Test Pin

This pin is used during IC shipping test. When PS = L -> H, 2.8 V is output for about 1 ms, so use to it at OPEN. Take note that there is a possibility of malfunction if used without OPEN processing.

Pin Function Description - Continued

26 TEST2 / Test Pin

This pin is for the delivery inspection of IC, and grounded before use.
In addition, using application without grounding may result to a malfunction.

27 NC

This pin is unconnected electrically with IC internal circuit.

28 IC Back Metal

The VQFN040V6060 package has a heat dissipation metal at the back of IC, and it is assumed that this metal will be heat-treated before use so be sure to connect it to the GND plane on the board with solder and use taking as wide a GND pattern as possible to secure a sufficient heat dissipation area.
In addition, the back metal is shorted to the back of IC chip, and since it is a GND potential, if it is shorted with a potential other than GND, it may malfunction or break. Never pass any wiring pattern other than GND at the back of IC.

Various Circuits for Protection

1 Temperature Protection Circuit (TSD)

This IC has a built-in thermal shutdown circuit as a measure to protect the IC from overheating. If the chip temperature of the IC exceeds 175 °C (Typ), the motor output will open and L level is output from the FO pin. In addition, it automatically returns to normal operation when the temperature drops below 150 °C (Typ). However, if, continuously, heat is applied further from the outside even if the TSD is operating, thermal runaway will occur and result in destruction.

2 Overcurrent Protection Circuit (OCP)

This IC has a built-in overcurrent protection circuit as a countermeasure against damage in the event of a short circuit between motor outputs, a ceiling fault, or a ground fault. This circuit latches the motor output to the OPEN state when the specified current flows for 4 µs (Typ), and outputs the L level from the FO pin. It will be restored by turning the power on again or resetting with the PS pin. The overcurrent protection circuit is a circuit that aims to prevent the IC from being destroyed by overcurrent in an abnormal state such as a motor output short circuit, and does not aim to protect or guarantee the set. Therefore, do not design the protection of the set using the function of this circuit. If the power is turned on again or restored by resetting in an abnormal state after overcurrent protection operation, take note that the overcurrent protection operation may be repeated in the order of latch -> return -> latch, which may cause heat generation or deterioration of the IC. If the Inductance value of wiring is large such as when the wiring is long at the time of ceiling fault, ground fault or short circuit, an overcurrent will flow and the output pin voltage will jump. If it exceeds the absolute maximum rating, it may result in destruction of the IC. Also, if a current that is greater than or equal to the output current rating and less than or equal to the OCP detection current flows, the IC may generate heat and the IC may deteriorate beyond Tjmax = 150 °C. Therefore, do not allow current exceeding the output rating to flow.

3 Malfunction Prevention Function When Low Voltage (UVLO)

This IC has a built-in under voltage lock out function to prevent false operation such as IC output during power supply under voltage. When the applied voltage to the VCC pin goes under 6 V (Typ), the motor output is set to OPEN. This switching voltage has a 1 V (Typ) hysteresis to prevent false operation by noise etc. Be aware that this circuit does not operate during power save mode. Also, the electrical angle is reset when the UVLO circuit operates.

4 Output OFF function When Overvoltage (OVLO)

This IC has a built-in over voltage lock OFF circuit to protect the IC output and the motor during power supply over voltage. When the applied voltage to the VCC pin goes over 32 V (Typ), the motor output is set to OPEN. This switching voltage has a 1 V (Typ) hysteresis and a 4 µs (Typ) mask time to prevent false operation by noise etc. Although this over voltage locked out circuit is built-in, there is a possibility of destruction if the absolute maximum value for power supply voltage is exceeded, therefore the absolute maximum value should not be exceeded. Be aware that this circuit does not operate during power save mode.

5 Malfunction Prevention Function When No Power Loading (Ghost Supply Prevention Function)

If a signal (logic input, MTH, VREF) is input when there is no power supplied to this IC, there is a function which prevents the false operation by voltage supplied via the electrostatic destruction prevention diode from these input pins to the VCC to this IC or to another IC's power supply. Therefore, there is no malfunction of the circuit even when voltage is supplied to these input pins while there is no power supply.

6 Operation in a Strong Magnetic Field

This IC is not intended to operate in a strong electric field. Therefore, when using it in a strong electric field, make sure that there are no malfunctions.

PWM Constant Current Control

1 Current Control Operation

When the output transistor is turned on, the output current increases, RNF voltage(voltage that external resistance attached the RNF pin and output current determined) reaches its voltage to be determined by the VREF pin and IC internal proper voltage, current detection comparator toggles and it becomes decay mode.
The output transistor turned on again after CR timer reaches decay count time.
This sequence occurs repeatedly that VREF voltage is determined by the VREF pin at pin setting mode.
VREF voltage and decay count time is determined by each registers setting at SPI setting mode.

2 Noise Canceling Function

To avoid false detection of the current detection comparator due to RNF spike noise that occurs when the output is turned on, minimum ON time t_{ONMIN} (blank time) is provided to disable current detection from turning ON of output transistor to minimum ON time. This allows constant current drive without an external filter.

3 CR Timer

In pin setting mode, the CR pin repeats charging and discharging between the V_{CRH} voltage and V_{CRL} voltage due to the external capacitor and resistance.
The current detection comparator detection is disabled in a section from the start of charging in V_{CRL} to V_{CRH}. This charging section is the minimum ON time t_{ONMIN}. Discharge starts after reaching V_{CRH} and when the output current reaches the set current value in this discharge section, the current decay mode is entered.
After that, when it is discharged and reaches V_{CRL}, it returns from current decay mode to output ON mode, and at the same time it starts charging.
The CR charge time t_{ONMIN} and discharge time $t_{DISCHARGE}$ are determined using the following equations (Typ) based on external components capacitor and resistance, and the sum of these two is the chopping cycle t_{CHOP} .

$$t_{ONMIN} \approx C \times \frac{R' \times R}{R' + R} \times ln\left(\frac{V_{CR} - V_{CRL}}{V_{CR} - V_{CRH}}\right) \text{[s]}$$

Where:
t_{ONMIN} is the Minimum ON Time
C is the External Capacitor
R is the External Resistor
R' is the CR Pin Internal Impedance 5 kΩ (Typ)
V_{CR} is the CR Pin internal charge Voltage
V_{CRH} is the Pin maximum Voltage
V_{CRL} is the CR Pin minimum Voltage

$$V_{CR} = V \times \frac{R}{R' + R} \text{ [V]}$$

Where:
V is the Internal Regulator Voltage 5 V (Typ)

$$V_{CRH} = V_{CR} - (V_{CR} - 1) \times exp(-tu/(C \times \frac{R' \times R}{R' + R})) \text{ [V]}$$

Where:
tu is the Internal proper time 3.32x10-7 s (Typ)

$$V_{CRL} = 0.4 \times exp\left(-\frac{td + C \times R \times \alpha}{C \times \mathrm{R}}\right) \text{[V]}$$

Where:
td is the Internal proper time 1.25×10^{-6} s (Typ)
α is the Internal proper value 0.0656 (Typ)

$$t_{DISCHARGE} \approx C \times R \times ln\left(\frac{V_{CRH}}{V_{CRL}}\right) \text{ [s]}$$

Where:
$t_{DISCHARGE}$ is the CR Discharge Time

$$t_{CHOP} = t_{ONMIN} + t_{DISCHARGE} \text{ [s]}$$

Where:
t_{CHOP} is the Chopping Cycle
In SPI setting mode, it is determined by register setting.

3 CR Timer - Continued

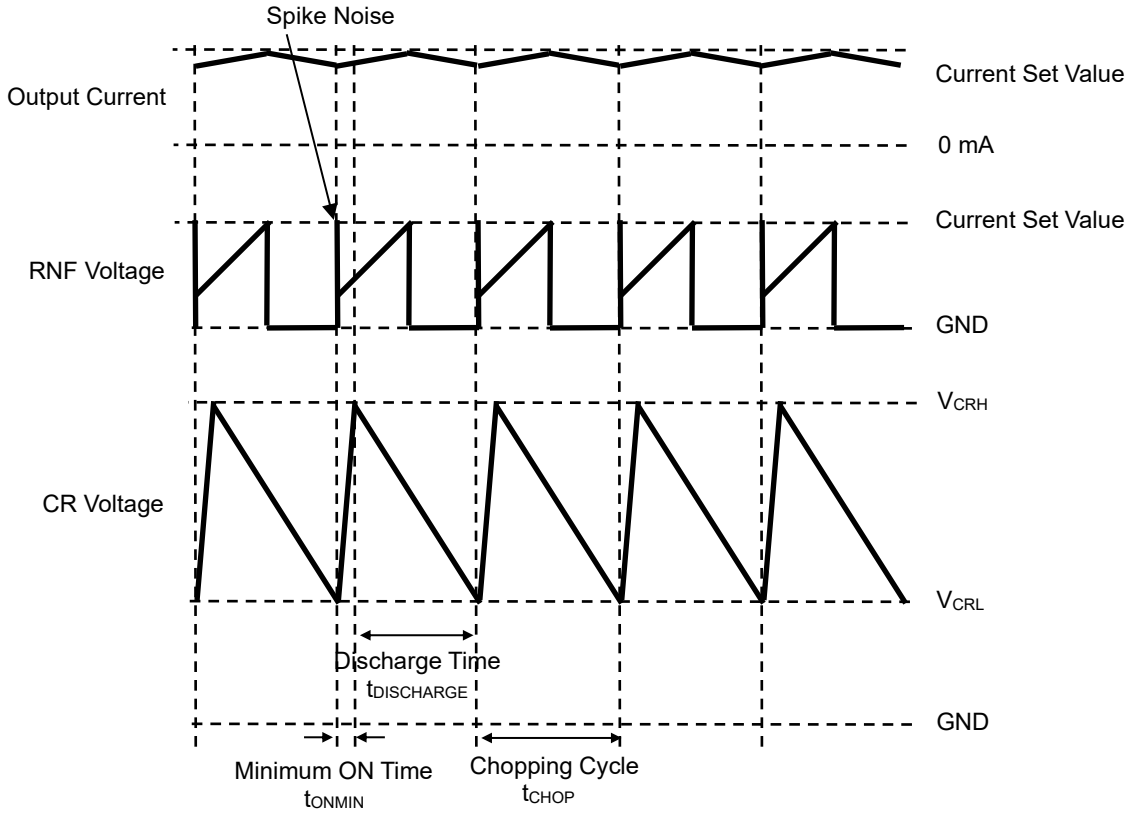


Figure 4. CR Voltage, RNF Voltage and Output Current Timing Chart

The resistance of the CR pin does not reach the V_{CRH} voltage when the resistance value is low so use 10 kΩ or more (10 kΩ to 200 kΩ is recommended). Regarding capacity, if a capacitor of several thousand pF or more is used, the minimum ON time t_{ONMIN} becomes longer, and depending on the inductance and resistance values of the motor coil, output current may flow more than the current set value (470 pF to 1500 pF is recommended).

Furthermore, if the chopping cycle t_{CHOP} is set too long, the ripple of output current becomes large which may reduce the average current and reduce the rotation efficiency so be careful. Select the optimal value to minimize motor drive noise, output current waveform distortion, etc. The CR pin is not used in SPI setting mode. Both t_{ONMIN} and $t_{DISCHARGE}$ can be decided in the register setting.

PWM Constant Current Control - Continued

4 Current Decay Mode

In PWM constant current drive, the current decay mode (FAST DECAY / SLOW DECAY) can be optionally set. The following diagrams show the route of state of output transistor and the motor regenerative current path during current decay for each decay mode.

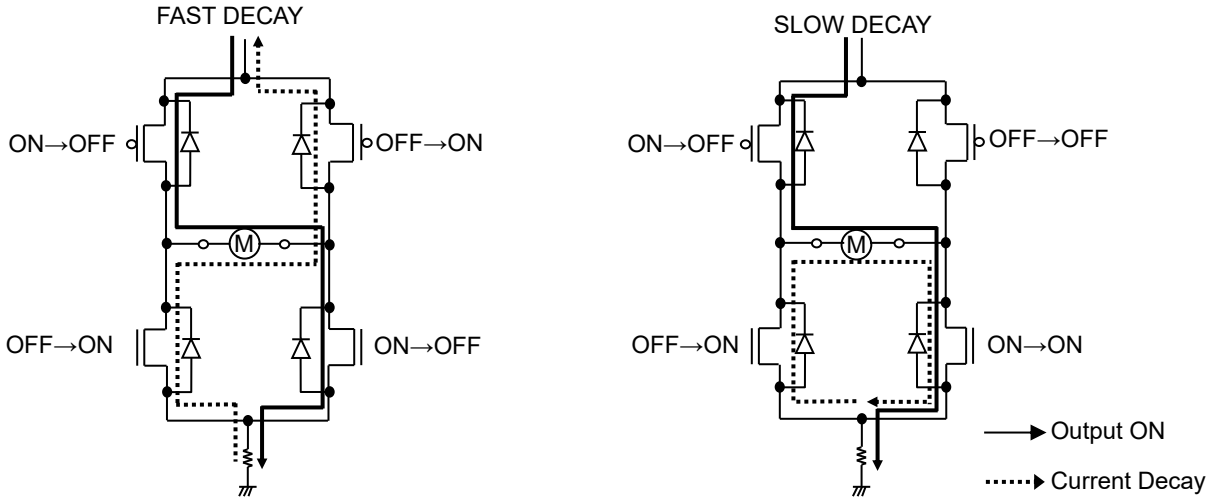


Figure 5. Regenerative Current Path During Current Decay

When in pin setting mode, set by the MTH pin voltage, and when in SPI setting mode, set by register setting.

MTH Pin Input Voltage [V]	Current Decay Mode
0 to 0.3	SLOW DECAY
0.4 to 1.0	MIX DECAY
1.5 to 3.5	FAST DECAY

The current decay setting in SPI setting mode is set in the register setting. Don't use missing setting in above table.
The features of each decay mode are as follows.

4.1 SLOW DECAY

The voltage applied between the motor coils during current decay is small, and the regenerative current gradually decreases so the current ripple is small, which is advantageous for motor torque. However, the output current increases. due to fall-off of current control characteristics in the low-current region, or due to reverse EMF of the output motors exhibited in half-step, quarter step, 1/8 step, 1/16 step and 1/32 step modes when driving at high pulse rate. The current waveform is distorted because it cannot follow the change in current limit value, and motor vibration increases. Thus, this decay mode is most suited to full step modes or low pulse rate drive half step, quarter step, 1/8 step, 1/16 step and 1/32 step modes.

4.2 FAST DECAY

The regenerative current decreases sharply so the distortion in current waveform in high pulse rate drive can be reduced. However, since the ripple in output current increases, the average current decreases;
(1) decrease in motor torque(it can be dealt with by increasing the current limit value, but it is necessary to consider the output rated current) and (2) dissipation in motor becomes large and heat generation increases. If there is no problem particularly with (1) and (2), this mode is most suited for half step, quarter step, 1/8 step, 1/16 step, and 1/32 step modes in high pulse rate drive.
MIX DECAY method / AUTO DECAY method are available as a way to improve the problems that occur in SLOW DECAY and FAST DECAY.

4.3 MIX DECAY

Switching between SLOW DECAY and FAST DECAY during current decay can improve the current controllability without increasing the current ripple. Also, depending on the voltage input to the MTH pin, time ratio can be changed for SLOW DECAY and FAST DECAY and can achieve the optimal control conditions for all motors. During MIX DECAY, the first half, x % (t_1 to t_2), of discharge section in the chopping cycle t_{CHOP} is SLOW DECAY, and the remaining section (t_2 to t_3) is FAST DECAY. However, if the current set value is not reached during the first half, x % (t_1 to t_2), of this discharge section, SLOW DECAY is not performed and only FAST DECAY is performed. The SPI setting mode is set by register setting.

4.4 AUTO DECAY

Normally, the SLOW DECAY mode is applied in decay, only when rapid decay requires switching to the FAST DECAY mode so that current controllability can be improved without increasing the current ripple. FAST DECAY is set only when the output current reaches the current set value during the minimum ON time. However, the AUTO DECAY mode can only be used in the SPI setting mode.

4 Current Decay Mode - Continued

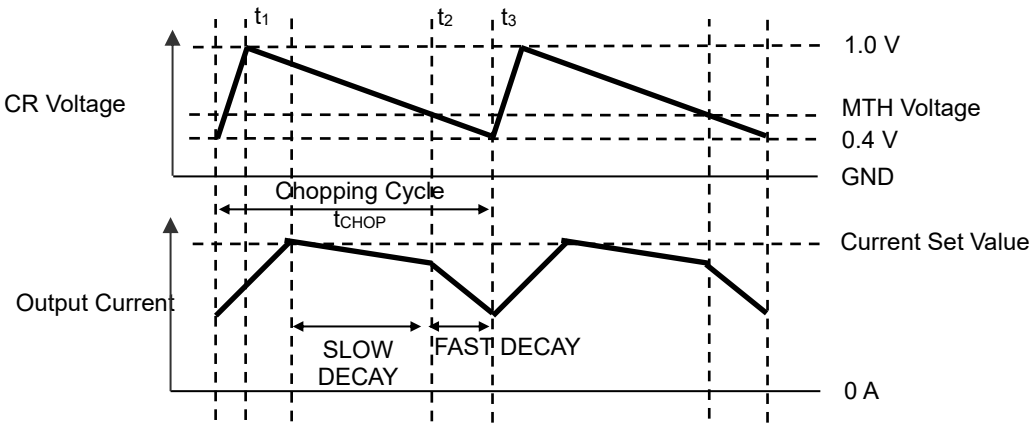


Figure 6. CR Voltage and Output Current During MIX DECAY

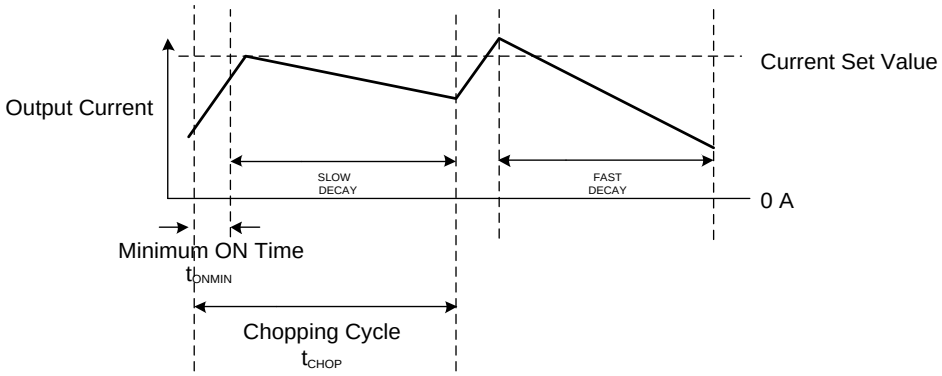


Figure 7. Output current during AUTO DECAY

Translator Circuit Operation in CLK-IN Drive System

This IC has a built-in translator circuit that may drive the stepping motor in the CLK-IN drive system. The translator circuit in the CLK-IN drive system is described as follows.

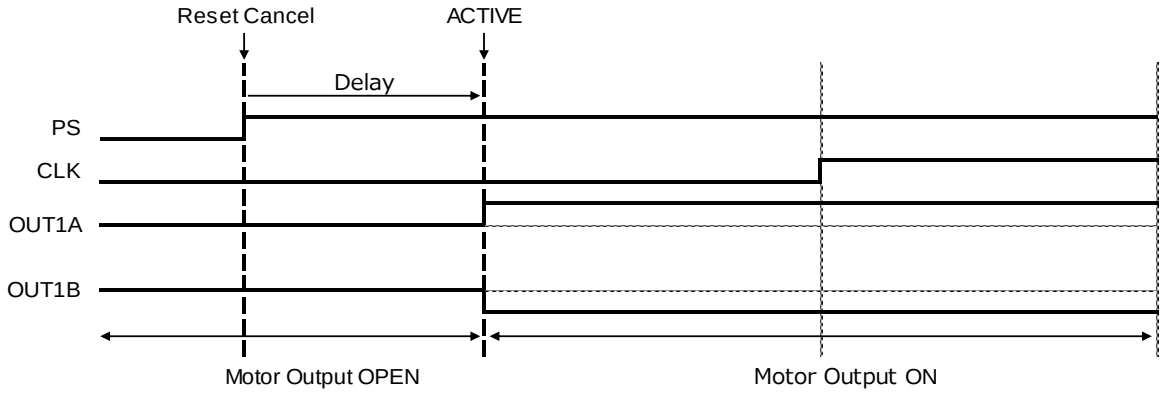
1 Reset Operation

The translator circuit goes through an initialization process in power ON reset function and the PS pin.

1.1 Initialization Process When Turning the Power ON

1.1.1 When Power ON in PS = L (This is the normal sequence so recommended to use this.)

When power is turned on, the power ON reset function will work inside the IC to initialize it. However, the motor output will remain in OPEN state as long as PS = L whether ENABLE = H or not. After turning on the power, by setting to PS = L -> H, the motor output will be in the ACTIVE state, and excitation will be applied at the initial electric angle.
However, take note that when in PS = L -> H, there is a delay of 1 ms (Max) until the motor output returns to the ACTIVE state from standby state to the normal state.



1.1.2 When Power ON in PS = H

After the power ON reset function works inside the IC, the power turns on and the circuit is initialized. If the motor output is ENABLE = H, it becomes active, and excitation is applied at the initial electric angle.

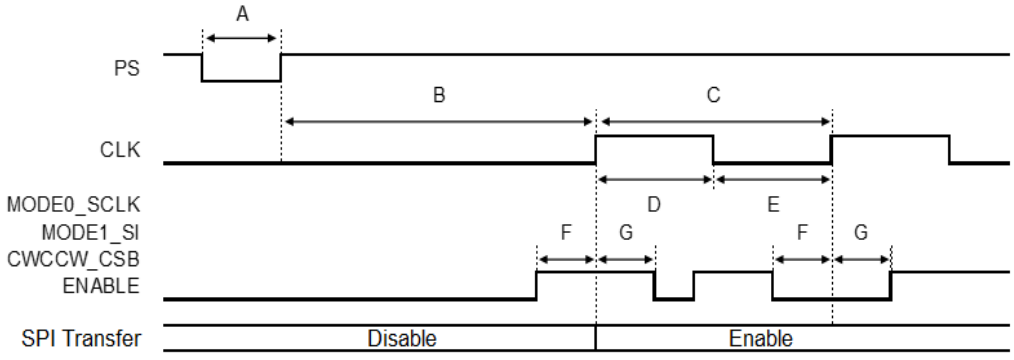
1.2 Initialization operation during motor operation

When initializing the translator circuit while the motor is operating, input a reset signal to the PS pin.
However, when PS = L -> H, there is a delay of 1 ms (Max) until the motor output returns to the ACTIVE state from the standby state to the normal state.

2 Control Input Timing

The translator circuit basically operates at the rising edge of CLK signal so observe the input timing as shown below. Take note that the translator circuit may behave unexpectedly if the input is set in violation of this timing. Also, take note that when in PS = L -> H, there will be a delay of 1 ms (Max) until the motor output returns to the ACTIVE state from the standby state to the normal state, and even with the CLK input in the delay section, the phase advance operation is not performed.

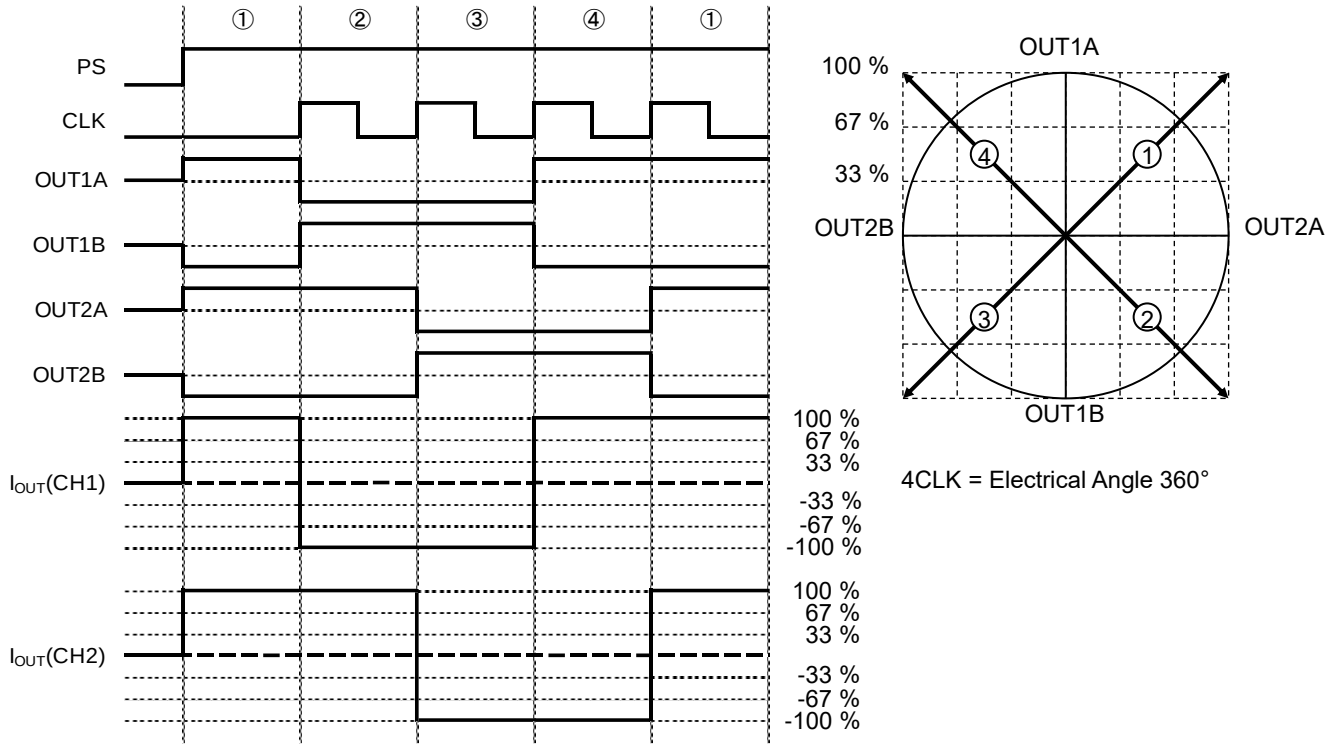
Similar sections are disabled for SPI transfer as well.



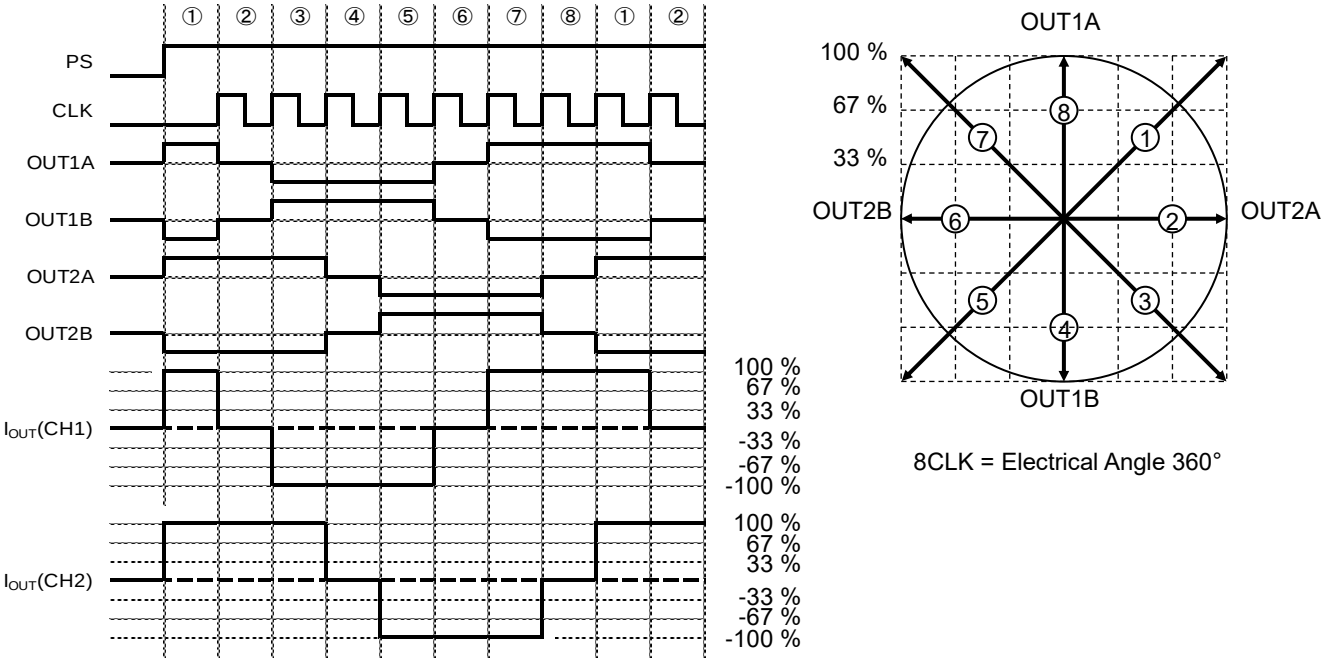
A: PS Minimum L Pulse width 20 µs
B: PS Rising Edge to CLK Rising Edge Input Maximum Delay Time 1 ms
C: CLK Minimum Cycle 4 µs
D: CLK Minimum Input H Pulse Width 2 µs
E: CLK Minimum Input L Pulse Width 2 µs
F: MODE0_SCLK, MODE1_SI, CWCCW_CSB and ENABLE Setup Time 1 µs
G: MODE0_SCLK, MODE1_SI, CWCCW_CSB and ENABLE Hold Time 1 µs

Translator Circuit Operation in CLK-IN Drive System - Continued

3 FULL STEP A, CWCCW_CSB = L, ENABLE = H

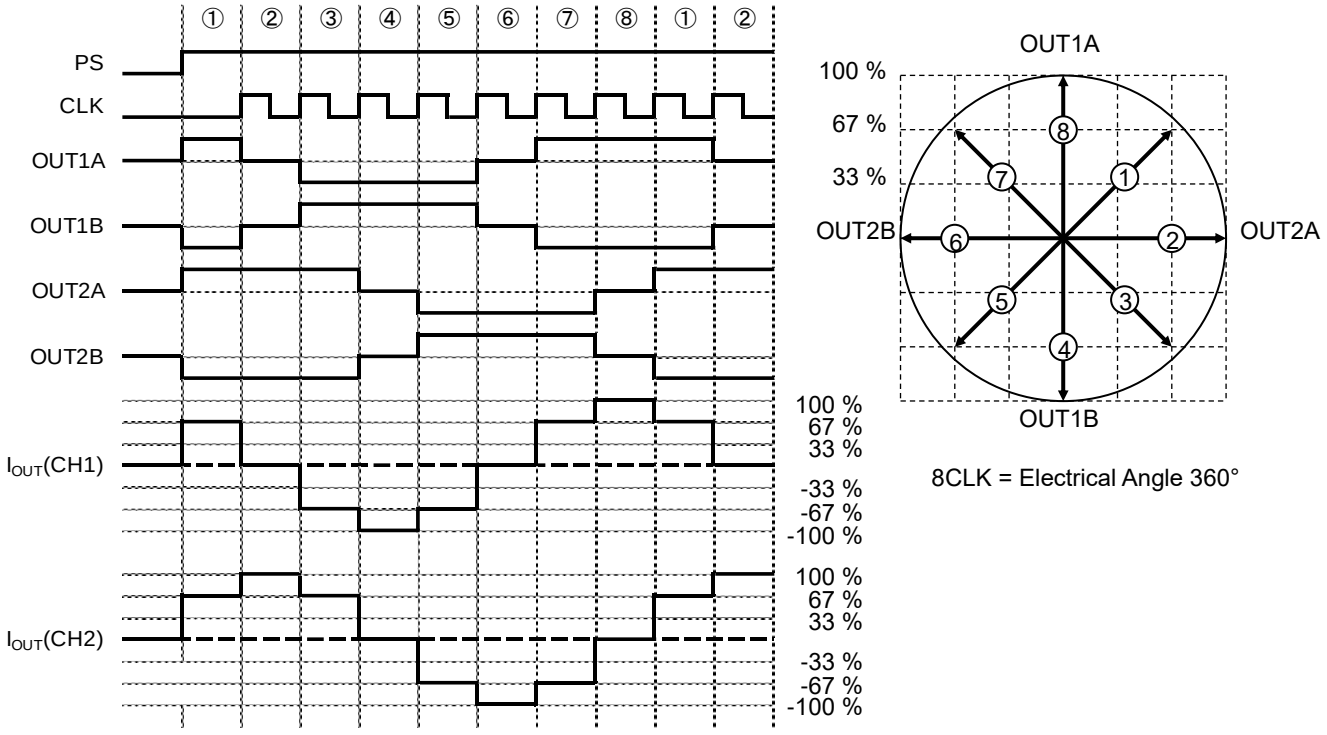


4 HALF STEP A, CWCCW_CSB = L, ENABLE = H

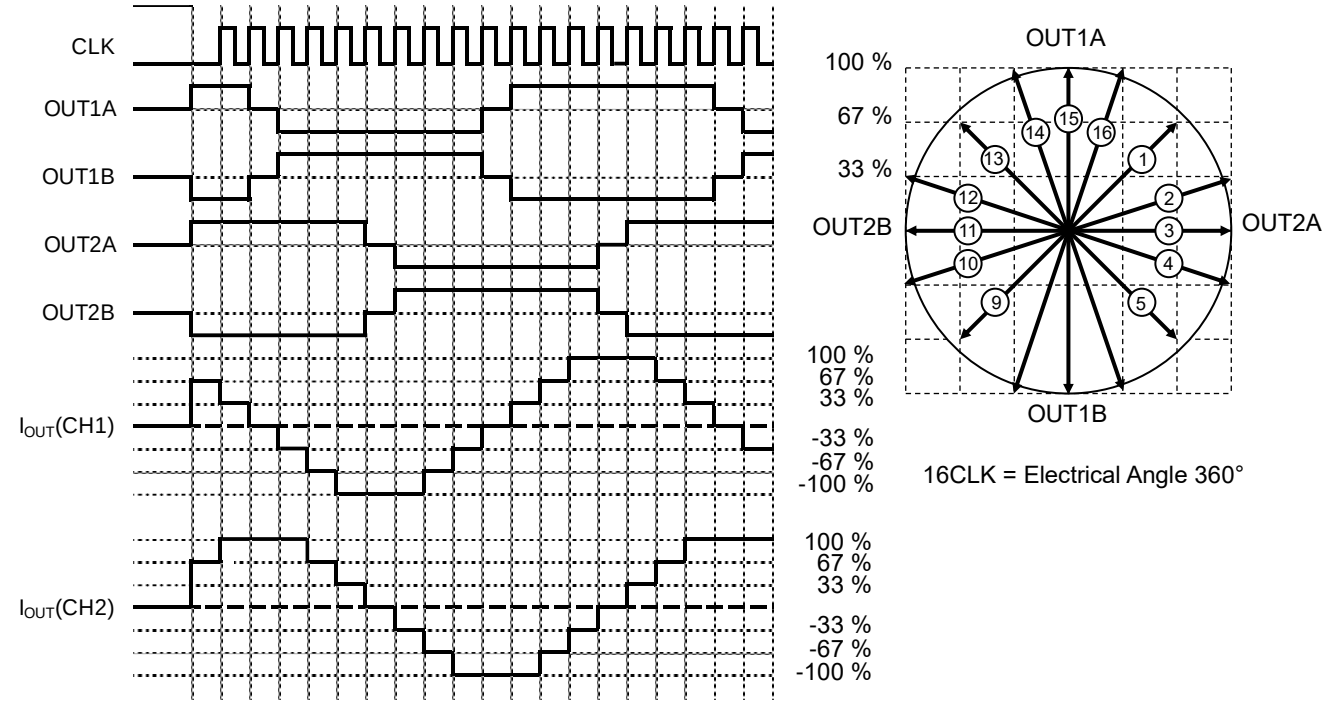


Translator Circuit Operation in CLK-IN Drive System - Continued

5 HALF STEP B, CWCCW_CSB = L, ENABLE = H

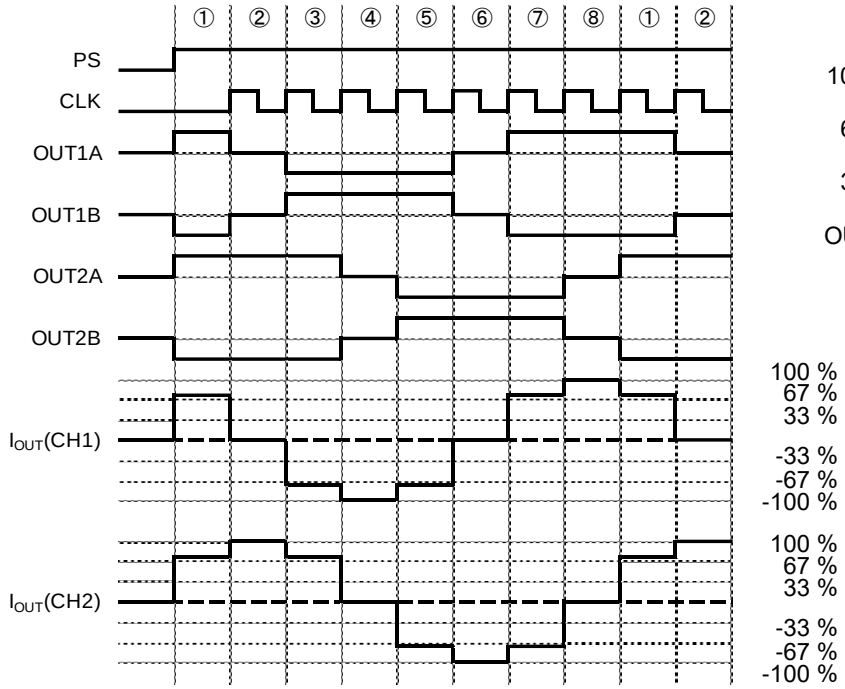


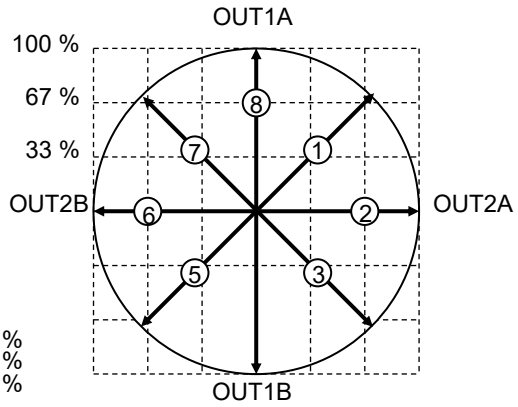
6 QUARTER STEP A, CWCCW_CSB = L, ENABLE = H



Translator Circuit Operation in CLK-IN Drive System - Continued

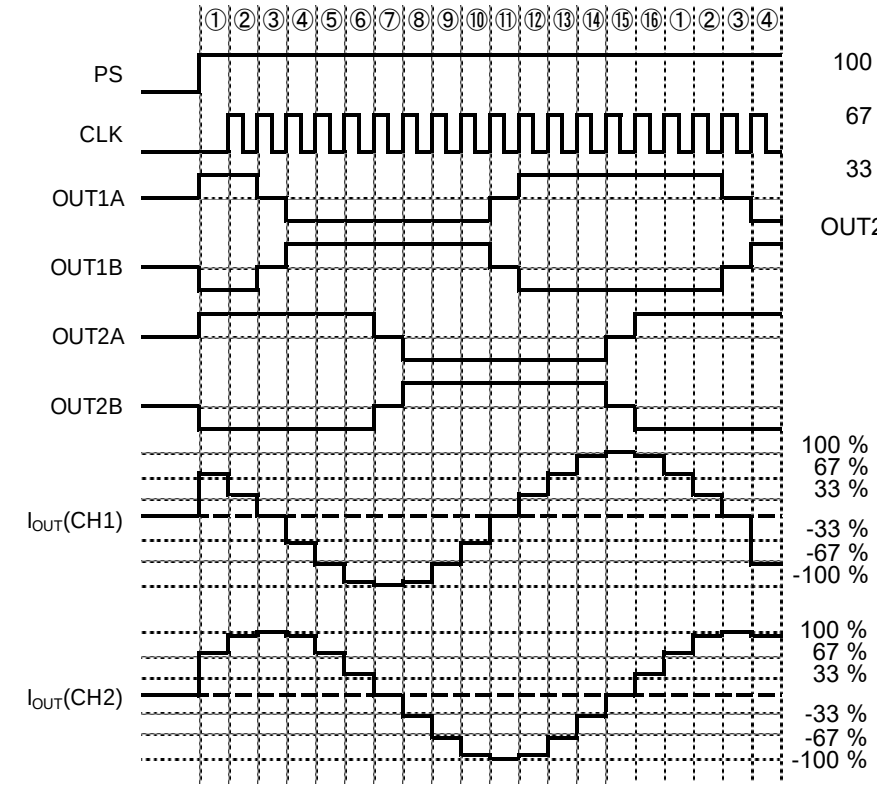
7 HALF STEP C, CWCCW_CSB = L, ENABLE = H

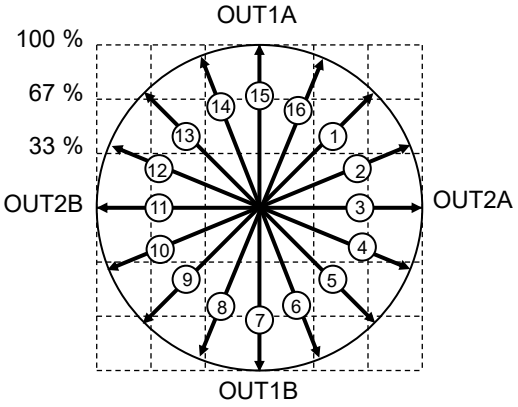




8CLK = Electrical Angle 360°

8 QUARTER STEP B, CWCCW_CSB = L, ENABLE = H





16CLK = Electrical Angle 360°

Translator Circuit Operation in CLK-IN Drive System – Continued

9 Step Sequence Table (FULL STEP B, HALF STEP C, QUARTER STEP B, 1/ 8 STEP, 1/ 16 STEP, 1/ 32 STEP)

Initial Excitation Position = Step Angle 45°

FULL STEP B	HALF STEP C	QUARTE RSTEP B	1/8 STEP	1/16 STEP	1/32 STEP	CH1 Current [%]	CH2 Current [%]	STEP Angle [°]
	1	1	1	1	1	100.00	0.00	0.00
					2	99.88	4.91	2.81
				2	3	99.52	9.80	5.63
					4	98.92	14.67	8.44
			2	3	5	98.08	19.51	11.25
					6	97.00	24.30	14.06
				4	7	95.69	29.03	16.88
					8	94.15	33.69	19.69
		2	3	5	9	92.39	38.27	22.50
					10	90.40	42.76	25.31
				6	11	88.19	47.14	28.13
					12	85.77	51.41	30.94
			4	7	13	83.15	55.56	33.75
					14	80.32	59.57	36.56
				8	15	77.30	63.44	39.38
					16	74.10	67.16	42.19
1	2	3	5	9	17	70.71	70.71	45.00
					18	67.16	74.10	47.81
				10	19	63.44	77.30	50.63
					20	59.57	80.32	53.44
			6	11	21	55.56	83.15	56.25
					22	51.41	85.77	59.06
				12	23	47.14	88.19	61.88
					24	42.76	90.40	64.69
		4	7	13	25	38.27	92.39	67.50
					26	33.69	94.15	70.31
				14	27	29.03	95.69	73.13
					28	24.30	97.00	75.94
			8	15	29	19.51	98.08	78.75
					30	14.67	98.92	81.56
				16	31	9.80	99.52	84.38
					32	4.91	99.88	87.19
	3	5	9	17	33	0.00	100.00	90.00
					34	-4.91	99.88	92.81
				18	35	-9.80	99.52	95.63
					36	-14.67	98.92	98.44
			10	19	37	-19.51	98.08	101.25
					38	-24.30	97.00	104.06
				20	39	-29.03	95.69	106.88
					40	-33.69	94.15	109.69
		6	11	21	41	-38.27	92.39	112.50
					42	-42.76	90.40	115.31
				22	43	-47.14	88.19	118.13
					44	-51.41	85.77	120.94
			12	23	45	-55.56	83.15	123.75
					46	-59.57	80.32	126.56
				24	47	-63.44	77.30	129.38
					48	-67.16	74.10	132.19

9 Step Sequence Table - Continued

FULL STEP B	HALF STEP C	QUARTE RSTEP B	EIGHTH STEP	1/16 STEP	1/32 STEP	CH1 Current [%]	CH2 Current [%]	STEP Angle [°]
2	4	7	13	25	49	-70.71	70.71	135.00
					50	-74.10	67.16	137.81
				26	51	-77.30	63.44	140.63
					52	-80.32	59.57	143.44
			14	27	53	-83.15	55.56	146.25
					54	-85.77	51.41	149.06
				28	55	-88.19	47.14	151.88
					56	-90.40	42.76	154.69
		8	15	29	57	-92.39	38.27	157.50
					58	-94.15	33.69	160.31
				30	59	-95.69	29.03	163.13
					60	-97.00	24.30	165.94
			16	31	61	-98.08	19.51	168.75
					62	-98.92	14.67	171.56
				32	63	-99.52	9.80	174.38
					64	-99.88	4.91	177.19
	5	9	17	33	65	-100.00	0.00	180.00
					66	-99.88	-4.91	182.81
				34	67	-99.52	-9.80	185.63
					68	-98.92	-14.67	188.44
			18	35	69	-98.08	-19.51	191.25
					70	-97.00	-24.30	194.06
				36	71	-95.69	-29.03	196.88
					72	-94.15	-33.69	199.69
		10	19	37	73	-92.39	-38.27	202.50
					74	-90.40	-42.76	205.31
				38	75	-88.19	-47.14	208.13
					76	-85.77	-51.41	210.94
			20	39	77	-83.15	-55.56	213.75
					78	-80.32	-59.57	216.56
				40	79	-77.30	-63.44	219.38
					80	-74.10	-67.16	222.19
3	6	11	21	41	81	-70.71	-70.71	225.00
					82	-67.16	-74.10	227.81
				42	83	-63.44	-77.30	230.63
					84	-59.57	-80.32	233.44
			22	43	85	-55.56	-83.15	236.25
					86	-51.41	-85.77	239.06
				44	87	-47.14	-88.19	241.88
					88	-42.76	-90.40	244.69
		12	23	45	89	-38.27	-92.39	247.50
					90	-33.69	-94.15	250.31
				46	91	-29.03	-95.69	253.13
					92	-24.30	-97.00	255.94
			24	47	93	-19.51	-98.08	258.75
					94	-14.67	-98.92	261.56
				48	95	-9.80	-99.52	264.38
					96	-4.91	-99.88	267.19

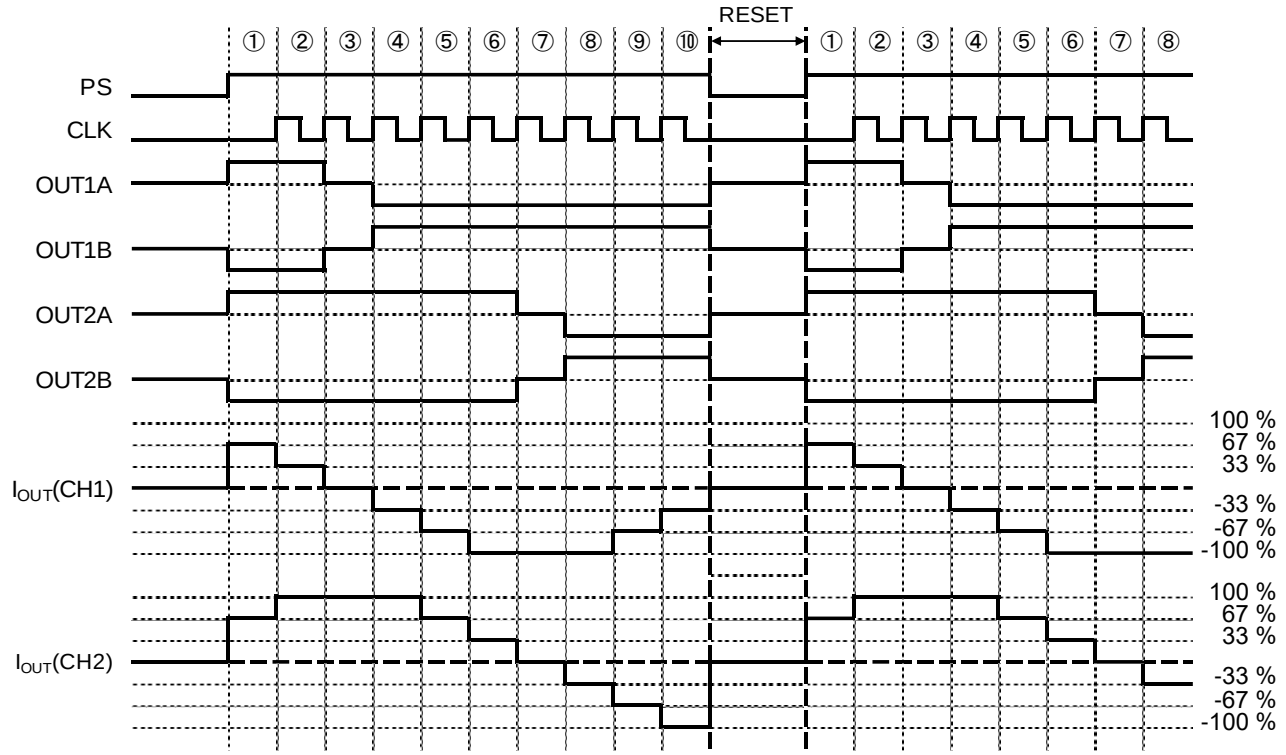
9 Step Sequence Table - Continued

FULL STEP B	HALF STEP C	QUARTE RSTEP B	EIGHTH STEP	1/16 STEP	1/32 STEP	CH1 Current [%]	CH2 Current [%]	STEP Angle [°]
	7	13	25	49	97	0.00	-100.00	270.00
					98	4.91	-99.88	272.81
				50	99	9.80	-99.52	275.63
					100	14.67	-98.92	278.44
			26	51	101	19.51	-98.08	281.25
					102	24.30	-97.00	284.06
				52	103	29.03	-95.69	286.88
					104	33.69	-94.15	289.69
		14	27	53	105	38.27	-92.39	292.50
					106	42.76	-90.40	295.31
				54	107	47.14	-88.19	298.13
					108	51.41	-85.77	300.94
			28	55	109	55.56	-83.15	303.75
					110	59.57	-80.32	306.56
				56	111	63.44	-77.30	309.38
					112	67.16	-74.10	312.19
4	8	15	29	57	113	70.71	-70.71	315.00
					114	74.10	-67.16	317.81
				58	115	77.30	-63.44	320.63
					116	80.32	-59.57	323.44
			30	59	117	83.15	-55.56	326.25
					118	85.77	-51.41	329.06
				60	119	88.19	-47.14	331.88
					120	90.40	-42.76	334.69
		16	31	61	121	92.39	-38.27	337.50
					122	94.15	-33.69	340.31
				62	123	95.69	-29.03	343.13
					124	97.00	-24.30	345.94
			32	63	125	98.08	-19.51	348.75
					126	98.92	-14.67	351.56
				64	127	99.52	-9.80	354.38
					128	99.88	-4.91	357.19

Translator Circuit Operation in CLK-IN Drive System – continued

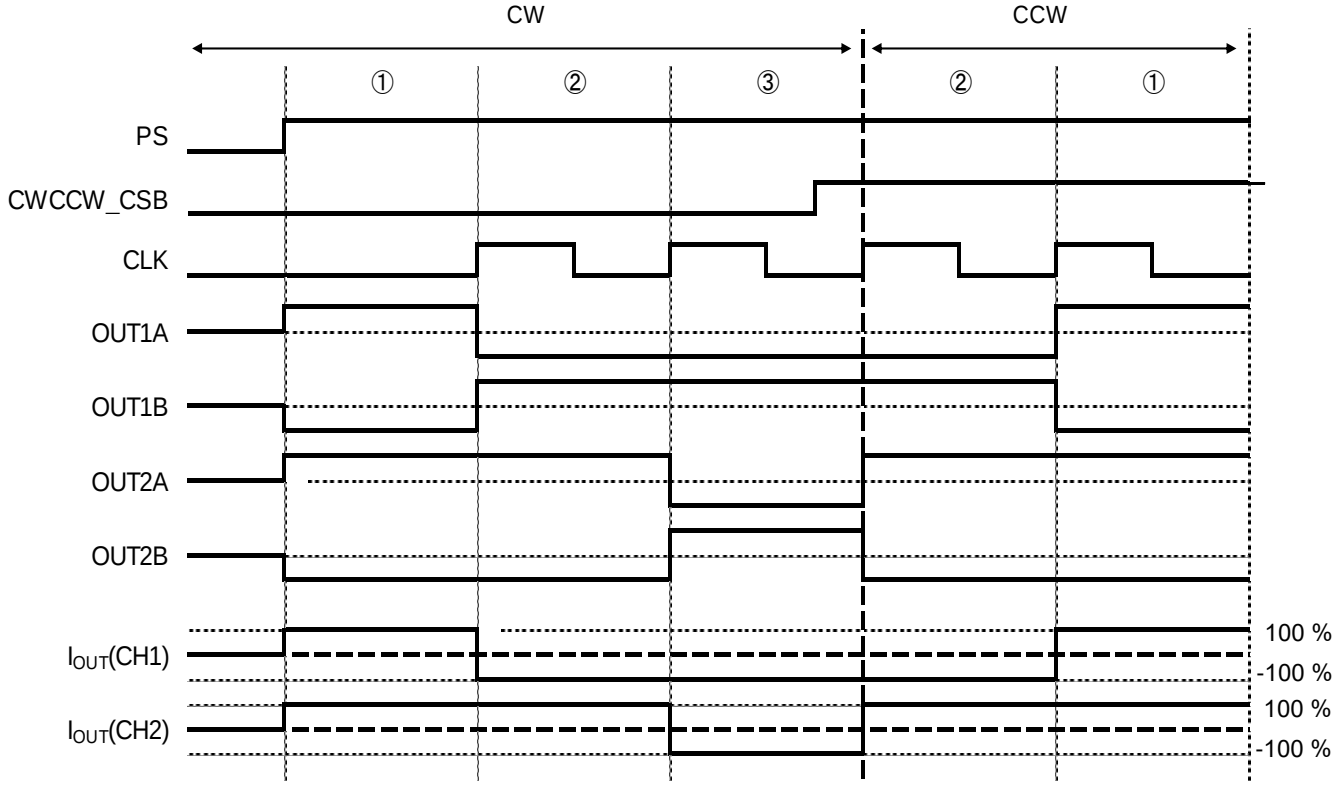
10 Reset timing chart (QUARTER STEP, CWCCW_CSB = L, ENABLE = H)

Input the PS pin to L to reset the translator circuit while the motor operates. Reset operation will run regardless of other input signals. At this point, the IC internal circuit will come to a standby mode, and the motor output will be set OPEN.



11 Motor rotation direction switching timing chart (FULL STEP A, ENABLE = H)

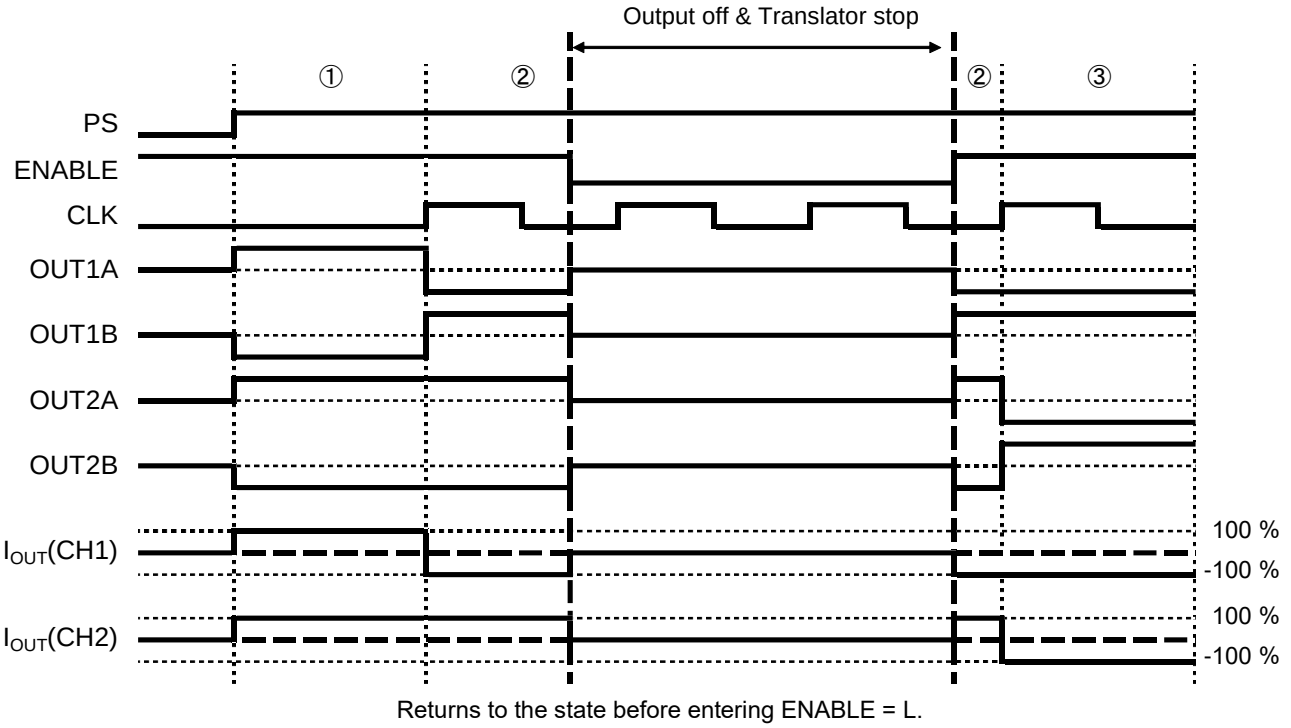
The switching of the motor rotation direction is reflected at the rising edge of CLK immediately after the CWCCW_CSB signal changes. However, even if the control on the driver IC side is supported, depending on the operating state of the motor at the time of switching, the motor may not be able to follow. Motor step-out and missteps may occur, so evaluate the switching sequence thoroughly.



Translator Circuit Operation in CLK-IN Drive System - Continued

12 ENABLE Switching Timing Chart (FULL STEP A)

ENABLE signal switching is reflected by changes in the ENABLE signal regardless of other input signals. In the ENABLE = L section, the phase advance operation of the internal translator circuit is stopped because the CLK input is cut off as the motor output becomes OPEN. Therefore, when returning from ENABLE = L to H, it returns to the state immediately before entering ENABLE = L. Since the excitation mode is switched even in the ENABLE = L section, when the excitation mode is switched in the ENABLE = L section, it will return by excitation mode after switching to return from ENABLE = L to H.



13 Motor Excitation Mode Switching

Switching the excitation mode is performed at the same time as the excitation mode setting signal changes regardless of CLK signal. This product has a built-in function to prevent motor step-out due to torque vector mismatch between transition excitations when switching the excitation mode. However, even if the control on the driver IC side is supported, the motor cannot follow depending on the operating state of the motor at the time of switching. Since motor step-out or mis-stepping may occur, carefully evaluate the excitation mode switching sequence before deciding or setting.

14 Precautions When Doing Both Motor Rotation Direction and Excitation Mode Switching

As shown in the figure below, after reset release (PS = L -> H), section A is defined as the period before the first CLK signal is input while section B is defined as the period after the first CLK signal is input.

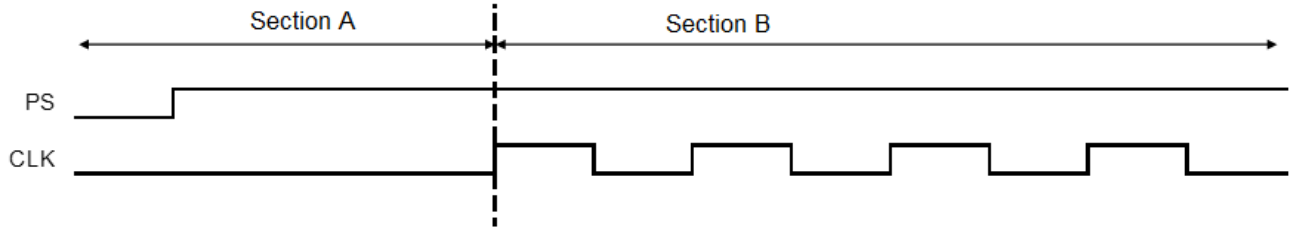
Section A

-> There are no restrictions on switching the motor rotation direction and excitation mode.

Section B

-> While in one CLK cycle or while in the ENABLE = L section, perform one from either motor rotation direction or excitation mode.

If this constraint is violated, a misstep (one more phase advance) may occur and the motor may step out. Therefore, when switching both motor rotation direction and excitation mode, be sure to input the reset signal to the PS pin and set it to the state of section A.



SPI Interface

This IC is equipped with SPI and can read various settings and IC status.

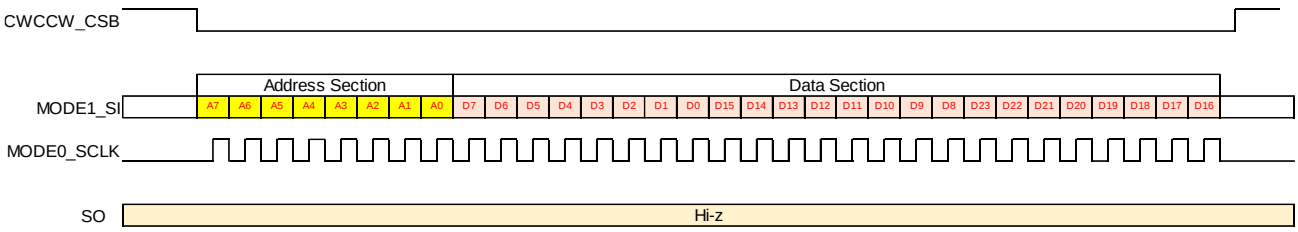
1 3 Wires 32 Bit SPI Input Method

Setting GAMOD1 = H and GAMOD2 = H will enable the 3 wires 32 bit SPI mode and will make the following pins useable as SPI input / output.

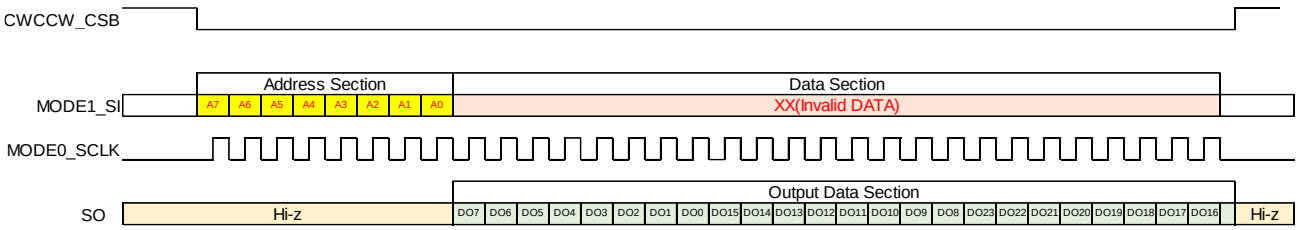
Pin Name	I/O	Description
CWCCW_CSB	I	Chip select signal L active
MODE0_SCLK	I	Serial clock Write: Captures data at the rising edge Read: Outputs data at falling edge
MODE1_SI	I	Serial data entry Input data is invalid when CWCCW_CSB is H
SO	O	Serial data output

The upper 8 bits are the register address and the lower 24 bits are the register data.
The register data is read/write in 'MSB first' every 8 bits.

When writing



When reading



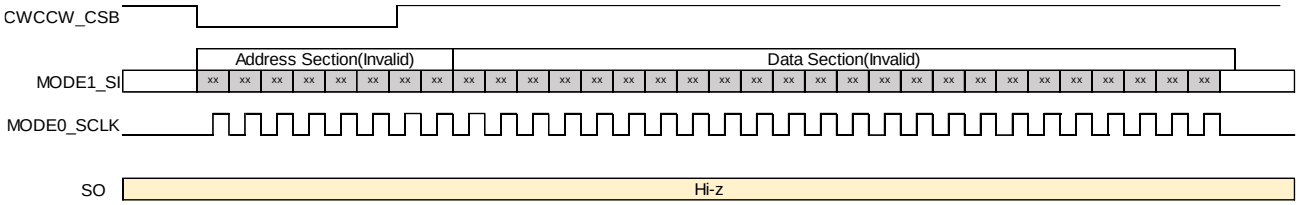
SPI Interface - Continued

2 3 Wires 32 Bit SPI Transmission Cancellation

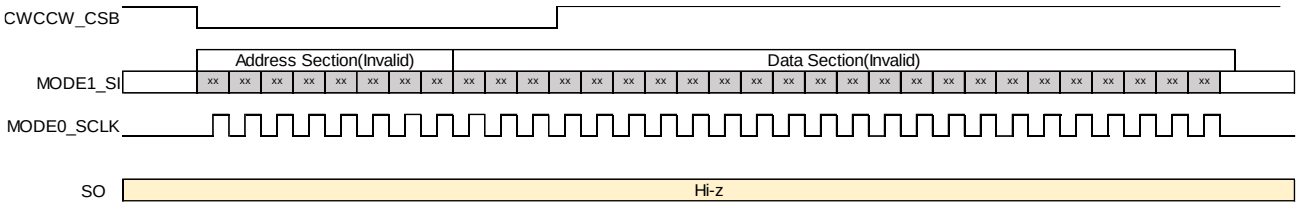
Hold the CWCCW_CSB pin at L while transmitting 32-bit data. If the CWCCW_CSB pin is set to H during transmission, the transmission will be cancelled.

When the number of transmission register data bits is 8 bits or more, the data cancellation range differs depending on the register type (Type1, Type2).

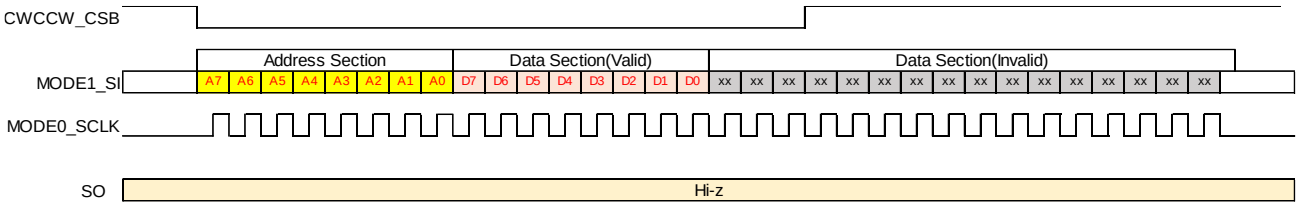
Transmission cancellation (register address)



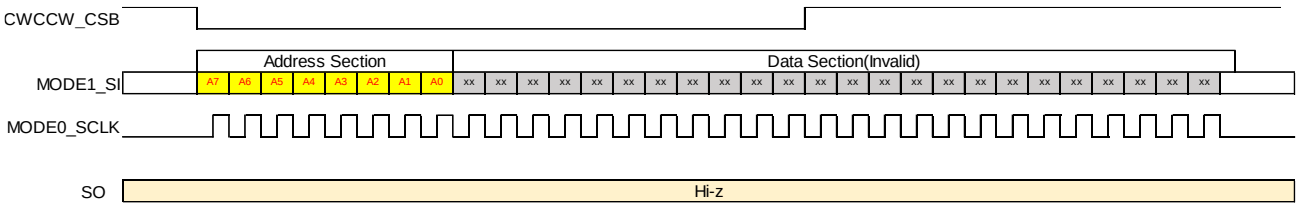
Transmission Register Data Cancellation (less than 8 bits)



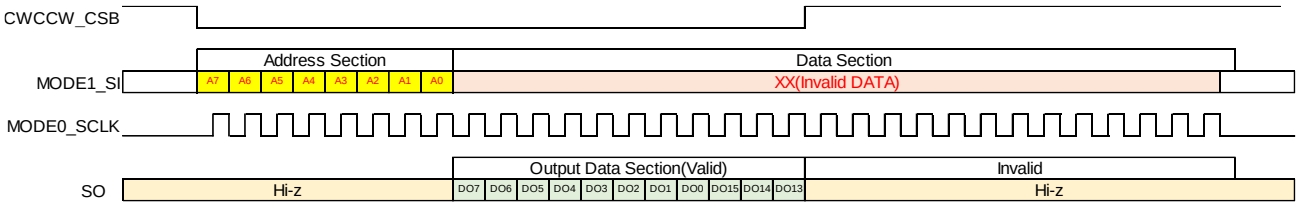
Transmission Register Data Cancellation (8 Bit or more, Type1)



Transmission Register Data Cancellation (8 Bit or more, Type2)



Read Cancellation



Command Register

1 Command Register Description

This IC has a command register consisting of 8-bit address + 24-bit data.

The write command register is roughly divided into Type 1 and Type 2, and Type1 and Type2 write reflect timings are different.

Write command register type	Description
Type1	Data is reflected every 8 bits of transmission
Type2	Reflected when all 24 bits of transmission are received Enabled after sending UNLOCK command *(Note 9)*

2 Command List

No.	Command	Hex	Function	Type	R/W
1	MODESET	01	MODE setting, rotation direction, High-efficiency Drive setting	Type1	R/W
2	READSEL	02	Read command settings	Type1	W
3	READ_READSEL	03	Read READSEL settings	-	R
4	READ_DIAGNOSTIC	04	Read TSD, OCP, OVLO protection status	-	R
5	READ_CURRENT_VREF	05	Read drive VREF set value	-	R
6	READ_MARGIN	06	Load state read	-	R
7	STOMGN_PEAKHOLD_CLEAR *(Note 9)*	07	STOMGN peak hold state OFF	Type2	W
8	VREFSET	10	Drive VREF setting	Type2	R/W
9	VREFMINSET	11	VREF setting for minimum drive during High-efficiency Drive	Type2	R/W
10	KESET	12	Motor constant setting	Type2	R/W
11	MTHSET	13	Current decay mode setting	Type2	R/W
12	CRTIMESET	14	Chopping time setting	Type2	R/W
13	MIN_FREQ_ON_SET	15	High-efficiency Drive OFF -> ON frequency setting	Type2	R/W
14	MIN_FREQ_OFF_SET	16	High-efficiency Drive ON -> OFF frequency setting	Type2	R/W
15	HIEF_SET	17	High-efficiency Drive setting	Type2	R/W
16	VBEMFAVESET	18	Internal induced-voltage reading setting	Type2	R/W
17	GAIN_SET	19	High-efficiency Drive gain setting 1	Type2	R/W
18	GAIN1_SET	1A	High-efficiency Drive gain setting 2	Type2	R/W
19	GAIN2_SET	1B	High-efficiency Drive gain setting 3	Type2	R/W
20	RESERVE	1C	RESERVE	-	-
21	RESERVE	1D	RESERVE	-	-
22	RESERVE	1E	RESERVE	-	-
23	VREFOFFSETSET	1F	OUT2A / OUT2B output current setting Offset setting	Type2	R/W
24	GAIN4_SET	20	High-efficiency Drive gain setting 5	Type2	R/W
25	GAIN5_SET	21	High-efficiency Drive gain setting 6	Type2	R/W
26	GAIN6_SET	22	High-efficiency Drive gain setting 7	Type2	R/W
27	VBEMFMONSET	23	Step-out margin read setting	Type2	R/W
28	STOMGN_PEAKHOLD_SET	24	STOMGN peak hold setting	Type2	R/W
29	FULLSTEPWINDOWSET	25	Current reading period setting during FULL STEP	Type2	R/W
30	HIEFSELMAX	26	Current decay ratio upper limit setting	Type2	R/W
31	HIEFSELMIN	27	Current decay ratio lower limit setting	Type2	R/W
32	UNLOCK	A0	Type2 command enabled	Type1	W

(Note 9) STOMGN_PEAKHOLD_CLEAR is a Type2 register, but it is enabled regardless of the UNLOCK command.

Do not use command addresses other than those in this table.

Command register-continued

3 Command Register Detailed Description

3.1 MODESET

MODESET	Hex	DATA								Initial	Remarks
Command	01	0	0	0	0	0	0	0	1	-	
D7-D0	-	0	D6	D5	D4	D3	D2	D1	D0	00	
D15-D8	-	0	0	0	0	0	0	0	0	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

Motor excitation mode setting

D3	D2	D1	D0	Description
0	0	0	0	FULL STEP A
0	0	0	1	HALF STEP A
0	0	1	0	HALF STEP B
0	0	1	1	QUARTER STEP A
0	1	0	0	FULL STEP B
0	1	0	1	HALF STEP C
0	1	1	0	QUARTER STEP B
0	1	1	1	1/8 STEP
1	0	0	0	1/16 STEP
1	0	0	1	1/32 STEP
1	0	1	0	Inhibit
1	0	1	1	Inhibit
1	1	0	0	Inhibit
1	1	0	1	Inhibit
1	1	1	0	Inhibit
1	1	1	1	Inhibit

Motor rotation direction setting

D4	Description
0	Clockwise (CH2 current outputs with a phase delay of 90° with respect to CH1 current.)
1	Counter Clockwise (CH2 current outputs with a phase advancement by 90° with respect to CH1 current.)

Output enable setting

D5	Description
0	Output enable OFF
1	Output enable ON

The output enable setting is valid only in SPI setting mode.
The relationship between the OUT1A/OUT1B/OUT2A/OUT2B pin outputs, the D5 output enable setting, and the ENABLE pin is as follows.

D5	ENABLE pin logic	OUT1A/OUT1B/OUT2A/OUT2B pin output
0	L	OPEN (electrical angle retention)
0	H	ACTIVE
1	L	ACTIVE
1	H	ACTIVE

High-efficiency Drive setting

D6	Description
0	High-efficiency Drive OFF
1	High-efficiency Drive ON

3 Command Register Detailed Description - Continued

3.2 READSEL

READSEL	Hex	DATA								Initial	Remarks
Command	02	0	0	0	0	0	0	1	0	-	
D7-D0	-	0	0	0	0	0	0	D1	D0	00	
D15-D8	-	0	0	0	0	0	0	D9	D8	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

MODESET Read Setting

D0	Description
0	MODESET command operates as a write command
1	MODESET command operates as a read command

Type 2 Command Read Settings

D1	Description
0	Type 2 command (command address 10h to 27h) operates as a write command
1	Type 2 command (command address 10h to 27h) operates as a read command

READ_MARGIN Read value setting

D9	D8	Description
0	0	12bit load state is read
0	1	STOMGN output voltage set value is read
1	0	Internally induced voltage value is read
1	1	Inhibit

3.3 READ_READSEL

READ_READSEL	Hex	DATA								Initial	Remarks
Command	03	0	0	0	0	0	0	1	1	-	
D7-D0	-	0	0	0	0	0	0	DO1	DO0	00	
D15-D8	-	0	0	0	0	0	0	DO9	DO8	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

READSEL D0 Reading

DO0	Description
0	READSEL command D0 setting reading. D0 = 0
1	READSEL command D0 setting reading. D0 = 1

READSEL D1 Reading

DO1	Description
0	READSEL command D1 setting reading. D1 = 0
1	READSEL command D1 setting reading. D1 = 1

READSEL D8 Reading

DO8	Description
0	READSEL command D8 setting reading. D8 = 0
1	READSEL command D8 setting reading. D8 = 1

READSEL D9 Reading

DO9	Description
0	READSEL command D9 setting reading. D9 = 0
1	READSEL command D9 setting reading. D9 = 1

3 Command Register Detailed Description - Continued

3.4 READ_DIAGNOSTIC

READ_DIAGNOSTIC	Hex	DATA								Initial	Remarks
Command	04	0	0	0	0	0	1	0	0	-	
D7-D0	-	1	0	0	0	DO3	DO2	DO1	DO0	88	
D15-D8	-	0	0	0	0	0	0	0	0	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

TSD Status Reading

DO0	Description
0	TSD undetected
1	TSD detected

TSD stated is detected, DO0 is 1.
When the TSD state is released after TSD state is detected, the read value holds DO0 = 1 until this command used.
Notice that SPI read sequence does not complete when read sequence does not exceed D23.
So the read value continue to hold DO0 = 1, TSD state is released also.

OVLO Status Reading

DO1	Description
0	OVLO undetected
1	OVLO detected

When VCC voltage exceeded the detection voltage during OVLO mask time, it will not be detected.
OVLO stated is detected, DO1 is 1.
When the OVLO state is released after OVLO state is detected, the read value holds DO1 = 1 until this command used.
Notice that SPI read sequence does not complete when read sequence does not exceed D23.
So the read value continue to hold DO1 = 1, OVLO state is released also.

OCP Status Reading

DO2	Description
0	OCP undetected
1	OCP detected

When detection current is exceeded during the OCP mask time, it will not be detected.
OCP stated is detected, DO2 is 1.
Even when the OCP state is released, the state of the IC is output OFF and the read value is detected.
DO2 clear PS = L or power supply OFF.

Initial Status Reading

DO3	Description
0	Second or more Reading
1	Initial read value after Power On

When this Command is used first time after IC power on, DO3 read value is 1.
Second time or more, DO3 read value is 0.
Notice that SPI read sequence does not complete when read sequence does not exceed D23.
So the read value continue to hold DO3 = 1, second or more Reading also.

3 Command Register Detailed Description - Continued

3.5 READ_CURRENT_VREF

READ_CURRENT_VREF	Hex	DATA								Initial	Remarks
Command	05	0	0	0	0	0	1	0	1	-	
D7-D0	-	0	0	0	0	0	0	DO1	DO0	00	
D15-D8	-	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	00	
D23-D16	-	0	0	0	0	0	0	0	DO16	00	

Drive VREF Setting Integer-side Reading

DO1	DO0	Description
0	0	0
0	1	1
1	0	2
1	1	3

Drive VREF Setting Decimal-side Reading

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

Drive VREF = VREF setting integer-side + VREF setting decimal-side
The decimal-side are values added to each bit as DO15 = 0.5, DO14 = 0.25, DO8 = 0.00390625 and so on.

Example: Read value DO7-DO0 = 01, DO15-DO8 = 5A
VREF setting integer-side = 01 = 1
VREF setting decimal-side = 5A = 0.25 + 0.0625 + 0.03125 + 0.0078125 = 0.3515625
Drive VREF = 1 + 0.3515625= 1.3515625

High-efficiency Drive Status Reading

DO16	Description
0	Normal operating condition
1	High-efficiency Drive state

3 Command Register Detailed Description - Continued

3.6 READ_MARGIN

READ_MARGIN	Hex	DATA								Initial	Remarks
Command	06	0	0	0	0	0	1	1	0	-	
D7-D0	-	0	0	0	DO4	DO3	DO2	DO1	DO0	00	
D15-D8	-	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

In READ_MARGIN, read value contents changes by READSEL D8 and D9.

3.6.1 D9 = 0 and D8 = 0: 12 Bit Load Status Reading

DO3	DO2	DO1	DO0	DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	Description
0	0	0	0	0	0	0	0	0	0	0	0	Load Status Heavy
0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	1	0	
:	:	:	:	:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	1	1	0	1	
1	1	1	1	1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	1	1	1	1	Load Status Small

DO3-DO0, DO15-DO8 is 12bit of load read value. If the value is large, the load is applied.
DO4 is inhibit.

3.6.2 READSEL D9 = 0 and D8 = 1: STOMGN Output Voltage Set Value Reading

STOMGN Output Voltage Set Value Integer Side

DO2	DO1	DO0	Description
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Inhibit
1	1	1	Inhibit

STOMGN output voltage set decimal-side

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

Reading of the STOMGN output voltage set value.
STOMGN output voltage set value = STOMGN output voltage set value integer-side + STOMGN output voltage set value decimal-side.
The decimal-side are values added to each bit as DO15 = 0.5, DO14 = 0.25, DO8 = 0.00390625 and so on.
DO4 and DO3 are inhibit.
Decimal-side is 8bit. However, circuit accuracy is around 4bit.

3 Command Register Detailed Description – Continued

3.6.2 READSEL D9 = 1 and D8 = 0: Internal Induced-voltage Value Reading

Internal Induced-voltage Value Integer-side

DO4	DO3	DO2	DO1	DO0	Description
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
:	:	:	:	:	:
1	0	0	0	0	16
:	:	:	:	:	
1	1	1	1	0	30
1	1	1	1	1	31

Internal induced-voltage Value decimal-side

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

Reading of the internal induced-voltage value.
Internal induced-voltage value = internal induced-voltage value integer-side + internal induced-voltage value decimal-side.
The decimal-side are values added to each bit as DO15 = 0.5, DO14 = 0.25, DO8 = 0.00390625 and so on.
Decimal-side is 8bit. However, circuit accuracy is around 4bit.
For the internal induced-voltage, refer to Induced-voltage Reading Circuit (Page 61).

3.7 STOMGN_PEAKHOLD_CLEAR

READ_CURRENT_VREF	Hex	DATA								Initial	Remarks
Command	07	0	0	0	0	0	1	1	1	-	
D7-D0	-	0	0	0	0	0	0	0	0	00	
D15-D8	-	0	0	0	0	0	0	0	0	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

If this command is used when the STOMGN pin is in peak hold status, it will disappear in the peak hold status.
This command does not depend on the value of D23-D0, but the peak hold status is released when a 24-bit data is transmitted.

3 Command Register Detailed Description – Continued

3.8 VREFSET

VREFSET	Hex	DATA								Initial	Remarks
Command	10	0	0	0	1	0	0	0	0	-	
D7-D0	-	0	0	0	0	0	0	D1	D0	01	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

Drive VREF Setting Integer-side

D1	D0	Description
0	0	0
0	1	1
1	0	2
1	0	3

Drive VREF Setting Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

Drive VREF = VREF setting integer-side + VREF setting decimal-side.
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D8 = 0.00390625 and so on.

Example: When setting to Drive VREF setting = 1.4
VREF setting integer-side = 1: D7-D0 = 01
VREF setting decimal-side = 0.4*(Note1)* ≈ 0.3984375 = 0.25 + 0.125 + 0.015625 + 0.0078125: D15-D8 = 66
(Note1) means setting the decimal-side to exactly 0.4 is not possible.

3 Command Register Detailed Description - Continued

3.9 VREFMINSET

VREFMINSET	Hex	DATA								Initial	Remarks
Command	11	0	0	0	1	0	0	0	1	-	
D7-D0	-	0	0	0	0	0	0	D1	D0	00	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	80	
D23-D16	-	0	0	0	0	0	0	0	0	00	

High-efficiency Drive VREF Minimum Value Setting Integer-side

D1	D0	Description
0	0	0
0	1	1
1	0	2
1	1	3

High-efficiency Drive VREF Minimum Value Setting Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

High-efficiency Drive VREF minimum value = VREF minimum value setting integer-side + VREF minimum value setting decimal-side.
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D8 = 0.00390625 and so on.
This register is not used in normal operations. If VREFSET setting is less than the VREFMINSET set value, the minimum setting for High-efficiency Drive will be 0 regardless of the set value.

Example: When setting to High-efficiency Drive VREF minimum value = 0.2
High-efficiency Drive VREF minimum value setting integer-side = 0: D7-D0 = 00
High-efficiency Drive VREF minimum value setting Integer-side = $0.2^{(Note1)} \approx 0.19921875$
= 0.125 + 0.0625 + 0.0078125 + 0.00390625: D15-D8 = 33
(Note1) means setting the decimal-side to exactly 0.2 is not possible.

3 Command Register Detailed Description – Continued

3.10 KESET

KESET	Hex	DATA								Initial	Remarks
Command	12	0	0	0	1	0	0	1	0	-	
D7-D0	-	D7	D6	D5	D4	D3	D2	D1	D0	01	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	40	
D23-D16	-	D23	D22	D21	D20	0	0	0	0	00	

Motor Integer Setting

D7	D6	D5	D4	D3	D2	D1	D0	:	D23	D22	D21	D20	Description
0	0	0	0	0	0	0	0	:	0	0	0	0	0
0	0	0	0	0	0	0	0	:	0	0	0	1	0.00000095367431640625
0	0	0	0	0	0	0	0	:	0	0	1	0	0.0000019073486328125
:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	:	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	:	1	1	0	1	0.99999713897705078125
1	1	1	1	1	1	1	1	:	1	1	1	0	0.9999980926513671875
1	1	1	1	1	1	1	1	:	1	1	1	1	0.99999904632568359375

The motor constant is set to 20 bits. There is no integer-side. Use the 20 bits as decimal numbers.
Motor constants are D7 = 0.5, D6 = 0.25 D0 = 0.00390625, D23 = 0.00000762939453125 and
D20 = 0.00000095367431640625 and so on which are values added to each bit.

3 Command Register Detailed Description - Continued

3.11 MTHSET

MTHSET	Hex	DATA								Initial	Remarks
Command	13	0	0	0	1	0	0	1	1	-	
D7-D0	-	0	0	0	0	0	0	D1	D0	00	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	00	
D23-D16	-	0	0	0	0	0	0	0	D16	00	

MTH Setting Integer-side

D1	D0	Description
0	0	0
0	1	1
1	0	2
1	1	3

MTH Setting Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

MTH setting = MTH setting integer-side + MTH setting decimal-side.
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D8 = 0.00390625 and so on.

AUTO DECAY mode setting

D16	Description
0	AUTO DECAY OFF
1	AUTO DECAY ON

D0-D15 bit setting are invalid and operate AUTO DECAY during current decay when AUTO DECAY is ON.

3 Command Register Detailed Description – Continued

3.12 CRTIMESET

CRTIMSET	Hex	DATA								Initial	Remarks
Command	14	0	0	0	1	0	1	0	0	-	
D7-D0	-	0	0	D5	D4	D3	D2	D1	D0	05	
D15-D8	-	0	0	D13	D12	D11	D10	D9	D8	20	
D23-D16	-	0	0	0	0	0	0	0	0	00	

PWM Constant Current Control Minimum ON Time Setting

D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	inhibit
0	0	0	0	0	1	0.083 µs
0	0	0	0	1	0	0.166 µs
:	:	:	:	:	:	:
0	0	0	1	0	1	0.4166 µs
:	:	:	:	:	:	:
1	1	1	1	1	0	5.166 µs
1	1	1	1	1	1	5.25 µs

PWM Constant Current Control Current Decay Time Setting

D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	inhibit
0	0	0	0	0	1	2 µs
0	0	0	0	1	0	4 µs
:	:	:	:	:	:	:
1	0	0	0	0	0	64 µs
:	:	:	:	:	:	:
1	1	1	1	0	1	122 µs
1	1	1	1	1	0	124 µs
1	1	1	1	1	1	126 µs

PWM constant current control chopping cycle is determined by minimum ON time + current decay time setting.
When using the SPI mode setting, setting of chopping cycle by the CR pin becomes disabled.

3 Command Register Detailed Description - Continued

3.13 MIN_FREQ_ON_SET

MIN_FREQ_ON_SET	Hex	DATA								Initial	Remarks
Command	15	0	0	0	1	0	1	0	1	-	
D7-D0	-	0	0	0	D4	D3	D2	D1	D0	00	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	20	
D23-D16	-	D23	D22	0	0	0	0	0	0	00	

High-efficiency Drive Enabled Frequency Setting (OFF -> ON) Integer-side

D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0	0	0	0	0	inhibit
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Hz
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Hz
:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	1	0	0	0	0	0	32 Hz
:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Hz
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Hz

High-efficiency Drive Enabled Frequency Setting (OFF -> ON) Decimal-side

D23	D22	Description
0	0	0 Hz
0	1	0.25 Hz
1	0	0.5 Hz
1	1	0.75 Hz

High-efficiency Drive enabled frequency setting (OFF -> ON) enables High-efficiency Drive valid (HIEFEN = H for pin setting mode or MODESET D5 = 1 when using SPI setting), and if input CLK satisfies the following condition expressions, a High-efficiency Drive is performed.

Input CLK frequency > High-efficiency Drive enabled frequency setting (OFF -> ON) x ratio

Ratio: The magnification rate determined by excitation mode

Excitation Mode	Ratio
FULL STEP A	4
FULL STEP B	4
HALF STEP A	8
HALF STEP B	8
HALF STEP C	8
QUARTER STEP A	16
QUARTER STEP B	16
EIGHTH STEP	32
1/16 STEP	64
1/32 STEP	128

3 Command Register Detailed Description – Continued

3.14 MIN_FREQ_OFF_SET

MIN_FREQ_OFF_SET	Hex	DATA								Initial	Remarks
Command	16	0	0	0	1	0	1	1	0	-	
D7-D0	-	0	0	0	D4	D3	D2	D1	D0	00	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	10	
D23-D16	-	D23	D22	0	0	0	0	0	0	00	

High-efficiency Drive Disabled Frequency Setting (ON -> OFF) Integer-side

D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0	0	0	0	0	inhibit
0	0	0	0	0	0	0	0	0	0	0	0	1	1 Hz
0	0	0	0	0	0	0	0	0	0	0	1	0	2 Hz
:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	1	0	0	0	0	16 Hz
:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	1	1	0	8190 Hz
1	1	1	1	1	1	1	1	1	1	1	1	1	8191 Hz

High-efficiency Drive Enabled Frequency Setting (ON -> OFF) Decimal Setting

D23	D22	Description
0	0	0 Hz
0	1	0.25 Hz
1	0	0.5 Hz
1	1	0.75 Hz

High-efficiency Drive disabled frequency setting (ON -> OFF) enables High-efficiency Drive valid (HIEFEN = H for pin setting mode or MODESET D5 = 1 when using SPI setting), and if input CLK satisfies the following condition expressions, the operation will switch from High-efficiency Drive to normal operation.
In addition, this setting must be set a value smaller than MIN_FREQ_ON_SET set value.

Input CLK frequency < High-efficiency Drive disabled frequency setting (ON -> OFF) x ratio

Ratio: The magnification rate determined from excitation mode

Excitation Mode	Ratio
FULL STEP A	4
FULL STEP B	4
HALF STEP A	8
HALF STEP B	8
HALF STEP C	8
QUARTER STEP A	16
QUARTER STEP B	16
EIGHTH STEP	32
1/16 STEP	64
1/32 STEP	128

3 Command Register Detailed Description - Continued

3.15 HIEF_SET

HIEF_SET	Hex	DATA								Initial	Remarks
Command	17	0	0	0	1	0	1	1	1	-	
D7-D0	-	0	0	0	D4	D3	D2	D1	D0	05	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	C0	
D23-D16	-	0	0	0	0	0	0	0	0	00	

High-efficiency Drive High-efficiency Rate Setting Integer-side

D4	D3	D2	D1	D0	Description
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
:	:	:	:	:	:
1	1	1	1	0	30
1	1	1	1	1	31

High-efficiency Drive High-efficiency Rate Setting Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	1	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	0.75
1	1	1	1	1	1	1	1	0.857

High-efficiency rate setting = High-efficiency rate setting integer-side + High-efficiency rate setting decimal-side.
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D8 = 0.00390625 and so on.

3 Command Register Detailed Description – Continued

3.16 VBEMFAVESET

VBEMFAVESET	Hex	DATA								Initial	Remarks
Command	18	0	0	0	1	1	0	0	0	-	
D7-D0	-	0	0	0	0	0	0	D1	D0	00	
D15-D8	-	0	0	0	0	0	0	D9	D8	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

Measurement Internal Induced-voltage Averaging Setting

D1	D0	Description
0	0	No average
0	1	Twice average
1	0	Four times average
1	1	Eight times average

Performs the process of averaging on the internal induced-voltage to measure within one OPEN cycle.
For the averaged value, use the value measured just before the output goes from OPEN to ACTIVE.
If the averaging process is enabled and if two times measurements/ four times measurement/ eight times measurement cannot be made while OPEN process, no average / two times / four times measurements will be used instead.

No Average: The values measured immediately before the change from OPEN to ACTIVE
Two Times Average: The average of the values measured immediately before the change from OPEN to ACTIVE and of the one measurement before that.
Four Times Average: The average of the values measured immediately before the change from OPEN to ACTIVE and of the three measurements before that.
Eight Times Average: The average of the values measured immediately before the change from OPEN to ACTIVE and of the seven measurements before that.

Measurement Internal Induced-voltage Acquisition Setting

D9	D8	Description
0	0	1 phase/2 phase alternately
0	1	Only 1 phase
1	0	Only 2 phases
1	1	Inhibit

Set the internal induced-voltage to be measured.

3 Command Register Detailed Description – Continued

3.17 GAIN_SET

GAIN_SET	Hex	DATA								Initial	Remarks
Command	19	0	0	0	1	1	0	0	1	-	
D7-D0	-	0	0	0	0	D3	D2	D1	D0	01	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	F0	
D23-D16	-	0	0	0	0	0	0	0	D16	00	

High-efficiency Drive, Drive Gain Setting Integer-side

D3	D2	D1	D0	Description
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
:	:	:	:	
1	1	1	0	14
1	1	1	1	15

High-efficiency Drive, Drive Gain Setting Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

High-efficiency Drive, drive gain setting = High-efficiency Drive, drive gain setting integer-side + High-efficiency Drive drive gain setting decimal-side.
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D8 = 0.00390625 and so on.
The drive gain setting during High-efficiency driving is enabled when GAMOD1, GAMOD2 = L, L or GAMOD1, GAMOD2 = H, H.

3 Command Register Detailed Description – Continued

3.18 GAIN1_SET

GAIN1_SET	Hex	DATA								Initial	Remarks
Command	1A	0	0	0	1	1	0	1	0	-	
D7-D0	-	0	0	0	0	D3	D2	D1	D0	02	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	F0	
D23-D16	-	0	0	0	0	0	0	0	0	00	

High-efficiency Drive, Drive Gain Setting Integer-side

D3	D2	D1	D0	Description
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
:	:	:	:	:
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

High-efficiency Drive, Drive Gain Setting Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

High-efficiency Drive, drive gain setting = High-efficiency Drive, drive gain setting integer-side + High-efficiency Drive, drive gain setting decimal-side.
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D8 = 0.00390625 and so on.
The drive gain setting during High-efficiency driving is enabled when GAMOD1, GAMOD2 = H, L.

3.19 GAIN2_SET

GAIN2_SET	Hex	DATA								Initial	Remarks
Command	1B	0	0	0	1	1	0	1	1	-	
D7-D0	-	0	0	0	0	D3	D2	D1	D0	04	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	F0	
D23-D16	-	0	0	0	0	0	0	0	0	00	

High-efficiency Drive, Drive Gain Setting Integer-side

D3	D2	D1	D0	Description
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
:	:	:	:	
1	1	1	0	14
1	1	1	1	15

3 Command Register Detailed Description - Continued

High-efficiency Drive, Drive Gain Setting Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

High-efficiency Drive, drive gain setting = High-efficiency Drive, drive gain setting integer-side + High-efficiency Drive, drive gain setting decimal-side.
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D8 = 0.00390625 and so on.
The drive gain setting during High-efficiency driving is enabled when GAMOD1, GAMOD2 = L, H.

3 Command Register Detailed Description – Continued

3.23 VREFOFFSETSET

VREFOFFSETSET	Hex	DATA								Initial	Remarks
Command	1F	0	0	0	1	1	1	1	1	-	
D7-D0	-	0	0	0	0	0	0	0	D0	00	
D15-D8	-	D15	0	0	0	0	0	D9	D8	00	
D23-D16	-	D23	D22	D21	D20	D19	D18	D17	D16	00	

OUT2A / OUT2B Output Current Setting Offset Setting

D0	Description
0	Offset Setting OFF
1	Offset Setting ON

OUT2A / OUT2B Output Current Setting Offset Set Value Integer-side

D9	D8	Description
0	0	0
0	1	1
1	0	2
1	1	3

OUT2A / OUT2B Output Current Setting Offset Set Value Symbol-side

D15	Description
0	1 (offset positive number)
1	-1 (offset negative number)

OUT2A / OUT2B Output Current Setting Offset Set Value Decimal-side

D23	D22	D21	D20	D19	D18	D17	D16	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

OUT2A / OUT2B output current setting offset setting value
= OUT2A / OUT2B output current setting offset set value symbol-side * (offset integer-side + offset decimal-side)
The decimal-side are values added to each bit as D23 = 0.5, D22 = 0.25, D16 = 0.00390625 and so on.
The symbol-side is determined by D15, and is treated as a positive offset when D15 = 0 and a negative offset when D15 = -1.

Therefore, when OUT2A / OUT2B output current setting is D0 = 1,
it becomes the VREFSET command set value+ OUT2A / OUT2B output current setting offset set value.
In addition, if OUT2A / OUT2B output current setting is less than 0 or if OUT2A / OUT2B output current setting is greater than 4, it will be clipped to 0 and 4, respectively.

If VREFOFFSETSET was set in pin setting mode, since the set value is added to the voltage value set from the VREF pin, do not use the offset setting with D0 = 0 (circuit initial value).

If High-efficiency Drive is enabled, set to D0 = 0 and do not use the offset setting.

3 Command Register Detailed Description - Continued

3.24 GAIN4_SET

GAIN4_SET	Hex	DATA								Initial	Remarks
Command	20	0	0	1	0	0	0	0	0	-	
D7-D0	-	D7	D6	D5	D4	D3	D2	D1	D0	00	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	FF	
D23-D16	-	D23	D22	D21	D20	0	0	0	0	00	

High-efficiency Drive, Drive Gain Setting Integer-side

D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	65534
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	65535

High-efficiency Drive, Drive Gain Setting Decimal-side

D23	D22	D21	D20	Description
0	0	0	0	0
0	0	0	1	0.0625
0	0	1	0	0.125
:	:	:	:	:
1	1	1	0	0.875
1	1	1	1	0.9375

High-efficiency Drive, drive gain setting
= High-efficiency Drive, drive gain setting integer-side + High-efficiency Drive, drive gain setting decimal-side.
The decimal-side are values added to each bit as D23 = 0.5, D22 = 0.25, D20 = 0.0625 and so on.
The drive gain setting during High-efficiency Drive for GAIN4_SET is enabled when GAMOD1, GAMOD2 = L, L or GAMOD1, GAMOD2 = H, H.

3.25 GAIN5_SET

GAIN5_SET	Hex	DATA								Initial	Remarks
Command	21	0	0	1	0	0	0	0	1	-	
D7-D0	-	D7	D6	D5	D4	D3	D2	D1	D0	01	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	FF	
D23-D16	-	D23	D22	D21	D20	0	0	0	0	00	

High-efficiency Drive, drive gain setting = High-efficiency Drive, drive gain setting integer-side + High-efficiency Drive
drive gain setting decimal-side.
The decimal-side are values added to each bit as D23 = 0.5, D22 = 0.25, D20 = 0.0625 and so on.
The drive gain setting during High-efficiency Drive for GAIN5_SET is enabled when GAMOD1, GAMOD2 = H, L.

3.26 GAIN6_SET

GAIN6_SET	Hex	DATA								Initial	Remarks
Command	22	0	0	1	0	0	0	1	0	-	
D7-D0	-	D7	D6	D5	D4	D3	D2	D1	D0	02	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	FF	
D23-D16	-	D23	D22	D21	D20	0	0	0	0	00	

High-efficiency Drive, drive gain setting
= High-efficiency Drive, drive gain setting integer-side + High-efficiency Drive drive gain setting decimal-side.
The decimal-side are values added to each bit as D23 = 0.5, D22 = 0.25, D20 = 0.0625 and so on.
The drive gain setting during High-efficiency Drive for GAIN6_SET is enabled when GAMOD1, GAMOD2 = L, H.

3 Command Register Detailed Description – Continued

3.27 VBEMFMONSET

VBEMFMONSET	Hex	DATA								Initial	Remarks
Command	23	0	0	1	0	0	0	1	1	-	
D7-D0	-	0	D6	D5	D4	D3	D2	D1	D0	00	
D15-D8	-	D15	0	D13	D12	D11	D10	D9	D8	00	
D23-D16	-	D23	D22	D21	D20	D19	D18	D17	D16	00	

STOMGN Output Pin Constant Factor

D3	D2	D1	D0	Description
0	0	0	0	x1
0	0	0	1	x2
0	0	1	0	x4
0	0	1	1	x8
0	1	0	0	x16
0	1	0	1	x32
0	1	1	0	x1/2
0	1	1	1	x1/4
1	0	0	0	x1/8
1	0	0	1	x1/16
1	0	1	0	x1/32
others				Inhibit

The above constant factor is applied to the internal induced-voltage.
If adding a moving average or offset, multiply the values by a constant after each process.

STOMGN Output Pin Moving Average

D6	D5	D4	Description
0	0	0	No moving average
0	0	1	$(a_n + a_{n-1})/2$
0	1	0	$(a_n + a_{n-1} + a_{n-2} + a_{n-3})/4$
0	1	1	$(2*a_n + a_{n-1} + a_{n-2})/4$
1	0	0	$(a_n + a_{n-1} + a_{n-2} + a_{n-3} + a_{n-4} + a_{n-5} + a_{n-6} + a_{n-7})/8$
1	0	1	$(a_n + a_{n-1} + a_{n-2} + \ldots + a_{n-14} + a_{n-15})/16$
1	1	0	inhibit
1	1	1	inhibit

a_n = the last measured internal induced-voltage. a_{n-1} = the previous internal induced-voltage.
a_{n-15} = the 15th previous internal induced-voltage.
Follow the settings in D6 to D4 to obtain a moving average using a_n to a_{n-15}.
The initial values of a_n to a_{n-15} are 0, respectively.

3 Command Register Detailed Description – Continued

STOMGN Output Pin Offset Integer-side

D13	D12	D11	D10	D9	D8	Description
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
:	:	:	:	:	:	:
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

STOMGN Output Pin Offset Symbol-side

D15	Description
0	1(Offset positive number)
1	-1(Offset negative number)

STOMGN Output Pin Offset decimal-side

D23	D22	D21	D20	D19	D18	D17	D16	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

STOMGN output pin offset = STOMGN output pin offset symbol-side * (offset integer-side + offset decimal-side)
The decimal-side are values added to each bit as D23 = 0.5, D22 = 0.25, D16 = 0.00390625 and so on.
The symbol-side is determined by D15, and is treated as a positive offset when D15 = 0 and a negative offset when D15 = -1.

3 Command Register Detailed Description - Continued

3.28 STOMGN_PEAKHOLD_SET

STOMGN_PEAKHOLD _SET	Hex	DATA								Initial	Remarks
Command	24	0	0	1	0	0	1	0	0	-	
D7-D0	-	D7	D6	D5	D4	D3	D2	D1	D0	00	
D15-D8	-	0	0	0	D12	0	D10	D9	D8	00	
D23-D16	-	D23	D22	D21	D20	D19	D18	D17	D16	00	

STOMGN PEAKHOLD Setting Constant

D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	0	0	PEAKHOLD Unnecessary
0	0	0	0	0	0	0	1	1 time
0	0	0	0	0	0	1	0	2 times
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	254 times
1	1	1	1	1	1	1	1	255 times

If D23-D8 (STOMGN PEAKHOLD threshold) is smaller continuously in the frequency set for D7-D0, with respect to internal STOMGN calculated value, the STOMGN output is not the internal STOMGN calculated value but instead, the minimum value of internal STOMGN calculated value detected during continuous PEAKHOLD OFF is output.

If D7-D0 = 00 is set, PEAKHOLD will not be used.

STOMGN PEAKHOLD Threshold Integer-side

D10	D9	D8	Description
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	inhibit
1	1	0	inhibit
1	1	1	inhibit

STOMGN PEAKHOLD Threshold Decimal-side

D23	D22	D21	D20	D19	D18	D17	D16	Description
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0.00390625
0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	0.98828125
1	1	1	1	1	1	1	0	0.9921875
1	1	1	1	1	1	1	1	0.99609375

STOMGN PEAKHOLD Threshold = (Integer-side + Decimal-side)
The decimal-side are values added to each bit as D23 = 0.5, D22 = 0.25, D16 = 0.00390625 and so on.

If set to STOMGN PEAKHOLD threshold >= 5, PEAKHOLD will not be used.

3 Command Register Detailed Description – Continued

PEAKHOLD Application Timing Mask When STOMGN PEAKHOLD ENABLE = L -> H

D12	Description
0	Timing Mask OFF
1	Timing Mask ON

Notice When ENABLE = L -> H.
If the STOMGN_PEAKHOLD_SET command was set and using the PEAKHOLD function, under the condition that the STOMGN output pin moving average setting of the VBEMFMONSET command is also used, it is recommended that the STOMGN_PEAKHOLD_SET command is set to either [1] or [2] below to prevent PEAKHOLD ON immediately after ENABLE L -> H.

[1] Turn on the PEAKHOLD timing mask (D12 = 1)
[2] STOMGN PEAKHOLD setting constant greater than STOMGN output pin moving average setting moving average number (VBEMFMONSET D6 to D4)

3 Command Register Detailed Description – Continued

3.29 FULLSTEPWINDOWSET

FULLSTEPWINDOWSET	Hex	DATA								Initial	Remarks
Command	25	0	0	1	0	0	1	0	1	-	
D7-D0	-	0	0	0	D4	0	D2	D1	D0	02	
D15-D8	-	0	0	0	0	0	0	D9	D8	00	
D23-D16	-	0	0	0	0	0	0	0	0	00	

FULLSTEPWINDOWSET Setting Cycle

D2	D1	D0	Description
0	0	0	Input CLK cycle x 4 x 1/2
0	0	1	Input CLK cycle x 4 x 1/4
0	1	0	Input CLK cycle x 4 x 1/8
:	:	:	:
1	0	1	Input CLK cycle x 4 x 1/64
1	1	0	Input CLK cycle x 1/128
1	1	1	Input CLK cycle x 1/256

Set the time to OPEN the motor drive when the excitation mode is FULL STEP during High-efficiency Drive.
Measure the input CLK cycle inside the IC and base on that cycle, decide the period to OPEN.

Non-High-efficiency Drive FULL STEP OPEN Setting

D4	Description
0	'Without' OPEN
1	'With' OPEN

Setting the motor drive to 'with' OPEN when the excitation mode is FULL STEP during non-High-efficiency Drive.
Set when using the STOMGN pin in FULL STEP.

High-efficiency Output OFF Period Setting

D9	D8	Description
0	0	1 CLK range
0	1	2 CLK range
1	0	3 CLK range
1	1	5 CLK range

Set the period to open the output during micro steps of 1/8 STEP or above during High-efficiency driving.

3 Command Register Detailed Description – Continued

3.30 HIEFSELMAX

HIEFSELMAX	Hex	DATA								Initial	Remarks
Command	26	0	0	1	0	0	1	1	0	-	
D7-D0	-	0	0	0	0	0	D2	D1	D0	00	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	CC	
D23-D16	-	D23	D22	D21	D20	0	0	0	0	00	

Pin Setting Mode High-efficiency Drive Current Decay Ratio Upper Limit Integer-side

D2	D1	D0	Description
0	0	0	0
0	0	1	1
0	1	0	2
:	:	:	
1	1	0	6
1	1	1	7

Pin Setting Mode High-efficiency Drive Current Decay Ratio Upper Limit Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	D23	D22	D21	D20	Description
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	0	1	
1	1	1	1	1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	1	1	1	1	

Pin setting mode High-efficiency Drive current decay ratio upper limit
= pin setting mode High-efficiency Drive current decay ratio upper limit integer-side
+ pin setting mode High-efficiency Drive current decay ratio upper limit decimal-side
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D20 = 0.000244141 and so on.

Pin setting mode High-efficiency Drive current decay ratio upper limit is valid only in pin setting mode. Decide the current decay ratio during High-efficiency driving in pin setting mode in conjunction with the set value of HIEFSELMIN command.

On how to decide, refer to HIEFSEL / High-efficiency Drive Setting Pin (Page 12).

3 Command Register Detailed Description – Continued

3.31 HIEFSELMIN

HIEFSELMIN	Hex	DATA								Initial	Remarks
Command	27	0	0	1	0	0	1	1	1	-	
D7-D0	-	0	0	0	0	0	D2	D1	D0	00	
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	01	
D23-D16	-	D23	D22	D21	D20	0	0	0	0	40	

Pin Setting Mode High-efficiency Drive Current Decay Ratio Lower Limit Integer-side

D2	D1	D0	Description
0	0	0	0
0	0	1	1
0	1	0	2
:	:	:	:
1	1	0	6
1	1	1	7

Pin Setting Mode High-efficiency Drive Current Decay Ratio Lower Limit Decimal-side

D15	D14	D13	D12	D11	D10	D9	D8	D23	D22	D21	D20	Description
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	1	0	0.0078125
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	0	0	0.5
:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	1	1	0	1	
1	1	1	1	1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	1	1	1	1	

Pin setting mode High-efficiency Drive current decay ratio lower limit
= pin setting mode High-efficiency Drive current decay ratio lower limit integer-side
+ pin setting mode High-efficiency Drive current decay ratio lower limit decimal-side
The decimal-side are values added to each bit as D15 = 0.5, D14 = 0.25, D20 = 0.000244141 and so on.

Pin setting mode High-efficiency Drive current decay ratio lower limit is valid only in pin setting mode.
Decide the current decay ratio during High-efficiency driving in pin setting mode in conjunction with the set value of HIEFSELMAX command.

On how to decide, refer to HIEFSEL / High-efficiency Drive Setting Pin (Page 12).

3 Command Register Detailed Description – Continued

3.32 UNLOCK

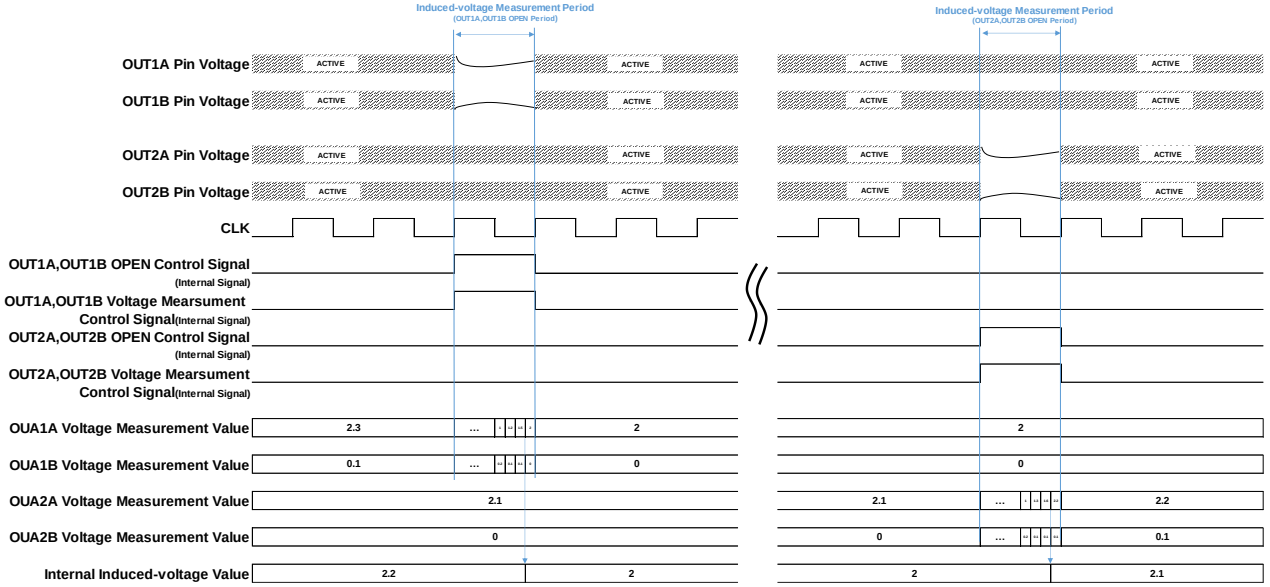
UNLOCK	Hex	DATA								Initial	Remarks
Command	A0	0	0	0	0	0	0	0	1	-	-
D7-D0	-	D7	D6	D5	D4	D3	D2	D1	D0	55	Password1
D15-D8	-	D15	D14	D13	D12	D11	D10	D9	D8	AA	Password2
D23-D16	-	D23	D22	D21	D20	D19	D18	D17	D16	AA	Password3

Setting Password1 = AA, Password2 = 55, Password3 = 55 will enable the Type2 commands (command addresses 10 to 27).
The initial values are Password1 = 55, Password2 = AA and Password3 = AA, and since Type2 command will be disabled after PS is released, always set the Password1 = AA, Password2 = 55 and Password3 = 55 when using the Type2 command.

Induced-voltage Reading Circuit

BD65520MUV measures the voltage of each pin during the period when the output pins OUT1A/OUT1B/OUT2A/OUT2B are OPEN, and calculate the voltage difference between OUT1A, OUT1B / OUT2A and OUT2B.

The measured value immediately before the change from OPEN to ACTIVE is the internally induced voltage value, and based on that value, High-efficiency Drive and step-out margin detection circuit operates.



It is possible to change the averaging and the measurement pin (OUT1A, OUT1B / OUT2A, OUT2B) to measure by register setting (VBEMFAVESET).

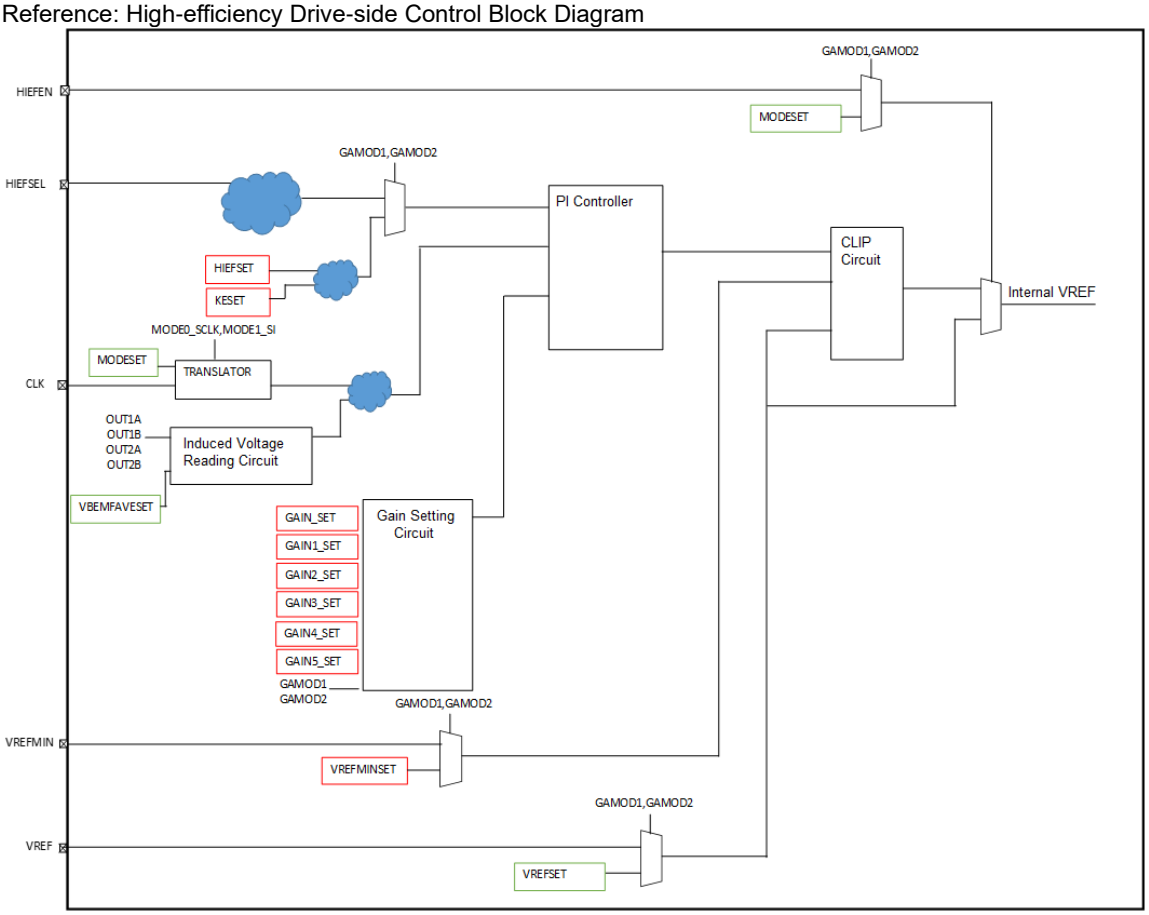
High-efficiency Drive

Adjust the internal VREF with the PI controller from the internal induced-voltage value of the induced-voltage reading circuit, the input cycle of the CLK pin and the excitation mode.
In SPI setting mode, High-efficiency Drive current value can be controlled by KESET register set value and HIEF_SET register set value. In the pin setting mode, the current value of High-efficiency Drive can be controlled by the HIEFSEL input voltage.

The P gain constant and I gain constant settings of the PI controller are decided as follows.

GAMOD2	GAMOD1	P Gain Constant Enabled Register
0	0	GAIN_SET
0	1	GAIN1_SET
1	0	GAIN2_SET
1	1	GAIN_SET
GAMOD2	**GAMOD1**	**I Gain Constant Enabled Register**
0	0	GAIN4_SET
0	1	GAIN5_SET
1	0	GAIN6_SET
1	1	GAIN4_SET

Reference: High-efficiency Drive-side Control Block Diagram



Step-out Margin Detection

Performs the operation below for the internal induced-voltage value of induced-voltage reading circuit, and outputs from the STOMGN pin as analog voltage output.

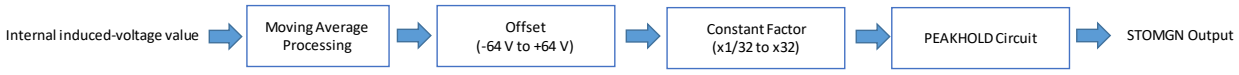


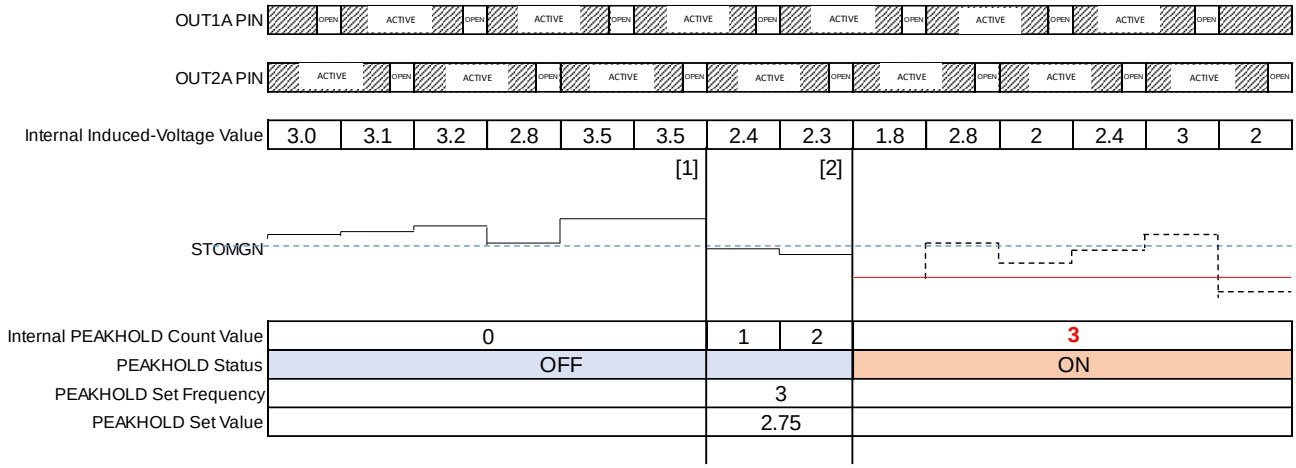
Figure 8. Step-out Margin Detection Block Diagram

Moving average processing, offset and constant factor can be changed by register setting (VBEMFMONSET).
However, adjust the offset and constant factor so that the STOMGN pin output is 0 V < STOMGN < 5 V.
If it is outside the range of 0 V < STOMGN < 5 V, it will be clipped to 0 V and 5 V, respectively.

PEAKHOLD Circuit

If STOMGN_PEAKHOLD_SET is set and the PEAKHOLD function is used, the pre-set threshold voltage below will continue and the STOMGN pin output the constant voltage regardless of internal induced-voltage.

[Waveform Example: PEAKHOLD Count Setting 3 and Threshold 2.75]



When the motor output pin is open, the induced-voltage is read and that value is used as internal induced voltage to calculate the STOMGN pin voltage value. Since the internal induced-voltage is less than or equal to the PEAKHOLD set value in [1], and because it fell below the PEAKHOLD set value three times in a row in [2], the STOMGN pin output will output a constant voltage regardless of the internal induced-voltage.

Power Dissipation

Confirm that the IC's chip temperature Tj is not over 150 °C, while considering the IC's power consumption (W), Thermal Resistance (°C/W) and ambient temperature (Ta). When Tj = 150 °C is exceeded the functions as a semiconductor do not
operate and problems such as parasitism and leaks occur. Constant use under these circumstances leads to deterioration and eventually destruction of the IC. Tjmax = 150 °C must be strictly obeyed under all circumstances.

1 Heat Calculation

The approximate power consumption of the IC can be calculated from the power supply voltage (VCC), circuit current (I_{CC}), output ON resistance (R_{ONH}, R_{ONL}) and motor output current value (I_{OUT}).
Here, the calculation method in FULL STEP drive and SLOW DECAY mode is shown.

$$W_{VCC} = V_{CC} \times I_{CC} \quad [W]$$

W_{VCC} : V_{CC} Power Consumption
V_{CC} : Supply Voltage
I_{CC} : Circuit Current

$$W_{DMOS} = W_{ON} + W_{DECAY} \quad [W]$$

$$W_{ON} = (R_{ONH} + R_{ONL}) \times {I_{OUT}}^2 \times 2 \times on\_duty \quad [W]$$

$$W_{DECAY} = (2 \times R_{ONL}) \times {I_{OUT}}^2 \times 2 \times (1 - on\_duty) \quad [W]$$

Where:
W_{DMOS} is the Output DMOS Power Consumption
W_{ON} is the Output ON Power Consumption
W_{DECAY} is the Power consumption during current regeneration
R_{ONH} is the Top-side Pch DMOS ON Resistance
R_{ONL} is the Bottom-side Nch DMOS ON Resistance
I_{OUT} is the Motor Output Current
on_duty is the PWM on duty= t_{ON}/t_{CHOP}
" 2 " is the H-bridge for 2ch

t_{ON} (Output ON time) differs depending on the inductance and resistance values of the motor coil and the current set value. Check by actual measurement or calculate by estimation.
t_{CHOP} is a chopping cycle determined by the constant current control.

Product No.	Top Pch DMOS ON Resistance R_{ONH} [Ω] (Typ)	Bottom Nch DMOS ON Resistance R_{ONL} [Ω] (Typ)
BD65520MUV	0.35	0.20

$$W\_total = W_{VCC} + W_{DMOS} \quad [W]$$

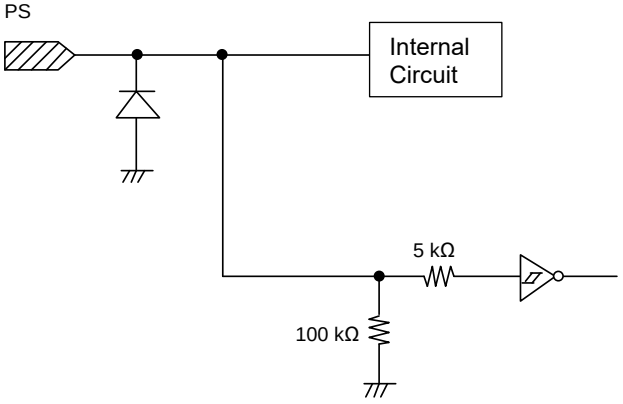
$$Tj = Ta + \theta ja \times W\_total \quad [°C]$$

Where:
W_total is the IC Entirety Power Consumption
Tj is the Temperature Junction
Ta is the Temperature Ambient
θja is the Thermal Resistance

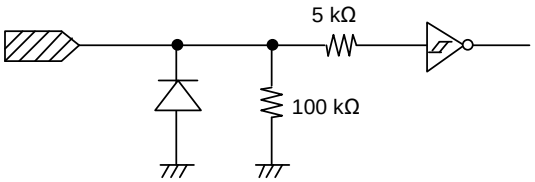
However, the thermal resistance value θja [°C/W] varies greatly depending on the board conditions. The above are only theoretically calculated values. In the actual thermal design, not only the theory but also the thermal evaluation of the application board to be used should be sufficiently performed, and the thermal design should have a sufficient margin so as not to exceed Tjmax = 150 °C. In addition, although it is basically unnecessary in normal usage, when it is used under particularly severe thermal conditions, take into account the heat generation of the IC is reduced by connecting a schottky diode to GND at the motor output pin.

I/O Equivalent Circuit

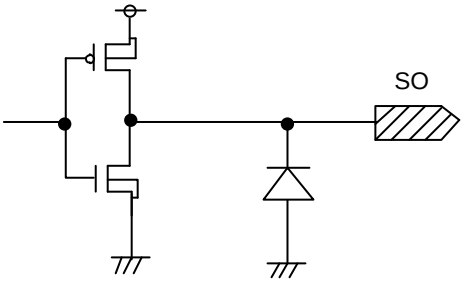
PS



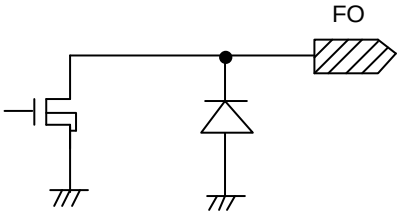
CWCCW_CSB
MODE0_SCLK
MODE1_SI
GAMOD2
GAMOD1
HIEFEN
ENABLE
CLK



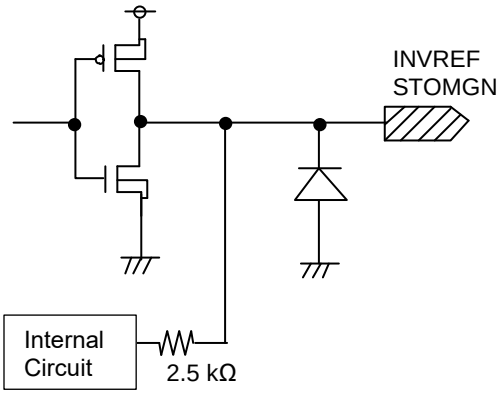
VREGA (Internal Power Supply)

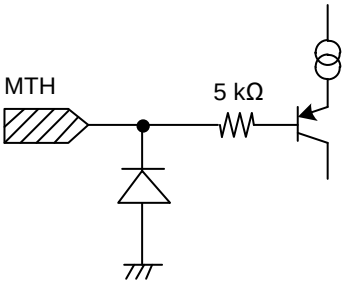


FO

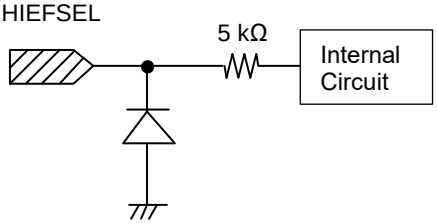


VREGA (Internal Power Supply)

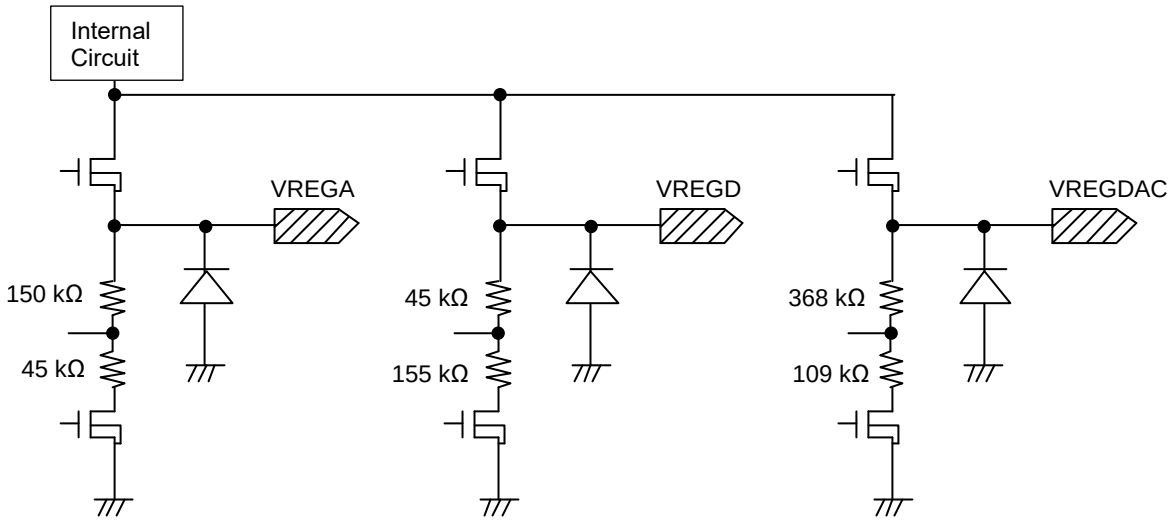




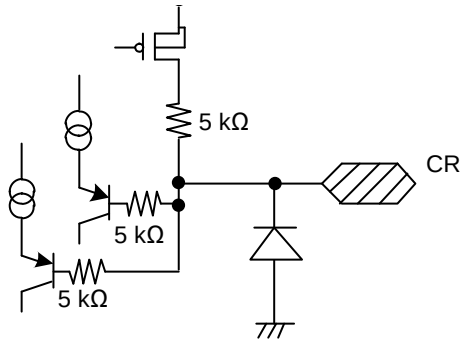
VREF
VREFMIN
HIEFSEL

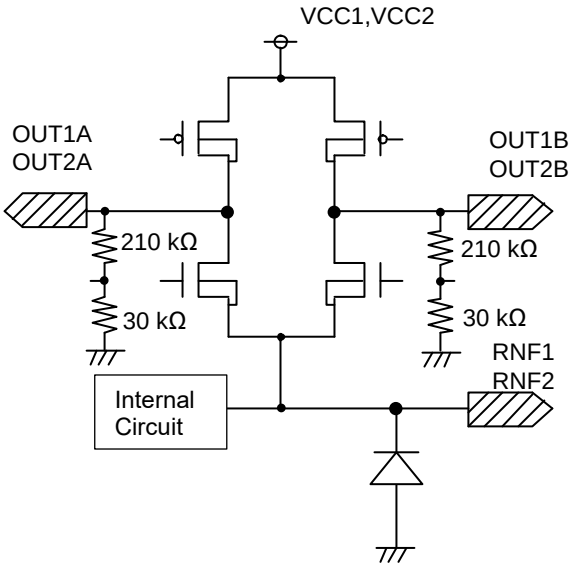


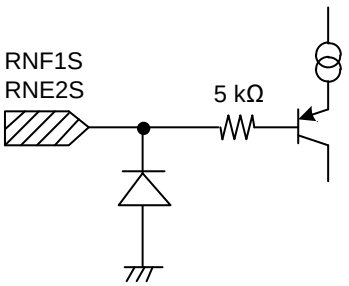
I/O Equivalent Circuit - Continued



VREGA (Internal Power Supply)







Application Example (Pin setting mode)

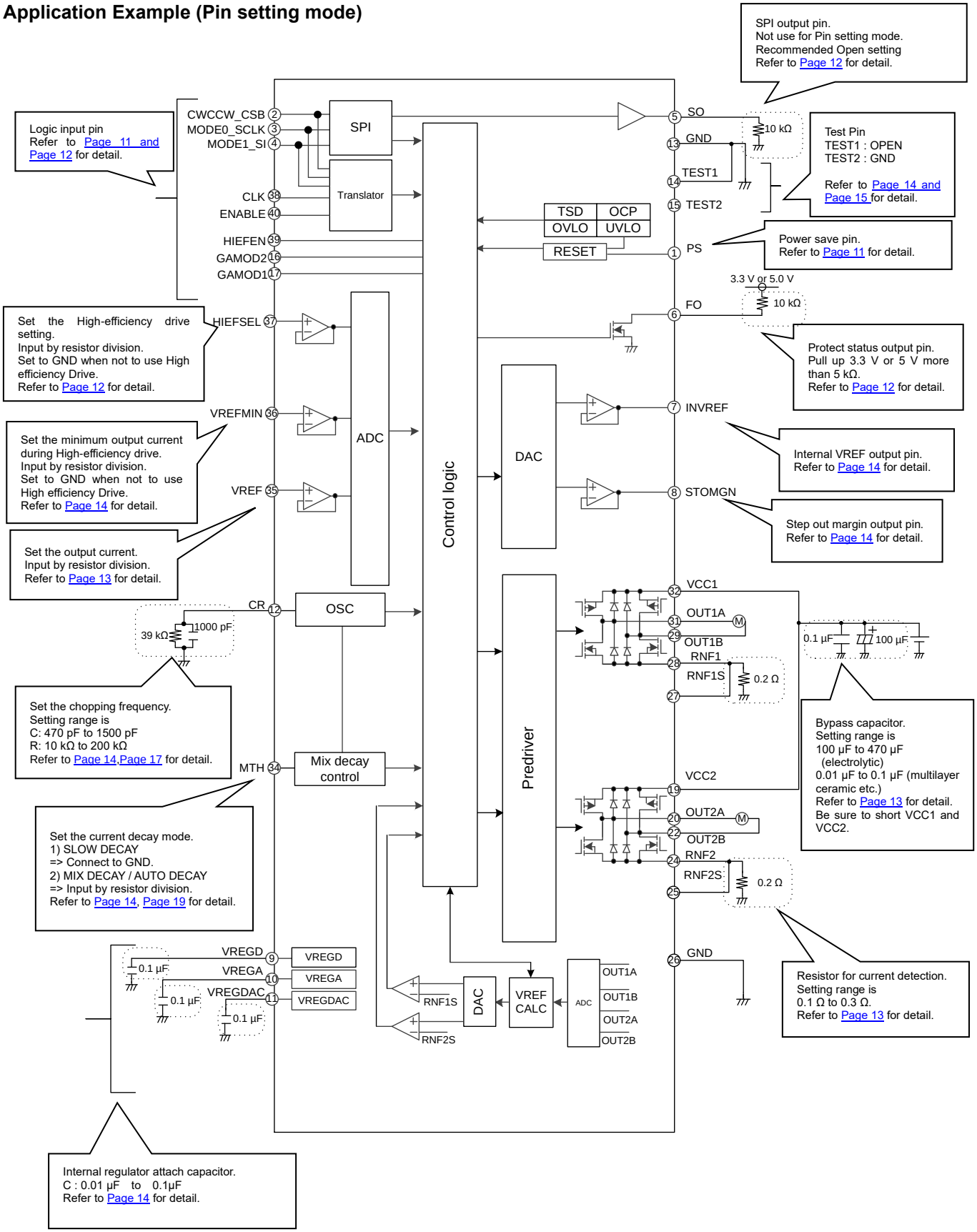


Figure 8. BD65520MUV Application Example (Pin setting mode)

Application Example (SPI setting mode)

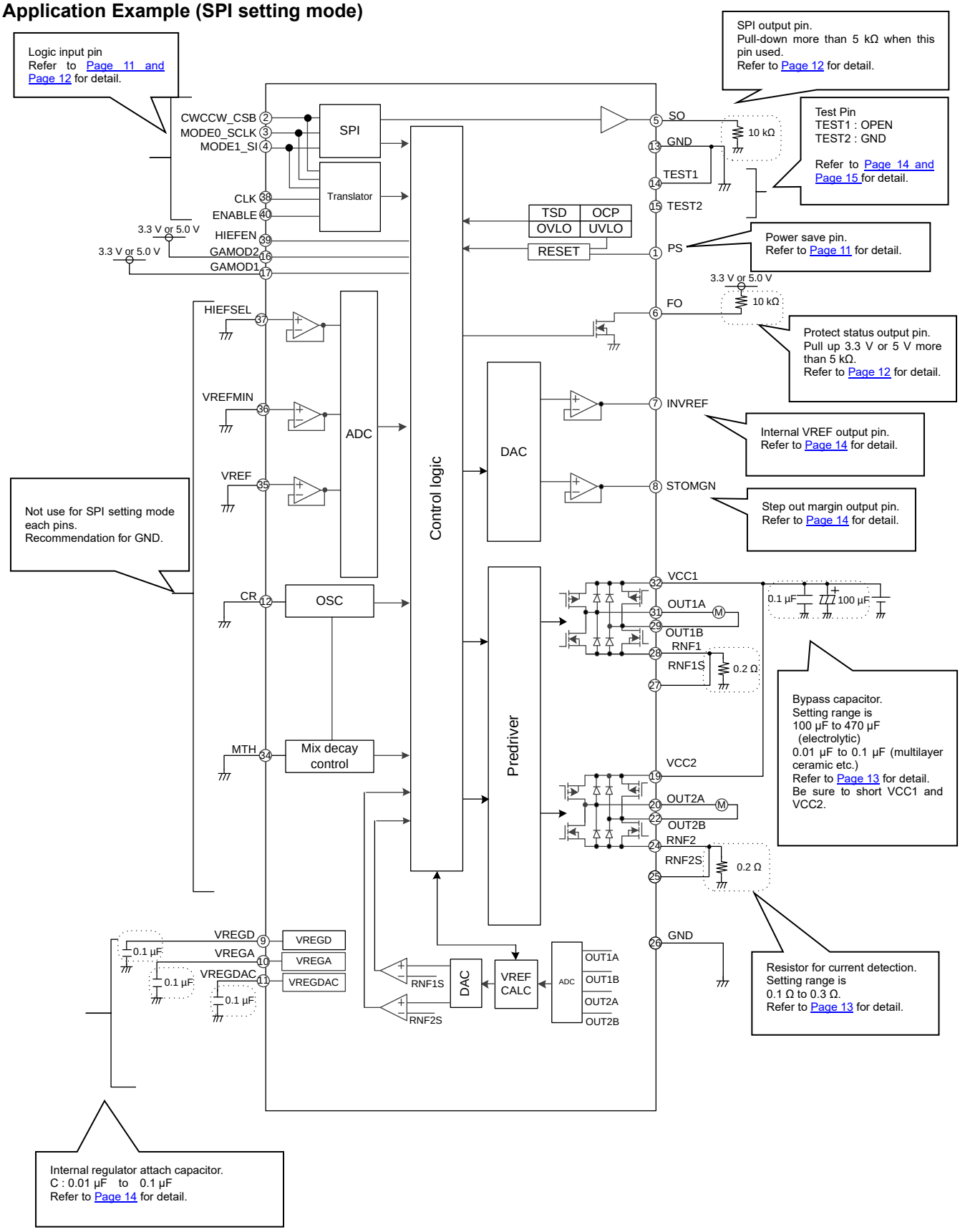


Figure 9. BD65520MUV Application Example (SPI setting mode)

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

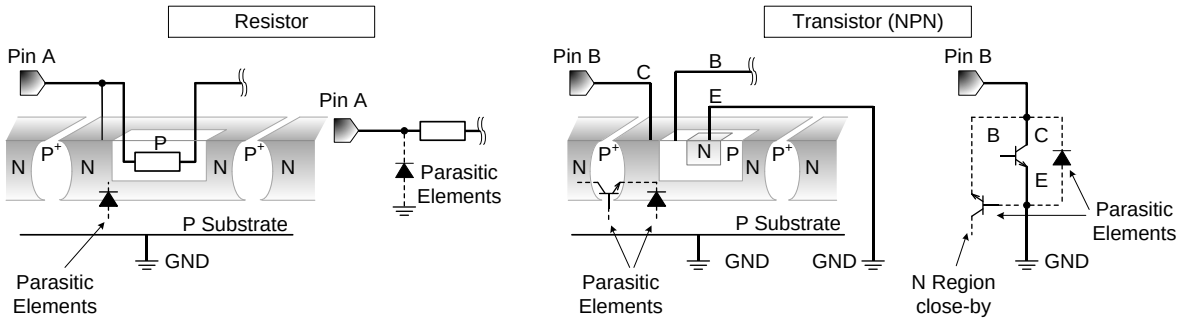


Figure 10. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

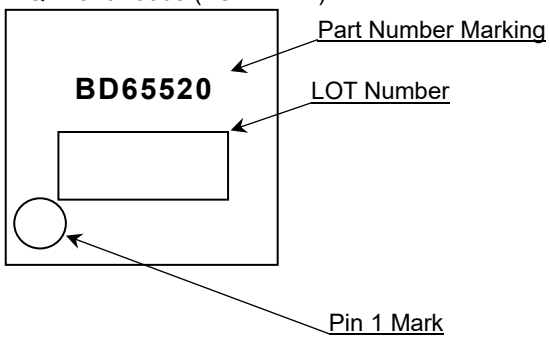
B	D	6	5	5	2	0	M	U	V	-	E 2

Package
MUV: VQFN040V6060

Packing and forming specification
E2: Reel-type embossed taping

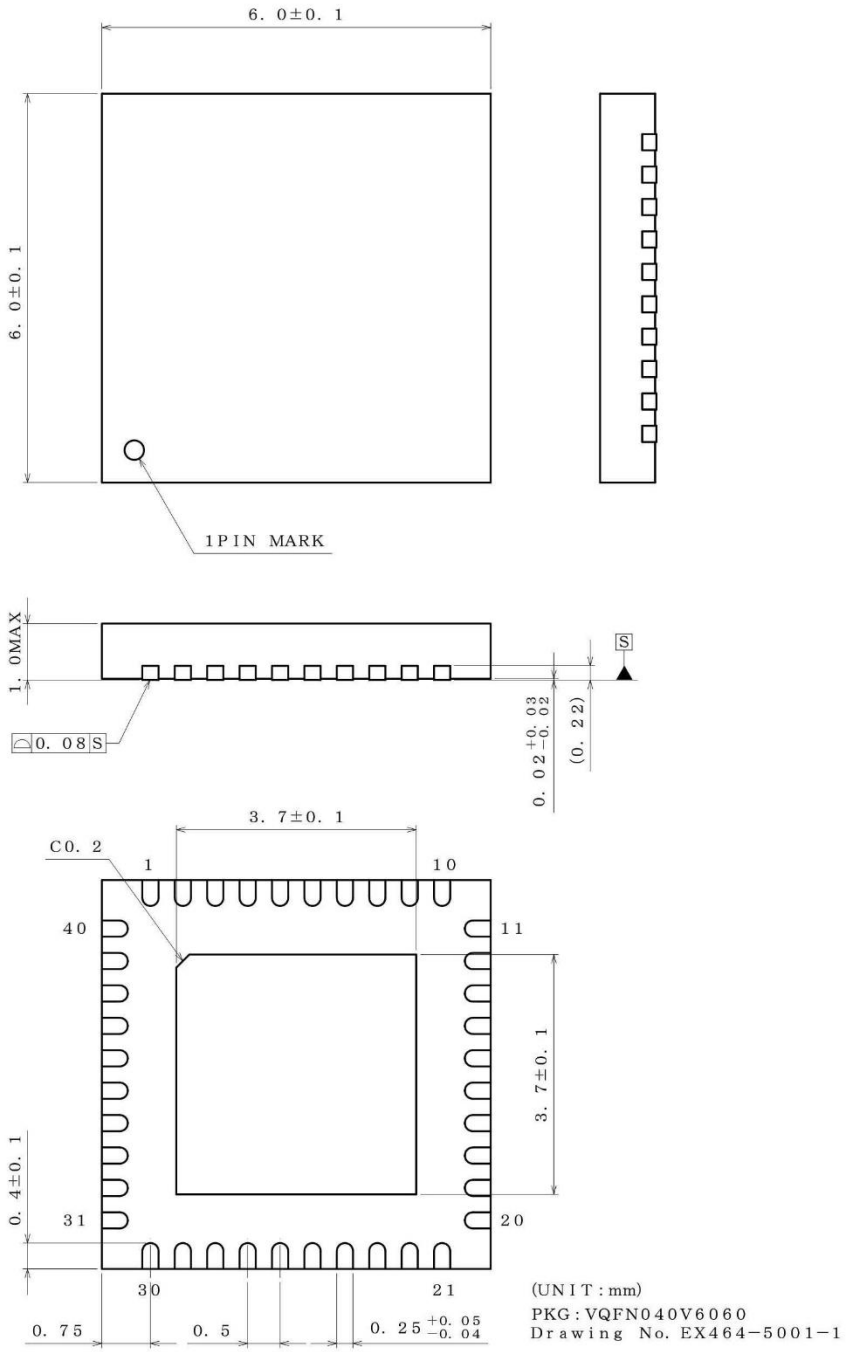
Marking Diagram

VQFN040V6060 (TOP VIEW)



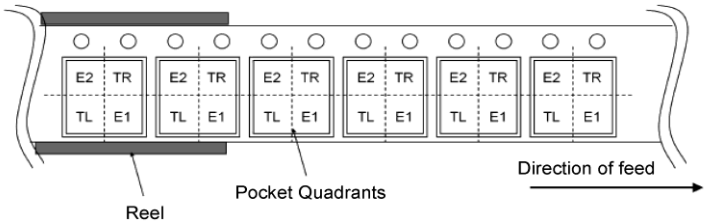
Physical Dimension and Packing Information

Package Name	VQFN040V6060



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Contents of Revision
14.Oct.2021	001	New Release
30.Oct.2023	002	Page 67 Modify RNF setting range. Page 68 Modify RNF setting range.

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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