Bi-directional VCM driver for Auto focus

BU64985GWZ

General Description

The BU64985GWZ is designed to drive Bi-directional voice coil motors. Additionally the driver is able to source the output current without the need for a direction control signal. The driver includes ISRC (intelligent slew rate control) to reduce mechanical ringing to optimize the camera's autofocus capabilities.

Features

- 1.8V Power Supply
- Bi-directional Constant Current Driver
- Current Source and Sink Output
- 10 bit Resolution Current Control
- 2-wire Serial Interface (I^2C Fm+ compatible)
- Integrated Current Sense Resistor
- Power-on Reset
- Thermal Shutdown Protection

Applications

- Mobile Camera Module
- Bi-directional VCM Actuators

Key Specifications

■Power Supply Range:	1.6V to 1.98V
■Standby Current:	0μA (Typ)
■Internal Resistance:	1.3Ω (Typ)
■Master Clock:	400kHz (Typ)
■Maximum Output Current:	+60mA, -60mA (Typ)
■Temperature Range:	-25°C to +85°C

Packages

	W (Typ) x D (Typ) x H (Max)
UCSP30L1A	0.77mm x 1.2mm x 0.33mm

Typical Application Circuit

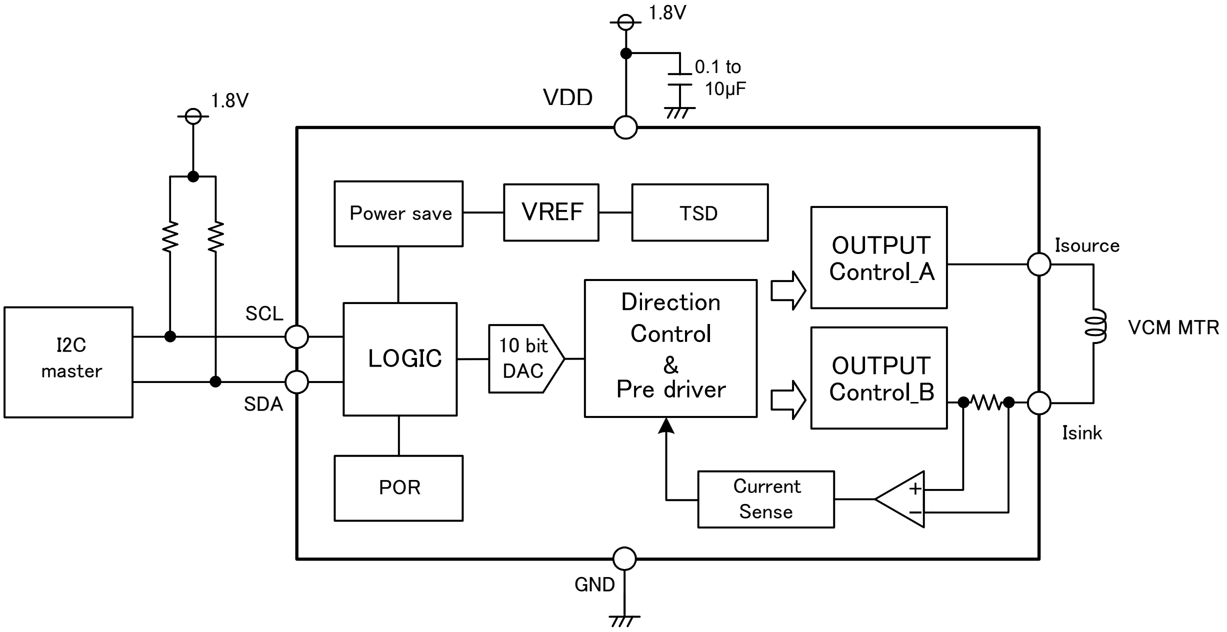


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

Pin Configuration

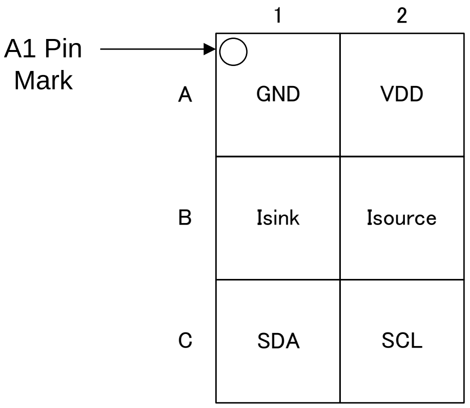


Figure 2. Pin Configuration (Top View)

Pin Descriptions

Pin No.	Symbol	Function
A1	GND	Ground
A2	VDD	Power supply voltage
B1	Isink	Output terminal
B2	Isource	Output terminal
C1	SDA	2-wire serial interface data input
C2	SCL	2-wire serial interface clock input

Block Diagram

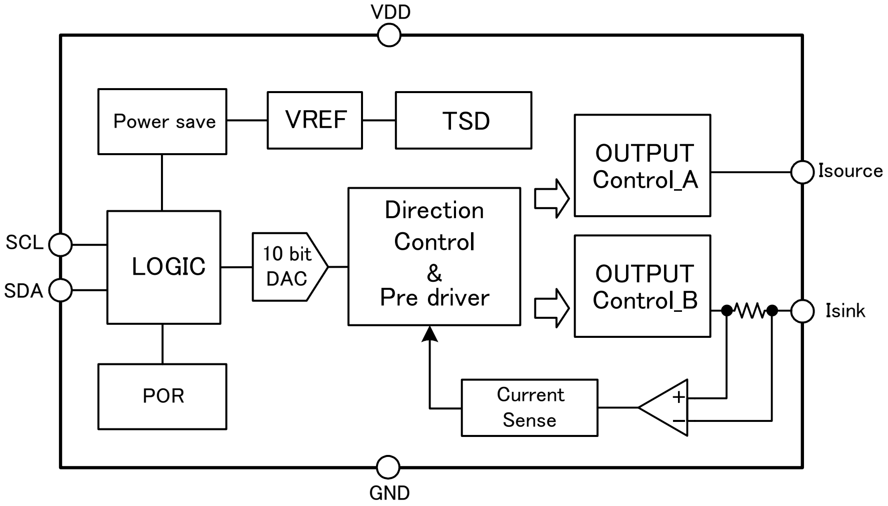


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	-0.5 to +2.5	V
Control Input voltage(Note1)	V_{IN}	-0.5 to +5.5	V
Power Dissipation	Pd	0.32(Note2)	W
Operating Temperature Range	Topr	-25 to +85	°C
Junction Temperature	Tjmax	125	°C
Storage Temperature Range	Tstg	-55 to +125	°C
Output Current	I_{OUT}	+200, -200(Note3)	mA

(Note 1) V_{IN} is 2-wire serial interface input pins (SCL, SDA).
(Note 2) UCSP30L1 package. Derate by 3.2 mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).
(Note 3) Must not exceed Pd, ASO, or Tjmax of 125°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Ratings

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	+1.6 to +1.98	V
Control Input Voltage(Note1)	V_{IN}	0.0 to +4.8	V
2-wire Serial Interface Frequency	f_{CLK}	1	MHz
Output Current	I_{OUT}	+60, -60(Note3)	mA

(Note 1) V_{IN} is 2-wire serial interface input pins (SCL, SDA).
(Note 3) Must not exceed Pd, ASO, or Tjmax of 125°C.

Electrical Characteristics (Unless Otherwise Specified Ta = 25 °C, VDD = 1.8 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Power Consumption						
Standby Current	I_{DDST}	-	0	5	μA	PS bit = 0, EN bit = DNC
Circuit Current 1	I_{DD1}	-	0.9	1.5	mA	PS bit = 1, EN bit = 0
Circuit Current 2	I_{DD2}	-	2.0	3.0	mA	PS bit = 1, EN bit = 1
Control Input (VIN = SCL, SDA)						
High Level Input Voltage	V_{INH}	1.2	-	4.8	V	
Low Level Input Voltage	V_{INL}	0	-	0.5	V	
Low Level Output Voltage	V_{INOL}	-	-	0.4	V	IIN = +3mA (SDA)
High Level Input Current	I_{INH}	-10	-	+10	μA	Input Voltage = 0.9 x V_{IN}
Low Level Input Current	I_{INL}	-10	-	+10	μA	Input Voltage = 0.1 x V_{IN}
Master Clock						
MCLK Frequency		-5	-	+5	%	400kHz (Typ)
10 Bit D/A Converter (for Controlling Output Current)						
Resolution		-	10	-	bits	
Differential Nonlinearity		-1	-	+1	LSB	
Integral Nonlinearity		-4	-	+4	LSB	
Output Current Performance						
Output Reference Current 1	I_{OREF1}	-3	0	+3	mA	DAC_code=0x200 (Initial Value)
Output Reference Current 2	I_{OREF2}	57	60	63	mA	DAC_code=0x3FF
Output Reference Current 3	I_{OREF3}	-63	-60	-57	mA	DAC_code=0x000
Output Resistance	R_{OUT}	-	1.3	1.7	Ω	

Power-up/Power-down Sequence and Function Timing Diagrams

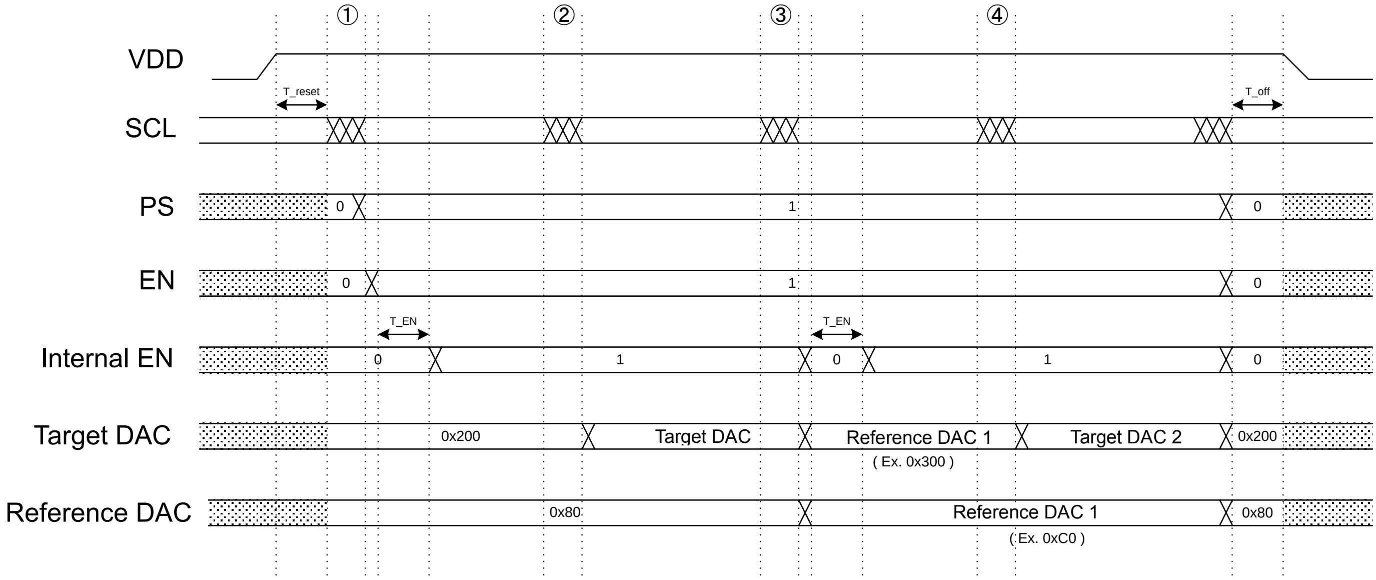


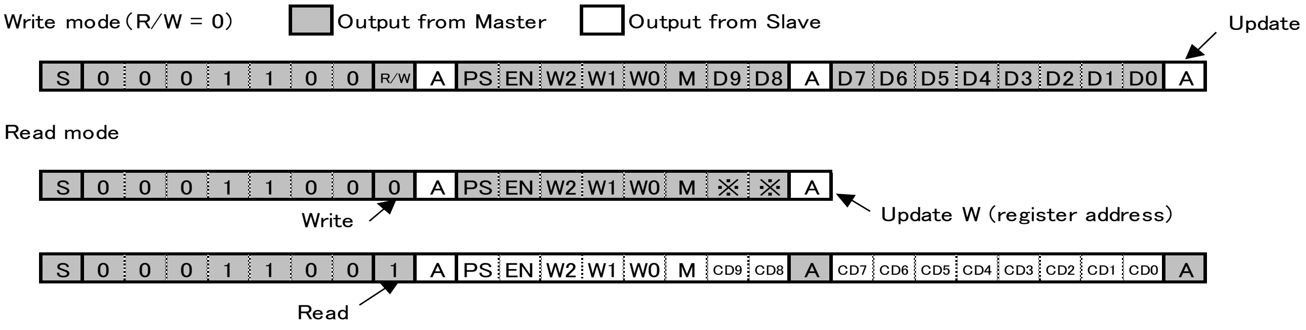
Figure 4. Timing Diagram

The following commands are shown in Figure , the timing diagram:
1=Power save release, 2=Target DAC code change #1, 3=Reference DAC code change, 4=Target DAC code change #2

Table 1. Power Sequence Timing Delays

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Time from VDD going high until first 2-wire Serial Interface command	T_reset	20	-	-	μs
Time delay for rush current protection	T_EN	47.5	50	52.5	μs
Time delay of last 2-wire Serial Interface command until VDD going low	T_off	1.3	-	-	μs

2-wire Serial BUS Format



S : start signal
A : acknowledge
P : stop signal
nA : non acknowledge
※ : Don`t care

Register Name	Setting Item	Description	Initial Value
R/W	Read/Write Setting	0 = Write to serial registers, 1 = Read from serial registers	0
PS	Serial Power Save	0 = Driver in standby mode, 1 = Driver in operating mode	0
EN	Enable	0 = Output current set to zero & idling current set to zero, 1 = Constant current drive	0
W2W1W0	Register Address	000 = Don’t care	0x0
		001 = Don’t care	
		010 = Target position DAC code [D9:D0]	
		011 = Reference DAC code [D7:D0]	
		100 = Actuator resonance frequency[D7:D3], Slew rate [D1:D0]	
		101 = ISRC setting – point A [D9:D0]	
		110 = ISRC setting – point B [D9:D0]	
		111 = Step resolution [D7:D5], Step time[D4:D0]	
M	Mode Select Signal	0 = Direct mode, 1 = ISRC or Step mode	0
D9 to D0	10-bit Data Setting	10-bit data programmed to the corresponding register address	0x200

Characteristics of the SDA and SCL Bus Lines for 2-wire Serial Interface (Ta = 25 °C, VDD = 1.6 to 1.98V)

Parameter	Symbol	STANDARD-MODE(Note 4)		FAST-MODE(Note 4)		Fm+(Note 4)		Unit
		Min	Max	Min	Max	Min	Max	
Hysterics of Schmitt trigger inputs	Vhys	-	-	0.05VDD	-	0.05VDD	-	V
Pulse width of spikes which must be suppressed by the input filter	tSP	0	50	0	50	0	50	ns
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	4.0	-	0.6	-	0.26	-	µs
LOW period of the SCL clock	tLOW	4.7	-	1.3	-	0.5	-	µs
High period of the SCL clock	tHIGH	4.0	-	0.6	-	0.26	-	µs
Set-up time for repeated START condition	tSU;STA	4.7	-	0.6	-	0.26	-	µs
Data hold time	tHD;DAT	0	3.45	0	0.9	0	0.45	µs
Data set-up time	tSU;DAT	250	-	100	-	50	-	ns
Set-up time for STOP condition	tSU;STO	4.0	-	0.6	-	0.26	-	µs
Bus free time between a STOP and START condition	tBUF	4.7	-	1.3	-	0.5	-	µs

(Note 4) STANDARD-MODE, FAST-MODE, and FAST-MODE PLUS (Fm+) 2-wire Serial Interface devices must be able to transmit or receive at the designated speed. The maximum bit transfer rates are 100 kbit/s for STANDARD-MODE devices, 400 kbit/s for FAST-MODE devices, and 1 Mbit/s for Fm+ devices.This transfer rates is based on the maximum transfer rate. For example the bus is able to drive 100 kbit/s clocks with Fm+.

2-wire Serial Interface Timing

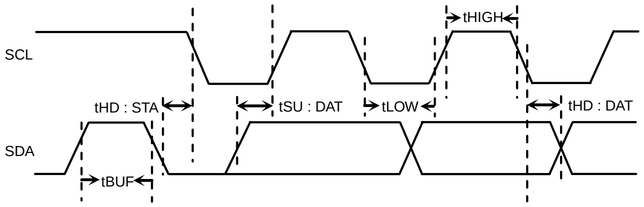


Figure 5. Serial Data Timing

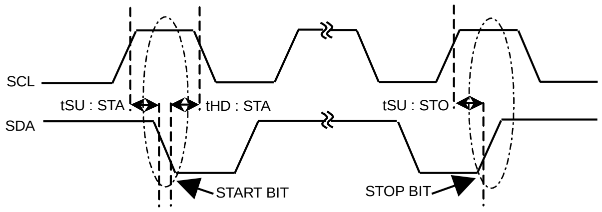


Figure 6. START and STOP Bit Timing

Power Control

The host is able to put the driver in standby mode as well as enable/set the output to Hi-Z via 2-wire Serial Interface. Standby mode is controlled by the PS bit and enable is controlled by the EN bit.

Please note that the PS bit is updated after the second byte is written/the second ACK from the driver is outputted during a three byte write. The EN bit is updated after the third byte is written/the third ACK from the driver is outputted during a three byte write. The third byte write is not required if only the standby (PS) setting is being updated.

Table 2. Power Control Register Data Format

Control Bit	Value	Function
PS	0	Driver in standby mode
	1	Driver in operating mode
EN	0	Driver output is Hi-Z
	1	Driver output is enabled

Description of Output Current Characteristics

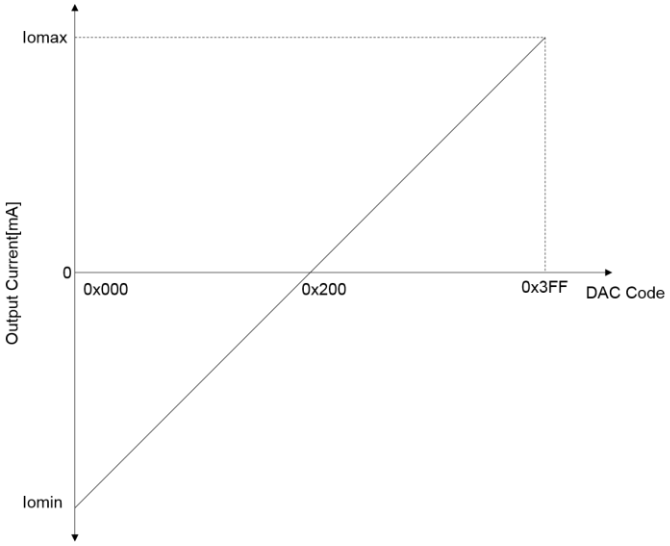


Figure 7. Description of Output Current Characteristics

The BU64985GWZ allows for configurable positive and negative output currents as well as the 0mA zero-cross reference point (REF). The 0mA REF value is set by modifying the W[2:0]=0b011 register with an 8-bit DAC code offset by 2 LSBs. For example a REF value of 0x55 is normally shown as [0101 0101] or DEC 085, however after adding 2 zeros to the LSB the binary value becomes [01 0101 0100] which corresponds to HEX 0x154 and DEC 340 for use in the below equation. Based on the adjusted REF value, the maximum output current of the BU64985GWZ is calculated as:

$$Io_{max} = \left(\frac{120}{1023}\right) * (0x3FF - REF) \qquad \text{[mA]}$$

Equation 1. Maximum Output Current Calculation

Additionally, based on the REF value, the minimum output current of the BU64985GWZ is calculated as:

$$Io_{min} = \left(\frac{120}{1023}\right) * -REF \qquad \text{[mA]}$$

Equation 2. Minimum Output Current Calculation

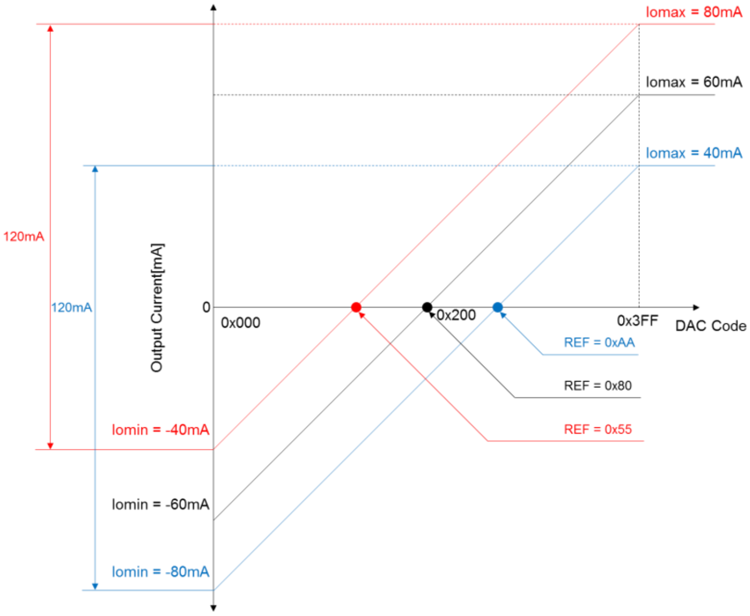


Figure 8. Example of Reference Code Setting

Please note that when calculating a REF value based on a target output current, the resulting REF value needs to be converted to an 8-bit DAC code by removing the 2 LSBs.

The reference DAC should be set based on the properties of the VCM actuator. A traditional VCM actuator uses a barrel that rests against the mechanical end of the actuator when no current is applied to the coil. Using a traditional VCM requires the reference DAC to be set to 0. Bidirectional VCM actuators have the natural position set based on the actuator manufacturers' process. Typically the reference DAC for bidirectional VCM actuators should be set so that the output current range matches the natural full stroke range as closely as possible. The reference DAC is set to 0x80 as a default after power initialization.

Controlling Mechanical Ringing

A VCM is an actuator technology that is intrinsically noisy due to the properties of the mechanical spring behavior. As current passes through the VCM, the lens moves and oscillates until the system reaches a steady state. The BU64985GWZ lens driver is able to control mechanical oscillations by using the integrated ISRC (intelligent slew rate control) function. ISRC is operated by setting multiple control parameters that are determined by the intrinsic characteristics of the VCM. The following illustrates how to best utilize ISRC to minimize mechanical oscillations.

Determining the Resonant Frequency of the VCM

Each VCM has a resonant frequency that can either be provided by the manufacturer or measured. The resonant frequency of an actuator determines the amount of ringing (mechanical oscillation) experienced after the lens has been moved to a target position and the driver output current held constant. To determine the resonant frequency, f_0, input a target DAC code by modifying the 10-bit TDAC[9:0] value in register W[2:0] = 0b010 that will target a final lens position approximately half of the actuator's full stroke. Take care to not apply too much current so that the lens does not hit the mechanical end of the actuator as this will show an incorrect resonant period. In order to start movement of the lens to the DAC code that was set in TDAC[9:0], the EN bit must be set to 1.

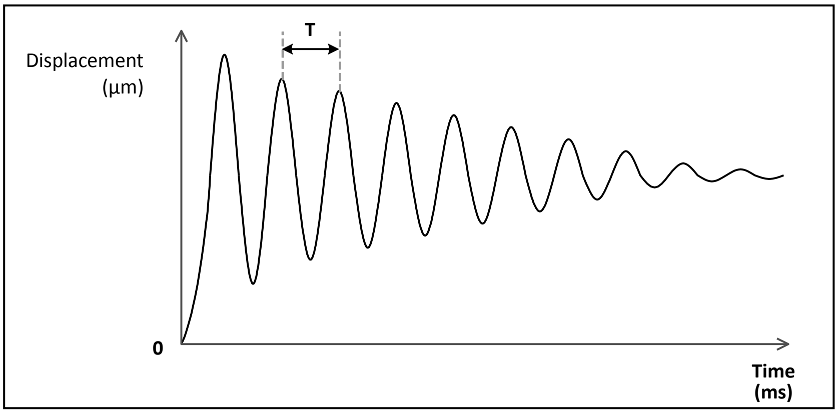


Figure 9. Actuator Displacement Waveform (ISRC Disabled)

The resonant frequency (Hz) of the actuator can be calculated with Equation 3 using the resonant period observed in Figure 9.

$$f_0 = (T)^{-1}$$

Equation 3. Resonant Frequency vs. Time Period Relationship

After calculating the correct resonant frequency, program the closest value in the three MSBs of the third byte of the W[2:0] = 0b100 register using the 5-bit rf[4:0] values from Table . When calculating the resonant frequency take care that different actuator samples' resonant frequencies might vary slightly and that the frequency tolerance should be taken into consideration when selecting the correct driver resonant frequency value.

Table 3. Resonant Frequency Settings

rf[4:0]	f_0	rf[4:0]	f_0	rf[4:0]	f_0	rf[4:0]	f_0
0b00000	-	0b01000	85 Hz	0b10000	125 Hz	0b11000	-
0b00001	50 Hz	0b01001	90 Hz	0b10001	130 Hz	0b11001	-
0b00010	55 Hz	0b01010	95 Hz	0b10010	135 Hz	0b11010	-
0b00011	60 Hz	0b01011	100 Hz	0b10011	140 Hz	0b11011	-
0b00100	65 Hz	0b01100	105 Hz	0b10100	145 Hz	0b11100	-
0b00101	70 Hz	0b01101	110 Hz	0b10101	150 Hz	0b11101	-
0b00110	75 Hz	0b01110	115 Hz	0b10110	-	0b11110	-
0b00111	80 Hz	0b01111	120 Hz	0b10111	-	0b11111	-

Selecting the Autofocus Algorithm's Target DAC Codes

The ISRC algorithm is a proprietary technology developed to limit the ringing of an actuator by predicting the magnitude of ringing created by an actuator and intelligently controlling the output signal of the driver to minimize the ringing effect. Due to the ringing control behavior of ISRC, it is unable to operate properly unless the lens is floating (lens lifted off of the mechanical end of the actuator). As such the ringing control behavior is broken into three separate operational areas in order to provide the most optimally controlled autofocus algorithm. Please note that bidirectional VCM actuators are inherently in a naturally floating position and as a result only the final target position is required for correct ISRC operation.

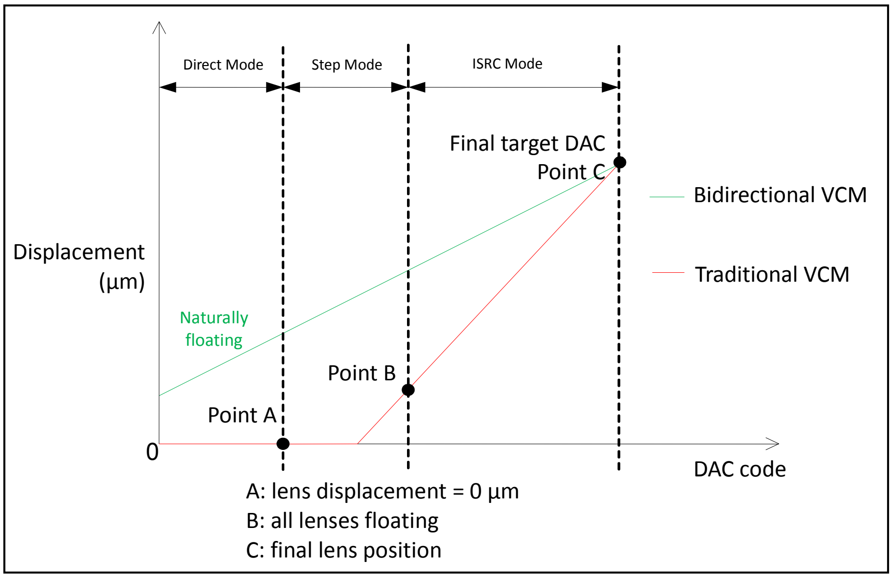


Figure 10. Lens Displacement vs. DAC Code with a Traditional VCM Actuator

Figure 10 illustrates the different operational modes that control the autofocus algorithm. The green line represents the ideal operation sequence of a bidirectional VCM actuator and the red line represents the ideal operation sequence of a conventional VCM actuator. Due to ISRC requiring a floating lens, a traditional VCM actuator (non-bidirectional) requires points A and B to be set in order to create a floating condition. In order to simplify the code sequence, it is possible to skip setting point A and instead only set point B, however if an optimized ringing control method is preferred, point A corresponds to the maximum amount of current that can be applied to all VCM units without floating the lens. Point B corresponds to the minimum amount of current that can be applied to the VCM so that all actuator units are floating. It should be noted that the target DAC codes could vary between different actuator units and that sufficient evaluation should be performed before selecting the point A and B target DAC codes. Point C is the final lens target position determined by the level of focus required for the image capture and bidirectional VCM actuators only require point C for proper ISRC operation.

The actuator manufacturer should be able to provide the required current for points A and B, however it is possible to test these points by slowly increasing the 10-bit value of TDAC[9:0] and measuring the lens movement using a laser displacement meter or some other device to measure lens displacement.

Output Current Control

After characterizing the VCM performance, the following should be performed in order to properly control the driver settings for optimized autofocus performance.

Setting Point A, B, and C DAC Codes

Points A, B, and C are defined by 10-bit DAC codes set with the following registers:

Table 4. Target DAC Code Register Locations

Location	W[2:0] Register	DAC Code Location	Description
Point C	0b010	TDAC[9:0]	Final lens position before image capture
Point A	0b101	ADAC[9:0]	Maximum output current without floating the lens
Point B	0b110	BDAC[9:0]	Minimum output current required to float the lens

Please note that when the reference DAC is set to a non-zero value, due to use with a bidirectional VCM actuator, points A and B are ignored and only point C is used for target DAC positions.

Controlling Direct Mode

Direct mode is when the driver outputs the desired amount of output current with no output current control. The time in which the lens reaches the position that corresponds to the amount of output current set by the 10-bit DAC code is ideally instant, ignoring the ringing effects. If the driver is set so that the lens is moved from a resting position to point C with direct mode, ringing and settling time will be at a maximum.

Direct mode is used either when M=0 or when M=1, the reference DAC is set to 0, and the present DAC code is less than the DAC code of point A.

M = 0 = ISRC mode disabled

When ISRC mode is disabled by setting the M bit equal to 0, the lens will traverse to the DAC code set for point C when the EN bit is set equal to 1.

M = 1 = ISRC mode enabled

The driver automatically uses direct mode if the present DAC code is less than the target DAC code corresponding to point A. Therefore during ISRC operation when the autofocus sequence has been started by setting the EN bit equal to 1, the driver will automatically decide to use direct mode to output current up to point A and then switch to step mode before continuing the autofocus sequence.

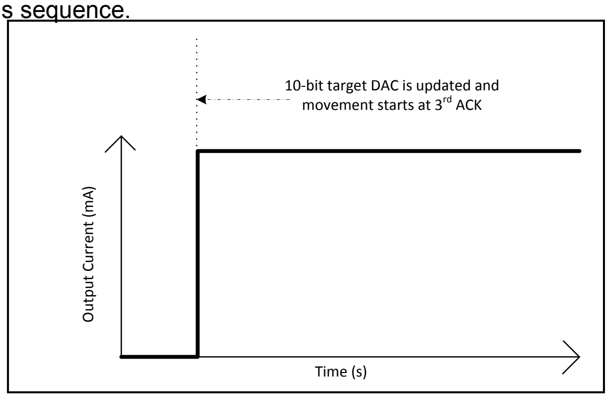


Figure 11. Direct Mode Output Current vs. Time

Controlling Step Mode

Step mode is the control period in which the lens is moved by small output current steps. During step mode it is possible to control the step resolution and step time in order to generate just enough output current to float the lens with minimal ringing effects. Ringing can be better controlled by choosing a large value for the step time and a small value for the step resolution with the trade off of a greater settling time. The step time and step resolution should be chosen depending on the acceptable system limits of ringing vs. settling time.

Step mode is used when M=1, the reference DAC set to 0, and the present DAC code is in between point A and point B. Typically this mode is only used during ISRC operation between point A and B, however it is possible to move the lens to point C using only step mode if point C is set such that point C is only 1 DAC code greater than point B.

Step mode is controlled by the 5-bit step time, stt[4:0], and 3-bit step resolution, str[2:0], values stored in register W[2:0] = 0b111. The step time is set by the 5 LSBs and the step resolution is set by the 3 MSBs of the third byte write while using register W[2:0] = 0b111.

Table 5. Step Time Settings

stt[4:0]	Step Time	stt[4:0]	Step Time	stt[4:0]	Step Time	stt[4:0]	Step Time
0b00000	-	0b01000	400 µs	0b10000	800 µs	0b11000	1200 µs
0b00001	50 µs	0b01001	450 µs	0b10001	850 µs	0b11001	1250 µs
0b00010	100 µs	0b01010	500 µs	0b10010	900 µs	0b11010	1300 µs
0b00011	150 µs	0b01011	550 µs	0b10011	950 µs	0b11011	1350 µs
0b00100	200 µs	0b01100	600 µs	0b10100	1000 µs	0b11100	1400 µs
0b00101	250 µs	0b01101	650 µs	0b10101	1050 µs	0b11101	1450 µs
0b00110	300 µs	0b01110	700 µs	0b10110	1100 µs	0b11110	1500 µs
0b00111	350 µs	0b01111	750 µs	0b10111	1150 µs	0b11111	1550 µs

Table 6. Step Resolution Settings

str[2:0]	Step Resolution	str[2:0]	Step Resolution	str[2:0]	Step Resolution	str[2:0]	Step Resolution
0b000	-	0b010	2 LSB	0b100	4 LSB	0b110	6 LSB
0b001	1 LSB	0b011	3 LSB	0b101	5 LSB	0b111	7 LSB

The BU64985GWZ has an absolute output current range of 120mA which corresponds to a step resolution of 0.117mA/LSB.

Using a normal VCM actuator (non-bidirectional), it is possible to skip step mode during ISRC operation if a simpler autofocus code sequence is desired. If there is no issue with moving the lens to point B using direct mode, then the DAC code for point A should be left equal to 0. Additionally if the point A register is not set after the driver is initialized, then the driver will automatically move the lens to point B with direct mode since the default value for point A is 0.

Controlling ISRC Mode

ISRC mode is the control period in which the lens is already floating and the driver smoothly moves the lens based on the proprietary behavior of the ISRC algorithm. ISRC operation keeps ringing at a minimum while achieving the fastest possible settling time based on the ISRC operational conditions.

ISRC mode is used when M=1, the reference DAC set to 0, and the present DAC code is greater than the DAC code for point B. ISRC mode is also used when M=1 and the reference DAC set to a non-zero value. If the target DAC code for point C is set so that the value is too large and will cause excess ringing, the point C DAC code is automatically updated with a driver pre-determined value to minimize the ringing effect. When M=1 and the reference DAC set to 0, the driver will automatically switch between direct mode, step mode, and ISRC mode when the point A, B, and C DAC code conditions are met. The condition for this automatic transitioning to occur is when the register values for point B and point C are set to values other than 0 and then the sequence will start when the EN bit is set equal to 1. Please note that updates to point B and C DAC codes should be avoided during a focus operation in order to minimize poor ringing effects.

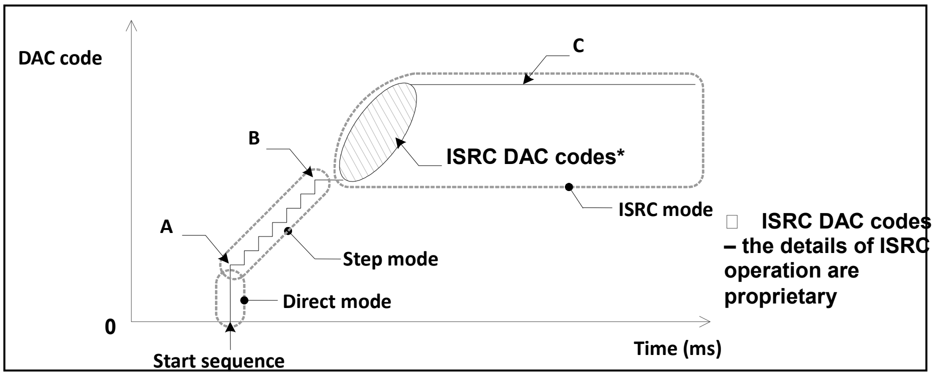


Figure 12. Three Mode Sequential Operation (Shown as DAC Codes) for Traditional VCM Actuators

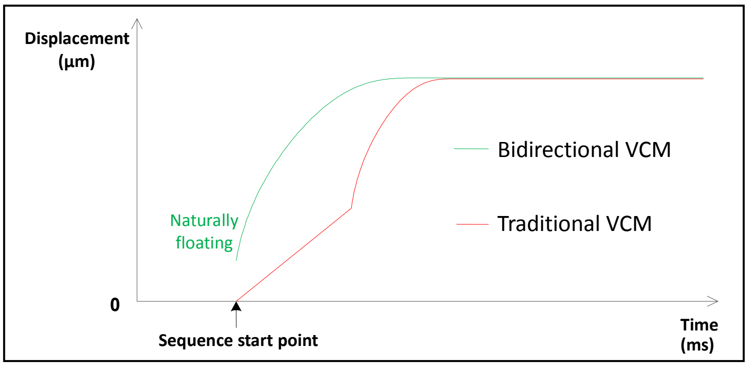


Figure 13. Three Mode Sequential Operation (Shown as Lens Displacement)

Bidirectional VCM actuators require a non-zero reference DAC to be set. If the reference DAC is set to any value other than 0, then the ISRC behavior will ignore point A, point B, and step mode settings and instead only use the point C final target DAC position due to the bidirectional VCM already existing in a floating state.

Controlling the ISRC Settling Time
The settling time of an actuator is the time it takes for ringing to cease. The BU64985GWZ is able to control the settling time by modifying the slew rate speed parameter, however care must be taken to balance settling time vs. acceptable ringing levels. By increasing the slew rate speed there is the possibility to decrease the settling time but the ability to control ringing is also decreased. Likewise, if less ringing is desired then there is a possibility to reduce the ringing levels by using a slower slew rate speed setting at the cost of longer settling times. The slew rate speed can be set by modifying the 2-bit slew_rate[1:0] value located at the 2 LSBs of register W[2:0]=0b100. Figure 4 shows the relationship of slew rate speed vs. settling time.

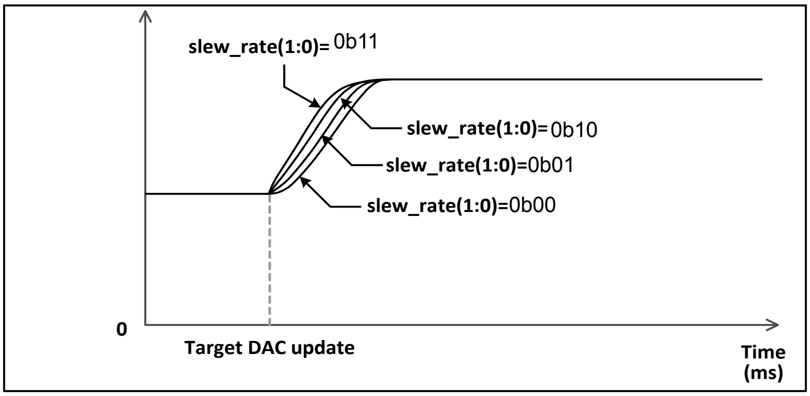


Figure 14. Slew Rate Speed vs. Settling Time

Table 7. Slew Rate Speed Settings

slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed
0b00	Slowest	0b01	Slow	0b10	Fast	0b11	Fastest

DAC Code Update Timing Considerations
Settling time is controlled by the resonant frequency of the actuator and the driver’s slew rate speed setting. Depending on the combination of these parameters, the settling time can be such that updating point C with a new DAC code before the lens has settled at the original point C DAC code can adversely affect the settling time due to increased ringing effects. Utilize the slew rate speed parameter in order to modify the settling time so that any updates to the point C DAC code do not occur before the lens has settled.

Please review the following example based on an actuator with a resonant frequency of 100 Hz:

Table 8. Relationship Between Slew Rate Speed and Settling Time Based on a 100Hz Actuator

Resonance Frequency f_0 (Hz)	slew_rate[1:0]	Settling Time (ms)
100	0b00	40
	0b01	24
	0b10	16
	0b11	12

In this example the settling time of the actuator can vary by up to ±5% due to the internal oscillator (MCLK) having a variance of ±5%. The settling time has a proportionally inverse relationship to the resonant frequency and therefore the settling time can be estimated as:

Table 9. Relationship Between Slew Rate Speed and Settling Time Based on a General Resonant Frequency f_0'

Resonance Frequency f_0' (Hz)	slew_rate[1:0]	Settling Time (ms)
f_0'	0b00	40 * (100 / f_0')
	0b01	24 * (100 / f_0')
	0b10	16 * (100 / f_0')
	0b11	12 * (100 / f_0')

Note that the orientation of the camera module can affect the settling time due to the influence of gravity on the barrel.

Register Map

Final target position, address W[2:0] = 0b010

Bit	Bit Name	Function
D0	TDAC[0]	Target position DAC code [0]
D1	TDAC[1]	Target position DAC code [1]
D2	TDAC[2]	Target position DAC code [2]
D3	TDAC[3]	Target position DAC code [3]
D4	TDAC[4]	Target position DAC code [4]
D5	TDAC[5]	Target position DAC code [5]
D6	TDAC[6]	Target position DAC code [6]
D7	TDAC[7]	Target position DAC code [7]
D8	TDAC[8]	Target position DAC code [8]
D9	TDAC[9]	Target position DAC code [9]

Reference DAC, address W[2:0] = 0b011

Bit	Bit Name	Function
D0	RDAC[0]	Reference DAC code [0]
D1	RDAC[1]	Reference DAC code [1]
D2	RDAC[2]	Reference DAC code [2]
D3	RDAC[3]	Reference DAC code [3]
D4	RDAC[4]	Reference DAC code [4]
D5	RDAC[5]	Reference DAC code [5]
D6	RDAC[6]	Reference DAC code [6]
D7	RDAC[7]	Reference DAC code [7]
D8		
D9		

Actuator settings, address W[2:0] = 0b100

Bit	Bit Name	Function
D0	slew_rate[0]	Slew rate [0]
D1	slew_rate[1]	Slew rate [1]
D2		
D3	rf[0]	Actuator resonance frequency [0]
D4	rf[1]	Actuator resonance frequency [1]
D5	rf[2]	Actuator resonance frequency [2]
D6	rf[3]	Actuator resonance frequency [3]
D7	rf[4]	Actuator resonance frequency [4]
D8		
D9		

Register Map – continued

ISRC parameter, address W[2:0] = 0b101

Bit	Bit Name	Function
D0	ADAC[0]	ISRC setting – point A [0]
D1	ADAC[1]	ISRC setting – point A [1]
D2	ADAC[2]	ISRC setting – point A [2]
D3	ADAC[3]	ISRC setting – point A [3]
D4	ADAC[4]	ISRC setting – point A [4]
D5	ADAC[5]	ISRC setting – point A [5]
D6	ADAC[6]	ISRC setting – point A [6]
D7	ADAC[7]	ISRC setting – point A [7]
D8	ADAC[8]	ISRC setting – point A [8]
D9	ADAC[9]	ISRC setting – point A [9]

ISRC Parameter, address W[2:0] = 0b110

Bit	Bit Name	Function
D0	BDAC[0]	ISRC setting – point B [0]
D1	BDAC[1]	ISRC setting – point B [1]
D2	BDAC[2]	ISRC setting – point B [2]
D3	BDAC[3]	ISRC setting – point B [3]
D4	BDAC[4]	ISRC setting – point B [4]
D5	BDAC[5]	ISRC setting – point B [5]
D6	BDAC[6]	ISRC setting – point B [6]
D7	BDAC[7]	ISRC setting – point B [7]
D8	BDAC[8]	ISRC setting – point B [8]
D9	BDAC[9]	ISRC setting – point B [9]

Step mode settings, address W[2:0] = 0b111

Bit	Bit Name	Function
D0	stt[0]	Step time [0]
D1	stt[1]	Step time [1]
D2	stt[2]	Step time [2]
D3	stt[3]	Step time [3]
D4	stt[4]	Step time [4]
D5	str[0]	Step resolution [0]
D6	str[1]	Step resolution [1]
D7	str[2]	Step resolution [2]
D8		
D9		

Power Dissipation

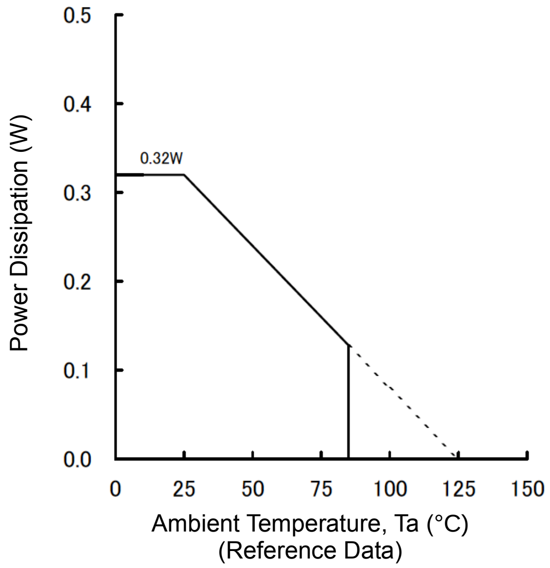


Figure 15. Power Dissipation

I/O Equivalent Circuits

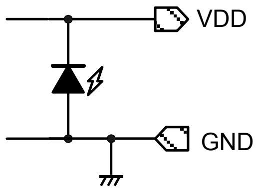
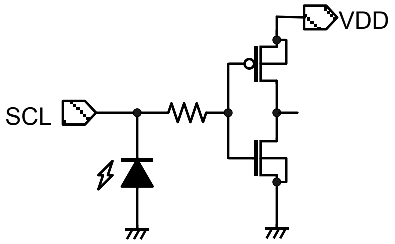
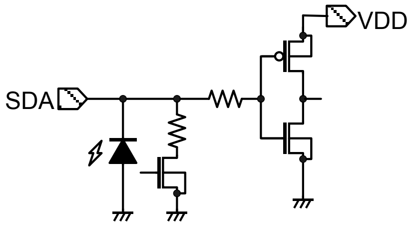
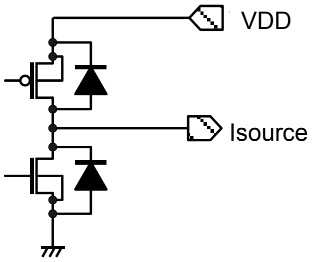
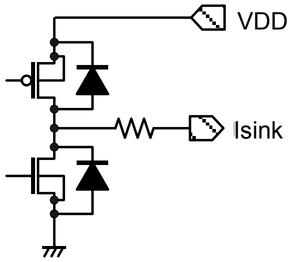
VDD	SCL	SDA
		
Isource	Isink	
		

Figure 16. Pin Equivalent Circuits

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

Operational Notes – continued

13. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

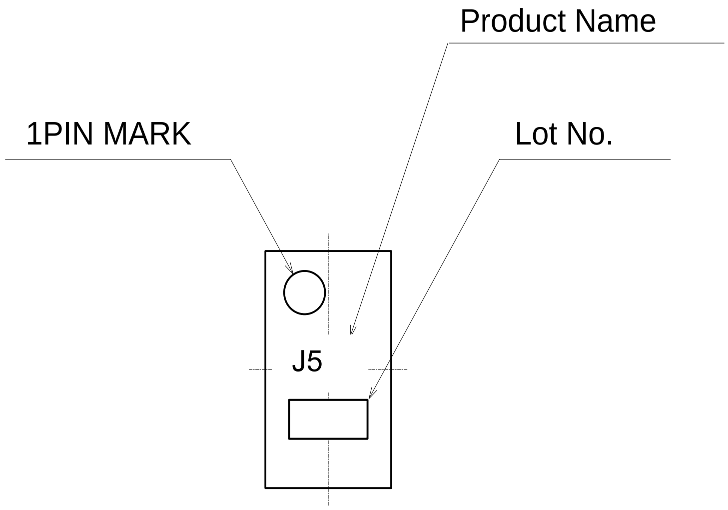
B U 6 4 9 8 5 G W Z   TR

Part Number
64985

Package
GWZ: UCSP30L1A

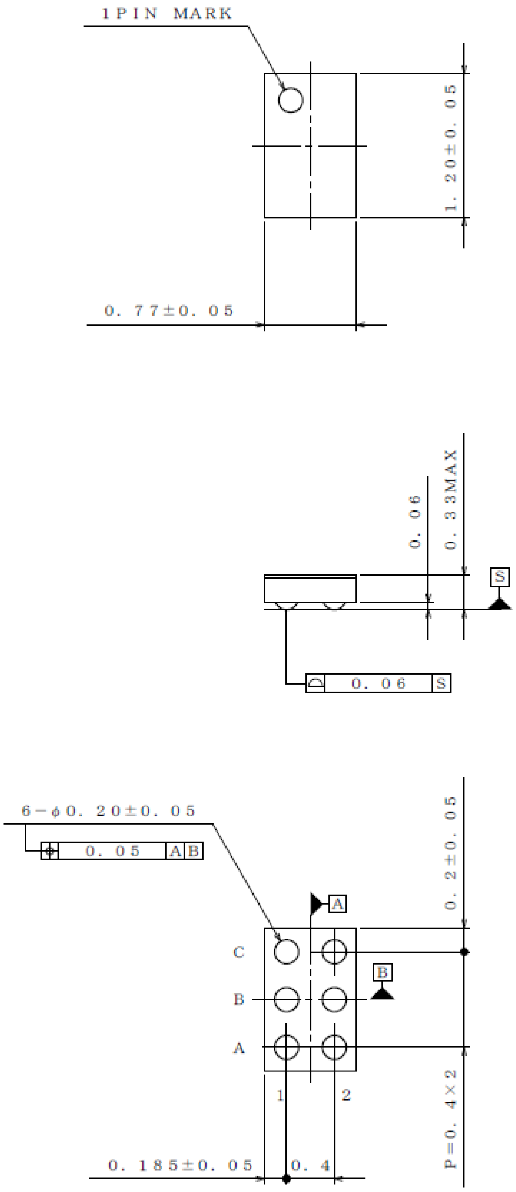
Packaging and forming specification
TR: Embossed carrier tape

Marking Diagrams



Physical Dimension Tape and Reel Information

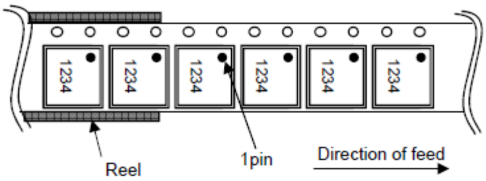
Package Name	UCSP30L1A(BU64985GWZ)



(Unit: mm)

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	6,000pcs
Direction of feed	TR The direction is the pin 1 of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand.



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
24. Jun. 2016	001	New Release
19. Aug. 2016	002	The REF of Figure 8 is changed 0x00 into 0x80. 13. Ceramic Capacitor of Operational Notes changed.
6. Oct. 2016	003	MCLK Frequency of Electrical Characteristics is changed +/-3 into +/-5. Guaranteed operating temperature of 2-wire Serial Interface is changed. Page4　Symbol name is changed.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   - [f] Sealing or coating our Products with resin or other coating materials
   - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   - [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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    [b] the temperature or humidity exceeds those recommended by ROHM
    [c] the Products are exposed to direct sunshine or condensation
    [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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