## Piezoelectric Actuator Driver

## BU64562GWZ

## -General Description

The BU64562GWZ is designed to drive Piezo motors for camera auto focus.
It has an integrated D/A converter for setting the output voltage.
This lens driver includes the slope sequence to reduce the driving noise of Piezo actuator.
The functional lens system can be controlled through 2-wire serial interface ( ${ }^{2} \mathrm{C}$ BUS compatible).

## OKey Specifications

- PMOS ON Resistance:
- NMOS ON Resistance:
- Standby current consumption:

■ High precision 15 MHz Oscillator: $0.70 \Omega$ (Typ.)
$0.70 \Omega$ (Тур.)
$0 \mu \mathrm{~A}$ (Typ.)
$\pm 3 \%$

- Operating temperature range: -25 to $+85^{\circ} \mathrm{C}$
-Package
W(Typ.) x D(Typ.) x H(Max.)
UCSP30L1


## -Features

■ Ultra-small chip size package

- Low ON-Resistance Power CMOS output
- Built-in 15 MHz Oscillator (OSC)
- 2-wire serial interface ( $I^{2} \mathrm{C}$ BUS compatible)
- 1.8 V can be put into each control input terminal
- Slew rate control function of output voltage
- Standby current consumption $0 \mu \mathrm{~A}$ (Typ.)


## - Applications

- Auto focus of cell phone
- Auto focus of Digital still camera
- Camera Modules
- Lens Auto focus
- Web, Tablet and PC Cameras


## -Typical Application Circuit



Figure 1. Typical Application Circuit

## -Pin Configuration

| 1 | 2 | 3 | 4 |
| :---: | :---: | :---: | :---: |
| A | SCL | SDA | OUTA |
| B | GND |  |  |
| PS | VCC | VM | OUTB |

Figure 2. Pin configuration (TOP VIEW)

## -Pin Description

| Ball No. | Ball Name | Function |
| :---: | :---: | :--- |
| A1 | SCL | 2-wire serial interface clock input |
| A2 | SDA | 2-wire serial interface data input |
| A3 | OUTA | Actuator terminal |
| A4 | GND | Ground |
| B1 | PS | Power save input |
| B2 | VCC | Power supply voltage |
| B3 | VM | VM output voltage |
| B4 | OUTB | Actuator terminal |

## -Block Diagram



Figure 3. Block Diagram

## - Absolute Maximum Ratings

| Parameter | Symbol | Limit | Unit |
| :--- | :---: | :---: | :---: |
| Power supply voltage | VCC | -0.3 to +5.5 | V |
| Power save input voltage | VPS | -0.3 to VCC +0.3 | V |
| Control input voltage (SCL, SDA) | VIN | -0.3 to VCC +0.3 | V |
| Power dissipation | Pd | $440^{* 1}$ | mW |
| Operating temperature range | Topr | -25 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Junction temperature | Tjmax | 125 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature range | Tstg | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |
| H-bridge output current | lout | -500 to $+500^{* 2}$ | mA |
|  | lout $($ peak $)$ | -850 to $+850^{* 3}$ | mA |

[^0]
## -Recommended Operating Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Power supply voltage | VCC | 2.3 | 3.0 | 4.8 | V |
| Power save input voltage | VPS | 0 | - | 4.8 | V |
| Control input voltage (SCL, SDA) | VIN | 0 | - | 4.8 | V |
| 2-wire serial interface transmission rate | SCL | - | - | 400 | kHz |
| H-bridge output current | IOUT | - | - | $\pm 400^{* 4}$ | mA |
|  | Iout $_{\text {(peak) }}$ | - | - | $\pm 750^{* 5}$ | mA |

*4 Must not exceed Pd, ASO.
*5 Must not exceed pulse width $=5 \mathrm{~ms}$ and Duty $=50 \%$.

- Electrical Characteristics (Unless otherwise specified $\mathrm{Ta}=\mathbf{2 5}^{\circ} \mathrm{C}, \mathrm{VCC}=3.0 \mathrm{~V}$ )

| Parameter | Symbol | Limit |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |  |
| Overall |  |  |  |  |  |  |
| Circuit current during standby operation | ICCST | - | 0 | 1 | $\mu \mathrm{A}$ | $P S=L$ |
| Circuit current | ICC | - | 1.8 | 3.0 | mA | $\mathrm{PS}=\mathrm{H}, \mathrm{SCL}=400 \mathrm{kHz}, 15 \mathrm{MHz}$ OSC active |
| UVLO |  |  |  |  |  |  |
| UVLO voltage | VUVLO | 1.8 | - | 2.2 | V |  |
| Power save input |  |  |  |  |  |  |
| High level input voltage | VPSH | 1.5 | - | VCC | V |  |
| Low level input voltage | VPSL | 0 | - | 0.5 | V |  |
| High level input current | IPSH | 15 | 30 | 60 | $\mu \mathrm{A}$ | $\mathrm{VINH}=3.0 \mathrm{~V}$, pull down resister $100 \mathrm{k} \Omega$ |
| Low level input current | IPSL | - | 0 | 1 | $\mu \mathrm{A}$ | $\mathrm{VINL}=0 \mathrm{~V}$ |
| Control input(SDA,SCL) |  |  |  |  |  |  |
| High level input voltage | VINH | 1.5 | - | VCC | V |  |
| Low level input voltage | VINL | 0 | - | 0.5 | V |  |
| Low level output voltage1 | VOL1 | - | - | 0.4 | V | IIN $=3.0 \mathrm{~mA} \mathrm{(SDA)}$ |
| Low level output voltage2 | VOL2 | - | - | 0.2 | V | $\mathrm{IIN}=0.7 \mathrm{~mA}(\mathrm{SDA})$ |
| High level input current | IINH | - 10 | - | 10 | $\mu \mathrm{A}$ | Input voltage = VCC |
| Low level input current | IINL | - 10 | - | 10 | $\mu \mathrm{A}$ | Input voltage = GND |
| H Bridge Drive |  |  |  |  |  |  |
| Output ON-Resistance | RONP | - | 0.7 | 0.85 | $\Omega$ |  |
|  | RONN | - | 0.7 | 0.85 | $\Omega$ |  |
| Cycle length of Sequence drive | TMIN | 10.35 | 10.67 | 11.00 | $\mu \mathrm{s}$ | ${ }^{*} 6$ Built in CLK 160 count, no load |
| Output rise time | Tr | - | 0.1 | 0.8 | $\mu \mathrm{s}$ | *7 No load |
| Output fall time | Tf | - | 0.02 | 0.4 | $\mu \mathrm{s}$ | ${ }^{* 7}$ No load |
| VM voltage |  |  |  |  |  |  |
| VM voltage (VM2=0x00) | VM00 | - 10 | 0 | 100 | mV |  |
| VM voltage (VM2=0x8F) | VM8F | 2.6 | 2.7 | 2.8 | V |  |
| VM voltage INL | VMINL | -4 | 0 | 4 |  | DAC_code $=0 \times 20$ to 0xFF, VCC $=4.8 \mathrm{~V}$ |
| VM voltage DNL | VMDNL | - 1 | 0 | 1 |  | DAC_code $=0 \times 20$ to 0xFF, VCC $=4.8 \mathrm{~V}$ |
| VM ON-Resistance | VMR | - | 0.7 | 0.85 | $\Omega$ |  |

*6 The time that 1 cycle of sequence drive at the below setting of 2-wire serial data
$\operatorname{ta}[7: 0]=0 \times 13, \operatorname{brake} 1[7: 0]=0 \times 03, \mathrm{tb}[7: 0]=0 \times 1 \mathrm{E}, \operatorname{brake} 2[7: 0]=0 \times 6 \mathrm{~B}, \mathrm{osc}[2: 0]=0 \times 0$
*7 Output switching wave


## - Typical Performance Curves



Figure 4. Output ON-Resistance (RONP + RONN)


Figure 6. VM voltage (VM2 = 0x8F)


Figure 5. VM ON-Resistance


Figure 7. Cycle length of sequence drive

## -2-wire Serial Interface Register detail



| Register name | Setting item | Description |
| :--- | :--- | :--- |
| PS | Serial power save | $0=$ Driver in standby mode, $1=$ Driver in operating mode |
| $\mathrm{T}[2: 0]$ | Test register <br> address | Test register $=000 \mathrm{~b}$ |
| $\mathrm{~W}[3: 0]$ | Register address | Setting Register address |
| $\mathrm{D}[9: 0]$ | Data bits | Setting Register data |

- Register Map

| Address | W3 | W2 | W1 | wo | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 0$ | 0 | 0 | 0 | 0 | Hize | 0 | 0 | 0 | 0 | START | MODE | dir |
| $0 \times 1$ | 0 | 0 | 0 | 1 | ta[7] | ta[6] | ta[5] | ta[4] | ta[3] | ta[2] | ta[1] | ta[0] |
| 0x2 | 0 | 0 | 1 | 0 | brake1[7] | brake1[6] | brake1[5] | brake1[4] | brake1[3] | brake1[2] | brake1[1] | brake1[0] |
| 0x3 | 0 | 0 | 1 | 1 | tb[7] | tb[6] | tb[5] | tb[4] | tb[3] | tb[2] | tb[1] | tb[0] |
| 0x4 | 0 | 1 | 0 | 0 | brake2[7] | brake2[6] | brake2[5] | brake2[4] | brake2[3] | brake2[2] | brake2[1] | brake2[0] |
| 0x5 | 0 | 1 | 0 | 1 | cnt[7] | $\mathrm{cnt}[6]$ | $\mathrm{cnt}[5]$ | $\mathrm{cnt}[4]$ | cnt[3] | $\mathrm{cnt}[2]$ | $\mathrm{cnt}[1]$ | cnt[0] |
| $0 \times 6$ | 0 | 1 | 1 | 0 | cnt[15] | cnt[14] | cnt[13] | $\operatorname{cnt[12]~}$ | cnt[11] | $\operatorname{cnt[10]}$ | cnt[9] | cnt[8] |
| 0x7 | 0 | 1 | 1 | 1 | pa | pb | osc[2] | osc[1] | osc[0] | cntck[2] | cntck[1] | cntck[0] |
| $0 \times 8$ | 1 | 0 | 0 | 0 | V1[7] | V1[6] | V1[5] | V1[4] | V1[3] | V1[2] | V1[1] | V1[0] |
| 0x9 | 1 | 0 | 0 | 1 | V2[7] | V2[6] | V2[5] | V2[4] | V2[3] | V2[2] | V2[1] | V2[0] |
| 0xA | 1 | 0 | 1 | 0 | step2[4] | step2[3] | step2[2] | step2[1] | step2[0] | step1[2] | step1[1] | step1[0] |
| 0xB | 1 | 0 | 1 | 1 | TEST | TEST | TEST | TEST | TEST | TEST | EXT | TEST |
| 0xC | 1 | 1 | 0 | 0 | TEST | TEST | TEST | TEST | TEST | TEST | TEST | TEST |
| 0xD | 1 | 1 | 0 | 1 | TEST | TEST | TEST | TEST | TEST | TEST | TEST | TEST |

## - Register catalogue

| Bit | Bit Name | Description | Reset |
| :--- | :---: | :--- | :---: |
| Address : 0x0 |  |  |  |
| $\mathrm{D}[7]$ | HiZE | Dead time setting (Reference 13 page) <br> (Lo: 1 cycle of osc[2:0] setting, Hi: Internal CLK 1 cycle (Typ. 66.67 ns)) | $0 \times 0$ |
| $\mathrm{D}[6: 3]$ | TEST | Set ‘0x0' | $0 \times 0$ |
| $\mathrm{D}[2]$ | START | Start setting for sequence (Reference 14 page) | $0 \times 0$ |
| $\mathrm{D}[1]$ | MODE | Mode of brake1 / brake2 setting for sequence (Reference 13 page) | $0 \times 0$ |
| $\mathrm{D}[0]$ | dir | Output direction setting while sequence (Reference 14 page) | $0 \times 0$ |

Address: 0x1

| $\mathrm{D}[7: 0]$ | $\operatorname{ta}[7: 0]$ | Drive waveform setting[7:0] (Reference 10 page) | $0 \times 00$ |
| :--- | :--- | :--- | :--- |

Address : 0x2

| $\mathrm{D}[7: 0]$ | brake1[7:0] | Drive waveform setting[7:0] (Reference 10 page) | $0 \times 00$ |
| :--- | :--- | :--- | :--- |

Address: 0x3

| $\mathrm{D}[7: 0]$ | $\mathrm{tb}[7: 0]$ | Drive waveform setting[7:0] | (Reference 10 page) |
| :--- | :--- | :--- | :--- |


| Address : 0x4 |
| :--- |
| $\mathrm{D}[7: 0]$ |
| brake2[7:0] | Drive waveform setting[7:0] (Reference 10 page) $\quad 0 \times 00$


| D[7:0] | cnt[7:0] | Drive time count setting[7:0] (Reference 12 page) | 0x00 |
| :---: | :---: | :---: | :---: |
| Address : 0x6 |  |  |  |
| D[7:0] | cnt[15:8] | Drive time count setting[15:8] (Reference 12 page) | 0x00 |
| Address : 0x7 |  |  |  |
| D[7] | pa | Output logic setting a (Reference 13 page) | 0x0 |
| D[6] | pb | Output logic setting b (Reference 13 page) | 0x0 |
| D[5:3] | osc[2:0] | Internal CLK basic cycle setting [2:0] (Reference 11 page) | 0x0 |
| $\mathrm{D}[2: 0]$ | cntck[2:0] | Drive time basic cycle setting[2:0] (It is possible to use Normal function only) (Reference 12 page) | 0x0 |


| Address : 0x8 |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| D[7:0] | V1[7:0] | For setting VM voltageBit [7:0] (Refere | ce 16, 17 page) | 0x00 |
| Address: 0x9 |  |  |  |  |
| D[7:0] | V2[7:0] | For setting VM voltageBit [7:0] (Refere | ce 16, 17 page) | 0x00 |
| Address: 0xA |  |  |  |  |
| D[7:3] | step2[4:0] | For setting slope of VM voltageBit [4:0] | (Reference 16, 17 page) | 0x00 |
| D[2:0] | step1[2:0] | For setting slope of VM voltageBit [2:0] | (Reference 16, 17 page) | 0x0 |


| Address : 0xB |  |  |  |
| :---: | :---: | :---: | :---: |
| D[7:2] | TEST | Set '0x0' | 0x00 |
| $\mathrm{D}[1]$ | EXT | Hi output while sequence, Low output at the stop mode (Reference 14 page) | 0x0 |
| D[0] | TEST | Set '0x0' | 0x0 |
| Address : 0xC |  |  |  |
| D[7:0] | TEST | Set '0x00' | 0x00 |

## 2-wire Serial Interface Data timing



Figure 8. Serial data timing


Figure 9. Start, Stop bit timing

Timing Characteristics (Unless otherwise specified, $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{VCC}=2.3$ to 4.8 V )

| Parameter | Symbol | FAST-MODE* ${ }^{\text {* }}$ |  |  | STANDARD-MODE* ${ }^{*}$ |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. | Min. | Typ. | Max. |  |
| SCL clock frequency | fSCL | - | - | 400 | - | - | 100 | kHz |
| High period of the SCL clock | tHIGH | 0.6 | - | - | 4.0 | - | - | $\mu \mathrm{s}$ |
| Low period of the SCL clock | tLOW | 1.3 | - | - | 4.7 | - | - | $\mu \mathrm{s}$ |
| Hold time (repeated) START condition | tHD:STA | 0.6 | - | - | 4.0 | - | - | $\mu \mathrm{s}$ |
| Set-up time (repeated) START condition | tSU:STA | 0.6 | - | - | 4.7 | - | - | $\mu \mathrm{s}$ |
| Data hold time | tHD:DAT | 0 | - | 0.9 | 0 | - | 3.45 | $\mu \mathrm{s}$ |
| Data set-up time | tSU:DAT | 100 | - | - | 250 | - | - | ns |
| Set-up time for STOP condition | tSU:STO | 0.6 | - | - | 4.0 | - | - | $\mu \mathrm{s}$ |
| Bus free time between a STOP and START condition | tBUF | 1.3 | - | - | 4.7 | - | - | $\mu \mathrm{s}$ |
| Pulse width of spikes which must be suppressed by the input filter | tl | 0 | - | 50 | 0 | - | 50 | ns |

*8 Standard-mode and Fast-mode 2-wire serial interface devices must be able to transmit or receive at that speed
The maximum bit transfer rates of 100 kHz for Standard-mode devices and 400 kHz for Fast-mode devices. This transfer rates is provided the maximum transfer rates, for example it is able to drive 100 kHz of clocks with Fast-mode.

## - Recommend to power supply turning on operation timing



Figure 10. Sequence of data input timing to power supply

| Parameter | Symbol | Recommendation limit |  | Unit |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. |  |  |
| PS input High voltage set-up time | tPS 1 | 50 | - | - | $\mu \mathrm{s}$ |
| 2-wire serial interface input data set-up time | tl 2 C 1 | 50 | - | - | $\mu \mathrm{s}$ |
| PS input Low voltage set-up time | tPS 2 | 0 | - | - | $\mu \mathrm{s}$ |
| 2-wire serial interface input data set-up time | tl 2 C 2 | 0 | - | - | $\mu \mathrm{s}$ |

## -Power Dissipation



Figure 11. Power dissipation Pd (W)

## - I/O equivalence circuits

VCC

## - Description of Functions

1) The structure of the driving wave for Piezo actuator

*9 The state at osc $=0 \times 0$ or osc $\neq 0 \times 0$ and $\mathrm{HiZE}=0 \times 0$ is HiZ .
*10 At mode $=0$, the output logic is a setting of a short brake.

| dir (Address: 0x0, Data: D[0]) | Output(1) | Output(2) | Note |
| :---: | :---: | :---: | :---: |
| 0 | OUTA | OUTB | Move to the direction of Macro |
| 1 | OUTB | OUTA | Move to the direction of infinity |

Driving wave is set by the 4 parameters of ta / brake1 / tb / brake2. OSC period is set by the OSC (Internal clock basic cycle setting).
ta $\quad$ On section is ( ta $+1-1$ ) $=$ ta counts for Forward (Reverse) state.
brake1 : On section is (brake1-1) count for short brake state.
tb : On section is (tb1-1) count for Reverse (Forward) state.
brake2 : On section is (brake2-1) count for short brake state.
(Ex.) In case of setting $1 \mathrm{cycle}=10.67 \mu \mathrm{~s}, \mathrm{ta}=1.27 \mu \mathrm{~s}$, brake1 $=0.13 \mu \mathrm{~s}$, $\mathrm{tb}=1.93 \mu \mathrm{~s}$, brake2 $=7.07 \mu \mathrm{~s}$. $\operatorname{osc}[2: 0](=$ Basic cycle setting $)=0 \times 0(=$ Basic cycle $=66.67 \mathrm{~ns})$, and ta $/$ brake1 $/ \mathrm{tb} / \mathrm{brake} 2$ setting below;

| $\operatorname{ta}[7: 0]$ | $=0 \times 13$ | $=19$ count | $\rightarrow$ ON section $=19+1-1=19$ count |
| :--- | :--- | :--- | :--- |
| brake1[7:0] | $=0 \times 03$ | $=3$ count | $\rightarrow$ ON section $=2$ count |
| $\operatorname{tb}[7: 0]$ | $=0 \times 1 \mathrm{E}$ | $=30$ count | $\rightarrow$ ON section $=29$ count |
| brake2[7:0] | $=0 \times 6 \mathrm{~B}$ | $=107$ count | $\rightarrow$ ON section = 106 count |

Table 1. Basic cycle setting [osc] Internal clock 1cycle = 66.67 ns (Typ.)

| osc[2:0] | Internal <br> clock cycle <br> number | osc[2:0] | Internal <br> clock cycle <br> number | osc[2:0] | Internal <br> clock cycle <br> number | osc[2:0] | Internal <br> clock cycle <br> number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 0$ | 1 | $0 \times 2$ | 3 | $0 \times 4$ | 5 | $0 \times 6$ | 7 |
| $0 \times 1$ | 2 | $0 \times 3$ | 4 | $0 \times 5$ | 6 | $0 \times 7$ | 8 |

Table 2. Driving waveform setting [ta]

| ta[7:0] | OSC <br> Cycle <br> number | $\operatorname{ta}[7: 0]$ | OSC <br> Cycle <br> number | ta[7:0] | OSC <br> Cycle <br> number | ta[7:0] | OSC <br> Cycle <br> number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 00$ | 1 | $0 \times 40$ | 64 | $0 \times 80$ | 128 | $0 \times C 0$ | 192 |
| $0 \times 01$ | 1 | $0 \times 41$ | 65 | $0 \times 81$ | 129 | $0 \times C 1$ | 193 |
| $0 \times 02$ | 2 | $0 \times 42$ | 66 | $0 \times 82$ | 130 | $0 \times C 2$ | 194 |
| $0 \times 03$ | 3 | $0 \times 43$ | 67 | $0 \times 83$ | 131 | $0 \times C 3$ | 195 |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| $0 \times 3 D$ | 61 | $0 \times 7 D$ | 125 | $0 \times B D$ | 189 | $0 \times F D$ | 253 |
| $0 \times 3 E$ | 62 | $0 \times 7 \mathrm{E}$ | 126 | $0 \times B E$ | 190 | $0 \times F E$ | 254 |
| $0 \times 3 F$ | 63 | $0 \times 7 F$ | 127 | $0 \times B F$ | 191 | $0 \times F F$ | 255 |

Table 3. Driving waveform setting [brake1]

| brake1[7:0] | OSC <br> Cycle <br> number | brake1[7:0] | OSC <br> Cycle <br> number | brake1[7:0] | OSC <br> Cycle <br> number | brake1[7:0] | OSC <br> Cycle <br> number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 00$ | 1 | $0 \times 40$ | 64 | $0 \times 80$ | 128 | $0 \times C 0$ | 192 |
| $0 \times 01$ | 1 | $0 \times 41$ | 65 | $0 \times 81$ | 129 | $0 \times C 1$ | 193 |
| $0 \times 02$ | 2 | $0 \times 42$ | 66 | $0 \times 82$ | 130 | $0 \times C 2$ | 194 |
| $0 \times 03$ | 3 | $0 \times 43$ | 67 | $0 \times 83$ | 131 | $0 \times C 3$ | 195 |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| $0 \times 3 D$ | 61 | $0 \times 7 \mathrm{D}$ | 125 | $0 \times B D$ | 189 | $0 \times F D$ | 253 |
| $0 \times 3 \mathrm{E}$ | 62 | $0 \times 7 \mathrm{E}$ | 126 | $0 \times B E$ | 190 | $0 \times F E$ | 254 |
| $0 \times 3 F$ | 63 | $0 \times 7 F$ | 127 | $0 \times B F$ | 191 | $0 \times F F$ | 255 |

Table 4. Driving waveform setting [tb]

| tb[7:0] | OSC <br> Cycle <br> number | tb[7:0] | OSC <br> Cycle <br> number | tb[7:0] | OSC <br> Cycle <br> number | $\operatorname{tb[7:0]}$ | OSC <br> Cycle <br> number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 00$ | 1 | $0 \times 40$ | 64 | $0 \times 80$ | 128 | $0 \times C 0$ | 192 |
| $0 \times 01$ | 1 | $0 \times 41$ | 65 | $0 \times 81$ | 129 | $0 \times C 1$ | 193 |
| $0 \times 02$ | 2 | $0 \times 42$ | 66 | $0 \times 82$ | 130 | $0 \times C 2$ | 194 |
| $0 \times 03$ | 3 | $0 \times 43$ | 67 | $0 \times 83$ | 131 | $0 \times C 3$ | 195 |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| $0 \times 3 D$ | 61 | $0 \times 7 D$ | 125 | $0 \times B D$ | 189 | $0 \times F D$ | 253 |
| $0 \times 3 \mathrm{E}$ | 62 | $0 \times 7 \mathrm{E}$ | 126 | $0 \times B E$ | 190 | $0 \times F E$ | 254 |
| $0 \times 3 F$ | 63 | $0 \times 7 F$ | 127 | $0 \times B F$ | 191 | $0 \times F F$ | 255 |

Table 5. Driving waveform setting [brake2]

| brake2[7:0] | OSC <br> Cycle <br> number | brake2[7:0] | OSC <br> Cycle <br> number | brake2[7:0] | OSC <br> Cycle <br> number | brake2[7:0] | OSC <br> Cycle <br> number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 00$ | 1 | $0 \times 40$ | 64 | $0 \times 80$ | 128 | $0 \times C 0$ | 192 |
| $0 \times 01$ | 1 | $0 \times 41$ | 65 | $0 \times 81$ | 129 | $0 \times C 1$ | 193 |
| $0 \times 02$ | 2 | $0 \times 42$ | 66 | $0 \times 82$ | 130 | $0 \times C 2$ | 194 |
| $0 \times 03$ | 3 | $0 \times 43$ | 67 | $0 \times 83$ | 131 | $0 \times C 3$ | 195 |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| $0 \times 3 D$ | 61 | $0 \times 7 D$ | 125 | $0 \times B D$ | 189 | $0 \times F D$ | 253 |
| $0 \times 3 E$ | 62 | $0 \times 7 E$ | 126 | $0 \times B E$ | 190 | $0 \times F E$ | 254 |
| $0 \times 3 F$ | 63 | $0 \times 7 F$ | 127 | $0 \times B F$ | 191 | $0 \times$ FF | 255 |

Table 6. Driving waveform basic cycle setting [cntck] (Normal sequence only)

| cntck[2:0] | Cycle <br> number | cntck[2:0] | Cycle <br> number | cntck[2:0] | Cycle <br> number | cntck[2:0] | Cycle <br> number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 0$ | 1 | $0 \times 2$ | 4 | $0 \times 4$ | 15 | $0 \times 6$ | 64 |
| $0 \times 1$ | 2 | $0 \times 3$ | 8 | $0 \times 5$ | 32 | $0 \times 7$ | 127 |

Table 7. Driving waveform count setting [cnt]

| cnt[15:0] | count <br> cycle <br> number | cnt[15:0] | count <br> cycle <br> number | cnt[15:0] | count <br> cycle <br> number | cnt[15:0] | count <br> cycle <br> number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $0 \times 0000$ | - | $0 \times 4000$ | 16384 | $0 \times 8000$ | 32768 | $0 \times C 000$ | 49152 |
| $0 \times 0001$ | - | $0 \times 4001$ | 16385 | $0 \times 8001$ | 32769 | $0 \times C 001$ | 49153 |
| $0 \times 0002$ | 2 | $0 \times 4002$ | 16386 | $0 \times 8002$ | 32770 | $0 \times C 002$ | 49154 |
| $0 \times 0003$ | 3 | $0 \times 4003$ | 16387 | $0 \times 8003$ | 32771 | $0 \times C 003$ | 49155 |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| $0 \times 3 F F D$ | 16381 | $0 \times 7 F F D$ | 32765 | $0 \times B F F D$ | 49149 | $0 x F F F D$ | 65533 |
| $0 \times 3 F F E$ | 16382 | $0 \times 7 F F E$ | 32766 | $0 x B F F E$ | 49150 | $0 x F F F E$ | 65534 |
| $0 \times 3 F F F$ | 16383 | $0 \times 7 F F F$ | 32767 | $0 x B F F F$ | 49151 | $0 x F F F F$ | 65535 |

Total Drive count number $=(\operatorname{cntck}[2: 0]) \times(\operatorname{cnt}[15: 0]) \quad(\operatorname{cntck}[2: 0]$ is valid for Normal sequence. $)$
(Ex.) In case, setting cntck[2:0] = 0x1, cnt[15:0] = 0x8000
$\operatorname{cntck}[2: 0] \times \operatorname{cnt}[15: 0]=2 \times 32768$
$=65536$ count
$=851.968 \mathrm{~ms}$ (In case of Driving waveform setting a cycle $=13 \mu \mathrm{~s}$ )
2) Driver function table

Sequence setting
mode $=0$, osc $=0 \times 0$ or osc $\neq 0 \times 0$ and HiZE $=0$

|  | I | II | III | IV | V | VI | VII | VII |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output(1) | HiZ | H | Hiz | L | L | L | L | L |
| Output(2) | L | L | L | L | HiZ | H | HiZ | L |
| State | HiZ | Forward | HiZ | Short <br> brake | HiZ | Reverse | Hiz | Short <br> brake |


|  | I | II | III | IV | V | VI | VII | VIII |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output(1) | $\underset{\substack{\rightarrow \mathrm{HiZ}(66.67 \mathrm{~ns}) \\ \hline}}{\text { ( }}$ | H | $\underset{\substack{\rightarrow \mathrm{L}}}{\mathrm{HiZ}(66.6 \mathrm{~ns})}$ | L | L | L | L | L |
| Output(2) | L | L | L | L | $\xrightarrow[\rightarrow H]{\mathrm{HiZ}(66.67 \mathrm{~ns})}$ | H | $\mathrm{HiZ}^{+11}$ | L |
| State | HiZ(66.67ns) $\rightarrow$ Forward | Forward | $\begin{gathered} \text { HiZ(66.67ns) } \\ \rightarrow \text { Short } \\ \text { brake } \\ \hline \end{gathered}$ | Short brake | HiZ(66.67ns) <br> $\rightarrow$ Reverse | Reverse | $\mathrm{Hiz}^{+11}$ | Short brake |

${ }^{*} 11$ The output (2) status of VII doesn't become from $\mathrm{HiZ}(66.67 \mathrm{~ns})$ to Low. It is outputted Hiz.
mode $=1$, osc $=0 \times 0$ or osc $\neq 0 \times 0$ and HiZE $=0$

|  | I | II | III | IV | V | VI | VII |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output(1) | HiZ | H | HiZ | HiZ | L | L | L |
| Output(2) | L | L | L | HiZ | HiZ | H | HiZ |
| State | HiZ | Forward | HiZ | HiZ | HiZ | Reverse | HiZ |
| Hiz |  |  |  |  |  |  |  |

mode $=1$, osc $\neq 0 \times 0$ and HiZE $=1$

|  | I | II | III | IV | V | VI | VII |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Output(1) | HiZ(66.67ns) <br> $\rightarrow H$ | H | HiZ | HiZ | L | L | $\mathrm{L}^{\text {Hi }}$ |
| Output(2) | L | L | L(66.67ns) <br> $\rightarrow$ HiZ | HiZ | HiZ(66.67ns) <br> $\rightarrow$ H | H | HiZ |
| State | HiZ(66.67ns) <br> $\rightarrow$ Forward | Forward | HiZ | HiZ | HiZ(66.67ns) <br> $\rightarrow$ Reverse | Reverse | HiZ |

*12 The output (1) status of VII doesn't become from Low (66.67 ns) to HiZ. It is outputted Low.
Truth table of pa and pb

| sequence | pa | pb | OUTA | OUTB | Function mode |
| :---: | :---: | :---: | :---: | :---: | :---: |
| OFF | 0 | 0 | HiZ | HiZ | STOP |
| OFF | 0 | 1 | L | H | Reverse |
| OFF | 1 | 0 | H | L | Forward |
| OFF | 1 | 1 | L | L | Short brake |
| ON | x | x | - | - | Follow with the sequence |

3) Normal sequence

Setting ta[7:0], brake1[7:0], tb[7:0], brake2[7:0], osc[2:0], HiZE, pa, pb, cntck[2:0], cnt[15:0], V2[7:0]
(When START bit is High, it is impossible to update. When Start bit is Low, it is possible to update.)



## 4) STOP sequence

It changes to the next state after short brake $16.7 \mu \mathrm{~s}$ (Typ.) when the state transition.
Shown in the following while the sequence is operating is done.

- When normal sequence ends
- When normal sequence cancels
* Special condition

There is a possibility that is not the pulse when $\{0 \times 6,0 \times 5\}$ address is small when Dir and START Bits are input at the same time after reset is released.
5) Output rise, fall waveform


A voltage $=($ VM voltage $)-($ Simulation DC output current at the only Resistance load) $\times$ (Upper side output ON-Resistance)
B voltage $=($ Simulation DC output current at the only Resistance load $) \times($ Lower side output ON-Resistance $)$
(Ex.) In case, the load is Resistance element $=2 \Omega$, capacity element $=0.033 \mu \mathrm{~F}$
$25^{\circ} \mathrm{C}, \mathrm{VM}=3 \mathrm{~V}$, Upper side output ON-Resistance $=1 \Omega$, Lower side output ON-Resistance $=1 \Omega$

A voltage $=(\mathrm{VM}$ voltage $)-((\mathrm{VM}$ voltage $) /(\operatorname{Load}(\mathrm{R})+$ Total ON-Resistance $)) \times$ (Upper side ON-Resistance) $=3 \mathrm{~V}-(3 \mathrm{~V} /(2 \Omega+(1 \Omega+1 \Omega))) \times 1 \Omega$
$=2.25 \mathrm{~V}$

B voltage $=((\mathrm{VM}$ voltage $) /(\operatorname{Load}(\mathrm{R})+$ Total ON-Resistance $)) \times($ Lower side ON-R)
$=(3 \vee /(2 \Omega+(1 \Omega+1 \Omega))) \times 1 \Omega$
$=0.75 \mathrm{~V}$
$\begin{array}{lll}\text { Rise time }=\text { Trise }(\mathrm{A} \times 0.1 \text { to } \mathrm{A} \times 0.9) & & =100 \mathrm{~ns} \text { (Typ.) } \\ \text { Fall time } & =\text { Tfall }((\mathrm{VM}-\mathrm{B}) \times 0.9+\mathrm{B} \text { to }(\mathrm{VM}-\mathrm{B}) \times 0.1+\mathrm{B}) & \\ & =100 \mathrm{~ns} \text { (Typ.) }\end{array}$
6) Setting method of VM voltage slope

The slope can be applied to the VM voltage by setting $\mathrm{V} 1[7: 0], \mathrm{V} 2[7: 0]$, step1[2:0] and step2[4:0]. V1 and V2 are bits for setting VM voltage. The step1 and step2 are bits for setting VM slope. VM voltage increase that it set it every $50 \mu \mathrm{~s}$.

It is necessary to enlarge the setting of V 2 more than V 1 .
LSB of each setting bits does not depend on the VCC voltage (LSB = 4.8 / $255=18.8 \mathrm{mV}$ (Typ.)).

- Normal function

Setting $\mathrm{V} 2[7: 0](\mathrm{V} 1[7: 0]=0 \times 00$, step1[2:0] $=0 \times 0$, step2[4:0] $=0 \times 00)$


- One time slope

Setting $\mathrm{V} 2[7: 0]$ and step2[4:0] (V1[7:0] $=0 \times 00$, step1[2:0] $=0 \times 0$ and cntck[2:0] $=0 \times 0)$

(1) $=50 \mu \mathrm{~s} \times \mathrm{V} 2[7: 0] /$ step2[4:0]
(2) $=50 \mu \mathrm{~s}$ (The first step output the keeping voltage.)
(3) $=50 \mu \mathrm{~s} \times(\mathrm{V} 2[7: 0] / \operatorname{step} 2[4: 0]-1)$
-Two times slope

1. Setting V1[7:0], V2[7:0], step1[2:0] and step2[4:0] (cntck[2:0] = 0x0)

(1) $=50 \mu \mathrm{~s} \times \mathrm{V} 1[7: 0] / \operatorname{step} 1[2: 0]$
(2) $=50 \mu \mathrm{~s} \times(\mathrm{V} 2[7: 0]-\mathrm{V} 1[7: 0]) /$ step2[4:0]
(3) $=50 \mu \mathrm{~s}$ (The first step output the keeping voltage.)
(4) $=50 \mu \mathrm{~s} \times((\mathrm{V} 2[7: 0]-\mathrm{V} 1[7: 0]) /$ step2[4:0] - 1)
(5) $=50 \mu \mathrm{~s} \times \mathrm{V} 1[7: 0] /$ step1[2:0]
2. Setting $\mathrm{V} 1[7: 0], \mathrm{V} 2[7: 0]$ and step2[4:0] (step1[2:0] $=0 \times 0$ and $\operatorname{cntck}[2: 0]=0 \times 0)$

(1) $=50 \mu \mathrm{~s} \times(\mathrm{V} 2[7: 0]-\mathrm{V} 1[7: 0]) /$ step2[4:0]
(2) $=50 \mu \mathrm{~s}$ (The first step output the keeping voltage.)
(3) $=50 \mu \mathrm{~s} \times(\mathrm{V} 2[7: 0]-\mathrm{V} 1[7: 0]) /$ step2[4:0]
3. Setting $\mathrm{V} 1[7: 0], \mathrm{V} 2[7: 0]$ and step1[2:0] (step2[4:0] $=0 \times 00$ and cntck[2:0] $=0 \times 0$ )

(1) $=50 \mu \mathrm{~s} \times \mathrm{V} 1[7: 0] /$ step1[2:0]
(2) $=50 \mu \mathrm{~s}$ (The first step output the keeping voltage.)
(3) $=50 \mu \mathrm{~s} \times \mathrm{V} 1[7: 0] /$ step1[2:0]

## -Operational Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings, such as the applied voltage (VCC) or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.
2) Storage temperature range (Tstq)

As long as the IC is kept within this range, there should be no problems in the IC's performance. Conversely, extreme temperature changes may result in poor IC performance, even if the changes are within the above range.
3) Power supply and wiring

Be sure to connect the power terminals outside the IC. Do not leave them open. Because a return current is generated by a counter electromotive force of the motor, take necessary measures such as putting a Capacitor between the power source and the ground as a passageway for the regenerative current. Be sure to connect a Capacitor of proper capacitance ( 0.1 to $10 \mu \mathrm{~F}$ ) between the power source and the ground at the foot of the IC , and ensure that there is no problem in properties of electrolytic Capacitors such as decrease in capacitance at low temperatures. When the connected power source does not have enough current absorbing capability, there is a possibility that the voltage of the power source line increases by the regenerative current exceeds the absolute maximum rating of this product and the peripheral circuits.
Therefore, be sure to take physical safety measures such as putting a zener diode for a voltage clamp between the power source the ground.
4) Ground terminal and wiring

The potential at GND terminal should be made the lowest under any operating conditions. Ensure that there are no terminals where the potentials are below the potential at GND terminal, including the transient phenomena.
Also prevent the voltage variation of the ground wiring patterns of external components. Use short and thick power source and ground wirings to ensure low impedance.
5) Thermal design

Use a proper thermal design that allows for a sufficient margin of the power dissipation at actual operating conditions.
6) Pin short and wrong direction assembly of the device

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.
7) Avoiding strong magnetic field

Malfunction may occur if the IC is used around a strong magnetic field.
8) ASO

Ensure that the output transistors of the motor driver are not driven under excess conditions of the absolute maximum ratings and ASO.
9) TSD circuit

This IC incorporates a TSD circuit. If the temperature of the chip reaches the below temperature, the motor coil output will be opened. The TSD circuit is designed only to shut off the IC to prevent runaway thermal operation. It is not designed to protect the IC or to guarantee its operation. Do not continue to use the IC after use of the TSD feature or use the IC in an environment where the its assumed that the TSD feature will be used.

| TSD ON temperature $\left[{ }^{\circ} \mathrm{C}\right]$ <br> (Typ.) | Hysteresis temperature $\left[{ }^{\circ} \mathrm{C}\right]$ <br> (Typ.) |
| :---: | :---: |
| 150 | 20 |

10) PS terminal

Release PS after rising VCC. PS works resetting logic as well. If keep connecting PS with VCC, resetting cannot be done cause malfunction or destroy.

## Status of this document <br> The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document formal version takes priority.

## -Ordering Information


E 2
Packaging and forming specification E2: Embossed tape and reel

## -Physical Dimension Tape and Reel Information

UCSP30L1 (BU64562GWZ)


- Marking Diagram(TOP VIEW)


## UCSP30L1 (BU64562GWZ)



## -Revision History

| Date | Revision |  |
| :---: | :---: | :---: |
| 9.Oct.2012 | 001 | New Release |

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| JAPAN | USA | EU | CHINA |
| :---: | :---: | :---: | :---: |
| CLASSIII | CLASSIII | CLASS II b | CLASSIII |
|  |  | CLASSIII |  |

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[h] Use of the Products in places subject to dew condensation
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6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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[d] the Products are exposed to high Electrostatic
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3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
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[^0]:    *1 Conditions: mounted on a glass epoxy board ( $50 \mathrm{~mm} \times 58 \mathrm{~mm} \times 1.75 \mathrm{~mm}$; 8 layers). In case of $\mathrm{Ta}>25^{\circ} \mathrm{C}$, reduced by $4.4 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$.
    *2 Must not exceed Pd, ASO, or Tjmax of $125^{\circ} \mathrm{C}$.
    *3 Must not exceed pulse width $=5 \mathrm{~ms}$ and Duty $=50 \%$.

