Gate Driver for Mobility and Power Tool

4.5 V to 60 V, Three-phase Brushless DC Motor Gate Driver

BD67870MWV-Z

General Description

The BD67870MWV-Z is a gate driver IC designed for three-phase brushless DC motor applications. The BD67870MWV-Z can drive three half-bridges consisting of six N-Channel power MOSFETs up to 60 V.

Features

- Wide 4.5 V to 60 V Input Voltage Range
- Bootstrap Gate Driver with Current Source Circuit for 100 % Duty Cycle Operation and High-impedance (Hi-Z) State with Trickle Charge Pump
- Super Low I_{VCCQ} (< 1 µA at Sleep Mode)
- Thermal Shutdown, Input V_{CC} and Gate Driver V_{REG} UVLO Protection
- Adjustable Dead Time Control by External Resistor from 10 ns to 3000 ns
- 6x PWM Mode (Input Logic)

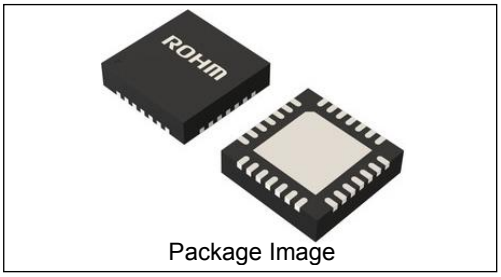
Applications

- Three-Phase, Brushless, DC Motors
- Permanent Magnet Synchronous Motors
- Power Tools
- E-Bikes, Mobility

Key Specifications

V_{CC} Range	4.5 V to 60 V
Gate Driver Strength (Source)	0.5 A (Typ)
Gate Driver Strength (Sink)	1.0 A (Typ)
V_{CC} UVLO	3.8 V (Typ)
Maximum Junction Temperature	+150 °C

Package	W (Typ) x D (Typ) x H (Max)
UQFN28AV040A	4.0 mm x 4.0 mm x 1.0 mm



Package Image

Typical Application Circuits

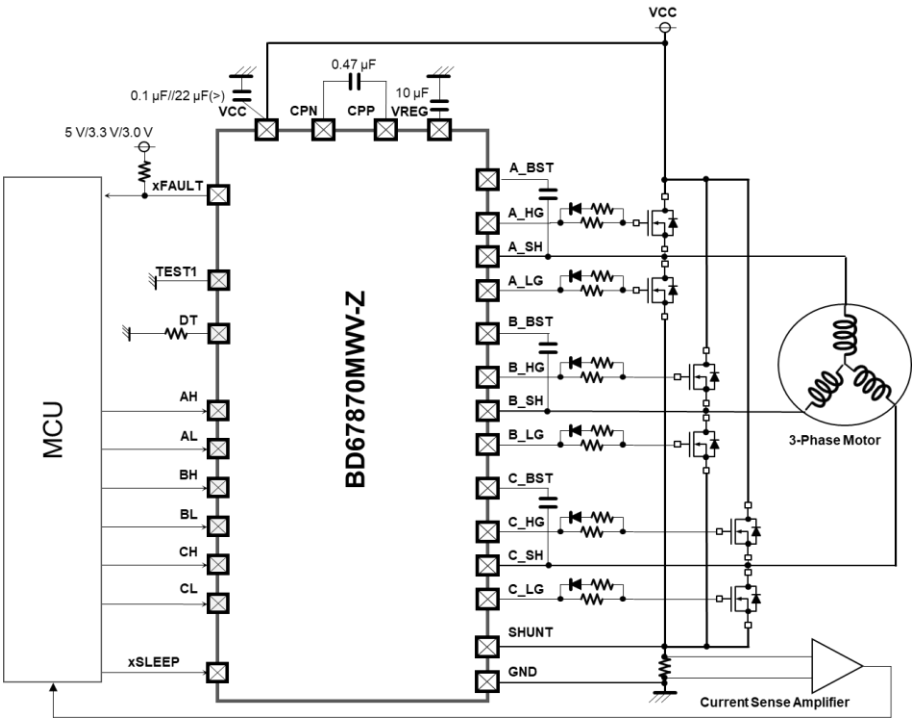


Figure 1. Application Example

Pin Configurations

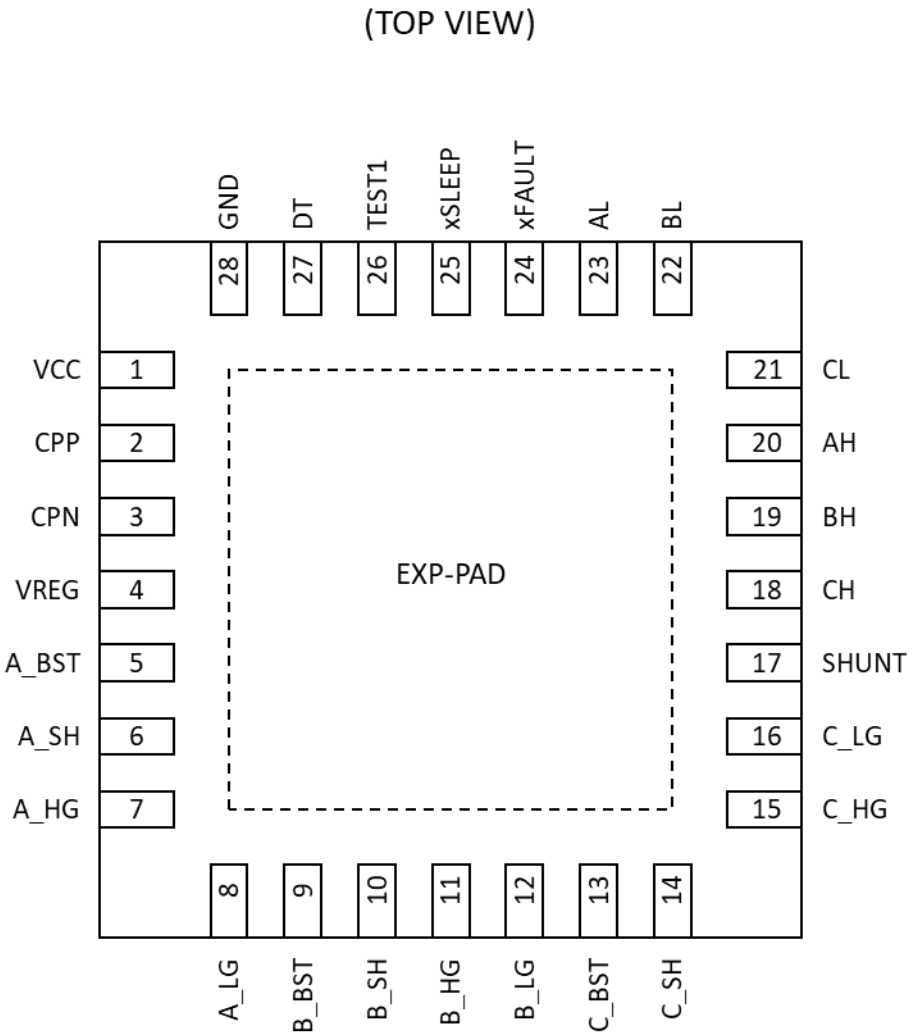


Figure 2. Package Reference

Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Input supply voltage. Bypass VCC to ground with a ceramic and electrolytic capacitor. 0.1μF ceramic capacitor and 22 μF or more electrolytic capacitor are recommended. Apply the same voltage as the drain voltage of the High-side MOSFET
2	CPP	Charge pump capacitor. Connect a ceramic capacitor between CPP and CPN. Ceramic capacitor is recommended. See component selection guide for recommended value.
3	CPN	
4	VREG	Gate drive supply output. Connect a ceramic capacitor between VREG and ground.
5	A_BST	Bootstrap phase A. Connect a ceramic capacitor to A_SH. See component selection guide for recommended value.
6	A_SH	High-side source connection phase A.
7	A_HG	High-side gate drive output phase A.
8	A_LG	Low-side gate driver output phase A.
9	B_BST	Bootstrap phase B. Connect a ceramic capacitor to B_SH. See component selection guide for recommended value.
10	B_SH	High-side source connection phase B.
11	B_HG	High-side gate driver output phase B.
12	B_LG	Low-side gate drive output phase B.
13	C_BST	Bootstrap phase C. Connect a ceramic capacitor to C_SH. See component selection guide for recommended value.
14	C_SH	High-side source connection phase C.
15	C_HG	High-side gate driver output phase C.
16	C_LG	Low-side gate driver output phase C.
17	SHUNT	Return path for low-side driver.
18	CH	Phase C high-side input.
19	BH	Phase B high-side input.
20	AH	Phase A high-side input.
21	CL	Phase C low-side input.
22	BL	Phase B low-side input.
23	AL	Phase A low-side input.
24	xFAULT	Open drain fault indicator pin.
25	xSLEEP	When the xSLEEP pin is driven to ground, the gate driver device is put into sleep mode
26	TEST1	Test output pin for internal use. For normal application this pin connect to GND or pull up to VREG with 100 kΩ.
27	DT	Pin to connect external dead time adjustment resistor. See operation section for calculation of resistor value.
28	GND	Ground.
-	EXP-PAD	Connect exposed pad to GND

Block Diagram

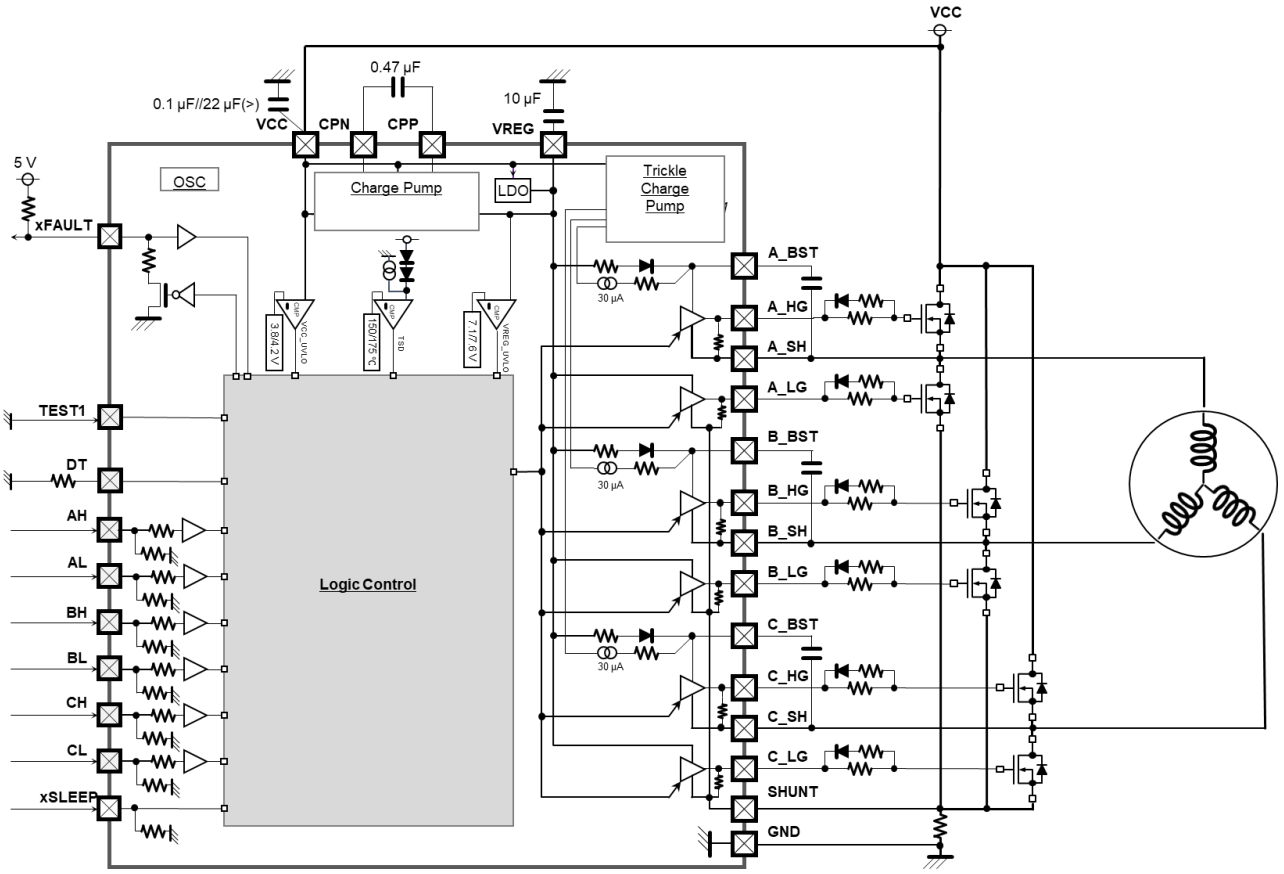


Figure 3. Functional Block Diagram

Absolute Maximum Ratings (respect to GND unless otherwise noted.)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{CC}	-0.3 to +65.0	V
CPP Pin Input Voltage	V_{CPP}	-0.3 to +15.5	V
CPN Pin Input Voltage	V_{CPN}	-0.3 to +15.5	V
VREG Pin Input Voltage	V_{REG}	-0.3 to +15.0	V
*_BST – *_SH (* = A, B, C) *(Note 1)*	V_{BST-SH}	-0.3 to +15.0	V
*_BST – *_HG (* = A, B, C) *(Note 1)*	V_{BST-HG}	-0.3 to +15.0	V
_BST (= A, B, C) *(Note 1)*	V_{BST}	-0.3 to +80.0	V
_HG (= A, B, C) *(Note 1) (Note 2)*	V_{HG}	-8.0 to +80.0	V
_LG (= A, B, C) *(Note 1)*	V_{LG}	-0.3 to +15.0	V
_SH (= A, B, C) *(Note 1) (Note 2)*	V_{SH}	-8.0 to +65.0	V
SHUNT Pin Input Voltage	V_{SHUNT}	-1.0 to +1.0	V
DT Pin Input Voltage	V_{DT}	-0.3 to +2.0	V
xSLEEP Pin Input Voltage	V_{xSLEEP}	-0.3 to +6.5	V
TEST1 Pin Input Voltage	V_{TEST1}	-0.3 to +6.5	V
Logic Input Voltage	V_{IN}	-0.3 to +6.5	V
xFAULT Pullup Voltage	V_O	-0.3 to +6.5	V
xFAULT Sink Performance	I_O	5	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) A,B and C is one of 3outputs name
(Note 2) Acceptable time duration of Negative Voltage depends on external capacitor value placed between *_BST and *_SH. (V*_BST – V*_SH must be ≤15 V). As a reference, it would be covered over 2 µs if the capacitor value is 1 µF

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{CC}	4.5	-	60	V
Input Voltage Ramp Rate at Power Up	$V_{CC\_RAMP\_UP}$	-	-	30.0	V/µs
Input Voltage Ramp Rate during Operation	$V_{CC\_RAMP\_ope}$	-	-	4.0	V/µs
Slew Rate on *_SH Pins	V_{SH_SR}	-	-	4.0	V/ns
DT Pin Input Voltage	V_{DT}	0.0	-	1.0	V
xSLEEP Pin Input Voltage	V_{xSLEEP}	0.0	-	5.5	V
TEST1 Pin Input Voltage	V_{TEST1}	0.0	-	5.5	V
xFAULT Pullup Voltage	V_O	0.0	-	5.5	V
Logic Input Voltage	V_{IN}	0.0	-	5.5	V
Minimum Pulse Input Width of xSLEEP	Tw	20	-	-	µs
Operating Temperature	Topr	-40	-	+125	°C
Operating Junction Temperature	Tj	-40	-	+150	°C

Thermal Resistance *(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 5)*	2s2p*(Note 6)*	
UQFN28AV040A				
Junction to Ambient	θ_{JA}	120.3	47.6	°C/W
Junction to Top Characterization Parameter *(Note 4)*	Ψ_{JT}	19.9	12.3	°C/W

(Note 3) Based on JESD51-2A (Still-Air).
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.
(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 7) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Electrical Characteristics (Unless otherwise specified V_{CC} = 24 V, Topr = 25 °C) *(Note 8)*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power Supply						
Input Supply Voltage	V_{CC}	4.5	-	60	V	
Quiescent Current	I_{VCC}	1.8	2.8	3.5	mA	V_{xSLEEP} ≥ 2.0 V (active mode) (A_SH, B_SH, C_SH) = (H, Z, L) R_{DT} = 100 kΩ
	I_{VCC2}	-	2.8	-	mA	V_{xSLEEP} ≥ 2.0 V (active mode) xH, xL is 20 kHz Switching R_{DT} = 100 kΩ
	I_{VCCQ}	-	-	1	μA	V_{xSLEEP} ≤ 0.6 V (sleep mode)
Control Logic						
Input Logic Low Threshold	V_{IL}	-	-	0.8	V	
Input Logic High Threshold	V_{IH}	2.0	-	-	V	
xSLEEP Input Low Threshold	V_{IL_xSLEEP}	-	-	0.6	V	
xSLEEP Input High Threshold	V_{IH_xSLEEP}	2.0	-	-	V	
Logic Input Current	$I_{IN(H)}$	3	6	10	μA	V_{IN} = 5.0 V
	$I_{IN(L)}$	-10	+1	+10	μA	V_{IN} = 0.8 V
Internal Pull-down Resistance	R_{PD}	640	800	960	kΩ	6 control pins
Fault Outputs (Open-Drain Outputs)						
Output Low Voltage	V_{OL}	-	-	0.5	V	I_O = 5 mA
Output High Leakage Current	I_{OH}	-	-	1	μA	V_O = 3.3 V
Protection Circuit						
V_{CC} Voltage as OK to Active	V_{CC_GOOD}	3.9	4.2	4.5	V	
V_{CC} UVLO Detecting Voltage	V_{CC_NG}	3.6	3.8	4.0	V	
V_{CC} Hysteresis	V_{CC_HYS}	0.2	0.4	0.6	V	
V_{REG} Threshold	V_{REG_GOOD}	7.2	7.6	8.0	V	
V_{REG} UVLO Detecting Voltage	V_{REG_NG}	6.7	7.1	7.5	V	
V_{REG} Hysteresis	V_{REG_HYS}	0.3	0.5	0.7	V	
TSD Detecting Temperature	T_{TSDON}	-	175	-	°C	
TSD Temperature as OK to Active	T_{TSDOFF}	-	150	-	°C	
TSD Hysteresis	T_{TSDHYS}	-	25	-	°C	
V_{REG} Start Up Delay	t_{REG}	-	850	-	μs	
Wake Up Time	t_{WAKEUP}	-	1	-	ms	V_{xSLEEP} ≥ 2.0 V (active mode)
Turn Off Time	t_{SLEEP}	-	4	-	μs	V_{xSLEEP} ≤ 0.6 V (sleep mode)

(Note 8) Voltage is measured from GND unless otherwise noted.

Electrical Characteristics - continued (Unless otherwise specified V_{CC} = 24 V, Topr = 25 °C) *(Note 8)*

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Gate Drive						
Bootstrap Diode Forward Voltage	V_{FBOOT}	-	-	0.9	V	I_F = 5 mA
V_{REG} Output Voltage	V_{REG}	10.0	12.5	13.5	V	V_{CC} = 6.25 V to 60 V
		2 x V_{CC}-1	-	2 x V_{CC}		V_{CC} = 4.5 V to 6.25 V
Gate Driver Strength (source)	I_{SRC}	-	0.5	-	A	Pulse width < 10 µs
Gate Driver Strength (sink)	I_{SNK}	-	1.0	-	A	Pulse width < 10 µs
HS Gate Drive Pull-up Resistance	R_{HS-UP}	2	5	8	Ω	I_D = 100 mA
HS Gate Drive Pull-down Resistance	R_{HS-DN}	1.0	3.0	5.5	Ω	I_D = 100 mA
HS Semiactive Pull-down Resistance	R_{HS-PDN}	-	-	16	kΩ	*_HG to *_SH : V_{GSHG} = 2 V
LS Gate Drive Pull-up Resistance	R_{LS-UP}	2	5	8	Ω	I_D = 100 mA
LS Gate Drive Pull-down Resistance	R_{LS-DN}	1.0	3.0	5.5	Ω	I_D = 100 mA
LS Passive Pull-down Resistance	R_{LS-PDN}	-	590	-	kΩ	
LS Automatic Turn-on Time	t_{LS}	-	0.5	-	µs	After $V_{REG} \geq V_{REG\_GOOD}$
Charge Pump Frequency	f_{CP}	-	110	-	kHz	
Turn On/Off Delay from 6inputs to 6outputs	t_{RISE}	-	25	60	ns	Rise Delay
	t_{FALL}	-	25	60	ns	Fall Delay
Matching Propagation Delay per Phase	t_{PD_MATCH}	-	+/-4	-	ns	
Matching Propagation Delay per Phase to Phase	$t_{PD\_MATCH\_PP}$	-	+/-4	-	ns	
Maximum Frequency of 6inputs	f_{MAX_6IN}	-	-	1000	kHz	R_{DT} = 0 Ω
Minimum Pulse Width	t_{MIN_6IN}	45	-	-	ns	V_{CC} = 4.5 V
Dead Time	t_{DEAD}	-	10	-	ns	R_{DT} = 0 Ω = Tied to GND
		-	110	-	ns	R_{DT} = 3.3 kΩ
		-	1800	-	ns	R_{DT} = 100 kΩ

(Note 8) Voltage is measured from GND unless otherwise noted.

Operation and Functionality

The BD67870MWV-Z (gate driver device) is three-phase Brushless DC Motor gate driver that is capable of driving external N-channel MOSFET in half-bridge configuration with 0.5 A sourcing and 1 A sinking capability.
The gate driver operates over a wide input voltage range of 4.5 V to 60 V while also supporting up to 100 % duty cycle output gate drive with trickle charge pump. A nominal gate drive voltage of 12.5 V allows operation of external N-channel MOSET for lower RDSON and lowering power losses. The gate drive features protection features such as input voltage under voltage lockout, gate driver power supply voltage under voltage lockout and internal thermal shutdown. Additionally, an adjustable dead time control circuit allows robust system operation.

Timing Chart

The timing chart of power up is shown in Figure 4, while power down is shown in Figure 5.
Power-up sequence starts after the voltage on V_{CC} is V_{CC} UVLO threshold (V_{CC_GOOD}) or above. After this the gate driver power supply V_{REG} starts to power-on. V_{REG} voltage must be V_{REG} UVLO (V_{REG_GOOD}) or above before the gate driver output is active and follow the input logic.
When xSLEEP pin is pulled below the input logic low level, the chip will enter sleep mode. After this point the gate driver will stop to follow the input logic signal.

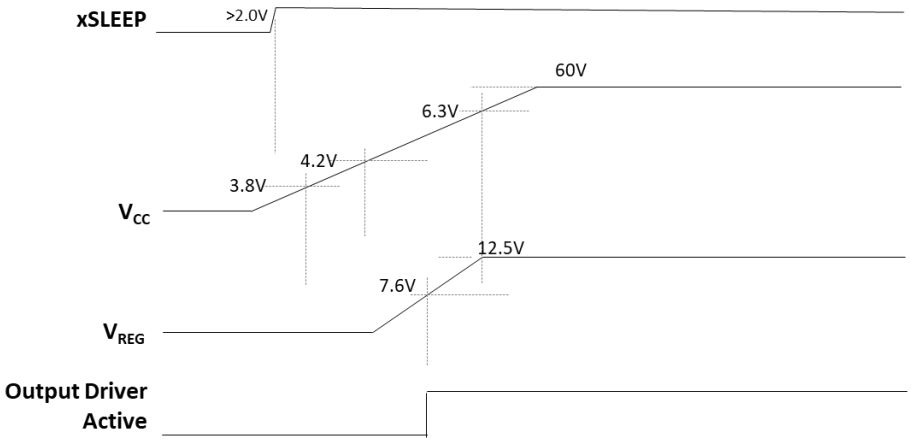


Figure 4. Timing Chart (power supply turn-on)

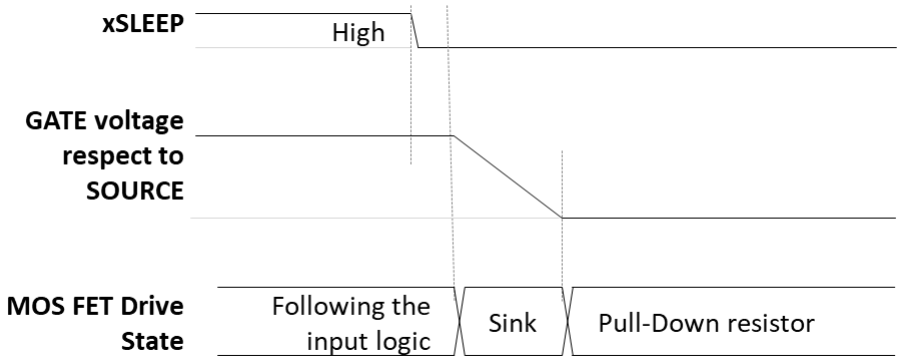


Figure 5. Timing Chart (xSLEEP pulled low)

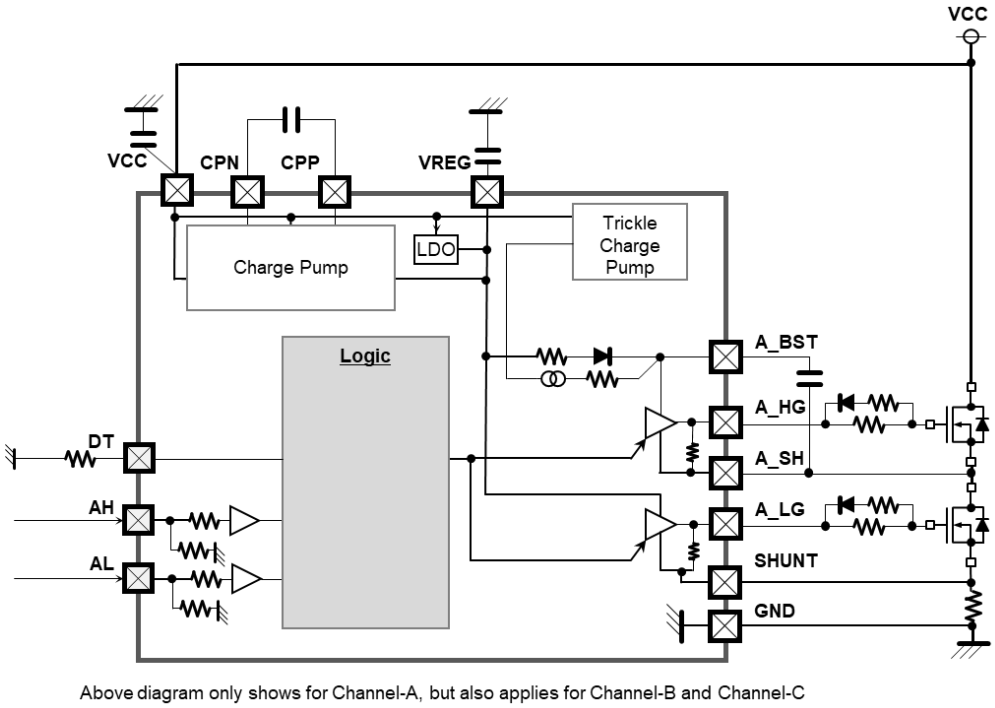
Operation and Functionality - continued

Gate Drive Architecture

The gate driver chip has both an internal high-side push-pull and an internal low-side push-pull driver to drive external N-channel MOSFETs. Input pin AH, BH, CH directly provide logic input signal for the high-side driver, while the AL, BL, CL pin provide logic input signal for the low-side driver.

The low-side driver is powered directly from the VREG pin and referenced to the SHUNT pin. The high-side driver on the other hand is powered by a bootstrap circuitry that includes an internal bootstrap diode and an external bootstrap capacitor. The bootstrap circuitry operates by taking power from VREG pin and, relying on the switching operation of the switching node, will create a floating supply between A_BST, B_BST, C_BST and A_SH, B_SH, C_SH pins. However, at very high output duty cycle operation there will not be enough off-time on the switching node to allow the bootstrap diode to recharge the external bootstrap capacitor thus causing the bootstrap capacitor to eventually lose charge. To circumvent this, an internal Current Source circuit is dedicated to always provide a small amount of charging current to the A_BST, B_BST, C_BST pin directly from the VCC pin thus allowing external bootstrap capacitor to not discharge and allowing 100 % output duty cycle operation with trickle charge pump.

Additionally, both the high-side driver and the low-side driver includes an internal pulldown resistor between the gate pin and the return pin to ensure the external MOSFET is not accidentally turned on when the respective gate driver does not have sufficient power.



Above diagram only shows for Channel-A, but also applies for Channel-B and Channel-C

Figure 6. Gate Driver Architecture

Operation and Functionality - continued

Gate Drive Power Supply (V_{REG})

The gate driver block is powered from the VREG pin. The VREG pin is powered from a combination of internal voltage converters (Table 1). Figure 14 shows V_{REG} Voltage vs Input Voltage at Different Load Currents. This measurement circuit is designed to evaluate the source capability of the V_{REG}. Placing a sink current at the load to check if the V_{REG} voltage can be maintained. The load for the V_{REG} are the low-side output and the charging path of the bootstrap capacitor.

Table 1. V_{REG} Operation (No Load)

V_{CC} Voltage [V]	Typical V_{REG} Output Voltage [V]	V_{REG} Operation Mode
$14.5 < V_{CC}$	12.5	LDO
$6.25 < V_{CC} \leq 14.5$	11.3 to 12.5	Charge Pump and LDO
$4.5 \leq V_{CC} \leq 6.25$	(2 x V_{CC}-1) to (2 x V_{CC})	Charge Pump

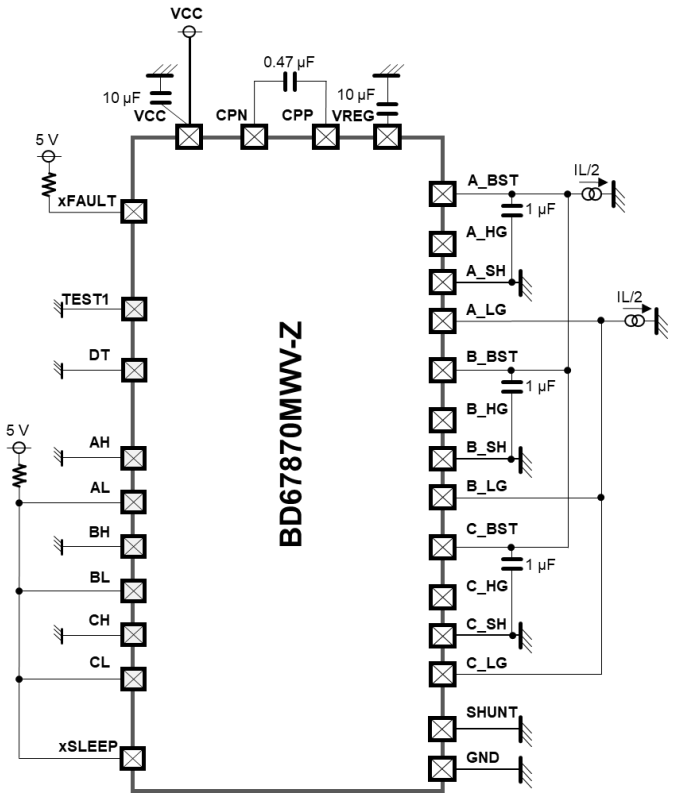


Figure 7. Measurement Circuit

Operation and Functionality - continued

Input Logic

Table 2 shows the input logic truth table for BD67870MWV-Z. In this version, the AH, BH, CH and AL, BL, CL input signals directly control the state of the A_HG, B_HG, C_HG and A_LG, B_LG, C_LG output drive signal as long as xSLEEP is high level. When AH, BH, CH and AL, BL, CL input signals are high level at the same time, the A_HG, B_HG, C_HG and A_LG, B_LG, C_LG output drive signals are forced low to prevent cross conduction of external N-channel MOSFET.

Table 2. BD67870MWV-Z Input Logic Truth Table (6x PWM Mode)

xSLEEP	AH (BH / CH)	AL (BL / CL)	A_HG (B_HG / C_HG)	A_LG (B_LG / C_LG)	A_SH (B_SH / C_SH)
0	X	X	L	L	Hi-Z
1	0	0	L	L	Hi-Z
1	0	1	L	H	GND
1	1	0	H	L	V_{CC}
1	1	1	L	L	Hi-Z

Cross Conduction Prevention

Input logic pins AH, BH, CH and AL, BL, CL is provided externally and controls the gate signal directly, there is a cross conduction prevention function that prevents both external N-channel MOSFET from turning on when both AH, BH, CH and AL, BL, CL input signals are a Table 2. BD67870MWV-Z will output both high-side drive signal A_HG, B_HG, C_HG and low-side drive signal A_LG, B_LG, C_LG to be low thus turning off .

Dead Time Adjustment

BD67870MWV-Z have dead time adjustment control function to prevent both external N-channel MOSFET from accidentally turning on at the same time during switchover when turning on/off of the respective external N-cannel MOSFET. The duration of the dead time can be adjusted by an external resistor connected to the DT pin and ground. The duration can be adjusted between 110 ns to 1800 ns by choosing a resistor between 3.3 kΩ to 100 kΩ (higher values should be avoided). The equation below shows the relationship between external resistor and the dead time duration. However, if an external resistor of 840 Ω or less is used, the dead time is 10 ns.(Figure 16) Please note that there are variations in ICs, so be careful when using resistors of 1 kΩ or less.

$$t_{DEAD} = 17.5 \times R_{DT} + 52 \quad (R_{DT} \geq 1\ k\Omega) \qquad [\text{ns}]$$

Where:

t_{DEAD}	[ns]	is the Dead time.
R_{DT}	[kΩ]	is the Dead time adjustment resistor that connected to the DT pin and ground.

For example, to set a 1 μs dead time, a 54.2 kΩ resistor should be used.
To disable dead time (in the case that micro-controller can provide dead time itself), tie the DT pin to ground.

Sleep Mode (xSLEEP input pin)

When the xSLEEP pin is driven to ground, the gate driver device is put into sleep mode and consumes little quiescent current in order to reduce power consumption from the input VCC pin. At this state, all the internal circuitry is disabled, and all the input logic pins are ignored. The gate driver output is put into high-impedance mode. When xSLEEP pin is driven high, the gate driver will start the power up sequence.

Operation and Functionality - continued

Protection

The BD67870MWV-Z has features to protect against input voltage V_{CC} under voltage lockout (V_{CC} UVLO), regulated driver voltage supply V_{REG} under voltage lockout (V_{REG} UVLO), and internal Thermal Shutdown (TSD).
For V_{CC} UVLO, the gate driver chip will turn off and all output drive voltages whenever the input voltage V_{CC} drops below V_{CC_NG} threshold. The gate driver will recover and turn back on when input voltage V_{CC} rises above V_{CC_GOOD}.
For both V_{REG} UVLO and TSD, the behavior of the output drive voltage, the xFAULT pin condition as well as the recovery method is shown in the table below.

Table 3. Behavior of V_{REG} UVLO and Internal Thermal Shutdown Protection Features

Fault	Condition	xFAULT	OUTPUT	Recovery
V_{REG} UVLO	$V_{REG} \leq V_{REG\_NG}$	Pulled Low	Hi-Z	Auto / xSLEEP = L
	$V_{REG} \geq V_{REG\_GOOD}$	Hi-Z	Active	
Thermal Shutdown	Internal die temperature $\geq T_{TSDON}$	Pulled Low	Hi-Z	Auto / xSLEEP = L
	Internal die temperature $\leq T_{TSDOFF}$	Hi-Z	Active	

xFAULT Pin

xFAULT indicates that a fault condition occurred in the gate driver chip. A pullup resistor to an externally supplied e.g. 5 V (depends on the Controller side input range) voltage is required to be connected to the xFAULT pin.
Normally xFAULT pin is in Hi-Z condition. If either an Under Voltage Lockout on V_{REG} voltage occurs, or a Thermal Shutdown (TSD) event occurs, the xFAULT pin on the device will be pulled low by an internal pulldown device. The xFAULT pin will only be pulled low during the duration of the fault condition.

De-glitcher for FAULT Condition

A 3 µs (Typ) de-glitching filter is employed to avoid any false detection of fault conditions that may be caused by noise conditions.

Application and Implementation Guide

Recommended External Components for Typical Application

Table 4. Recommended External Components
(*) denotes “A/B/C”

Components	PIN 1	PIN 2	Recommended
VCC Bypass Bulk Capacitor	VCC	GND	≥ 22 µF, > 2 x V_{CC} rated Bulk Capacitor
VCC Bypass Ceramic Capacitor	VCC	GND	≥ 0.1 µF, > 2 x V_{CC} rated X5R or X7R Ceramic Capacitor
Charge Pump Capacitor	CPP	CPN	470 nF, V_{CC} rated X5R or X7R Ceramic Capacitor
Regulator Bypass Capacitor	VREG	GND	≥ 10 µF, > 25 V rated X5R or X7R Ceramic Capacitor
Pull up of xFAULT	xFAULT	≤ 5.5 V	Pullup resistor for suitable voltage for the controller
Dead Time Adjust Resistor	DT	GND	Pulldown resistor
Gate Resistor	*_HG/ *_LG	Gate of MOS	Gate control resistor (≤ 10 Ω)
Bootstrap Capacitor	*_BST	*_SH	Bootstrap capacitor

Application Example

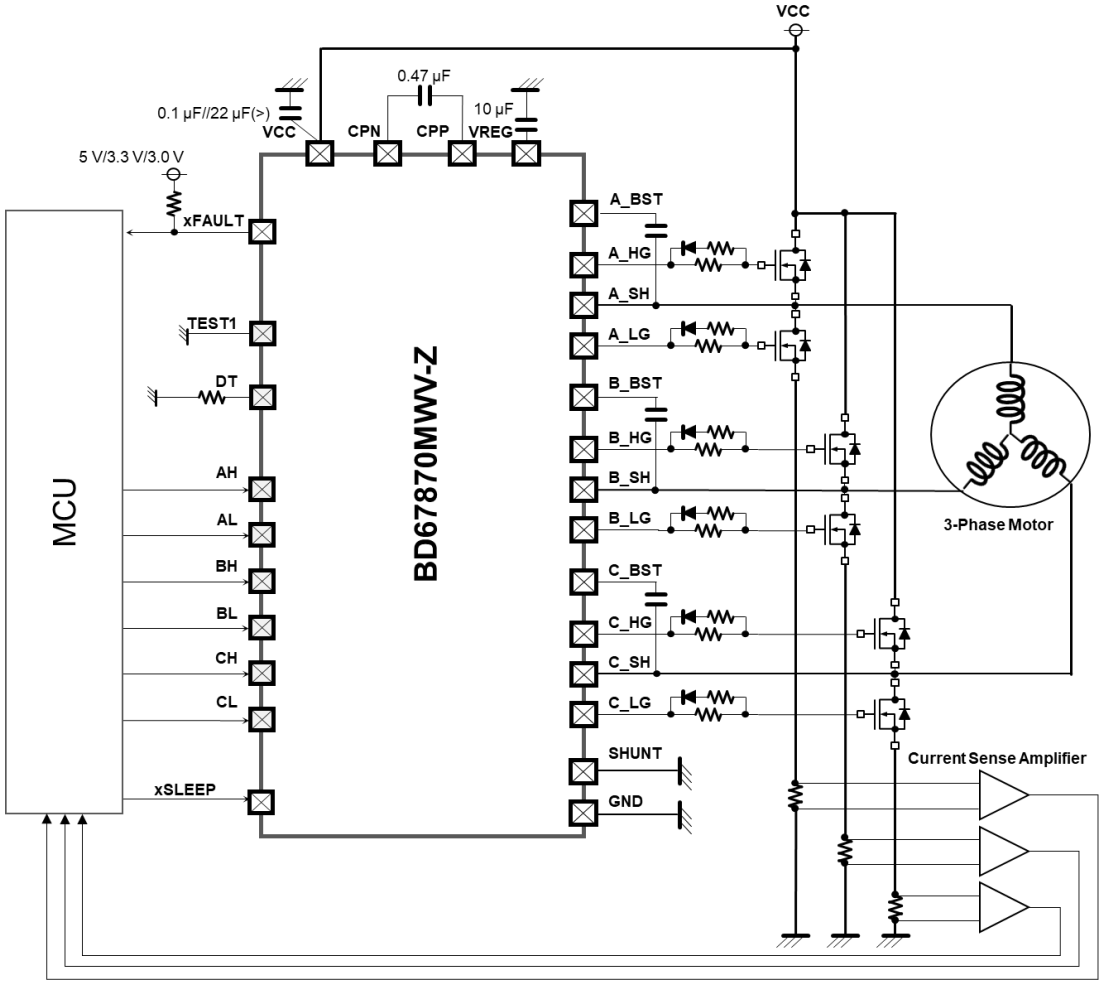


Figure 8. Application Example (Three Shunt)

Application and Implementation Guide - continued

Input Power Supply Capacitor Recommendation

Two types of capacitors are recommended to be used on input power supply line VCC. A electrolytic bulk capacitor 22 µF or above that has voltage rating is 2 x V_{CC} or above voltage should be placed near the main connection point of the power supply. A ceramic capacitor (X5R or X7R) 0.1 µF or above with voltage rating 2 x V_{CC} or above voltage should be placed in parallel to supply high frequency components. In addition, it is recommended to place similar ceramic capacitors in between the drain of each high-side MOSFET to the source of the low-side MOSFET for each leg of the 3 phase half-bridges.

Bootstrap Capacitor and VREG Capacitor Calculation

Bootstrap Capacitor hold the electrical charge to drive the high-side MOSFET while it is turning on. The charge of the bootstrap capacitor will be used towards charging to high-side MOSFET gate capacitor. It is recommended to follow the below equation:

$$C_{BOOST} \geq 10 \times Qg \quad [\text{nF}]$$

Where:

C_{BOOST}	[nF]	is the capacitance of the bootstrap capacitor.
Qg	[nC]	is the total MOSFET gate charge.

For example, when the high-side MOSFET Qg= 100 nC, select a bootstrap capacitor of value ≥ 1 µF with a voltage rating ≥ 2x V_{REG} (ie. 25 V). This Bootstrap capacitor is driven by current limiting driver, and it has an ability of Min 30 mA. It has to be considered about Bootstrap sequence time duration for enough charging up time.
VREG capacitor holds the charge to supply all of the high-side drivers and low-side drivers. The value should be larger than 6 times or above of the bootstrap capacitor. It is recommended to follow the below equation:

$$C_{VREG} \geq 6 \times C_{BOOST} \quad [\text{nF}]$$

Where:

C_{VREG}	[nF]	is the capacitance of the VREG capacitor.

For example, when C_{BOOST} = 1 µF, then select the capacitor on V_{REG} is 6 µF or above. However, we recommend 10 µF for this because the actual capacitance value will be affected by DC biasing. Also select the VREG capacitor voltage rating to be 25 V or above. This VREG capacitor is driven by current limiting driver, depends on V_{CC} range (Please refer to Table 1)

Application and Implementation Guide - continued

Gate Resistor Guide for Suitable Gate Current Control

The BD67870MWV-Z is voltage mode gate drivers and includes a strong internal source and sink MOSFET which has low resistance. To limit the slew rate of the gate voltage, it is necessary to include a network of series gate resistor.
The calculation of the series gate resistor depends on the total gate charge of the MOSFET being driver, the voltage of the gate driver power supply, the miller plateau voltage of the MOSFET as well as the desired slew rate of the gate voltage.
The figure below shows a configuration where the turn-on is limited by series gate resistor R1, while the turn-off is a parallel combination of R1 and R2. This will create different turn-on and turn-off time.

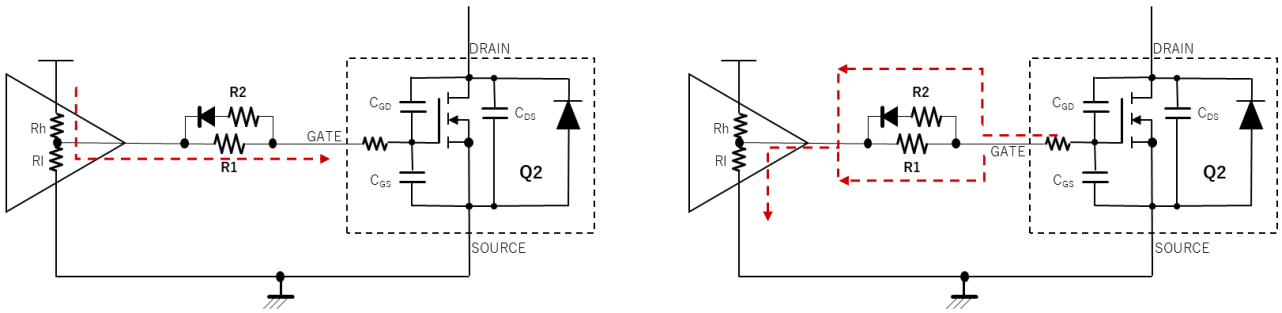


Figure 9. Gate Resistor Configuration for Asymmetrical Turn-on and Turn-off

Parallel MOSFET Configuration

For higher current applications, it may be necessary to connect MOSFET in parallel. For such designs, it is important to pay attention to certain aspect of circuit and PCB design. In particular, issues such as current crowding causing to one path heating up more than the other, and self-excited oscillations may occur.
The Figure 10 below shows parasitic components such as drain inductance, source inductance, and gate inductance that if not paid attention to may lead to self-excited oscillations. In general rule, all these inductances should be minimized by using thicker and shorter PCB paths. In addition, individual gate resistors should be used for each parallel MOSFET to ensure more symmetrical current flow.
Additionally, the value of bootstrap capacitor and VREG pin capacitor should be scaled up appropriately to take into account a larger total gate charge that the chip needs to drive.

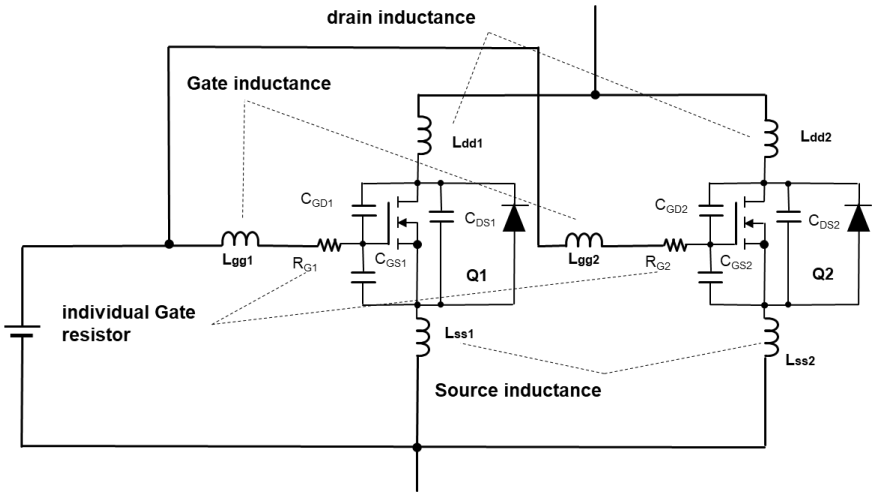


Figure 10. Parasitic Components when Designing for Parallel MOSFET Configuration

PCB Layout Guidelines

High current switching gate driver application require that PCB layout guidelines be followed to ensure optimal performance. In general, below are some important points to consider:

Parasitic inductances should be minimized as they will cause unwanted voltage spikes due to high di/dt current slew rates. This is particularly important on the traces where switching currents operate: drain of power MOSFET, source of power MOSFET, and gate driver output connection to the MOSFET gate. To reduce parasitic PCB trace inductance, use wide copper traces for all the high switching current paths.

1. Place all power supply capacitors (charge pump capacitors, input filter capacitor for VCC pin, capacitor on VREG pin) as close as possible to their respective pins. Route the ground side of the VCC and VREG capacitors to the GND pin of the gate driver device.

2. Separate the path for the input V_{CC} voltage into the gate driver chip from the V_{CC} voltage going to the 3 half-bridges. The path going to the half-bridges is a high current path and as such PCB trace should be wide and if possible connected on multiple layers. Place a bulk electrolytic capacitor near the VCC pin and also a local ceramic capacitors near to the high-side MOSFET drains.

3. Place the bootstrap capacitors for the high-side gate drivers as close as possible to the gate driver chip and when possible on the same layer as the gate driver chip to avoid any vias that introduce parasitic inductance.

4. Layout the high current paths from the VCC pin towards the 3 phases of the half-bridges and towards the return GND path symmetrically to avoid any current crowding and to allow each leg to flow current in a balanced manner.

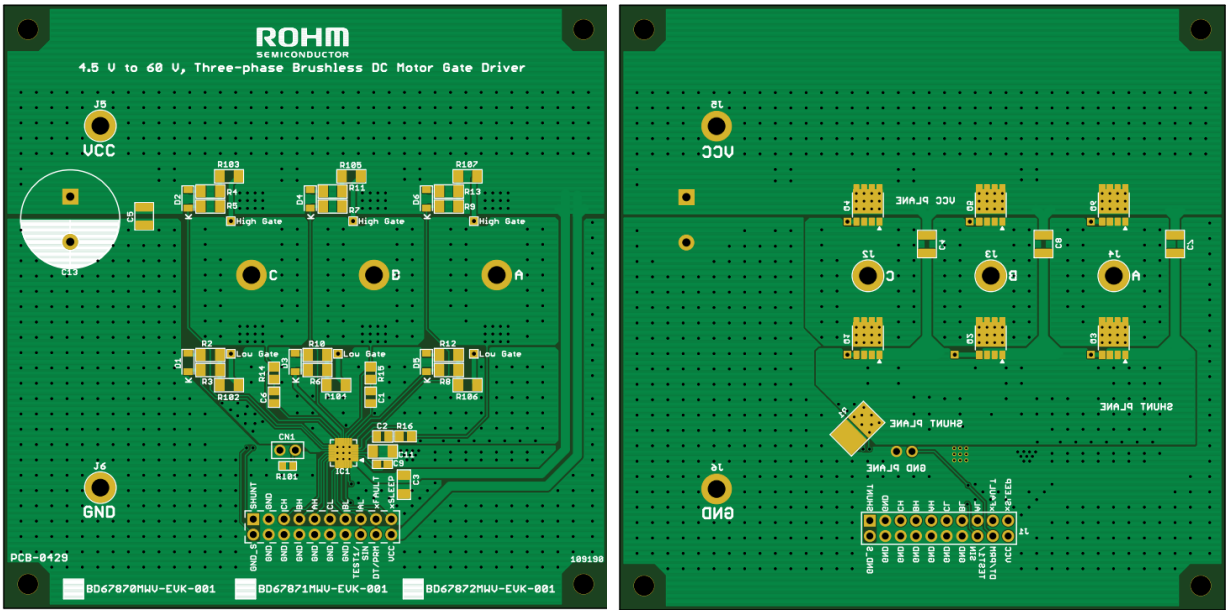


Figure 11. Top View of Recommended PCB Layout (100 mm x 100 mm)

Typical Performance Curves (Reference Data)

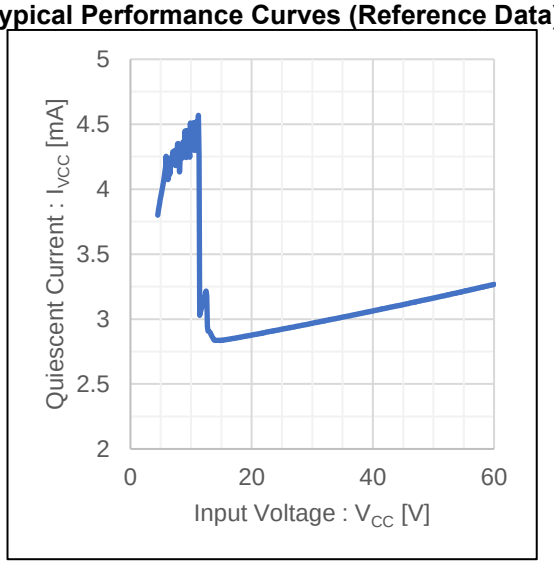


Figure 12. Quiescent Current vs Input Voltage

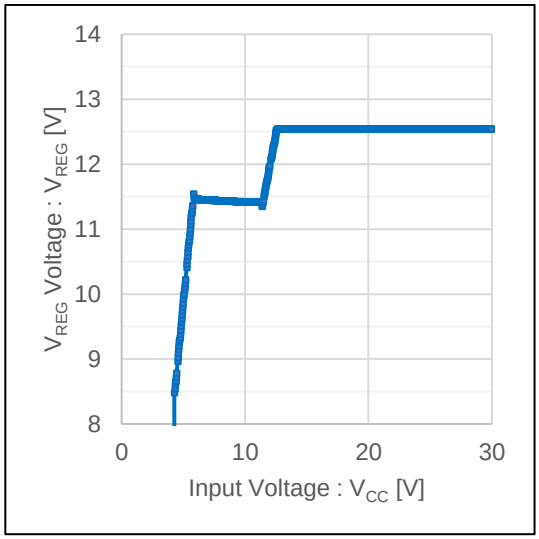


Figure 13. V_{REG} Voltage vs Input Voltage (No Load)

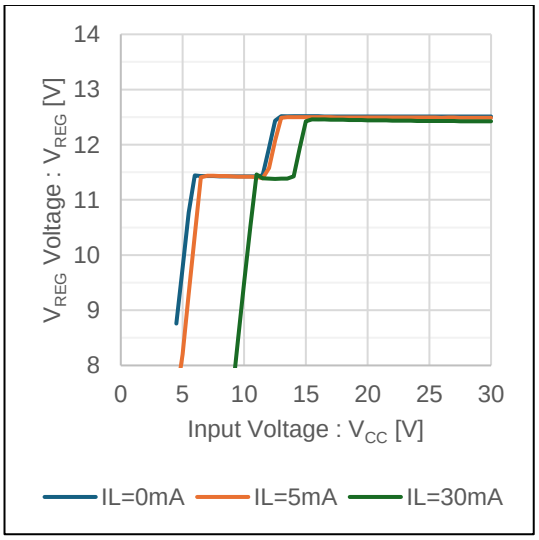


Figure 14. V_{REG} Voltage vs Input Voltage at Different Load Currents

Typical Performance Curves (Reference Data) - continued

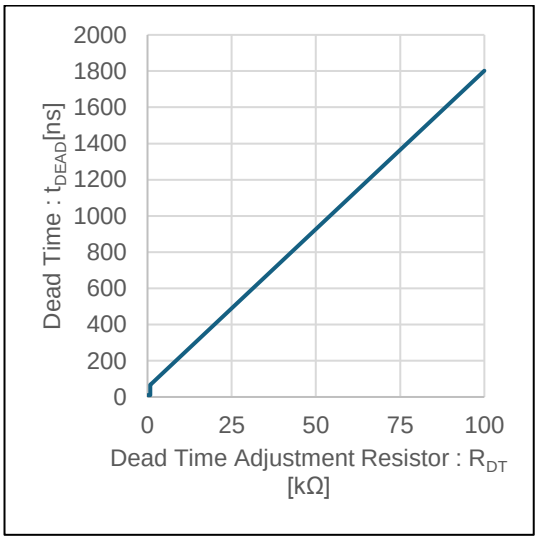


Figure 15. Dead Time vs Dead Time Adjustment Resistor

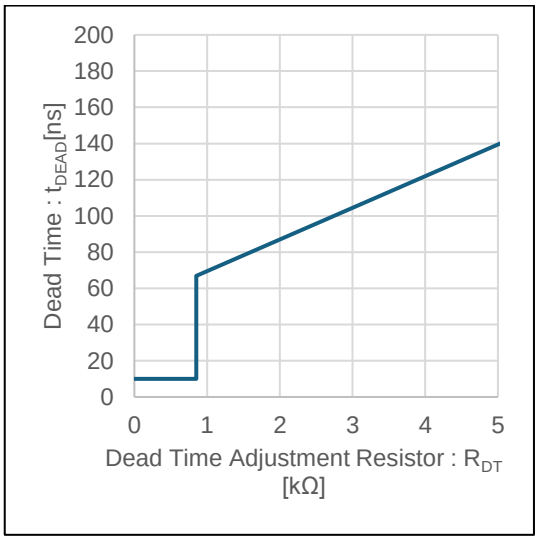


Figure 16. Dead Time vs Dead Time Adjustment Resistor (Zoom)

Characteristic Data (Reference Data)

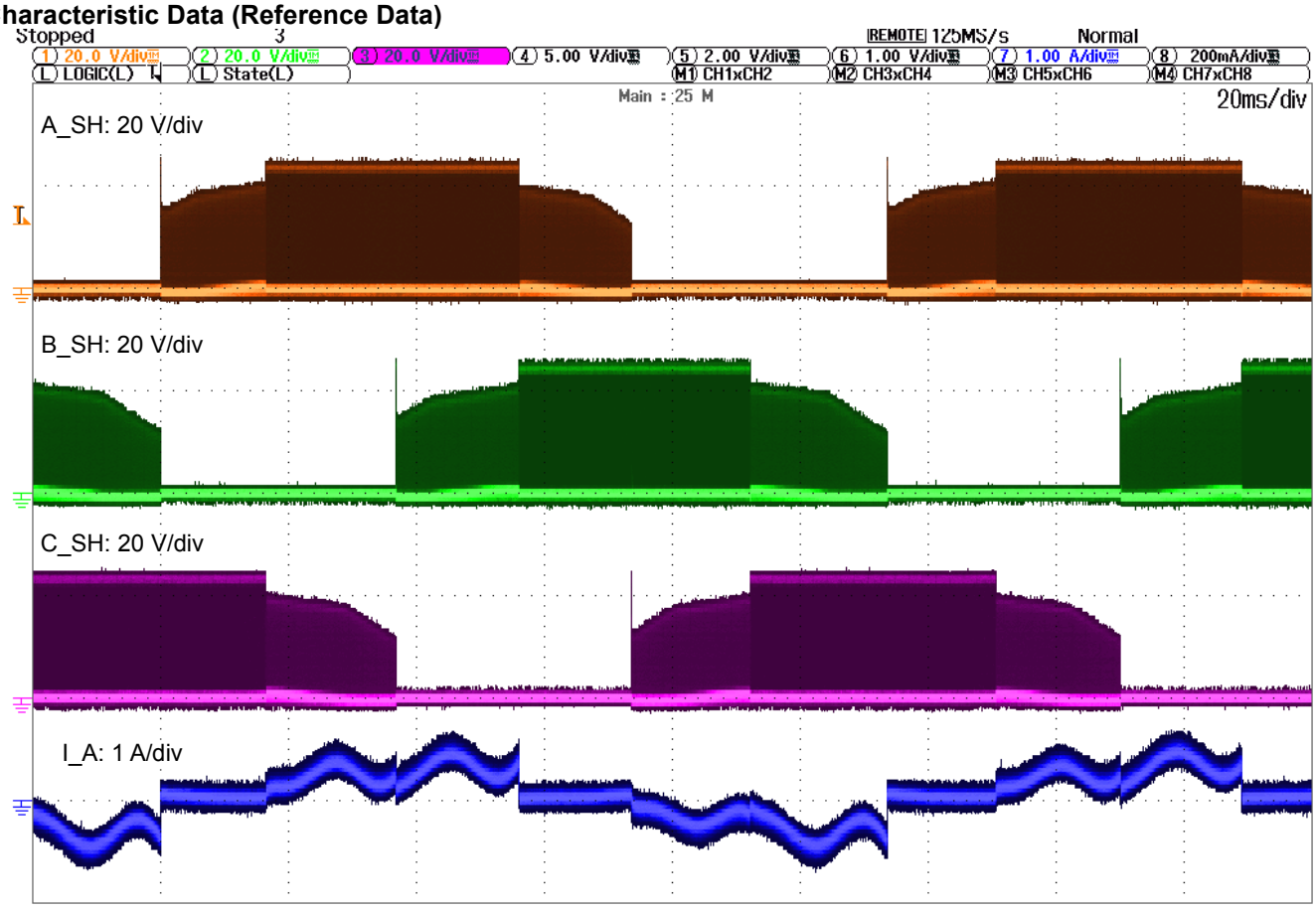


Figure 17. *_SH Waveform of Trapezoidal Motor Control
(PWM frequency = 20 kHz, Dead Time = 3 µs, V_{CC} = 24 V, Duty = 12.5 %)

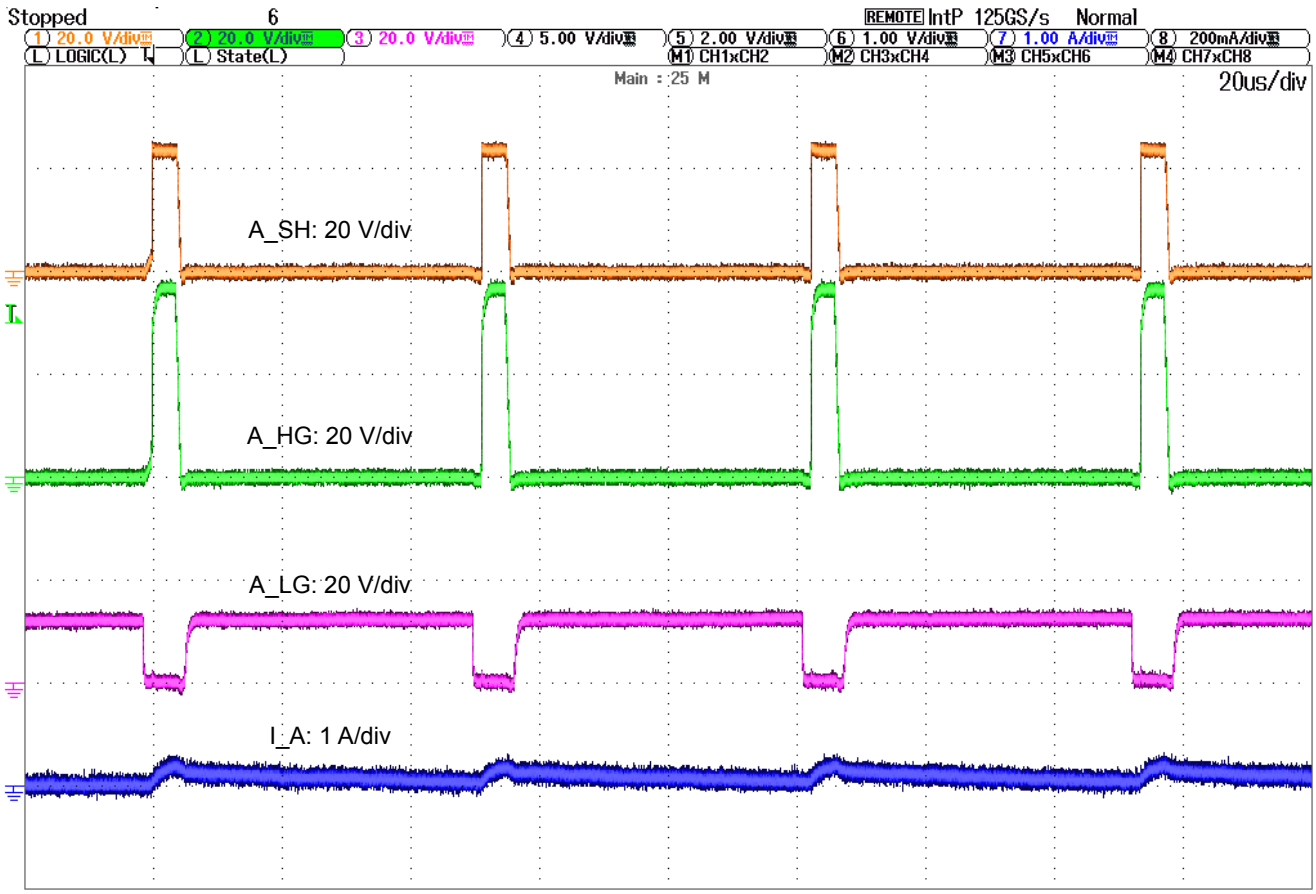


Figure 18. Gate Waveform of Trapezoidal Motor Control
(PWM frequency = 20 kHz, Dead Time = 3 µs, V_{CC} = 24 V, Duty = 12.5 %)

Characteristic Data (Reference Data) - continued

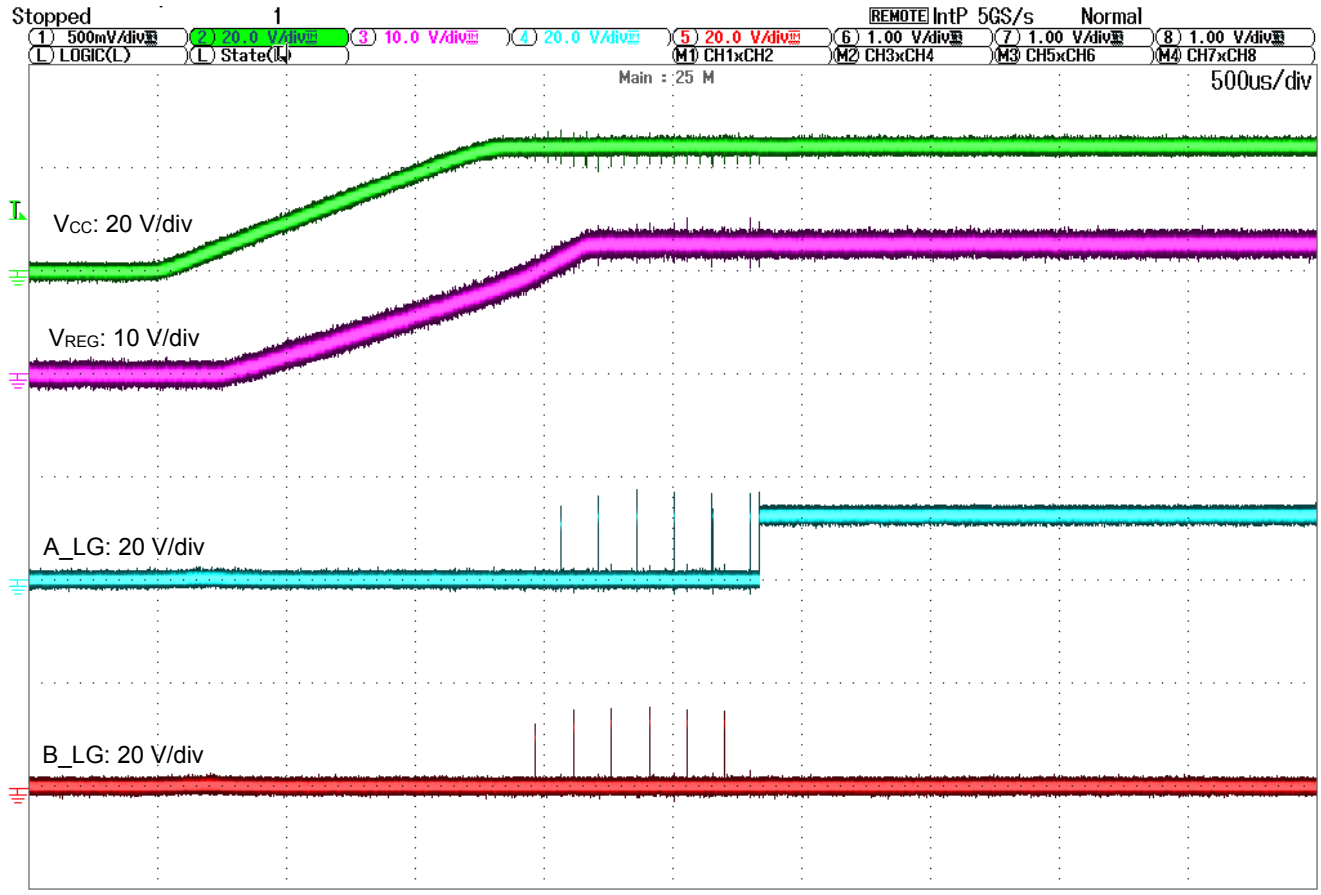


Figure 19. Start-up Sequence on Slow V_{CC} Start up

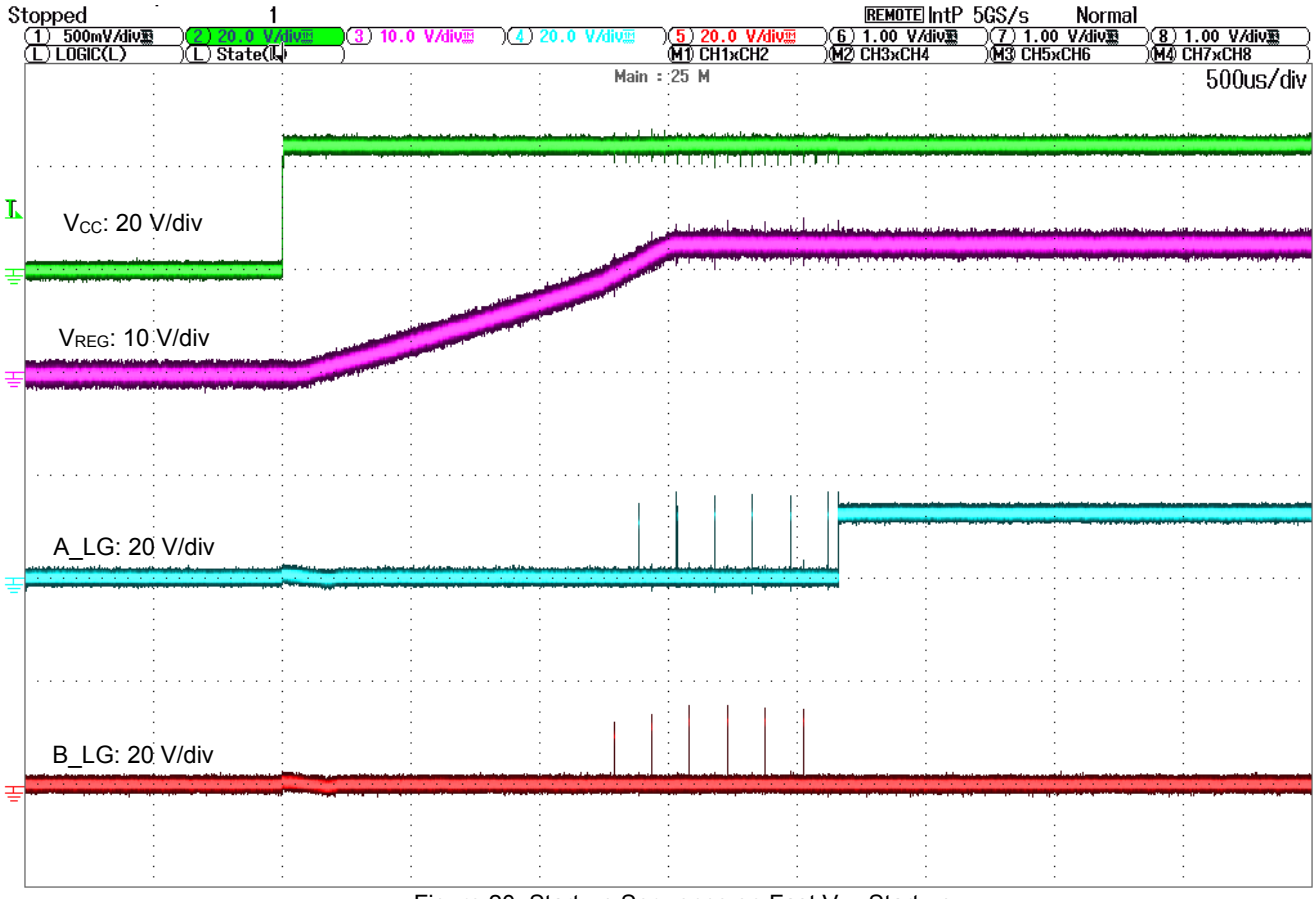


Figure 20. Start-up Sequence on Fast V_{CC} Start up

Characteristic Data (Reference Data) - continued

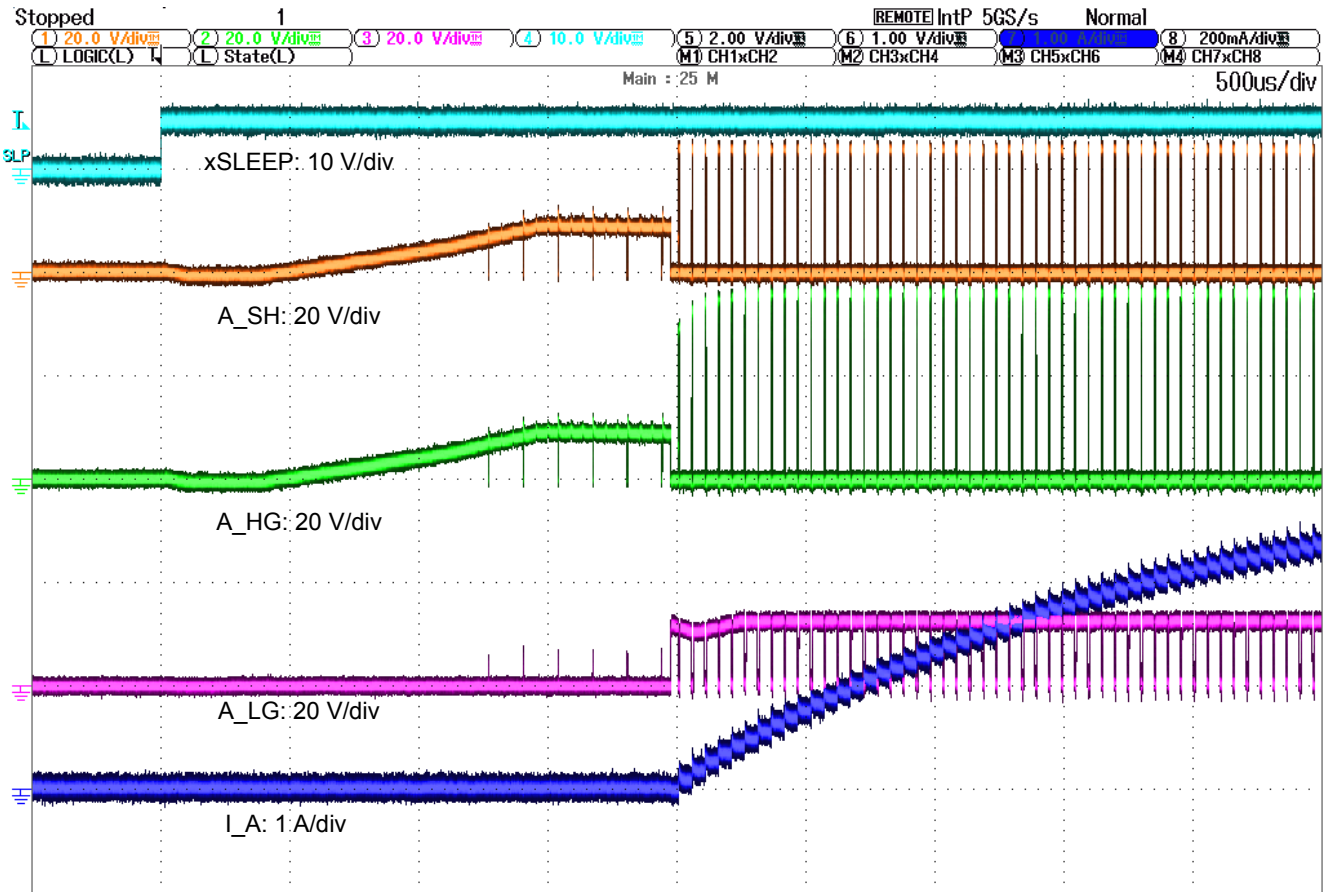


Figure 21. Sleep Recovery

ESD Ratings

Item	Value	Unit
Human Body Model (HBM)	+/-2000	V
Charged Device Model (CDM)	+/-750	V

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

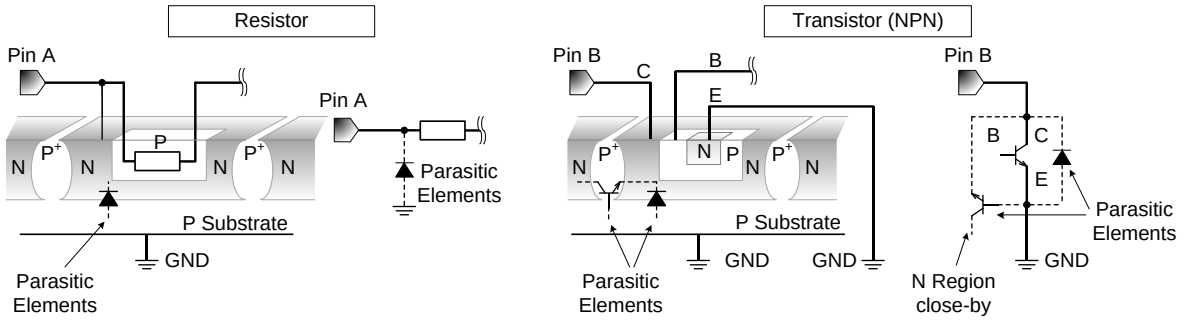


Figure 22. Example of Monolithic IC Structure

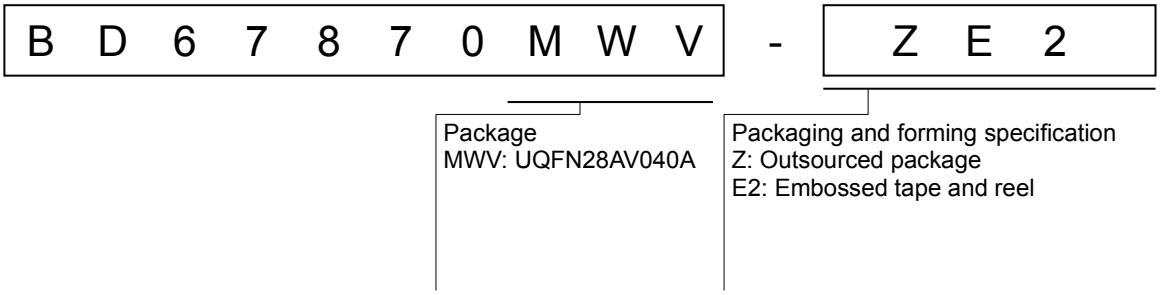
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

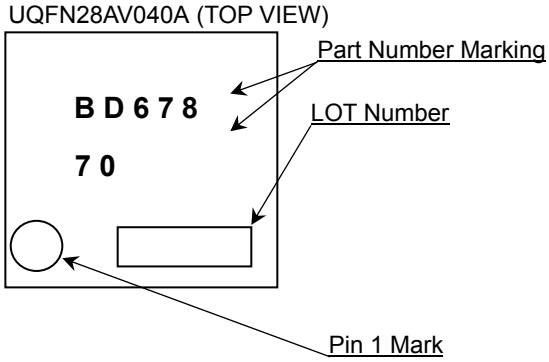
12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

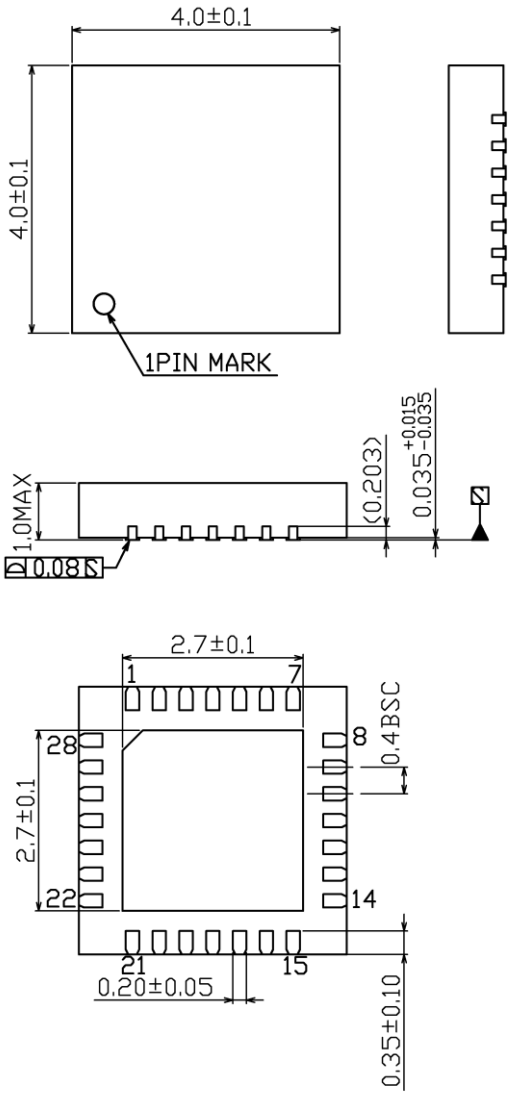


Marking Diagram



Physical Dimension and Packing Information

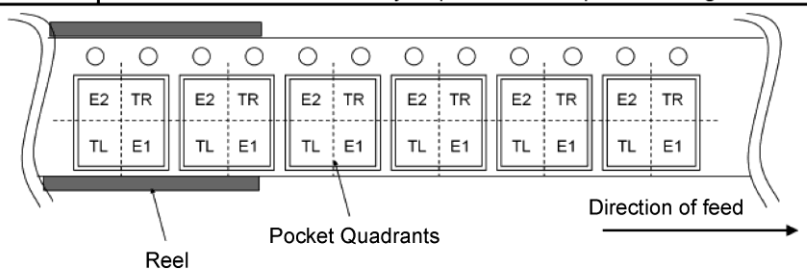
Package Name	UQFN28AV040A



(UNIT:mm)
PKG:UQFN28AV040A
Drawing No.EX001-0129

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
29.Jan.2025	001	New Release

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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