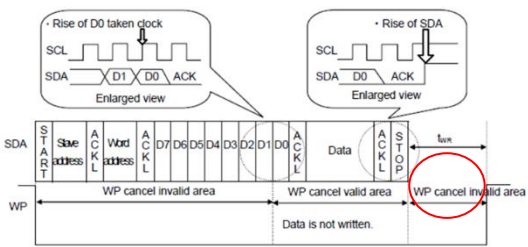
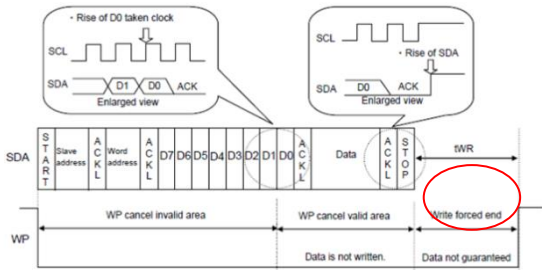


EEPROM Series

Difference between BR24G-3 and BR24L-W

WP Function

Comparison of WP valid timing

BR24G-3	BR24L-W
<p>Write cancel is invalid during write cycle (tWR).</p> <p>From BR24G08-3 Datasheet</p> <p>WP pin is usually fixed to 'H' or 'L', but when WP is used to cancel a write cycle, consider the following WP valid timing diagram. During write cycle execution, setting WP='H' inside the cancel valid area will successfully cancel the write cycle operation. In both Byte Write cycle and Page Write cycle, the area from the first start condition of command to the rise of clock at D0 (the first byte data in a Page Write cycle) is the cancel invalid area. WP input in this area becomes "Don't care". The area from the rise of SCL at D0 to the stop condition input is the cancel valid area. Furthermore, after the execution of forced end by WP, the IC enters standby status.</p>  <p>Figure 42. WP Valid Timing</p>	<p>Write cancel is valid during write cycle (tWR).</p> <p>From BR24L***-W Datasheet</p> <p>WP pin is usually fixed to 'H' or 'L', but when WP is used to cancel a write cycle, consider the following WP valid timing diagram. During write cycle execution, setting WP='H' inside the cancel valid area will successfully cancel the write cycle operation. In both Byte Write cycle and Page Write cycle, the area from the first start condition of command to the rise of clock at D0 (the first byte data in a Page Write cycle) is the cancel invalid area. WP input in this area becomes "Don't care". Set the setup time from the rise of SCL at D0 to 100ns or more. The area from the rise of SCL at D0 to the end of internal automatic write (tWR) is the cancel valid area. Setting WP='H' during tWR, write is ended forcibly and the data of the current address is not guaranteed, therefore, write it once again. (Refer to Fig.50.) After the execution of forced end by WP, the IC enters standby status, so there is no need to wait for tWR (5ms at maximum).</p>  <p>Fig.50 WP valid timing</p>

Comparison of main electrical characteristics

BR24G-3 is characteristically upward compatible with BR24L-W.

Parameter		Symbol	BR24G-3		BR24L-W	
			Limits	Condition	Limits	Condition
Memory Cell Characteristics	Write Cycles		1,000,000 times (min)	Ta=25°C	1,000,000 times (min)	Ta=25°C
	Data Retention		40years (min)	Ta=25°C	40years (min)	Ta=25°C
Recommended Operating Ratings	Power Source Voltage	VCC	1.6V to 5.5V	-	1.8V to 5.5V	-
DC Characteristics	Input Low Voltage	VIL	-0.3V to 0.3VCC	1.7V ≤ VCC ≤ 5.5V	-0.3V to 0.2VCC	1.8V ≤ VCC < 2.5V
					-0.3V to 0.3VCC	2.5V ≤ VCC ≤ 5.5V
	Input High Voltage	VIH	0.7VCC to VCC+1.0 V	1.7 ≤ VCC ≤ 5.5V	0.8VCC to VCC+1.0V	1.8V ≤ VCC < 2.5V
0.7VCC to VCC+1.0 V					2.5V ≤ VCC ≤ 5.5V	
AC Characteristics (Comparison in Fast-mode)	Clock Frequency	fSCL	400kHz (max)	VCC=1.6 to 5.5V	400kHz (max)	VCC=2.5 to 5.5V
	Data Clock High Period	tHIGH	0.6us (min)		0.6us (min)	
	Data Clock Low Period	tLOW	1.2us (min)		1.2us (min)	
	SDA, SCL (INPUT) Rise Time	tR	1.0us (max)		0.3us (max)	
	SDA, SCL (INPUT) Fall Time	tF	1.0us (max)		0.3us (max)	
	Start Condition Hold Time	tHD:STA	0.6us (min)		0.6us (min)	
	Start Condition Setup Time	tCSH	0.6us (min)		0.6us (min)	
	Input Data Hold Time	tDIH	0ns (min)		0ns (min)	
	Input Data Setup Time	tPD1	100ns (min)		100ns (min)	
	Output Data Delay Time	tPD0	0.1us to 0.9us		0.1us to 0.9us	
	Output Data Hold Time	tSV	0.1us (min)		0.1us (min)	
	Stop Condition Setup Time	tDF	0.6us (min)		0.6us (min)	
	Bus Free Time	fSK	1.2us (min)		1.2us (min)	
	Write Cycle Time	tKH	5ms (max)		5ms (max)	
	Noise Spike Width (SDA and SCL)	tSKL	0.1us (max)		0.1us (max)	
	WP Hold Time	tCS	1us (min)		0ns (min)	
	WP Setup Time	tCSS	0.1us (min)		0.1us (min)	
WP High Period	tDIS	1.0us (min)	1.0us (min)			

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