

# Serial EEPROM Series Standard EEPROM

## SPI BUS EEPROM

### BR25G2MFJ-5A

#### General Description

BR25G2MFJ-5A is a 2Mbit serial EEPROM of SPI BUS Interface.

#### Features

- SPI BUS Mode (CPOL, CPHA) = (0, 0), (1, 1)
- Page Size: 256 Byte
- Bit Format: 262144 x 8 bit
- 256 Byte Write Lockable Identification Page (ID Page)
- Address Auto Increment Function at Read Operation
- Auto Erase and Auto End Function at Data Rewrite
- Write Protect Block Setting by Software  
Memory Array 1/4, 1/2, Whole
- HOLD Function by the HOLDB Pin
- Prevention of Write Mistake  
Write Prohibition at Power On  
Write Prohibition by the WPB Pin  
Write Prohibition Block Setting  
Prevention of Write Mistake at Low Voltage
- Data at Shipment  
Memory Array: FFh  
ID Page : FFh  
Status Register WPEN, BP1, BP0: 0, 0, 0  
Lock Status LS: 0

#### Key Specifications

- Supply Voltage: 1.7 V to 5.5 V
- Ambient Operating Temperature: -40 °C to +85 °C
- Clock Frequency: 10 MHz (Max)
- Write Time: 3.5 ms (Max)
- Write Cycles: 4 Million Times (Ta = 25 °C)
- Data Retention: 200 Years (Ta = 55 °C)

#### Package

SOP-J8

W (Typ) x D (Typ) x H (Max)  
4.9 mm x 6.0 mm x 1.65 mm

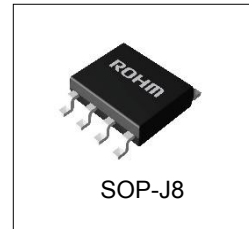


Figure 2

#### Applications

- Ordinary Electronic Equipment (such as AV Equipment, OA Equipment, Telecommunication Equipment, Home Electronic Appliances, Amusement Equipment, etc.).

#### Typical Application Circuit

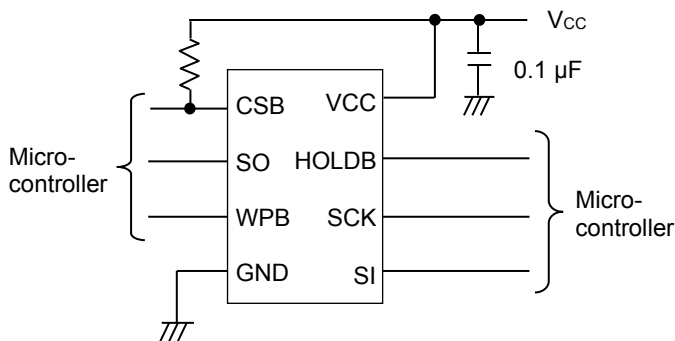


Figure 1. Typical Application Circuit

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## Pin Configuration

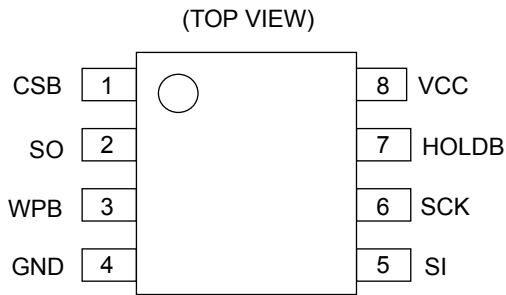


Figure 3. Pin Configuration

## Pin Description

Pin No.	Pin Name	Input/Output	Descriptions
1	CSB	Input	Chip select input
2	SO	Output	Serial data output
3	WPB	Input	Write protect input
4	GND	-	All input/output reference voltage, 0 V
5	SI	Input	Serial data input
6	SCK	Input	Serial clock input
7	HOLDB	Input	Hold input
8	VCC	-	Power supply

## Block Diagram

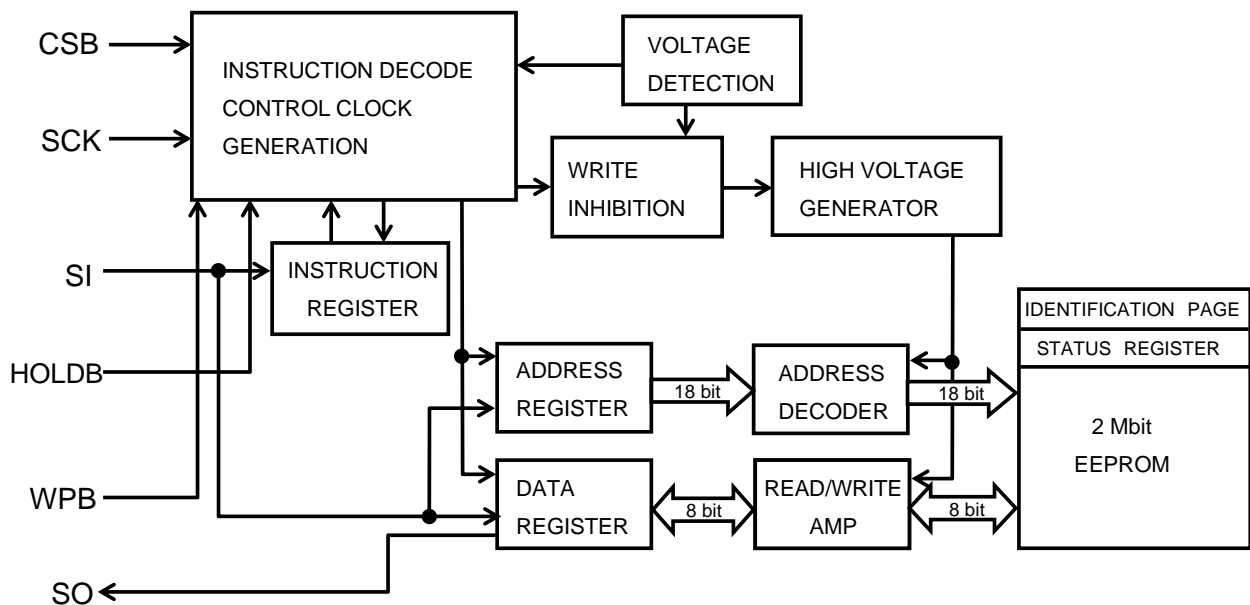


Figure 4. Block Diagram

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	$V_{CC}$	-0.3 to +6.5	V	Ta = 25 °C
Terminal Voltage	-	-0.3 to $V_{CC}+1.0$	V	Ta = 25 °C. The maximum value of pin voltage is not over than 6.5 V. When the pulse width is 50 ns or less, the minimum value of pin voltage is -1.0 V.
Electro Static Discharge (Human Body Model)	$V_{ESD}$	-3000 to +3000	V	Ta = 25 °C
Maximum Output LOW Current (SO)	$I_{OLMAX}$	10	mA	Ta = 25 °C
Maximum Output HIGH Current (SO)	$I_{OHMAX}$	-10	mA	Ta = 25 °C
Maximum Junction Temperature	$T_{jmax}$	150	°C	-
Storage Temperature Range	$T_{stg}$	-65 to +150	°C	-

**Caution 1:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Caution 2:** Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

## Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s <sup>(Note 3)</sup>	2s2p <sup>(Note 4)</sup>	
SOP-J8				
Junction to Ambient	$\theta_{JA}$	149.3	76.9	°C/W
Junction to Top Characterization Parameter <sup>(Note 2)</sup>	$\Psi_{JT}$	18	11	°C/W

(Note 1) Based on JESD51-2A (Still-Air)

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 $\mu$ m

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 $\mu$ m	74.2 mm x 74.2 mm	35 $\mu$ m	74.2 mm x 74.2 mm	70 $\mu$ m

**Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	1.7	-	5.5	V
Ambient Operating Temperature	T <sub>a</sub>	-40	-	+85	°C
Bypass Capacitor <sup>(Note 5)</sup>	C	0.1	-	-	μF

(Note 5) Connect a bypass capacitor between the IC's VCC and GND pin.

**Input/Output Capacitance (T<sub>a</sub> = 25 °C, f = 5 MHz)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance <sup>(Note 6)</sup>	C <sub>IN</sub>	-	-	8	pF	V <sub>IN</sub> = GND
Output Capacitance <sup>(Note 6)</sup>	C <sub>OUT</sub>	-	-	8	pF	V <sub>OUT</sub> = GND

(Note 6) Not 100 % Tested.

**Memory Cell Characteristics (V<sub>CC</sub> = 1.7 V to 5.5 V)**

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Write Cycles <sup>(Note 7) (Note 8)</sup>	-	4,000,000	-	-	Times	T <sub>a</sub> = 25 °C
Data Retention <sup>(Note 7)</sup>	-	200	-	-	Years	T <sub>a</sub> = 55 °C

(Note 7) Not 100 % Tested.

(Note 8) The Write Cycles is defined for unit of 4 data bytes with the same address bits of WA17 to WA2.

Electrical Characteristics (Unless otherwise specified, Ta = -40 °C to +85 °C, V<sub>CC</sub> = 1.7 V to 5.5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage	V <sub>IH</sub>	0.7V <sub>CC</sub>	-	V <sub>CC</sub> +1.0	V	-
Input Low Voltage	V <sub>IL</sub>	-0.3 <sup>(Note 9)</sup>	-	+0.3V <sub>CC</sub>	V	-
Output Low Voltage 1	V <sub>OL1</sub>	0	-	0.4	V	I <sub>OL</sub> = 3.0 mA, 2.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Output Low Voltage 2	V <sub>OL2</sub>	0	-	0.2	V	I <sub>OL</sub> = 1.0 mA, 1.7 V ≤ V <sub>CC</sub> < 2.5 V
Output High Voltage 1	V <sub>OH1</sub>	0.8V <sub>CC</sub>	-	V <sub>CC</sub>	V	I <sub>OH</sub> = -2.0 mA, 2.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Output High Voltage 2	V <sub>OH2</sub>	0.8V <sub>CC</sub>	-	V <sub>CC</sub>	V	I <sub>OH</sub> = -400 μA, 1.7 V ≤ V <sub>CC</sub> < 2.5 V
Input Leakage Current	I <sub>LI</sub>	-1	-	+1	μA	V <sub>IN</sub> = 0 V to V <sub>CC</sub>
Output Leakage Current	I <sub>LO</sub>	-1	-	+1	μA	V <sub>OUT</sub> = 0 V to V <sub>CC</sub> , CSB = V <sub>CC</sub>
Supply Current (WRITE) <sup>(Note 10)</sup>	I <sub>CC1</sub>	-	-	3.0	mA	V <sub>CC</sub> = 5.5 V, f <sub>SCK</sub> = 10 MHz, t <sub>EW</sub> = 3.5 ms V <sub>IH</sub> /V <sub>IL</sub> = 0.9V <sub>CC</sub> /0.1V <sub>CC</sub> , SO = OPEN
Supply Current (READ) <sup>(Note 10)</sup>	I <sub>CC2</sub>	-	-	1.0	mA	V <sub>CC</sub> = 1.7 V, f <sub>SCK</sub> = 5 MHz V <sub>IH</sub> /V <sub>IL</sub> = 0.9V <sub>CC</sub> /0.1V <sub>CC</sub> , SO = OPEN
	I <sub>CC3</sub>	-	-	1.5	mA	V <sub>CC</sub> = 2.5 V, f <sub>SCK</sub> = 5 MHz V <sub>IH</sub> /V <sub>IL</sub> = 0.9V <sub>CC</sub> /0.1V <sub>CC</sub> , SO = OPEN
	I <sub>CC4</sub>	-	-	3.0	mA	V <sub>CC</sub> = 5.5 V, f <sub>SCK</sub> = 5 MHz V <sub>IH</sub> /V <sub>IL</sub> = 0.9V <sub>CC</sub> /0.1V <sub>CC</sub> , SO = OPEN
	I <sub>CC5</sub>	-	-	4.0	mA	V <sub>CC</sub> = 5.5 V, f <sub>SCK</sub> = 10 MHz V <sub>IH</sub> /V <sub>IL</sub> = 0.9V <sub>CC</sub> /0.1V <sub>CC</sub> , SO = OPEN
Standby Current	I <sub>SB</sub>	-	-	5	μA	V <sub>CC</sub> = 5.5 V CSB = HOLDB = WPB = V <sub>CC</sub> , SCK = SI = V <sub>CC</sub> or 0 V, SO = OPEN

(Note 9) When the pulse width is 50 ns or less, it is -1.0 V.

(Note 10) The average value during operation.

## AC Characteristics (Unless otherwise specified, Ta = -40 °C to +85 °C, CL = 30 pF, VCC = 1.7 V to 5.5 V)

Parameter	Symbol	1.7 V ≤ VCC < 2.5 V			2.5 V ≤ VCC < 4.5 V			4.5 V ≤ VCC ≤ 5.5 V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SCK Frequency	f <sub>SCK</sub>	0.01	-	5	0.01	-	5	0.01	-	10	MHz
SCK High Time	t <sub>SCKWH</sub>	80	-	-	80	-	-	40	-	-	ns
SCK Low Time	t <sub>SCKWL</sub>	80	-	-	80	-	-	40	-	-	ns
CSB High Time	t <sub>CS</sub>	85	-	-	85	-	-	40	-	-	ns
CSB Setup Time	t <sub>CSS</sub>	60	-	-	60	-	-	30	-	-	ns
CSB Hold Time	t <sub>CSH</sub>	60	-	-	60	-	-	30	-	-	ns
SCK Setup Time	t <sub>SCKS</sub>	60	-	-	60	-	-	30	-	-	ns
SCK Hold Time	t <sub>SCKH</sub>	60	-	-	60	-	-	30	-	-	ns
SI Setup Time	t <sub>DIS</sub>	20	-	-	20	-	-	10	-	-	ns
SI Hold Time	t <sub>DIH</sub>	20	-	-	20	-	-	10	-	-	ns
Data Output Delay Time	t <sub>PD</sub>	-	-	80	-	-	50	-	-	30	ns
Output Hold Time	t <sub>OH</sub>	0	-	-	0	-	-	0	-	-	ns
Output Disable Time	t <sub>OZ</sub>	-	-	80	-	-	80	-	-	50	ns
HOLDB Setting Setup Time	t <sub>HFS</sub>	0	-	-	0	-	-	0	-	-	ns
HOLDB Setting Hold Time	t <sub>HFH</sub>	40	-	-	40	-	-	30	-	-	ns
HOLDB Release Setup Time	t <sub>HRS</sub>	0	-	-	0	-	-	0	-	-	ns
HOLDB Release Hold Time	t <sub>HRH</sub>	60	-	-	60	-	-	30	-	-	ns
Time from HOLDB to Output High-Z	t <sub>HOZ</sub>	-	-	80	-	-	80	-	-	50	ns
Time from HOLDB to Output Change	t <sub>HPD</sub>	-	-	100	-	-	80	-	-	50	ns
SCK Rise Time <sup>(Note 11)</sup>	t <sub>RC</sub>	-	-	2	-	-	2	-	-	2	μs
SCK Fall Time <sup>(Note 11)</sup>	t <sub>FC</sub>	-	-	2	-	-	2	-	-	2	μs
Output Rise Time <sup>(Note 11)</sup>	t <sub>RO</sub>	-	-	40	-	-	40	-	-	20	ns
Output Fall Time <sup>(Note 11)</sup>	t <sub>FO</sub>	-	-	40	-	-	40	-	-	20	ns
Write Time	t <sub>EW</sub>	-	-	3.5	-	-	3.5	-	-	3.5	ms

(Note 11) Not 100 % Tested.

## AC Characteristics Condition

Parameter	Symbol	Conditions	Unit
Load Capacitance	CL	30	pF
Input Rise Time	-	50	ns
Input Fall Time	-	50	ns
Input Voltage	-	0.2V <sub>CC</sub> / 0.8V <sub>CC</sub>	V
Input/Output Judgment Voltage	-	0.3V <sub>CC</sub> / 0.7V <sub>CC</sub>	V

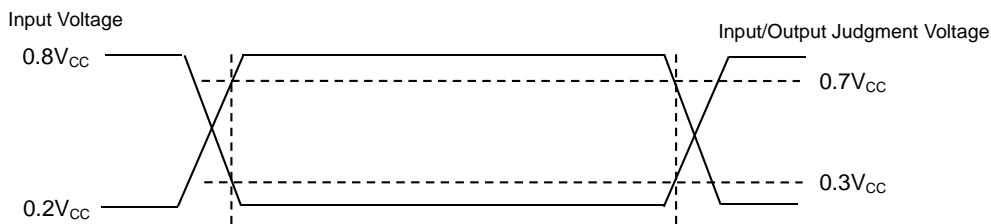


Figure 5. Input/Output Judgment Voltage

Input/Output Timing

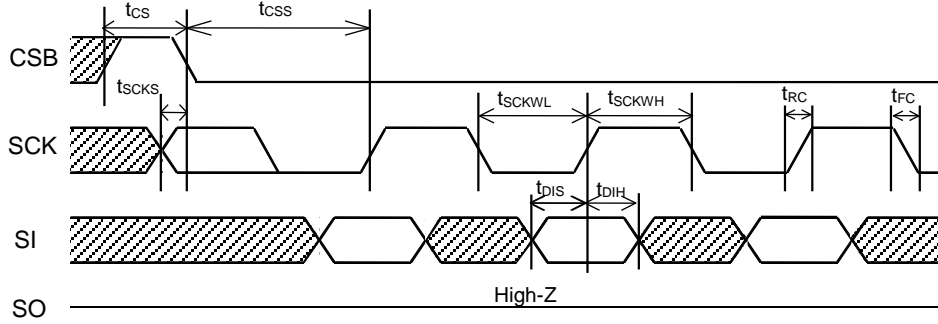


Figure 6-(a). Input Timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the Most Significant Bit MSB.

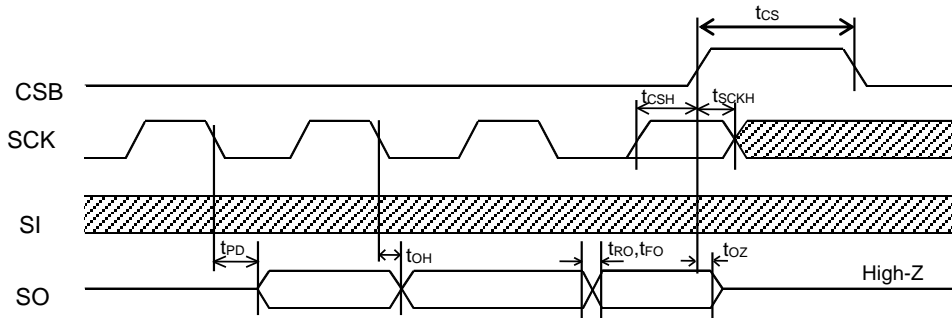


Figure 6-(b). Input/Output Timing

SO is output in sync with data fall edge of SCK. Data is output from the Most Significant Bit MSB.

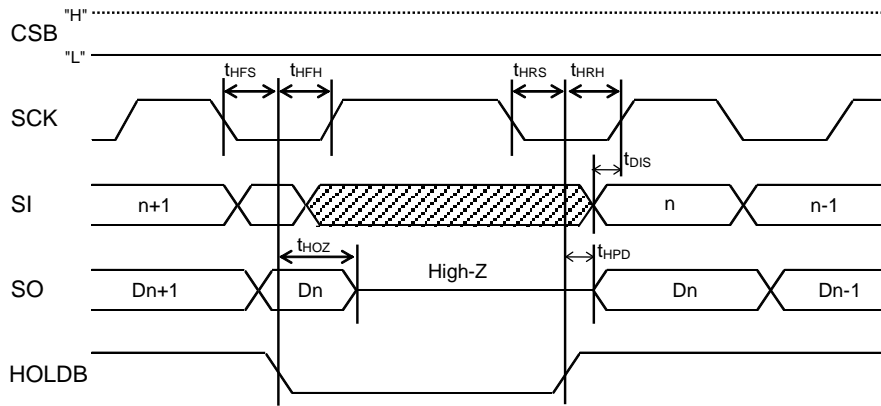


Figure 6-(c). HOLD Timing



Typical Performance Curves

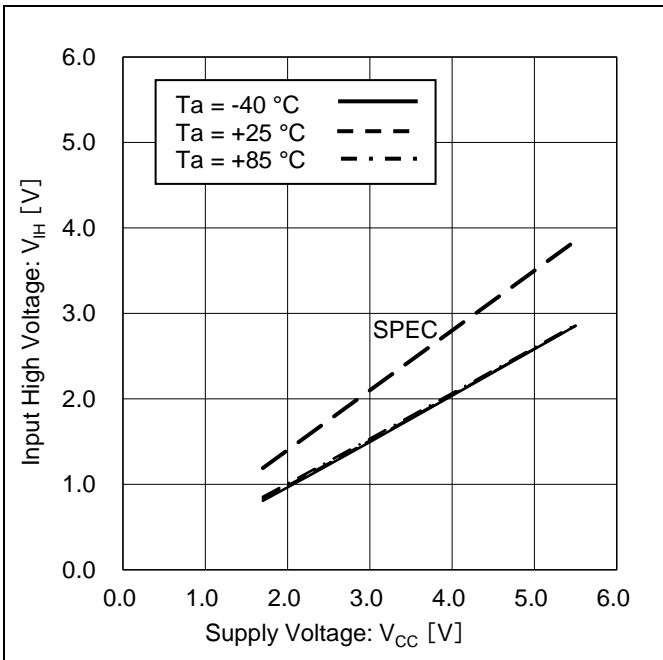


Figure 7. Input High Voltage vs Supply Voltage (CSB, SCK, SI, HOLDB, WPB)

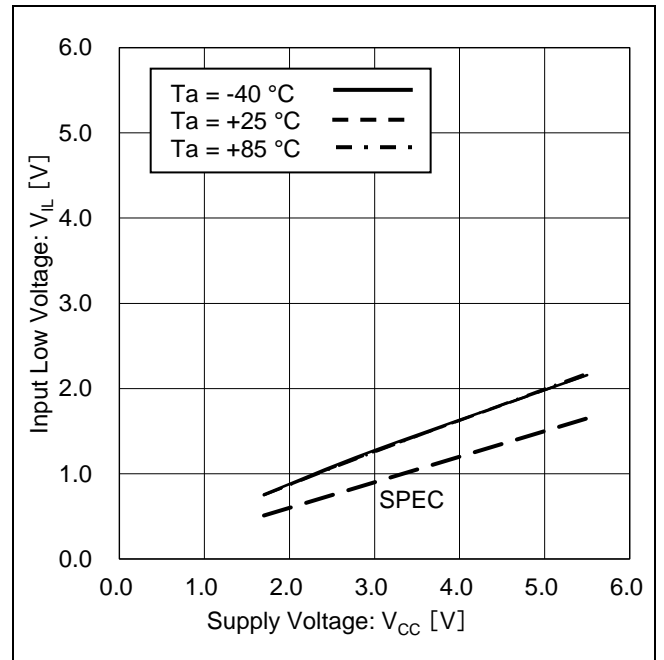


Figure 8. Input Low Voltage vs Supply Voltage (CSB, SCK, SI, HOLDB, WPB)

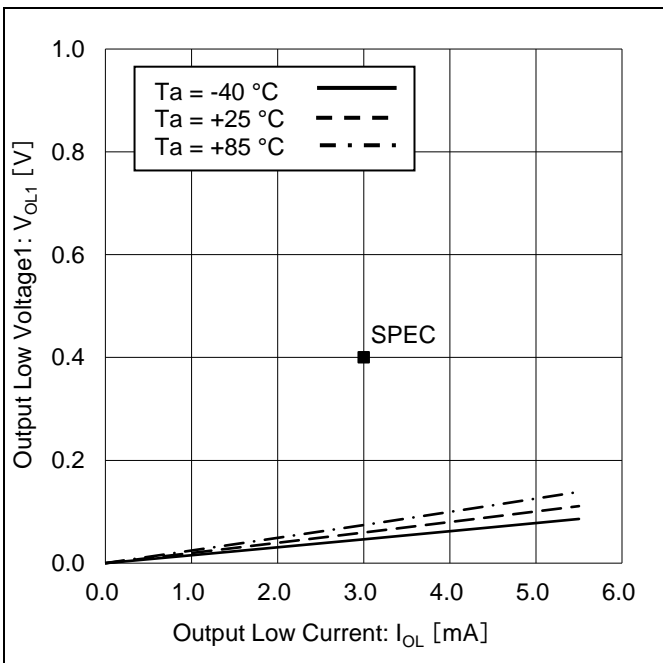


Figure 9. Output Low Voltage1 vs Output Low Current (V<sub>CC</sub> = 2.5 V)

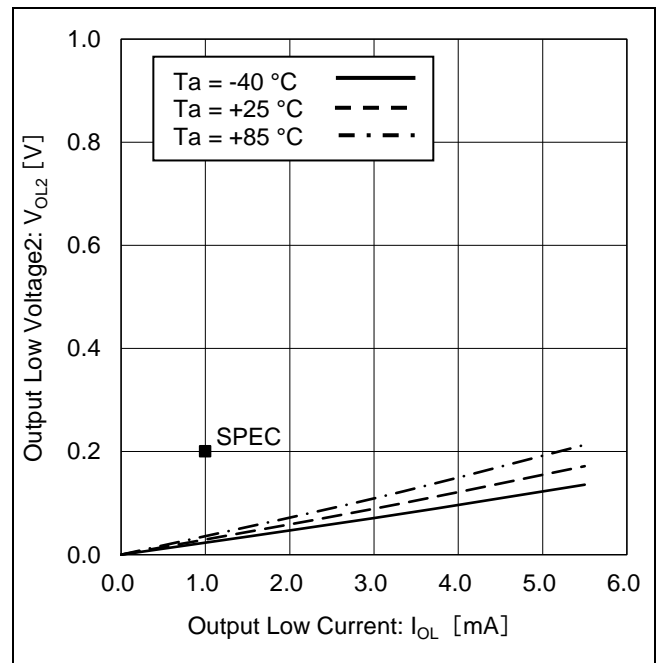


Figure 10. Output Low Voltage2 vs Output Low Current (V<sub>CC</sub> = 1.7 V)

Typical Performance Curves - continued

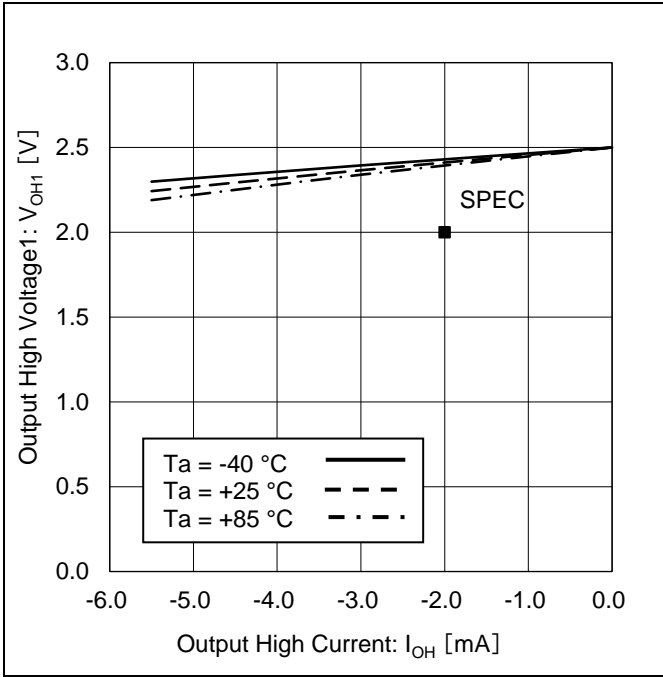


Figure 11. Output High Voltage1 vs Output High Current (V<sub>CC</sub> = 2.5 V)

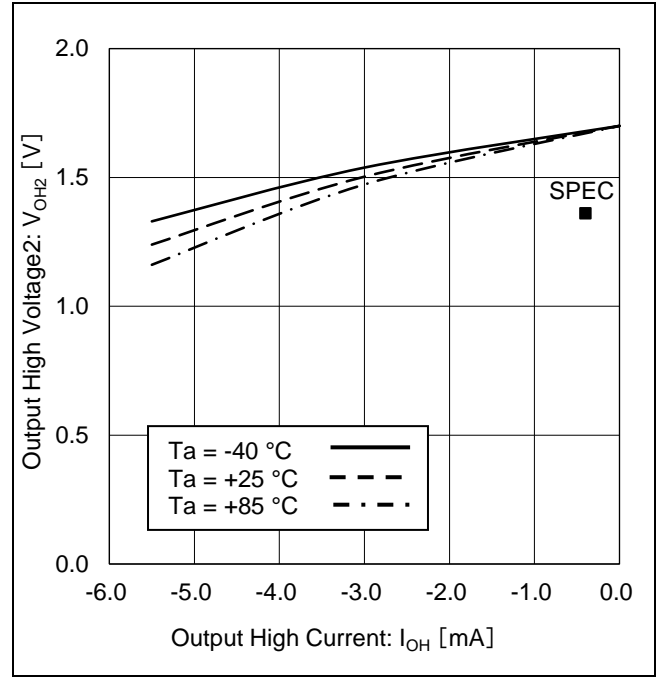


Figure 12. Output High Voltage2 vs Output High Current (V<sub>CC</sub> = 1.7 V)

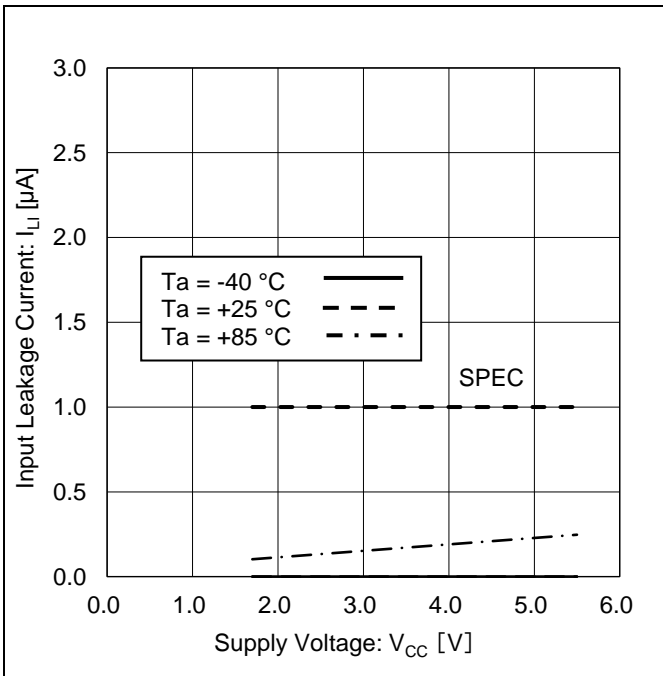


Figure 13. Input Leakage Current vs Supply Voltage (CSB, SCK, SI, HOLDB, WPB)

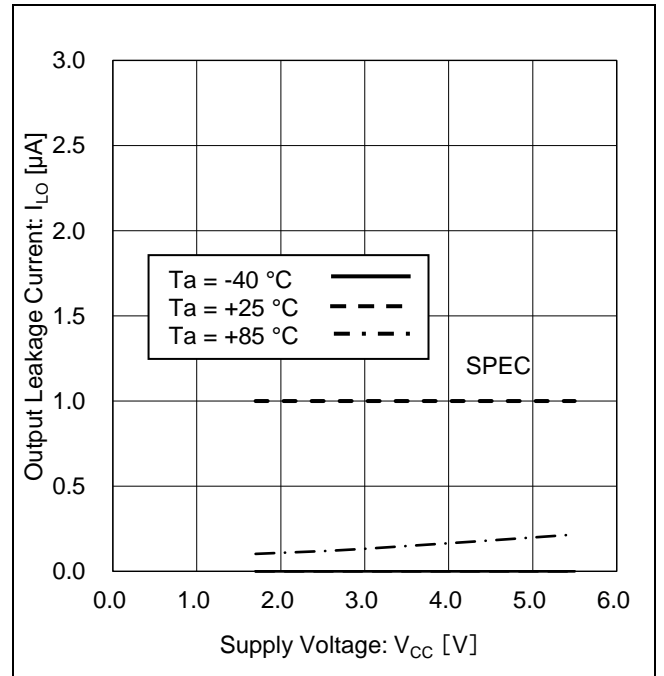


Figure 14. Output Leakage Current vs Supply Voltage (SO)

Typical Performance Curves - continued

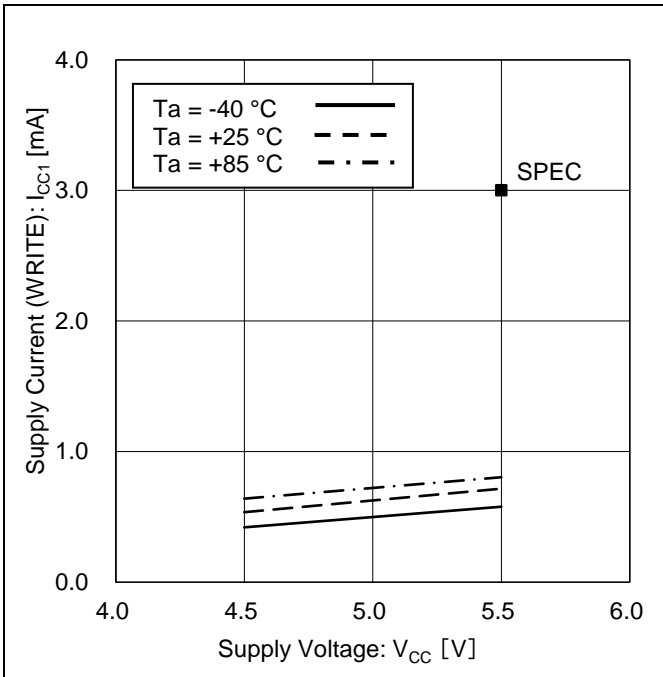


Figure 15. Supply Current (WRITE) vs Supply Voltage

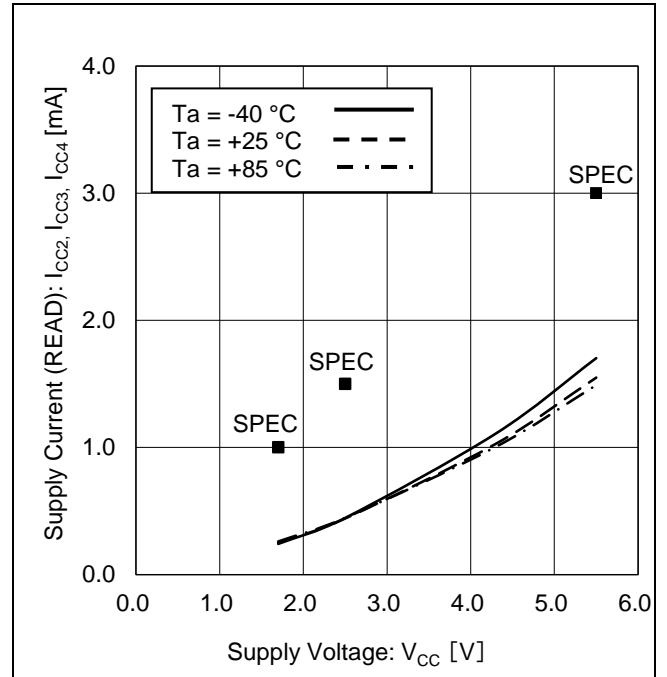


Figure 16. Supply Current (READ) vs Supply Voltage

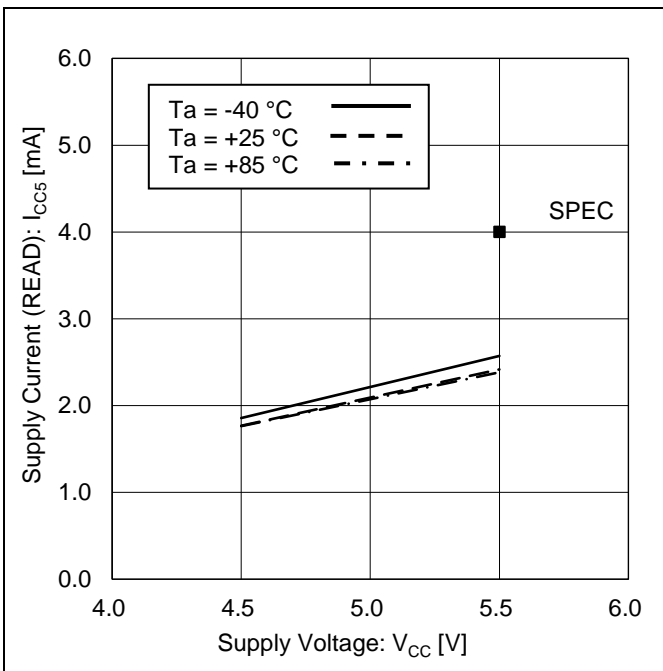


Figure 17. Supply Current (READ) vs Supply Voltage

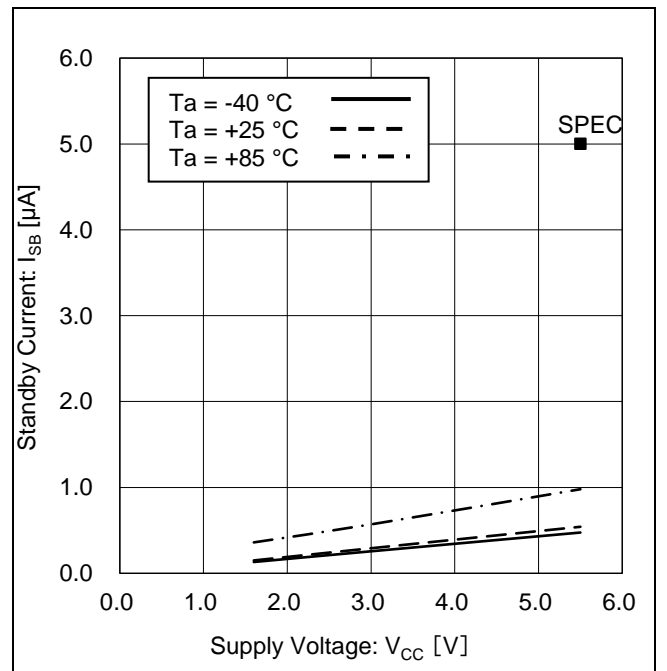


Figure 18. Standby Current vs Supply Voltage

Typical Performance Curves - continued

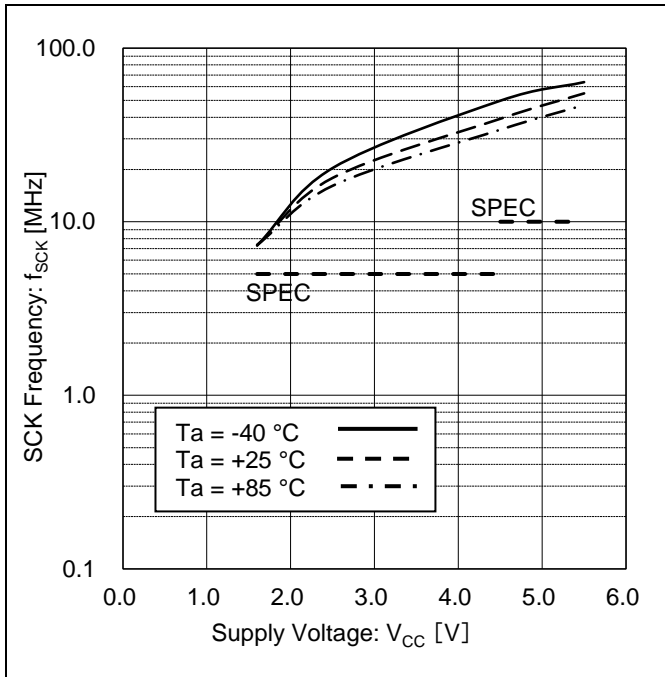


Figure 19. SCK Frequency vs Supply Voltage

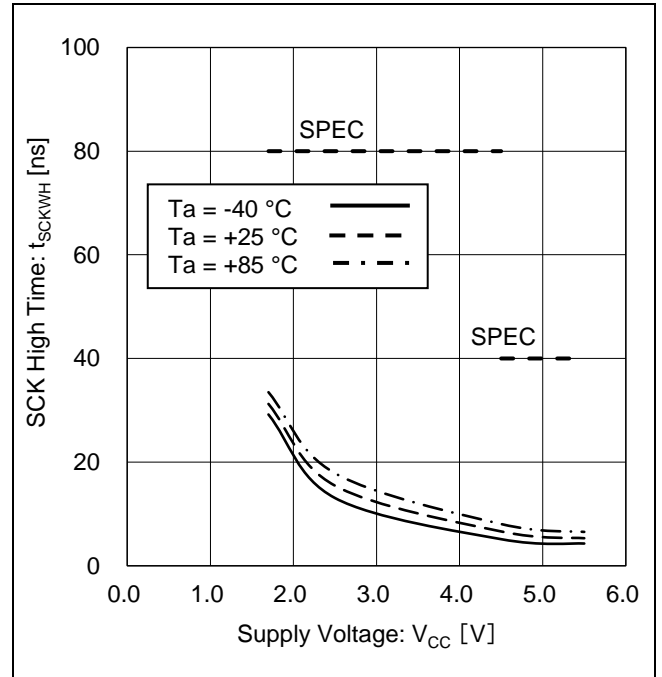


Figure 20. SCK High Time vs Supply Voltage

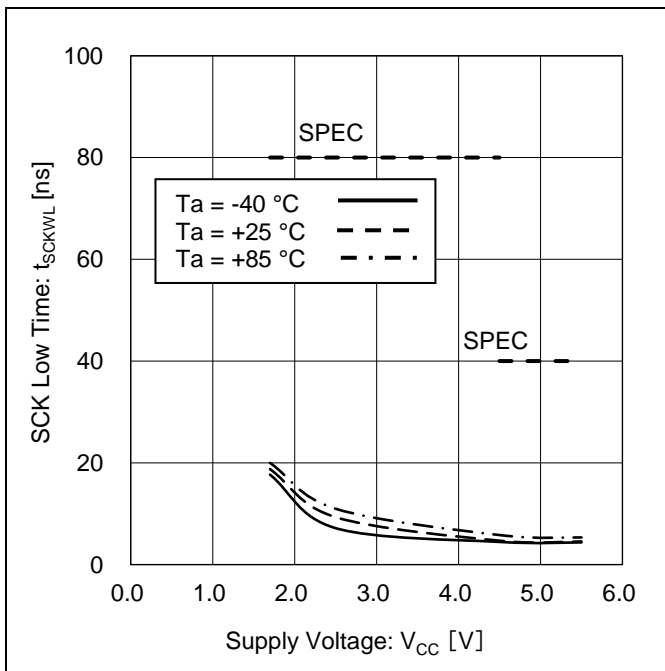


Figure 21. SCK Low Time vs Supply Voltage

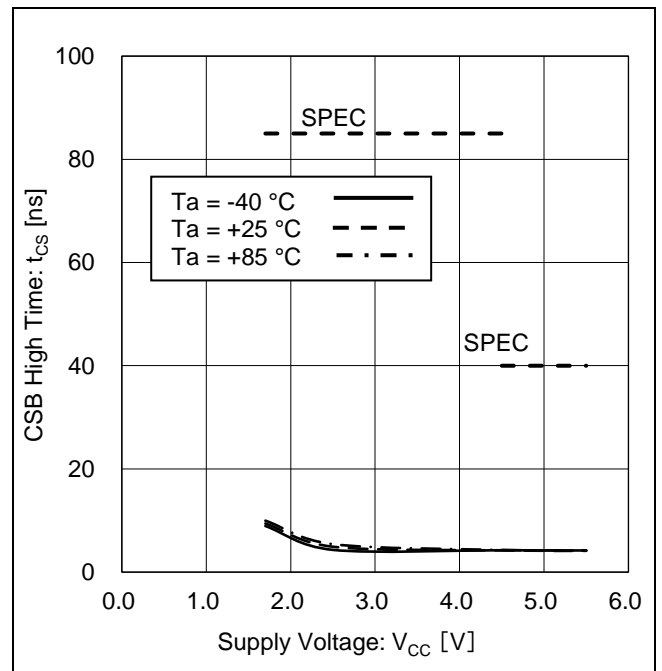


Figure 22. CSB High Time vs Supply Voltage

Typical Performance Curves - continued

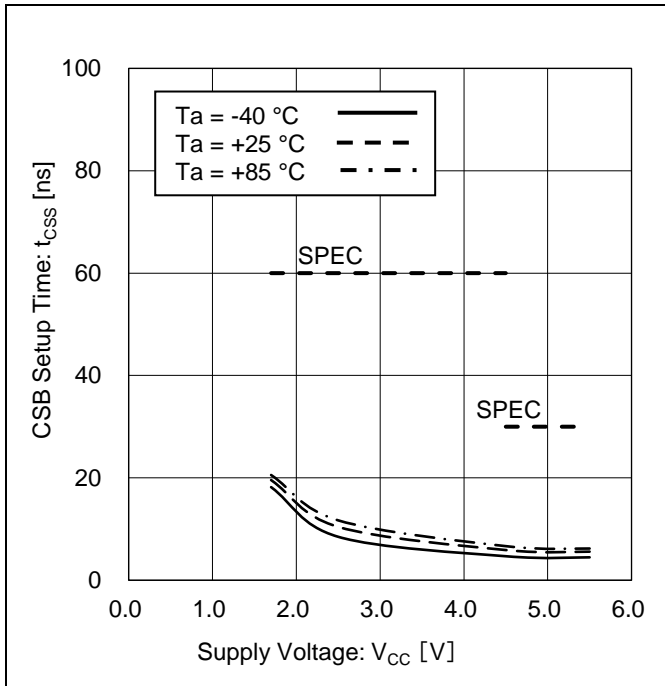


Figure 23. CSB Setup Time vs Supply Voltage

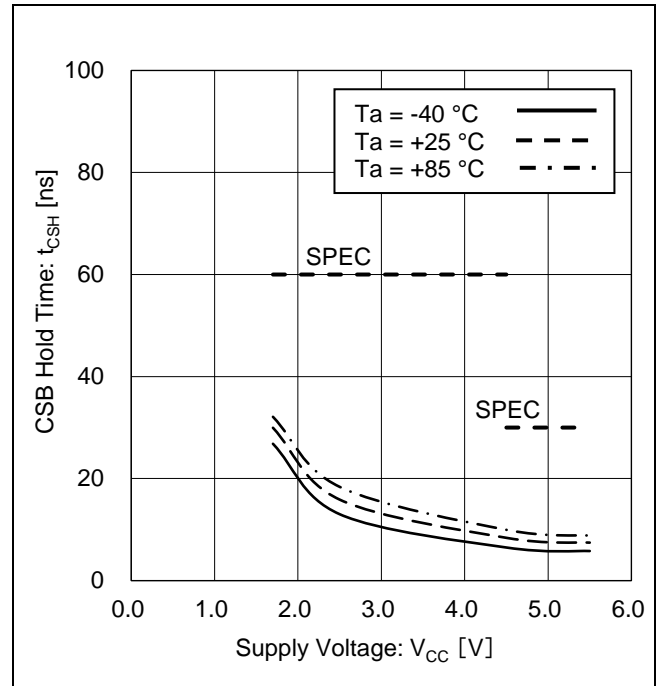


Figure 24. CSB Hold Time vs Supply Voltage

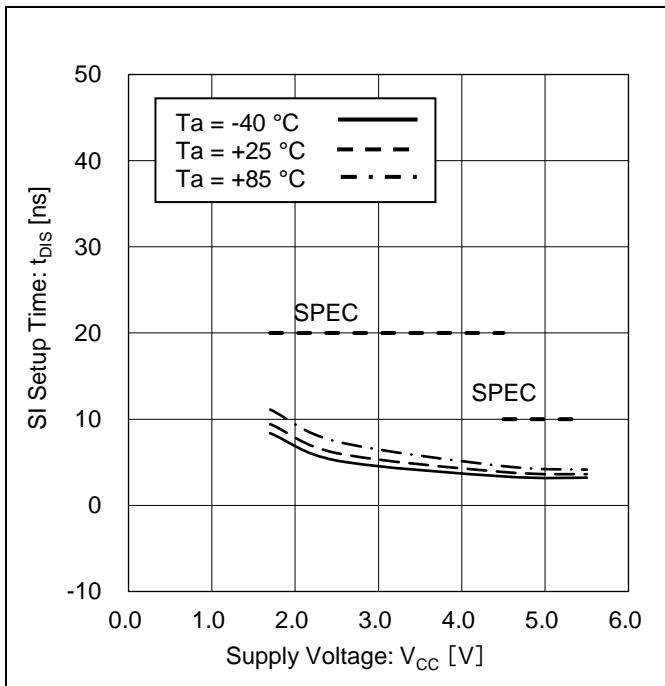


Figure 25. SI Setup Time vs Supply Voltage

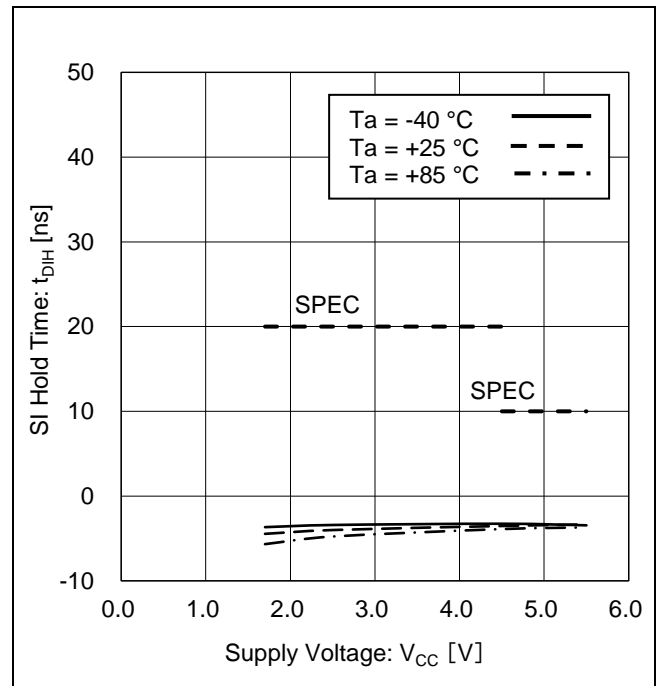


Figure 26. SI Hold Time vs Supply Voltage

Typical Performance Curves - continued

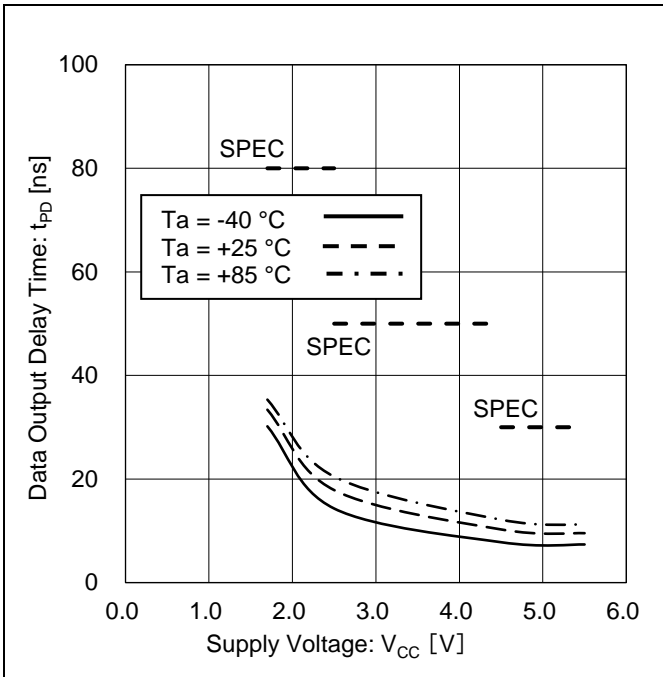


Figure 27. Data Output Delay Time vs Supply Voltage

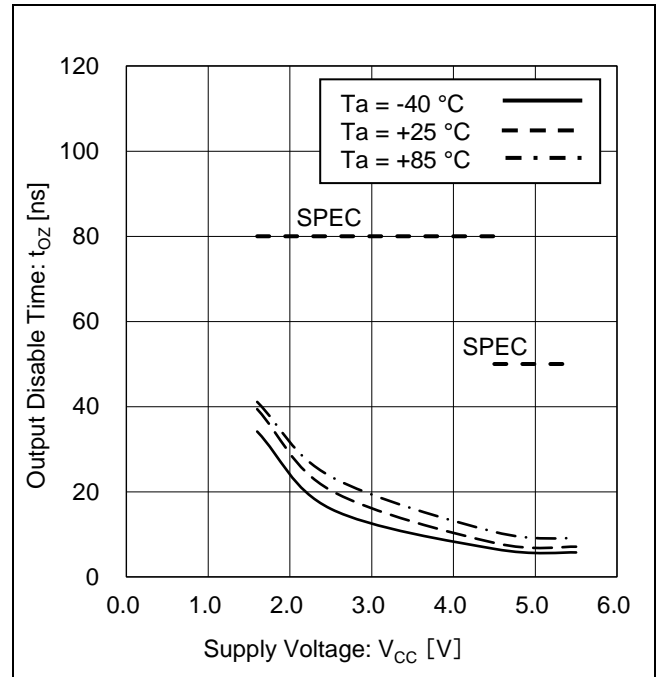


Figure 28. Output Disable Time vs Supply Voltage

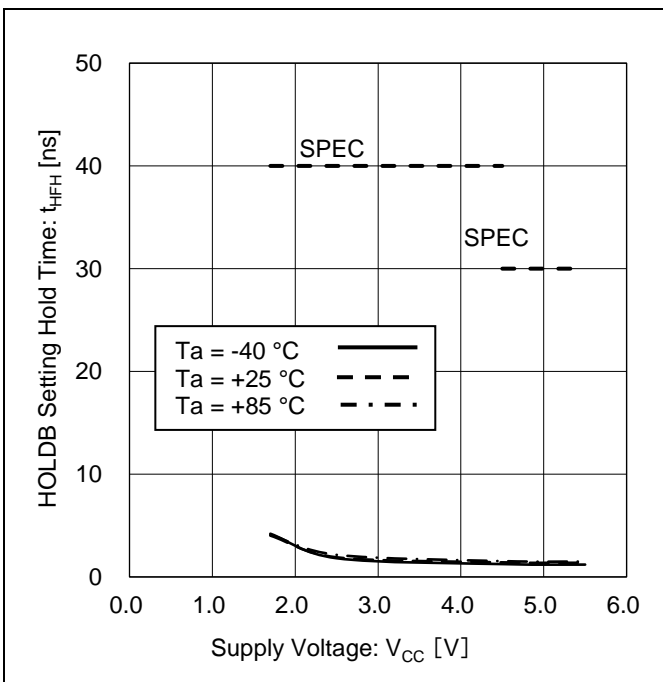


Figure 29. HOLDB Setting Hold Time vs Supply Voltage

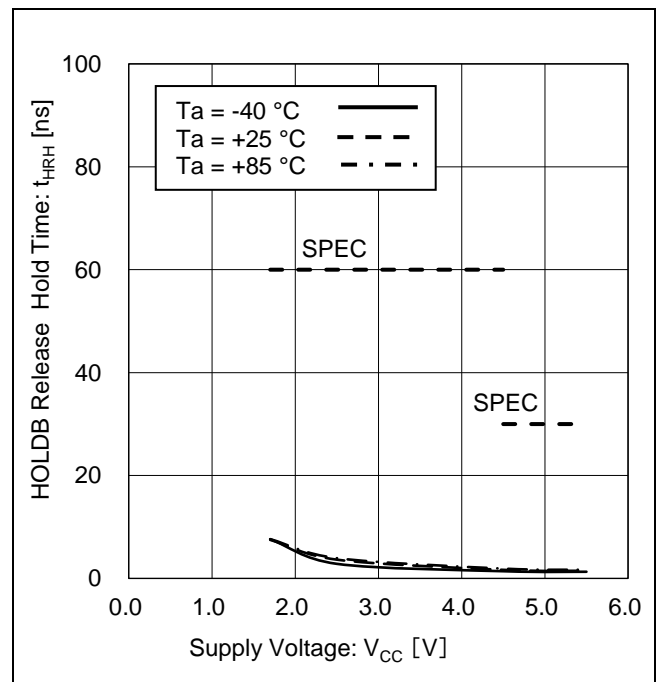


Figure 30. HOLDB Release Hold Time vs Supply Voltage

Typical Performance Curves - continued

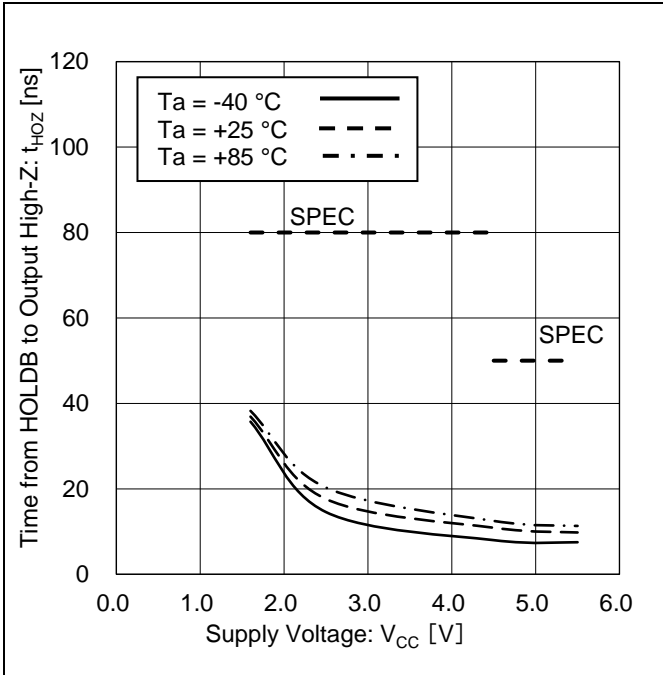


Figure 31. Time from HOLDB to Output High-Z vs Supply Voltage

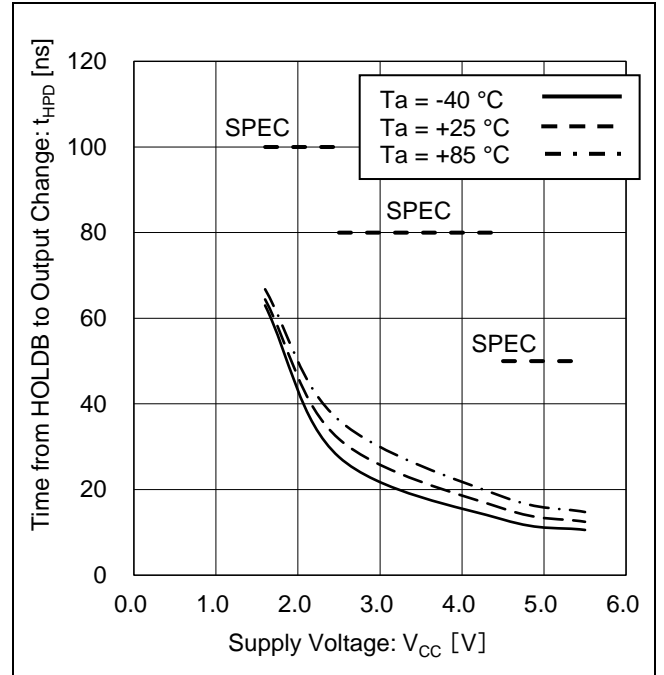


Figure 32. Time from HOLDB to Output Change vs Supply Voltage

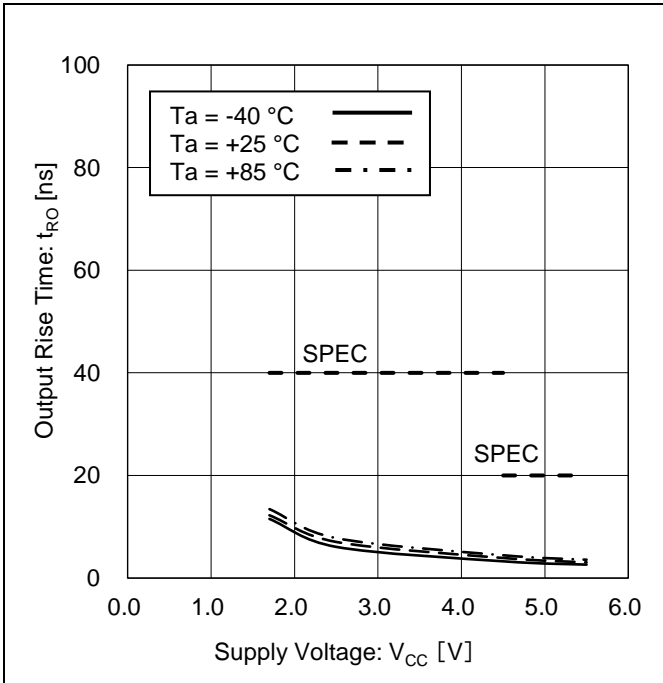


Figure 33. Output Rise Time vs Supply Voltage

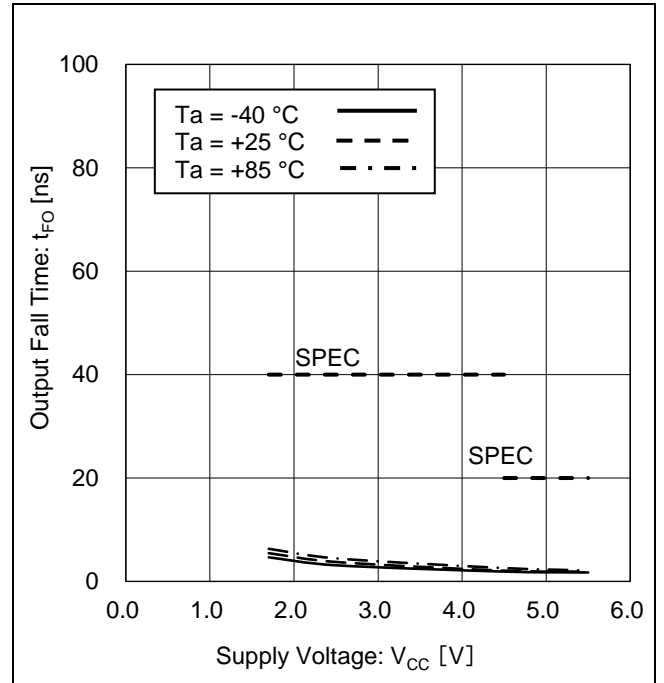


Figure 34. Output Fall Time vs Supply Voltage

## Typical Performance Curves - continued

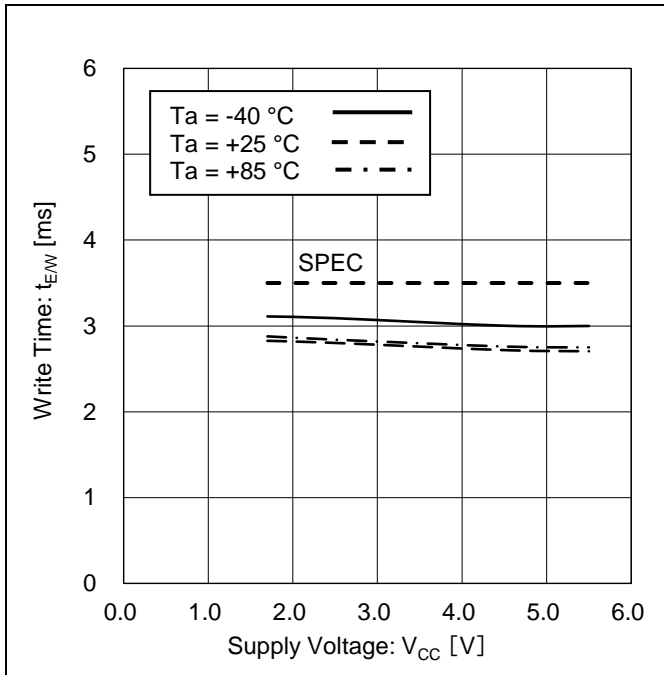


Figure 35. Write Time vs Supply Voltage



## Function Explanation

### 1. Status Register

This IC has the Status Registers. Status Register are of 8 bits and express the following parameters.

WPEN, BP0 and BP1 can be set by Write Status Register command. These 3 bits are memorized into the EEPROM, therefore are valid even when supply voltage is turned off.

Write Cycles and Data Retention of Status Register are same as characteristics of the EEPROM.

WEN can be set by Write Enable command and Write Disable command. WEN becomes write disable status when supply voltage is turned off.  $\overline{R/B}$  is for write confirmation, therefore cannot be set externally.

The values of Status Register can be read by Read Status Register command.

Table 1. Status Register

D7	D6	D5	D4	D3	D2	D1	D0
WPEN	0	0	0	BP1	BP0	WEN	$\overline{R/B}$

Table 2. Function of Status Register

bit	Memory Location	Function	Content
WPEN	EEPROM	Pin Enable/Disable designation bit for the WPB pin WPEN = 0 = Invalid, WPEN = 1 = Valid	WPEN bit enables/disables the function of the WPB pin.
BP1 BP0	EEPROM	EEPROM Write Disable Block designation bit	BP1 and BP0 bits designate the Write Disable Block of EEPROM. Refer to Table 3. Write Disable Block Setting.
WEN	Register	Write Enable/Write Disable Confirmation bit WEN = 0 = Prohibited WEN = 1 = Permitted	WEN bit indicates the status of write enable or write disable for WRITE, WRSR, WRID, LID.
$\overline{R/B}$	Register	Write Cycle Status (READY/BUSY) Confirmation bit $\overline{R/B}$ = 0 = READY, $\overline{R/B}$ = 1 = BUSY	$\overline{R/B}$ bit indicates the status of READY or BUSY of the write cycle.

Table 3. Write Disable Block Setting

Status Register		Protected Block	Protected Addresses
BP1	BP0		
0	0	None	None
0	1	Upper 1/4	30000h to 3FFFFh
1	0	Upper 1/2	20000h to 3FFFFh
1	1	Whole Memory	00000h to 3FFFFh, ID Page

## Function Explanation - continued

## 2. Write Protect Mode by the WPB pin

By setting WPB = Low with WPEN = 1, Write Status Register command is disabled. Only when WPEN bit is set "1", the WPB pin functions become valid. However, when write cycle is in execution, no interruption can be made.

Table 4. Write Protect Mode

WPEN bit	WPB pin	Instruction	
		WRSR	WRITE/WRID/LID
0	X	Writable	Writable
1	High	Writable	Writable
1	Low	Write Protected	Writable

WPB is normally fixed to High or Low for use, but when WPB is controlled so as to cancel Write Status Register command, pay attention to the following WPB Valid Timing.

Write Status Register command is executed, by setting WPB = Low in cancel valid area, command can be cancelled. The Data area (from 7th fall of SCK to 16th rise of SCK) becomes the cancel valid area. However, once write is started, any input cannot be cancelled. WPB input becomes Don't Care, and cancellation becomes invalid.

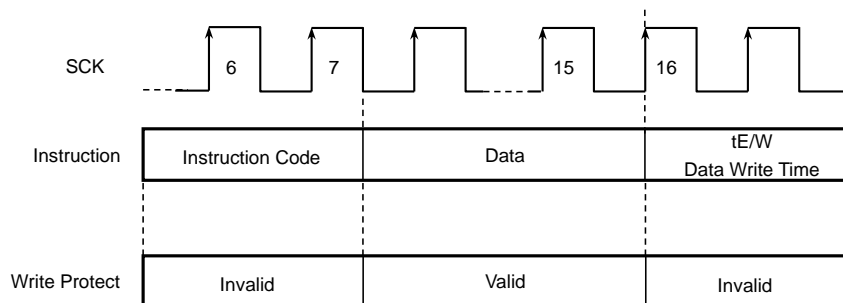


Figure 36. WPB Valid Timing (WRSR)

## 3. Hold Mode by the HOLDB pin

By the HOLDB pin, serial communication can be stopped temporarily (HOLD status). The HOLDB pin carries out serial communications normally when it is High. To get in HOLD status, at serial communication, when SCK = Low, set the HOLDB pin Low.

At HOLD status, SCK and SI become Don't Care, and SO becomes high impedance (High-Z).

To release the HOLD status, set HOLDB = High, when SCK = Low. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after WA5 address input at Read command, after release of HOLD status, by starting WA4 address input, Read command can be restarted. When in HOLD status, leave CSB = Low. When it is set CSB = High in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

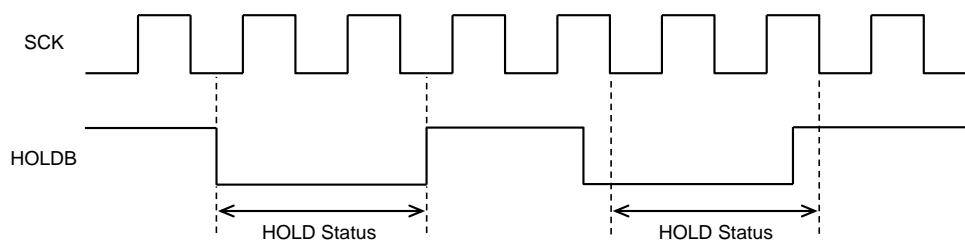


Figure 37. HOLD Status

## Function Explanation - continued

## 4. ID Page

This IC has 256 byte Write Lockable Identification Page (ID Page) in addition to Memory Array. By setting Lock Status (LS) bit to "1" with Lock ID Page command, it is prohibited to write to ID page permanently. It is not reversible to set from ID Page Lock Status (LS = "1") to ID Page Lock Release status (LS = "0").

Table 5. Function of Lock Status

bit	Memory Location	Function	Content
LS	EEPROM	ID Page Lock/Release Status designation bit LS = 0 = ID Page Lock Release LS = 1 = ID Page Lock	LS bit can set Lock Status to ID Page.

## 5. ECC Function

This IC has ECC bits for Error Correction to each 4 data bytes with the same address bits of WA17 to WA2. In the Read operation, even if there is 1 bit data error in the 4 bytes, IC corrects to correct data by ECC function and outputs data corrected. Even if write operation is started with only 1 byte data input, this IC rewrites the data of 4 bytes with the same address bits of WA17 to WA2 and the data of ECC bits added to these 4 bytes data. In order to maximize Write Cycles specified, it is recommended to write with data input of each 4 bytes with the same address bits of WA17 to WA2.

Table 6. Example of 4 data bytes with the same address bits of WA17 to WA2 (Address 00000h, 00001h, 00002h, 00003h)

Same Address Bits from WA17 to WA2																Non-Common		Address
WA 17	WA 16	WA 15	WA 14	WA 13	WA 12	WA 11	WA 10	WA 9	WA 8	WA 7	WA 6	WA 5	WA 4	WA 3	WA 2	WA 1	WA 0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00000h
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	00001h
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	00002h
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	00003h

## Instruction Mode

After setting the CSB pin from High to Low, to execute each command, input Instruction Code, Address and Data from the Most Significant Bit MSB.

Table 7. Instruction Mode

Instruction	Content	Instruction Code (8 bit)	Address (MSB) / Data (8 bit)	Address (8 bit)	Address (LSB) (8 bit)	Data (8 bit)
WREN	Write Enable	0000 0110	-	-	-	-
WRDI	Write Disable	0000 0100	-	-	-	-
READ	Read	0000 0011	WA17, WA16 <sup>(Note 12)</sup>	WA15 to WA8	WA7 to WA0	D7 to D0 Output
WRITE	Write	0000 0010	WA17, WA16 <sup>(Note 12)</sup>	WA15 to WA8	WA7 to WA0	D7 to D0 Input
RDSR	Read Status Register	0000 0101	D7 to D0 Output <sup>(Note 13)</sup>	-	-	-
WRSR	Write Status Register	0000 0001	D7 to D0 Input <sup>(Note 13)</sup>	-	-	-
RDID	Read ID Page	1000 0011	0000 0000	0000 0000	WA7 to WA0	D7 to D0 Output
WRID	Write ID Page	1000 0010	0000 0000	0000 0000	WA7 to WA0	D7 to D0 Input
RDLS	Read Lock Status	1000 0011	0000 0000	0000 0100	0000 0000	D7 to D0 Output <sup>(Note 14)</sup>
LID	Lock ID page	1000 0010	0000 0000	0000 0100	0000 0000	D7 to D0 Input <sup>(Note 14)</sup>

(Note 12) WA23 to WA18 = Don't Care

(Note 13) Refer to Figure 44 and Figure 45

(Note 14) Refer to Figure 48 and Figure 49

## Timing Chart

## 1. Write Enable Command (WREN)

It is set to write enable status by Write Enable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Enable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

Before carrying out Write command, Write Status Register command, Write ID Page command and Lock ID Page command, it is necessary to set write enable status by the Write Enable command.

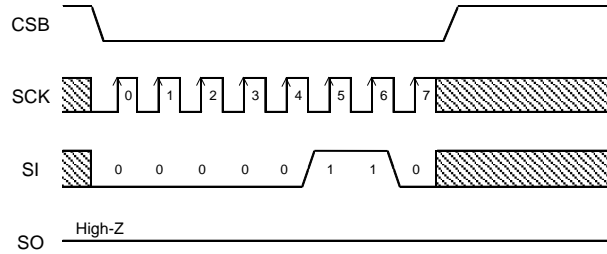


Figure 38. Write Enable Command

## 2. Write Disable Command (WRDI)

It is set to write disable status, WEN bit becomes to "0", by Write Disable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Disable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

If Write command, Write Status Register command, Write ID Page command or Lock ID Page command is input in the write disable status, commands are cancelled. And even in the write enable status, once Write command, Write Status Register command, Write ID Page command or Lock ID Page is executed, it gets in the write disable status.

After power on, this IC is in write disable status.

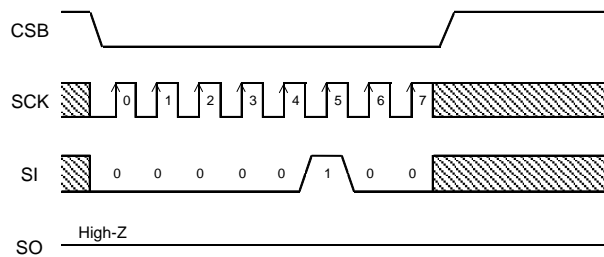


Figure 39. Write Disable Command

## Timing Chart - continued

## 3. Read Command (READ)

By Read command, data of EEPROM can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read command. This IC starts data output of the designated address. Data output is started from SCK fall of 31 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bit), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM Array. After reading data of the most significant address, by continuing increment read, data of the least significant address is read.

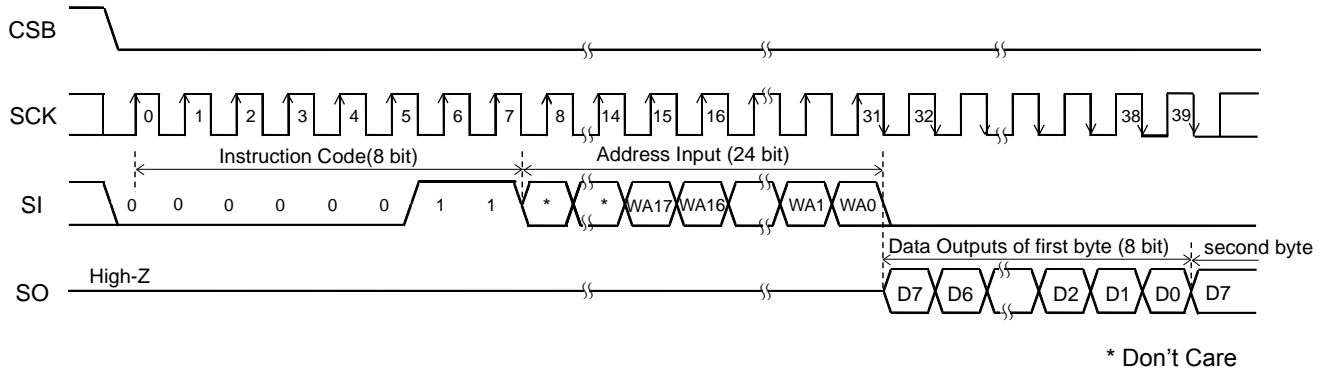


Figure 40. Read Command

## 4. Write Command (WRITE)

By Write command, data of EEPROM can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write command. Then, by making CSB to High, the IC starts write operation. The write time of EEPROM requires time of  $t_{EW}$  (Max 3.5 ms). To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write command is not executed, and this Write command is cancelled.

During write operation, other than Read Status Register command is not accepted.

This IC has Page Write function, and after input of data for 1 byte (8 bit), by continuing data input without setting CSB High to Low, data up to 256 byte can be written for one  $t_{EW}$ . In Page Write, the addressed lower 8 address bits are incremented internally at every time when data of 1 byte is inputted and data is written to respective addresses. When the data input exceeds the last address byte of the page, address rolls over to the first address byte of the same page. It is not recommended to input data over 256 byte, it is recommended to input data in 256 byte. In case of the data input over 256 byte, it is explained in Table 9.

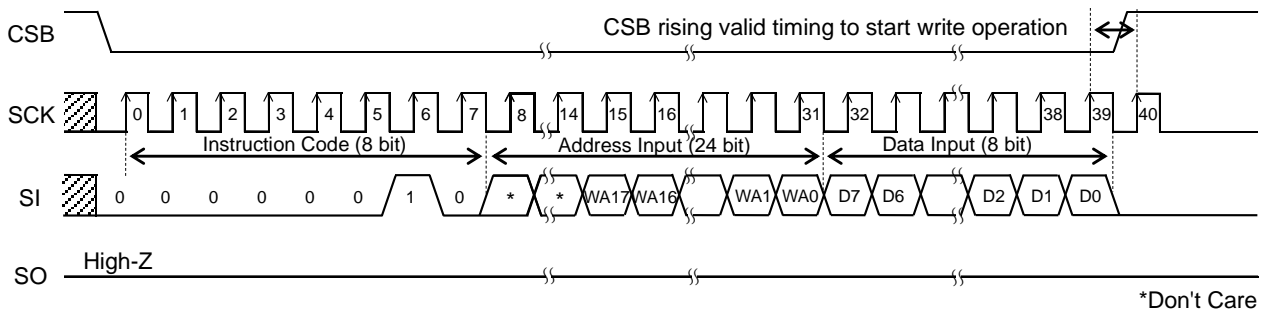


Figure 41. Write Command (Byte Write)

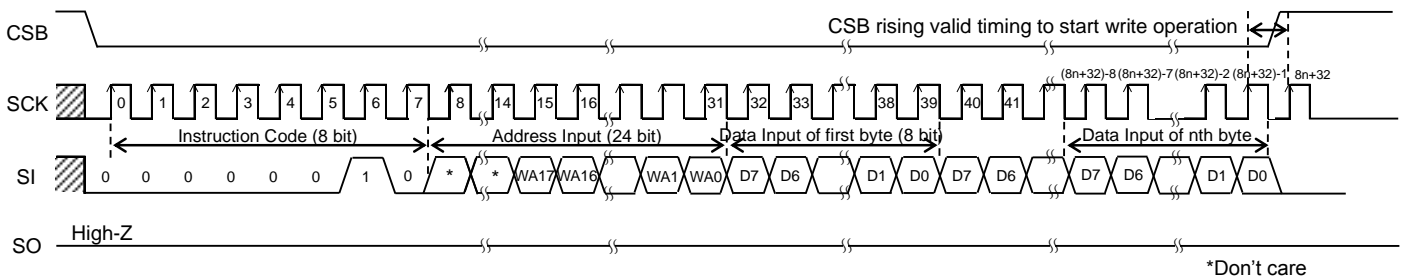


Figure 42. Write Command (Page Write)

## Timing Chart - continued

## 5. Page Write Function

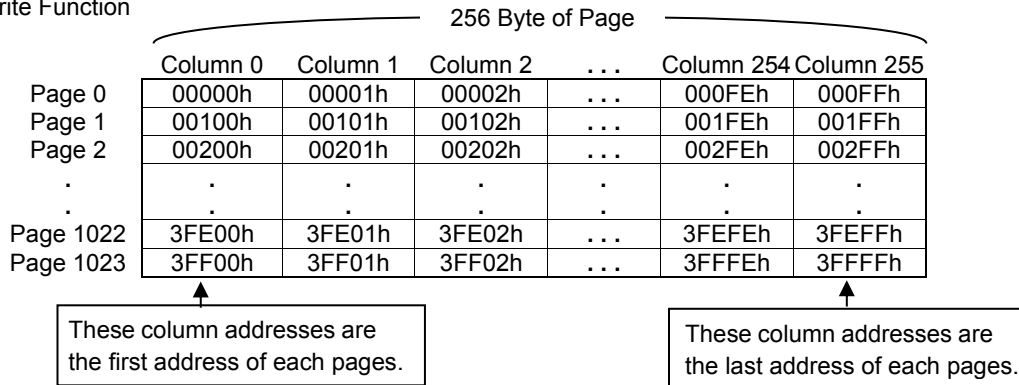


Figure 43. EEPROM physical address for Page Write command (256 Byte)

(1) In case of Page Write command with 256 byte or lower data input

Table 8. Example of Page Write with 2 byte data input

No.	4 Byte group	Group 0				...	...	Group 63			
	Addresses of Page 0	00000h	00001h	00002h	00003h	00004h	...	000FCh	000FDh	000FEh	000FFh
1	Previous Data	00h	01h	02h	03h	04h	...	FCh	FDh	FEh	FFh
2	Input data for Page Write (2 Byte)	AAh	55h	-	-	-	...	-	-	-	-
3	The Data after Write operation	AAh	55h	02h	03h	04h	...	FCh	FDh	FEh	FFh

No.1: These data are EEPROM data before Write operation.

No.2: Inputted 2 byte data AAh, 55h from address 00000h.

No.3: If Write operation is executed with the data of No.2, the data are changed from the data of No.1 to the data of No.3. The data of address 00000h, 00001h are changed to data AAh, 55h, the data of address 00002h, 00003h, the 4 byte group of Group 0, are over-written to data 02h, 03h.  
When Write command is cancelled, EEPROM data keep No.1.

(2) In case of Page Write command with more than 256 byte data input

Table 9. Example of Page Write with 258 byte data input

No.	4 Byte group	Group 0				...	...	Group 63			
	Addresses of Page 0	00000h	00001h	00002h	00003h	00004h	...	000FCh	000FDh	000FEh	000FFh
1	Previous Data	00h	01h	02h	03h	04h	...	FCh	FDh	FEh	FFh
2	Input data for Page Write (258 Byte)	55h	AAh	55h	AAh	55h	...	55h	AAh	55h	AAh
		FFh	00h	-	-	-	...	-	-	-	-
3	The Data after Write operation	FFh	00h	02h	03h	55h	...	55h	AAh	55h	AAh

No.1: These data are initial EEPROM data before Write operation.

No.2: Inputted 258 byte data 55h, AAh, --, 55h, AAh, FFh, 00h from address 00000h.

The data of address 00000h, 00001h are set to data 55h, AAh first. The data of address 00002h, 00003h are set to data 55h, AAh. After inputting data to Maximum byte (000FFh), the data address 00000h, 00001h are set to data FFh, 00h again. No data input to address 00002h, 00003h again.

No.3: If Page Write operation is executed with the data of No.2, the data are changed from the data of No.1 to the data of No.3. The data of address 00000h, 00001h are changed to FFh, 00h inputted data later, not to 55h, AAh inputted data first. The data of address 00002h, 00003h, the 4 byte group of Group 0, are over-written to 02h, 03h of Previous Data, not to 55h, AAh inputted data first. The data of other addresses are changed to 55h, AAh --, 55h, AAh. When Write command is cancelled, EEPROM data keep No.1.

(3) Roll Over

In Page Write command, when data is set to the last address of a page (e.g. address "000FFh" of page 0), the next data will be set to the first address of the same page (e.g. address "00000h" of page 0). Page Write address increment is available in the same page including the address designated at first.

## Timing Chart - continued

## 6. Read Status Register Command (RDSR)

By Read Status register command, data of status register can be read. As for this command, set CSB to Low, then input Instruction Code of Read Status Register command. This IC starts data output of the status register. Data output is started from SCK fall of 7 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, this IC repeats to output data of the status register. Even in write operation, Read Status Register command can be executed.

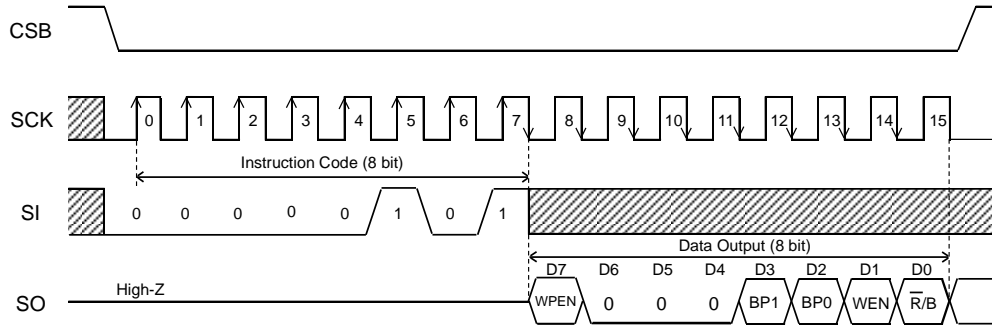


Figure 44. Read Status Register Command

## 7. Write Status Register Command (WRSR)

Write Status Register command can write status register data. The data can be written by this command are 3 bits, that is, WPEN (D7), BP1 (D3) and BP0 (D2) among 8 bits of status register. As for this command, set CSB to Low, and input Instruction Code of Write Status Register command, and input data. Then, by making CSB to High, this IC starts write operation. Write Time requires time of  $t_{EW}$  as same as Write command. As for CSB rise, start CSB after taking the last data bit (D0), and before the next SCK clock starts. At other timing, command is cancelled. To the write disabled block, write cannot be made, and only read can be made. During write operation, other than Read Status Register command is not accepted.

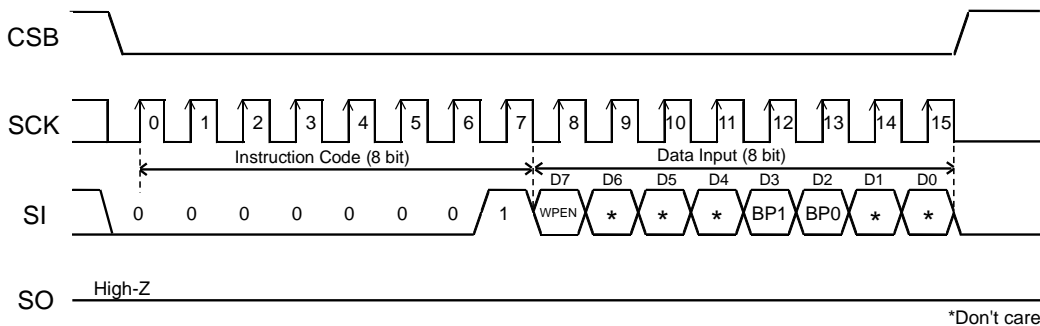


Figure 45. Write Status Register Command



## Timing Chart - continued

## 8. Read ID Page Command (RDID)

By Read ID Page command, data of ID Page can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read ID Page command. By inputting lower address bits WA7 to WA0, it is possible to address to 256 byte ID Page. Data output is started from SCK fall of 31 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, data of the next address can be read. After reading data of the most significant address of ID Page, by continuing increment read, data of the least significant address of ID Page is read.

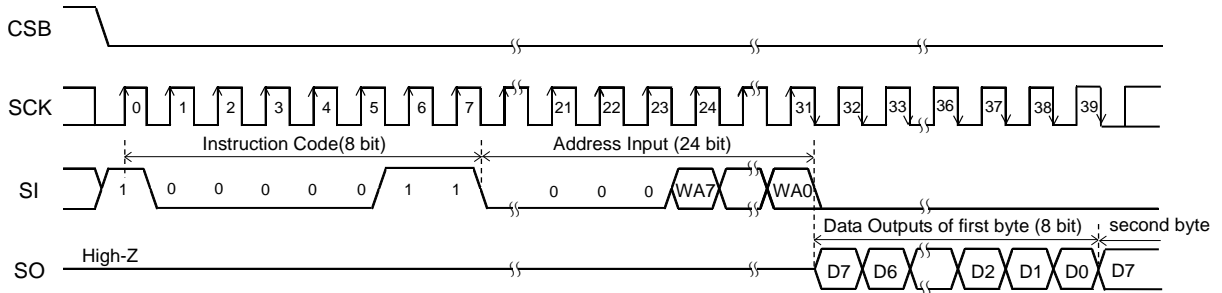


Figure 46. Read ID Page Command

## 9. Write ID Page Command (WRID)

By Write ID Page command, data of ID Page can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write ID Page command. By inputting lower address bits WA7 to WA0, it is possible to address to 256 byte ID Page. Then, by making CSB to High, the IC starts write operation. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write ID Page command is not executed, and this Write ID Page command is cancelled. The write time of EEPROM requires time of  $t_{EW}$  (Max 3.5 ms).

During write operation, other than Read Status Register command is not accepted.

In case of Lock Status (LS) bit "1", Write ID Page command can't be executed.

Write ID Page command has Page Write Function same as Write command.

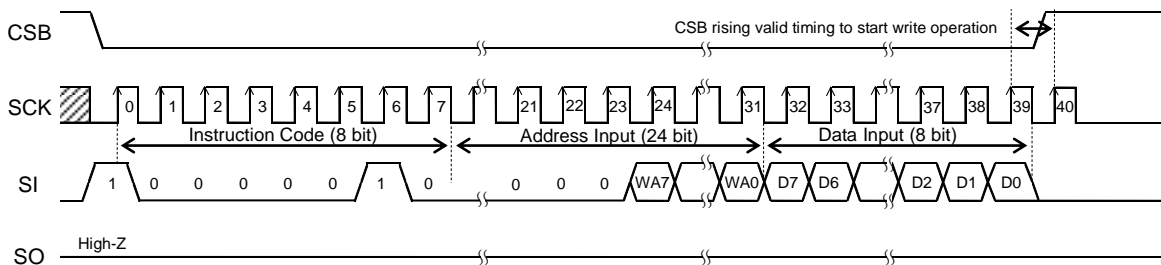


Figure 47. Write ID Page Command

## Timing Chart - continued

## 10. Read Lock Status Command (RDLS)

By Read Lock Status command, data of Lock Status can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read Lock Status command. Data output is started from SCK fall of 31 clock, and from D7 to D0 sequentially. The data D0 indicates Lock Status bit. The data D7 to D1 are Don't Care. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, this IC repeats to output data of the Lock Status byte. In case of Lock Status (LS) bit "1", ID Page is locked, Write ID Page command can't be executed. In case of LS bit "0", ID Page is released to lock, Write ID Page command can be executed.

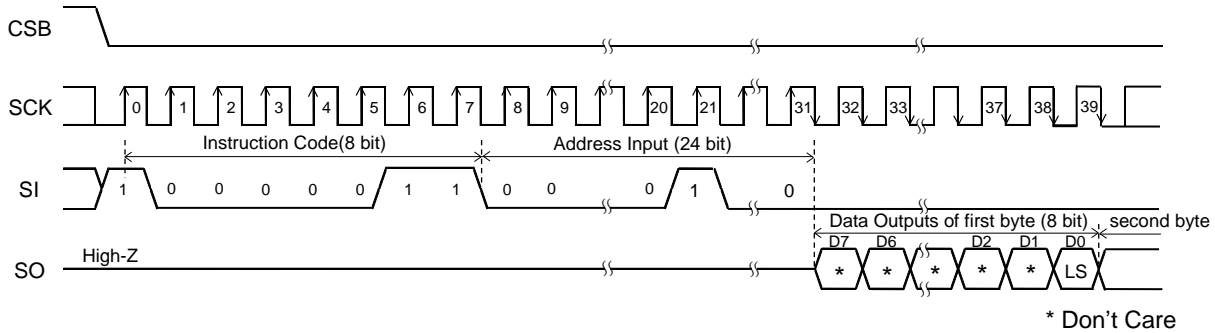


Figure 48. Read Lock Status Command

## 11. Lock ID Page Command (LID)

By Lock ID Page command, data of Lock Status can be written. In case of Lock Status (LS) bit "1", Lock ID Page command can't be executed permanently. As for this command, set CSB to Low, then input address and data after Instruction Code of Lock ID Page command. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Lock ID Page command is not executed, and this Lock ID Page command is cancelled. The write time of EEPROM requires time of  $t_{EW}$  (Max 3.5 ms). During write operation, other than Read Status Register command is not accepted.

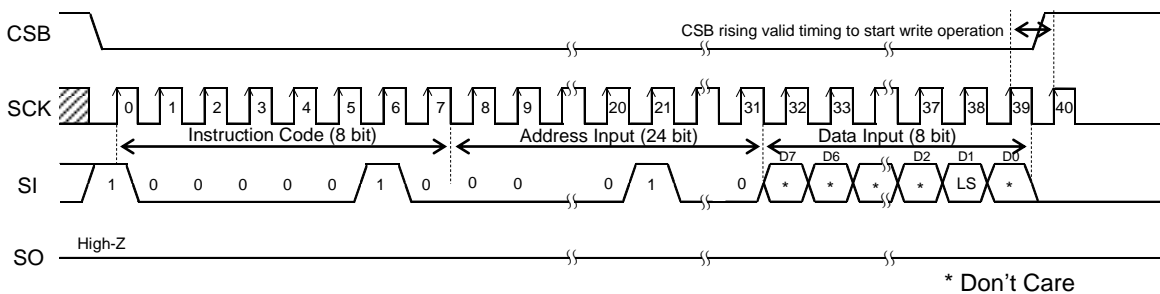


Figure 49. Lock ID Page Command

## At Standby State

## 1. Standby Current

Set CSB = High, and be sure to set SCK, SI, WPB and HOLDB inputs = Low or High. Do not input intermediate voltage.

## 2. Timing

As shown in Figure.50, at standby, when SCK is High, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB = High status.

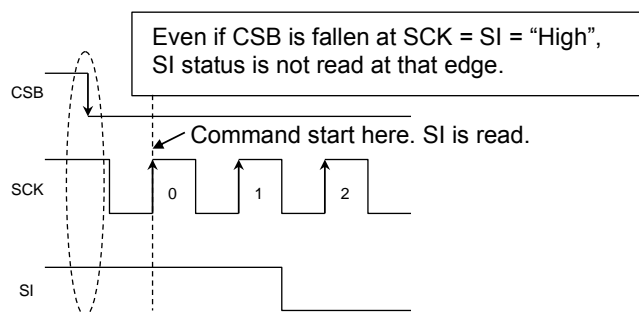


Figure 50. Operating Timing

## Method To Cancel Each Command

### 1. READ, RDID, RDLS

Method to cancel: cancel by CSB = High

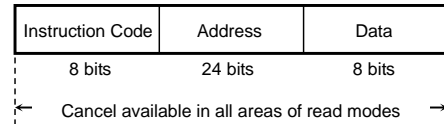


Figure 51. READ, RDID, RDLS Cancel Valid Timing

### 2. RDSR

Method to cancel: cancel by CSB = High

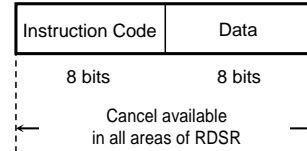


Figure 52. RDSR Cancel Valid Timing

### 3. WRITE, WRID, LID

#### a: Instruction Code, Address Input Area

Cancellation is available by CSB = High.

#### b: Data Input Area (D7 to D1 input area)

Cancellation is available by CSB = High.

#### c: Data Input Area (D0 area)

When CSB is started, write starts.

After CSB rise, cancellation cannot be made by any means.

#### d: $t_{EW}$ Area

Cancellation is available by CSB = High. However, when write starts (CSB is started) in the area c, cancellation cannot be made by any means. And by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

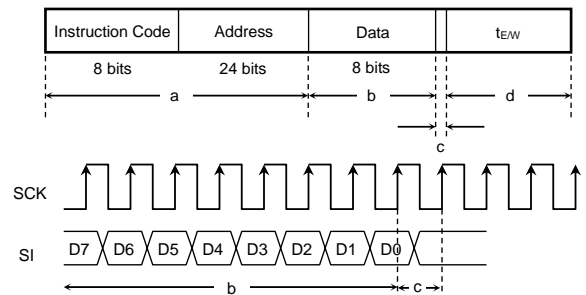


Figure 53. WRITE, WRID, LID Cancel Valid Timing

Note 1) If  $V_{CC}$  is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.

Note 2) If CSB is started at the same timing as that of the SCK rise, write execution/cancel becomes unstable, therefore, it is recommended to rise in SCK = Low area. As for SCK rise, assure timing of  $t_{CSS}/t_{CSH}$  or higher.

### 4. WRSR

#### a: From Instruction code to 15th rising of SCK

Cancel by CSB = High.

#### b: From 15th rising of SCK to 16th rising of SCK (write enable area)

When CSB is started, write starts.

#### c: After 16th rising of SCK

Cancel by CSB = High.

However, when write starts (CSB is started) in the area b, cancellation cannot be made by any means. And, by inputting on SCK clock, cancellation cannot be made.

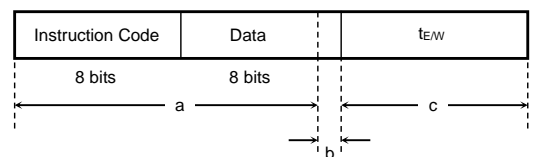
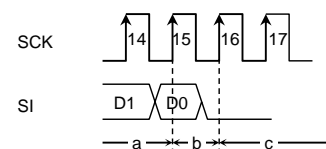


Figure 54. WRSR Cancel Valid Timing

Note 1) If  $V_{CC}$  is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.

Note 2) If CSB is started at the same timing as that of the SCK rise, write execution/cancel becomes unstable, therefore, it is recommended to rise in SCK = Low area. As for SCK rise, assure timing of  $t_{CSS}/t_{CSH}$  or higher.

### 5. WREN/WRDI

#### a: From instruction code to 7th rising of SCK

Cancel by CSB = High.

#### b: Cancellation is not available when CSB is started after 7th clock.

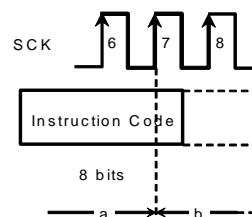


Figure 55. WREN/WRDI Cancel Valid Timing

Application Examples

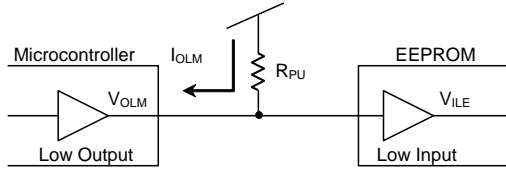
High Speed Operation

In order to realize stable high speed operations, pay attention to the following input/output pin conditions.

1. Pull Up, Pull Down Resistance for Input Pins

When to attach pull up, pull down resistance to EEPROM input pins, select an appropriate value for the microcontroller  $V_{OL}$ ,  $I_{OL}$  from  $V_{IL}$  characteristics of this IC.

2. Pull Up Resistance



$$R_{PU} \geq \frac{V_{CC} - V_{OLM}}{I_{OLM}} \quad (1)$$

$$V_{OLM} \leq V_{ILE} \quad (2)$$

Example) When  $V_{CC} = 5 \text{ V}$ ,  $V_{ILE} = 1.5 \text{ V}$ ,  $V_{OLM} = 0.4 \text{ V}$ ,  $I_{OLM} = 2 \text{ mA}$ , from the equation (1).

$$R_{PU} \geq \frac{5 - 0.4}{2 \times 10^{-3}}$$

$$R_{PU} \geq 2.3 \text{ [k}\Omega\text{]}$$

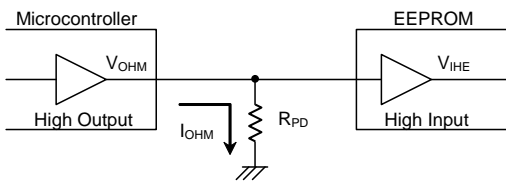
$V_{ILE}$  :  $V_{IL}$  of EEPROM  
 $V_{OLM}$  :  $V_{OL}$  of Microcontroller  
 $I_{OLM}$  :  $I_{OL}$  of Microcontroller

Figure 56. Pull Up Resistance

With the value of  $R_{PU}$  to satisfy the above equation,  $V_{OLM}$  becomes 0.4 V or lower, and with  $V_{ILE} (= 1.5 \text{ V})$ , the equation (2) is also satisfied.

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make the CSB pin pull up.

3. Pull Down Resistance



$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad (3)$$

$$V_{OHM} \geq V_{IHE} \quad (4)$$

Example) When  $V_{CC} = 5 \text{ V}$ ,  $V_{OHM} = V_{CC} - 0.5 \text{ V}$ ,  $I_{OHM} = 0.4 \text{ mA}$ ,  $V_{IHE} = V_{CC} \times 0.7 \text{ V}$ , from the equation (3),

$$R_{PD} \geq \frac{5 - 0.5}{0.4 \times 10^{-3}}$$

$$R_{PD} \geq 11.3 \text{ [k}\Omega\text{]}$$

$V_{IHE}$  :  $V_{IH}$  of EEPROM  
 $V_{OHM}$  :  $V_{OH}$  of Microcontroller  
 $I_{OHM}$  :  $I_{OH}$  of Microcontroller

Figure 57. Pull Down Resistance

Further, by amplitude  $V_{IHE}$ ,  $V_{ILE}$  of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of  $V_{CC}/\text{GND}$  level to input, more stable high speed operations can be realized. On the contrary, when amplitude of  $0.8V_{CC}/0.2V_{CC}$  is input, operation speed becomes slow. (Note 15)

In order to realize more stable high speed operation, it is recommended to make the values of  $R_{PU}$ ,  $R_{PD}$  as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of  $V_{CC}/\text{GND}$  level.

(Note 15) At this moment, operating timing guaranteed value is guaranteed.

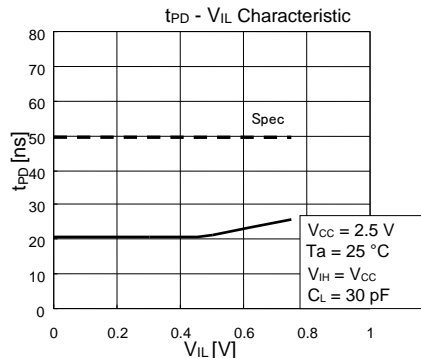


Figure 58.  $V_{IL}$  dependency of Data Output Delay Time  $t_{PD}$

## Application Examples - continued

### 4. SO Load Capacitance Condition

Load capacitance of the SO pin affects upon delay characteristic of SO output. (Data Output Delay Time, Time from HOLDB to High-Z) In order to make output delay characteristic into higher speed, make SO load capacitance small. In concrete, "Do not connect many devices to SO bus", "Make the wire between the controller and EEPROM short", and so forth.

### 5. Other Cautions

Make the wire length from the Microcontroller to EEPROM input signal same length, in order to prevent setup/hold violation to EEPROM, owing to difference of wire length of each input.

## I/O Equivalence Circuits

### 1. Input (CSB, SCK, SI, HOLDB, WPB)

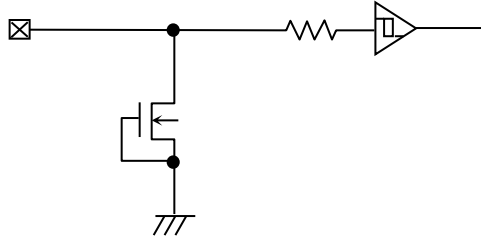


Figure 59. Input Equivalent Circuit (CSB, SCK, SI, HOLDB, WPB)

### 2. Output (SO)

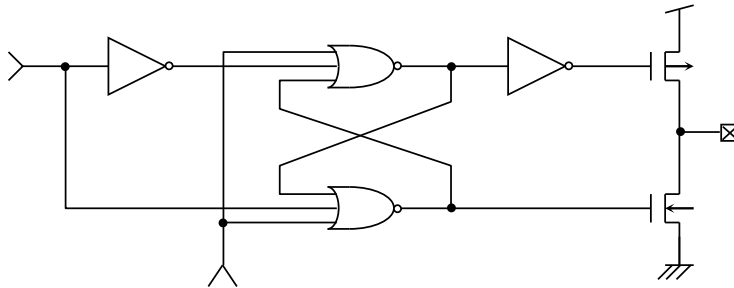


Figure 60. Output Equivalent Circuit (SO)

### Caution on Power-up Conditions

At power-up, as the  $V_{CC}$  rises, the IC's internal circuits may go through unstable low voltage area, making the IC's internal circuit not completely reset, hence, malfunction like miswriting and misread may occur. To prevent it, this IC is equipped with Power-on Reset circuit. In order to ensure its operation, at power-up, please observe the conditions below. In addition, set the power supply rise so that the supply voltage constantly increases from  $V_{BOT}$  to  $V_{CC}$  level. Furthermore,  $t_{INIT}$  is the time from the power become stable to the start of the first command input.

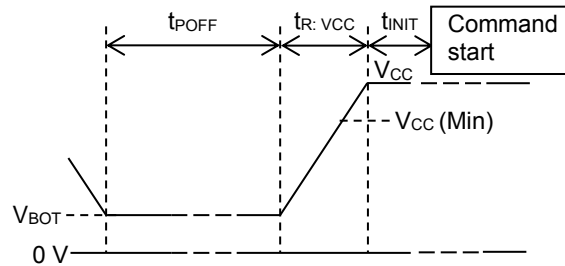


Figure 61. Rise Waveform Diagram

#### Power-Up Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage at Power OFF	$V_{BOT}$	-	-	0.3	V
Power OFF Time <sup>(Note 16)</sup>	$t_{POFF}$	1	-	-	ms
Initialize Time <sup>(Note 16)</sup>	$t_{INIT}$	0.1	-	-	ms
Supply Voltage Rising Time <sup>(Note 16)</sup>	$t_{R:VCC}$	0.001	-	100	ms

(Note 16) Not 100 % Tested.

At power ON/OFF, set CSB = High (=  $V_{CC}$ ).

When CSB is Low, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CSB = High. (When CSB is in High status, all inputs are canceled.)

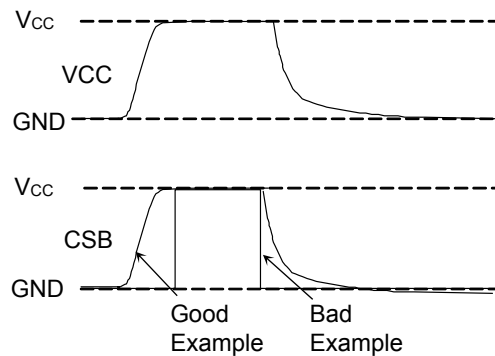


Figure 62. CSB Timing at power ON/OFF

(Good example) the CSB pin is pulled up to  $V_{CC}$ .

At power OFF, take 1 ms or higher before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

(Bad example) the CSB pin is Low at power ON/OFF.

In this case, CSB always becomes Low (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.

Even when CSB input is High-Z, the status becomes like this case, which please note.

### Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ = 1.2 V) or below, data rewrite is prevented.

## Noise Countermeasures

### 1. VCC Noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1  $\mu$ F) between IC VCC and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board VCC and GND.

### 2. SCK Noise

When the rise time ( $t_{RC}$ ) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2 V, if noises exist at SCK input, set the noise amplitude 0.2 V<sub>p-p</sub> or below. And it is recommended to set the rise time ( $t_{RC}$ ) of SCK 100 ns or below. In the case when the rise time is 100 ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

### 3. WPB Noise

During execution of Write Status Register command, if there exist noises on the WPB pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

## Operational Notes

### 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

### 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

### 5. Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

### 6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

### 7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

### 8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

### 9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

### 10. Regarding the Input Pin of the IC

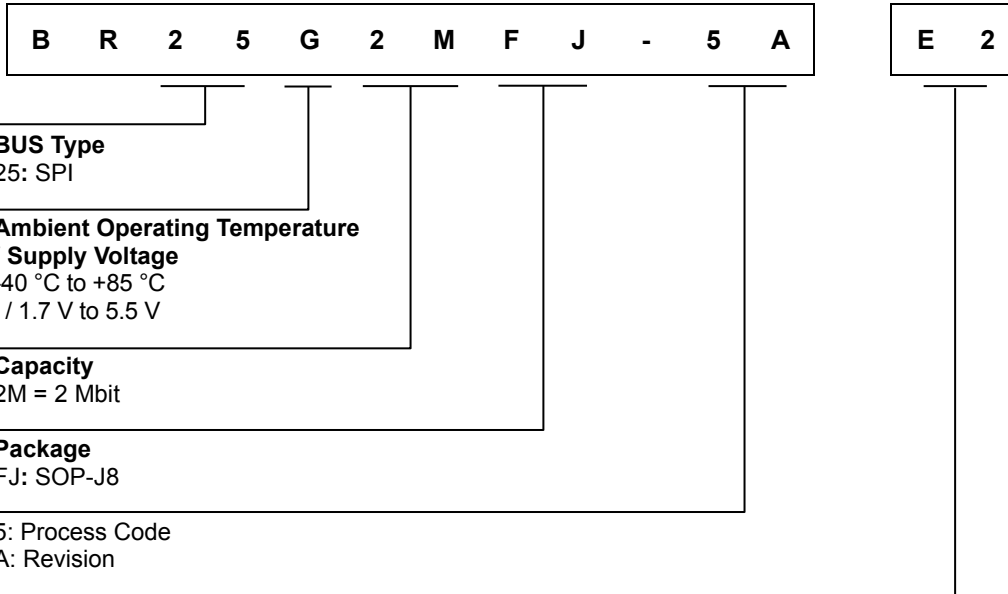
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

### 11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.



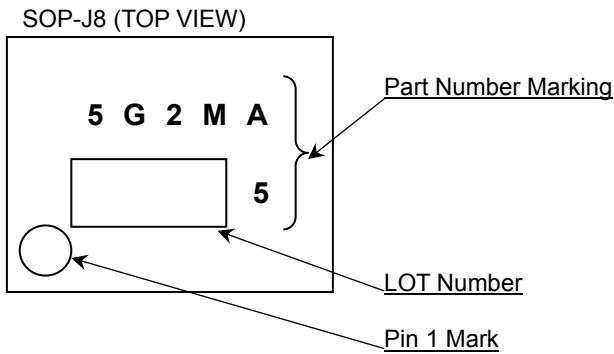
Ordering Information



Packaging and Forming Specification

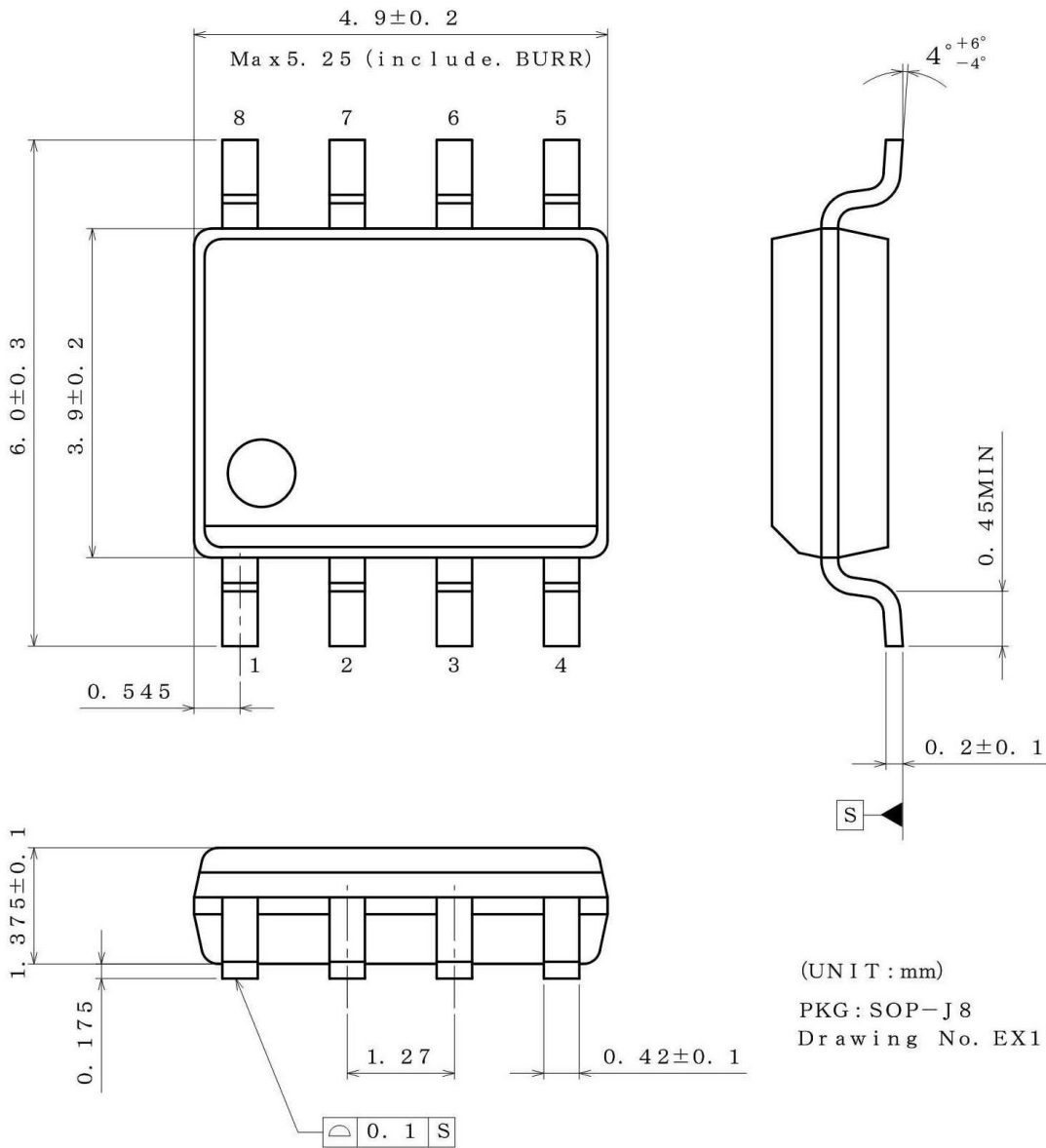
E2: Embossed tape and reel

Marking Diagram



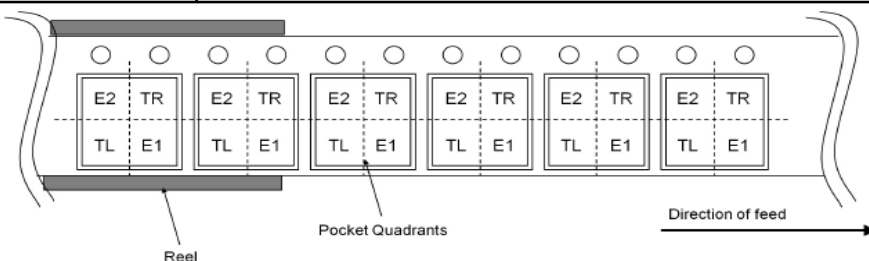
Physical Dimension and Packing Information

Package Name	SOP-J8
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< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



**Revision History**

Date	Revision	Changes
19.Mar.2024	001	New Release

# Notice

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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