28 V/5 A built-in FET

E-Fuse, 3 V-28 V, 5 A, 16 mΩ
BD58020GW

BD58020GW

General Description

BD58020GW is an Over Voltage, Over Current and Over Temperature Protection IC (OV, OC & OT Protection IC). BD58020GW has a built-in low ON-resistance 16 mΩ (Typ) Nch FET which immediately prevents damage to the downstream components, when fault condition occurs. The BD58020GW also has temperature protection function for 2 external NTC thermistors input which allows monitoring 2 different places in an application. The Over Voltage and Over Current level can be set by external resistors or internal fixed resistors.

Features

- Programmable Over Voltage Protection with External Resistors
- Programmable Over Current Limit with External Resistor
- Ultra-Fast Over Voltage Response Time: Typ 50 ns
- Built-in 16 mΩ NMOS FET
- Over Temperature Protection & 2 Different Thermal Monitor Support with NTC
- Programmable Brownout Detection
- Bi-directional I/O for Providing Temperature Fault Condition
- Active Discharge Support at VOUT
- Battery Mode Support
- USB On the Go (OTG) Support

Applications

- Smart Home Appliances
- Plug Adapter or Battery Applications
- Portable Device

Key Specifications

- Input Voltage Range: 3.0 V to 28 V (3.6 V for Start-up)
- BAT Voltage Range: 2.7 V to 5.5 V
- Max Continuous Current: 5.0 A (Typ)
- Nch FET ON Resistance: 16 mΩ (Typ)
- OVP Response Time: 50 ns (Typ)
- Quiescent Current: 128 µA (Typ), 200 µA (Max)
- Low Iq Mode / VBAT Current: 2.77 µA (Typ)
- Operating Junction Temperature:-40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
UCSP55M1C (16Pin)	1.7 mm x 1.7 mm x 0.62 mm 0.4 mm pitch 16-Balls

Typical Application Circuits

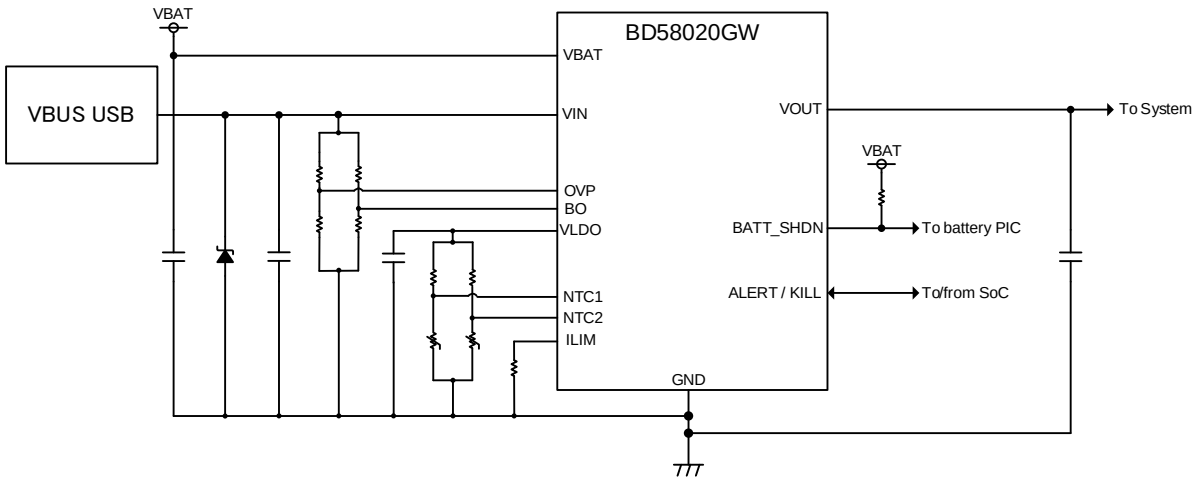


Figure 1. Typical Application Circuit

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

Pin Configuration

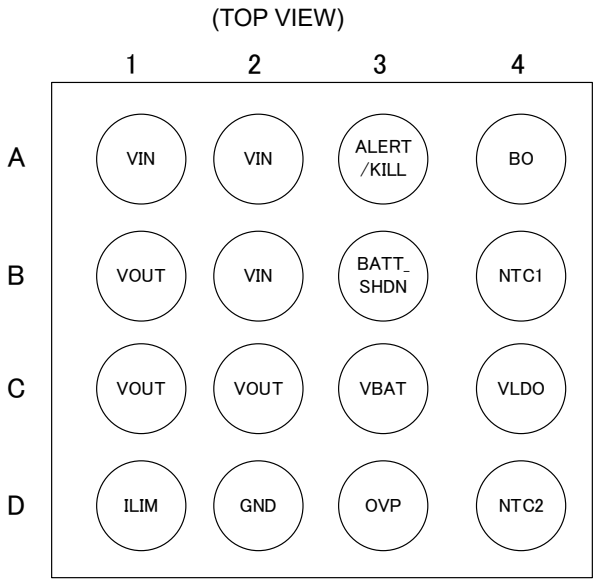


Figure 2. Pin Configuration (TOP VIEW)

Pin Descriptions

Ball No.	Pin Name	Function
A1, A2, B2	VIN	Dedicated power to protection IC.
A3	ALERT/KILL	ALERT (output): provides temp fault status. KILL (input): kill signal from SoC to shut off system power.
C3	VBAT	Input from battery.
B1, C1, C2	VOUT	Output of internal switch.
B3	BATT_SHDN	Open-drain output to disconnect battery pack from charger.
B4	NTC1	Input to NTC sensing comparator 1.
A4	BO	Input to brownout detection.
C4	VLDO	Voltage rail for NTC thermistor.
D1	ILIM	Pin to set OC limit threshold using an external resistor.
D2	GND	Ground pin.
D3	OVP	Input to over voltage protection circuit.
D4	NTC2	Input to NTC sensing comparator 2.

Block Diagram

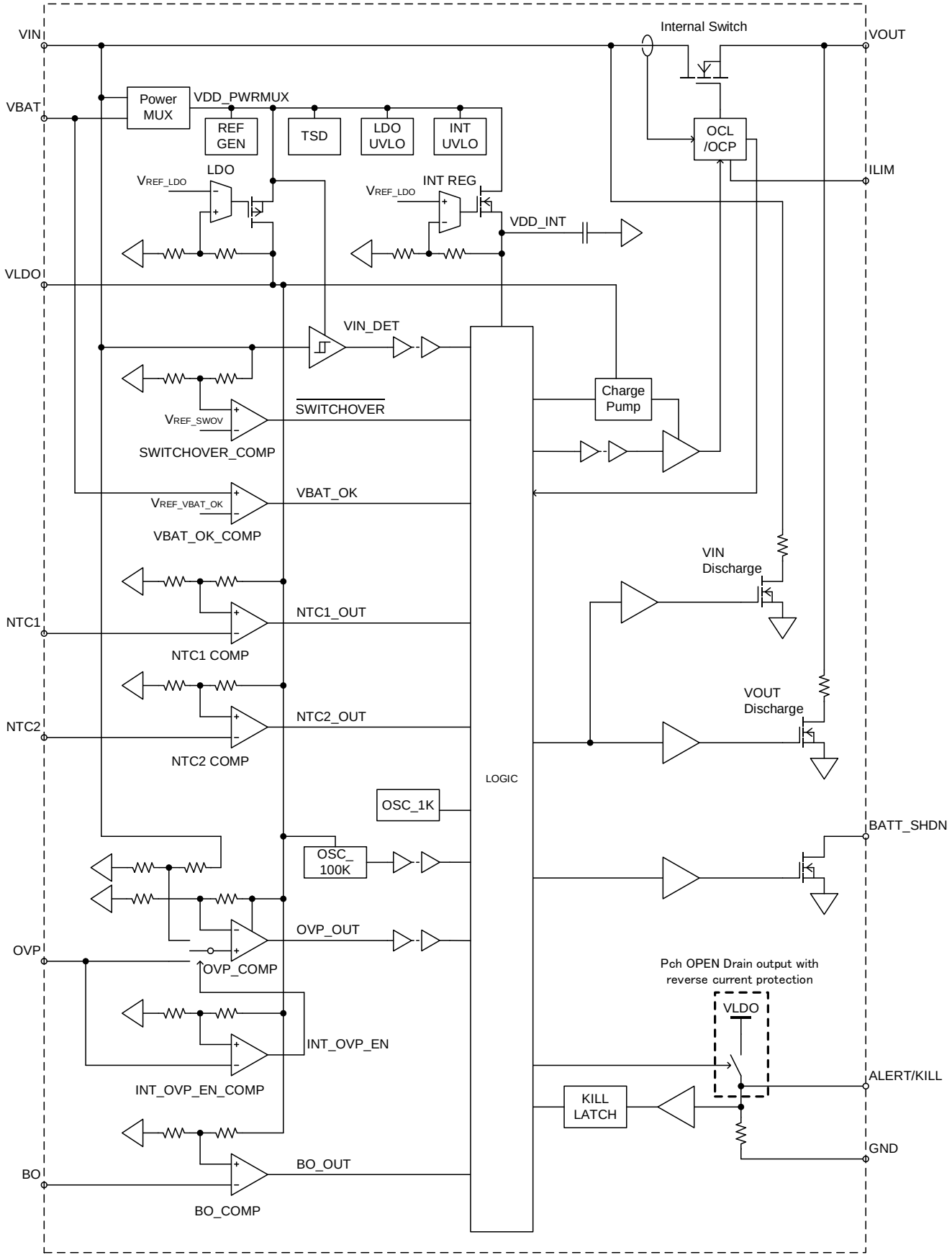


Figure 3. Block Diagram

Description of Blocks

Power MUX
The power multiplexer block. See Function Descriptions for details.

LDO
The LDO generates 1.8 V from Power MUX output, VDD_PWRMUX, to be supplied to thermistors and internal circuits.

LDO UVLO
UVLO circuit for LDO, which monitors the output voltage of LDO and turns off the switch when the output voltage drops.

INT REG
An internal regulator circuit that operates even when power is supplied from the VBAT to power the internal logic circuit.

INT UVLO
UVLO circuit for INT REG. The IC shuts down when INT REG falls below the minimum voltage required to operate the internal logic circuit.

REF GEN
The REF GEN generates the reference voltage for the LDO.

TSD
Thermal shutdown circuit to protect ASIC from internal over temperature.
When TSD event occurs, internal switch is turned OFF. Switch turns ON after temperature hysteresis is overcome.

VIN DET
The block detects that power is connected to VIN.
LDO turns on continuously when VIN DET is detected.

SWITCHOVER COMP
The comparator that detects a drop in VIN.
When VIN falls below $V_{SWITCHOVER}$, internal switch turns OFF and the power supply of the internal power supply switches from VIN to VBAT.

VBAT OK COMP
The comparator that detects VBAT voltage.
When the VBAT voltage exceeds $V_{REF\_VBAT\_OK}$, the multiplexer generates internal power supply voltages from VBAT. However, it gives priority to the logic of SWITCHOVER COMP.

NTC1 COMP / NTC2 COMP
The comparator that detects over temperature by comparing NTC1, NTC2 pin voltage with the reference voltage. When over temperature is detected, NTCX_OUT goes high.
See Function Descriptions for the operation when overtemperature is detected.

OVP COMP
The comparator that detects overvoltage of VIN by comparing the OVP pin voltage with the reference voltage.
When overvoltage is detected, OVP_OUT goes high.
See Function Descriptions for the operation when overvoltage detected.

INTERNAL OVP ENABLE COMP
The comparator detects that the OVP pin is shorted to GND and enables the Internal OVP.

BO COMP
The comparator that detects brownout by comparing BO pin voltage with the reference voltage.
When brownout is detected, BO_OUT goes high.
See Function Descriptions for the operation when brownout detected.

OSC_1K, OSC_100K
The oscillator for internal clock generation.

Description of Blocks – continued

Internal Switch
A low ON-resistance Nch MOSFET switch.
See Function Descriptions for the Logic of the Internal switch when the protection function is detected.

Charge Pump
The charge pump circuit that generates the gate voltage of the internal switch.

OCL / OCP
The overcurrent limit and overcurrent protection block.
Controls the current flowing through the internal switch so that it does not exceed the overcurrent threshold.
See Function Descriptions for details.

VOUT Discharge, VIN Discharge
Internal resistive discharge path from VOUT to GND when internal switch is turned OFF for all fault conditions except OVP. At the same time, VIN pin is also pulled down at 10 kΩ.

BATT_SHDN
The open drain output pin to output the shutdown signal to the battery.

ALERT/KILL
I/O pin for ALERT signal output and KILL signal input. This pin is equipped with the reverse protection as indicated in the block diagram.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
VBAT Pin Voltage	V_{VBAT}	-0.3 to +7.0	V
VIN Pin Voltage	V_{VIN}	-0.3 to +30	V
VOUT Pin Voltage	V_{OUT}	-0.3 to +30	V
ALERT/KILL Pin Voltage	V_{ALERT}	-0.3 to +4.5	V
OVP Pin Voltage	V_{OVP}	-0.3 to +2.2	V
BATT_SHDN Pin Voltage	V_{BATT_SHDN}	-0.3 to +7.0	V
BO Pin Voltage	V_{BO}	-0.3 to +2.2	V
VLDO Pin Voltage	V_{LDO}	-0.3 to +4.5	V
NTC1 Pin Voltage	V_{NTC1}	-0.3 to +4.5	V
NTC2 Pin Voltage	V_{NTC2}	-0.3 to +2.2	V
ILIM Pin Voltage	V_{ILIM}	-0.3 to +2.2	V
VOUT to VIN Current at OFF	I_{OUT_OFF}	0.500	A
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

ESD Ratings

Parameter	Value	Unit
Human-body model (HBM)	±2000	V
Charged-device model (CDM)	±500	V

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 3)*	
UCSP55M1C				
Junction to Ambient	θ_{JA}	178.5	75.8	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	9.0	8.0	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-9.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.5 mm x 101.5 mm x 1.6 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.5 mm x 101.5 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	99.5 mm x 99.5 mm	35 µm	99.5 mm x 99.5 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating Junction Temperature	Topr	-40	+25	+125	°C	
VIN Pin Voltage	V_{VIN}	3.0	-	28	V	3.6 V for Start-up
VBAT Pin Voltage	V_{VBAT}	2.7	-	5.5	V	
VLDO Capacitor *(Note 4)*	C_{LDO}	0.10	0.22	0.70	µF	Ta = 0 °C to +125 °C
		0.19	0.47	0.70	µF	Ta = -40 °C to +125 °C
VIN Capacitor *(Note 4)*	C_{VIN}	0.10	-	-	µF	
VOUT Capacitor *(Note 4)*	C_{VOUT}	0.10	-	2200	µF	
BATT_SHDN Pin Voltage	V_{BATT_SHDN}	0	-	5.5	V	
ALERT/KILL Pin Voltage	V_{ALERT}	0	-	3.6	V	
BO Pin Voltage	V_{BO}	0	-	V_{LDO}	V	
OVP Pin Voltage	V_{OVP}	0	-	V_{LDO}	V	
NTC1 Pin Voltage	V_{NTC1}	0	-	3.6	V	
NTC2 Pin Voltage*(Note 5)*	V_{NTC2}	0	-	V_{LDO}	V	
ILIM Pin Voltage	V_{ILIM}	0	-	V_{LDO}	V	

(Note 4) Ceramic capacitor is recommended. The capacitor value including temperature change, DC bias change, and aging change must be considered.
(Note 5) NTC2 has lower operational max voltage as there is a internal diode at the pin toward VLDO for test purpose. That is the reason why NTC2 has lower operational max compared to NTC1.

Electrical Characteristics (Unless otherwise specified V_{VIN} = 5.0 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power Supply Inputs						
VIN Consumption Current 1	I_{q_VIN1}	-	128	200	µA	VIN = 5.0 V
VIN Consumption Current 2	I_{q_VIN2}	-	138	200	µA	VIN = 24 V
VBAT Consumption Current 1	I_{q_VBAT1}	-	2.77	3.90	µA	VBAT = 5.0 V, VIN = 0 V, C_{LDO} = 0.22 µF, , VLDO 50 kΩ pull down, D_{NTC} = 0.20 % (Typ), 0.25 % (Max), Ta = 25 °C
		-	2.77	4.40	µA	Ta = -40 °C to +50 °C
VBAT Consumption Current 2	I_{q_VBAT2}	-	19	-	µA	VBAT = 5.0 V, VIN = 0 V, During T_NTC_ON, VLDO: no load
VBAT Consumption Current 3	I_{q_VBAT3}	-	2.5	-	µA	VBAT = 5.0 V, VIN = 0 V, During T_NTC_OFF, VLDO: no load
VBAT Consumption Current 4	I_{q_VBAT4}	-	1	-	µA	VBAT = 5 V, VIN = 5 V, VLDO: no load VIN > $V_{SWITCHOVER}$
Power MUX Switchover Threshold	$V_{SWITCHOVER}$	2.870	3.000	3.130	V	VIN sweep down
Power MUX Switchover Release Threshold	$V_{SWITCHOVER\_REL}$	3.450	3.600	3.750	V	VIN sweep up
VBAT OK Threshold	V_{VBAT_OK}	2.400	2.500	2.600	V	VBAT sweep up
VBAT OK Release Threshold	$V_{VBAT\_OK\_REL}$	2.067	2.167	2.267	V	VBAT sweep down
Internal Switch						
Internal Switch ON Resistance	R_{DSON}	-	16	24	mΩ	At nominal supply voltage output for USB (VIN = 5 V)
Internal Switch Current	I_{SW}	5.0	-	-	A	Continuous current
SOFTSTART Slew Rate	SR_{SS}	0.128	0.160	0.192	V/ms	
Inrush Current	I_{INRUSH}	-	-	200	mA	Peak current while VOUT ramps up to VIN (24 V), COUT = 1000 µF
VIN Discharge Resistance	R_{DIS_VIN}	7	10	13	kΩ	VIN = 5.0 V
VOUT Discharge Resistance	R_{DIS_VOUT}	200	300	400	Ω	VOUT = 2.0 V
LDO						
LDO Output Voltage	V_{LDO}	1.773	1.800	1.827	V	
LDO Current Capability	I_{LDO}	2.0	-	-	mA	
LDO UVLO Threshold	V_{LDO_UVLO}	1.623	1.674	1.724	V	VLDO sweep down
LDO UVLO Hysteresis	V_{LDO_HYS}	36	54	72	mV	

Electrical Characteristics (Unless otherwise specified V_{VIN} = 5.0 V, Ta = 25 °C) – continued

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VREF						
VREF THERM	V_{REF_THERM}	0.873	0.900	0.927	V	NTC1 / NTC2 sweep down
VREF THERM Release	$V_{REF\_THERM\_REL}$	1.240	1.280	1.320	V	
Ratio of V_{REF_THERM} to V_{LDO}	α_{TRIP}	0.4925	0.5000	0.5075	V/V	V_{REF_THERM} / V_{LDO}
Ratio of V $V_{REF\_THERM\_REL}$ to V_{LDO}	α_{TRIP_REL}	0.7001	0.7111	0.7221	V/V	$V_{REF\_THERM\_REL}$ / V_{LDO}
Over Temperature Trip Point Accuracy	T_{TRIP}	-1	-	+1	°C	THERM : NCP15WF104F03RC, Excluding R_{BIAS} and NCP15WF104F03RC error, Ta > 50 °C
VREF OVP	V_{REF_OVP}	1.164	1.200	1.236	V	OVP sweep up
VREF OVP Hysteresis	$V_{REF\_OVP\_HYS}$	-	100	-	mV	
VREF BO	V_{REF_BO}	1.164	1.200	1.236	V	BO sweep down
VREF BO Hysteresis	$V_{REF\_BO\_HYS}$	-	100	-	mV	
OVP						
Internal OVP Enable Threshold	$V_{OVP\_INT\_EN}$	120	160	200	mV	OVP sweep down
Internal OVP Enable Threshold Hysteresis	$V_{OVP\_INT\_EN\_HYS}$	-	40	-	mV	
Internal OVP Threshold	V_{OVP_INT}	5.82	6.00	6.18	V	VIN sweep up
Internal OVP Threshold Hysteresis	$V_{OVP\_INT\_HYS}$	-	200	-	mV	
OVP Pin Capacitance	C_{OVP}	-	-	10	pF	
Over Current Limit						
OCL Setting 1	I_{OCL1}	0.178	0.214	0.251	A	R_{ILIM} = 13 kΩ
OCL Setting 2	I_{OCL2}	0.443	0.515	0.588	A	R_{ILIM} = 4.7 kΩ
OCL Setting 3	I_{OCL3}	0.843	0.958	1.073	A	R_{ILIM} = 2.4 kΩ
OCL Setting 4	I_{OCL4}	1.50	1.66	1.83	A	R_{ILIM} = 1.3 kΩ
OCL Setting 5	I_{OCL5}	1.94	2.09	2.24	A	R_{ILIM} = 1.0 kΩ
TSD						
TSD Detect Temperature	T_{TSDH}	-	150	-	°C	
TSD Release Temperature	T_{TSDL}	-	125	-	°C	
I/O						
BATT_SHDN Pulldown Resistor	R_{SHDN}	-	20	30	Ω	BATT_SHDN = 50 µA
ALERT/KILL Pulldown Resistor	R_{ALERT}	100	150	200	kΩ	ALERT/KILL = 1 V
ALERT Output High Level	V_{ALERT_H}	V_{LDO}-0.2	-	V_{LDO}	V	
KILL Input High Level	V_{KILL_H}	1.26	-	3.60	V	
KILL Input Low Level	V_{KILL_L}	-0.30	-	+0.54	V	
Output Logic Timing						
Wait Delay Time	t_{DELAY_WAIT}	20.7	23.7	26.8	ms	
ALERT Delay Time	t_{DELAY_ALERT}	400	500	600	ms	
KILL Delay Time	t_{DELAY_KILL}	0.8	1.0	1.2	s	
OCL Debounce Time	t_{OCL_BLNK}	80	100	120	ms	
OCL Release Time	t_{OCL_REL}	80	100	120	ms	
OCP Recovery Time	t_{OCP_REC}	200	250	300	ms	
OVP Delay Time	t_{DELAY_OVP}	-	50	100	ns	
OVP Recovery Time	$t_{DELAY\_OVP\_REC}$	24	30	36	ms	
BROWNOUT Recovery Time	$t_{DELAY\_BO\_REC}$	400	500	600	ms	
NTC Sampling Interval Time	t_{NTC_SAMPLE}	2.36	2.62	2.88	s	
Duty Cycle for NTC Sampling	D_{NTC}	-	0.20	0.25	%	

Typical Performance Curves

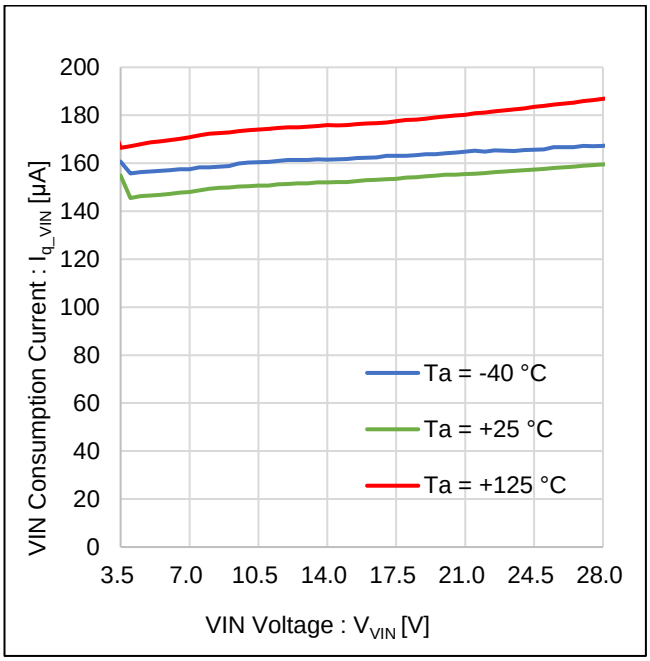


Figure 4. VIN Consumption Current vs VIN Voltage

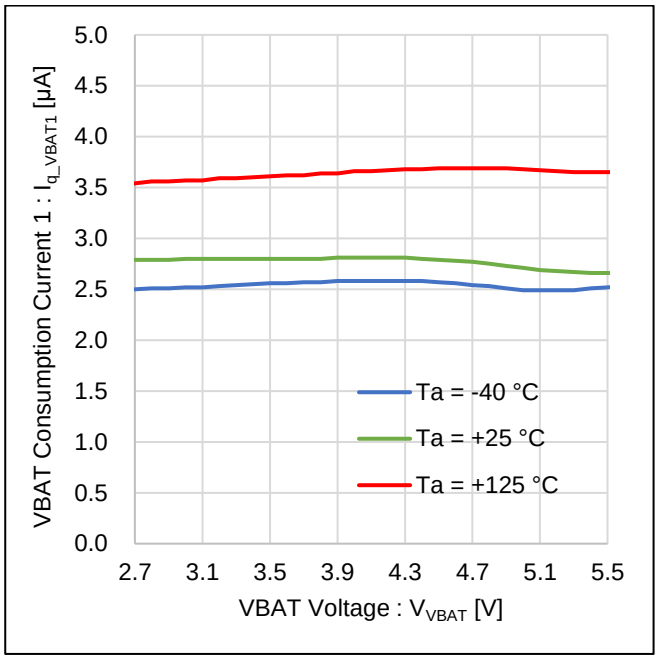


Figure 5. VBAT Consumption Current 1 vs VBAT Voltage

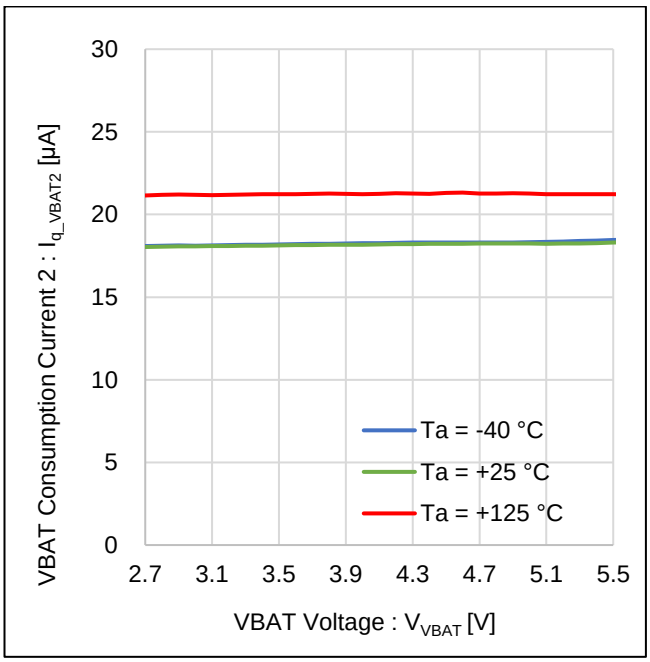


Figure 6. VBAT Consumption Current 2 vs VBAT Voltage

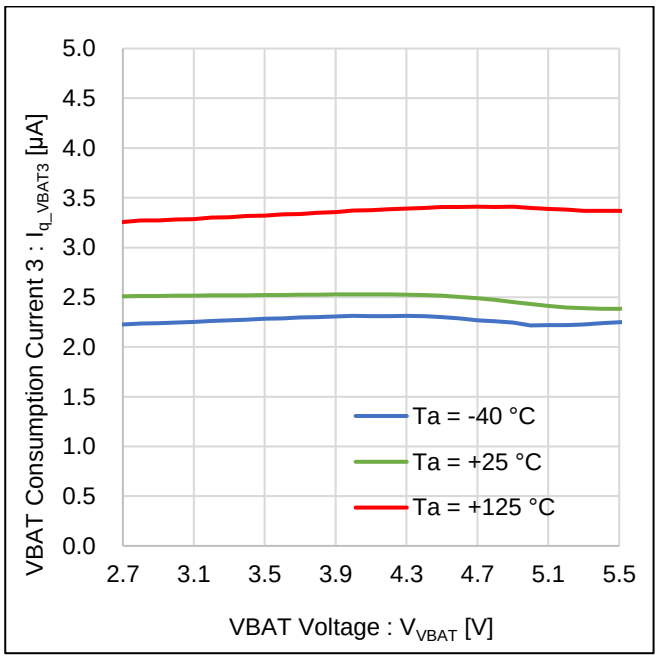


Figure 7. VBAT Consumption Current 3 vs VBAT Voltage

Typical Performance Curves - continued

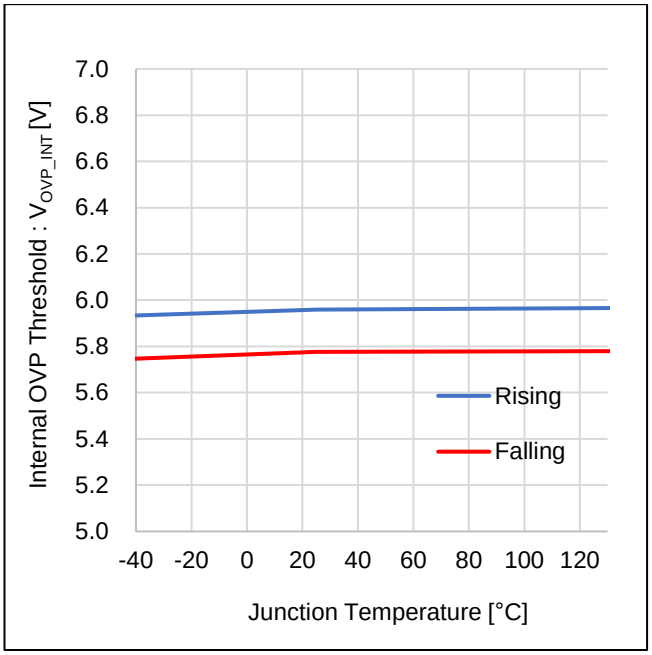


Figure 8. Internal OVP Threshold vs Temperature

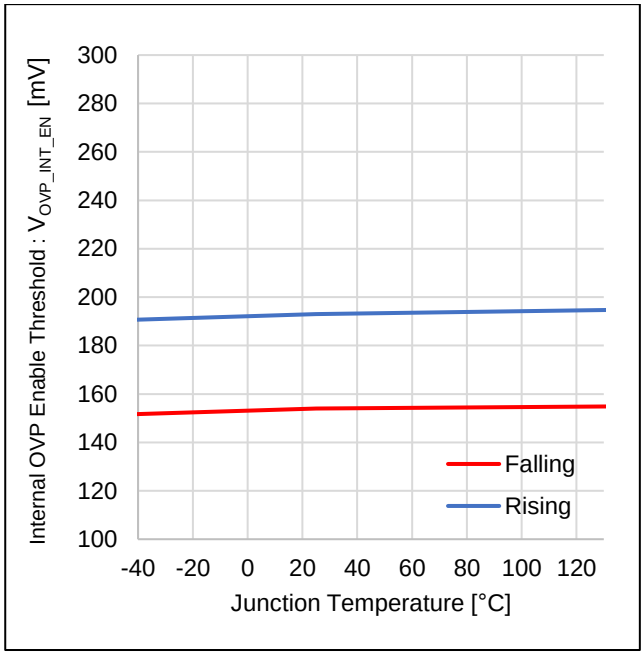


Figure 9. Internal OVP Enable Threshold vs Temperature

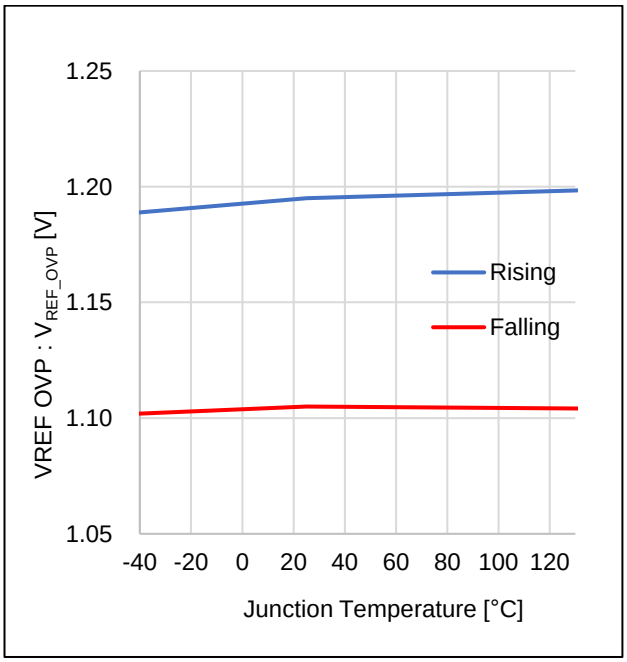


Figure 10. VREF OVP vs Temperature

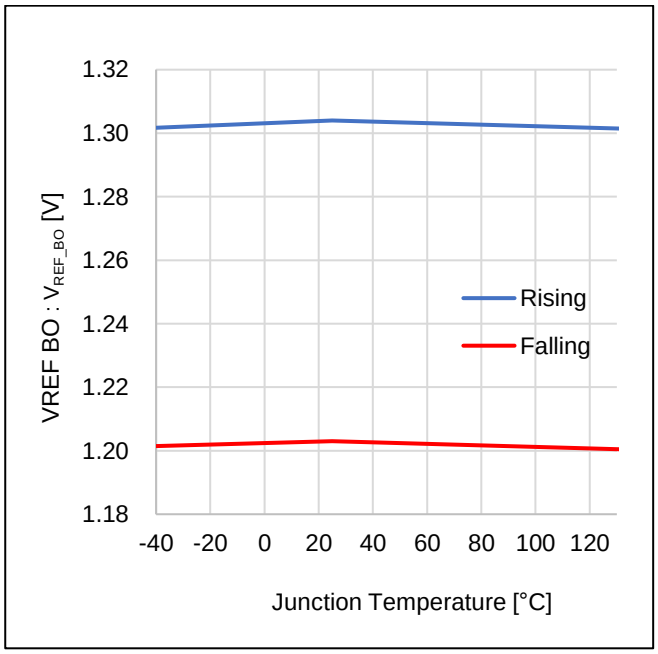


Figure 11. VREF BO vs Temperature

Typical Performance Curves - continued

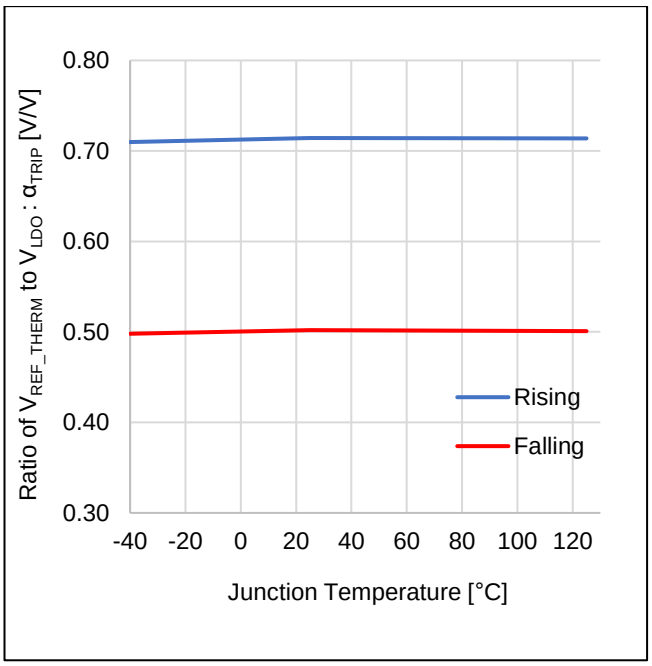


Figure 12. α_{TRIP} (V_{REF_THERM} / V_{LDO}) vs Temperature

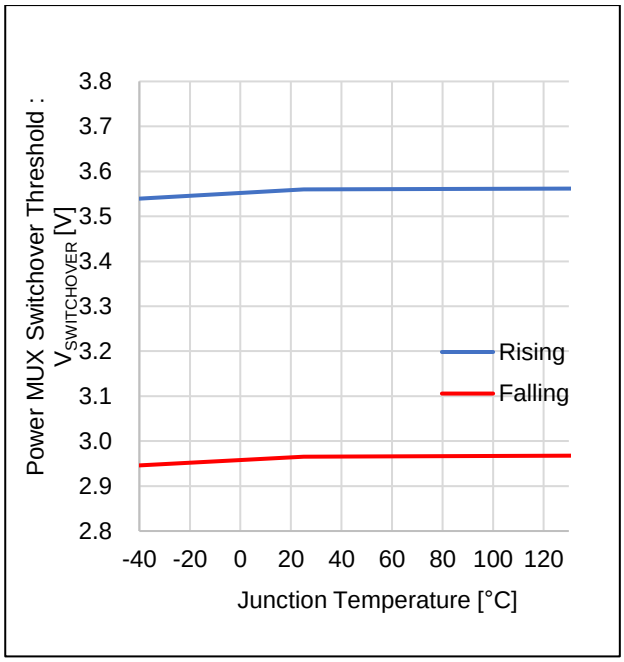


Figure 13. Power MUX Switchover Threshold vs Temperature

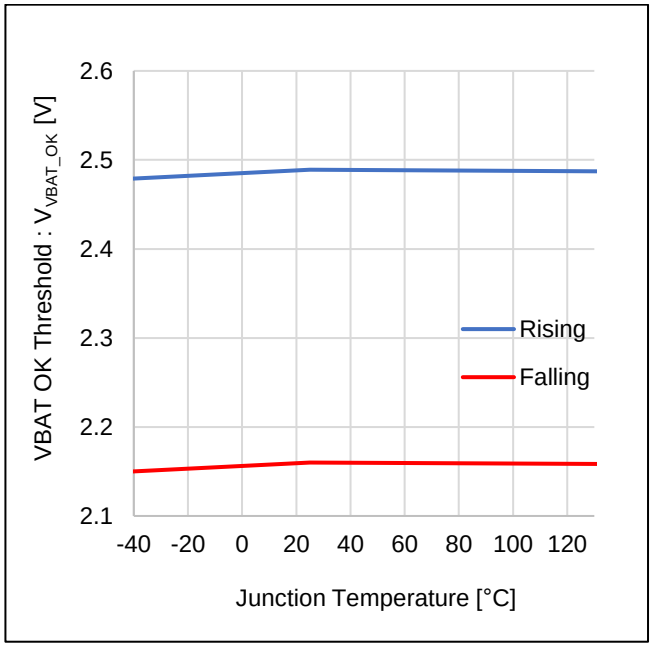


Figure 14. VBAT OK Threshold vs Temperature

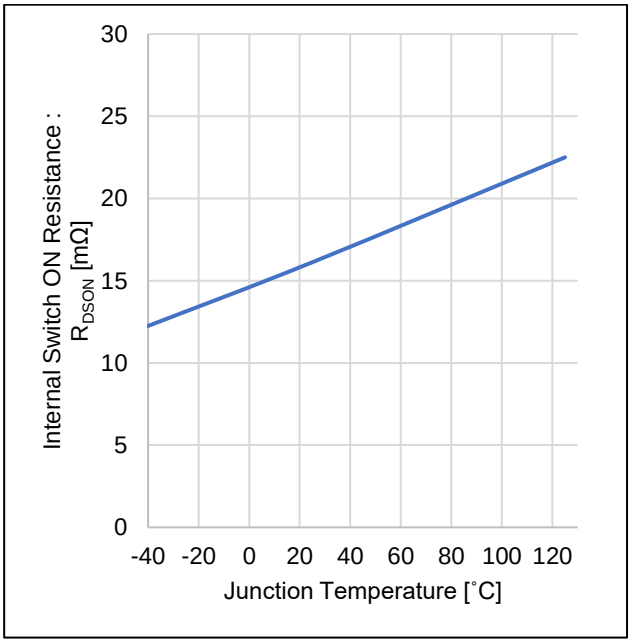


Figure 15. Internal Switch ON Resistance vs Temperature

Typical Performance Curves - continued

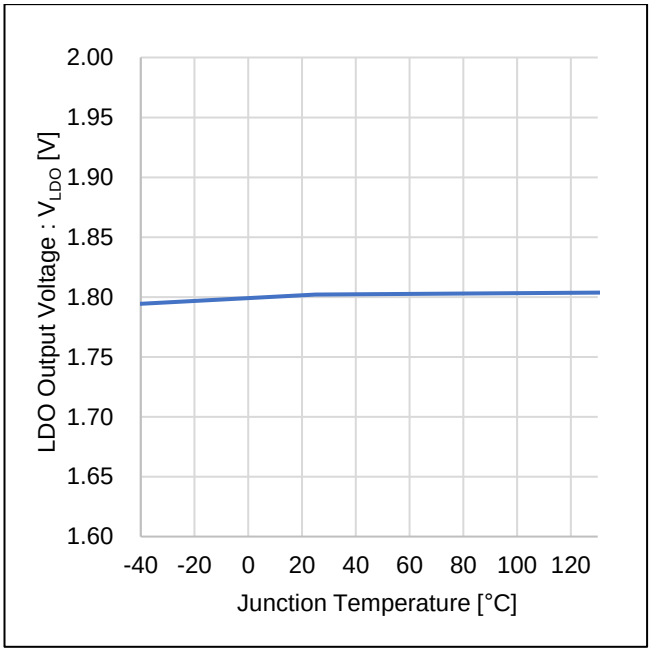


Figure 16. LDO Output Voltage vs Temperature

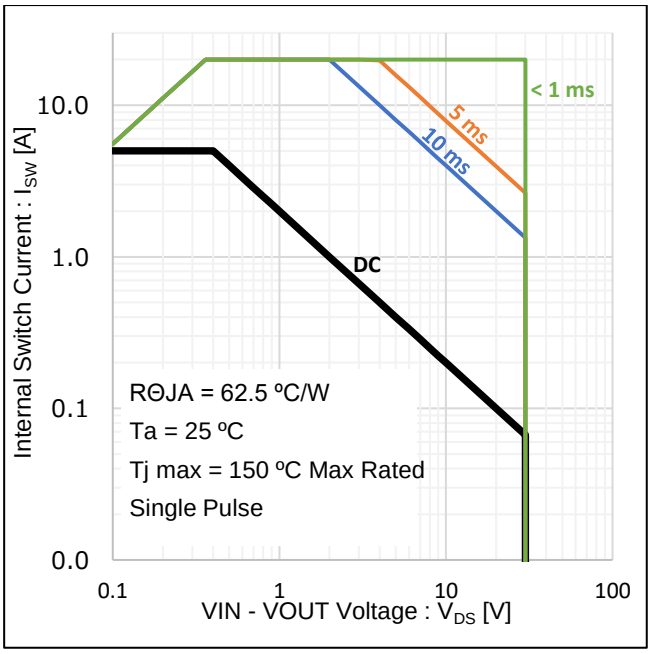


Figure 17. Safe Operation Area (SOA)

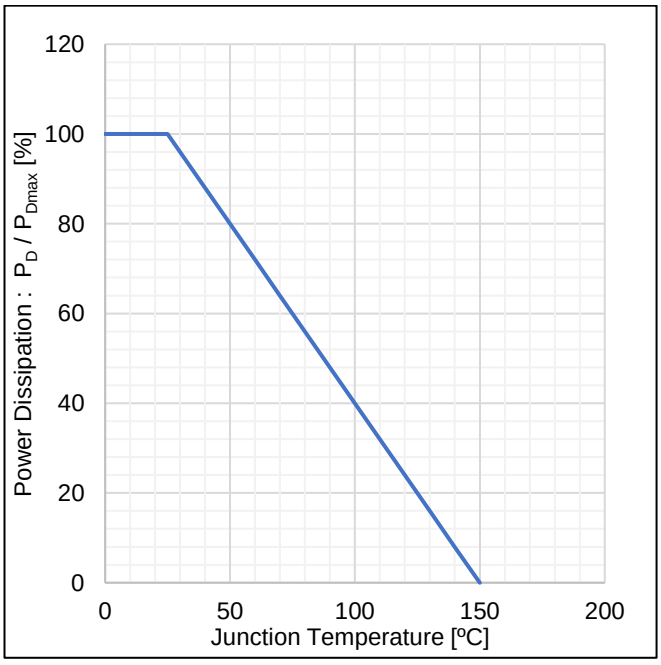


Figure 18. Derating Curve for SOA

Typical Performance Curves - continued

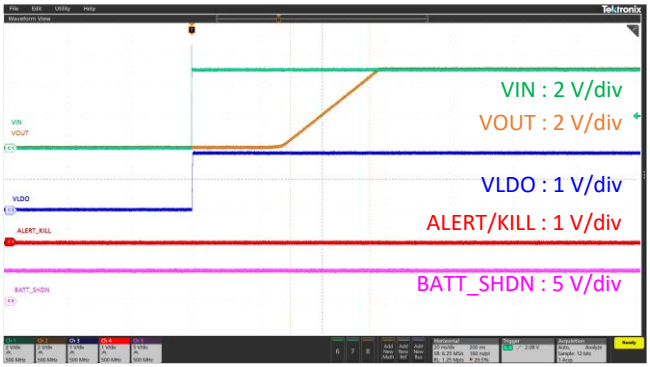


Figure 19. Start Up through VIN

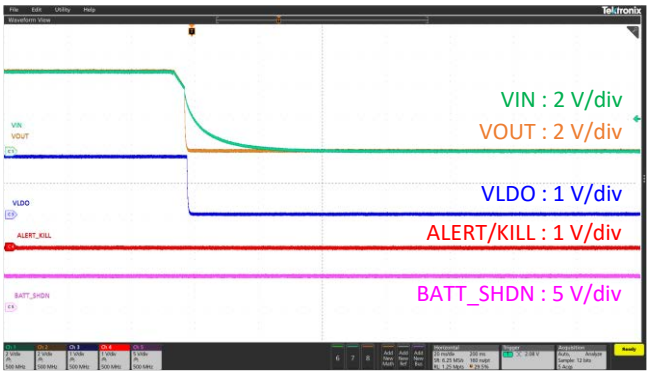


Figure 20. Shutdown through VIN

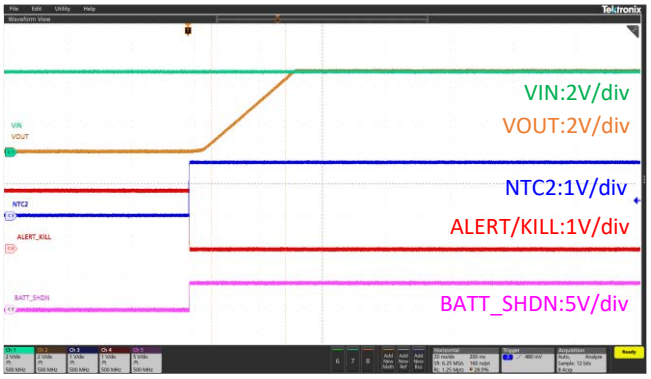


Figure 21. Start Up through NTC Pin

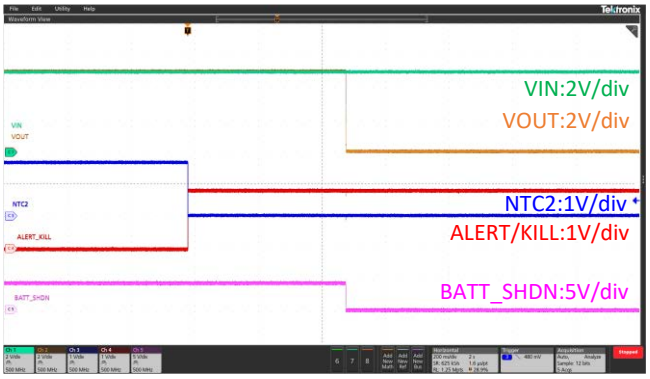


Figure 22. Shutdown through NTC Pin

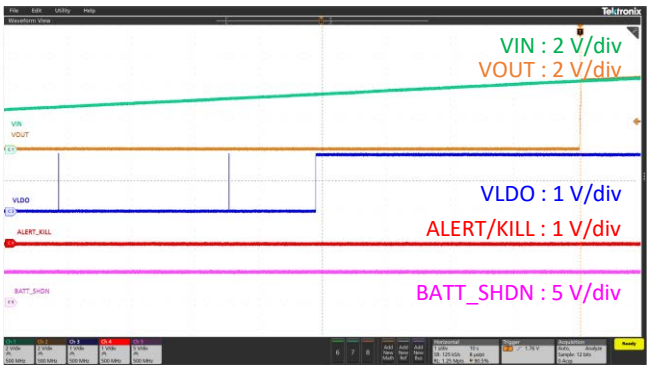


Figure 23. PWR_MUX Switchover Function
(VIN sweep up, VBAT = 4.2 V)

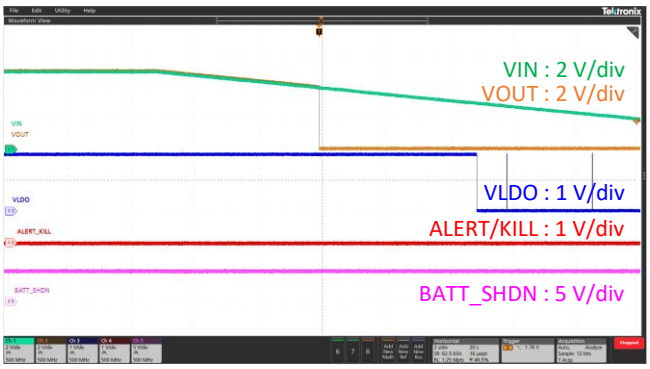


Figure 24. PWR_MUX Switchover Function
(VIN sweep down, VBAT = 4.2 V)

Typical Performance Curves - continued

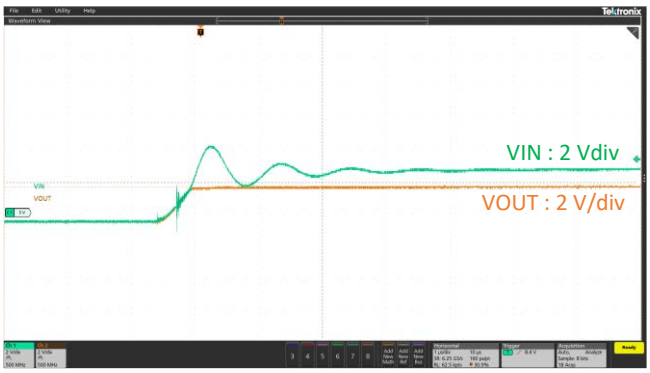


Figure 25. OVP Response (OVP Pin = GND)

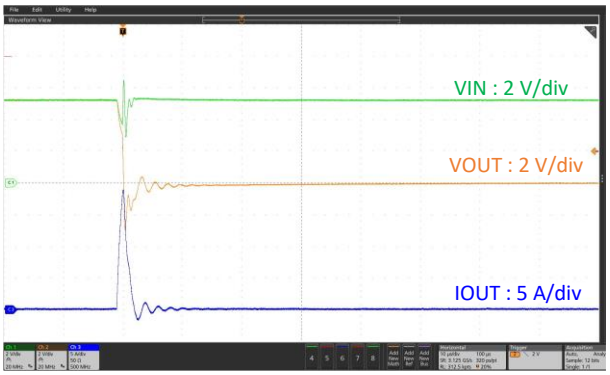


Figure 26. Short Circuit Protection Response

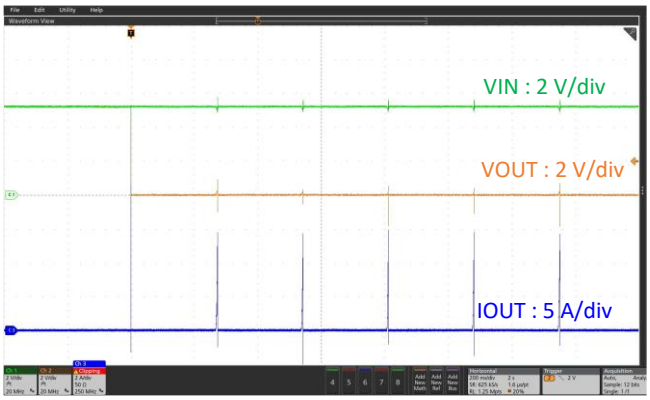


Figure 27. Short Circuit Protection Response (Zoom out)

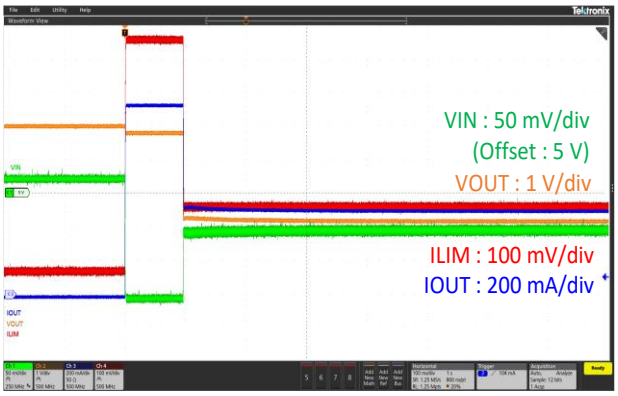


Figure 28. OCL Function (OCL = 500 mA Setting)

State Transition Diagram

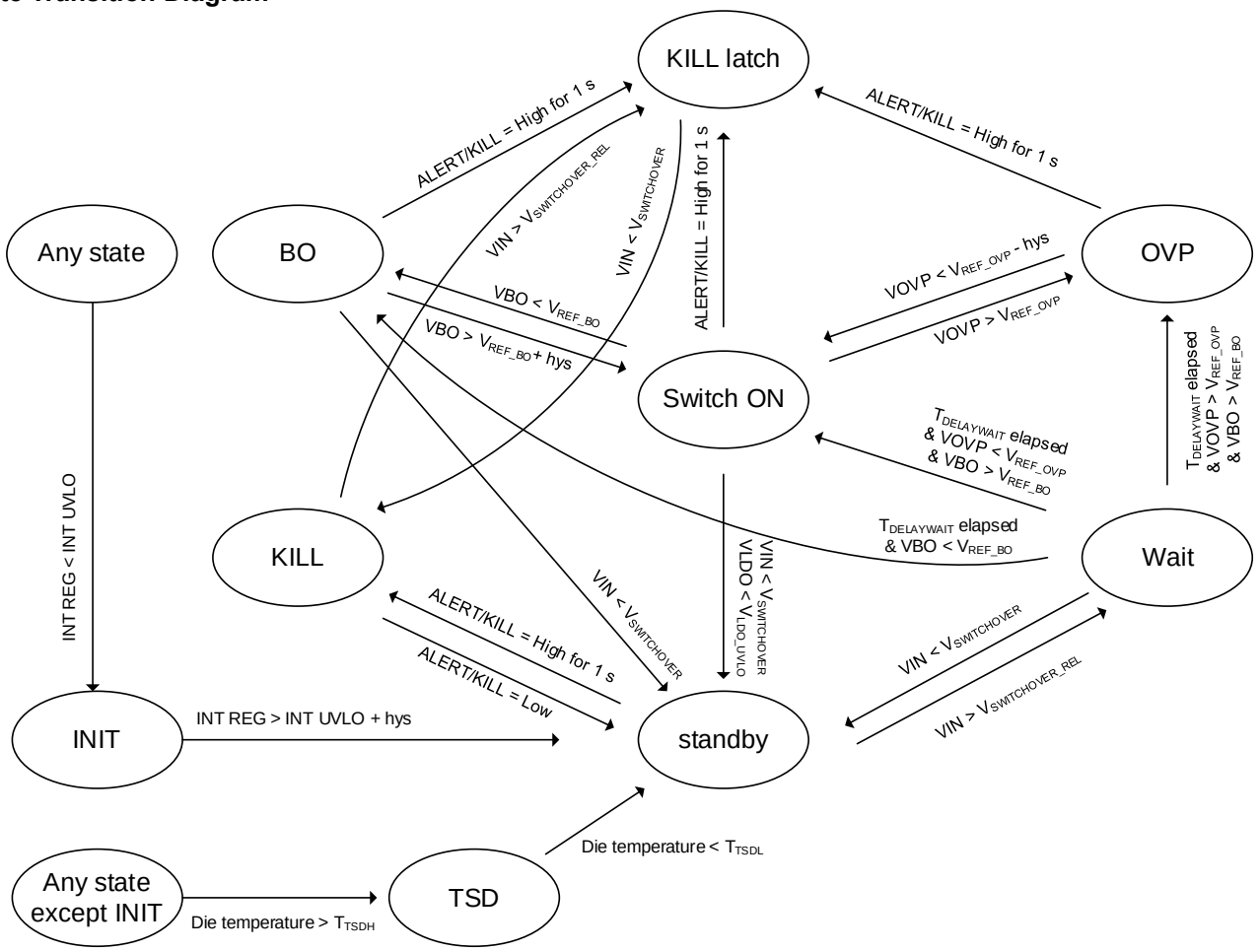


Figure 29. State Transition Diagram

Table 1. Outputs in Each State

	INIT	standby	KILL	Wait	Switch ON	BO	OVP	KILL latch	Over Temp	TSD
LDO	ON(UVLO)	Burst	ON	ON	ON	ON	ON	ON	ON	OFF
Internal Switch	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
VIN Discharge	OFF	ON	ON	ON	OFF	ON	OFF	ON	ON	OFF
VOUT Discharge	OFF	ON	ON	ON	OFF	ON	OFF	ON	ON	OFF
BATT_SHDN	HiZ	HiZ	Hiz	HiZ	HiZ	HiZ	HiZ	L	L	HiZ
ALERT/KILL	HiZ	L	-	L	L	L	L	-	H	L
Over Temp Sense	OFF	ON	ON	OFF	ON	ON	ON	ON	ON	OFF

When NTCx (x = 1, 2) < V_{REF_THERM}, the Over Temp state will be overlapped. When the Over Temp state is overlapped, the Over Temp state takes priority over the outputs. When NTCx > $V_{REF\_THERM\_REL}$, the Over Temp state is released, and the state return to the original state.

During the Wait state, hysteresis of comparators for OVP, BO and Over Temp detection are disabled, those of thresholds are fixed V_{REF_OVP}, V_{REF_BO}, and V_{REF_THERM}. Also, ALERT/KILL is fixed at Low. And delay time of $t_{DELAY\_OVP\_REC}$, $t_{DELAY\_BO\_REC}$, and t_{DELAY_ALERT} is eliminated and immediate response.

Startup and Shutdown Sequence

The startup and shutdown sequence are shown in the figure below. When VIN voltage exceeds the threshold of $V_{SWITCHOVER\_REL}$, the transition to the Wait state duration of t_{DELAY_WAIT}. During the Wait state, hysteresis of comparators for OVP, BO and Over Temp detection are disabled, those of thresholds are fixed V_{REF_OVP}, V_{REF_BO}, and V_{REF_THERM}. And delay time of $t_{DELAY\_OVP\_REC}$, $t_{DELAY\_BO\_REC}$ and t_{DELAY_ALERT} is eliminated and immediate response. After t_{DELAY_WAIT}, VOUT ramps up if the following conditions.

OVP < V_{REF_OVP} & BO > V_{REF_BO} & NTC1, NTC2 > V_{REF_THERM}

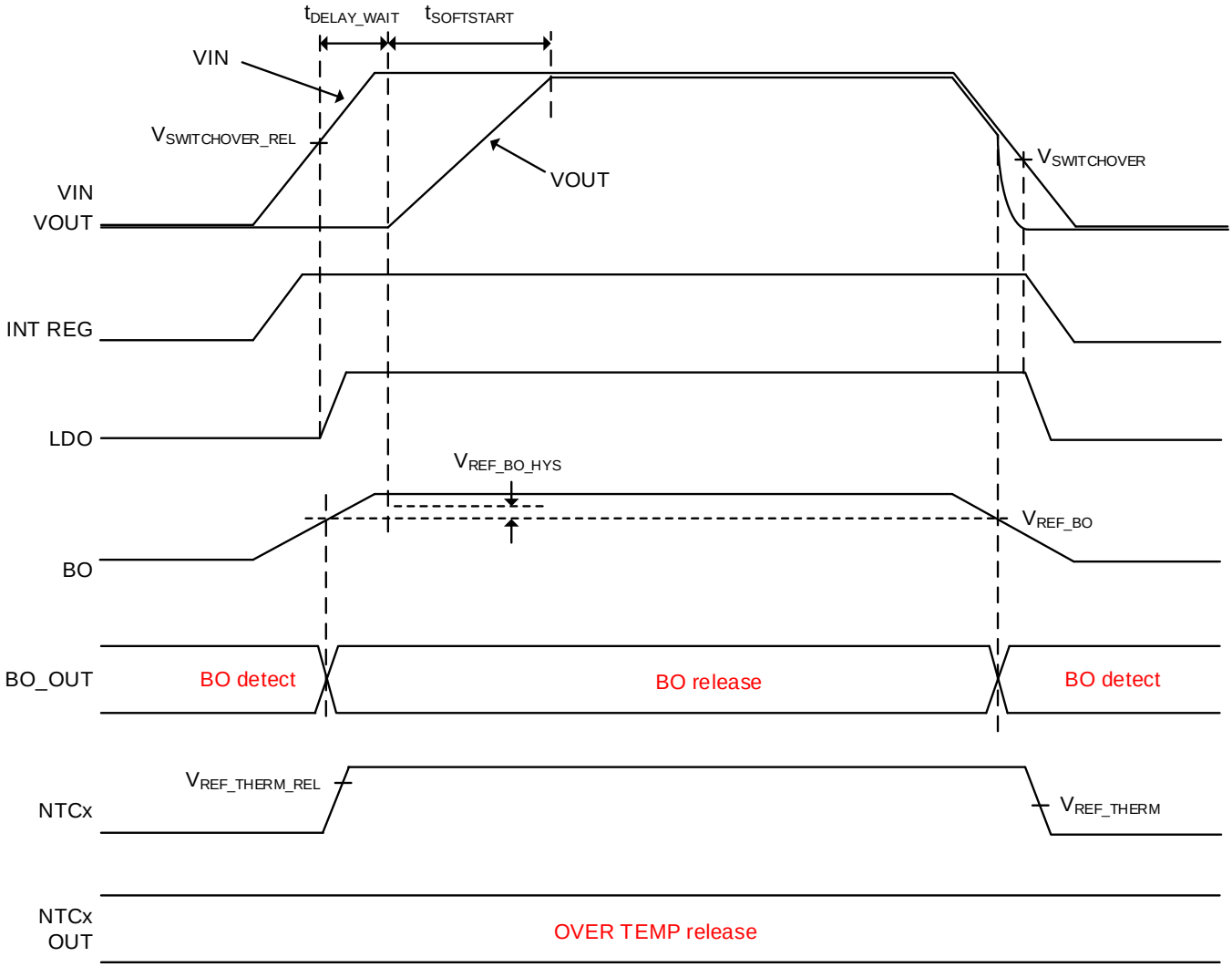


Figure 30. Startup and shutdown sequence when VIN only supplied

Function Descriptions

LDO UVLO

LDO UVLO is built-in to prevent the IC from malfunctioning when the output voltage of LDO is low. When LDO UVLO is detected, Internal Switch turns OFF and all protection functions are stopped. It is necessary to input the following voltage to VIN and VBAT to release LDO UVLO because the voltage drops between VIN and VLDO, and between VBAT and VLDO.

VIN > 3.6 V or VBAT > 2.5 V

Once LDO UVLO is released, the dropout voltage between VIN and VLDO is suppressed, and then IC can be operated down to the following voltages.

VIN > 3.0 V or VBAT > 2.5 V

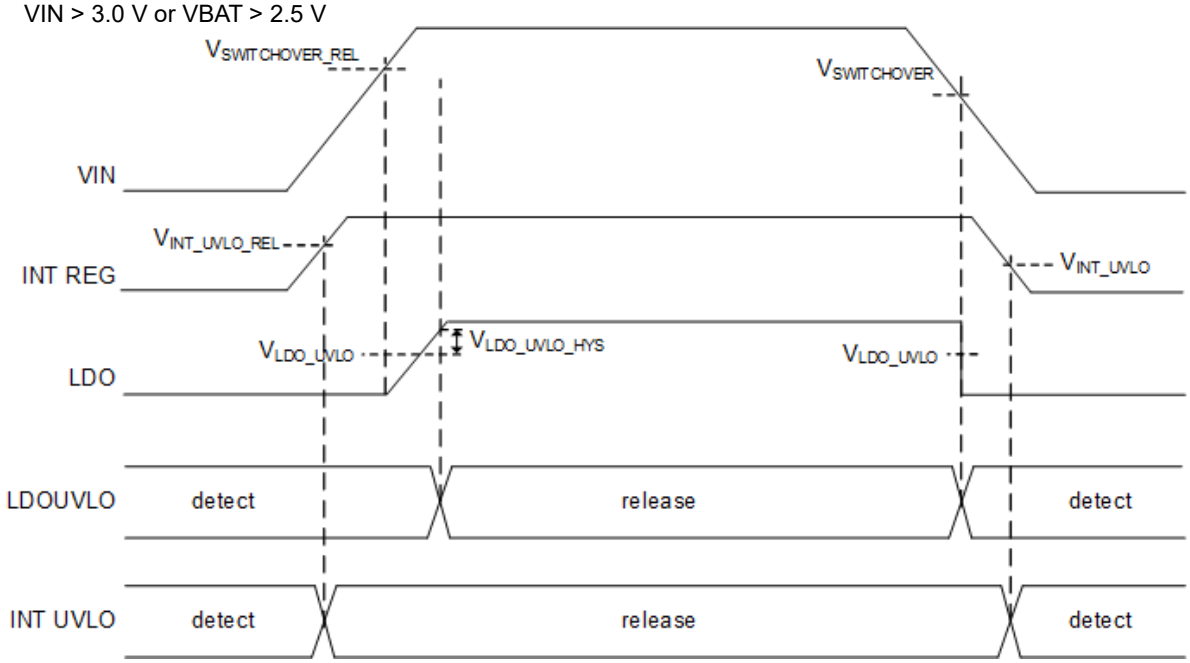


Figure 31. LDO UVLO Detection, Release Condition

Burst Operation LDO

While power is supplied from the VBAT, the LDO operates intermittently (burst operation) to reduce the current consumption of the VBAT. The LDO is on once every 2.62 s for about 5 ms. But when over temperature is detected, it keeps on until the over temperature is released. Also, over Temperature detection is masked for about 2.5 ms after LDO UVLO is released, and after the masking time, transition to the Over Temp state.

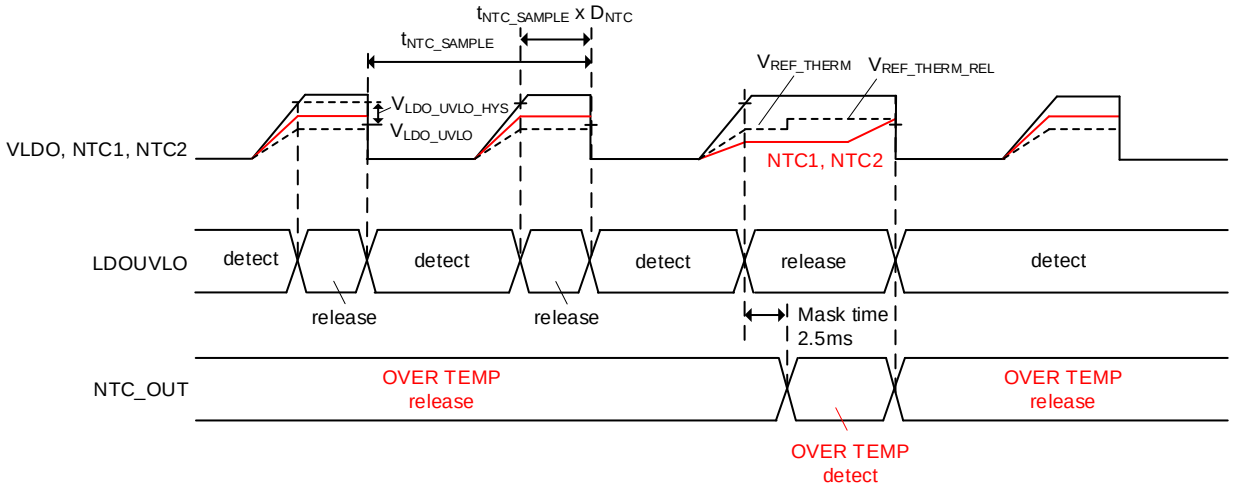


Figure 32. Timing Chart of Burst Operation LDO (When VBAT only supplied)

Function Descriptions - continued

Soft Start

The soft start function suppresses the inrush current. The soft start function is activated every time when the device returns from each protection function.

Over Temperature Protection

The over temperature can be detected by connecting the point where the voltage between the LDO output and GND is divided by a resistor and NTC thermistor to the NTCx pin. When the NTC voltage falls below V_{REF_THERM}, the ALERT and BATT_SHDN signals are output, and the internal switch is turned off. When the NTC voltage exceeds $V_{REF\_THERM\_REL}$, the internal switch is turned on with a soft start. There are two detection pin NTC1 and NTC2. When over temperature protection is not used, connect all NTCx pin to the VLDO. If there is only one temperature monitoring point, connect the unused NTCx pin to the VLDO, or short circuit multiple NTCx pin and connect them to the thermistor. Each pin has the same threshold and the operation when detection and release is also same as follows. The delay time of t_{DELAY_ALERT} is counted separately for NTC1 and NTC2.
Also, during t_{DELAY_WAIT}, hysteresis is disabled, threshold is fixed V_{REF_THERM}. ALERT/KILL is also fixed at Low during t_{DELAY_WAIT}.

Monitor pin: NTC1, NTC2
Detect threshold: V_{REF_THERM}
Release threshold: $V_{REF\_THERM\_REL}$

When detection,
- Internal load switch: OFF, after t_{DELAY_ALERT}
- Active discharge: ON, after t_{DELAY_ALERT}
- ALERT/KILL: H, immediately
- BATT_SHDN: L, after t_{DELAY_ALERT}

When release,
- Internal load switch: ON with soft start function
- Active discharge: OFF, immediately
- ALERT/KILL: L, immediately
- BATT_SHDN: H, immediately

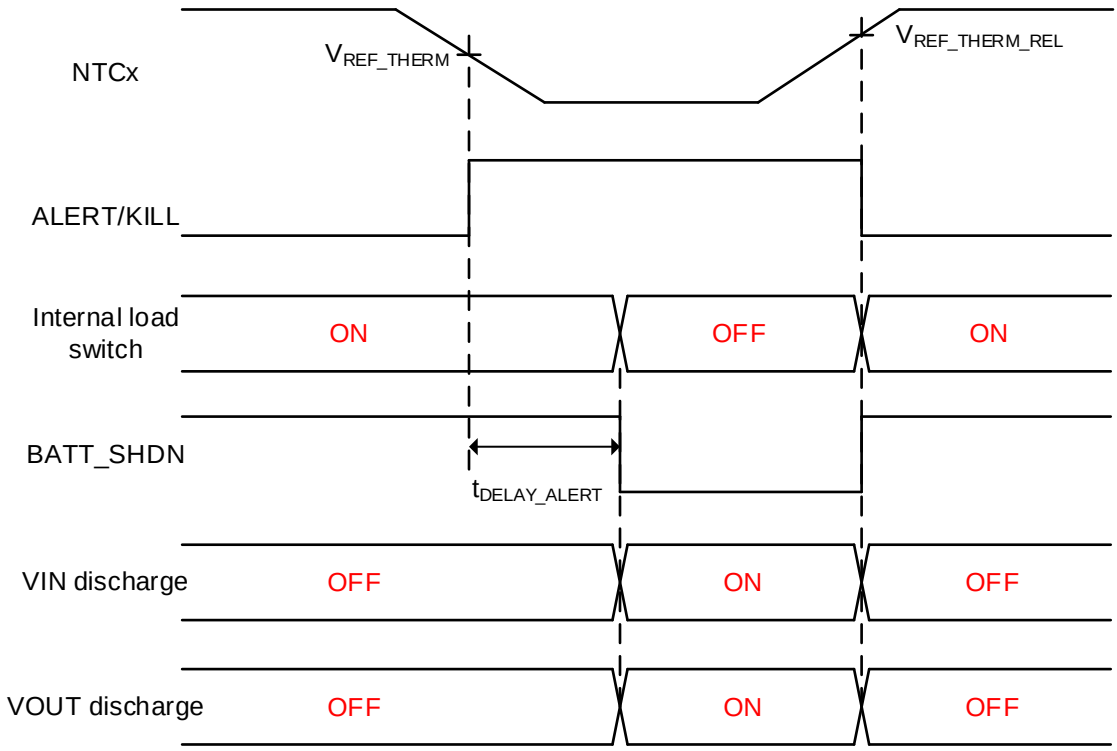


Figure 33. Over Temperature Protection Timing Chart

Function Descriptions - continued

When Use NTC1 Pin as EN

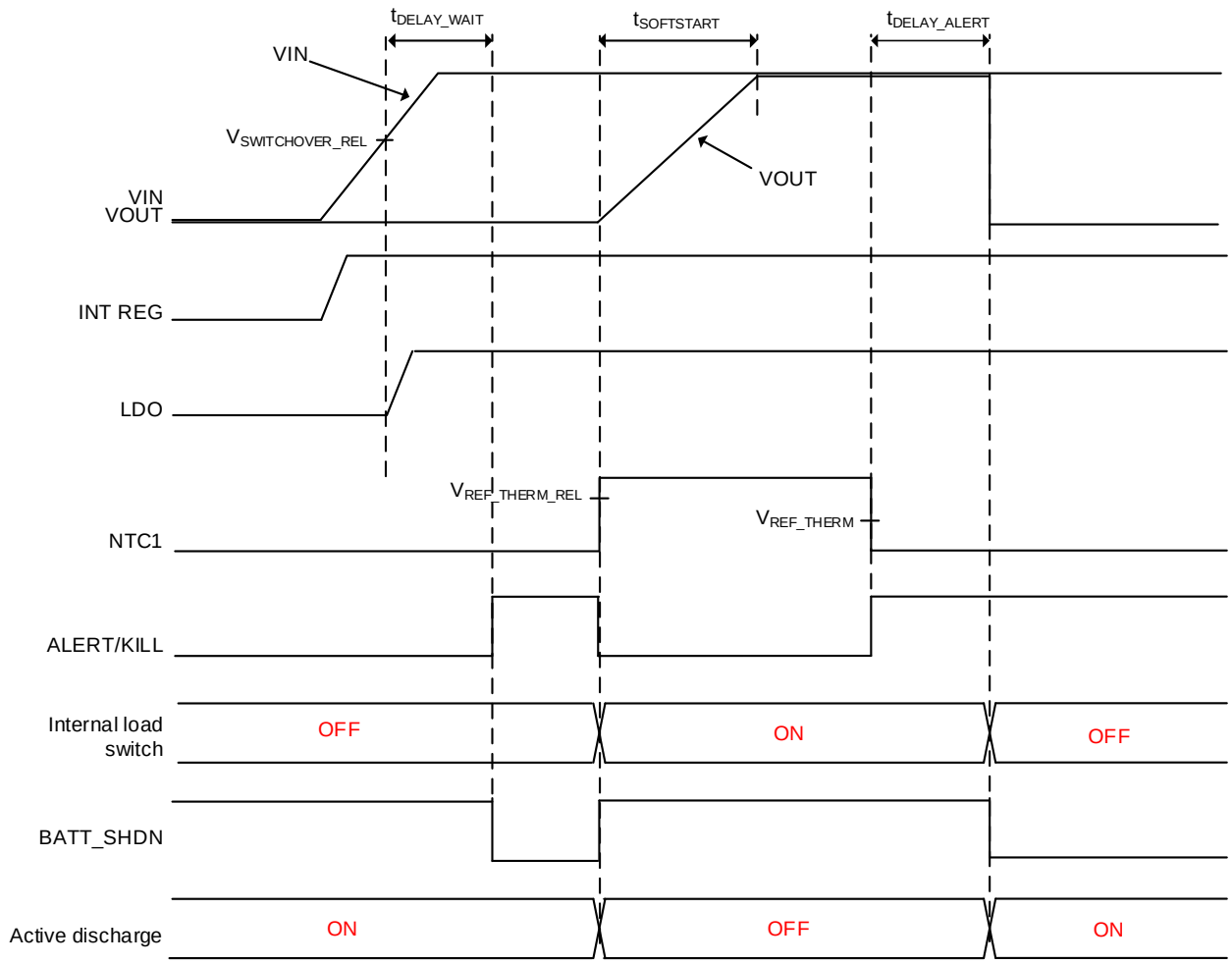


Figure 34. Timing Chart when use NTC1 as EN

The NTC1 pin can also be used as EN.
The Internal switch turns ON with a soft start at the timing when the NTC1 pin voltage exceeds $V_{REF\_THERM\_REL}$.
ALERT/KILL goes High when the NTC1 pin voltage drops below V_{REF_THERM}, and after t_{DELAY_ALERT}, the switch turns off and BATT_SHDN goes Low.

Function Descriptions - continued

Over Voltage Protection

By connecting the resistive divider point between VIN pin and GND to the OVP pin, the overvoltage of VIN can be detected. When the OVP voltage exceed V_{REF_OVP}, the internal switch is turned off, immediately. When the OVP voltage falls below the threshold, the internal switch is turned on with a soft start. The detection threshold, hysteresis, and operations when detection and release are as follows. Also, during t_{DELAY_WAIT}, hysteresis is disabled, threshold is fixed V_{REF_OVP}. The OVP pin has a parasitic capacitance of 10 pF (Max), so pay attention to the voltage divider resistor value.

Monitor pin: OVP
Detect threshold: V_{REF_OVP}
Hysteresis: $V_{REF\_OVP\_HYS}$

When detection,
Internal load switch: OFF, after t_{DELAY_OVP}
Active discharge: -
ALERT/KILL: -
BATT_SHDN: -

When release,
Internal load switch: ON with soft start, after $t_{DELAY\_OVP\_REC}$
Active discharge: -
ALERT/KILL: -
BATT_SHDN: -

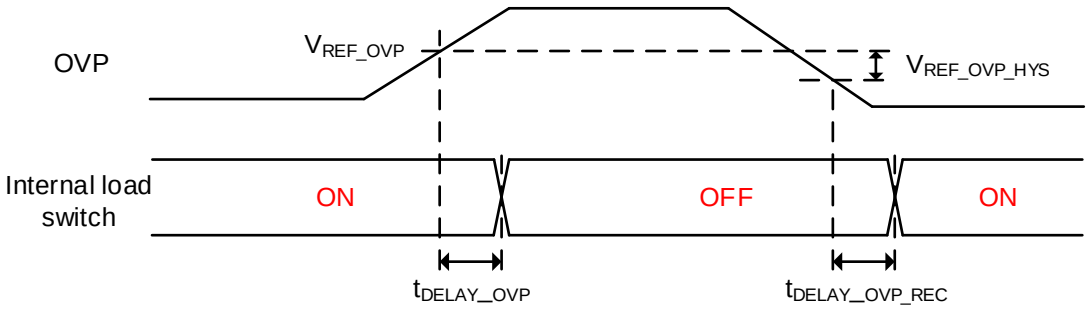


Figure 35. OVP Timing Chart

Function Descriptions - continued

Internal Over Voltage Protection

The IC has an internal OVP function in case the OVP pin is shorted to ground. When the OVP voltage drops below $V_{OVP\_INT\_EN}$, the internal OVP is enabled and directly monitors the VIN pin voltage. When the OVP pin voltage exceeds $V_{OVP\_INT\_EN} + V_{OVP\_INT\_EN\_HYS}$, it returns to OVP pin monitoring. The detection threshold, hysteresis, and operations when detection and release are as follows.

Monitor pin: VIN
Detect threshold: V_{OVP_INT}
Hysteresis: $V_{OVP\_INT\_HYS}$

When detection,
Internal load switch: OFF, after t_{DELAY_OVP}
Active discharge: -
ALERT/KILL: -
BATT_SHDN: -

When release,
Internal load switch: ON, after $t_{DELAY\_OVP\_REC}$
Active discharge: -
ALERT/KILL: -
BATT_SHDN: -

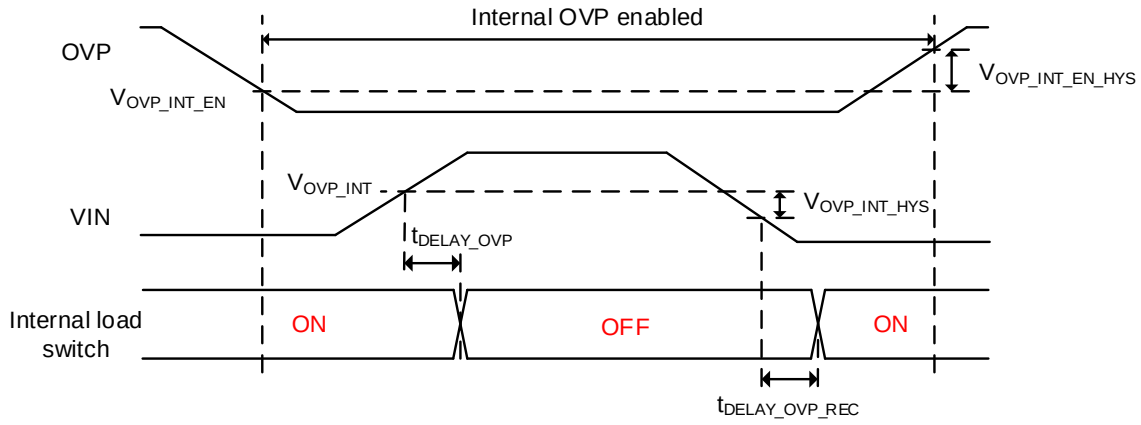


Figure 36. Internal OVP Timing Chart

Function Descriptions - continued

Over Current Limit Function and Over Current Protection Function and Internal Thermal Shutdown

The BD58020GW has an overcurrent limiting function (OCL), which limits the current flowing through the internal switch when an overload is connected to VOUT. When the current flowing through the internal switch exceeds I_{OCL}, the OCL feedback is enabled and the current through the switch is limited after t_{OCL_BLNK}. Also, OCL feedback is disabled after the overcurrent is released and t_{OCL_REL}. If the overcurrent condition continues and the junction temperature reaches the thermal shutdown detection temperature 150 °C (Typ), the LDO and the internal switch are turned off. The thermal shutdown function has hysteresis; when the junction temperature drops to 125 °C (Typ), the IC restarts with a soft start. Also, if an overcurrent flows during $t_{SOFTSTART}$, the current is immediately limited.

If the catastrophic overcurrent exceeding the I_{OCP}, the overcurrent protection (OCP) is activated and the internal switch is immediately turned off. After t_{OCP_REC}, and then restarts.

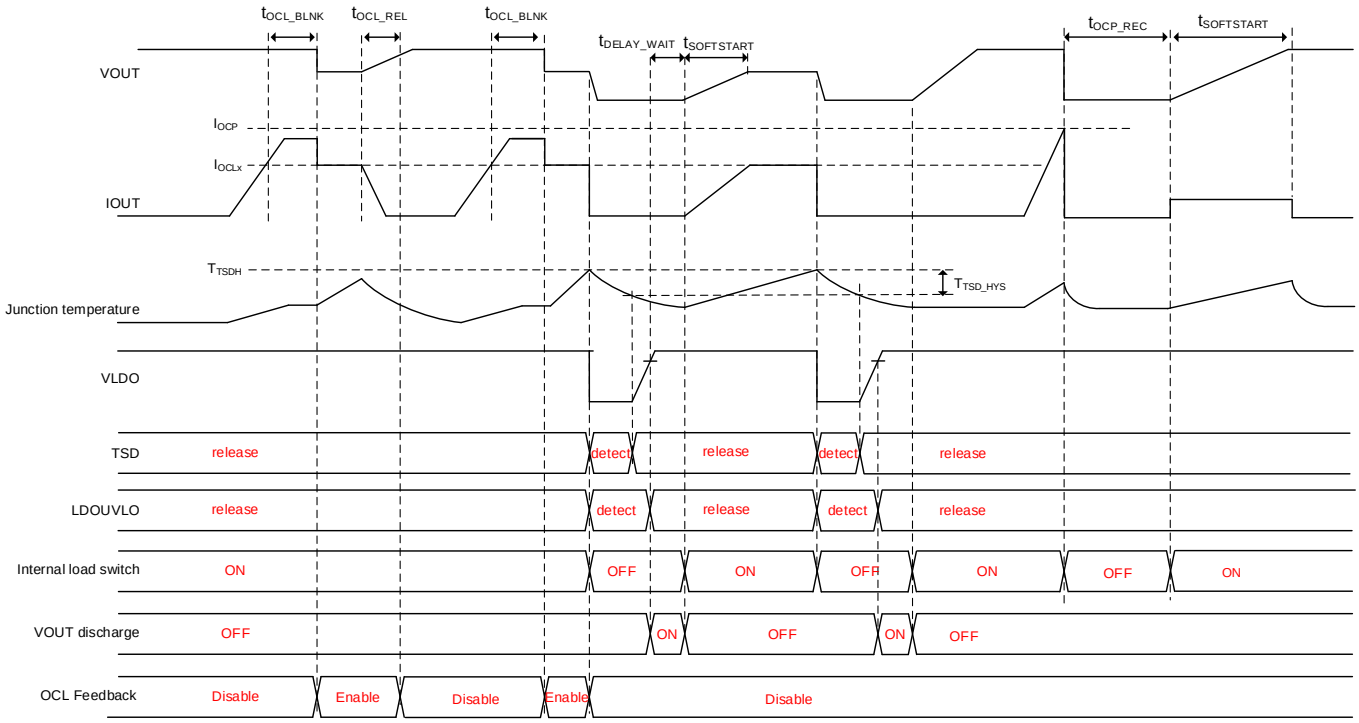


Figure 37. Over Current Limit Function and Over Current Protection Function Timing Chart

Function Descriptions - continued

Short Circuit Protection

If the VOUT voltage is low, the current flowing through the internal switch cannot be detected correctly. Therefore, a short circuit protection function is provided to prevent destruction of the IC. If the VOUT voltage does not rise even if the gate voltage of the internal switch rises, the internal switch is turned off, waits for OCP recovery time, t_{OCP_REC}, and then restarts.

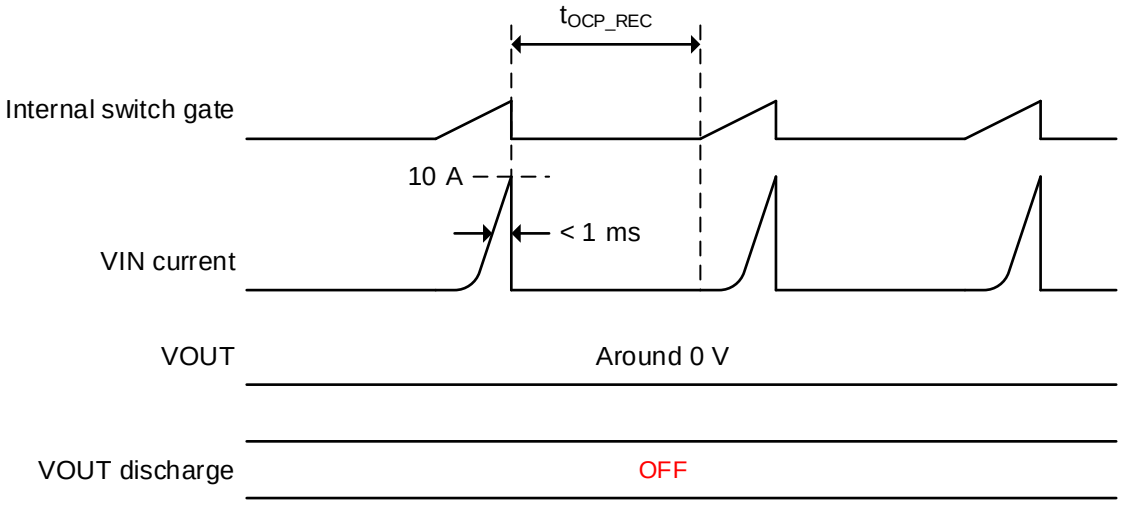


Figure 38. Short Circuit Protection Timing Chart

Brownout Protection

The brownout can be detected by connecting the resistor divider point between VIN pin and GND to BO pin. When the BO voltage falls below V_{REF_BO}, the internal switch is turned off. When the BO voltage exceeds the threshold, the internal switch is turned on with a soft start. When Brownout protection feature is not used, please connect BO pin to VLDO. The detection threshold, hysteresis, and operation at detection and release are as follows. Also, during t_{DELAY_WAIT}, hysteresis is disabled, threshold is fixed V_{REF_BO}.

Monitor pin: BO
Detect threshold: V_{REF_BO}
Hysteresis: $V_{REF\_BO\_HYS}$

When detection,
- Internal load switch: OFF, immediately
- Active Discharge: ON, immediately
- ALERT/KILL: -
- BATT_SHDN: -

When release,
- Internal load switch: ON with soft start, after $t_{DELAY\_BO\_REC}$
- Active Discharge: OFF, after $t_{DELAY\_BO\_REC}$
- ALERT/KILL: -
- BATT_SHDN: -

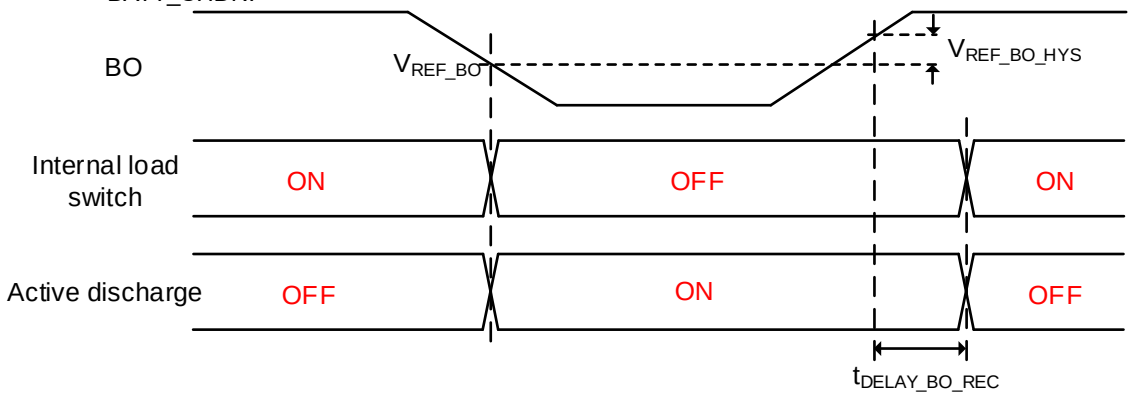


Figure 39. Brownout Timing Chart

Function Descriptions - continued

KILL Function

When the KILL signal is input to the ALERT/KILL pin for more than the t_{DELAY_KILL} period, the KILL latch is latched high. While the KILL latch is high, the internal switch logic is off and BATT_SHDN is low. The KILL latch is reset by a voltage drop on the VIN pin. The detection threshold, the release threshold, and operations when detection and release are as follows.

Monitor pin detect: ALERT/KILL
Monitor pin release: VIN
Detect threshold: V_{KILL_H}
Release threshold: $V_{SWITCHOVER}$

When detection,
- Internal load switch: OFF, after t_{DELAY_KILL}
- Active discharge: ON, after t_{DELAY_KILL}
- ALERT/KILL: -
- BATT_SHDN: L, after t_{DELAY_KILL}

When release,
- KILL latch: L, immediately
- Internal load switch: ON, after VIN exceeds $V_{SWITCHOVER\_REL}$ and t_{DELAY_WAIT} elapses
- Active discharge: OFF, after VIN exceeds $V_{SWITCHOVER\_REL}$ and t_{DELAY_WAIT} elapses
- ALERT/KILL: -
- BATT_SHDN: H, immediately

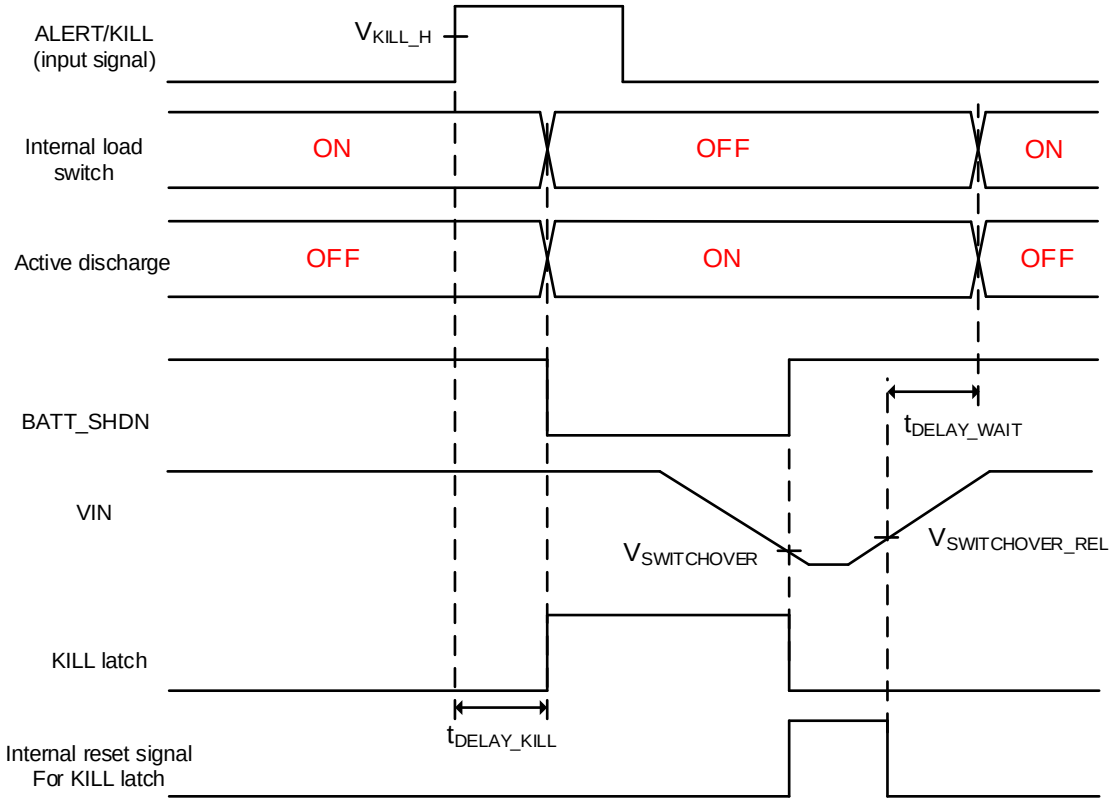


Figure 40. KILL Function Timing Chart

Function Descriptions - continued

KILL Function (When VIN voltage is below $V_{SWITCHOVER}$)

Even if the VIN voltage is lower than $V_{SWITCHOVER}$(VBAT is applied), when ALERT/KILL pin is driven to H for more than the t_{DELAY_KILL} period, the IC enters the KILL state and BATT_SHDN becomes L. However, the KILL state is not latched, and BATT_SHDN becomes H as soon as ALERT/KILL is driven to L. Also, when the t_{DELAY_KILL} period, VLDO keeps on. After the t_{DELAY_KILL} period, the LDO operates intermittently (burst operation) to reduce the current consumption of the VBAT.

Monitor pin detect: ALERT/KILL
Monitor pin release: ALERT/KILL
Detect threshold: V_{KILL_H}
Release threshold: V_{KILL_L}

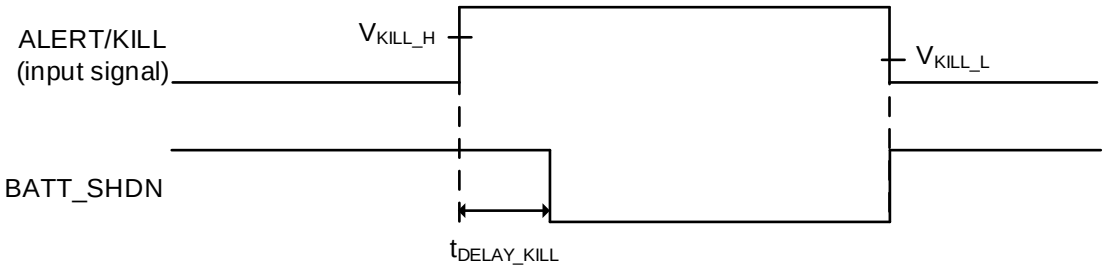


Figure 41. KILL Function (When VIN is below $V_{SWITCHOVER}$) Timing Chart

Power MUX Function

Power MUX generates power supply, VDD_PWRMUX, for internal circuits and LDO from VIN or VBAT according to input conditions. When VIN voltage exceeds the threshold of $V_{SWITCHOVER\_REL}$ VDD_PWRMUX is generated from VIN. On the other hand, when VIN voltage is lower than $V_{SWITCHOVER}$ and VBAT voltage is higher than V_{VBAT_OK}, VDD_PWRMUX is generated from VBAT. When VIN voltage is lower than $V_{SWITCHOVER}$ and VBAT voltage is lower than V_{VBAT_OK}, VDD_PWRMUX is generated from higher voltage source between VIN and VBAT by diode-or circuit.
When VIN is below $V_{SWITCHOVER}$, the circuits except for the overheat protection stop, and the current consumption is suppressed.

VIN > $V_{SWITCHOVER}$: VDD_PWRMUX is powered from VIN
VIN < $V_{SWITCHOVER}$ and VBAT > V_{VBAT_OK}: VDD_PWRMUX is powered from VBAT
VIN < $V_{SWITCHOVER}$ and VBAT < V_{VBAT_OK}: VDD_PWRMUX is powered from higher voltage source between VIN and VBAT

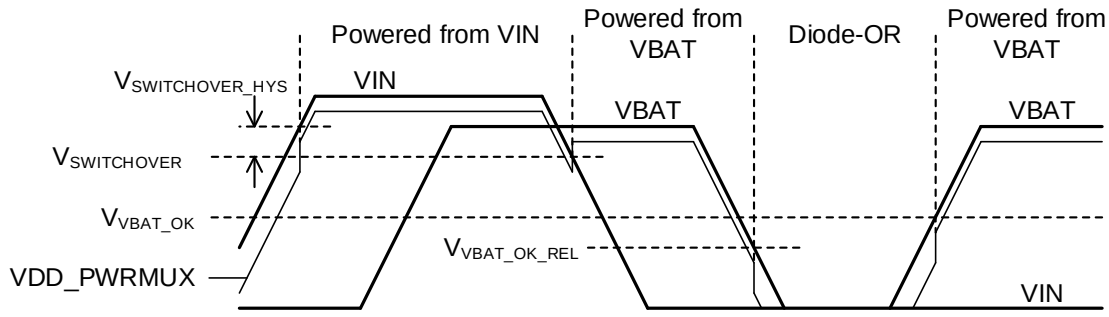


Figure 42. VDD_PWRMUX and VIN, VBAT

Host/OTG Mode

In OTG mode, power is first supplied from VOUT to VIN through the body diode of the Internal Nch MOSFET. When VIN voltage exceeds $V_{SWITCHOVER\_REL}$, and BO voltage exceeds V_{REF_BO}, the Internal switch turns on. When VIN grounded, large current flows from VOUT to VIN. To prevent the large current from flowing, please limit the current of the power supply connected to the VOUT.

Application Information

Over Temperature Protection Setting

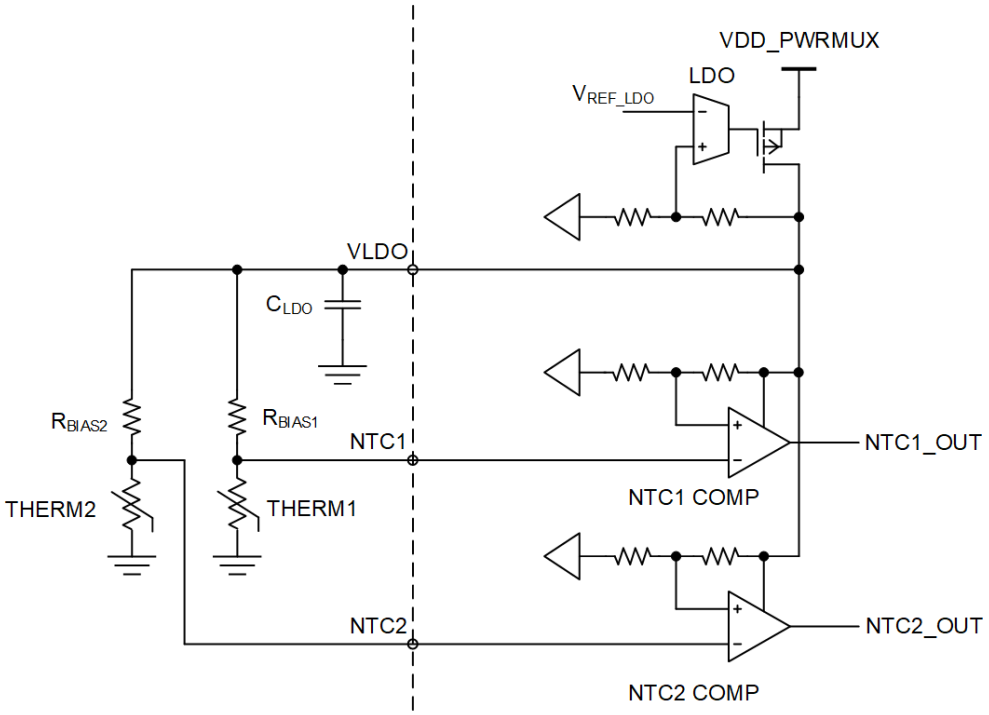


Figure 43. Circuit Diagram around Over Temperature Protection Setting

The detection temperature is set by R_{BIASx} and THERMx. Set R_{BIASx} according to the following formula.

$$R_{\mathrm{BIASx}} = \left(\frac{1-\alpha_{\mathrm{TRIP}}}{\alpha_{\mathrm{TRIP}}}\right) R_{\mathrm{NTC\_TEMP\_TRIP}}$$

Where:
$R_{\mathrm{NTC\_TEMP\_TRIP}}$ is the resistance of the thermistor at the detection temperature.
α_{TRIP} is the ratio of V_{REF_THERM} to V_{LDO}.

To calculate the error in detection temperature, calculate min/max of $R_{NTC\_TEMP\_TRIP}$ from min/max of α_{TRIP} and R_{BIASx} in reverse order of the above procedure.

$$R_{\mathrm{NTC\_TEMP\_TRIP\_max}} = \left(\frac{\alpha_{\mathrm{TRIP\_max}}}{1-\alpha_{\mathrm{TRIP\_max}}}\right) R_{\mathrm{BIASx\_max}}$$

$$R_{\mathrm{NTC\_TEMP\_TRIP\_min}} = \left(\frac{\alpha_{\mathrm{TRIP\_min}}}{1-\alpha_{\mathrm{TRIP\_min}}}\right) R_{\mathrm{BIASx\_min}}$$

The temperature of the thermistor at min/max of $R_{NTC\_TEMP\_TRIP}$ is the min/max of the detection temperature. When calculating the temperature from $R_{NTC\_TEMP\_TRIP}$, the tolerance of the thermistor must be included in the calculation. To calculate the release temperature, replace α_{TRIP} with α_{TRIP_REL} in the above procedure.

Application Information - continued

Examples of the detection temperature setting is presented below.
B: Constants that describe the relationship between temperature and resistance of thermistor.
R0: Resistance value of the thermistor at Ta = 25 °C

Detect temperature = 80 °C
Thermistor: NCP15WF104F03RC (without variability, β = 4250 K (25/50 °C), R0 = 100 kΩ)
R_{BIAS}: 10.5 kΩ ± 0 %

	Min	Typ	Max	Unit
Detect temperature	79.3	80.2	81.0	°C
Release temperature	54.8	56.2	57.5	°C
Thermal hysteresis	23.5	24.0	24.5	°C

Detect temperature = 70 °C
Thermistor: NCP15WF104F03RC (without variability, β = 4250 K (25/50 °C), R0 = 100 kΩ)
R_{BIAS}: 15 kΩ ± 0 %

	Min	Typ	Max	Unit
Detect temperature	69.5	70.3	71.1	°C
Release temperature	46.1	47.4	48.7	°C
Thermal hysteresis	22.4	22.9	23.4	°C

Detect temperature = 60 °C
Thermistor: NCP15WF104F03RC (without variability, β = 4250 K (25/50 °C), R0 = 100 kΩ)
R_{BIAS}: 22.1 kΩ ± 0 %

	Min	Typ	Max	Unit
Detect temperature	59.4	60.1	60.9	°C
Release temperature	37.1	38.4	39.6	°C
Thermal hysteresis	21.3	21.8	22.2	°C

Detect temperature = 50 °C
Thermistor: NCP15WF104F03RC (without variability, β = 4250 K (25/50 °C), R0 = 100 kΩ)
R_{BIAS}: 33.2 kΩ ± 0 %

	Min	Typ	Max	Unit
Detect temperature	49.3	50.0	50.7	°C
Release temperature	28.2	29.3	30.5	°C
Thermal hysteresis	20.2	20.7	21.1	°C

Application Information - continued

OVP, BO Settings

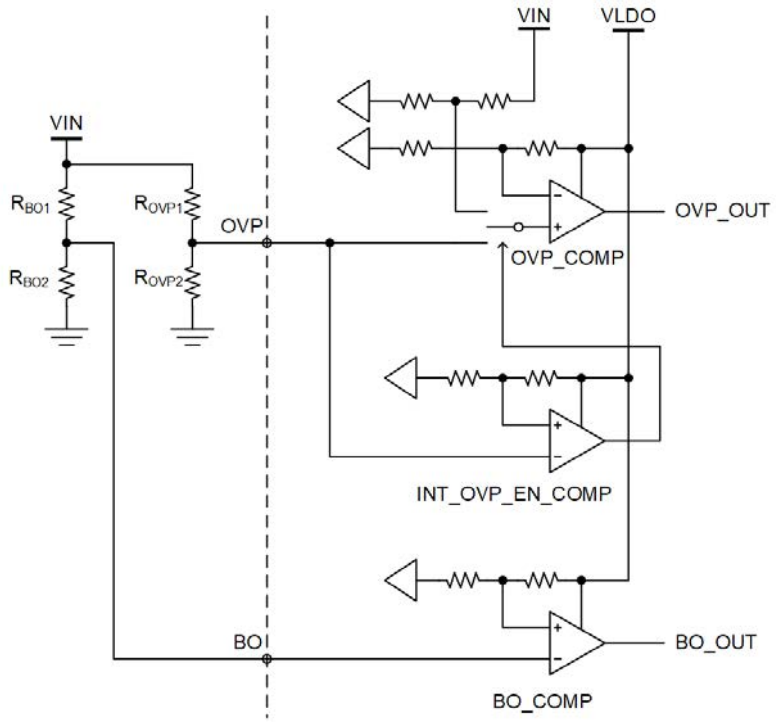


Figure 44. Circuit Diagram around OVP, BO Setting

OVP and BO are detected by comparing the resistive divider between VIN and GND with the reference voltage as shown in the figure. The detector threshold can be set by the following formula.

$$V_{\mathrm{OVP}} = V_{\mathrm{REF\_OVP}} \times \frac{R_{\mathrm{OVP1}} + R_{\mathrm{OVP2}}}{R_{\mathrm{OVP2}}}$$

$$V_{\mathrm{BO}} = V_{\mathrm{REF\_BO}} \times \frac{R_{\mathrm{BO1}} + R_{\mathrm{BO2}}}{R_{\mathrm{BO2}}}$$

The OVP function can be changed to internal OVP with fixed threshold by connecting the OVP pin to GND. The internal OVP monitors the VIN pin voltage, and the threshold value is $V_{\mathrm{OVP\_INT}}$.

Application Information - continued

OCL Settings

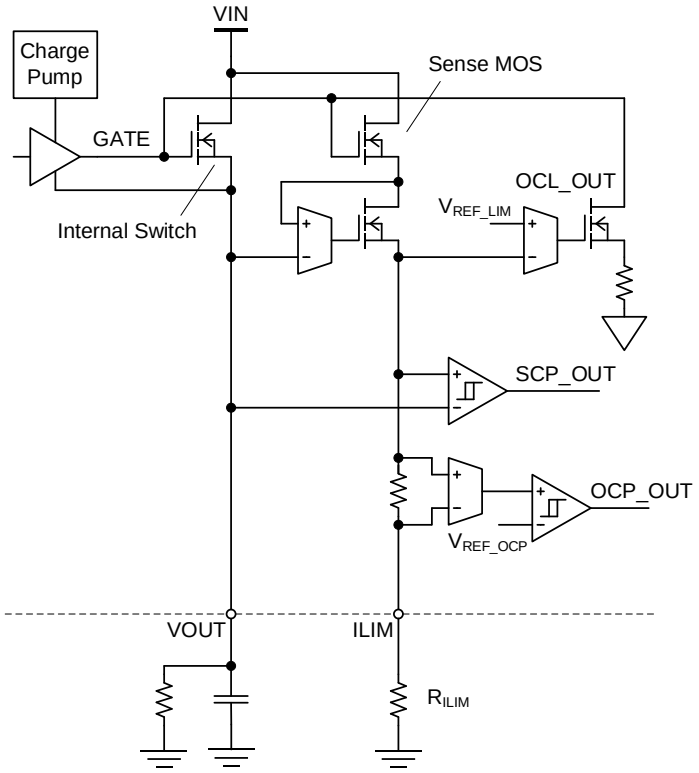


Figure 45. Circuit Diagram around OCL Setting

The overcurrent limit can be set by the resistance R_{ILIM} between the ILIM pin and GND. The R_{ILIM} should be placed in the vicinity of the IC. The current flowing through the ILIM pin is proportional to that flowing through the VOUT pins. The resistor R_{ILIM} connected to the ILIM pin converts this current to a voltage. When the ILIM voltage reaches V_{REF_LIM}, it lowers gate voltage of the internal switch and limits the current. The current limit is as following formula.

$$I_{\mathrm{OCL}} = 999.34 \times {R_{ILIM}}^{-0.8928}$$

$$R_{ILIM} = 2289.53 \times {I_{OCL}}^{-1.1201}$$

LDO Output Capacitor

The BD58020GW has a built-in LDO for reference of over temperature protection and internal circuit power supply. Even if the over temperature protection function is not used, connect a ceramic capacitor C_{LDO} with an effective capacitance of 0.1 µF or more between the V_{LDO} and GND. The C_{LDO} should be placed in the vicinity of the IC.

Application Examples

USB and Battery configuration

Example design parameters
VBAT = 2.7 V to 5.5 V
VIN = 0 V to 5.25 V
OVP threshold = 6.0 V
BO threshold = 4.0 V
OverTempProtection1 = OverTempProtection2 = 60 °C
OCL threshold = 2.09 A

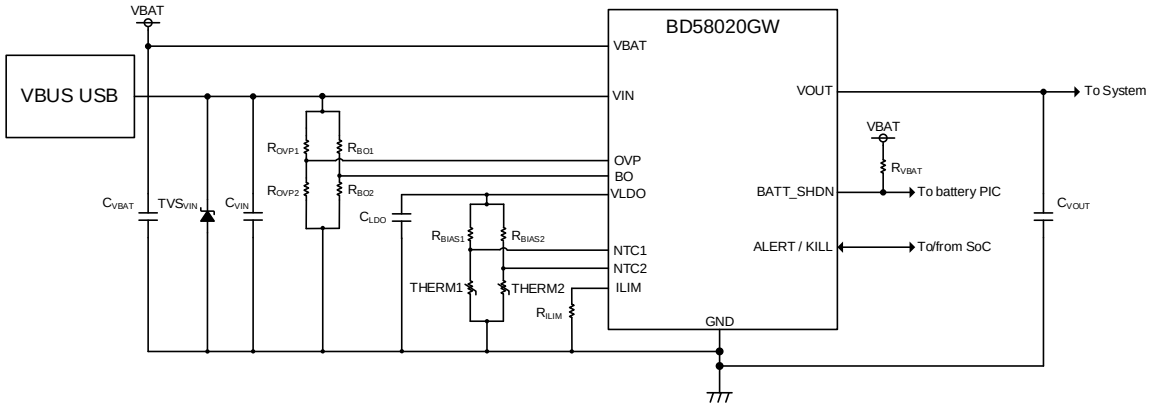


Figure 46. Application Circuits of USB and Battery Configuration

Table 2. BOM List of USB and Battery Configuration

Contents	Reference	Manufacturer	Parts Name	Descriptions	Size (mm)
TVS diode	TVS_{VIN}	ROHM semiconductor	VS6V3UC1QST18R	6.3V TVS diode	1006
Capacitor	C_{VIN}	Murata Electronics	GRM153R61A105ME95	1.0 µF	1005
Capacitor	C_{VOUT}	Murata Electronics	GRM153R61A105ME95	1.0 µF	1005
Capacitor	C_{VBAT}	Murata Electronics	GRM153R61A105ME95	1.0 µF	1005
Capacitor	C_{LDO}	Murata Electronics	GRM155R71A224KE01	0.22 µF *(Note 6)*	1005
		Murata Electronics	GRM155R71A474KE01	0.47 µF *(Note 7)*	1005
Resistor	R_{OVP1}	ROHM semiconductor	MCR01SMQPF4023	402 kΩ	1005
Resistor	R_{OVP2}	ROHM semiconductor	MCR01SMQPF1003	100 kΩ	1005
Resistor	R_{BO1}	ROHM semiconductor	MCR01SMQPF3483	348 kΩ	1005
Resistor	R_{BO2}	ROHM semiconductor	MCR01SMQPF1503	150 kΩ	1005
Resistor	R_{ILIM}	ROHM semiconductor	MCR01SMQPF1001	1 kΩ	1005
Resistor	R_{BIAS1}	ROHM semiconductor	MCR01SMQPF2212	22.1 kΩ	1005
Resistor	R_{BIAS2}	ROHM semiconductor	MCR01SMQPF2212	22.1 kΩ	1005
Resistor	R_{VBAT}	ROHM semiconductor	MCR01SMQPF1003	100 kΩ	1005
Thermistor	THERM1	Murata Electronics	NCP15WF104F03RC	100 kΩ / 4250 K	1005
Thermistor	THERM2	Murata Electronics	NCP15WF104F03RC	100 kΩ / 4250 K	1005

(Note 6) When Ta = 0 °C to +125 °C
(Note 7) When Ta = -40 °C to +125 °C

Application Examples - continued

AC/DC Adapter System - configuration

Example design parameters
VIN = 0 V to 18.9 V
OVP threshold = 21.6 V
BO threshold = 15 V
OverTempProtection1 = OverTempProtection2 = 60 °C
OCL threshold = 2.09 A

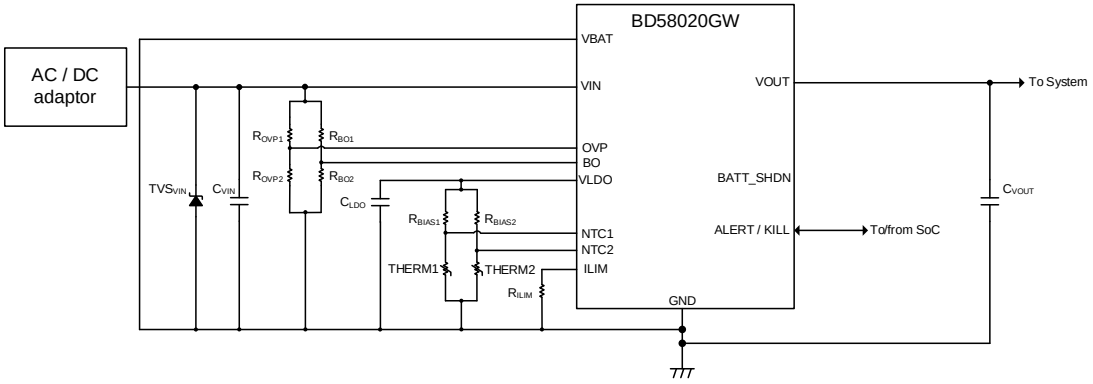


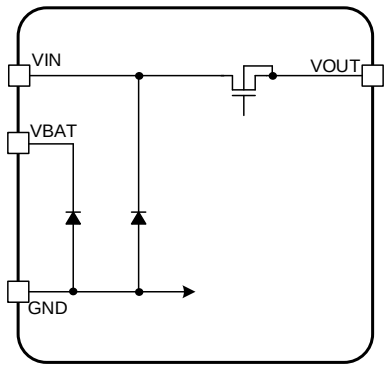
Figure 47. Application Circuits of AC/DC Adapter System Configuration

Table 3. BOM List of AC/DC Adapter System Configuration

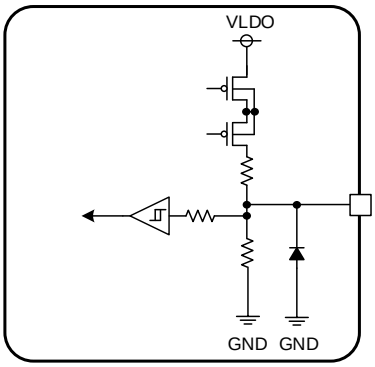
Contents	Reference	Manufacturer	Parts Name	Descriptions	Size (mm)
TVS diode	TVS_{VIN}	ROHM semiconductor	SMF20V	20 V TVS diode	1.6 x 3.5
Capacitor	C_{VIN}	Murata Electronics	GRM155R61E105MA12D	1.0 µF	1005
Capacitor	C_{VOUT}	Murata Electronics	GRM155R61E105MA12D	1.0 µF	1005
Capacitor	C_{LDO}	Murata Electronics	GRM155R71A224KE01	0.22 µF *(Note 6)*	1005
		Murata Electronics	GRM155R71A474KE01	0.47 µF *(Note 7)*	1005
Resistor	R_{OVP1}	ROHM semiconductor	MCR01SMQPF5103	510 kΩ	1005
Resistor	R_{OVP2}	ROHM semiconductor	MCR01SMQPF3002	30 kΩ	1005
Resistor	R_{BO1}	ROHM semiconductor	MCR01SMQPF1503	150 kΩ	1005
Resistor	R_{BO2}	ROHM semiconductor	MCR01SMQPF1302	13 kΩ	1005
Resistor	R_{ILIM}	ROHM semiconductor	MCR01SMQPF1001	1 kΩ	1005
Resistor	R_{BIAS1}	ROHM semiconductor	MCR01SMQPF2212	22.1 kΩ	1005
Resistor	R_{BIAS2}	ROHM semiconductor	MCR01SMQPF2212	22.1 kΩ	1005
Thermistor	THERM1	Murata Electronics	NCP15WF104F03RC	100 kΩ / 4250 K	1005
Thermistor	THERM2	Murata Electronics	NCP15WF104F03RC	100 kΩ / 4250 K	1005

(Note 6) When Ta = 0 °C to +125 °C
(Note 7) When Ta = -40 °C to +125 °C

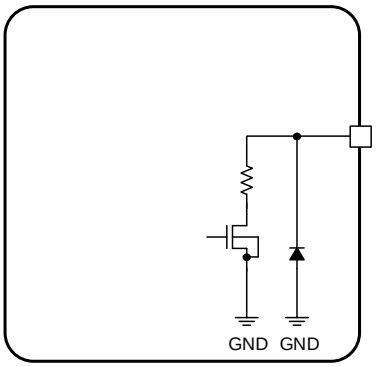
I/O Equivalence Circuits



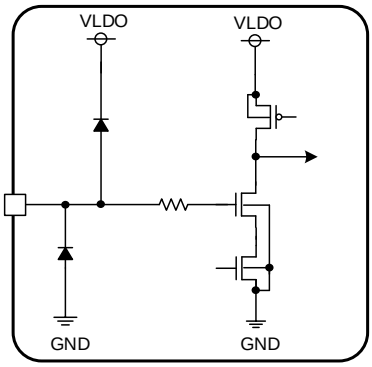
(A1, A2, B1, B2, C1, C2, C3)



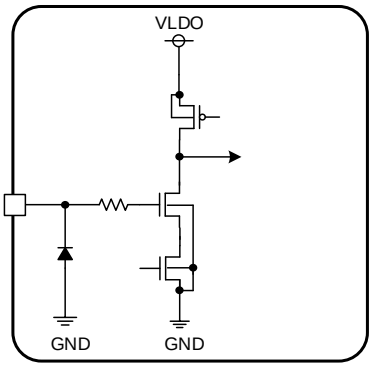
(A3)



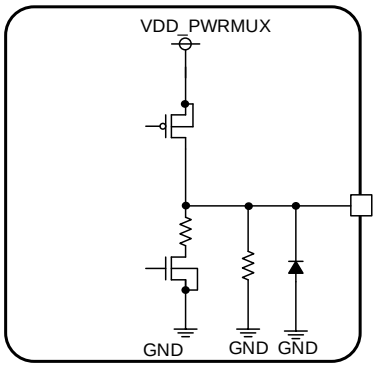
(B3)



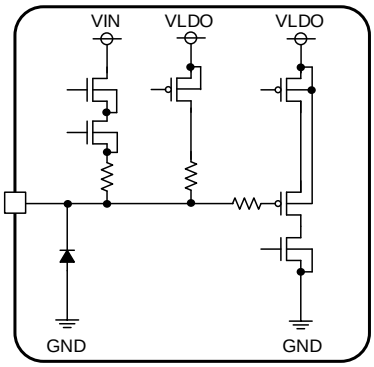
(A4, D4)



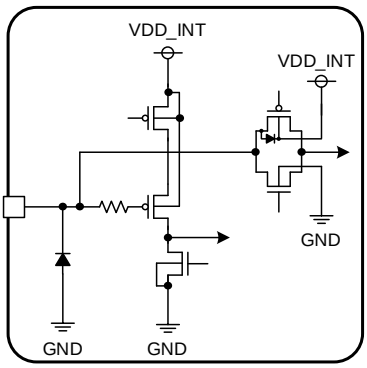
(B4)



(C4)



(D1)



(D3)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

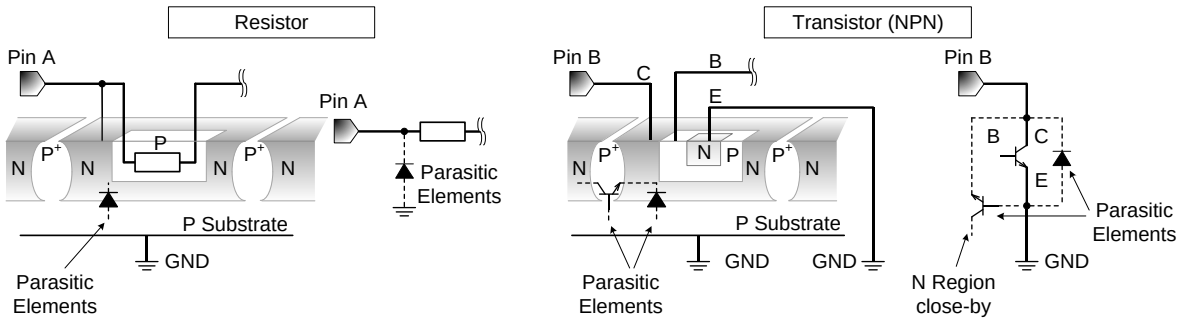


Figure 48. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

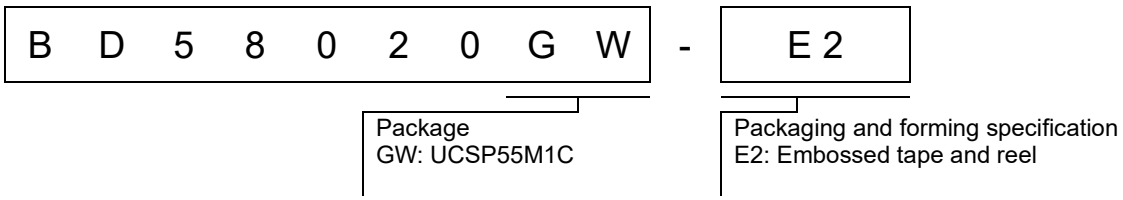
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

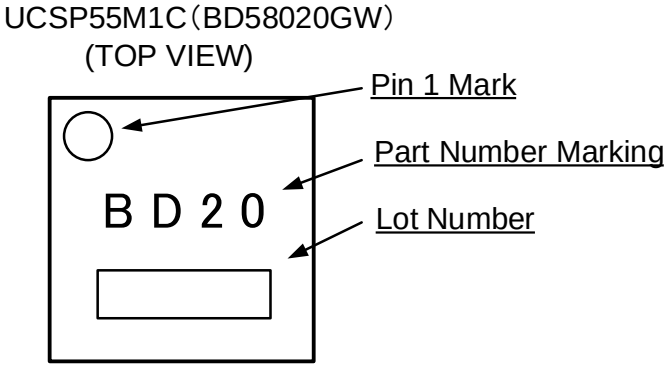
14. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

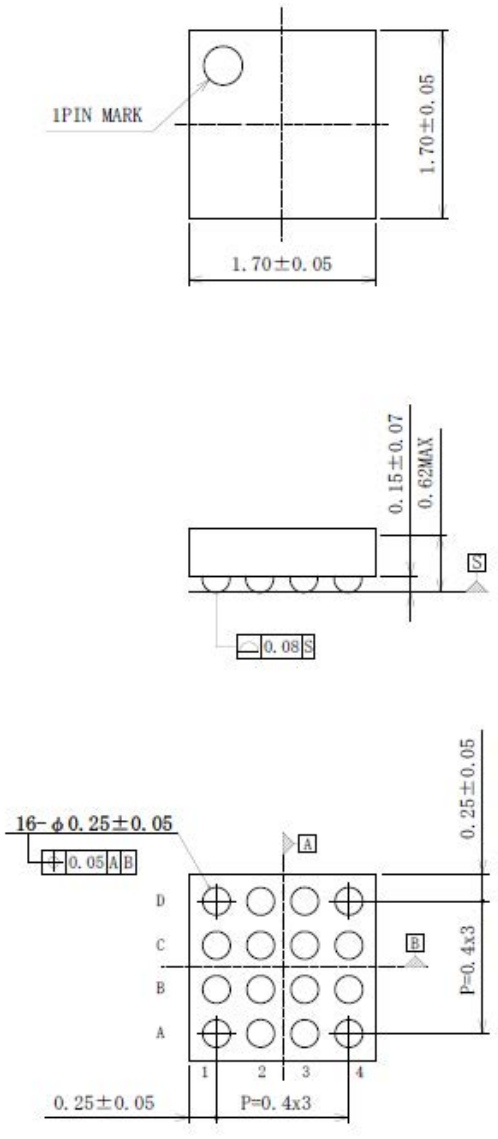


Marking Diagrams



Physical Dimension and Packing Information

Package Name	UCSP55M1C (BD58020GW)

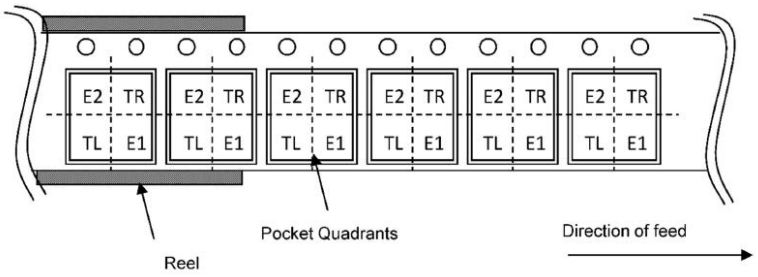


(UNIT:mm)

Drawing No.:EX972-5003

Packing form, Quantity, PIN1 Orientation and Weight

Packing Form		Tape&Reel
Packing Quantity	[pcs/Reel]	3,000
PIN 1 Orientation		E2



Revision History

Date	Revision	Changes
27.Mar.2024	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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