

LVDS Interface ICs

35bit LVDS Transmitter 35:5 Serializer



BU8254KVT No.13057ECT06

Description

LVDS Interface IC of ROHM "Serializer" "Deserializer" operate from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

Features

- 1) 35bits data of parallel LVCMOS level inputs are converted to five channels of LVDS data stream.
- 2) 30bits of RGB data and 5bits of timing and control data(HSYNC,VSYNC,DE,CNTL1,CNTL2) are transmitted up to 784Mbps effective rate per LVDS channel.
 - 3) Support clock frequency from 8MHz up to 112MHz.
 - 4) Support consumer video format including 480i, 480P, 720P and 1080i as well.
 - 5) Clock edge selectable
 - 6) Power down mode
 - 7) Support spread spectrum clock generator.
 - 8) Support reduced swing LVDS for low EMI.
 - 9) 30bit LVDS receiver is recommended to use BU90R104.

Applications

Flat Panel Display

Precaution

- ■This chip is not designed to protect from radioactivity.
- ■The chip is made strictly for the specific application or equipment.

Then it is necessary that the unit is measured as need.

■This document may be used as strategic technical data which subjects to COCOM regulations.

Technical Note

Block Diagram

BU8254KVT

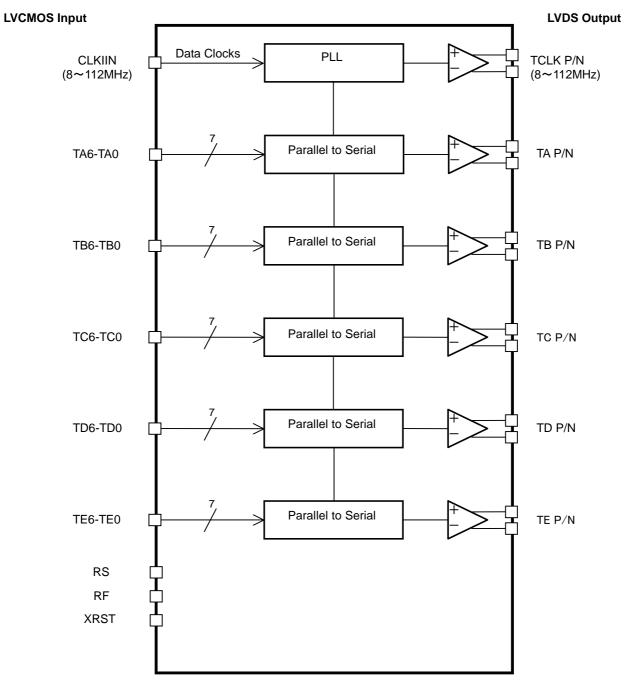


Fig.1 Block Diagram

●TQFP64V Package Outline and Specification

TQFP64V

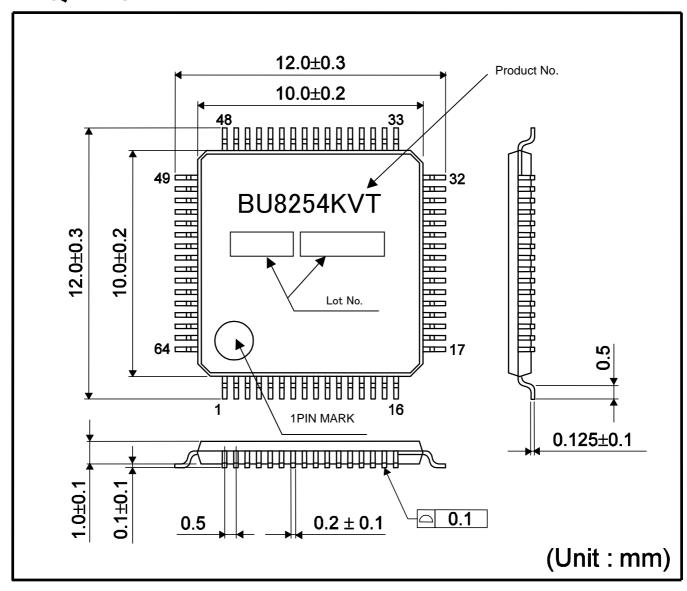


Fig.2 TQFP64V Package Outline and Specification

Pin configuration

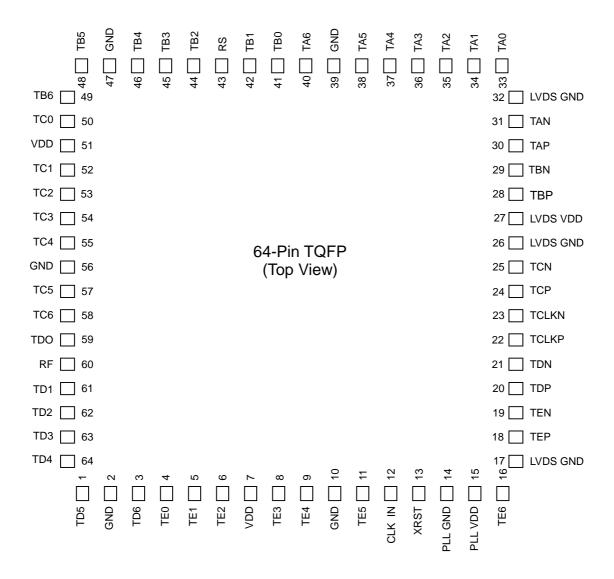


Fig.3 Pin Diagram (Top View)

●Pin Description

Table 1 : Pin Description

Table 1 : Pin Description									
Pin Name	Pin No.	Туре	Descriptions						
TAP, TAN	30,31	LVDS OUT							
TBP, TBN	28,29	LVDS OUT							
TCP, TCN	24,25	LVDS OUT	LVDS data out.						
TDP, TDN	20,21	LVDS OUT							
TEP, TEN	18,19	LVDS OUT							
TCLKP, TCLKN	22,23	LVDS OUT	LVDS clock out.						
TA0∼TA6	33,34,35,36,37,38,40	IN							
TB0∼TB6	41,42,44,45,46,48,49	IN							
TC0~TC6	50,52,53,54,55,57,58	IN	Pixel data inputs.						
TD0~TD6	59,61,62,63,64,1,3	IN							
TE0~TE6	4,5,6,8,9,11,16	IN							
XRST	13	IN	H : Normal operation, L : Power down (all outputs are Hi-Z)						
			LVDS swing mode, V _{REF} *1 select.						
			RS LVDS Swing Small Swing Input Support						
RS	43	IN	V _{DD} 350mV N/A						
			0.6~1.4V	350mV	RS-V _{REF}				
			GND	200mV	N/A				
			*1 V _{REF} is Input Refere	nce Voltage.	_				
RF	60	IN	Input clock triggeri H: Rising edge, L						
VDD	51,7	Power	Power supply pins		s and digital core.				
CLKIN	12	IN	Clock input.						
GND	2,10,39,47,56	Ground	Ground pins for LV	CMOS inputs and	digital core.				
LVDS VDD	27	Power	Power supply pins for LVDS outputs.						
LVDS GND	17,26,32	Ground	Ground pins for LV	DS outputs.					
PLLVDD	15	Power	Power supply pin f	or PLL core.					
PLLGND	14	Ground	Ground pins for PLL core.						

Electrical characteristics

■Rating

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Rati	Units	
1 didiffeter	Symbol	Min	Max	Office
Supply Voltage	V_{DD}	-0.3	4.0	V
Input Voltage	V _{IN}	-0.3	V _{DD} +0.3	V
Output Voltage	V _{OUT}	-0.3	V _{DD} +0.3	V
Storage Temperature Range	Tstg	-55	125	°C

Table 3: Package Power

PACKAGE	Power Dissipation (mW)	De-rating (mW/°C) *1		
TQFP64V	700	7.0		
TQFF04V	1000 ^{*2}	10.0 ^{*2}		

At temperature Ta >25°C

The material of PCB board :The FR4 glass epoxy board.(3% or less copper foil area) (It is recommended to apply the above package power requirement to PCB board

when the small swing input mode is used)

Table 4: Recommended Operating Conditions

Parameter	Symbol		Ratings	Ratings		Conditions
	Mi	Min	Тур	Max	Units	Conditions
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	VDD,LVDSVDD,PLLVDD
Operating	Tonr	-40	-	85	°C	Clock frequency from 8MHz up to 90MHz
Temperature Range	Topr	0	-	70	°C	Cock frequency from 90MHz up to 112MHz

Package power when mounting on the PCB board. The size of PCB board $:70 \times 70 \times 1.6 (\text{mm}^3)$

■DC characteristics

Table 5 : LVCMOS DC Specifications (VDD=3.0V~3.6V, Ta=-40°C~85°C)

Parameter	Symbol	Rating			Units	Conditions
Farameter	Symbol	Min	Тур	Max	Offics	Conditions
High Level Input Voltage	V _{IH}	V _{DD} × 0.8	-	V_{DD}	V	exclude RS pin
Low Level Input Voltage	V _{IL}	GND	-	$V_{DD} \times 0.2$	٧	exclude No pili
High Level Input Voltage	V _{IHRS}	V _{DD} × 0.8	-	V_{DD}		RS pin
Low Level Input Voltage	V _{ILRS}	GND	-	0.2		Ko pili
Small Swing Voltage	V _{DDQ} *1	1.2	-	2.8	V	
Input Reference Voltage	V_{REF}	-	V _{DDQ} /2	-	-	Small Swing(RS=V _{DDQ} /2)
Small Swing High Level Input Voltage	V _{SH} ^{*2}	V _{DDQ} /2 +200mV	-	-	V	V _{REF} =V _{DDQ} /2
Small Swing Low Level Input Voltage	V _{SL} *2	-		V _{DDQ} /2 -200mV	V	V _{REF} =V _{DDQ} /2
Input Current	I _{INC}	-		±10	μΑ	$0V \le V_{IN} \le V_{DD}$

^{*1:} V_{DDQ} voltage defines max voltage of small swing input. It is not an actual input voltage.

Table 6: LVDS Transmitter DC Specifications(VDD=3.0V~3.6V, Ta=-40°C~85°C)

Parameter	Symbol	Rating			Units	Conditions	
i arameter	Symbol	Min	Тур	Min	Office	Conditions	
Differential Output Voltage	V _{OD}	250	350	450	mV	RL=100Ω	Normal swing RS=V _{DD}
Differential Output Voltage	VOD	100	200	300	mV	KL=10032	Reduced swing RS=GND
Change in VOD between complementary output states	ΔV _{OD}	-	-	35	mV	RL=100Ω	
Common Mode Voltage	V _{OC}	1.125	1.25	1.375	V		
Change in VOC between complementary output states	ΔV _{OC}	-	-	35	mV		
Output Short Circuit Current	I _{OS}	-	-	-24	mA	V_{OUT} =0V, RL=100 Ω	
Output TRI-STATE Current	l _{OZ}	-	-	±10	μA	XRST=0V, V _{OUT} =0V to V _{DD}	

^{*2:} Small swing signal is applied to TA[6:0], TB[6:0], TC[6:0], TD[6:0] TE[6:0], CLKIN.

■Supply Current

Table 7 : Supply Current

Doromotor	Cumbal	Rating			Lloito	Conditions	Conditions	
Parameter	Symbol	Min	Тур	Max	Units	Conditions		
Transmitter Supply		-	57	-	mA	RL=100Ω,CL=5pF V _{DD} =3.3V,RS=V _{DD} Gray Scale Pattern	f=85MHz	
Current	I _{TCCG}	-	42	-	mA	RL=100 Ω ,CL=5pF V _{DD} =3.3V,RS=GND Gray Scale Pattern	f=85MHz	
Transmitter Supply Current	I _{TCCW}	-	62	-	mA	RL=100Ω,CL=5pF V _{DD} =3.3V,RS=V _{DD} Worst Case pattern	f=85MHz	
		-	45	-	mA	RL=100Ω,CL=5pF V _{DD} =3.3V,RS=GND Worst Case pattern	f=85MHz	
Transmitter Power Down Supply Current	I _{TCCS}	-	-	10	μA	XRST=L		

Gray Scale Pattern

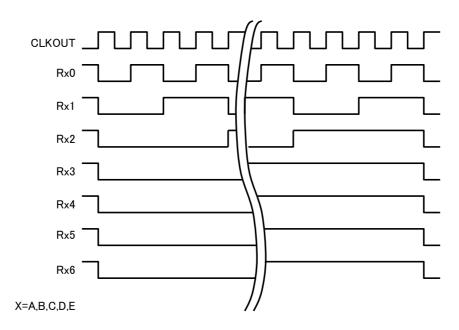


Fig.4 Gray scale pattern

Worst Case Pattern (Maximum Power condition)

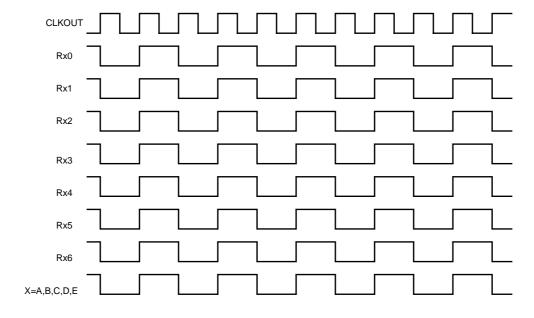


Fig.5 Worst Case Pattern

■AC characteristics

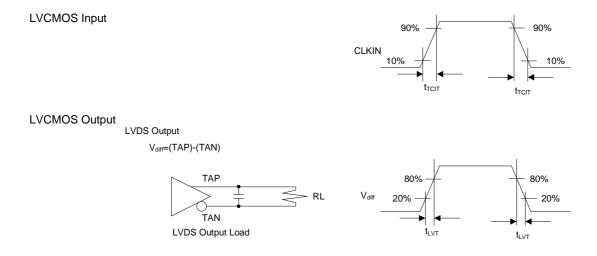
Table 8: Switching Characteristics

Table 8 : Switching Characteristics								
Parameter	Symbol	Min	Тур	Max	Units			
CLK IN Transition time	tтсіт	-	-	5.0	ns			
CLK IN Period	t _{TCP}	8.93	-	125.0	ns			
CLK IN High Time	t _{TCH}	0.35t _{TCP}	0.5t _{TCP}	0.65t _{TCP}	ns			
CLK IN Low Time	t _{TCL}	0.35t _{TCP}	0.5t _{TCP}	0.65t _{TCP}	ns			
CLK IN to TCLK+/-Delay	t _{TCD}	-	t _{TCP}	-	ns			
LVSMOS Data Set up to CLK IN	t _{TS}	2.5	-	-	ns			
LVCMOS Data Hold from CLK IN	tтн	0	-	-	ns			
LVDS Transition Time	t _{LVT}	-	0.6	1.5	ns			
Output Data Position 0	t _{TOP1}	-0.2	0.0	+0.2	ns			
Output Data Position 1	t _{TOP0}	$\frac{\text{trcp}}{7}$ -0.2	<u>ttcp</u> 7	$\frac{\text{tTCP}}{7} + 0.2$	ns			
Output Data Position 2	t _{TOP6}	$2\frac{\text{tTCP}}{7}$ -0.2	2 trcp 7	$2\frac{\text{tTCP}}{7} + 0.2$	ns			
Output Data Position 3	t _{TOP5}	$3\frac{\text{tTCP}}{7}$ -0.2	3 ttcp 7	$3\frac{\text{tTCP}}{7} + 0.2$	ns			
Output Data Position 4	t _{TOP4}	$4\frac{\text{tTCP}}{7}$ -0.2	4 ttcp 7	$4\frac{\text{tTCP}}{7} + 0.2$	ns			
Output Data Position 5	t _{TOP3}	$5\frac{\text{tTCP}}{7}$ -0.2	5 ttcp 7	$5\frac{\text{tTCP}}{7} + 0.2$	ns			
Output Data Position 6	t _{TOP2}	$6\frac{\text{tTCP}}{7}$ -0.2	6 ttcp 7	$6\frac{\text{tTCP}}{7} + 0.2$	ns			
Phase Locked Loop Set Time	t _{TPLL}	-	-	10.0	ms			

BU8254KVT Technical Note

AC Timing

■AC Timing Diagrams



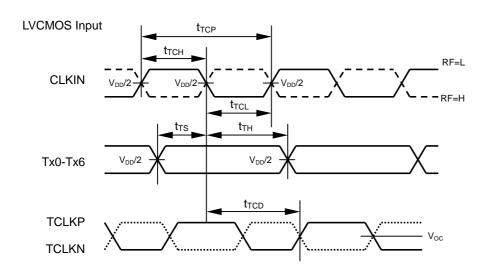


Fig.6 AC Timing Diagrams

■Small Swing Inputs

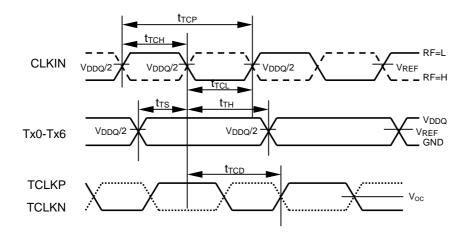


Fig.7 Small Swing Inputs

Technical Note

■AC Timing Diagrams

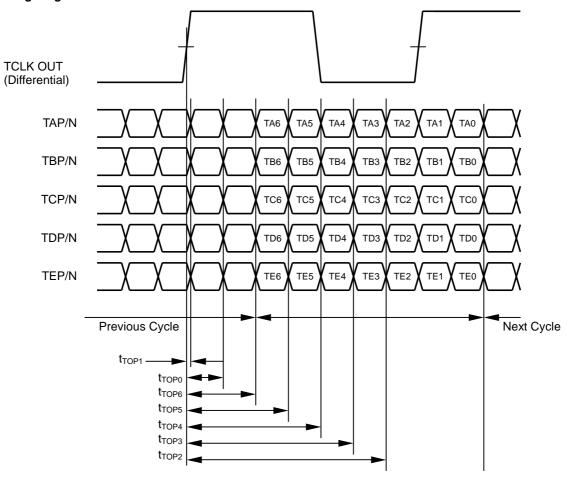


Fig.8 AC Timing Diagrams

■Phase Locked Loop Set Time

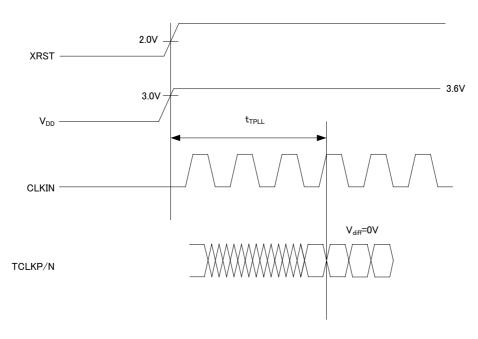


Fig.9 Phase Locked Loop Set Time

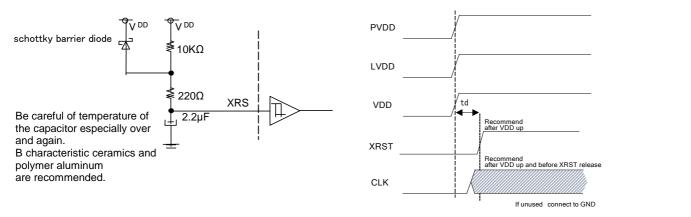
System Timing Requirement

System Timing Requirement is mandatory by following two methods.

- ①The method of using CR circuit.(In the case that CLK does not stop after power supply)
- ②The method of using external specific IC. (In the case that CLK turns on/off after power supply)

It is recommend to do enough examination for target application.

(1) The method of using CR circuit. (In the case that CLK does not stop after power supply)



td is approximately equal to 20ms when the left RC coleus are applied.

Fig.10 The method of using CR circuit.

2 The method of using external specific IC. (In the case that CLK turns on/off after power supply)

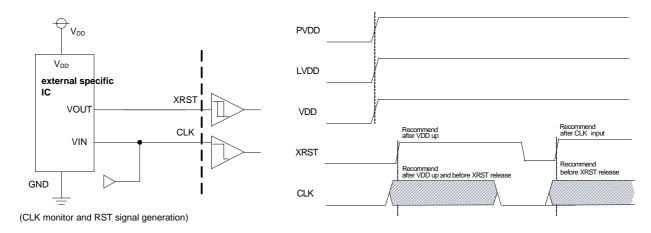


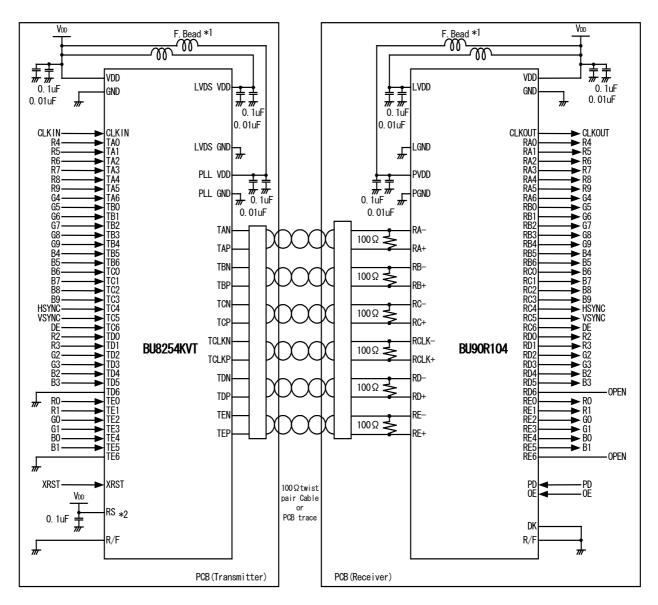
Fig.11 The method of using external specific IC.

●10bit LVCMOS Level Input

Example:

BU8254KVT: LVCMOS level input/Falling edge/Normal swing

BU90R104: Falling edge



^{*1 :} Recommended Parts: F.Bead : BLM18A-Series (Murata Manufacturing)

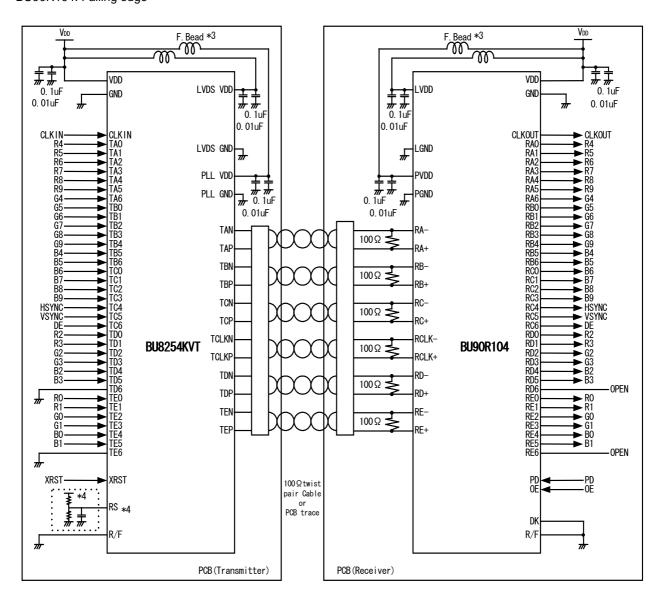
^{*2} If RS pin is tied to VDD, LVDS swing is 350m V. If RS pin is tied to GND, LVDS swing is 200m V.

●10bit Small Swing Input

Example:

BU8254KVT: LVCMOS level input/Falling edge/Normal swing

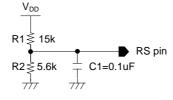
BU90R104: Falling edge



*3 : Recommended Parts:

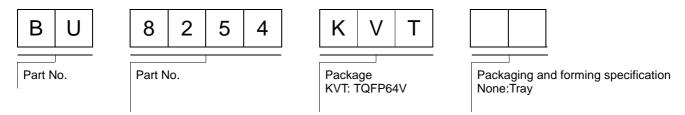
F.Bead : BLM18A-Series (Murata Manufacturing)

*4 : RS pin acts as VREF input pin when input voltage is set to half of high level signal input. We recommend to locate by-pass condenser near the RS pin.

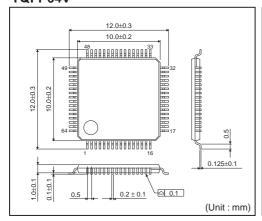


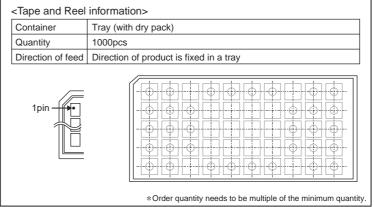
Example for LVCMOS(1.8V input)(R1,R2)=(1.5k Ω ,5.6k Ω)

Ordering Part Number



TQFP64V





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JAPAN	USA EU		CHINA
CLASSⅢ	CLASSⅢ	CLASS II b	CLASSIII
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