Low Duty LCD Segment Driver For Automotive COG Application

BU91R66CH-M Max 960 Segments (240SEG x 4COM)

Obsolete

General Description

BU91R66CH-M is a 1/4, 1/3, 1/2 Duty or Static COG type LCD driver that can be used for automotive applications and can drive up to 960 LCD Segments.
This driver can be cascaded up-to maximum of 4 drivers for larger LCD panel application.
It supports VA LCD displays, which has better optical performance with higher LCD voltage driving and higher frame frequency driving.
This driver includes read function for display data and command registers, wherein it is possible to detect malfunction due to noise.
It can also support other error detections such as interface checksum detection, glass breaking detection, logic error detection and SEG / COM toggle detection.
A defective mounting of COG can easily be controlled by using terminals to measure ITO resistance.
It can support operating temperature of up to +105 °C and compliant for AEC-Q100, as required for Automotive Application.

Features

- AEC-Q100 Compliant(Note 1)
- 1/4, 1/3, 1/2 Duty or Static Drive Selectable
  - 1/4 Duty Drive: Max 960 Segments
  - 1/3 Duty Drive: Max 720 Segments
  - 1/2 Duty Drive: Max 480 Segments
  - Static Drive: Max 240 Segments
- Integrated Buffer AMP for LCD Driving
- Integrated Oscillator Circuit and Software Programmable Frame Frequency from 66 Hz to 488 Hz
- Support External Clock Input
- Integrated EVR Function to Adjust LCD Contrast
- Integrated Power On Reset Circuit
- No External Components
- Low Power Consumption Design
- Support Display Inhibit Control
- Configurable COM Driving Order
- Support Max 4 Drivers Cascade Connection (BU91R64 / R65 / R66CH-M Available)
- Support Register and Display Data Read-back Function
- Support LCD Contact Resistance Measurement
- Support Error Detection and Status Read Function
  - Glass Breaking Detection
  - Interface Checksum
  - Logic Error Detection
  - SEG / COM Toggle Detection

(Note 1) Quality Information:
There is data when LSI was put on a temporary package.
Please use it as reference data.

Key Specifications

Supply Voltage Range:	+2.7 V to +6.0 V
LCD Drive Power Supply Range:	+2.7 V to +6.0 V
Operating Temperature Range:	-40 °C to +105 °C
Max Segments:	960 Segments
Display Duty:	1/4, 1/3, 1/2, Static Selectable
Bias:	1/2, 1/3 Selectable
Interface:	2-wire / 3-wire Serial Interface Selectable

Special Characteristics

ESD(HBM)(Note 2):	±2,000 V(Typ)
Latch-up Current(Note 2):	±100 mA(Typ)

(Note 2) There is data when LSI was put on a temporary package.

Applications

- Instrument Clusters
- Climate Controls
- Car Audios / Radios
- Meters
- White Goods
- Healthcare Products
- Battery Operated Applications

etc.

Package

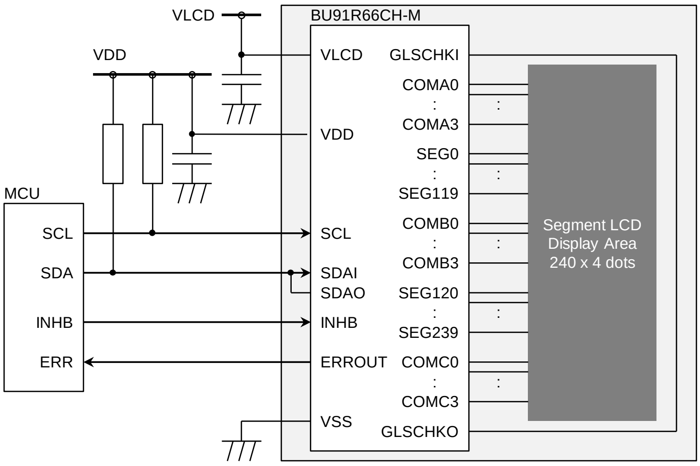
Au Bump Chip

〇Product structure : Silicon integrated circuit 〇This product has no designed protection against radioactive rays.

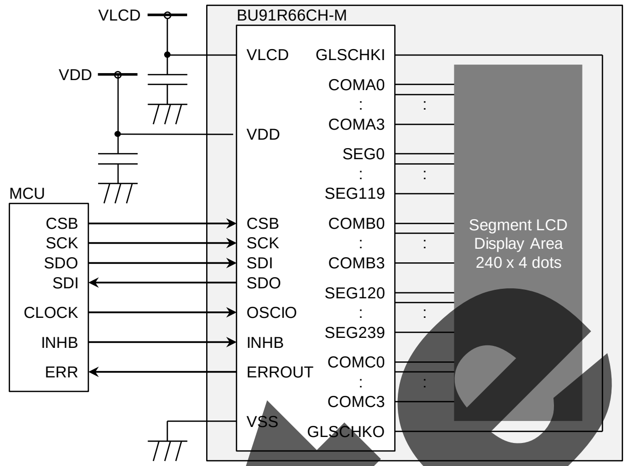
Contents

Typical Application Circuit

2-wire Serial Interface

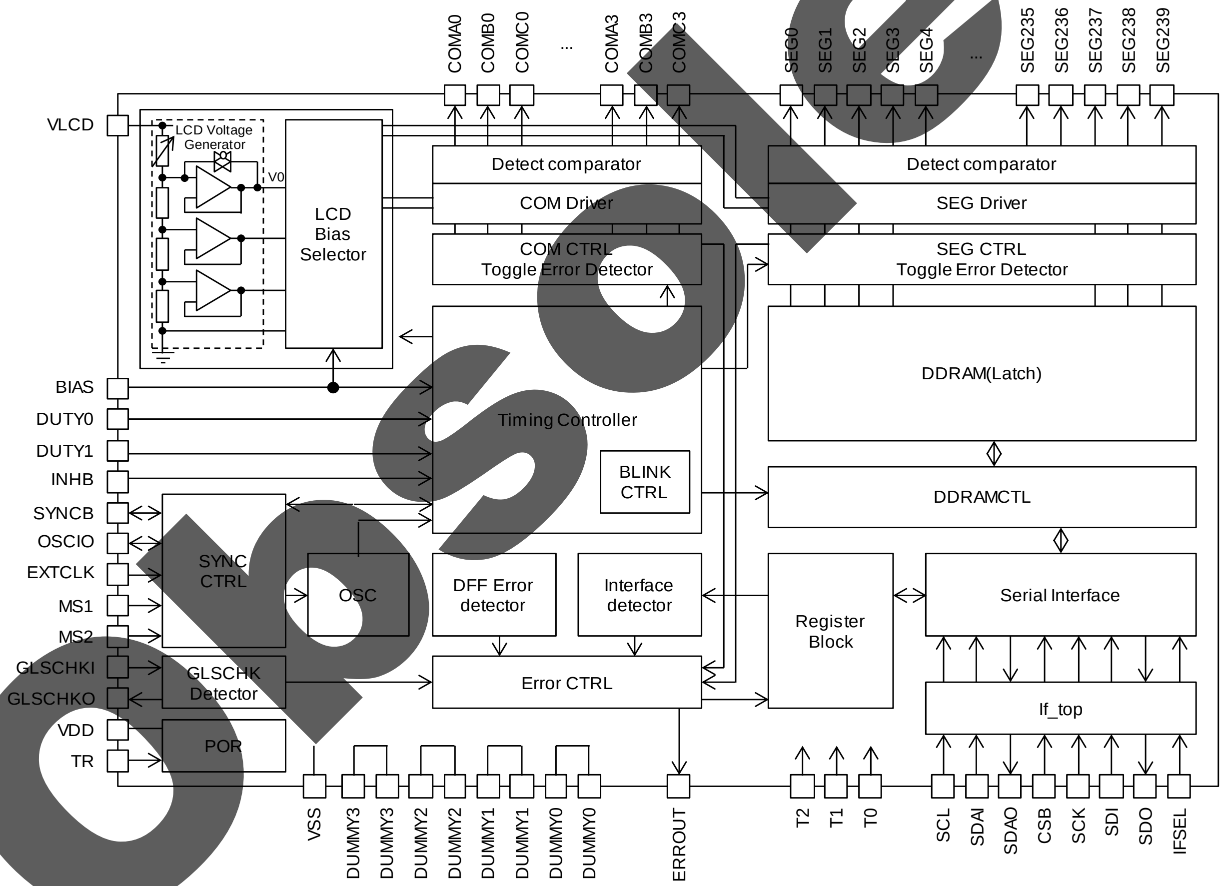


3-wire Serial Interface



Insert capacitance (C ≥ 0.1 µF) between VDD / VLCD and VSS

Block Diagram



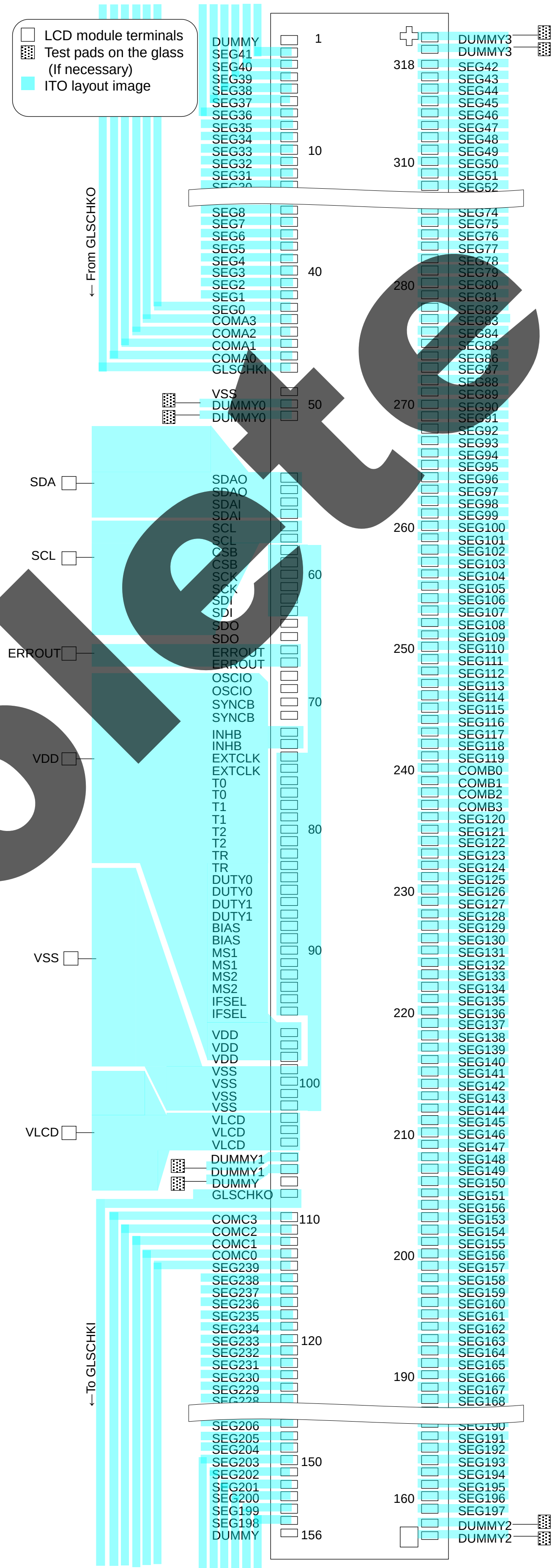
Terminal Description

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Handling when unused</th></tr>
<tr><td>VDD</td><td>I</td><td>Power supply for logic</td><td>-</td></tr>
<tr><td>VLCD</td><td>I</td><td>Power supply for LCD driving circuit</td><td>-</td></tr>
<tr><td>VSS</td><td>I</td><td>Ground</td><td>-</td></tr>
<tr><td>MS1</td><td>I</td><td rowspan="2">Single-/Multi-chip setting
<table>
<tr><th rowspan="2">MS2</th><th rowspan="2">MS1</th><th colspan="2">2-wire Interface</th><th>3-wire Interface</th></tr>
<tr><th>Function</th><th>Slave Address[7:1]</th><th>Function</th></tr>
<tr><td>VSS</td><td>VSS</td><td>Master</td><td>0111110 / 0111000</td><td>Master</td></tr>
<tr><td>VSS</td><td>VDD</td><td>Slave1</td><td>0111111 / 0111001</td><td>Slave1</td></tr>
<tr><td>VDD</td><td>VSS</td><td>Slave2</td><td>0111110 / 0111000</td><td>Slave2</td></tr>
<tr><td>VDD</td><td>VDD</td><td>Slave3</td><td>0111111 / 0111001</td><td>Slave3</td></tr>
</table></td><td>VDD / VSS</td></tr>
<tr><td>MS2</td><td>I</td><td>VDD / VSS</td></tr>
<tr><td>EXTCLK</td><td>I</td><td>Clock mode setting
VDD: External Clock Mode, VSS: Internal Clock Mode</td><td>VDD / VSS</td></tr>
<tr><td>OSCIO</td><td>I/O</td><td>Clock input / output setting
External Clock Mode: input of external clock
Internal Clock Mode: output of internal clock</td><td>OPEN</td></tr>
<tr><td>SYNCB</td><td>I/O</td><td>Synchronous signal input / output for multi-chip mode
Master: Synchronous signal output
Slave: master SYNCB signal input</td><td>OPEN</td></tr>
<tr><td>IFSEL</td><td>I</td><td>MCU Interface select
VDD: 3-wire Serial Interface
VSS: 2-wire Serial Interface</td><td>VDD / VSS</td></tr>
<tr><td>SDAI</td><td>I</td><td>Serial data input for 2-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SDAO</td><td>O</td><td>Serial data output for 2-wire Serial Interface</td><td>OPEN</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial clock for 2-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select for 3-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SCK</td><td>I</td><td>Serial clock for 3-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SDI</td><td>I</td><td>Serial data input for 3-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SDO</td><td>O</td><td>Serial data output for 3-wire Serial Interface</td><td>OPEN</td></tr>
<tr><td>INHB</td><td>I</td><td>Inhibit display status in spite of Display On by command setting
VDD: Keep display status by command setting
VSS: Inhibit display status. All SEG and COM terminals output VSS level.</td><td>VDD</td></tr>
<tr><td>DUTY0</td><td>I</td><td rowspan="2">Duty Drive select
<table>
<tr><th>DUTY1</th><th>DUTY0</th><th>Duty Drive</th></tr>
<tr><td>VSS</td><td>VSS</td><td>1/4 Duty Drive</td></tr>
<tr><td>VSS</td><td>VDD</td><td>1/3 Duty Drive</td></tr>
<tr><td>VDD</td><td>VSS</td><td>1/2 Duty Drive</td></tr>
<tr><td>VDD</td><td>VDD</td><td>Static Drive (also set to 1/1 Bias)</td></tr>
</table></td><td>VDD / VSS</td></tr>
<tr><td>DUTY1</td><td>I</td><td>VDD / VSS</td></tr>
<tr><td>BIAS</td><td>I</td><td>LCD Bias select
VDD: 1/2 Bias, VSS: 1/3 Bias (Static Drive: don’t care)</td><td>VDD / VSS</td></tr>
<tr><td>GLSCHKO</td><td>O</td><td>Output for glass breaking detection
Connect to GLSCHKI for glass breaking detection.</td><td>OPEN</td></tr>
<tr><td>GLSCHKI</td><td>I</td><td>Input for glass breaking detection
Connect to GLSCHKO for glass breaking detection.</td><td>VSS</td></tr>
<tr><td>ERROUT</td><td>O</td><td>Output data of error detection
VDD: Abnormal status, VSS: Normal status</td><td>OPEN</td></tr>
<tr><td>DUMMY0 to DUMMY3</td><td>-</td><td>Can be used for the contact resistance measurement.</td><td>OPEN</td></tr>
<tr><td>DUMMY</td><td>-</td><td>Open</td><td>OPEN</td></tr>
<tr><td>TR</td><td>I</td><td>POR enable setting(Note 1)
VDD: POR disable, VSS: POR enable</td><td>VSS</td></tr>
<tr><td>T0, T1, T2</td><td>I</td><td>Test input (ROHM use only)
Must be connected to VSS.</td><td>VSS</td></tr>
<tr><td>SEG0 to SEG239</td><td>O</td><td>Segment output for LCD driving</td><td>OPEN</td></tr>
<tr><td>COMA0 to COMA3</td><td>O</td><td>Common output for LCD driving</td><td>OPEN</td></tr>
<tr><td>COMB0 to COMB3</td><td>O</td><td>Common output for LCD driving</td><td>OPEN</td></tr>
<tr><td>COMC0 to COMC3</td><td>O</td><td>Common output for LCD driving</td><td>OPEN</td></tr>
</table>

(Note 1) This function is guaranteed by design, not tested in production process. Software Reset is necessary to initialize IC in case of TR = VDD.

Recommended ITO Layout

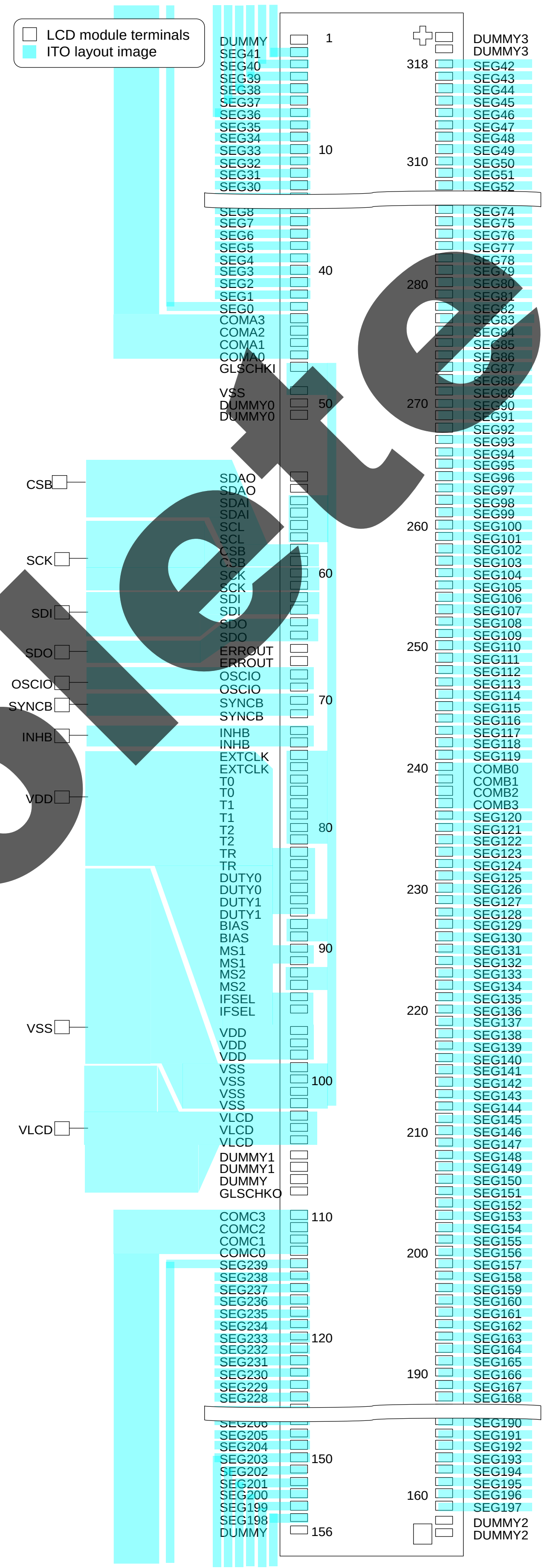
Function	Setting
POR	USE TR = VSS
Error Detection	YES (Glass Breaking Detection, Contact Resistance Check)
Multi-chip Mode	NO
Duty Drive	1/4 Duty Drive (DUTY0, DUTY1) = (VSS, VSS)
Bias Setting	1/3 Bias BIAS = VSS
I/F	2-wire Serial Interface IFSEL = VSS
Clock Mode	Internal Clock Mode EXTCLK = VSS
Master/Slave	Master (MS1, MS2) = (VSS, VSS)
Inhibit Function	NO INHB = VDD



(Bump side up)

Recommended ITO Layout – continued

Function	Setting
POR	Not USE TR = VDD
Error Detection	NO
Multi-chip Mode	YES
Duty Drive	Static Drive (DUTY0, DUTY1) = (VDD, VDD)
Bias Setting	Static Drive BIAS = VSS
I/F	3-wire Serial Interface IFSEL = VDD
Clock Mode	Internal Clock Mode EXTCLK = VSS
Master/Slave	Slave1 (MS1, MS2) = (VDD, VSS)
Inhibit Function	YES INHB = MCU control



(Bump side up)

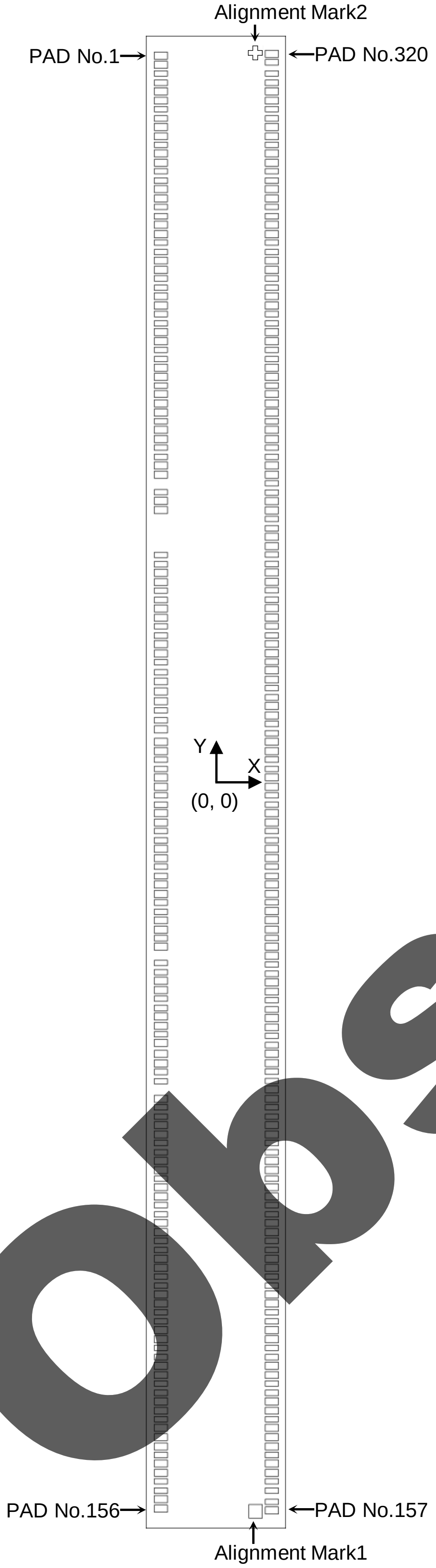
Recommended ITO Layout – continued

Terminal Resistance

PAD No.	Terminal Name	Maximum Resistance
52, 53	SDAO	1,500 Ω
54, 55	SDAI	1,500 Ω
56, 57	SCL	1,500 Ω
58, 59	CSB	1,500 Ω
60, 61	SCK	1,500 Ω
62, 63	SDI	1,500 Ω
64, 65	SDO	1,500 Ω
66, 67	ERROUT	1,500 Ω
68, 69	OSCIO	1,500 Ω
70, 71	SYNCB	1,500 Ω
72, 73	INHB	1,500 Ω
96 to 98	VDD	400 Ω
99 to 102	VSS	400 Ω
103 to 105	VLCD	400 Ω

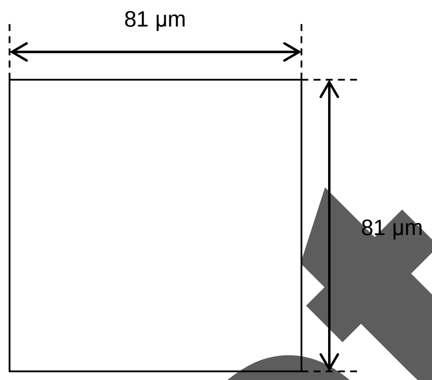
Refer to Glass Breaking Detection for GLSCHKI and GLSCHKO terminal resistance.

PAD Arrangement



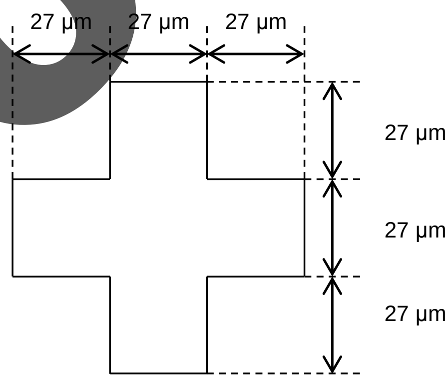
(Bump side up)

Alignment Mark 1



Mark Center Coordinates
(X,Y) = (226.00, -4175.00)

Alignment Mark 2



Mark Center Coordinates
(X,Y) = (226.00, 4175.00)

The origin of X/Y coordinates is the center of the chip with bump side up.

Dimension

Table 1. Dimension (Completion Size)

Mark		Topic	Specification Limit
Chip Size X		Chip Size: X Direction	785 µm ± 40 µm
Chip Size Y		Chip Size: Y Direction	8,515 µm ± 40 µm
Chip Thickness		Chip Thickness	300 µm ± 20 µm
PAD	A (PAD No. 1 to PAD No. 320)	Bump Size: X Direction	75 µm ± 3.0 µm
	B (PAD No. 1 to PAD No. 320)	Bump Size: Y Direction	36.0 µm ± 3.0 µm
	C (PAD No. 1 to PAD No. 320)	Average of Bump Height	15.0 µm ± 3.0 µm

Refer to **PAD Arrangement** for the definition of X/Y coordinates.

Table 2. Bump Specs and Dimensions

Topic	Specification Limit
Bump Structure	Straight Bump
Bump Co-planarity on Chip	3.0 µm or less
Bump Hardness (Microvicker's Meter)	50 HV ± 20 HV
Bump Strength	7.35 mg/µm^2 or more

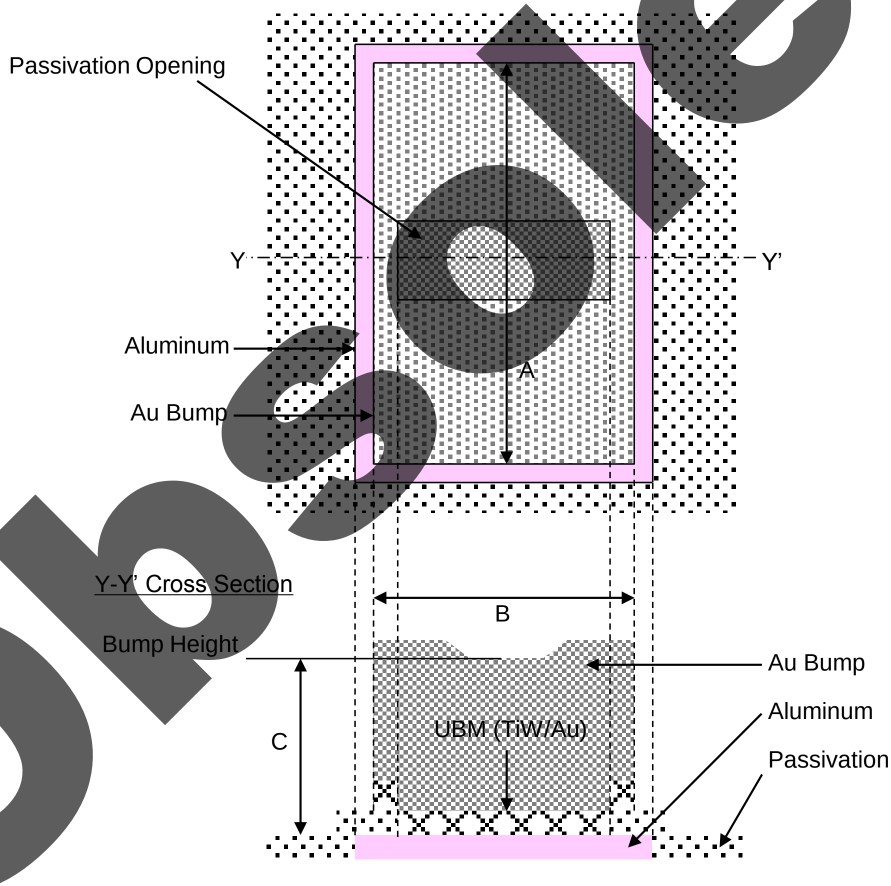


Figure 1. PAD / Bump Information

PAD Coordinates

Unit: µm

PAD No	Terminal Name	Bump Center X	Bump Center Y	Bump Size X	Bump Size Y
1	DUMMY	-320.50	4156.50	75	36
2	SEG41	-320.50	4105.50	75	36
3	SEG40	-320.50	4054.50	75	36
4	SEG39	-320.50	4003.50	75	36
5	SEG38	-320.50	3952.50	75	36
6	SEG37	-320.50	3901.50	75	36
7	SEG36	-320.50	3850.50	75	36
8	SEG35	-320.50	3799.50	75	36
9	SEG34	-320.50	3748.50	75	36
10	SEG33	-320.50	3697.50	75	36
11	SEG32	-320.50	3646.50	75	36
12	SEG31	-320.50	3595.50	75	36
13	SEG30	-320.50	3544.50	75	36
14	SEG29	-320.50	3493.50	75	36
15	SEG28	-320.50	3442.50	75	36
16	SEG27	-320.50	3391.50	75	36
17	SEG26	-320.50	3340.50	75	36
18	SEG25	-320.50	3289.50	75	36
19	SEG24	-320.50	3238.50	75	36
20	SEG23	-320.50	3187.50	75	36
21	SEG22	-320.50	3136.50	75	36
22	SEG21	-320.50	3085.50	75	36
23	SEG20	-320.50	3034.50	75	36
24	SEG19	-320.50	2983.50	75	36
25	SEG18	-320.50	2932.50	75	36
26	SEG17	-320.50	2881.50	75	36
27	SEG16	-320.50	2830.50	75	36
28	SEG15	-320.50	2779.50	75	36
29	SEG14	-320.50	2728.50	75	36
30	SEG13	-320.50	2677.50	75	36
31	SEG12	-320.50	2626.50	75	36
32	SEG11	-320.50	2575.50	75	36
33	SEG10	-320.50	2524.50	75	36
34	SEG9	-320.50	2473.50	75	36
35	SEG8	-320.50	2422.50	75	36
36	SEG7	-320.50	2371.50	75	36
37	SEG6	-320.50	2320.50	75	36
38	SEG5	-320.50	2269.50	75	36
39	SEG4	-320.50	2218.50	75	36
40	SEG3	-320.50	2167.50	75	36
41	SEG2	-320.50	2116.50	75	36
42	SEG1	-320.50	2065.50	75	36
43	SEG0	-320.50	2014.50	75	36
44	COMA3	-320.50	1963.50	75	36
45	COMA2	-320.50	1912.50	75	36
46	COMA1	-320.50	1861.50	75	36
47	COMA0	-320.50	1810.50	75	36
48	GLSCHKI	-320.50	1759.50	75	36
49	VSS	-320.50	1659.50	75	36
50	DUMMY0	-320.50	1608.50	75	36
51	DUMMY0	-320.50	1557.50	75	36
52	SDAO	-320.50	1298.80	75	36
53	SDAO	-320.50	1247.80	75	36
54	SDAI	-320.50	1196.80	75	36
55	SDAI	-320.50	1145.80	75	36
56	SCL	-320.50	1094.80	75	36
57	SCL	-320.50	1043.80	75	36
58	CSB	-320.50	992.80	75	36
59	CSB	-320.50	941.80	75	36
60	SCK	-320.50	890.80	75	36

PAD No	Terminal Name	Bump Center X	Bump Center Y	Bump Size X	Bump Size Y
61	SCK	-320.50	839.80	75	36
62	SDI	-320.50	788.80	75	36
63	SDI	-320.50	737.80	75	36
64	SDO	-320.50	685.05	75	36
65	SDO	-320.50	630.05	75	36
66	ERROUT	-320.50	575.05	75	36
67	ERROUT	-320.50	520.05	75	36
68	OSCIO	-320.50	465.05	75	36
69	OSCIO	-320.50	410.05	75	36
70	SYNCB	-320.50	355.05	75	36
71	SYNCB	-320.50	300.05	75	36
72	INHB	-320.50	228.85	75	36
73	INHB	-320.50	177.85	75	36
74	EXTCLK	-320.50	126.85	75	36
75	EXTCLK	-320.50	75.85	75	36
76	T0	-320.50	24.85	75	36
77	T0	-320.50	-26.15	75	36
78	T1	-320.50	-77.15	75	36
79	T1	-320.50	-128.15	75	36
80	T2	-320.50	-179.15	75	36
81	T2	-320.50	-230.15	75	36
82	TR	-320.50	-281.15	75	36
83	TR	-320.50	-332.15	75	36
84	DUTY0	-320.50	-383.15	75	36
85	DUTY0	-320.50	-434.15	75	36
86	DUTY1	-320.50	-485.15	75	36
87	DUTY1	-320.50	-536.15	75	36
88	BIAS	-320.50	-587.15	75	36
89	BIAS	-320.50	-638.15	75	36
90	MS1	-320.50	-689.15	75	36
91	MS1	-320.50	-740.15	75	36
92	MS2	-320.50	-791.15	75	36
93	MS2	-320.50	-842.15	75	36
94	IFSEL	-320.50	-893.15	75	36
95	IFSEL	-320.50	-944.15	75	36
96	VDD	-320.50	-1035.55	75	36
97	VDD	-320.50	-1086.55	75	36
98	VDD	-320.50	-1137.55	75	36
99	VSS	-320.50	-1188.55	75	36
100	VSS	-320.50	-1239.55	75	36
101	VSS	-320.50	-1290.55	75	36
102	VSS	-320.50	-1341.55	75	36
103	VLCD	-320.50	-1392.55	75	36
104	VLCD	-320.50	-1443.55	75	36
105	VLCD	-320.50	-1494.55	75	36
106	DUMMY1	-320.50	-1557.50	75	36
107	DUMMY1	-320.50	-1608.50	75	36
108	DUMMY	-320.50	-1659.50	75	36
109	GLSCHKO	-320.50	-1710.50	75	36
110	COMC3	-320.50	-1810.50	75	36
111	COMC2	-320.50	-1861.50	75	36
112	COMC1	-320.50	-1912.50	75	36
113	COMC0	-320.50	-1963.50	75	36
114	SEG239	-320.50	-2014.50	75	36
115	SEG238	-320.50	-2065.50	75	36
116	SEG237	-320.50	-2116.50	75	36
117	SEG236	-320.50	-2167.50	75	36
118	SEG235	-320.50	-2218.50	75	36
119	SEG234	-320.50	-2269.50	75	36
120	SEG233	-320.50	-2320.50	75	36

Refer to **PAD Arrangement** for the definition of X/Y coordinates.

PAD Coordinates – continued

Unit: μm

PAD No	Terminal Name	Bump Center X	Bump Center Y	Bump Size X	Bump Size Y
121	SEG232	-320.50	-2371.50	75	36
122	SEG231	-320.50	-2422.50	75	36
123	SEG230	-320.50	-2473.50	75	36
124	SEG229	-320.50	-2524.50	75	36
125	SEG228	-320.50	-2575.50	75	36
126	SEG227	-320.50	-2626.50	75	36
127	SEG226	-320.50	-2677.50	75	36
128	SEG225	-320.50	-2728.50	75	36
129	SEG224	-320.50	-2779.50	75	36
130	SEG223	-320.50	-2830.50	75	36
131	SEG222	-320.50	-2881.50	75	36
132	SEG221	-320.50	-2932.50	75	36
133	SEG220	-320.50	-2983.50	75	36
134	SEG219	-320.50	-3034.50	75	36
135	SEG218	-320.50	-3085.50	75	36
136	SEG217	-320.50	-3136.50	75	36
137	SEG216	-320.50	-3187.50	75	36
138	SEG215	-320.50	-3238.50	75	36
139	SEG214	-320.50	-3289.50	75	36
140	SEG213	-320.50	-3340.50	75	36
141	SEG212	-320.50	-3391.50	75	36
142	SEG211	-320.50	-3442.50	75	36
143	SEG210	-320.50	-3493.50	75	36
144	SEG209	-320.50	-3544.50	75	36
145	SEG208	-320.50	-3595.50	75	36
146	SEG207	-320.50	-3646.50	75	36
147	SEG206	-320.50	-3697.50	75	36
148	SEG205	-320.50	-3748.50	75	36
149	SEG204	-320.50	-3799.50	75	36
150	SEG203	-320.50	-3850.50	75	36
151	SEG202	-320.50	-3901.50	75	36
152	SEG201	-320.50	-3952.50	75	36
153	SEG200	-320.50	-4003.50	75	36
154	SEG199	-320.50	-4054.50	75	36
155	SEG198	-320.50	-4105.50	75	36
156	DUMMY	-320.50	-4156.50	75	36
157	DUMMY2	320.50	-4168.60	75	36
158	DUMMY2	320.50	-4117.60	75	36
159	SEG197	320.50	-4054.50	75	36
160	SEG196	320.50	-4003.50	75	36
161	SEG195	320.50	-3952.50	75	36
162	SEG194	320.50	-3901.50	75	36
163	SEG193	320.50	-3850.50	75	36
164	SEG192	320.50	-3799.50	75	36
165	SEG191	320.50	-3748.50	75	36
166	SEG190	320.50	-3697.50	75	36
167	SEG189	320.50	-3646.50	75	36
168	SEG188	320.50	-3595.50	75	36
169	SEG187	320.50	-3544.50	75	36
170	SEG186	320.50	-3493.50	75	36
171	SEG185	320.50	-3442.50	75	36
172	SEG184	320.50	-3391.50	75	36
173	SEG183	320.50	-3340.50	75	36
174	SEG182	320.50	-3289.50	75	36
175	SEG181	320.50	-3238.50	75	36
176	SEG180	320.50	-3187.50	75	36
177	SEG179	320.50	-3136.50	75	36
178	SEG178	320.50	-3085.50	75	36
179	SEG177	320.50	-3034.50	75	36
180	SEG176	320.50	-2983.50	75	36

PAD No	Terminal Name	Bump Center X	Bump Center Y	Bump Size X	Bump Size Y
181	SEG175	320.50	-2932.50	75	36
182	SEG174	320.50	-2881.50	75	36
183	SEG173	320.50	-2830.50	75	36
184	SEG172	320.50	-2779.50	75	36
185	SEG171	320.50	-2728.50	75	36
186	SEG170	320.50	-2677.50	75	36
187	SEG169	320.50	-2626.50	75	36
188	SEG168	320.50	-2575.50	75	36
189	SEG167	320.50	-2524.50	75	36
190	SEG166	320.50	-2473.50	75	36
191	SEG165	320.50	-2422.50	75	36
192	SEG164	320.50	-2371.50	75	36
193	SEG163	320.50	-2320.50	75	36
194	SEG162	320.50	-2269.50	75	36
195	SEG161	320.50	-2218.50	75	36
196	SEG160	320.50	-2167.50	75	36
197	SEG159	320.50	-2116.50	75	36
198	SEG158	320.50	-2065.50	75	36
199	SEG157	320.50	-2014.50	75	36
200	SEG156	320.50	-1963.50	75	36
201	SEG155	320.50	-1912.50	75	36
202	SEG154	320.50	-1861.50	75	36
203	SEG153	320.50	-1810.50	75	36
204	SEG152	320.50	-1759.50	75	36
205	SEG151	320.50	-1708.50	75	36
206	SEG150	320.50	-1657.50	75	36
207	SEG149	320.50	-1606.50	75	36
208	SEG148	320.50	-1555.50	75	36
209	SEG147	320.50	-1504.50	75	36
210	SEG146	320.50	-1453.50	75	36
211	SEG145	320.50	-1402.50	75	36
212	SEG144	320.50	-1351.50	75	36
213	SEG143	320.50	-1300.50	75	36
214	SEG142	320.50	-1249.50	75	36
215	SEG141	320.50	-1198.50	75	36
216	SEG140	320.50	-1147.50	75	36
217	SEG139	320.50	-1096.50	75	36
218	SEG138	320.50	-1045.50	75	36
219	SEG137	320.50	-994.50	75	36
220	SEG136	320.50	-943.50	75	36
221	SEG135	320.50	-892.50	75	36
222	SEG134	320.50	-841.50	75	36
223	SEG133	320.50	-790.50	75	36
224	SEG132	320.50	-739.50	75	36
225	SEG131	320.50	-688.50	75	36
226	SEG130	320.50	-637.50	75	36
227	SEG129	320.50	-586.50	75	36
228	SEG128	320.50	-535.50	75	36
229	SEG127	320.50	-484.50	75	36
230	SEG126	320.50	-433.50	75	36
231	SEG125	320.50	-382.50	75	36
232	SEG124	320.50	-331.50	75	36
233	SEG123	320.50	-280.50	75	36
234	SEG122	320.50	-229.50	75	36
235	SEG121	320.50	-178.50	75	36
236	SEG120	320.50	-127.50	75	36
237	COMB3	320.50	-76.50	75	36
238	COMB2	320.50	-25.50	75	36
239	COMB1	320.50	25.50	75	36
240	COMB0	320.50	76.50	75	36

Refer to **PAD Arrangement** for the definition of X/Y coordinates.

PAD Coordinates – continued

Unit µm

PAD No	Terminal Name	Bump Center X	Bump Center Y	Bump Size X	Bump Size Y
241	SEG119	320.50	127.50	75	36
242	SEG118	320.50	178.50	75	36
243	SEG117	320.50	229.50	75	36
244	SEG116	320.50	280.50	75	36
245	SEG115	320.50	331.50	75	36
246	SEG114	320.50	382.50	75	36
247	SEG113	320.50	433.50	75	36
248	SEG112	320.50	484.50	75	36
249	SEG111	320.50	535.50	75	36
250	SEG110	320.50	586.50	75	36
251	SEG109	320.50	637.50	75	36
252	SEG108	320.50	688.50	75	36
253	SEG107	320.50	739.50	75	36
254	SEG106	320.50	790.50	75	36
255	SEG105	320.50	841.50	75	36
256	SEG104	320.50	892.50	75	36
257	SEG103	320.50	943.50	75	36
258	SEG102	320.50	994.50	75	36
259	SEG101	320.50	1045.50	75	36
260	SEG100	320.50	1096.50	75	36
261	SEG99	320.50	1147.50	75	36
262	SEG98	320.50	1198.50	75	36
263	SEG97	320.50	1249.50	75	36
264	SEG96	320.50	1300.50	75	36
265	SEG95	320.50	1351.50	75	36
266	SEG94	320.50	1402.50	75	36
267	SEG93	320.50	1453.50	75	36
268	SEG92	320.50	1504.50	75	36
269	SEG91	320.50	1555.50	75	36
270	SEG90	320.50	1606.50	75	36
271	SEG89	320.50	1657.50	75	36
272	SEG88	320.50	1708.50	75	36
273	SEG87	320.50	1759.50	75	36
274	SEG86	320.50	1810.50	75	36
275	SEG85	320.50	1861.50	75	36
276	SEG84	320.50	1912.50	75	36
277	SEG83	320.50	1963.50	75	36
278	SEG82	320.50	2014.50	75	36
279	SEG81	320.50	2065.50	75	36
280	SEG80	320.50	2116.50	75	36
281	SEG79	320.50	2167.50	75	36
282	SEG78	320.50	2218.50	75	36
283	SEG77	320.50	2269.50	75	36
284	SEG76	320.50	2320.50	75	36
285	SEG75	320.50	2371.50	75	36
286	SEG74	320.50	2422.50	75	36
287	SEG73	320.50	2473.50	75	36
288	SEG72	320.50	2524.50	75	36
289	SEG71	320.50	2575.50	75	36
290	SEG70	320.50	2626.50	75	36
291	SEG69	320.50	2677.50	75	36
292	SEG68	320.50	2728.50	75	36
293	SEG67	320.50	2779.50	75	36
294	SEG66	320.50	2830.50	75	36
295	SEG65	320.50	2881.50	75	36
296	SEG64	320.50	2932.50	75	36
297	SEG63	320.50	2983.50	75	36
298	SEG62	320.50	3034.50	75	36
299	SEG61	320.50	3085.50	75	36
300	SEG60	320.50	3136.50	75	36
301	SEG59	320.50	3187.50	75	36
302	SEG58	320.50	3238.50	75	36
303	SEG57	320.50	3289.50	75	36
304	SEG56	320.50	3340.50	75	36
305	SEG55	320.50	3391.50	75	36
306	SEG54	320.50	3442.50	75	36
307	SEG53	320.50	3493.50	75	36
308	SEG52	320.50	3544.50	75	36
309	SEG51	320.50	3595.50	75	36
310	SEG50	320.50	3646.50	75	36
311	SEG49	320.50	3697.50	75	36
312	SEG48	320.50	3748.50	75	36
313	SEG47	320.50	3799.50	75	36
314	SEG46	320.50	3850.50	75	36
315	SEG45	320.50	3901.50	75	36
316	SEG44	320.50	3952.50	75	36
317	SEG43	320.50	4003.50	75	36
318	SEG42	320.50	4054.50	75	36
319	DUMMY3	320.50	4117.60	75	36
320	DUMMY3	320.50	4168.60	75	36

Refer to PAD Arrangement for the definition of X/Y coordinates.

Absolute Maximum Ratings (VSS = 0 V)

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Maximum Voltage1	VDD	-0.5	-	+7.0	V	Power Supply
Supply Current1	I_{VDD}	-5	-	+5	mA	For VDD
Maximum Voltage2	VLCD	-0.5	-	+7.0	V	LCD Drive Voltage
Supply Current2	I_{VLCD}	-5	-	+5	mA	For VLCD
Input Voltage Range	V_{IN}	-0.5	-	+7.0	V	-
Output Voltage Range	V_{OUT}	-0.5	-	+7.0	V	-
Human Body Model (HBM) *(Note 1), (Note 2)*	V_{ESD}	-	±2,000	-	V	-
Latch-up Current *(Note 1), (Note 3)*	I_{LU}	-	±100	-	mA	-
Maximum Junction Temperature	Tjmax	-55	-	+125	°C	-
Storage Temperature Range	Tstg	-55	-	+125	°C	-

(Note 1) Not 100 % tested. There is data when LSI was put on a temporary package. Use as a reference data.
(Note 2) Testing standards: JESD22-A114E
(Note 3) Testing standards: JESD78
Caution : *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Recommended Operating Conditions

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Operational Temperature	Topr	-40	-	+105	°C	-
Power Supply Voltage 1	VDD	2.7	-	6.0	V	Power Supply
Power Supply Voltage 2	VLCD	2.7	-	6.0	V	LCD Drive Voltage

Electrical Characteristics

DC Characteristics

(Unless otherwise specified, Ta = -40 °C to +105 °C, VDD / VLCD = 2.7 V to 6.0 V, VSS = 0 V)

Parameter		Symbol	Limits			Unit	Condition
			Min	Typ	Max		
"H" Level Input Voltage1		V_{IH1}	0.7VDD	-	VDD	V	SCL, SDAI
"L" Level Input Voltage1		V_{IL1}	VSS	-	0.3VDD	V	
"H" Level Input Voltage2		V_{IH2}	0.8VDD	-	VDD	V	CSB, SCK, SDI, INHB, OSCIO *(Note)*
"L" Level Input Voltage2		V_{IL2}	0	-	0.2VDD	V	
"H" Level Input Current		I_{IH}	-	-	1	µA	SCL, SDAI, CSB, SCK, SDI, INHB, OSCIO, TR, MS1, MS2, EXTCLK, IFSEL, DUTY0, DUTY1, BIAS, GLSCHKI
"L" Level Input Current		I_{IL}	-1	-	-	µA	
"H" Level Output Voltage1		V_{OH1}	VDD-0.9	-	VDD	V	SDO, ERROUT (I_{LOAD} = -1 mA)
"L" Level Output Voltage1		V_{OL1}	VSS	-	0.9	V	SDO, ERROUT (I_{LOAD} = +1 mA)
"L" Level Output Voltage2		V_{OL2}	VSS	-	0.4	V	SDAO (I_{LOAD} = +3 mA)
LCD Driver On Resistance	SEG	R_{ON1}	-	3	-	kΩ	I_{LOAD} = ±10 µA
	COM	R_{ON2}	-	3	-	kΩ	
Standby Current		I_{VDD1}	-	-	5.0	µA	Display Off (DISPOFF), Oscillation stop
		I_{VLCD1}	-	-	5.0	µA	
Operating Current		I_{VDD2}	-	0.7	20.0	µA	VDD = 5.0 V, VLCD = 5.0 V, Ta = +25 °C, 1/4 Duty Drive, 1/3 Bias Frame Inversion FR = 142.4 Hz setting (External Clock = 3.42 kHz) All outputs are open.
		I_{VLCD2}	-	15.0	60.0	µA	

(Note) For External Clock Mode and slave mode.

[Reference Data]

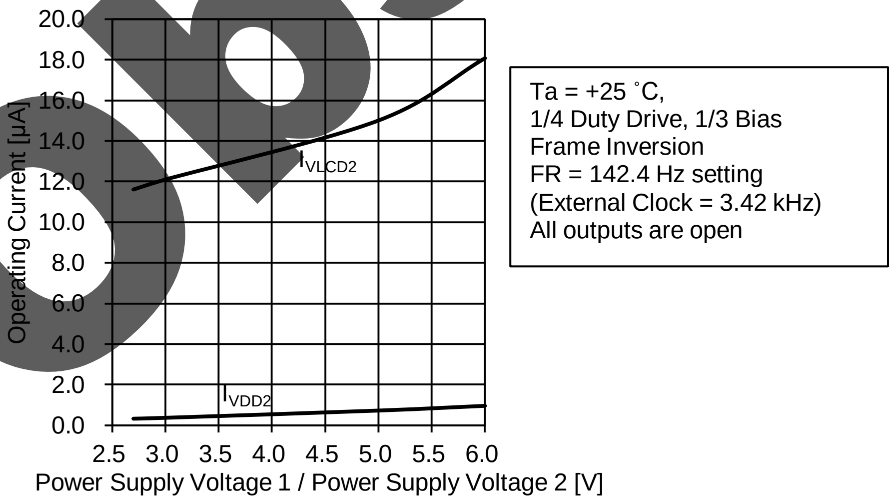


Figure 2. Operating Current vs Power Supply Voltage

Electrical Characteristics – continued

Oscillation Characteristics

(Unless otherwise specified, Ta = -40 °C to +105 °C, VDD / VLCD = 2.7 V to 6.0 V, VSS = 0 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Frame Frequency 1	f_{CLK1}	99.7	142.4	185.1	Hz	MODESET3 P0 = “0”, FRSET(P2 to P0) = “101” (142.4 Hz setting) VDD = 2.7 V to 6.0 V, Ta = -40 °C to +105 °C
Frame Frequency 2	f_{CLK2}	128.2	142.4	156.6	Hz	MODESET3 P0 = “0”, FRSET(P2 to P0) = “101” (142.4 Hz setting) VDD = 5.0 V, Ta = -40 °C to +105 °C
External Clock Rise Time	tr_{CLK}	-	-	0.3	µs	External Clock Mode
External Clock Fall Time	tf_{CLK}	-	-	0.3	µs	
External Clock Frequency	f_{CLK3}	800	-	12,000	Hz	
External Clock Duty	t_{DTY}	30	50	70	%	
Frame Frequency Range in External Clock Mode	f_{FRAME}	33	-	500	Hz	

Keep Frame Frequency range from 33 Hz to 500 Hz in case of External Clock Mode, also keep external clock frequency range from 800 Hz to 12,000 Hz.
The calculation formula is shown in **5. Frame Rate Set (FRSET)**.

[Reference Data]

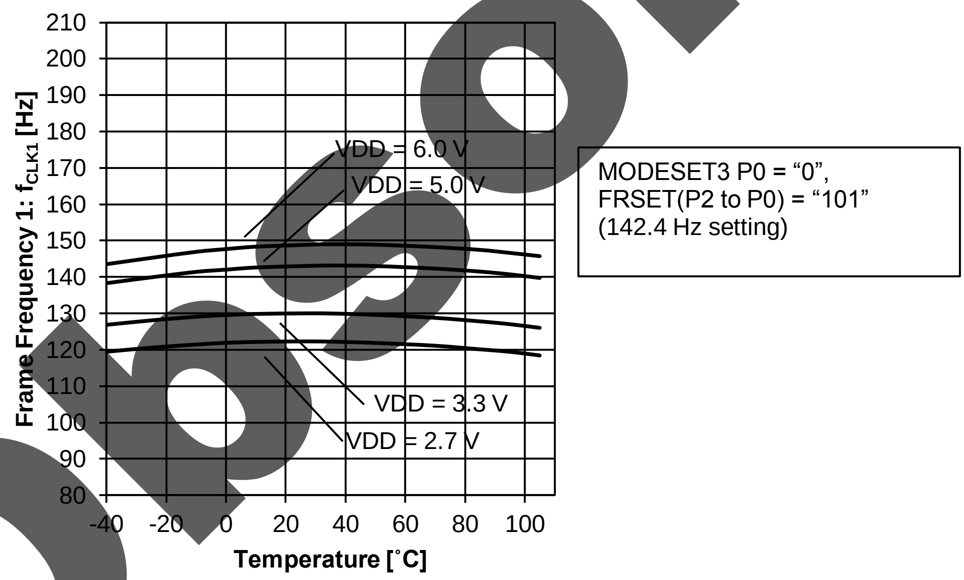


Figure 3. Frame Frequency vs Temperature

Electrical Characteristics – continued

2-wire Serial Interface Characteristics

(Unless otherwise specified, Ta = -40 °C to +105 °C, VDD = 2.7 V to 6.0 V, VSS = 0 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input Rise Time	tr	-	-	0.3	µs	-
Input Fall Time	tf	-	-	0.3	µs	-
SCL Cycle Time	t_{CYC}	2.5	-	-	µs	-
“H” Level SCL Pulse Width	t_{SHW}	0.6	-	-	µs	-
“L” Level SCL Pulse Width	t_{SLW}	1.3	-	-	µs	-
SDA Setup Time	t_{SDS}	0.1	-	-	µs	-
SDA Hold Time	t_{SDH}	0.1	-	-	µs	-
Bus Free Time	t_{BUF}	1.3	-	-	µs	-
START Condition Hold Time	$t_{HD;STA}$	0.6	-	-	µs	-
START Condition Setup Time	$t_{SU;STA}$	0.6	-	-	µs	-
STOP Condition Setup Time	$t_{SU;STO}$	0.6	-	-	µs	-

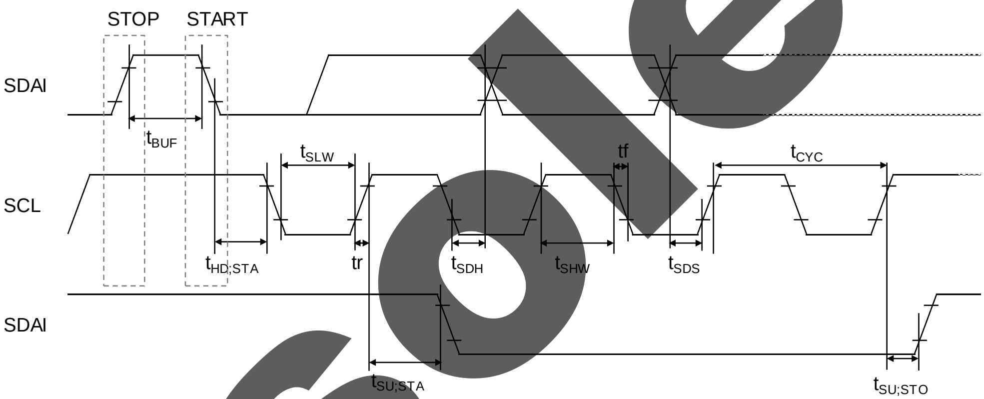
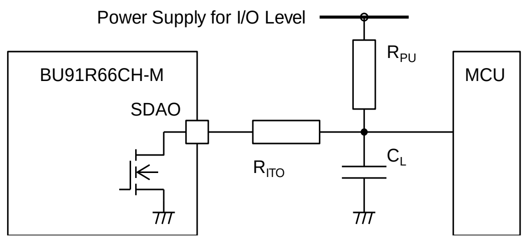


Figure 4. Interface Timing of 2-wire Serial Interface

Since SDAO is an open-drain output, Read access time depends on ITO resistance R_{ITO}, Pull-up resistance R_{PU} and load capacitance C_L.

R_{ITO}: ITO resistance on the LCD glass. (Any component is not necessary to be attached.)
R_{PU}: Pull-up resistance on PCB. 1 kΩ ≤ R_{PU} ≤ 10 kΩ is recommended.
C_L: A parasitic capacitance to VSS in an application circuit. (Any component is not necessary to be attached.)

R_{PU} should be determined with consideration of V_{IL} in MCU side.



Electrical Characteristics – continued

3-wire Serial Interface Characteristics

(Unless otherwise specified, Ta = -40 °C to +105 °C, VDD = 2.7 V to 6.0 V, VSS = 0 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input Rise Time	tr	-	-	80	ns	-
Input Fall Time	tf	-	-	80	ns	-
SCK Cycle Time	t_{SCYC}	400	-	-	ns	-
"H" Level SCK Pulse Width (Write)	t_{SHWW}	120	-	-	ns	Write Access
"H" Level SCK Pulse Width (Read)	t_{SHWR}	200	-	-	ns	Read Access
"L" Level SCK Pulse Width (Write)	t_{SLWW}	120	-	-	ns	Write Access
"L" Level SCK Pulse Width (Read)	t_{SLWR}	1.6	-	-	µs	Read Access
SDI Setup Time	t_{SDS}	120	-	-	ns	-
SDI Hold Time	t_{SDH}	120	-	-	ns	-
CSB Setup Time	t_{CSS}	120	-	-	ns	-
CSB Hold Time	t_{CSH}	120	-	-	ns	-
"H" CSB Pulse Width	t_{CHW}	120	-	-	ns	-
SDO Output Delay Time	t_{DC}	-	-	1.5	µs	R_{ITO} = 1.0 kΩ, C_L = 10 pF
SDO Rise Time	t_{DR}	-	-	1.5	µs	R_{ITO} = 1.0 kΩ, C_L = 10 pF

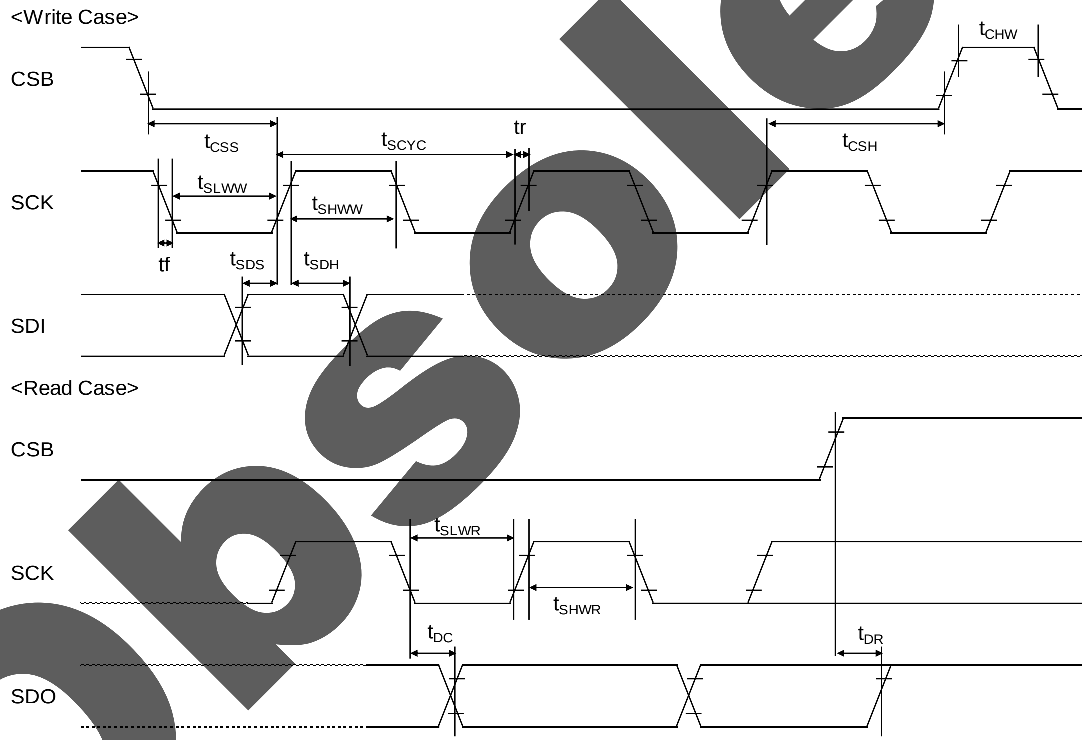
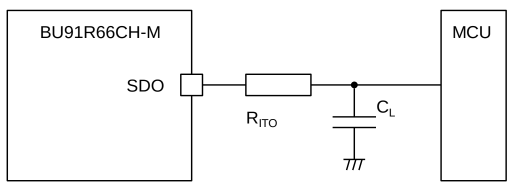


Figure 5. Interface Timing of 3-wire Serial Interface

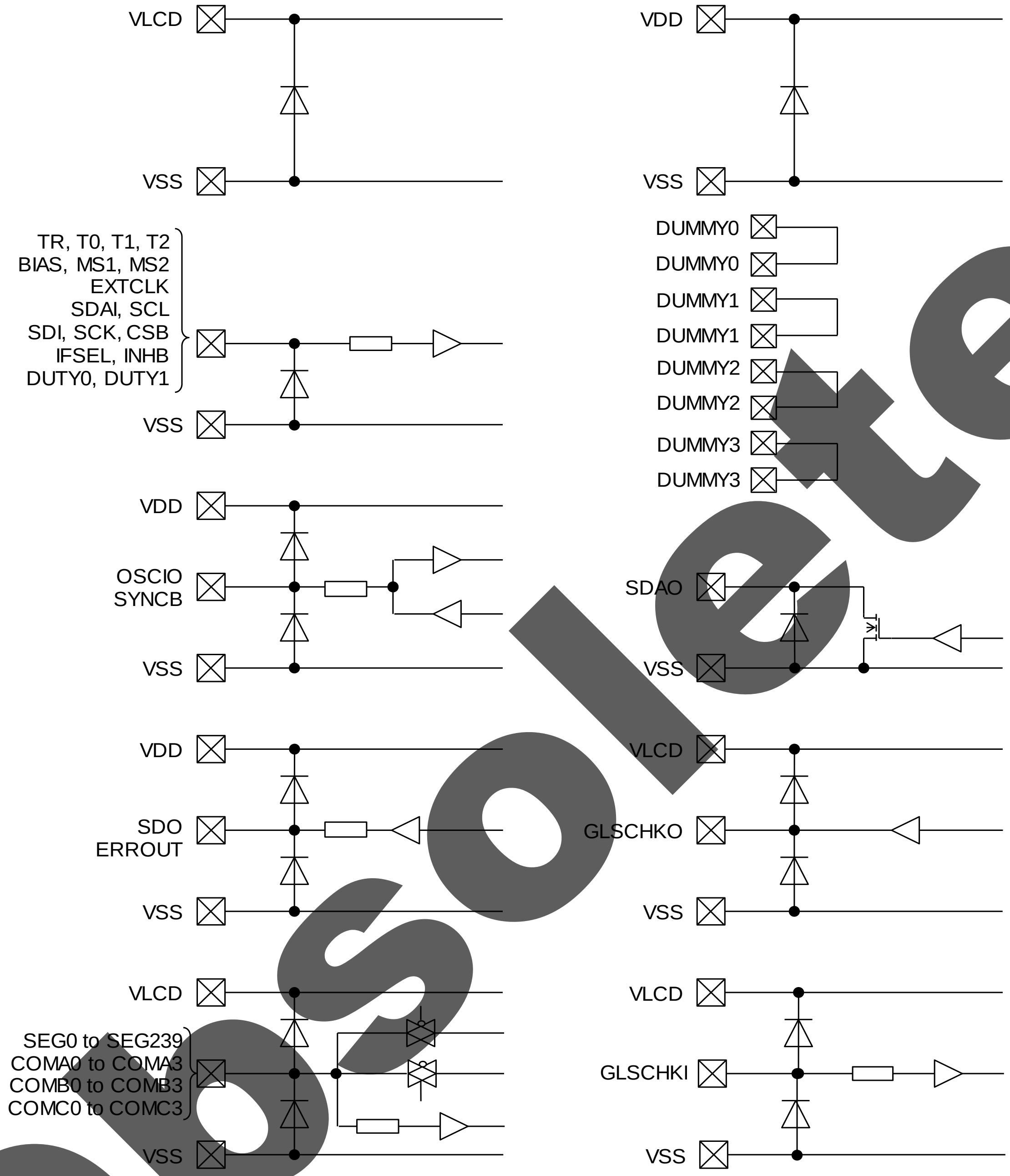
"t_{DC}" and "t_{DR}" depend on ITO resistance R_{ITO} and load capacitance C_L.

R_{ITO}: ITO resistance on the LCD glass. (Any component is not necessary to be attached.)

C_L: A parasitic capacitance to VSS in an application circuit. (Any component is not necessary to be attached.)



I/O Equivalence Circuit



MCU Interface

BU91R66CH-M supports two MCU Interfaces. In IFSEL = VSS, 2-wire Serial Interface (hereinafter referred to as “2-wire”) is available. And in IFSEL = VDD, 3-wire Serial Interface (hereinafter referred to as “3-SPI”) is available.

START and STOP Condition (2-wire)

In IFSEL = VSS, BU91R66CH-M is controlled by 2-wire signals (SDAI, SCL).
It is necessary to generate “START Condition” and “STOP Condition” when sending command or Display Data.

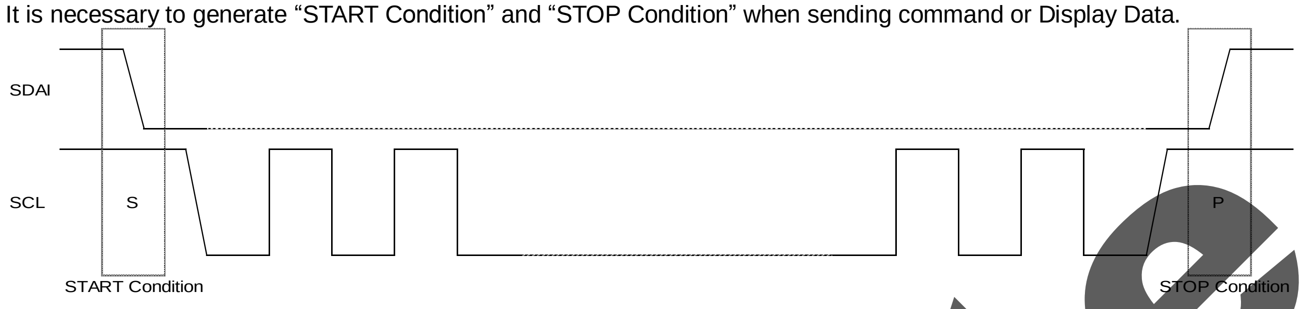


Figure 6. 2-wire Command / Data Transfer Format

Acknowledge (ACK) (2-wire)

Data format is comprised of 8-bit data to SDAI. And an acknowledge bit is returned from SDAO terminal after the 8-bit data is sent. SDAO is also used in Display Data read-back and Command Registers read-back. The serial data input line (SDAI) and the serial data output line (SDAO) are separated in PAD assignment, but both terminals can be connected together to facilitate a single line SDA.

After the transfer of 8-bit data (Slave Address, Control Byte, Command, Display Data), release the SDA line at the falling edge of the eighth clock. The SDA line is then pulled low until the falling edge of the ninth clock SCL. (Output cannot be pulled high because of open-drain NMOS output structure). If the acknowledge function is not required, keep SDA line at low level from the eighth falling edge to the ninth falling edge of SCL.

Not acknowledged bit (NACK) will be returned in following cases.

(1) Incorrect Slave Address
(2) Different Sub Address (in receiving Display Data, CNTSET and COMSET commands)

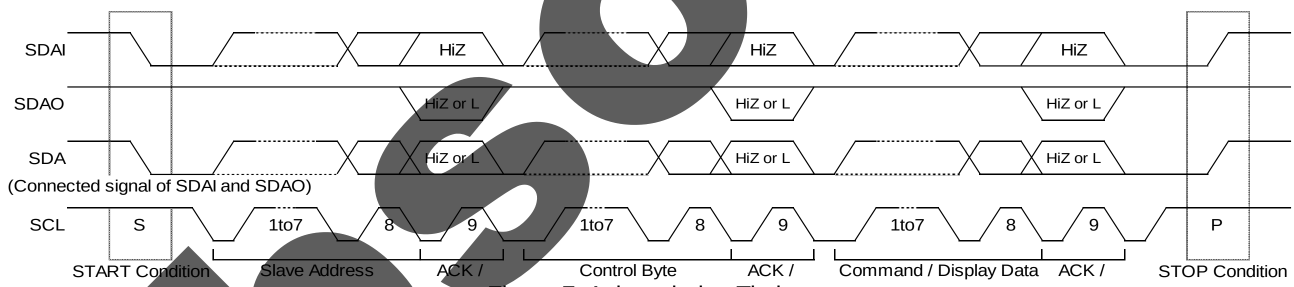


Figure 7. Acknowledge Timing

When Slave Address cannot be recognized correctly in the first data transfer, NACK will be generated and next transfer will be invalid. Even in the invalid status, BU91R66CH-M will return to valid status by receiving “START Condition” again.

Consider MCU Interface Characteristics such as Input rise time and Setup / Hold time when transferring command and data. Refer to **2-wire Serial Interface Characteristics**.

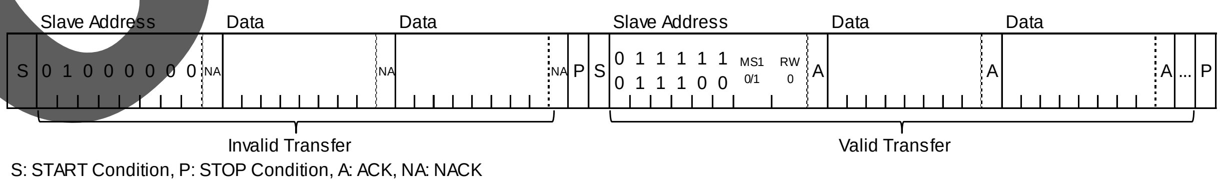


Figure 8. Wrong Slave Address Case

MCU Interface - continued

Command / Display Data Transfer Method (2-wire)

Issue Slave Address after generating “START Condition”. The first byte after Slave Address must be Control Byte. The Control Byte consists of 8bits: CO, RS, and 6 undefined bits. The first bit is CO: continuous data bytes / single data byte selector, the second bit is RS: Command / Display Data selector and the others are undefined bits.

CO	Function
0	Continuous data bytes available after the Control Byte.
1	Only single data byte available after the Control Byte. After the data byte, Control Byte can be accepted again.

RS	Function
0	Command is received after the Control Byte.
1	Display Data is received after the Control Byte. Continuous Display Data is available regardless of CO value.

The following procedure shows how to transfer Command and Display Data.

(1) Generate “START Condition”.
(2) Issue Slave Address.(Note 1)
(3) Transfer Control Byte.
(4) Transfer Command and Display Data.
(5) Generate “STOP Condition”.

(Note 1) Slave Address is specified by MS1 setting. (2-wire mode only)

MS1	Slave Address [7:1]
0	0111110 / 0111000
1	0111111 / 0111001

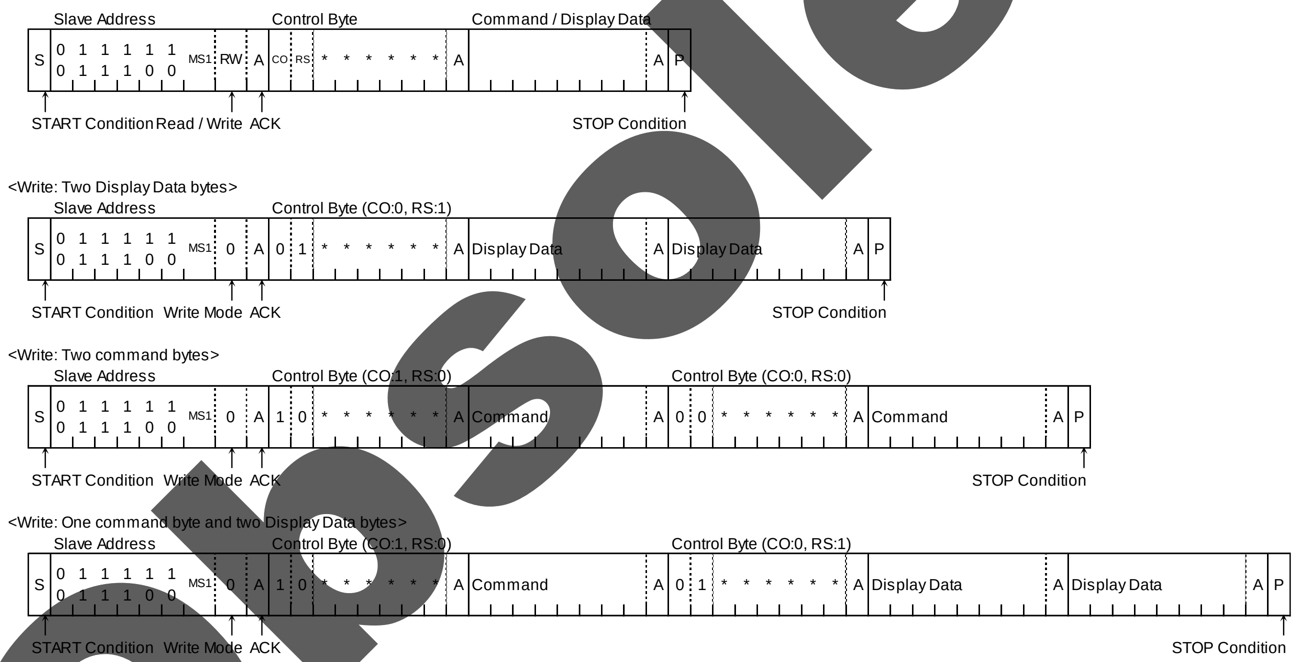


Figure 9. 2-wire Interface Protocol

BU91R66CH-M cannot accept Control Byte / Command once it enters into continuous data transfer state. “STOP Condition” and “START Condition” are necessary in order to accept Command again. If “START Condition” or “STOP Condition” is received during Command / Display Data transfer, the byte in transferring will be cancelled.
Then if Slave Address is received after the “START Condition”, BU91R66CH-M enters into Control Byte transfer state.

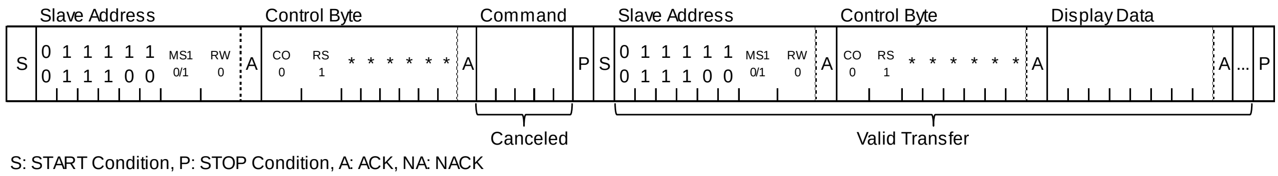


Figure 10. Case of Exiting Data Transfer State in 2-wire

MCU Interface - continued

Display Data Transfer Method (2-wire)

For Display Data write, set R/W bit in Slave Address byte to “0” (Write Mode) and Bit6 in Control Byte to “1”. BU91R66CH-M has a Display Data RAM (DDRAM) of 240 x 4 = 960-bit. SADSET, ADSET1 and ADSET2 commands specify the address where the first Display Data Byte is written. To define internal address correctly, set ADSET1 command before ADSET2. The address is automatically incremented in every 4-bit data and the Display Data is written to DDRAM at the same timing. Smaller Display Data than 4-bit will be cancelled in the transfer.

Burst write into DDRAM is available by transferring data continuously. The address is returned to 00h by the auto-increment function after writing Display Data to the last address. BU91R66CH-M escapes from the burst mode by STOP Condition.

Ex. in 1/4 Duty Drive, the address is returned to 00h (for SEG0) after writing data into address = EFh (for SEG239). In case of Static Drive Mode, maximum address is 3Bh (for SEG236 to SEG239).

The relationships between input Display Data, DDRAM address map and SEG output are as follows.

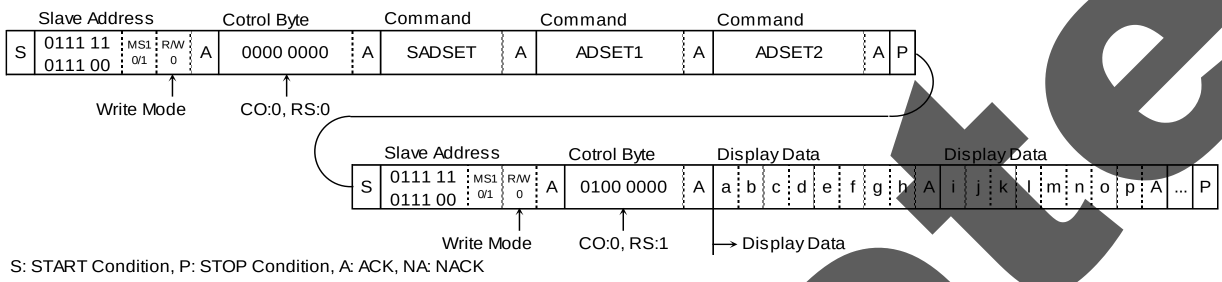


Figure 11. Display Data Transfer in 2-wire

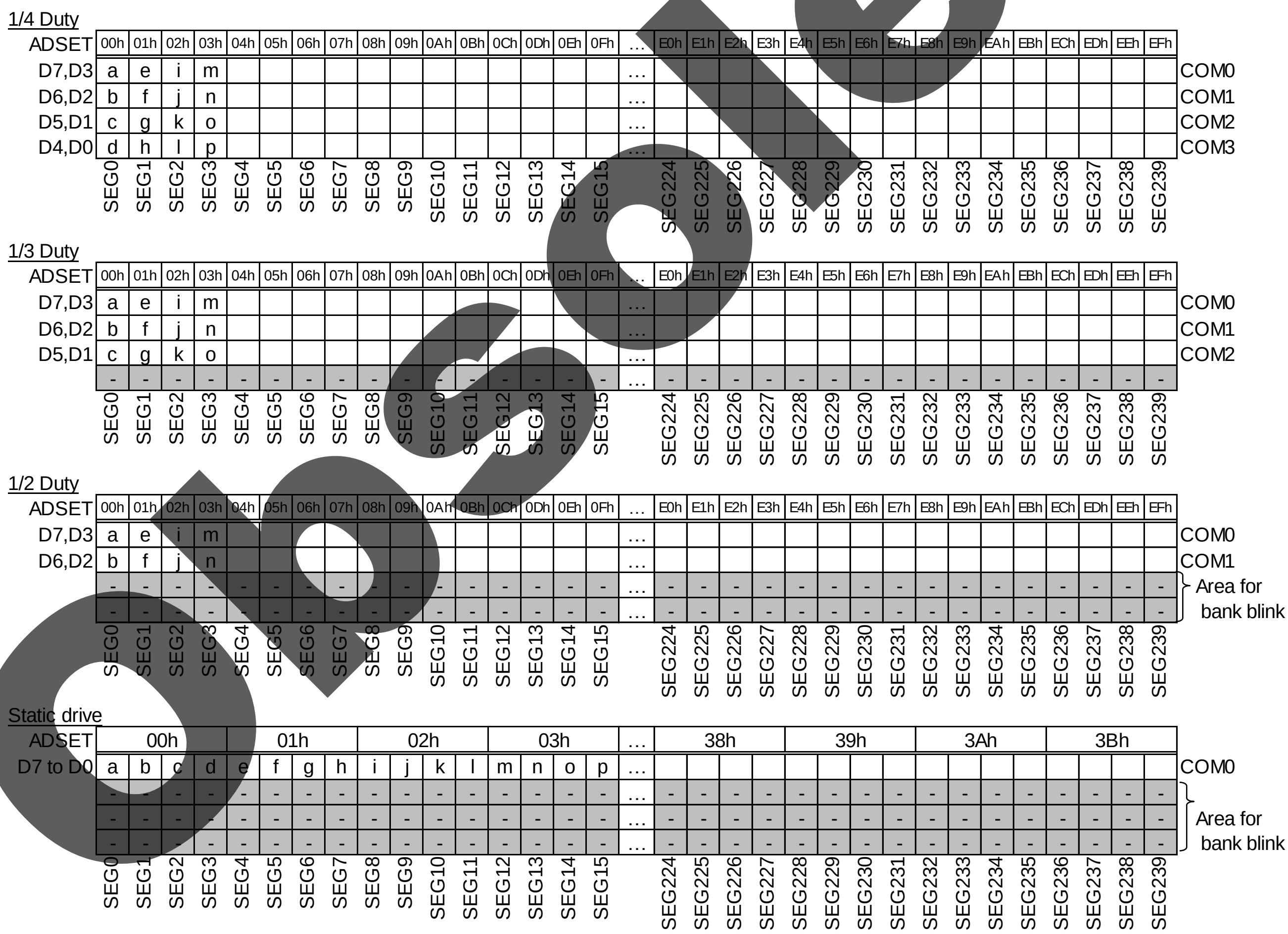


Figure 12. DDRAM Address Map in Write Mode

MCU Interface - continued

Display Data Read-back Method (2-wire)

For Read Mode, set R/W bit in Slave Address byte to “1”. In advance, Read_data bit in RDCTL must be set to “1” for reading Display Data. The Display Data values can be read during Read Mode. The sequence of the Display Data read-back is shown below.

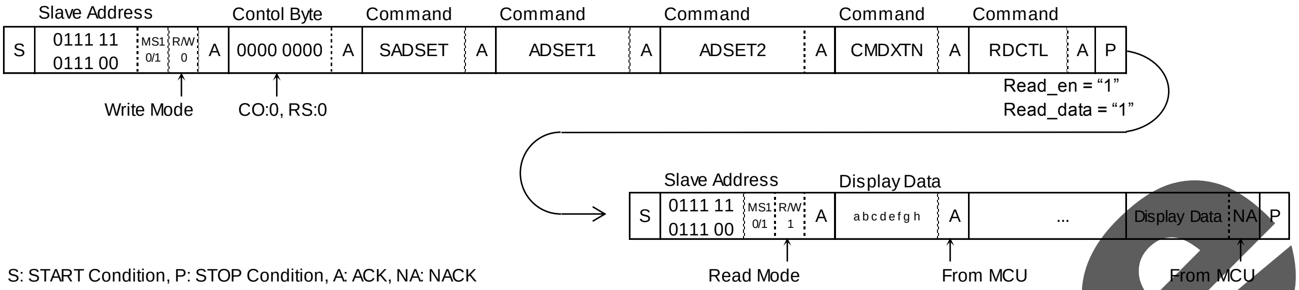


Figure 13. Display Data Read-back in 2-wire

During Read Mode, the Display Data can be read from the DDRAM through the SDAO line. The data will output synchronized with falling edge of SCL input.
SADSET, ADSET1 and ADSET2 must be set first during Write Mode in advance. To define internal address correctly, set ADSET1 command before ADSET2. If DDRAM address is not specified before Display Data read, the current DDRAM address is used as the first read address. Address will be incremented automatically by +2 addresses after 8-bit data output. The Address will be set to 00h automatically after maximum address.
MCU must reply ACK to BU91R66CH-M after each 8-bit data output to keep Read Mode. If MCU replies no ACK response (NACK), BU91R66CH-M will escape Read Mode and SDAO output status will be released.

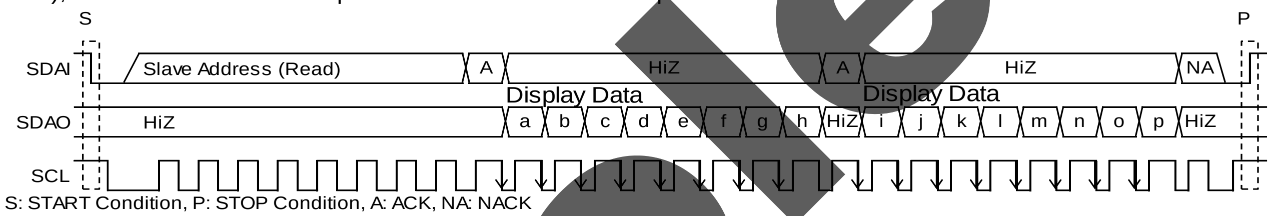


Figure 14. Bit-Assignment in Display Data Read-back in 2-wire

1/4 Duty

ADSET	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	…	E0h	E1h	E2h	E3h	E4h	E5h	E6h	E7h	E8h	E9h	EAh	EBh	ECh	EDh	EEh	EFh	
D7,D3	a	e	i	m													…																	COM0
D6,D2	b	f	j	n													…																	COM1
D5,D1	c	g	k	o													…																	COM2
D4,D0	d	h	l	p													…																	COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15		SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239	

1/3 Duty

ADSET	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	…	E0h	E1h	E2h	E3h	E4h	E5h	E6h	E7h	E8h	E9h	EAh	EBh	ECh	EDh	EEh	EFh	
D7,D3	a	e	i	m													…																	COM0
D6,D2	b	f	j	n													…																	COM1
D5,D1	c	g	k	o													…																	COM2
D4,D0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	…	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15		SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239	

1/2 Duty

ADSET	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	…	E0h	E1h	E2h	E3h	E4h	E5h	E6h	E7h	E8h	E9h	EAh	EBh	ECh	EDh	EEh	EFh	
D7,D3	a	e	i	m													…																	COM0
D6,D2	b	f	j	n													…																	COM1
D5,D1	c	g	k	o													…																	Area for
D4,D0	d	h	l	p													…																	bank blink
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15		SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239	

Static drive

ADSET	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	…	E0h	E1h	E2h	E3h	E4h	E5h	E6h	E7h	E8h	E9h	EAh	EBh	ECh	EDh	EEh	EFh	
D7,D3	a	e	i	m													…																	COM0
D6,D2	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	…	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
D5,D1	c	g	k	o	*	*	*	*	*	*	*	*	*	*	*	*	…	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Area for
D4,D0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	…	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	bank blink
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15		SEG224	SEG225	SEG226	SEG227	SEG228	SEG229	SEG230	SEG231	SEG232	SEG233	SEG234	SEG235	SEG236	SEG237	SEG238	SEG239	

Figure 15. DDRAM Address Map in Read Mode

MCU Interface - continued

Command Registers Read-back Method (2-wire)

For Read Mode, set R/W bit in Slave Address bye to “1”. In advance, Read_data bit in RDCTL must be set to “0” for reading Command Registers. The Command Registers can be read during Read Mode. The sequence of the Command Registers read-back is shown below and is similar to the Display Data read sequence.

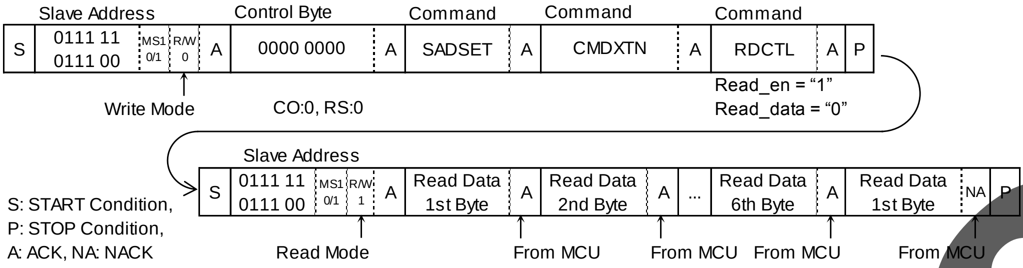


Figure 16. Command Registers Read-back Method in 2-wire

After the sixth byte data, the first byte data will be outputted again. Command Registers read-back mode can be released at NACK condition (Same as Read Display Data).

Table 3. Command Registers Map for Read-back

Byte	Bit	Read Data	Remark
1st Byte	D7	Enable for Glass Breaking Detection	MODESET2 P3
	D6	Enable for Interface Checksum Detection	MODESET2 P2
	D5	Enable for Logic Error Detection	MODESET2 P1
	D4	Enable for SEG / COM Toggle Detection	MODESET2 P0
	D3	Status of Glass Breaking Detection	1: Abnormal, 0: Normal
	D2	Status of Interface Checksum Detection	1: Abnormal, 0: Normal
	D1	Status of Logic Error Detection	1: Abnormal, 0: Normal
	D0	Status of SEG / COM Toggle Detection	1: Abnormal, 0: Normal
2nd Byte	D7	Display On	MODESET1 P3
	D6	Blink Mode	BLKCTL1 P2
	D5	2x frequency in frame Inversion	MODESET3 P1
	D4	Inversion Mode	MODESET3 P2
	D3	Higher Frequency Mode	MODESET3 P0
	D2	Frame Rate Bit2	FRSET P2
	D1	Frame Rate Bit1	FRSET P1
	D0	Frame Rate Bit0	FRSET P0
3rd Byte	D7	Blink Freq. Bit1	BLKCTL1 P1
	D6	Blink Freq. Bit0	BLKCTL1 P0
	D5	Blink Area Select	BLKCTL2 P1
	D4	EVR Bit4	COMSET P3
	D3	EVR Bit3	CNTSET P3
	D2	EVR Bit2	CNTSET P2
	D1	EVR Bit1	CNTSET P1
	D0	EVR Bit0	CNTSET P0
4th Byte	D7	IFCHKSUM Bit3	CHKSUM P3
	D6	IFCHKSUM Bit2	CHKSUM P2
	D5	IFCHKSUM Bit1	CHKSUM P1
	D4	IFCHKSUM Bit0	CHKSUM P0
	D3	0	-
	D2	COMSET Bit2	COMSET P2
	D1	COMSET Bit1	COMSET P1
	D0	COMSET Bit0	COMSET P0
5th Byte	D7	0	-
	D6	0	-
	D5	Sub Address Set Bit1	SADSET P1
	D4	Sub Address Set Bit0	SADSET P0
	D3	0	-
	D2	0	-
	D1	0	-
	D0	1	-
6th Byte	D7	Address Set Bit7	ADSET1 P3
	D6	Address Set Bit6	ADSET1 P2
	D5	Address Set Bit5	ADSET1 P1
	D4	Address Set Bit4	ADSET1 P0
	D3	Address Set Bit3	ADSET2 P3
	D2	Address Set Bit2	ADSET2 P2
	D1	Address Set Bit1	ADSET2 P1
	D0	Address Set Bit0	ADSET2 P0

MCU Interface - continued

Command / Display Data Transfer Method (3-SPI)

In IFSEL = VDD, BU91R66CH-M is controlled by 3-wire signals (CSB, SCK, and SDI). First, Interface counter is initialized with CSB = high, then CSB = low enables SDI and SCK input.
D7 to D0 follows continuously after CSB = low. Internal data is latched at the rising edge of SCK. Command is converted to 8-bit parallel data at the rising edge of the eighth SCK. Display Data is stored at the fourth and the eighth falling edge of SCK.
The protocol of 3-SPI transfer is as follows.

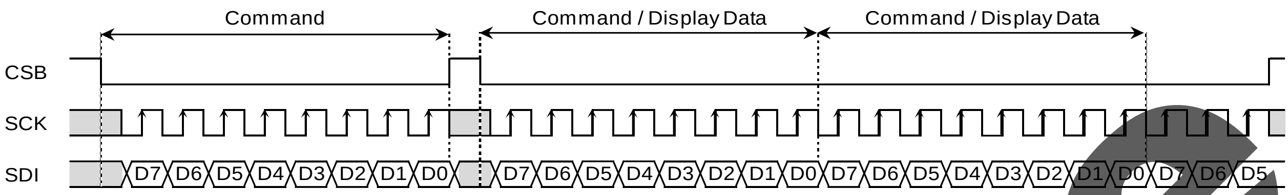


Figure 17. Command / Data Transfer in 3-SPI Command / Data Transfer in 3-SPI

Command Transfer Method (3-SPI)

After CSB changes from high to low, the first byte is always a command input. To escape Display Data transfer condition or to send command again, CSB should be set from low to high then set to low.

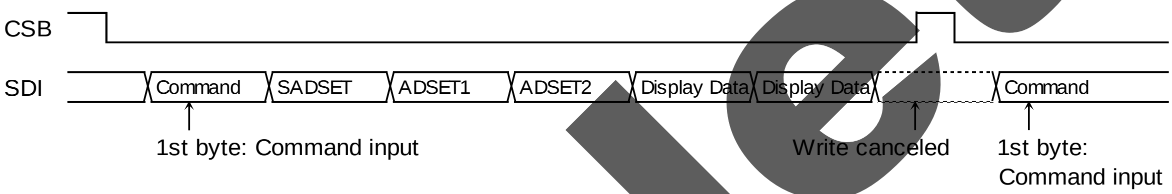


Figure 18. Escape from Data Transfer Condition in 3-SPI

Command transfer is done by 8-bit unit, so if CSB is set from low to high with less than 8-bit data transfer, command will be cancelled. It will be able to transfer command when CSB = low again.

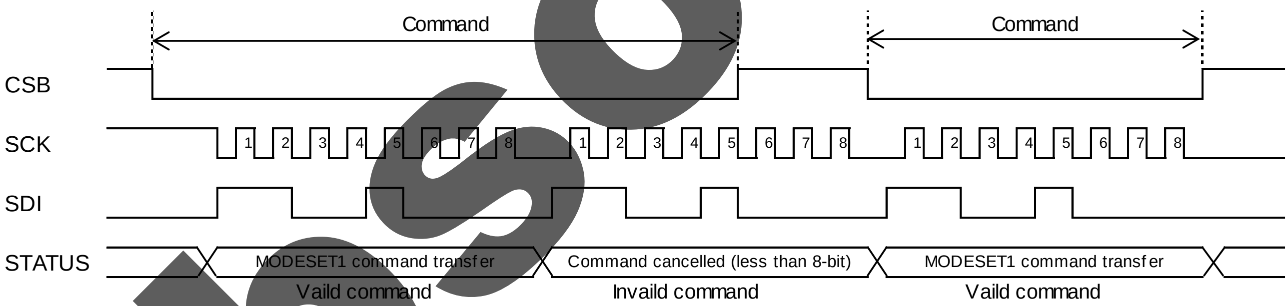


Figure 19. Case of Less Than 8-bit Data Transfer in 3-SPI

MCU Interface - continued

Display Data Transfer Method (3-SPI)

In 3-SPI, BU91R66CH-M enters to Display Data write state after receiving ADSET2 command. BU91R66CH-M has a Display Data RAM (DDRAM) of 240 x 4 = 960-bit. SADSET, ADSET1 and ADSET2 commands specify the address where the first Display Data Byte is written. To define internal address correctly, set ADSET1 command before ADSET2. The address is automatically incremented in every 4-bit data and the Display Data is written to DDRAM at the same timing. Smaller Display Data than 4-bit will be cancelled in the transfer.

Burst write into DDRAM is available by transferring data continuously. The address is returned to 00h by the auto-increment function after writing Display Data to the last address. BU91R66CH-M escapes from the burst mode by setting CSB to high.

Ex. in 1/4 Duty Drive mode, the address is returned to 00h (for SEG0) after writing Display Data into address = EFh (for SEG239). In case of Static Drive Mode, maximum address is 3Bh (for SEG236 to SEG239).

The DDRAM address map is same as the one in 2-wire Serial Interface (Refer to **Figure 12. DDRAM Address Map in Write Mode**).

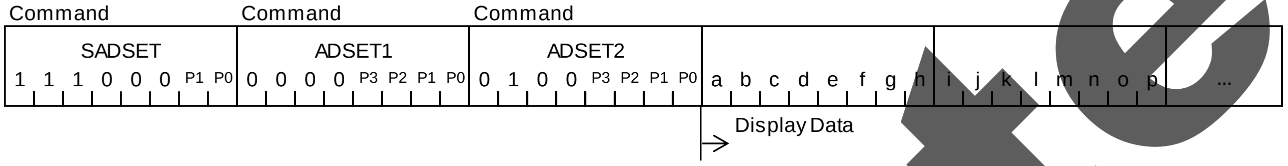


Figure 20. Display Data Transfer and Bit Assignment in 3-SPI

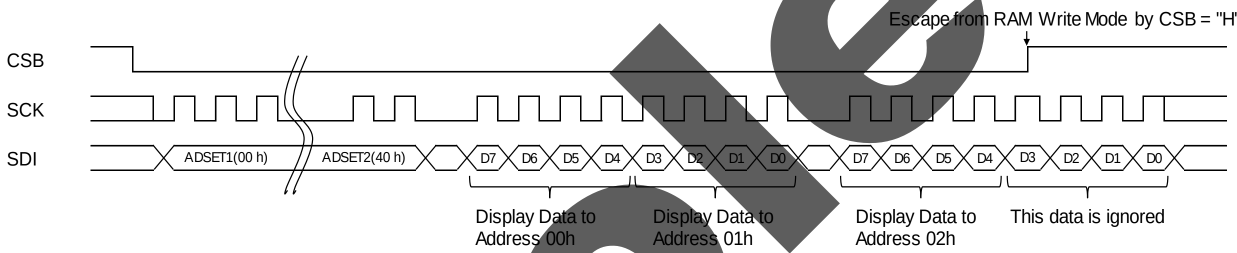


Figure 21. Case of Less Than 4-bit Write Data Transfer in 3-SPI

MCU Interface - continued

Display Data Read-back Method (3-SPI)

Set Read_en = “1” and Read_data = “1” in RDCTL register to enter to Display Data Read Mode. The Display Data values can be read during this mode. The sequence of the Display Data Read-back is shown below.

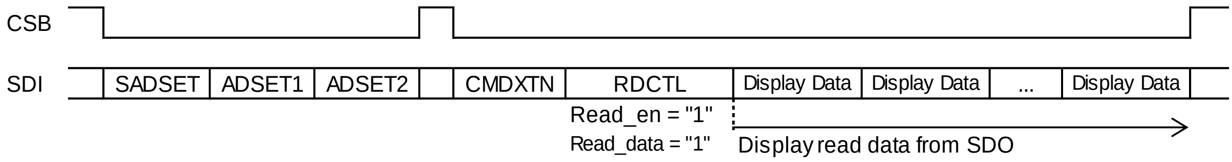


Figure 22. Display Data Read-back in 3-SPI

During Display Data Read Mode, the Display Data can be read from the DDRAM through the SDO line. The data will output synchronized with falling edge of SCK input.
SADSET, ADSET1 and ADSET2 must be set first during Write Mode in advance. To define internal address correctly, set ADSET1 command before ADSET2. If DDRAM address is not specified before Display Data read, the current DDRAM address is used as the first read address. Address will be incremented automatically by +2 addresses after 8-bit data output. The Address will be set to 00h automatically after maximum address. Display Data Read Mode will be released by setting CSB to high (SDO output also be stopped).
The DDRAM address map is same as the one in 2-wire Serial Interface (Refer to **Figure 15. DDRAM Address Map in Read Mode**).

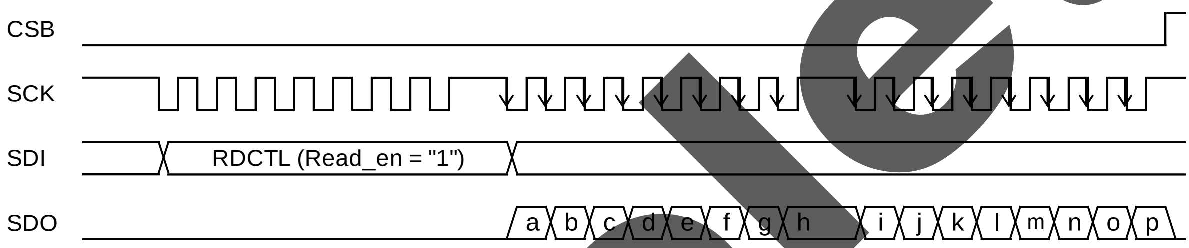


Figure 23. Bit-Assignment in Display Data Read-back in 3-SPI

Command Registers Read-back Method (3-SPI)

Set Read_en = “1” and Read_data = “0” in RDCTL register to enter Command Registers Read Mode. The Command Registers values can be read during this mode. The sequence of the Command Registers read-back is shown below.

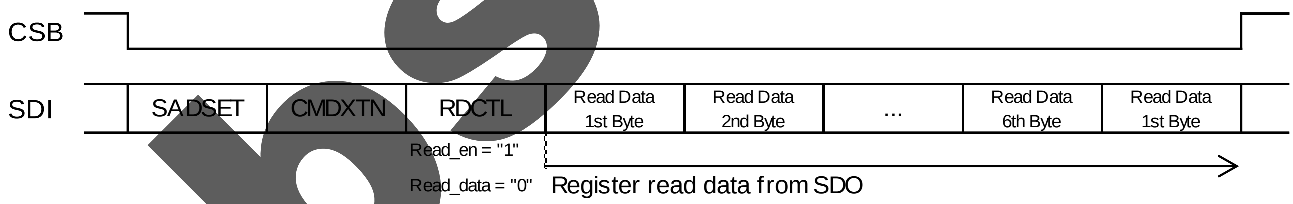


Figure 24. Command Registers Read-back in 3-SPI

After reading the 6th byte data, the first byte data will be output again. Command Registers Read Mode will be released after CSB change from low to high. (SDO stops).
The Command Registers Map is same as the one in 2-wire. Refer to **Table 3. Command Registers Map for Read-back**.

OSC (Oscillator)

In master chip (MS1 = VSS and MS2 = VSS), the clock mode can be selected by EXTCLK. The clock signals for logic and analog circuit can be generated in internal oscillator if EXTCLK = VSS or can be provided from external clock input if EXTCLK = VDD.

Clock Mode	EXTCLK	OSCIO
Internal Clock Mode	VSS	To Output Internal Generated Clock Signal
External Clock Mode	VDD	To Input External Clock

In cascaded connection, slave chip (MS1 = VDD or MS2 = VDD) is always in External Clock Mode regardless of EXTCLK.

In case of External Clock Mode, a clock signal should be always supplied to BU91R66CH-M. Removing the clock may freeze the LCD in a DC state which is not suitable for the LCD.

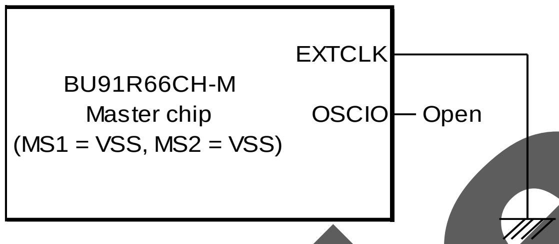


Figure 25. Internal Clock Mode

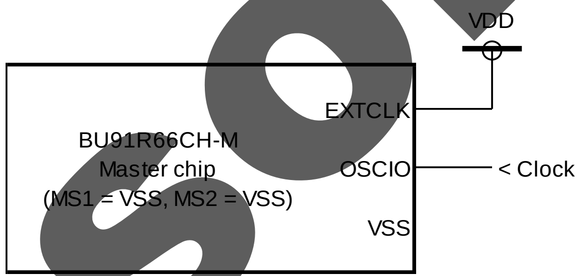


Figure 26. External Clock Mode

SYNC CTRL (Multi-chip Structure)

BU91R66CH-M supports large display application by connecting up to four IC in cascade. BU91R66CH-M can be combined with BU91R64CH-M and BU91R65CH-M.
The relationship of MS1 / MS2 setting, OSCIO, SYNCB and SADSET are shown below. To synchronize each IC, connect the synchronizing signal (SYNCB) and the synchronous clock (OSCIO) from the Master to Slave ICs.

In case of 2-wire Serial Interface

MS2	MS1	Mode	Slave Address [7:1]	OSCIO				SYNCB		SADSET (P1,P0)
				EXTCLK = VDD (Note 1)		EXTCLK = VSS (Note 2)				
				I/O	Connected to	I/O	Connected to	I/O	Connected to	
VSS	VSS	Master	0111 110 / 0111 000	IN	MCU	OUT	Slave1 to Slave3 (OSCIO)	OUT	Slave1 to Slave3 (SYNCB)	(0,*)
VSS	VDD	Slave1	0111 111 / 0111 001	IN	MCU	IN	Master (OSCIO)	IN	Master (SYNCB)	(0,*)
VDD	VSS	Slave2	0111 110 / 0111 000	IN	MCU	IN	Master (OSCIO)	IN	Master (SYNCB)	(1,*)
VDD	VDD	Slave3	0111 111 / 0111 001	IN	MCU	IN	Master (OSCIO)	IN	Master (SYNCB)	(1,*)

(*: don't care)
(Note 1) Frame rate is fixed (24 clock / frame) regardless of FRSET and MODESET3.
(Note 2) Frame rate depends on FRSET and MODESET3. All of Master and Slave1 to Slave3 must be same setting in the registers.

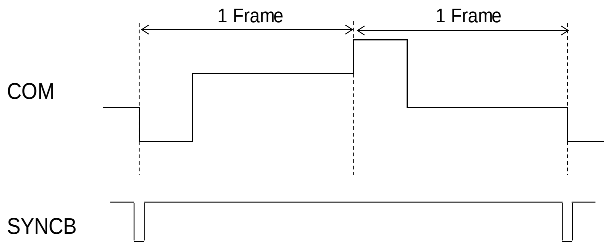
In case of 3-wire Serial Interface

MS2	MS1	Mode	OSCIO				SYNCB		SADSET (P1,P0)
			EXTCLK = VDD (Note 1)		EXTCLK = VSS (Note 2)				
			I/O	Connected to	I/O	Connected to	I/O	Connected to	
VSS	VSS	Master	IN	MCU	OUT	Slave1 to Slave3 (OSCIO)	OUT	Slave1 to Slave3 (SYNCB)	(0, 0)
VSS	VDD	Slave1	IN	MCU	IN	Master (OSCIO)	IN	Master (SYNCB)	(0, 1)
VDD	VSS	Slave2	IN	MCU	IN	Master (OSCIO)	IN	Master (SYNCB)	(1, 0)
VDD	VDD	Slave3	IN	MCU	IN	Master (OSCIO)	IN	Master (SYNCB)	(1, 1)

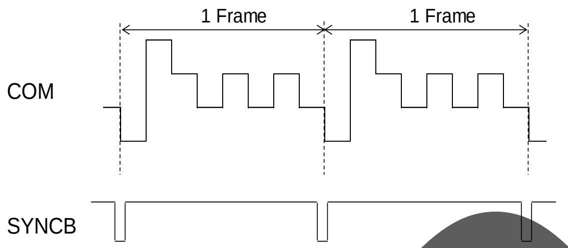
(Note 1) Frame rate is fixed (24 clock / frame) regardless of FRSET and MODESET3.
(Note 2) Frame rate depends on FRSET and MODESET3. All of Master and Slave1 to Slave3 must be same setting in the registers.

SYNC CTRL (Multi-chip Structure) - continued

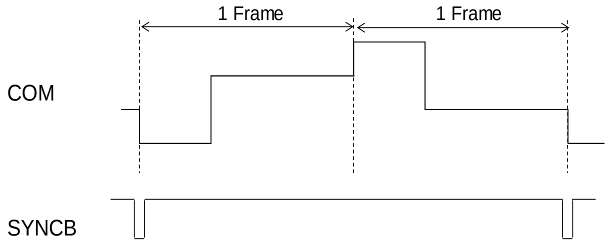
The relationship between COM and SYNCB timing is as follows.



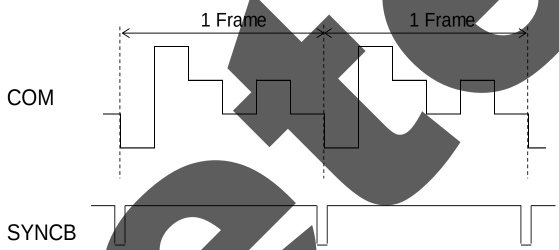
(a-1) 1/4 Duty Drive and Frame Inversion



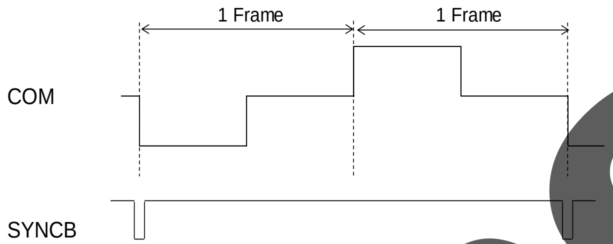
(a-2) 1/4 Duty Drive and Line Inversion



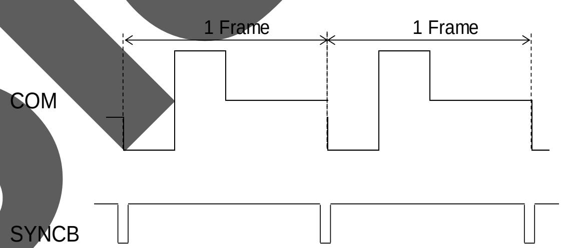
(b-1) 1/3 Duty Drive and Frame Inversion



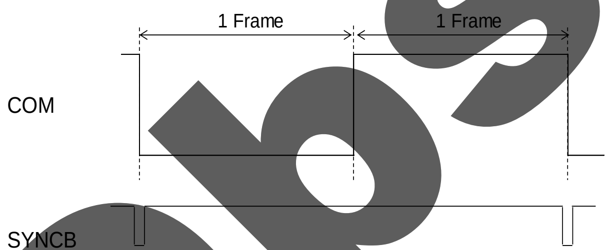
(b-2) 1/3 Duty Drive and Line Inversion



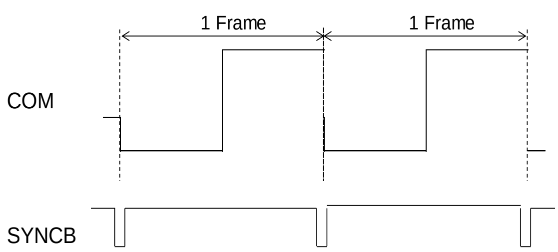
(c-1) 1/2 Duty Drive and Frame Inversion (1/2bias)



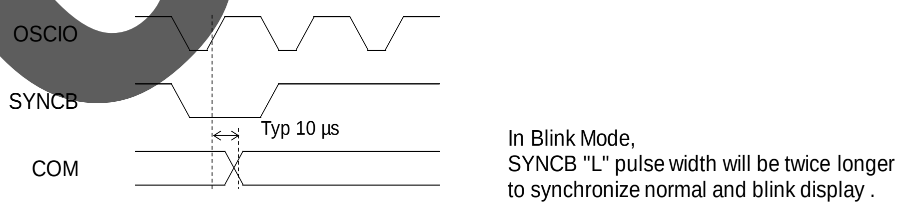
(c-2) 1/2 Duty Drive and Line Inversion (1/2bias)



(d-1) Static Drive and Frame Inversion



(d-2) Static Drive and Line Inversion



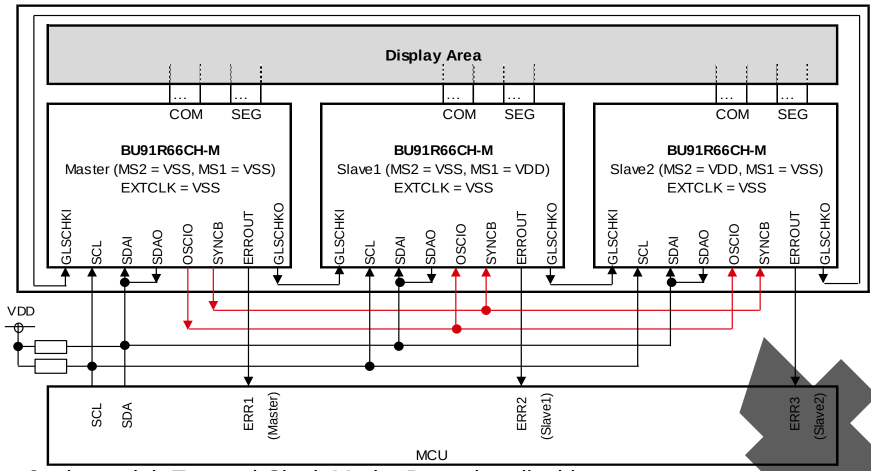
(e) Driver timing waveform

Figure 27. Synchronization of Multi-chip Cascaded Connection

SYNC CTRL (Multi-chip Structure) - continued

The example of cascaded connection

<2-wire serial, Internal Clock Mode, Detection enable>



<3-wire serial, External Clock Mode, Detection disable>

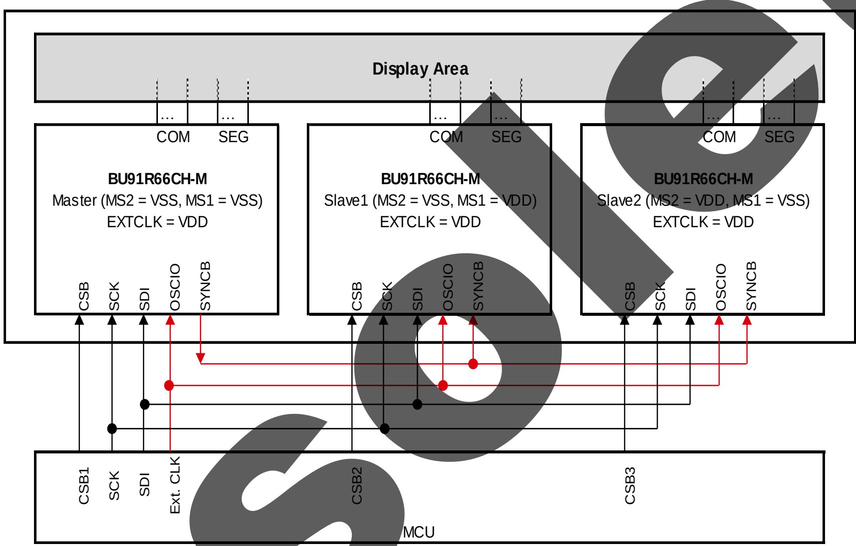


Figure 28. Example of Cascaded Connection

<Different Duty Panel Combination>

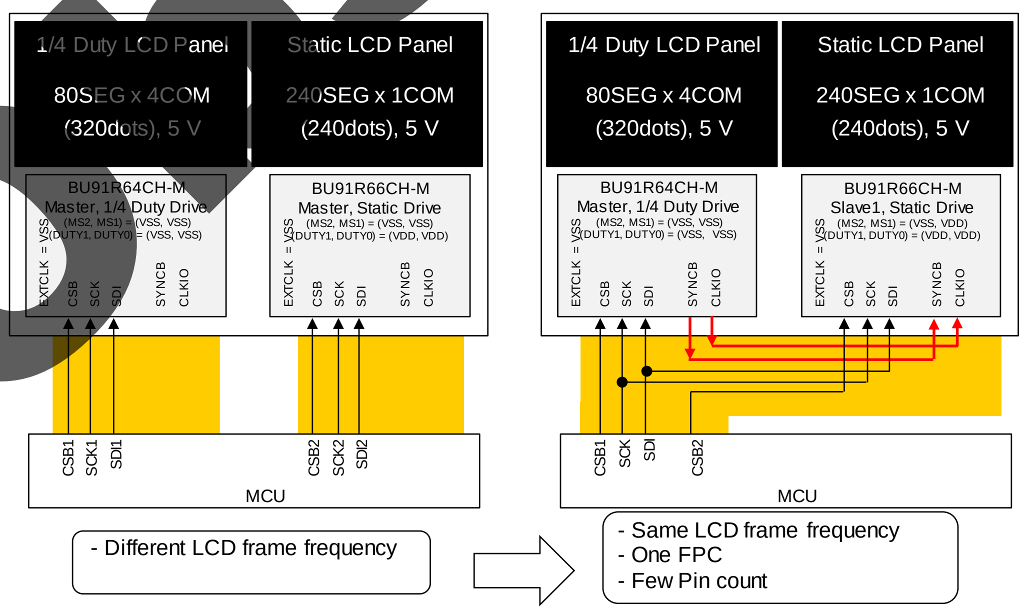


Figure 29. Example Different Duty Drive Panel Configuration

LCD Driver Voltage Generator / LCD Bias Selector

BU91R66CH-M generates LCD driving voltage with on-chip Buffer AMP. 1/3 or 1/2 Bias Drive can be selected by external terminal (BIAS) setting. Line / frame inversion can be set by MODESET3 command. Refer to **LCD Driving Waveform**.

POR and Reset Initialize Condition

BU91R66CH-M has POR (Power On Reset) circuit. Keep Power On / Off specification and sequence described in **Cautions in Power On / Off**. Initial condition after executing Software Reset and POR is as follows.
- Display is off.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Each Command Registers are reset initialize condition. Refer to **Detailed Command Description**.

Blink Control (Blink Timing Generator)

Blink function is asserted by Blink Control1 command (BLKCTL1). In All Segments Blink Mode, all dots blink is available. In Bank Blink Mode, individual dot blink is available only in 1/2 Duty and Static Drive mode. Refer to **6. Blink Control1 (BLKCTL1).** The Displayed RAM mapping is switched at blink frequency as following images.

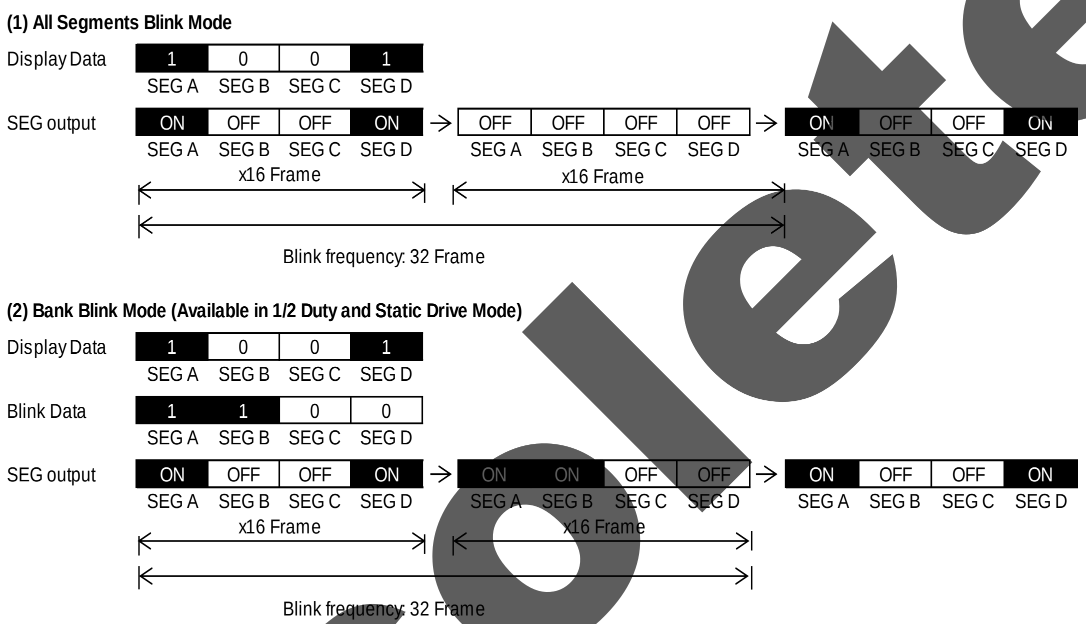


Figure 30. Bank Blink Mode Function (Blink Frequency as 32 Frame Case)

Blink data can be written in Blink Control 2 command (BLKCTL2) P1 = “1”. The command sequence and the relationship between data input and DDRAM Address Map are as follows.

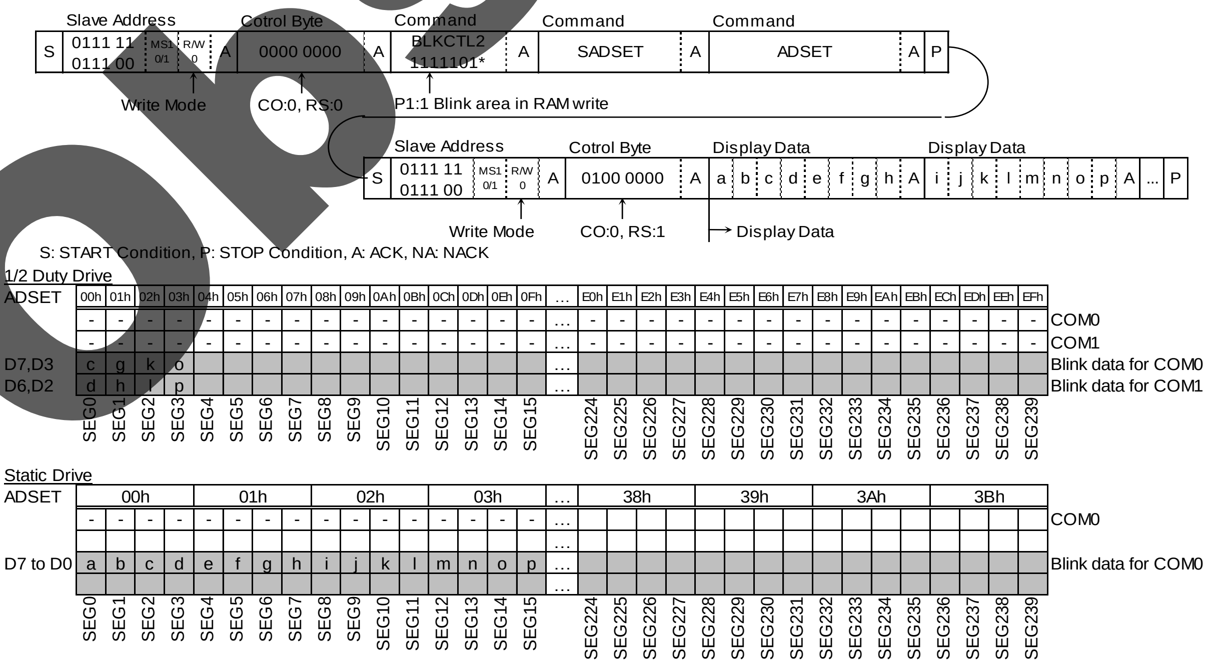


Figure 31. DDRAM Address Map of Blink Area (Bank Blink Mode)

Error Detection

BU91R66CH-M has the following Error Detection functions. When one of functions in a following table detects abnormal status, ERROUT terminal output high level. Then the item with abnormal status can be identified by reading Command Registers.
MCU can detect all events which cause abnormal display by these functions. MCU can take action such as stopping the display or informing other devices about the abnormal display state when LCD module encountered problem.

Table 4. Detection Functions

Item	Detected Error	Detection Function Availability	Detection Timing
Glass Breaking Detection	LCD Glass Breaking	During DISPON	By DISPON Command
Checksum Detection	I/F Communication Error	Always	By CHKSUM Command
Logic Error Detection	Logic DFF Malfunction	During DISPON	Always in DISPON
SEG / COM Toggle Detection	SEG / COM Output Level Error	During DISPON	Always in DISPON
Contact Resistance Check	COG Bonding Status	(No Power Applied)	(In LCD Module Assembly)

Block diagram and data path of Detection block are shown below.

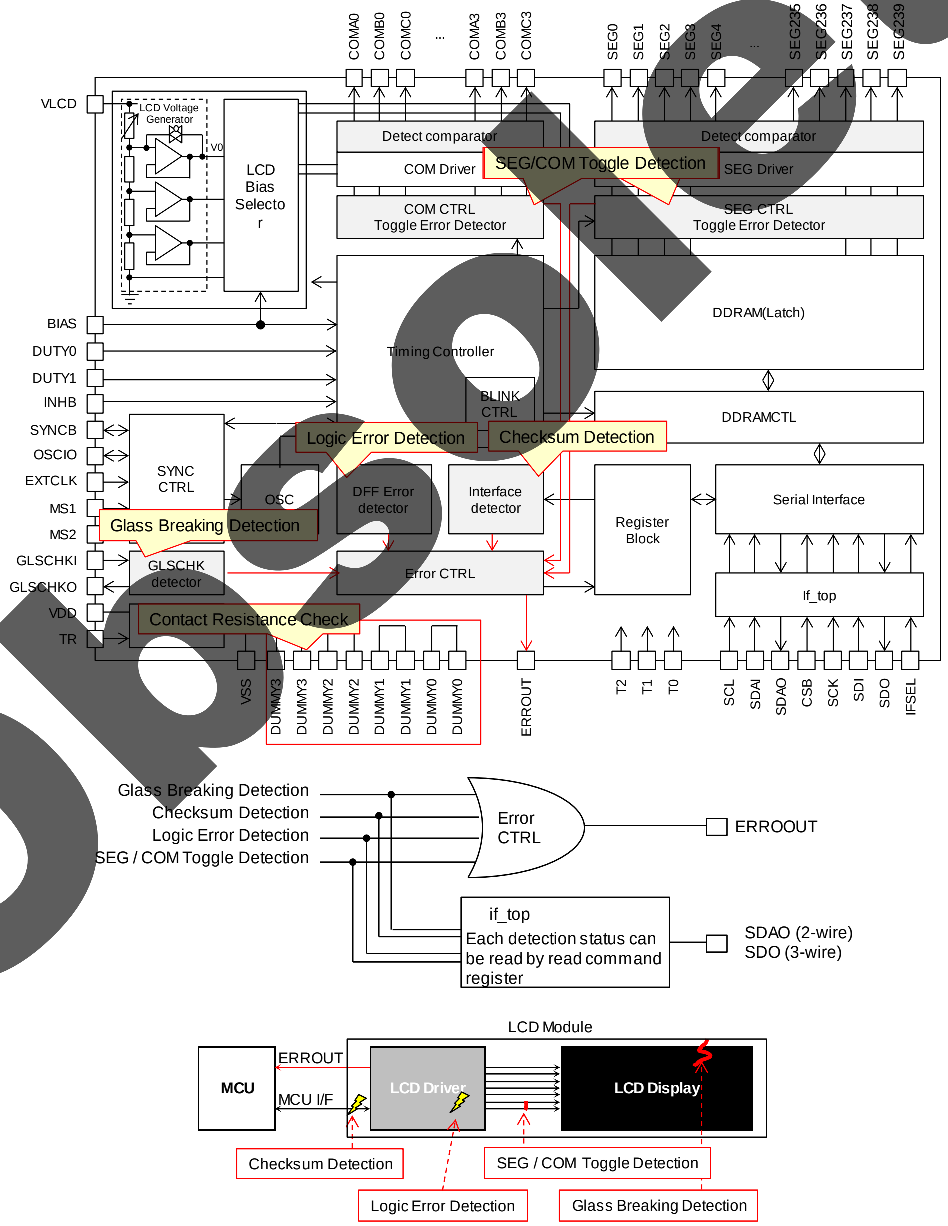


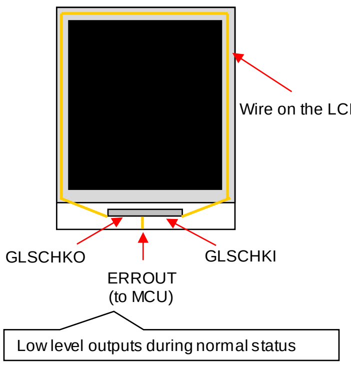
Figure 32. Detection Block and Data Path

Error Detection - continued

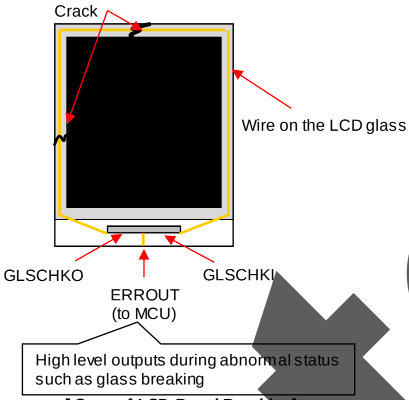
Glass Breaking Detection

BU91R66CH-M can detect LCD glass breaking status.

In Single-chip Use Case,



[Case of LCD Panel No Breaking]



[Case of LCD Panel Breaking]

In Multi-chip Cascaded Use Case,

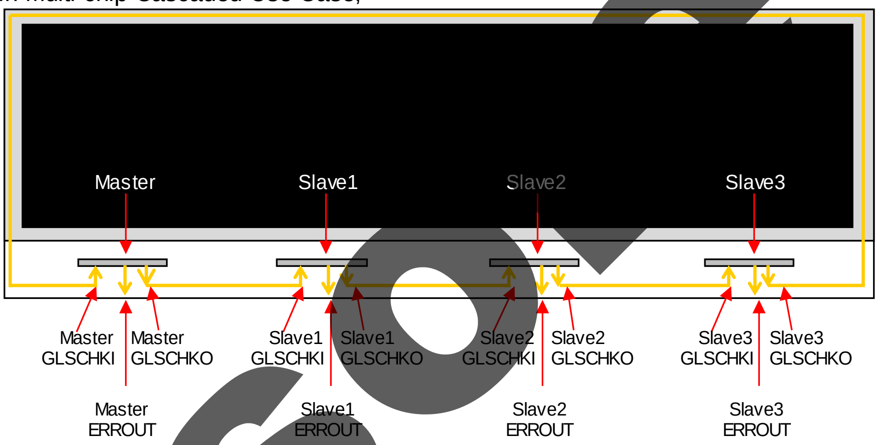


Figure 33. Glass Breaking Detection

Glass Breaking Detection – continued

Glass breaking detection will be judged after 4 frames from MODESET1 command (DISPON). High level will be judged at the end of the second frame after MODESET1 command (DISPON) and low level will be judged at the end of the fourth frame after the command. See following sequence.

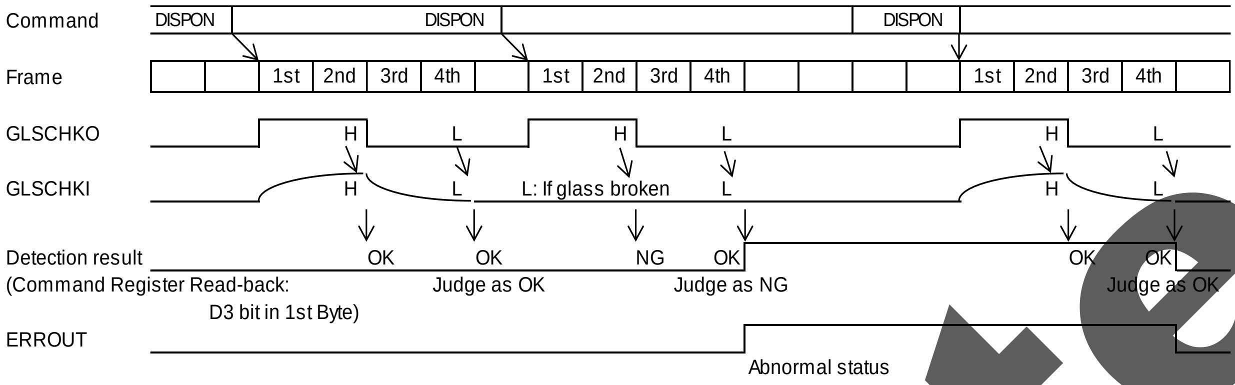


Figure 34. Sequence of Glass Breaking Detection

Thus, the detection period depends on the Frame Frequency setting. It is necessary to consider ITO wiring resistance and capacitance to keep the following calculation:

$$2 \times \tau < 2 \times Frame\ Duty \qquad [s] \qquad (A)$$

where:
τ is the CR time constant. $\tau = C \times R$. C: ITO capacitance, R: ITO resistance.

< Calculation example >
When Frame rate = 200 Hz, Wire length around LCD glass = 500 counts, ITO sheet count = 60 Ω and ITO capacitance = 100 pF

$$ITO\ registance = 60[\Omega] \times 500\ [count] = 30{,}000 \qquad [\Omega]$$

$$2 \times \tau = 2 \times C \times R = 2 \times 100[pF] \times 30[k\Omega] = 6 \qquad [\mu s]$$

$$2 \times Frame\ Duty = 2 \times \frac{1}{200} = 10 \qquad [ms]$$

In this case, (A) is satisfied. So glass check function will work correctly.

Error Detection - continued

Checksum Detection

This function detects the error due to command or Display Data alteration by electric noise during transfer from MCU. Checksum detection will be judged after every CHKSUM command. See following sequence.

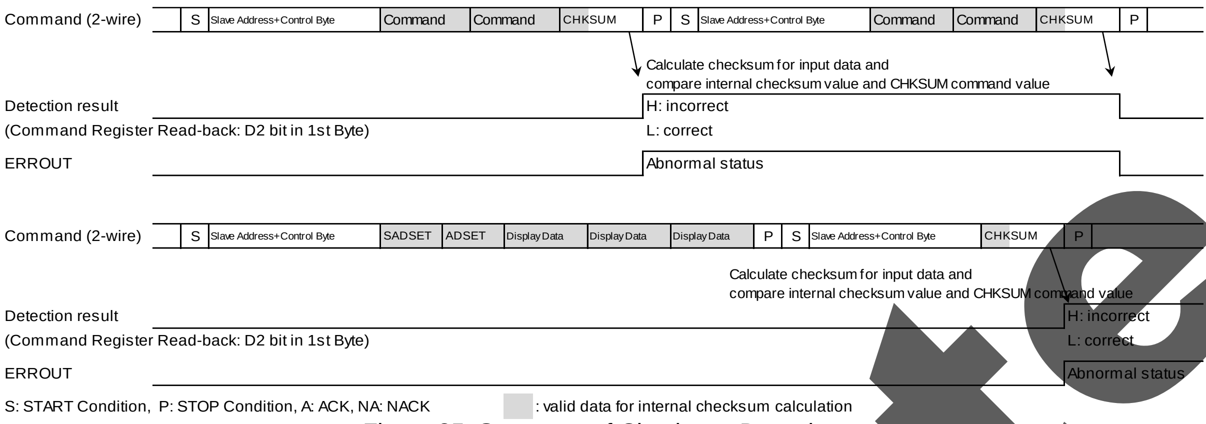
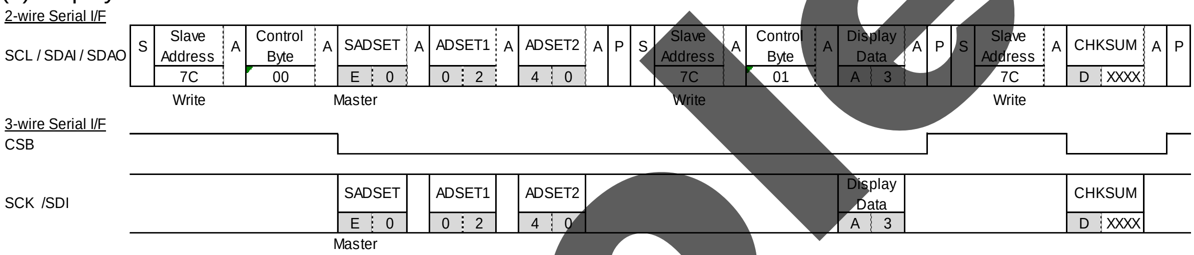


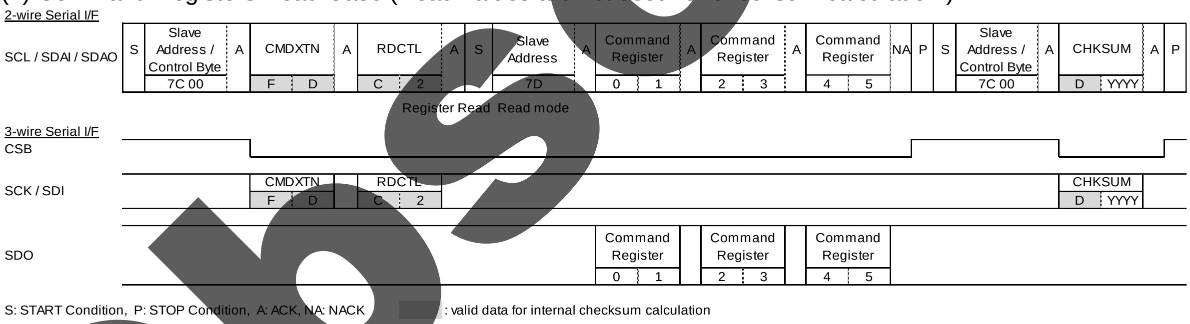
Figure 35. Sequence of Checksum Detection

Checksum calculation example:

(1) Display Data Write Case



(2) Command Registers Read Case (Read values are not used for checksum calculation.)



Calculation (1) RAM Write Case

	Hex	Dec
SADSET upper 4-bit	E	14
SADSET lower 4-bit	0	0
ADSET1 upper 4-bit	0	0
ADSET1 lower 4-bit	2	2
ADSET2 upper 4-bit	4	4
ADSET2 lower 4-bit	0	0
Display Data upper 4-bit	A	10
Display Data lower 4-bit	3	3
CHKSUM upper 4-bit	D	13
Sum	2E	46

"XXXX" is the lower 4-bit of Sum: "Eh"

Calculation (2) Read Case

	Hex	Dec
CMDXTN upper 4-bit	F	15
CMDXTN lower 4-bit	D	13
RDCTL upper 4-bit	C	12
RDCTL lower 4-bit	2	2
CHKSUM upper 4-bit	D	13
Sum	37	55

"YYYY" is the lower 4-bit of Sum: "7h"

Figure 36. Example of Checksum Calculation

In 2-wire, the checksum calculation value will be same in ICs which use same Slave Address and different sub address.
In 3-wire, all IC's checksum values will be same.

Error Detection - continued

Logic Error Detection

This function detects occurrence of registers (DFF) errors due to electric noise. DFFs for detection are placed around logic area. Judgement is always proceeding in DISPON status. Logic error detection will be judged after every 2 frames from DISPON command. See following sequence.

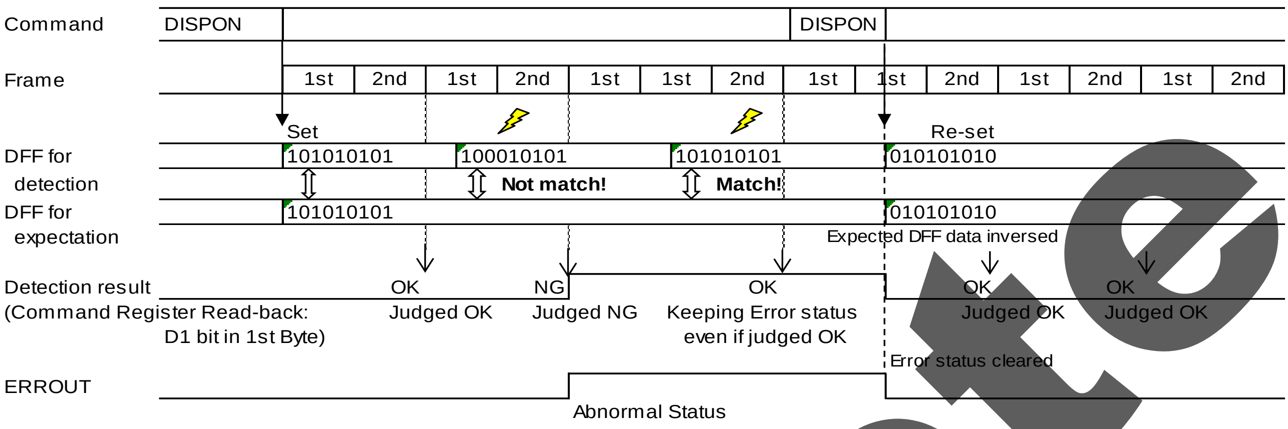


Figure 37. Sequence of Logic Error Detection

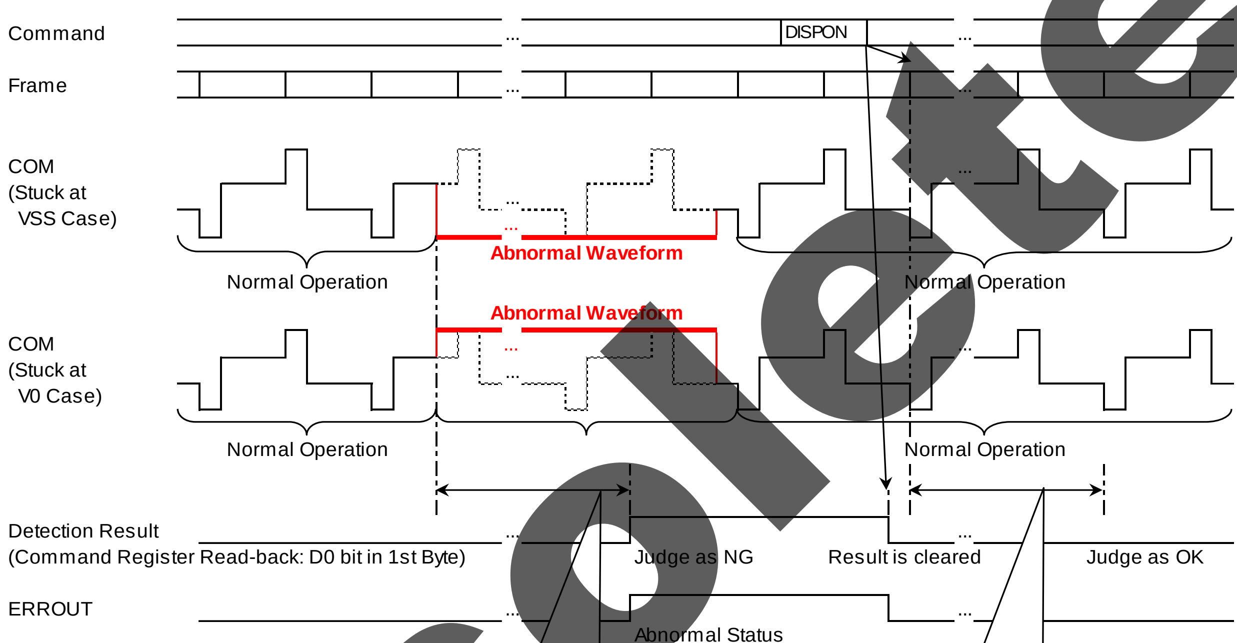
Error Detection - continued

SEG / COM Toggle Detection

This function is to detect whether SEG / COM output toggle (AC inversion) in DDRAM data bit = “1”.
Detectable status are considered as following conditions,

(1) SEG / COM waveform stuck at VSS level (SEG can detect in DDRAM data bit = “1” case only).
  (a) LCD broken.
  (b) ITO wiring connected to VSS line.
  (c) SEG / COM output broken such as short with VSS level.

(2) SEG / COM waveform stuck at V0 level (SEG can detect in DDRAM data bit = “1” case only).
  (a) LCD broken.
  (b) ITO wiring connected to VLCD line.
  (c) SEG / COM output broken such as short with VLCD / V0 level.



	Max Frame
1/4 Duty	244
1/3 Duty	183
1/2 Duty	122
Static	61

Figure 38. Sequence of SEG / COM Toggle Detection

Contact Resistance Check

COG contact resistance can be inspected by measuring resistance in DUMMY0, DUMMY1, DUMMY2 and DUMMY3 terminals. Abnormal COG bonding status can be detected if the values are outliers.

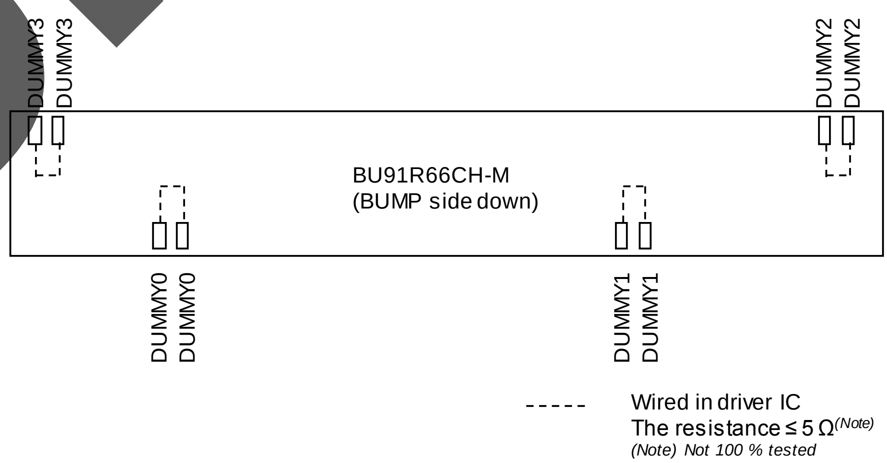


Figure 39. DUMMY PADs for the Contact Resistance Measurement

Command / Function List

Description List of Command / Function

No.	Command	Function	Identify Sub Address by SADSET	Available in CMDXTN Mode
Normal Command				
1	Mode Set 1 (MODESET1)	Display On / Off	-	No
2	Address Set1 (ADSET1)	DDRAM Address Setting (MSB side)	-	No
3	Address Set2 (ADSET2)	DDRAM Address Setting (LSB side)	-	No
4	Sub Address Set (SADSET)	IC Selecting	-	No
5	Frame Rate Set (FRSET)	Frame Frequency	-	No
6	Blink Control1 (BLKCTL1)	Blink Mode / Blink Frequency Setting	-	No
7	Blink Control2 (BLKCTL2)	Blink Area Setting	-	No
8	Command Extension (CMDXTN)	Access enable for extended commands	-	-
Extension Command				
9	Software Reset (SWRST)	Software Reset	-	Yes
10	Mode Set 2(MODESET2)	Error Detection Control	-	Yes
11	Mode Set 3(MODESET3)	Line / Frame Inversion, Frame Frequency	-	Yes
12	Contrast Setting (CNTSET)	Contrast adjustment	Yes	Yes
13	Read Control (RDCTL)	Read Control	-	Yes
14	Checksum(CHKSUM)	Checksum Trigger and Expected Value	-	Yes
15	COM Set (COMSET)	COM driving order select, Contrast adjustment	Yes	Yes

Detailed Command Description

1. Mode Set 1 (MODESET1)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	P3	*	*	*

(*: don't care)

Set Display On and Off

P3	Setup	Reset Initialize Condition
0	Display Off (DISPOFF)	○
1	Display On (DISPON)	-

Display Off: Regardless of DDRAM data, all Segment and Common output will be stopped (VSS level).
Display On: Segment and Common output will be active and will start to read the Display Data from DDRAM.

Detailed Command Description – continued

2. Address Set1 (ADSET1)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
0	0	0	0	P3	P2	P1	P0

Set upper portion of address. (P3 to P0 = "0000" in reset initialize condition)
To define internal address correctly, set ADSET1 command before ADSET2.

3. Address Set2 (ADSET2)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
0	1	0	0	P3	P2	P1	P0

Set lower portion of address. (P3 to P0 = "0000" in reset initialize condition)
To define internal address correctly, set ADSET1 command before ADSET2.
Don't set out of range address, otherwise address will be set to 00000000.
In 3-SPI case, next transferred data will be recognized as Display Data.

Internal Register	MSB Address [7]	Address [6]	Address [5]	Address [4]	Address [3]	Address [2]	Address [1]	LSB Address [0]
Command	ADSET1 P3	ADSET1 P2	ADSET1 P1	ADSET1 P0	ADSET2 P3	ADSET2 P2	ADSET2 P1	ADSET2 P0

The range of address (8-bit) is shown as bellow.
1/4, 1/3 and 1/2 Duty Drive: 00h to EFh
Static Drive: 00h to 3Bh

4. Sub Address Set (SADSET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	1	1	0	0	0	P1	P0

Set sub address to define one of BU91R6xCH sub address.
The following command can be set independently after SADSET command.
- Display Data write
- Display Data read
- Command Registers read
- Contrast Setting (CNTSET)
- COM set (COMSET)

In 2-wire Serial Interface mode

P1	P0	Available IC	Reset Initialize Condition
0	*	Master or Slave1 *(Note 1)* (MS2 = VSS)	○
1	*	Slave2 or Slave3 *(Note 1)* (MS2 = VDD)	-

(Note 1): Bit1 of Slave Address selects one of "Master / Slave1" or one of "Slave2 / Slave3".
(*: don't care)

In 3-wire Serial Interface mode

P1	P0	Available IC	Reset Initialize Condition
0	0	Master (MS2 = VSS, MS1 = VSS)	○
0	1	Slave1 (MS2 = VSS, MS1 = VDD)	-
1	0	Slave2 (MS2 = VDD, MS1 = VSS)	-
1	1	Slave3 (MS2 = VDD, MS1 = VDD)	-

Detailed Command Description – continued

5. Frame Rate Set (FRSET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	1	1	0	1	P2	P1	P0

Set Frame Frequency
In Internal Clock Mode, Frame Frequency is calculated as shown in the following table.

Table 5. Frame Frequency (Internal Clock Mode)

MODESET3		FRSET			Frame Freqency [Hz] (Number of Clock Pulses)		Reset Initilaze Condition
P1	P0	P2	P1	P0	Line Inversion	Frame Inversion	
0	0	0	0	0	65.7 (624)		-
0	0	0	0	1	74.3 (552)		-
0	0	0	1	0	85.4 (480)		-
0	0	0	1	1	122.0 (336)		-
0	0	1	0	0	131.4 (312)		-
0	0	1	0	1	142.4 (288)		○
0	0	1	1	0	155.3 (264)		-
0	0	1	1	1	170.8 (240)		-
0	1	0	0	0	189.8 (216)		-
0	1	0	0	1	213.5 (192)		-
0	1	0	1	0	244.0 (168)		-
0	1	0	1	1	284.7 (144)		-
0	1	1	0	0	427.1 (96)		-
0	1	1	0	1	569.4 (72) (Prohibited)		-
0	1	1	1	0	854.2 (48) (Prohibited)		-
0	1	1	1	1	1708.3 (24) (Prohibited)		-
1	0	0	0	0	65.7 (624)	131.4 (312)	-
1	0	0	0	1	74.3 (552)	148.6 (276)	-
1	0	0	1	0	85.4 (480)	170.8 (240)	-
1	0	0	1	1	122.0 (336)	244.0 (168)	-
1	0	1	0	0	131.4 (312)	262.8 (156)	-
1	0	1	0	1	142.4 (288)	284.7 (144)	-
1	0	1	1	0	155.3 (264)	310.6 (132)	-
1	0	1	1	1	170.8 (240)	341.7 (120)	-
1	1	0	0	0	189.8 (216)	379.6 (108)	-
1	1	0	0	1	213.5 (192)	427.1 (96)	-
1	1	0	1	0	244.0 (168)	488.1 (84)	-
1	1	0	1	1	284.7 (144)	569.4 (72) (Prohibited)	-
1	1	1	0	0	427.1 (96)	854.2 (48) (Prohibited)	-
1	1	1	0	1	569.4 (72) (Prohibited)	1138.9 (36) (Prohibited)	-
1	1	1	1	0	854.2 (48) (Prohibited)	1708.3 (24) (Prohibited)	-
1	1	1	1	1	1708.3 (24) (Prohibited)	3416.7 (12) (Prohibited)	-

In External Clock Mode, Frame Frequency is calculated as shown in following table,

Table 6. Frame Frequency (External Clock Mode)

MODESET3		FRSET			Frame Freqency [Hz]		Reset Initilaze Condition
P1	P0	P2	P1	P0	Line Inversion	Frame Inversion	
0	*	*	*	*	External Clock / 24		○
1	*	*	*	*	External Clock / 24	External Clock / 12	-

(*: don't care)

(Example 1)
EXTCLK = VDD
External Clock: 1,800 Hz
MODESET3 P1: 0
Frame Frequency = External Clock / 24 = 1,800 / 24 = 75 Hz @Line / Frame Inversion

(Example 2)
EXTCLK = VDD
External Clock: 3,500 Hz
MODESET3 P1: 1
Frame Frequency = External Clock / 24 = 3,500 / 24 = 145.8 Hz @Line Inversion
Frame Frequency = External Clock / 12 = 3,500 / 12 = 291.7 Hz @Frame Inversion

Detailed Command Description – continued

6. Blink Control1 (BLKCTL1)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	1	1	1	0	P2	P1	P0

Set Blink Mode

P2	Blink Mode	Reset Initialize Condition
0	All Segments Blink Mode	○
1	Bank Blink Mode	-

Bank Blink Mode is available in 1/2 Duty Drive and Static Drive.

Set Blink Frequency

P1	P0	Blink Frequency	Reset Initialize Condition
0	0	Off	○
0	1	32 Frames	-
1	0	64 Frames	-
1	1	128 Frames	-

About Frame Frequency calculation, refer to **5. Frame Rate Set (FRSET)**.
About Bank Blink Mode, refer to **Blink Control (Blink Timing Generator)**.

7. Blink Control2 (BLKCTL2)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	1	1	1	1	0	P1	*

(*: don't care)

Set Blink Area in 1/2 Duty Drive and Static Drive in Bank Blink Mode

P1	DDRAM Write Area	Reset Initialize Condition
0	Normal Display Area	○
1	Blink Area	-

This register is available only in 1/2 Duty Drive and Static Drive.
About data writing to blink area, refer to **Blink Control (Blink Timing Generator)**.

Detailed Command Description – continued

8. Command Extension (CMDXTN)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	0	P0

Set CMDXTN Mode Effective

P0	Mode	Reset Initialize Condition
0	Ineffective CMDXTN Mode (Normal Mode)	○
1	CMDXTN Mode (Extension Mode)	-

The following extension commands are accessible only in CMDXTN mode,

1. SWRST
2. MODESET2
3. MODESET3
4. CNTSET
5. RDCTL
6. CHKSUM
7. COMSET

To access normal command such as DISPON etc., set P0 = “0” (ineffective CMDXTN mode).
Refer to **Command / Function List**.

9. Software Reset (SWRST)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	*	*	P0

(*: don’t care)

This register can be accessed in CMDXTN mode only.

Set software reset effective

P0	Operation	Reset Initialize Condition
0	No Operation	○
1	Software Reset Execute	-

When “Software Reset” is executed, BU91R66CH-M will be reset to initial condition.
Refer to **POR and Reset Initialize Condition.**

Detailed Command Description – continued

10. Mode Set 2 (MODESET2)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	0	0	1	P3	P2	P1	P0

This register can be accessed in CMDXTN mode only.

Set Glass breaking detection to enable

P3	Setup	Reset Initialize Condition
0	Disable	○
1	Enable	-

Set Checksum detection to enable

P2	Setup	Reset Initialize Condition
0	Disable	○
1	Enable	-

Set Logic error detection to enable

P1	Setup	Reset Initialize Condition
0	Disable	○
1	Enable	-

Set SEG / COM toggle detection to enable

P0	Setup	Reset Initialize Condition
0	Disable	○
1	Enable	-

ERROUT output function will be effective when any bit of P3 to P0 is set to enable, refer to **Detailed Command Description**.

11. Mode Set 3 (MODESET3)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	0	1	0	0	P2	P1	P0

This register can be accessed in CMDXTN mode only.

Set LCD Driving Mode

P2	Driving Mode	Reset Initialize Condition
0	Line Inversion Mode	○
1	Frame Inversion Mode	-

Power consumption is reduced in the following order: Line inversion > Frame inversion
Typically, when driving large capacitance LCD, Line inversion will increase the influence of crosstalk.
Regarding driving waveform, refer to **LCD Driving Waveform**.

Set x2 Frame frequency in Frame inversion mode

P1	Mode	Reset Initialize Condition
0	Normal Frequency Mode	○
1	x2 Frequency in Frame Inversion	-

This command is only effective in Frame inversion mode.
In detail, refer to **5. Frame Rate Set (FRSET)**.

Set Frame Frequency Mode

P0	Frame Frequency Mode	Reset Initialize Condition
0	Normal Frequency Mode	○
1	High Frequency Mode	-

In detail, refer to **5. Frame Rate Set (FRSET)**.

Detailed Command Description – continued

12. Contrast Setting (CNTSET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	0	1	1	P3	P2	P1	P0

This register can be accessed in CMDXTN mode only.
This command can set sub address individually by SADSET command.

Set EVR for Contrast adjustment.
BU91R66CH-M is able to control V0 voltage level (the maximum level voltage of LCD driving) by a 32-step electrical volume register (EVR).

Table 7. V0 Voltage Setting

Unit: V

COMSET	CNTSET				Formula	VLCD [V]							Reset Initialize Condition
P3	P3	P2	P1	P0		6.0	5.5	5.0	4.0	3.5	3.0	2.5	
0	0	0	0	0	1.000 * VLCD	6.000	5.500	5.000	4.000	3.500	3.000	2.500	O
0	0	0	0	1	0.967 * VLCD	5.802	5.323	4.839	3.871	3.387	2.903	2.419	-
0	0	0	1	0	0.937 * VLCD	5.622	5.156	4.688	3.750	3.281	2.813	2.344	-
0	0	0	1	1	0.909 * VLCD	5.454	5.000	4.545	3.636	3.182	2.727	2.273	-
0	0	1	0	0	0.882 * VLCD	5.292	4.853	4.412	3.529	3.088	2.647	2.206	-
0	0	1	0	1	0.857 * VLCD	5.142	4.714	4.286	3.429	3.000	2.571	2.143	-
0	0	1	1	0	0.833 * VLCD	4.998	4.583	4.167	3.333	2.917	2.500	2.083	-
0	0	1	1	1	0.810 * VLCD	4.860	4.459	4.054	3.243	2.838	2.432	2.027	-
0	1	0	0	0	0.789 * VLCD	4.734	4.342	3.947	3.158	2.763	2.368	1.974	-
0	1	0	0	1	0.769 * VLCD	4.614	4.231	3.846	3.077	2.692	2.308	1.923	-
0	1	0	1	0	0.750 * VLCD	4.500	4.125	3.750	3.000	2.625	2.250	1.875	-
0	1	0	1	1	0.731 * VLCD	4.386	4.024	3.659	2.927	2.561	2.195	1.829	-
0	1	1	0	0	0.714 * VLCD	4.284	3.929	3.571	2.857	2.500	2.143	1.786	-
0	1	1	0	1	0.697 * VLCD	4.182	3.837	3.488	2.791	2.442	2.093	1.744	-
0	1	1	1	0	0.681 * VLCD	4.086	3.750	3.409	2.727	2.386	2.045	1.705	-
0	1	1	1	1	0.666 * VLCD	3.996	3.667	3.333	2.667	2.333	2.000	1.667	-
1	0	0	0	0	0.652 * VLCD	3.912	3.587	3.261	2.609	2.283	1.957	1.630	-
1	0	0	0	1	0.638 * VLCD	3.828	3.511	3.191	2.553	2.234	1.915	1.596	-
1	0	0	1	0	0.625 * VLCD	3.750	3.438	3.125	2.500	2.188	1.875	1.563	-
1	0	0	1	1	0.612 * VLCD	3.672	3.367	3.061	2.449	2.143	1.837	1.531	-
1	0	1	0	0	0.600 * VLCD	3.600	3.300	3.000	2.400	2.100	1.800	1.500	-
1	0	1	0	1	0.588 * VLCD	3.528	3.235	2.941	2.353	2.059	1.765	1.471	-
1	0	1	1	0	0.576 * VLCD	3.456	3.173	2.885	2.308	2.019	1.731	1.442	-
1	0	1	1	1	0.566 * VLCD	3.396	3.113	2.830	2.264	1.981	1.698	1.415	-
1	1	0	0	0	0.555 * VLCD	3.330	3.056	2.778	2.222	1.944	1.667	1.389	-
1	1	0	0	1	0.545 * VLCD	3.270	3.000	2.727	2.182	1.909	1.636	1.364	-
1	1	0	1	0	0.535 * VLCD	3.210	2.946	2.679	2.143	1.875	1.607	1.339	-
1	1	0	1	1	0.526 * VLCD	3.156	2.895	2.632	2.105	1.842	1.579	1.316	-
1	1	1	0	0	0.517 * VLCD	3.102	2.845	2.586	2.069	1.810	1.552	1.293	-
1	1	1	0	1	0.508 * VLCD	3.048	2.797	2.542	2.034	1.780	1.525	1.271	-
1	1	1	1	0	0.500 * VLCD	3.000	2.750	2.500	2.000	1.750	1.500	1.250	-
1	1	1	1	1	0.491 * VLCD	2.946	2.705	2.459	1.967	1.721	1.475	1.230	-

Prohibited Setting

Avoid setting EVR of "V0 < 2.5 V" and "V0 > VLCD – 0.6 V" condition. BU91R66CH-M output voltage will be unstable in such conditions.

Detailed Command Description – continued

13. Read Control (RDCTL)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	1	0	0	1	*	P1	P0

(*: don't care)

This register can be accessed in CMDXTN mode only.

Set Read enable (This bit is available in 3SPI mode only. In 2-wire, this bit is undefined.)

P1	Read_en	Reset Initialize Condition
0	Read disable (Write Mode)	○
1	Read enable (Read Mode)	-

Set Read data

P0	Read_mode	Reset Initialize Condition
0	Command Registers Read	○
1	DDRAM Data Read	-

14. Checksum (CHKSUM)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	1	0	1	P3	P2	P1	P0

This register can be accessed in CMDXTN mode only.

P3 to P0: The sum of all Command Registers value for interface checksum function. Set this value after calculating the sum of each Command Registers value. In detail, refer to **Checksum Detection**.

Detailed Command Description – continued

15. COM Set (COMSET)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1	1	1	0	P3	P2	P1	P0

This register can be accessed in CMDXTN mode only.
This command can set sub address individually by SADSET command.

P3: Set MSB of CNTSET
Refer to Contrast Setting command (CNTSET).

P2 to P0: Set COM scanning order of COMA, COMB and COMC individually.
- P2: Set COMC Scanning Order
- P1: Set COMB Scanning Order
- P0: Set COMA Scanning Order

P2 (COMC)	P1 (COMB)	P0 (COMA)	Duty Drive	Toggle Order of COM*0 to COM*3	Reset Initialize Condition
0	0	0	1/4 Duty	COM*0→COM*1→COM*2→COM*3	○
			1/3 Duty	COM*0→COM*1→COM*2(Note 1)	
			1/2 Duty	COM*0→COM*1(Note 2)	
			Static	COM*0(Note 3)	
1	1	1	1/4 Duty	COM*3→COM*2→COM*1→COM*0	-
			1/3 Duty	COM*3→COM*2→COM*1(Note 1)	
			1/2 Duty	COM*1→COM*0(Note 2)	
			Static	COM*0(Note 3)	

(*: A for P0, or B for P1, or C for P3)
(*Note 1*) COMA3 = COMA0
(*Note 2*) COMA2 = COMA0, COMA3 = COMA1
(*Note 3*) COMA1 / 2 / 3 = COMA0

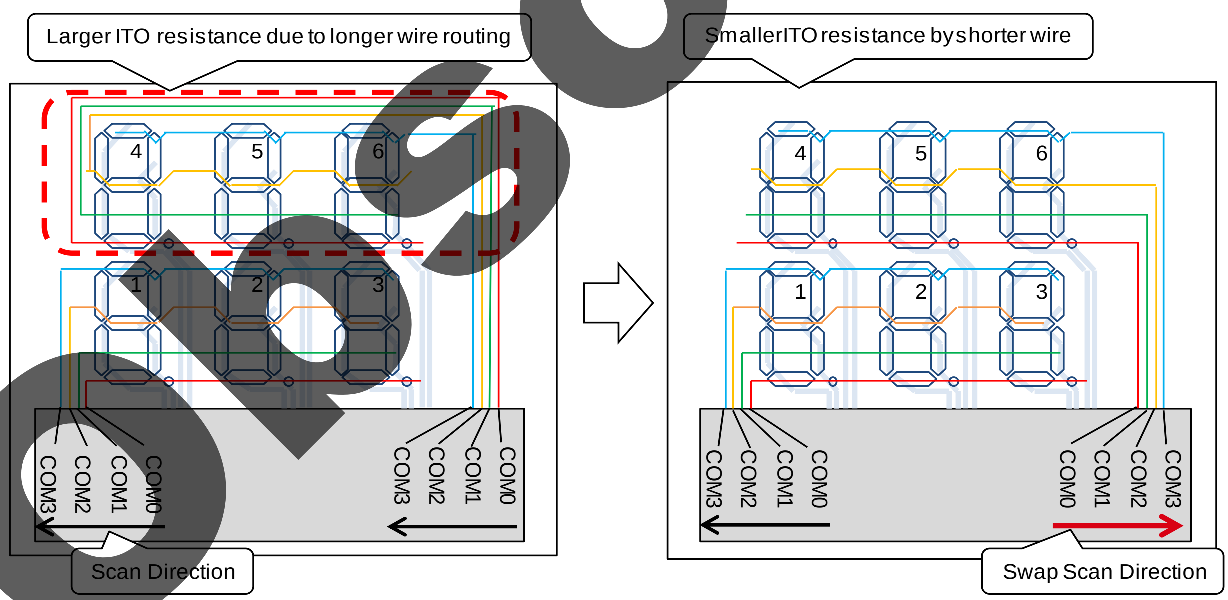
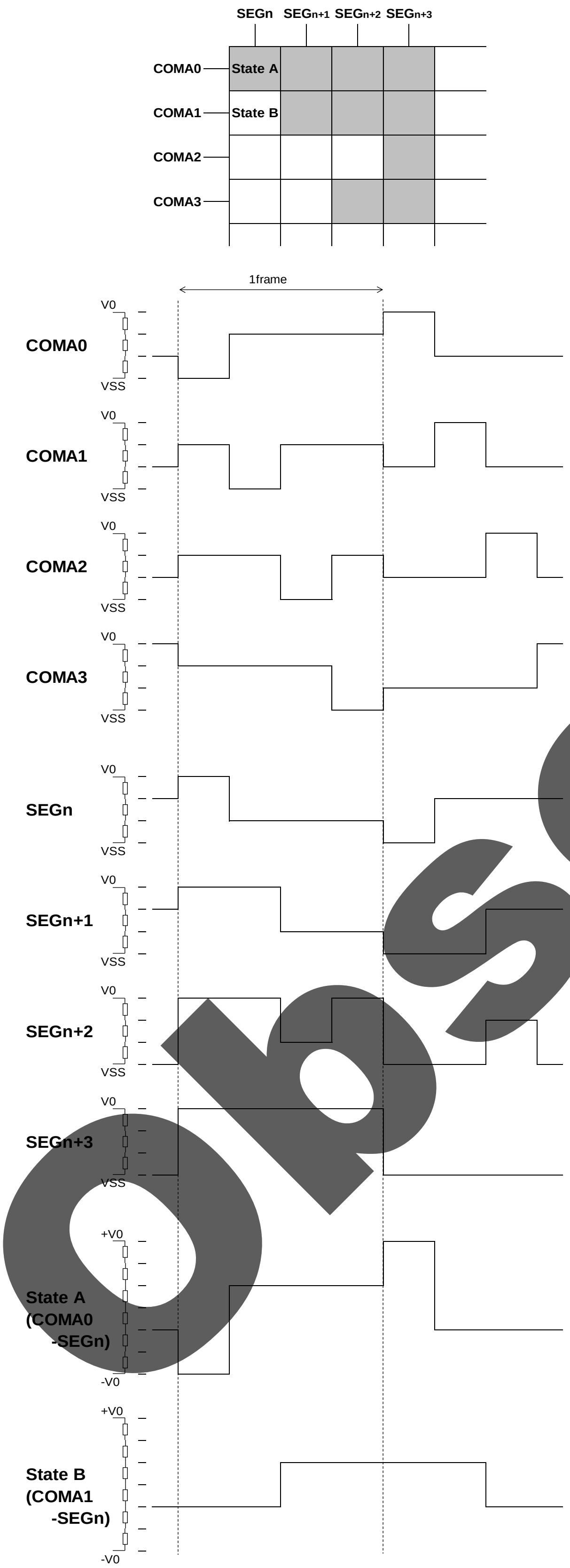


Figure 40. COM Scan Direction Image

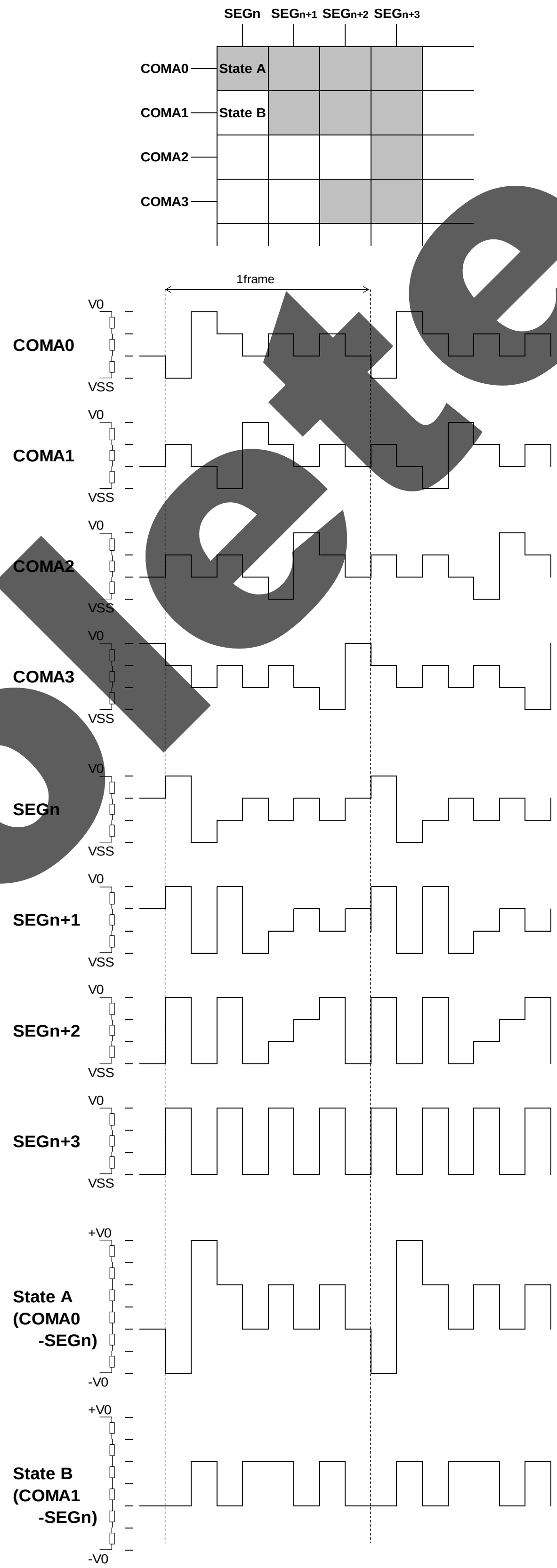
LCD Driving Waveform

1/3 Bias, 1/4 Duty Drive

Frame Inversion



Line Inversion

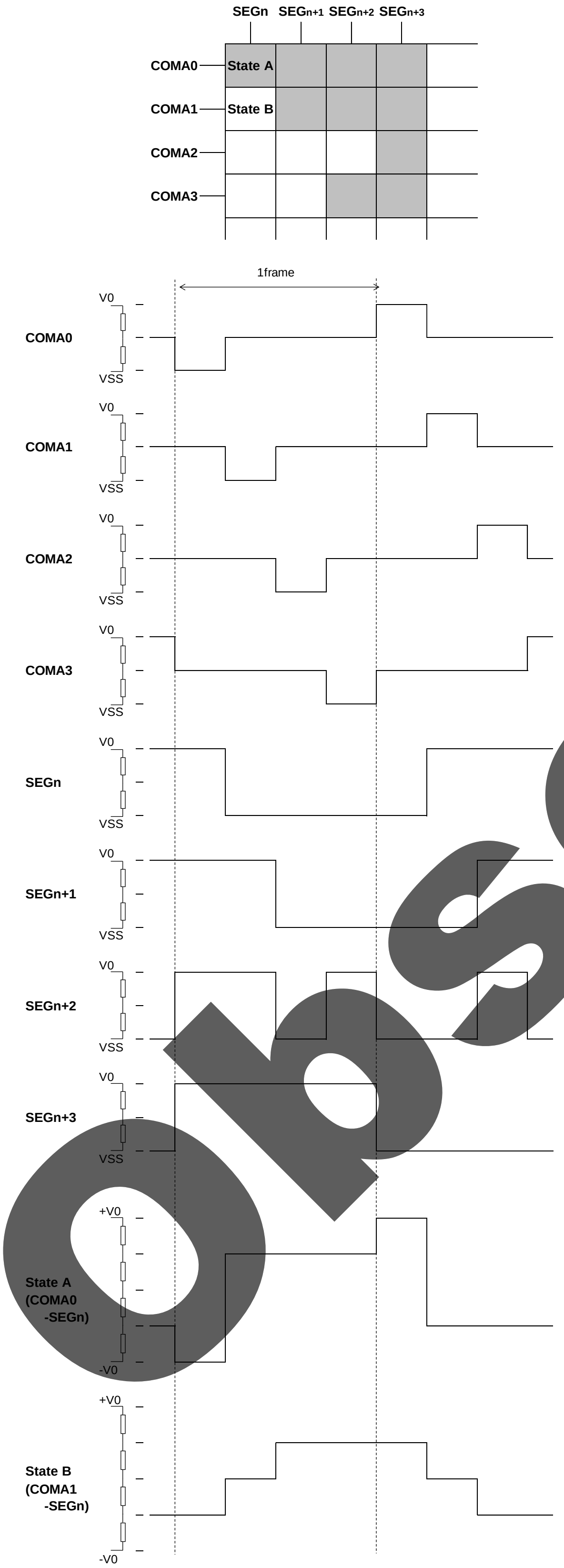


COMSET P2 = “0”, Normally white type LCD case

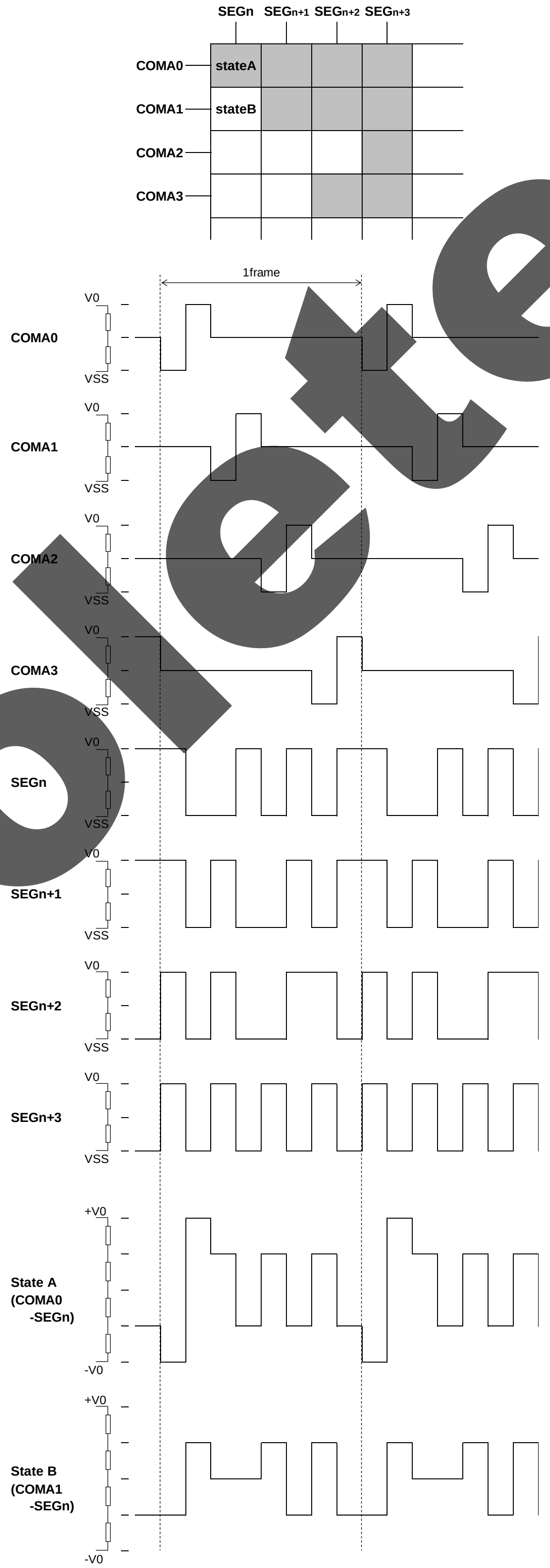
LCD Driving Waveform - continued

1/2 Bias, 1/4 Duty Drive

Frame Inversion



Line Inversion

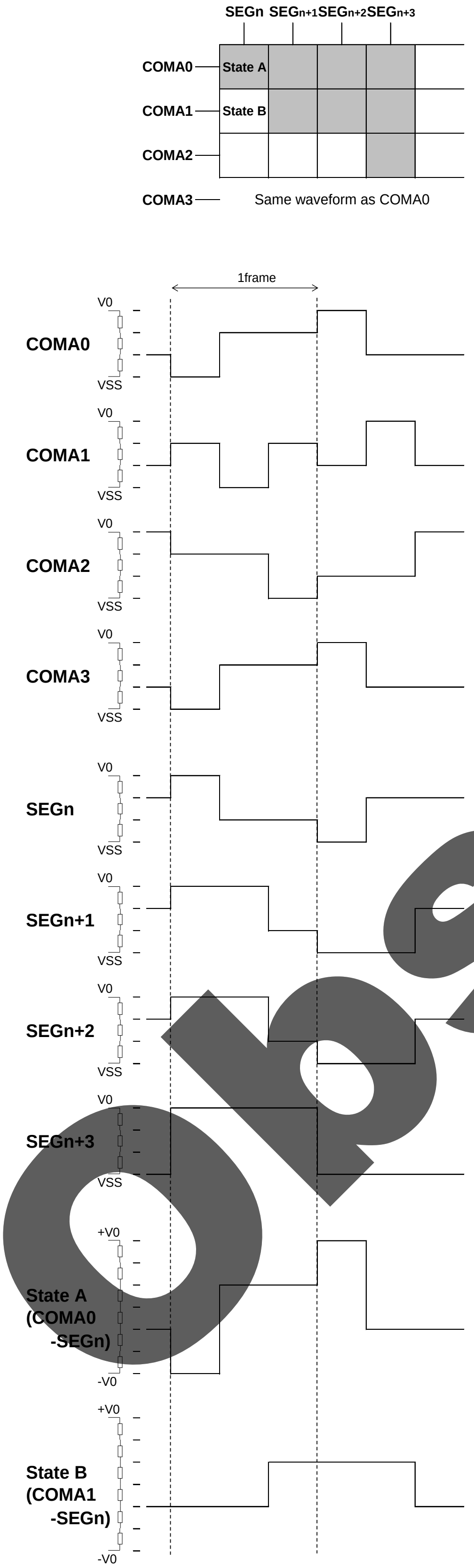


COMSET P2 = “0”, Normally white type LCD case

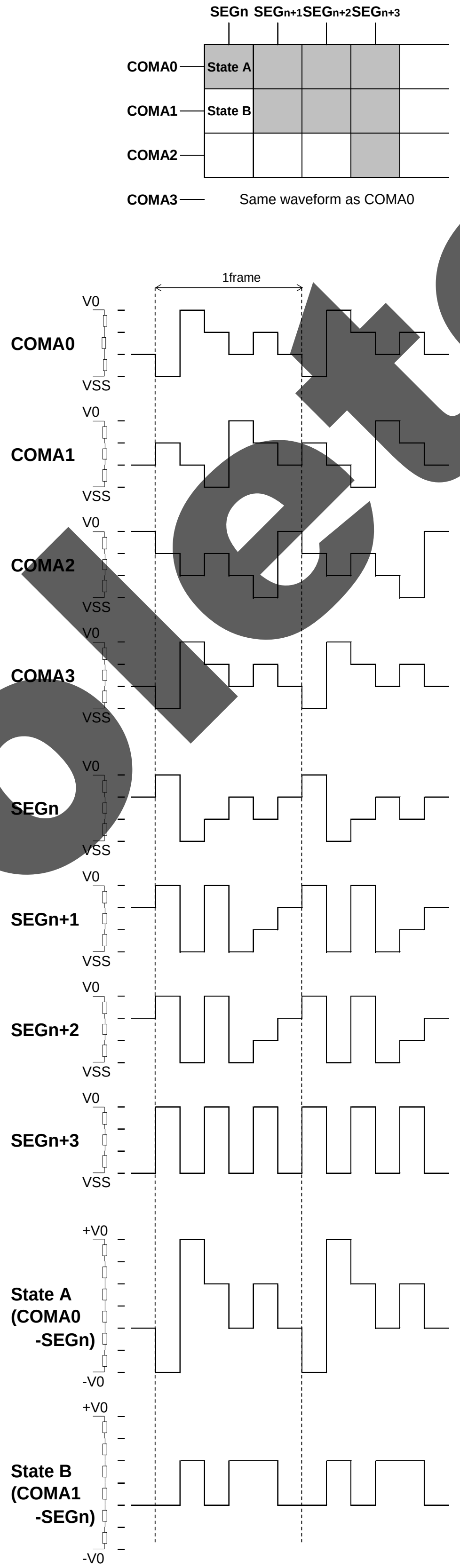
LCD Driving Waveform - continued

1/3 Bias, 1/3 Duty Drive

Frame Inversion



Line Inversion

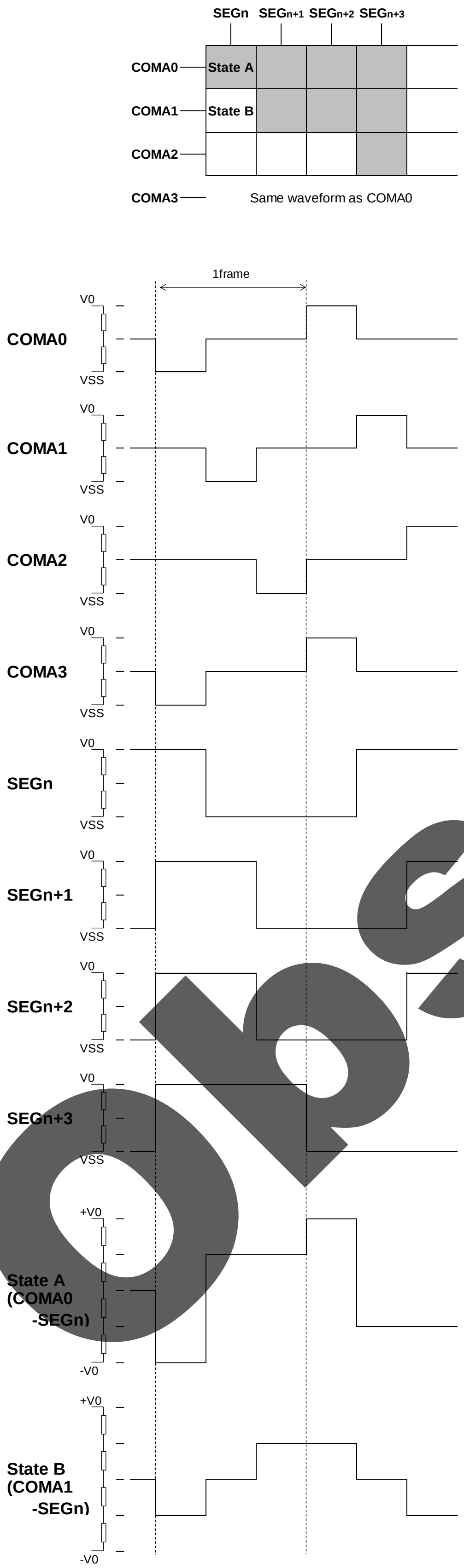


COMSET P2 = “0”, Normally white type LCD case

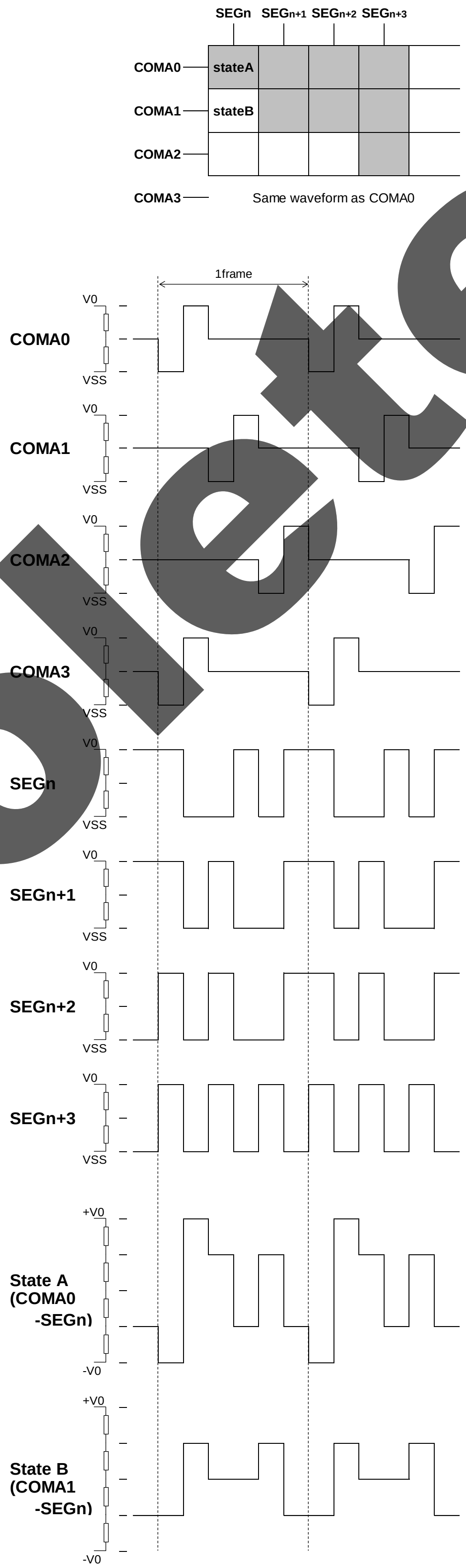
LCD Driving Waveform - continued

1/2 Bias, 1/3 Duty Drive

Frame Inversion



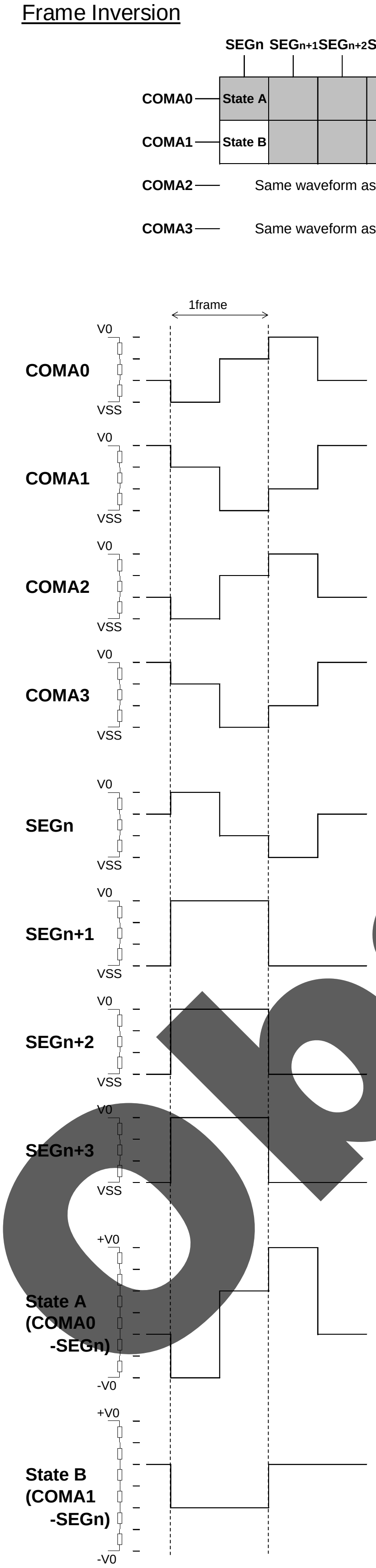
Line Inversion

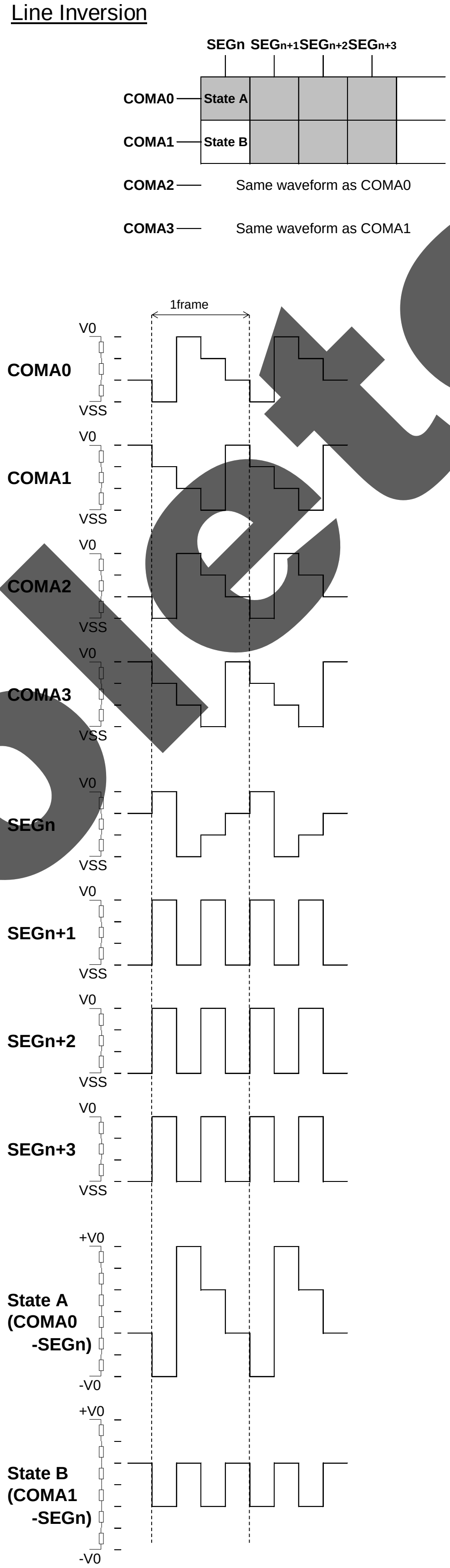


COMSET P2 = “0”, Normally white type LCD case

LCD Driving Waveform - continued

1/3 Bias, 1/2 Duty Drive



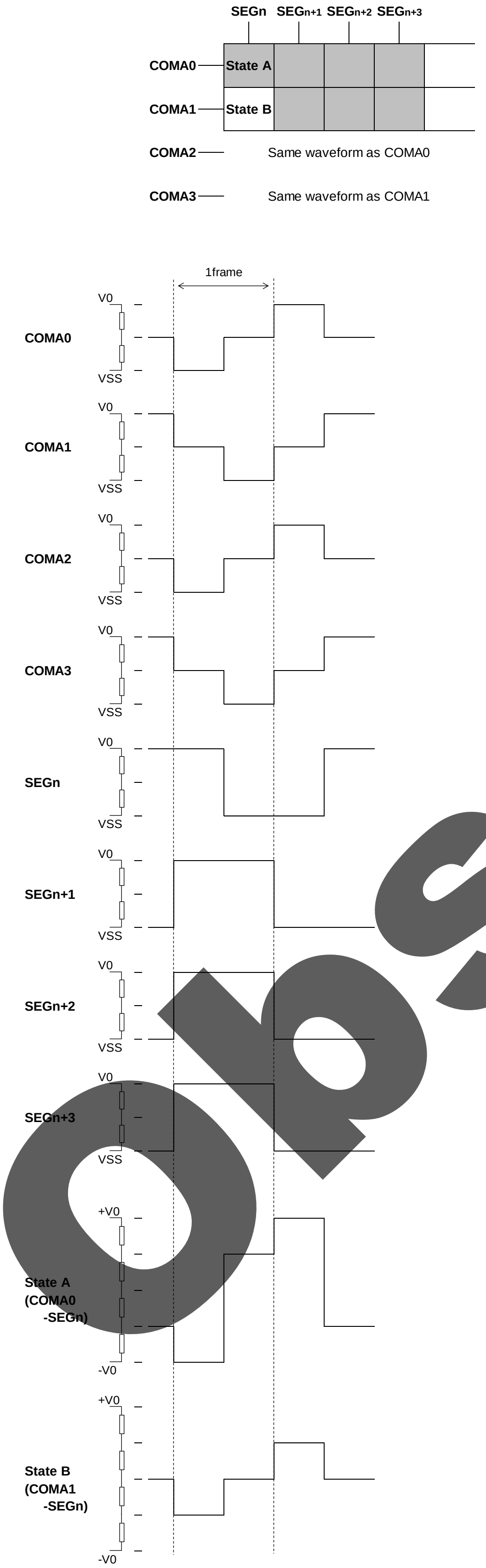


COMSET P2 = “0”, Normally white type LCD case

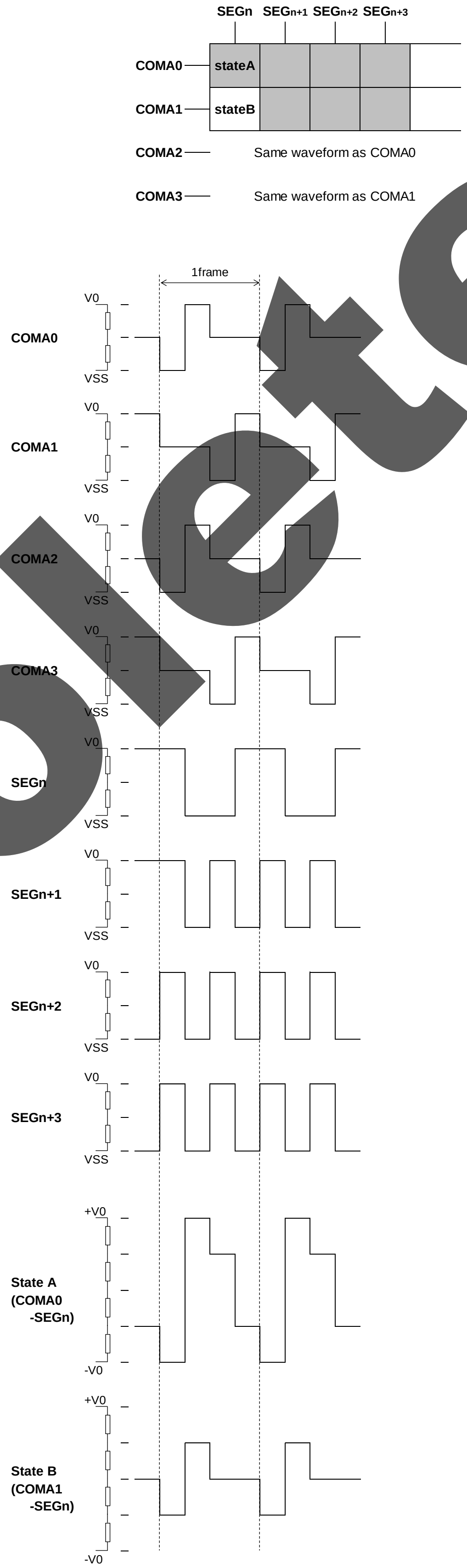
LCD Driving Waveform - continued

1/2 Bias, 1/2 Duty Drive

Frame Inversion



Line Inversion

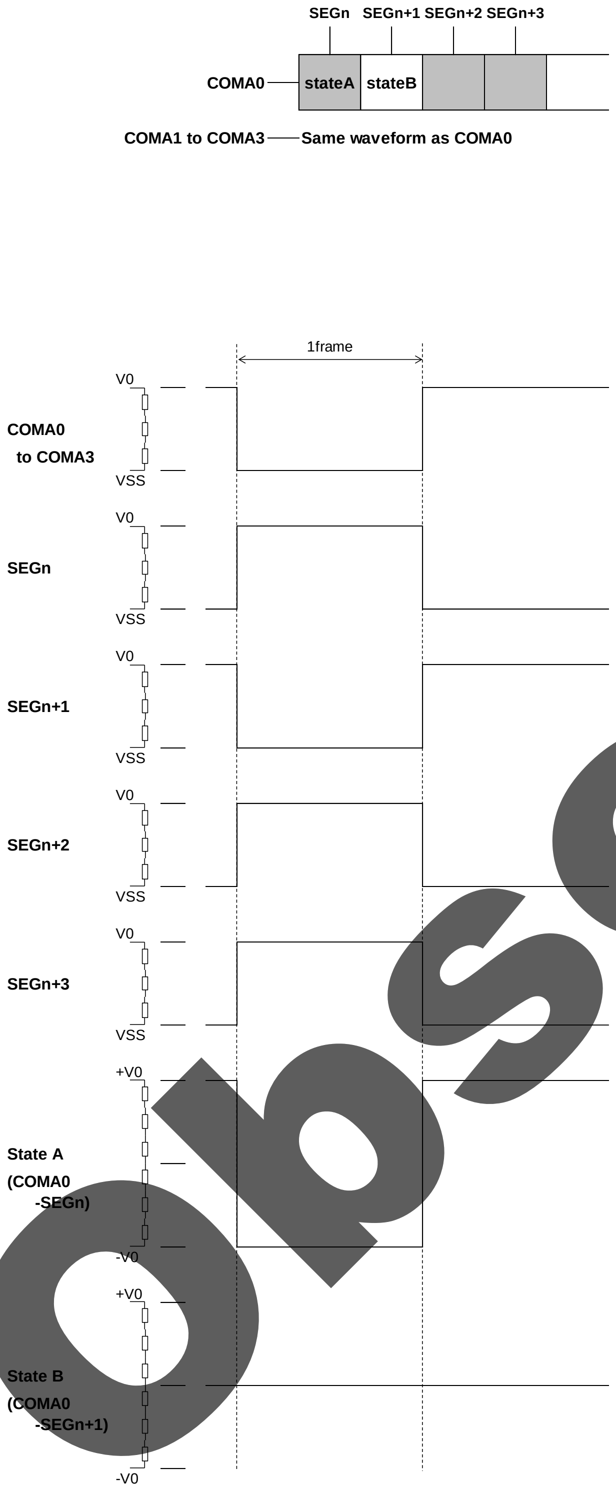


COMSET P2 = “0”, Normally white type LCD case

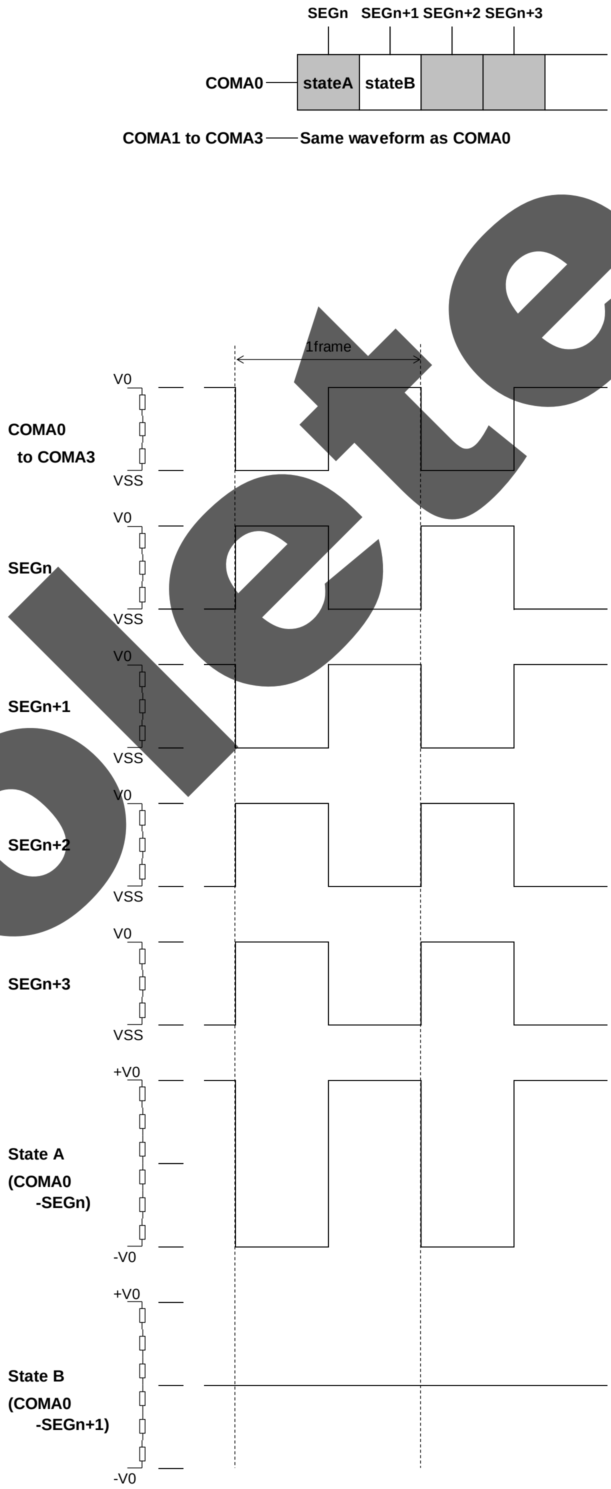
LCD Driving Waveform - continued

Static Drive

Frame Inversion



Line Inversion



Normally white type LCD case

Example of Display Data

In case of LCD layout pattern shown in Figure 41. Example COM Line Pattern and Figure 42. Example SEG Line Pattern and DDRAM data shown in Table 8. DDRAM Data Example, display pattern will be shown as in Figure 43. Example Display Pattern.

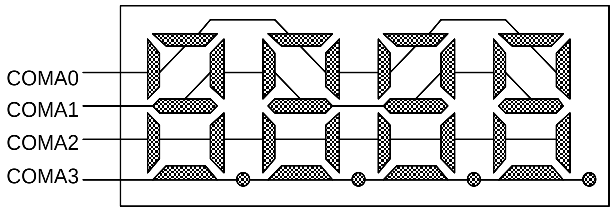


Figure 41. Example COM Line Pattern

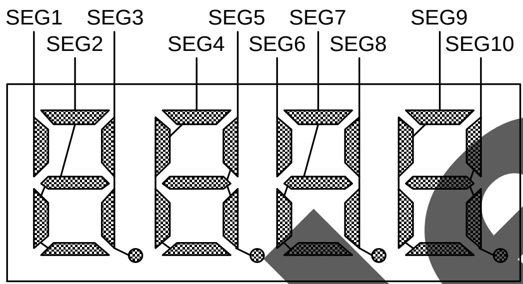


Figure 42. Example SEG Line Pattern

Table 8. DDRAM Data Example

	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COMA0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
COMA1	0	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
COMA2	0	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
COMA3	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Address	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h

(The COM scan order: COMSET P0 = “0”)

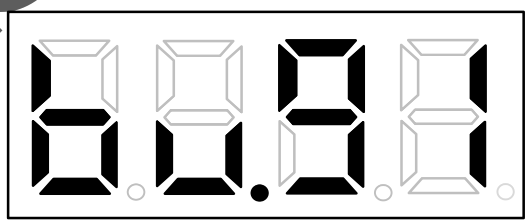


Figure 43. Example Display Pattern

Initialize Sequence

Follow the Power On sequence below to set IC to initial reset condition.

Power On
↓
START Condition
↓
9 clock pulses in SCL with SDA = High level
↓
STOP Condition
↓
START Condition
↓
9 clock pulses in SCL with SDA = High level
↓
STOP Condition
↓
START Condition
↓
Issue Slave Address
↓
Issue Control Byte
↓
Issue CMDXTN (Enter to Extension Mode)
↓
Issue SWRST (Execute Software Reset).

After Power On and before sending initialize sequence, each register value, DDRAM address and DDRAM data are random if POR is disabled by TR = VDD or Power On sequence cannot keep the conditions in **Figure 45. Power On / Off Waveform**.

Start Sequence

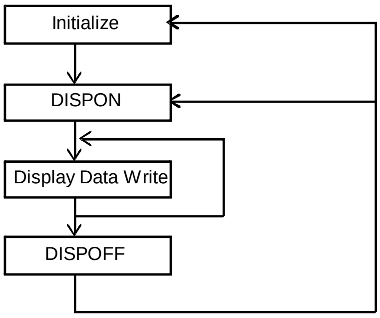
Start Sequence Example1

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power On	-	-	-	-	-	-	-	-	VDD = 0 V→3.3 V (t_R = 1 ms), VLCD = 0 V→5.0 V
2	Wait 100 µs	-	-	-	-	-	-	-	-	Initialize BU91R66CH-M
3	START	-	-	-	-	-	-	-	-	START Condition
4	Dummy Byte	1	1	1	1	1	1	1	1	9 clock pulses in SCL with SDA = High level
5	STOP	-	-	-	-	-	-	-	-	STOP Condition
6	START	-	-	-	-	-	-	-	-	START Condition
7	Dummy Byte	1	1	1	1	1	1	1	1	9 clock pulses in SCL with SDA = High level
8	STOP	-	-	-	-	-	-	-	-	STOP Condition
9	START	-	-	-	-	-	-	-	-	START Condition
10	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
11	Control Byte	0	0	0	0	0	0	0	0	Issue Control Byte
12	CMDXTN	1	1	1	1	1	1	0	1	Enter to Extension Mode
13	SWRST	1	0	0	0	0	0	0	1	Software Reset
14	STOP	-	-	-	-	-	-	-	-	STOP Condition
15	START	-	-	-	-	-	-	-	-	START Condition
16	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
17	Control Byte	0	0	0	0	0	0	0	0	Issue Control Byte
18	MODESET1	1	1	0	0	0	0	0	0	Display Off
19	CMDXTN	1	1	1	1	1	1	0	1	Enter to Extension Mode
20	MODESET2	1	0	0	1	0	0	0	0	All detections: disabled
21	MODESET3	1	0	1	0	0	0	0	0	Line Inversion, Normal Frequency Mode
22	CNTSET	1	0	1	1	0	0	0	0	V0 = 1.000 x VLCD level
23	RDCTL	1	1	0	0	1	0	0	0	Read setting (disabled)
24	COMSET	1	1	1	0	0	0	0	0	COM Set
25	CMDXTN	1	1	1	1	1	1	0	0	Enter to Normal Mode
26	FRSET	1	1	1	0	1	1	0	1	Frame frequency = 142.4 Hz
27	BLKCTL1	1	1	1	1	0	0	0	0	Blink off
28	BLKCTL2	1	1	1	1	1	0	0	0	Data write access to Normal Display Area
29	SADSET	1	1	1	0	0	0	0	0	Sub Address Set
30	ADSET1	0	0	0	0	0	0	0	0	Address Set1 (MSB side 4-bit)
31	ADSET2	0	1	0	0	0	0	0	0	Address Set2 (LSB side 4-bit)
32	STOP	-	-	-	-	-	-	-	-	STOP Condition
33	START	-	-	-	-	-	-	-	-	START Condition
34	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
35	Control Byte	0	1	0	0	0	0	0	0	Issue Control Byte
36	Display Data	*	*	*	*	*	*	*	*	Address 00h to 01h
	Display Data	*	*	*	*	*	*	*	*	Address 02h to 03h
	:	:	:	:	:	:	:	:	:	:
	Display Data	*	*	*	*	*	*	*	*	Address EEh to EFh
37	STOP	-	-	-	-	-	-	-	-	STOP Condition
38	START	-	-	-	-	-	-	-	-	START Condition
39	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
40	Control Byte	0	0	0	0	0	0	0	0	Issue Control Byte
41	MODESET1	1	1	0	0	1	0	0	0	Display On
42	STOP	-	-	-	-	-	-	-	-	STOP Condition

(*: don't care)

Start Sequence – continued

Start Sequence Example2



Initialize Sequence

DISPON Sequence

Display Data Write Sequence

DISPOFF Sequence

BU91R66CH-M is initialized with “Initialize Sequence”, starts to display with “DISPON Sequence”, updates Display Data with “Display Data Write Sequence” and stops the display with “DISPOFF Sequence”.
Execute “DISPON Sequence” when MCU starts display again.

Initialize Sequence

Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
VDD on									
VLCD on									
Wait for 100 µs									
START									
Dummy Byte	1	1	1	1	1	1	1	1	Keep high in ACK bit
STOP									
START									
Dummy Byte	1	1	1	1	1	1	1	1	Keep high in ACK bit
STOP									
START									
Slave Address	0	1	1	1	1	1	0	0	
Control Byte	0	0	0	0	0	0	0	0	
CMDXTN	1	1	1	1	1	1	0	1	Enter to Extension Mode
SWRST	1	0	0	0	0	0	0	1	Software Reset
STOP									
START									
Slave Address	0	1	1	1	1	1	0	0	
Control Byte	0	0	0	0	0	0	0	0	
MODESET1	1	1	0	0	0	0	0	0	Display Off
CMDXTN	1	1	1	1	1	1	0	1	Enter to Extension Mode
MODESET2	1	0	0	1	0	0	0	0	All detections: disabled
MODESET3	1	0	1	0	0	0	0	0	Inversion / FR setting
CNTSET	1	0	1	1	0	0	0	0	Contrast Set
RDCTL	1	1	0	0	1	0	0	0	Read setting
COMSET	1	1	1	0	0	0	0	0	COM Set
CMDXTN	1	1	1	1	1	1	0	0	Enter to Normal Mode
FRSET	1	1	1	0	1	1	0	1	Frame Frequency
BLKCTL1	1	1	1	1	0	0	0	0	Blink setting
BLKCTL2	1	1	1	1	1	0	0	0	Data write setting
SADSET	1	1	1	0	0	0	0	0	Sub Address Set
ADSET1	0	0	0	0	0	0	0	0	Address Set1
ADSET2	0	1	0	0	0	0	0	0	Address Set2
STOP									
START									
Slave Address	0	1	1	1	1	1	0	0	
Control Byte	0	1	0	0	0	0	0	0	
Display Data	*	*	*	*	*	*	*	*	
:									
STOP									

DISPON Sequence

Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
START									
Slave Address	0	1	1	1	1	1	0	0	
Control Byte	0	0	0	0	0	0	0	0	
CMDXTN	1	1	1	1	1	1	0	1	Enter to Extension Mode
MODESET2	1	0	0	1	0	0	0	0	All detections: disabled
MODESET3	1	0	1	0	0	0	0	0	Inversion / FR setting
CNTSET	1	0	1	1	0	0	0	0	Contrast Set
RDCTL	1	1	0	0	1	0	0	0	Read setting
COMSET	1	1	1	0	0	0	0	0	COM Set
CMDXTN	1	1	1	1	1	1	0	0	Enter to Normal Mode
FRSET	1	1	1	0	1	1	0	1	Frame Frequency
BLKCTL1	1	1	1	1	0	0	0	0	Blink setting
BLKCTL2	1	1	1	1	1	0	0	0	Data write setting
MODESET1	1	1	0	0	1	0	0	0	Display On
STOP									

Display Data Write Sequence

Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
START									
Slave Address	0	1	1	1	1	1	0	0	
Control Byte	0	0	0	0	0	0	0	0	
MODESET1	1	1	0	0	1	0	0	0	Display On
CMDXTN	1	1	1	1	1	1	0	1	Enter to Extension Mode
MODESET2	1	0	0	1	0	0	0	0	All detections: disabled
MODESET3	1	0	1	0	0	0	0	0	Inversion / FR setting
CNTSET	1	0	1	1	0	0	0	0	Contrast Set
RDCTL	1	1	0	0	1	0	0	0	Read setting
COMSET	1	1	1	0	0	0	0	0	COM Set
CMDXTN	1	1	1	1	1	1	0	0	Enter to Normal Mode
FRSET	1	1	1	0	1	1	0	1	Frame Frequency
BLKCTL1	1	1	1	1	0	0	0	0	Blink setting
BLKCTL2	1	1	1	1	1	0	0	0	Data write setting
SADSET	1	1	1	0	0	0	0	0	Sub Address Set
ADSET1	0	0	0	0	0	0	0	0	Address Set1
ADSET2	0	1	0	0	0	0	0	0	Address Set2
STOP									
START									
Slave Address	0	1	1	1	1	1	0	0	
Control Byte	0	1	0	0	0	0	0	0	
Display Data	*	*	*	*	*	*	*	*	
:									
STOP									

DISPOFF Sequence

Input	D7	D6	D5	D4	D3	D2	D1	D0	Description
START									
Slave Address	0	1	1	1	1	1	0	0	
Control Byte	0	0	0	0	0	0	0	0	
MODESET1	1	1	0	0	0	0	0	0	Display Off
STOP									

(*: don’t care)

Abnormal operation may occur in BU91R66CH-M due to the effect of noise or other external factor. To avoid this phenomenon, it is highly recommended to input command according to sequence described above during initialization, Display On / Off and refresh of Display Data.

Cautions in Power On / Off

Please keep Power On / Off sequence as below waveform. To prevent incorrect display, malfunction and abnormal current, VDD must be turned on before VLCD in power up sequence. VDD must be turned off after VLCD in power down sequence. Please satisfies t1 > 0 ns, t2 > 0 ns.
To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

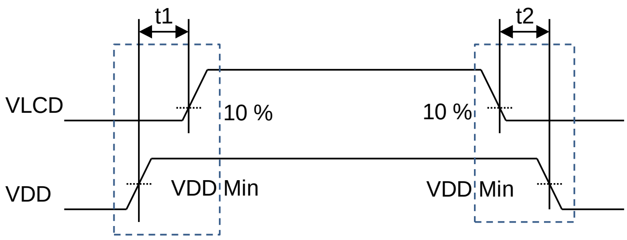


Figure 44. Recommended Power On / Off Sequence

BU91R66CH-M has "POR" (Power On Reset) circuit and Software Reset function. Keep the following recommended Power On conditions in order to power up properly.
Set power up conditions to meet the recommended t_R, t_F, t_{OFF}, and V_{BOT} specification below in order to ensure POR operation. Set terminal TR = VSS to enable POR circuit.

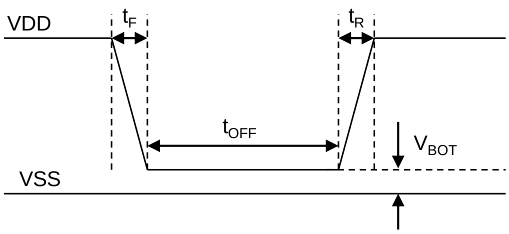


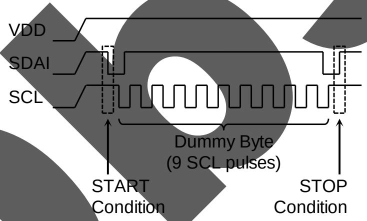
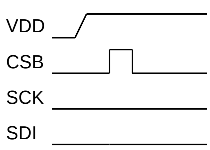
Figure 45. Power On / Off Waveform

Recommended condition of t_R, t_F, t_{OFF}, V_{BOT} (Ta = 25 °C)

t_R *(Note)*	t_F *(Note)*	t_{OFF} *(Note)*	V_{BOT} *(Note)*
1 ms to 500 ms	1 ms to 500 ms	Min 20 ms	Less than 0.1 V

(Note) This function is guaranteed by design, not tested in production process.

If it is difficult to keep above conditions, execute the following sequence as quickly as possible after Power On. Setting TR = VDD disables the POR circuit, in such case, execute the following sequence. Note that however it cannot accept command while supply is unstable or below the minimum supply range. Note also that software reset is not a complete alternative to POR function.

2-wire Serial Interface	3-wire Serial Interface
1. Generate one dummy byte with START and STOP Conditions SDAI must be "1" as data.  Figure 46. Dummy Clock / STOP / START Condition	1. Set CSB to High level.  Figure 47. CSB Timing
2. Execute Software Reset as follows Send START Condition Send Slave Address (7Ch, 7Eh, 70h or 72h) Send Control Byte (00h) Send CMDXTN command (FDh) Send SWRST command (81h)	2. Set CSB to low level, then execute Software Reset as follows: Send CMDXTN command (FDh) Send SWRST command (81h)

Display Off Operation in External Clock Mode

Clock stop timing in Display Off

After receiving MODESET1 Display Off (DISPOFF), BU91R66CH-M enters to DISPOFF sequence synchronized with frame then Segment and Common terminals output VSS level.

Therefore, in External Clock Mode, it is necessary to input the external clock (minimum 26 clock pulses) based on each Frame Frequency setting after sending MODESET1 DISPOFF command.

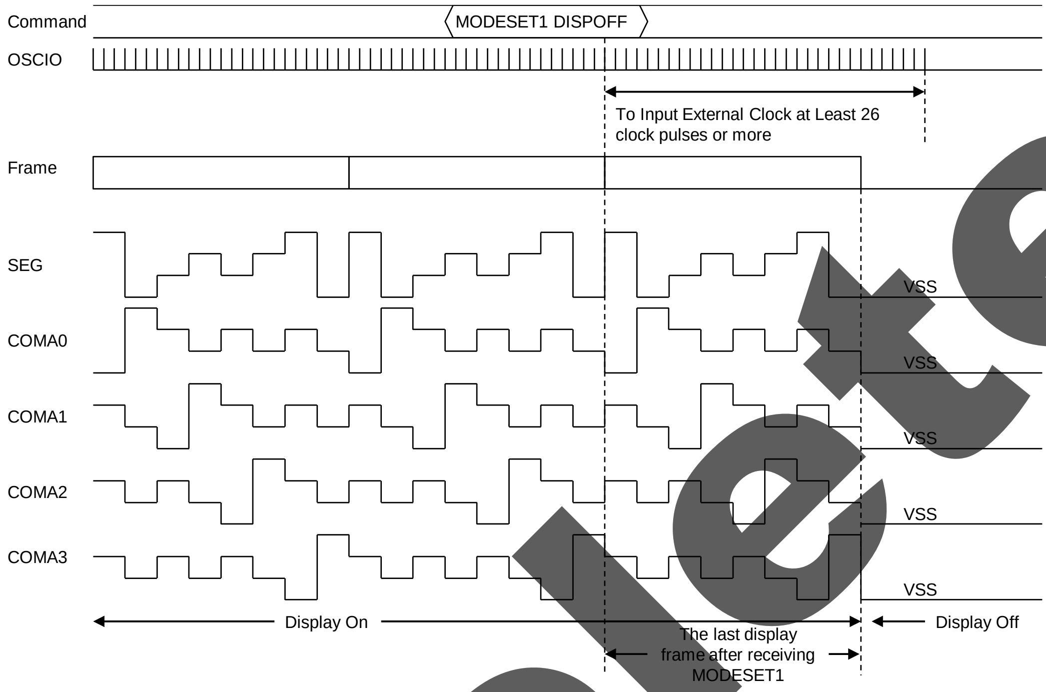


Figure 48. External Clock Stop Timing

In case of External Clock Mode, a clock signal shall be always supplied to BU91R66CH-M. Removing the clock may freeze the LCD in a DC state which is not suitable for the LCD.

In Multi-chip Structure in Internal Clock Mode

In multi-chip structure and in internal clock mode, clock signal for Slave 1 to Slave 3 display are provided by Master IC. So if Master IC receives Display Off before Slave ICs, the clock from Master IC will stop and Slave ICs hold the SEG and COM level not VSS level, then causes abnormal display. To prevent this issue, DISPOFF must be sent to Slave ICs earlier than to Master IC.

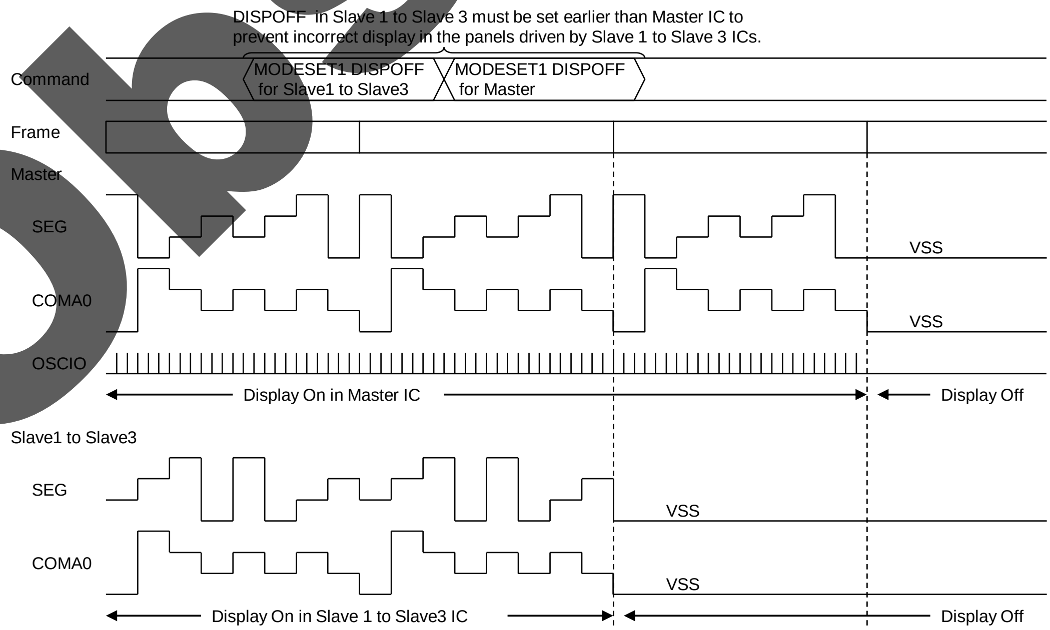


Figure 49. DISPOFF Sequence in Multi-chip Structure

Note on The Multiple Device Connection to 2-wire Serial Interface.

Do not access the other device without power supply (VDD) to the BU91R66CH-M.

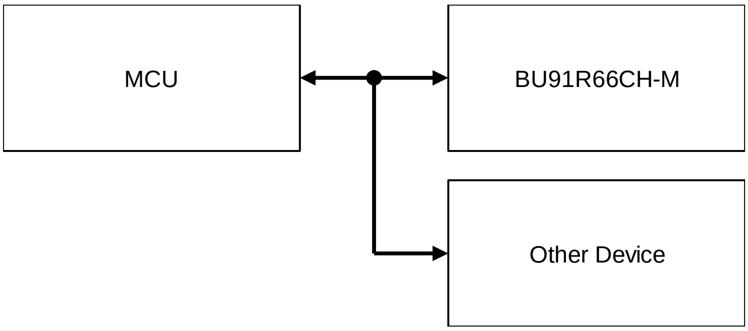


Figure 50. Example of BUS Connection

To control the slope of the falling edge, a capacitor is connected between gate and drain of a NMOS transistor as shown in the following figure. The gate is in a high-impedance state when the power supply (VDD) is not supplied.

In this condition, the gate voltage is pulled up by the current flow through the capacitance as a result of the SDAO signal's transition from low to high.

The NMOS transistor turns on and draws some current (Ids) from the SDAO if the gate voltage (Vg) is higher than the threshold voltage (Vth).

An external resistor (R) is connected between the power line and SDAO line to keep the SDA line as logic high. But the line cannot be kept as logic high if the voltage drop (R*Ids) is large.

Apply power supply (VDD) to BU91R66CH-M when the multiple devices are on the same bus.

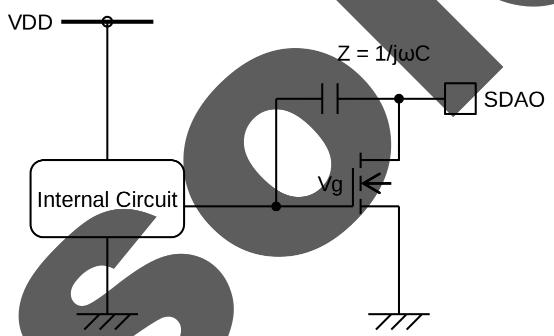


Figure 51. SDA Output Cell Structure

Note in Case that the SDA is stuck at LOW

Normally, BU91R66CH-M SDA status is controlled by MCU, so it set SDA to VSS level only in ACK timing and in output "0" case during Read Mode. If the data line (SDAO) is stuck at LOW by BU91R66CH-M unexpectedly, MCU should send one dummy byte with START and STOP Conditions as shown in **Figure 52. Recovery Sequence from SDA Stuck**. BU91R66CH-M will release SDAO stuck within this sequence.

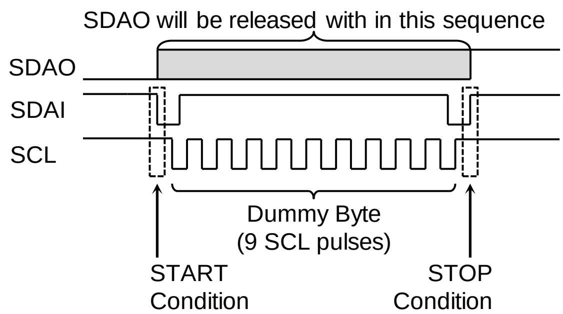


Figure 52. Recovery Sequence from SDA Stuck

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. **Ceramic Capacitor**
When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Operational Notes – continued

12. **Disturbance Light**
In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.
.

Ordering Information

B	U	9	1	R	6	6	C	H	-	M	3	B	W

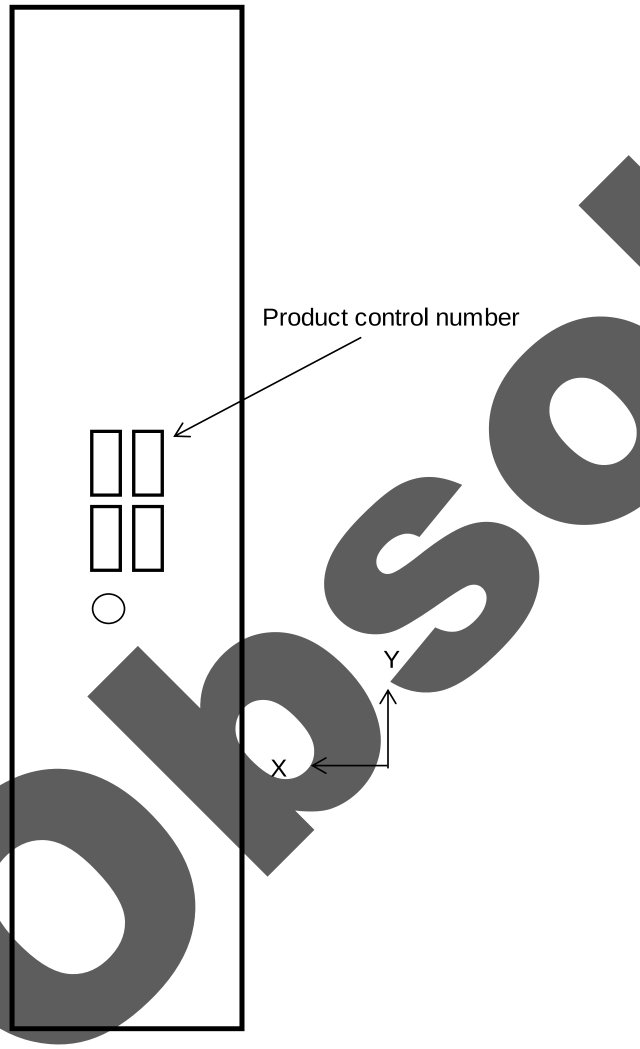
Part Number: BU91R66CH

Product Rank
M: for Automotive

Minimum Order Quantity (MOQ)

Orderable Part Number	Minimum Order Quantity
BU91R66CH-M3BW	3,600 pcs

Marking Diagram



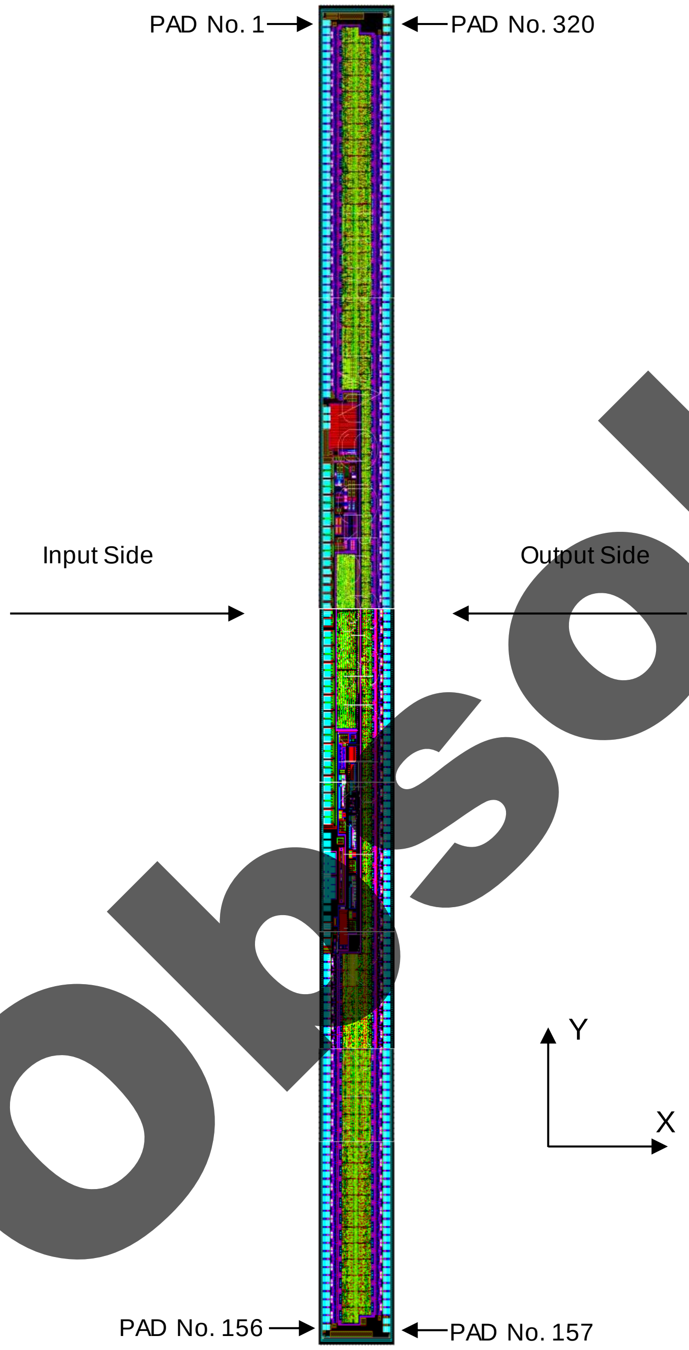
(Bump side down)

Refer to **PAD Arrangement** for the definition of X/Y coordinates.

Packing Quantity

Packing QTY. (Standard QTY)	Tray:	60	pcs / tray
	Block:	300	pcs / block (1 block = 5 trays)
	Vacuum Pack:	1,800	pcs / vacuum pack (1 vacuum pack = 6 blocks)
	Inner Box:	3,600	pcs / inner box (1 inner box = 2 vacuum packs)
	Outer Box:	7,200	pcs / outer box (1 outer box = 2 inner boxes)

Pellet Drawing

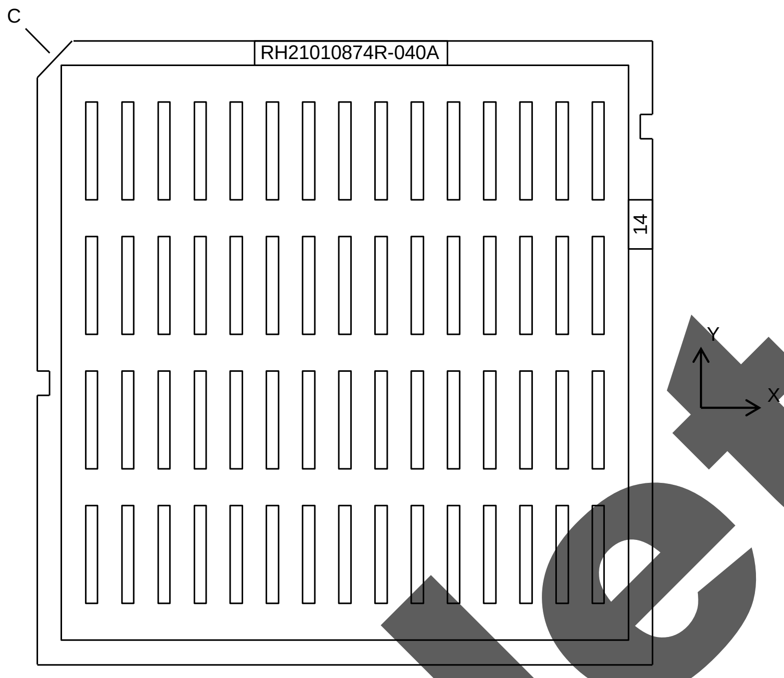


(Bump side up)

Refer to **PAD Arrangement** for the definition of X/Y coordinates.

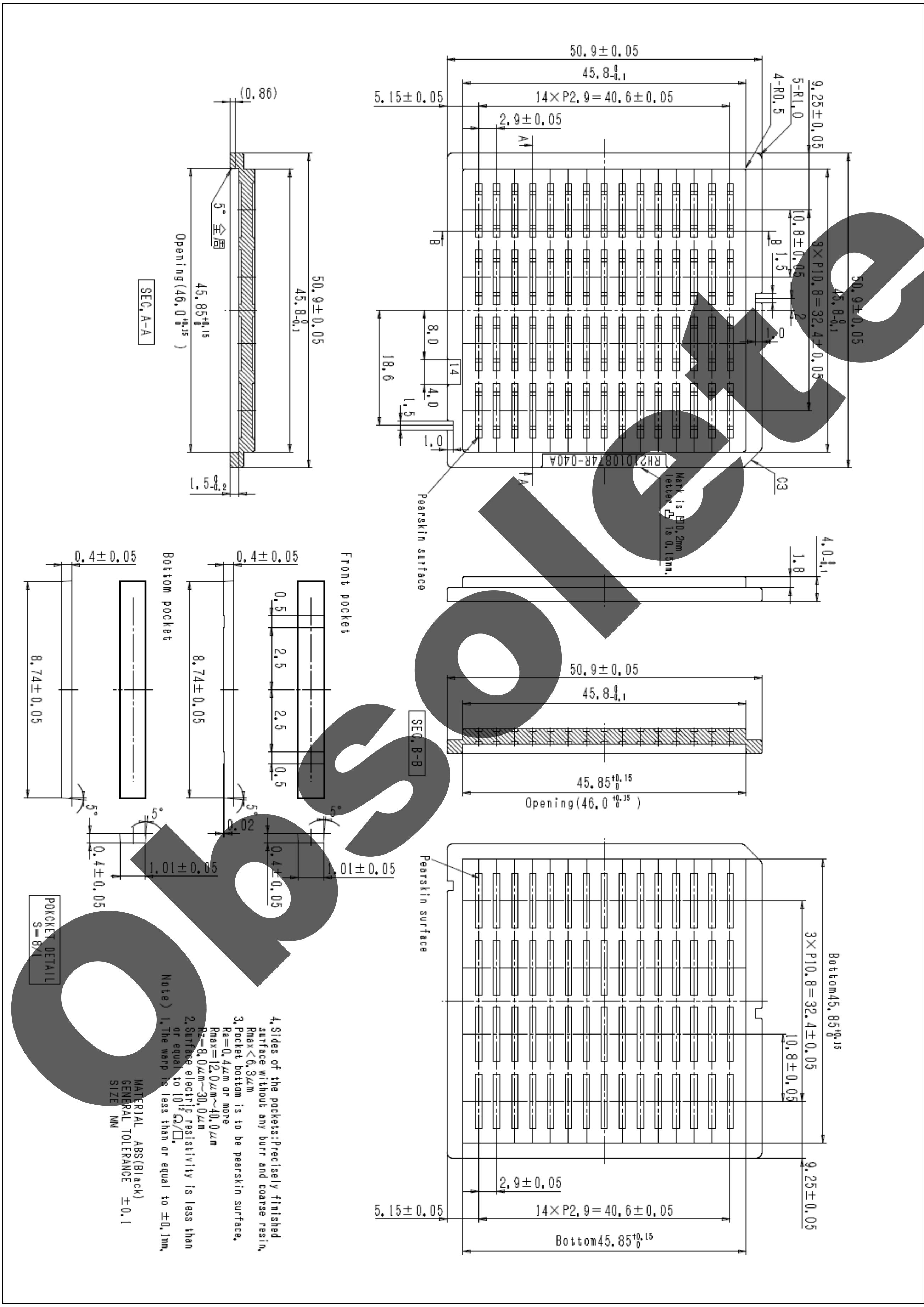
Package Condition

Products should be aligned to the same direction with bump side up.
"Chamfering" side is aligned with X/Y direction of the chip as shown in the following drawing.



Refer to **PAD Arrangement** for the definition of X/Y coordinates.

Tray Physical Dimension



Revision History

Date	Revision	Changes
04.Mar.2019	001	The first release
27.Sep. 2019	002	Updating Minimum Order Quantity and Packing Quantity Minor modifications by formality check

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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