Datasheet

Low Duty LCD Segment Driver For Automotive COG Application

BU91R63CH-M Max 176 segments (SEG44 x COM4)

General Description

BU91R63CH-M is a 1/4, 1/3, 1/2 duty or Static COG type LCD driver that can be used for automotive applications and can drive up to 176 LCD segments.
It can support operating temperature of up to +105 °C and compliant for AEC-Q100, as required for Automotive Application. It has integrated display RAM for reducing CPU load. Also, it is designed with low power consumption and no external component needed. It includes read function for display RAM and command register, which make it possible to detect malfunction due to noise. Also a defective mounting of COG can easily be controlled by using pins to measure ITO resistance.

Features

- AEC-Q100 Compliant *(Note 1)*
- 1/4, 1/3, 1/2 Duty or Static Setting Selectable
  - 1/4 Duty Drive: Max 176 Segments
  - 1/3 Duty Drive: Max 132 Segments
  - 1/2 Duty Drive: Max 88 Segments
  - Static Drive: Max 44 Segments
- Integrated Buffer AMP for LCD Driving
- Support Read Register and Display RAM Function
- Support ITO Resistance Measurement
- Integrated Oscillator Circuit
- Integrated EVR Function to Adjust LCD Contrast
- Integrated Power On Reset Circuit
- No External Components
- Low Power Consumption Design

(Note 1) Quality Information:
There is data when LSI was put on a temporary package.
Please use it as reference data.

Key Specifications

- Supply Voltage Range: +2.7 V to +6.0 V
- LCD Drive Power Supply Range: +2.7 V to +6.0 V
- Operating Temperature Range: -40 °C to +105 °C
- Max Segments: 176 Segments
- Display Duty: 1/4, 1/3, 1/2, Static Selectable
- Bias: 1/2, 1/3 Selectable
- Interface: 2-wire Serial Interface

Special Characteristics

- ESD(HBM): ±2,000 V
- Latch-up Current: ±100 mA

Applications

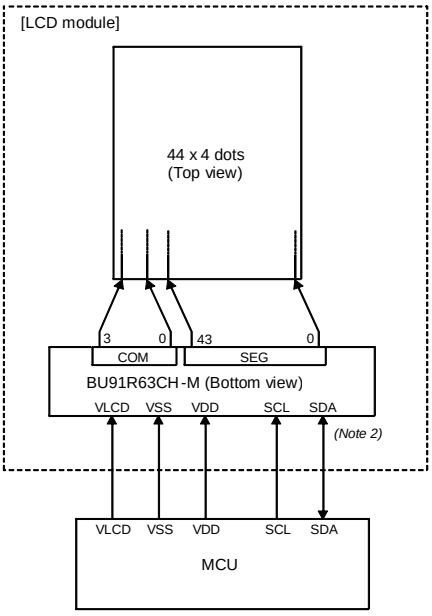
- Instrument Clusters
- Climate Controls
- Car Audios / Radios
- Metering
- White Goods
- Healthcare Products
- Battery Operated Applications

etc.

Package

Au BUMP Chip

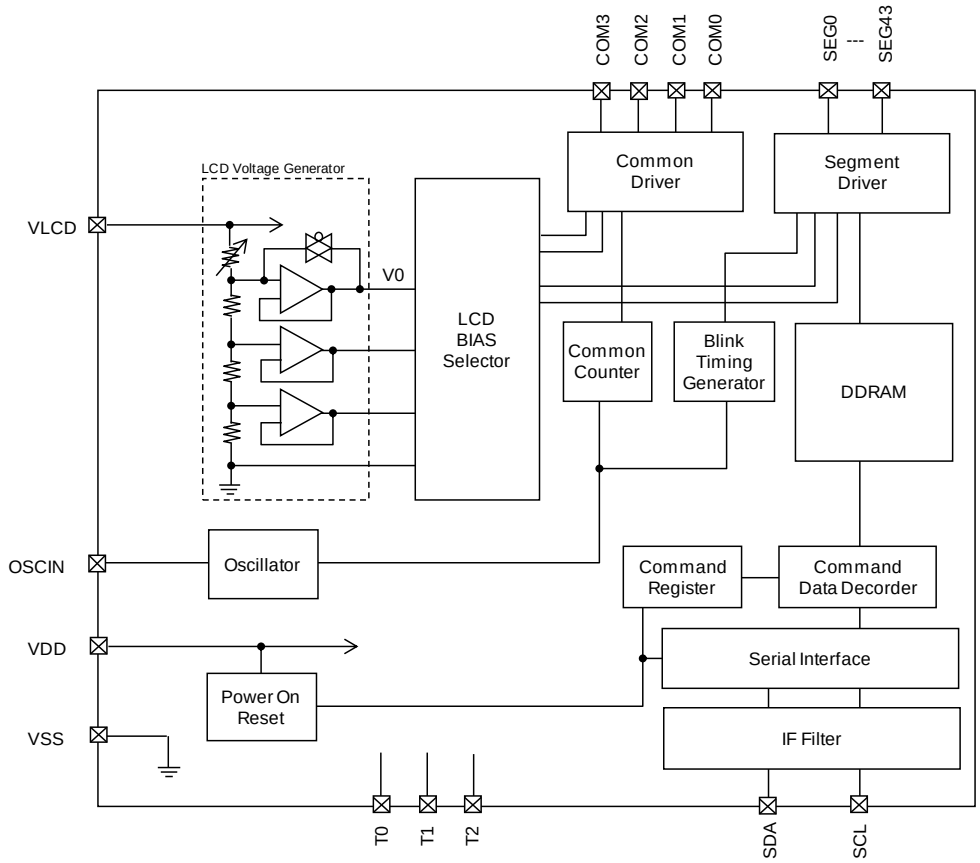
Typical Application Circuit



(Note 2) SDA of BU91R63CH-M needs pull-up resistor because it is an open-drain output.
In case that SCL of MCU has open-drain structure, it also needs pull-up resistor.

○Product structure: Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Block Diagram

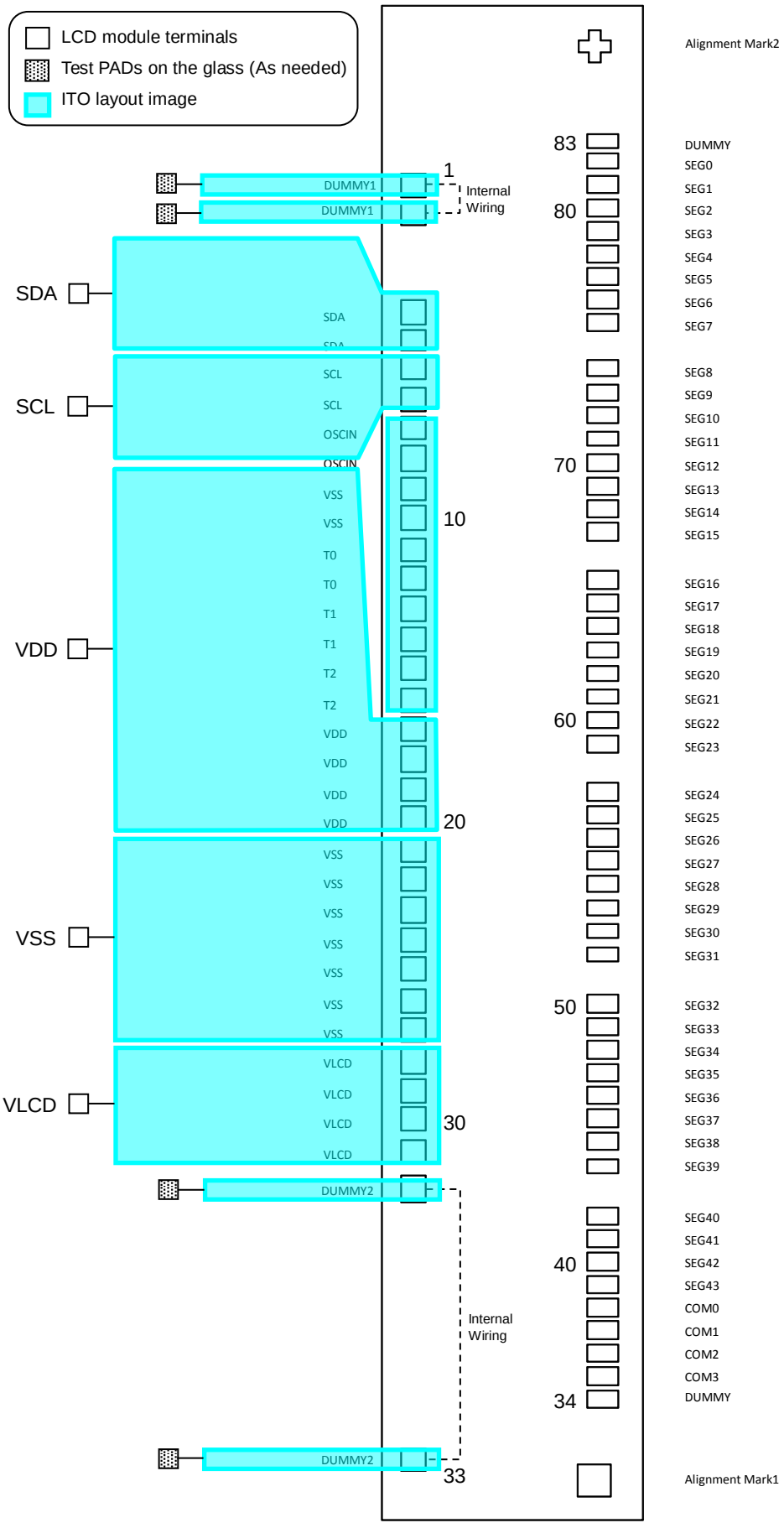


Terminal Description

Terminal Name	I/O	Function	Handling when unused
T0	I	POR enable setting VDD: POR disable *(Note)* VSS: POR enable	VSS
T1	I	Test input (ROHM use only) Must be connected to VSS.	VSS
T2	I	Test input (ROHM use only) Must be connected to VSS.	VSS
DUMMY	-	Open	OPEN
DUMMY1 DUMMY2	-	Can be used for COG resistance measurement.	OPEN
OSCIN	I	External clock input External clock and Internal clock can be selected by command Must be connected to VSS when using internal oscillator	VSS
SDA	I/O	Serial data input-output terminal	-
SCL	I	Serial clock terminal	-
VSS	I	Ground	-
VDD	I	Power supply for logic	-
VLCD	I	Power supply for LCD driving circuit	-
SEG0 to SEG43	O	SEGMENT output for LCD driving	OPEN
COM0 to COM3	O	COMMON output for LCD driving	OPEN

(Note) Not 100 % tested. Software Reset is necessary to initialize IC in case of T0 = VDD.

Recommended ITO Layout

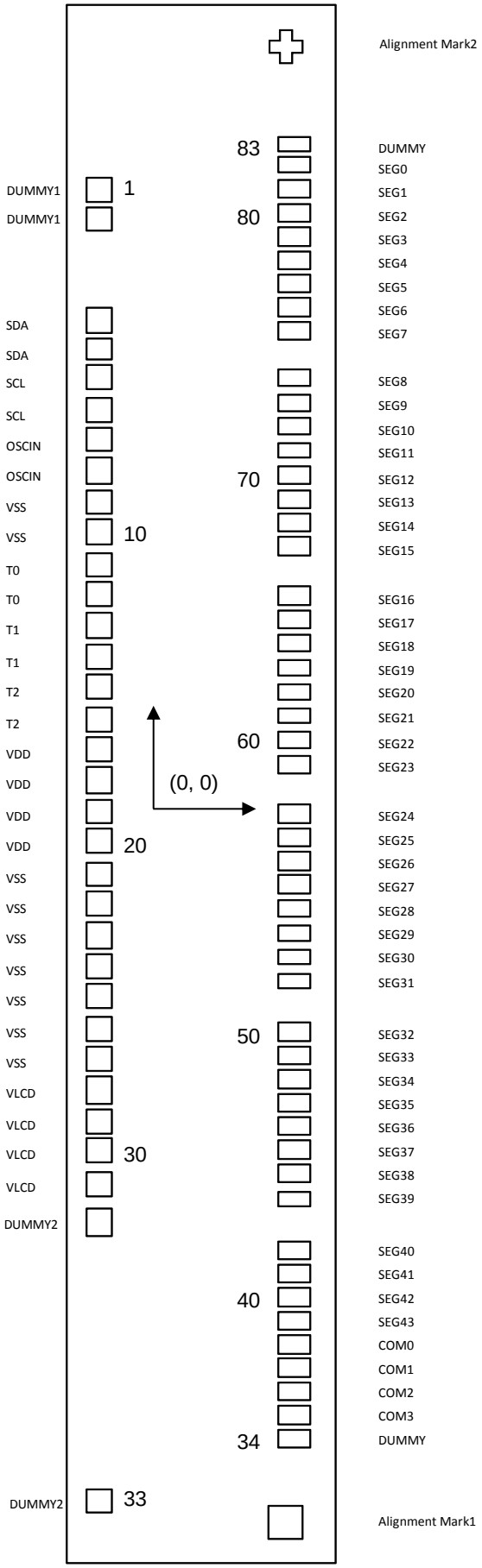


Recommended ITO Layout – continued

Terminal Resistance

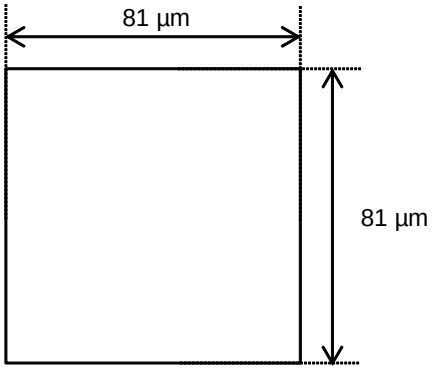
PAD No.	Terminal Name	Maximum Resistance
3, 4	SDA	1,500 Ω
5, 6	SCL	1,500 Ω
7, 8	OSCIN	1,500 Ω
11, 12	T0	1,500 Ω
13, 14	T1	1,500 Ω
15, 16	T2	1,500 Ω
17 to 20	VDD	400 Ω
9, 10, 21 to 27	VSS	400 Ω
28 to 31	VLCD	400 Ω

PAD Arrangement



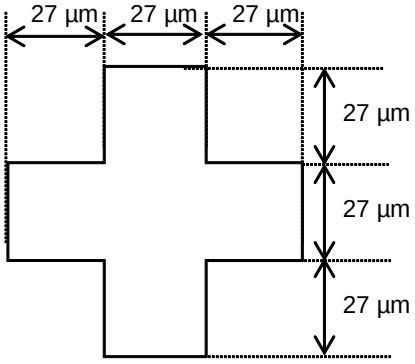
Item	Size		Unit
	X	Y	
Chip size	650	3560	µm
Chip thickness	230		µm
Bump height	15 ± 3		µm
Bump hardness	50 ± 20		Hv

Alignment Mark 1



Mark center coordinate
(X, Y) = (206.6, -1685.0)

Alignment Mark 2



Mark center coordinate
(X, Y) = (206.6, 1685.0)

Dimension

Table 1. Dimension (Completion Size)

Mark		Topic	Specification Limit
Chip Size X		Chip Size: X Direction	625 ± 40 μm
Chip Size Y		Chip Size: Y Direction	3,535 ± 40 μm
Chip Thickness		Chip Thickness	230 ± 20 μm
Input PAD	A (PAD1 to PAD33)	Bump Size: X Direction	60.0 ± 3.0 μm
	B (PAD1 to PAD33)	Bump Size: Y Direction	55.0 ± 3.0 μm
	C (PAD1 to PAD33)	Average of Bump Height	15.0 ± 3.0 μm
Output PAD	A' (PAD34 to PAD83)	Bump Size: X Direction	75.0 ± 3.0 μm
	B' (PAD34 to PAD83)	Bump Size: Y Direction	39.0 ± 3.0 μm
	C' (PAD34 to PAD83)	Average of Bump Height	15.0 ± 3.0 μm

Table 2. Bump Specs and Dimensions

Topic	Specification Limit
Bump Structure	Straight Bump
Bump Co-planarity on Chip	3.0 μm or less
Bump Hardness (Microvicker's Meter)	50 Hv ± 20 Hv
Bump Strength	7.25 mg/μm^2 or more

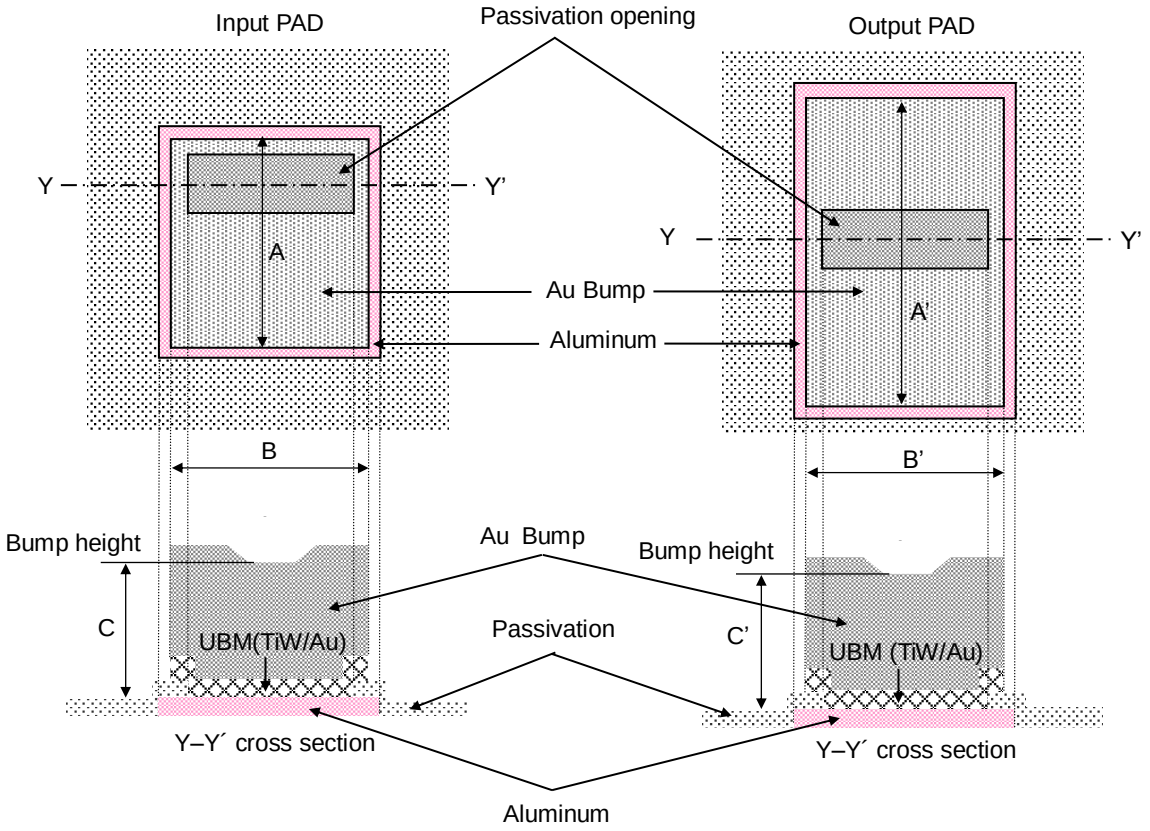


Figure 1. PAD / Bump Information

PAD Coordinates

Unit:µm

No	Terminal Name	BUMP Center		BUMP Size	
		X	Y	X	Y
1	DUMMY1	-248.00	1340.00	60	55
2	DUMMY1	-248.00	1270.00	60	55
3	SDA	-248.00	1045.00	60	55
4	SDA	-248.00	975.00	60	55
5	SCL	-248.00	905.00	60	55
6	SCL	-248.00	835.00	60	55
7	OSCIN	-248.00	765.00	60	55
8	OSCIN	-248.00	695.00	60	55
9	VSS	-248.00	625.00	60	55
10	VSS	-248.00	555.00	60	55
11	T0	-248.00	485.00	60	55
12	T0	-248.00	415.00	60	55
13	T1	-248.00	345.00	60	55
14	T1	-248.00	275.00	60	55
15	T2	-248.00	205.00	60	55
16	T2	-248.00	135.00	60	55
17	VDD	-248.00	65.00	60	55
18	VDD	-248.00	-5.00	60	55
19	VDD	-248.00	-75.00	60	55
20	VDD	-248.00	-145.00	60	55
21	VSS	-248.00	-215.00	60	55
22	VSS	-248.00	-285.00	60	55
23	VSS	-248.00	-355.00	60	55
24	VSS	-248.00	-425.00	60	55
25	VSS	-248.00	-495.00	60	55
26	VSS	-248.00	-565.00	60	55
27	VSS	-248.00	-635.00	60	55
28	VLCD	-248.00	-705.00	60	55
29	VLCD	-248.00	-775.00	60	55
30	VLCD	-248.00	-845.00	60	55
31	VLCD	-248.00	-915.00	60	55
32	DUMMY2	-248.00	-1005.00	60	55
33	DUMMY2	-248.00	-1636.00	60	55
34	DUMMY	227.00	-1496.55	75	39
35	COM3	227.00	-1442.55	75	39
36	COM2	227.00	-1388.55	75	39
37	COM1	227.00	-1334.55	75	39
38	COM0	227.00	-1280.55	75	39
39	SEG43	227.00	-1226.55	75	39
40	SEG42	227.00	-1172.55	75	39
41	SEG41	227.00	-1118.55	75	39
42	SEG40	227.00	-1064.55	75	39
43	SEG39	227.00	-950.90	75	39
44	SEG38	227.00	-896.90	75	39
45	SEG37	227.00	-842.90	75	39
46	SEG36	227.00	-788.90	75	39
47	SEG35	227.00	-734.90	75	39
48	SEG34	227.00	-680.90	75	39
49	SEG33	227.00	-626.90	75	39
50	SEG32	227.00	-572.90	75	39
51	SEG31	227.00	-458.85	75	39
52	SEG30	227.00	-404.85	75	39
53	SEG29	227.00	-350.85	75	39
54	SEG28	227.00	-296.85	75	39
55	SEG27	227.00	-242.85	75	39
56	SEG26	227.00	-188.85	75	39
57	SEG25	227.00	-134.85	75	39
58	SEG24	227.00	-80.85	75	39
59	SEG23	227.00	33.20	75	39
60	SEG22	227.00	87.20	75	39
61	SEG21	227.00	141.20	75	39
62	SEG20	227.00	195.20	75	39
63	SEG19	227.00	249.20	75	39
64	SEG18	227.00	303.20	75	39
65	SEG17	227.00	357.20	75	39
66	SEG16	227.00	411.20	75	39
67	SEG15	227.00	525.25	75	39
68	SEG14	227.00	579.25	75	39
69	SEG13	227.00	633.25	75	39
70	SEG12	227.00	687.25	75	39
71	SEG11	227.00	741.25	75	39
72	SEG10	227.00	795.25	75	39
73	SEG9	227.00	849.25	75	39
74	SEG8	227.00	903.25	75	39
75	SEG7	227.00	1017.30	75	39
76	SEG6	227.00	1071.30	75	39
77	SEG5	227.00	1125.30	75	39
78	SEG4	227.00	1179.30	75	39
79	SEG3	227.00	1233.30	75	39
80	SEG2	227.00	1287.30	75	39
81	SEG1	227.00	1341.30	75	39
82	SEG0	227.00	1395.30	75	39
83	DUMMY	227.00	1449.30	75	39

Refer to PAD Arrangement for the definition of X/Y coordinates.

Absolute Maximum Ratings (VSS = 0 V)

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Maximum Voltage1	VDD	-0.5	-	+7.0	V	Power Supply
Maximum Voltage2	VLCD	-0.5	-	+7.0	V	LCD Drive Voltage
Input Voltage Range	V_{IN}	-0.5	-	+7.0	V	-
Human Body Model (HBM)*(Note 1), (Note 2)*	V_{ESD}	-	±2,000	-	V	-
Latch-up Current*(Note 1), (Note 3)*	I_{LU}	-	±100	-	mA	-
Maximum Junction Temperature	Tjmax	-55	-	+125	°C	-
Storage Temperature Range	Tstg	-55	-	+125	°C	-

(Note 1) Please use as reference data.
(Note 2) Testing standards: JESD22-A114E
(Note 3) Testing standards: JESD78
Caution: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Recommend Operating Conditions (VSS = 0 V)

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Operational Temperature	Topr	-40	-	+105	°C	-
Power Supply Voltage 1	VDD	2.7	-	6.0	V	Power Supply
Power Supply Voltage 2	VLCD	2.7	-	6.0	V	LCD Drive Voltage

Electrical Characteristics

DC Characteristics (Unless otherwise specified, Ta = -40 °C to +105 °C, VDD = 2.7 V to 6.0 V, VSS = 0 V)

Parameter		Symbol	Limits			Unit	Condition
			Min	Typ	Max		
“H” Level Input Voltage		V_{IH}	0.7VDD	-	VDD	V	SDA, SCL, OSCIN
“L” Level Input Voltage		V_{IL}	VSS	-	0.3VDD	V	SDA, SCL, OSCIN
“H” Level Input Current		I_{IH}	-	-	1	µA	SDA, SCL, OSCIN, T0, T1, T2
“L” Level Input Current		I_{IL}	-1	-	-	µA	SDA, SCL, OSCIN, T0, T1, T2
SDA “L” Level Output Voltage		V_{OLSDA}	0	-	0.4	V	I_{LOAD} = -3 mA
LCD Driver On Resistance	SEG	R_{ON}	-	3	-	kΩ	I_{LOAD} = ±10 µA
	COM	R_{ON}	-	3	-	kΩ	
Standby Current		I_{VDD1}	-	-	5.0	µA	Display Off, Oscillation Off
		I_{VLCD1}	-	-	5.0	µA	
Operating Current		I_{VDD2}	-	2.0	10.0	µA	VDD = 3.3 V, VLCD = 3.3 V, Ta = 25 °C, Power save mode1, 1/3 bias, Frame inversion Frame Frequency = 80 Hz setting
		I_{VLCD2}	-	5.5	20.0	µA	

Electrical Characteristics – continued

Oscillation Characteristics (Unless otherwise specified,Ta = -40 °C to +105 °C, VDD = 2.7 V to 6.0 V, VSS = 0 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Frame Frequency 1	f_{CLK1}	56	80	104	Hz	DISCTL 80 Hz setting, VDD = 2.7 V to 6.0 V, Ta = -40 °C to +105 °C
Frame Frequency 2	f_{CLK2}	72	80	88	Hz	DISCTL 80 Hz setting, VDD = 3.5 V, Ta = -40 °C to +105 °C
External Clock Rise Time	tr_{CLK}	-	-	0.3	µs	External Clock Mode
External Clock Fall Time	tf_{CLK}	-	-	0.3	µs	
External Clock Frequency	f_{CLK3}	30,000	-	300,000	Hz	
External Clock Duty	T_{DTY}	30	50	70	%	

Keep external clock frequency range from 30,000 Hz to 300,000 Hz.
The calculation formula for frame frequency at external clock mode is shown in Set IC Operation (ICSET).

[Reference Data]

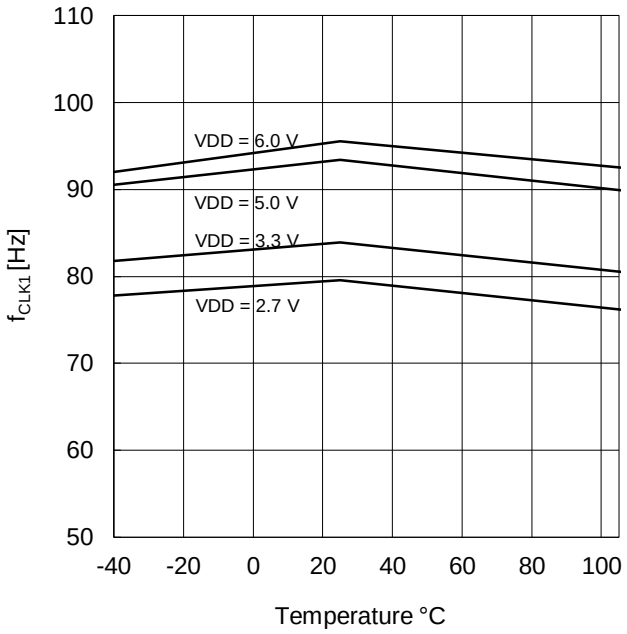


Figure 2. Frame Frequency Typical Temperature Characteristics

Electrical Characteristics - continued

MPU Interface Characteristics (Unless otherwise specified, Ta = -40 °C to +105 °C, VDD = 2.7 V to 6.0 V, VSS = 0 V)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Input Rise Time	tr	-	-	0.3	µs	
Input Fall Time	tf	-	-	0.3	µs	
SCL Cycle Time	t_{CYC}	2.5	-	-	µs	
“H” Level SCL Pulse Width	t_{HW}	0.6	-	-	µs	
“L” Level SCL Pulse Width	t_{LW}	1.3	-	-	µs	
SDA Setup Time	t_{SDS}	100	-	-	ns	
SDA Hold Time	t_{SDH}	100	-	-	ns	
Bus Free Time	t_{BUF}	1.3	-	-	µs	
START Condition Hold Time	$t_{HD;STA}$	0.6	-	-	µs	
START Condition Setup Time	$t_{SU;STA}$	0.6	-	-	µs	
STOP Condition Setup Time	$t_{SU;STO}$	0.6	-	-	µs	

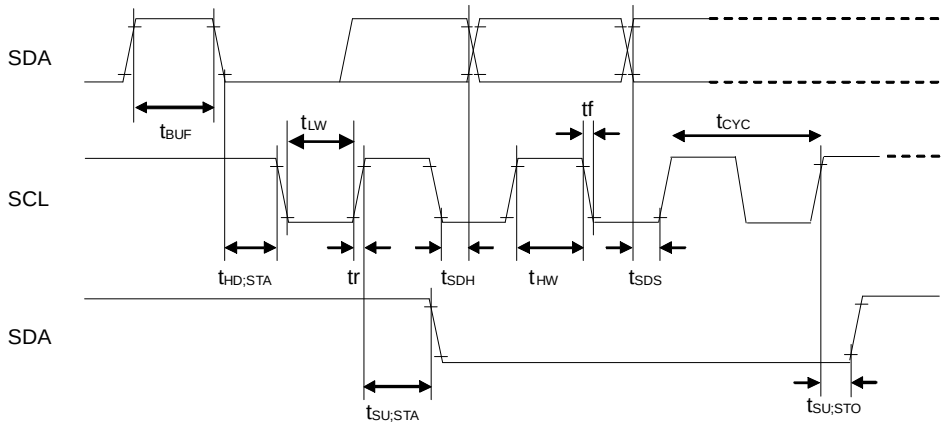
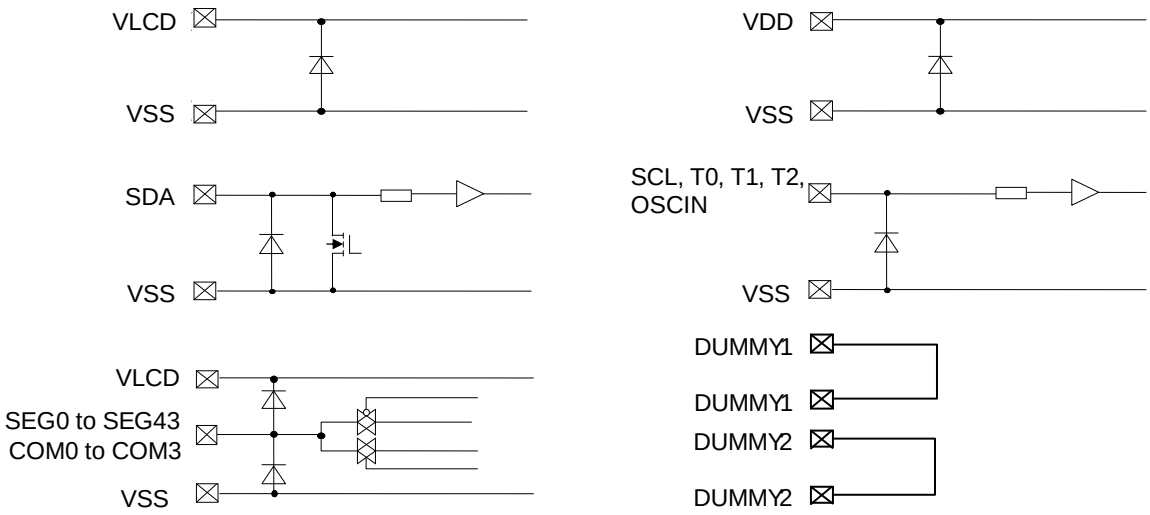


Figure 3. Interface Timing

I/O Equivalence Circuit



Functional Descriptions

Command / Data Transfer Method

BU91R63CH-M transfers command or data by 2-wire signal (SDA, SCL).

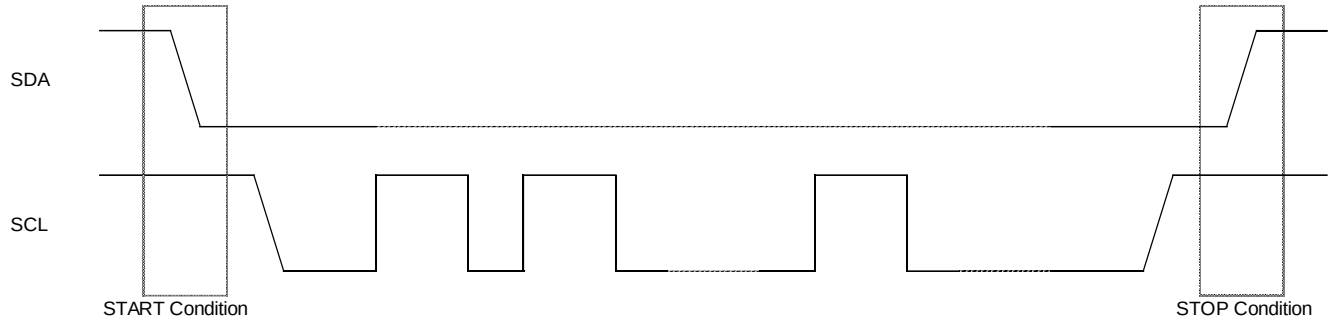


Figure 4. 2-wire Command/Data Transfer Format

It is necessary to generate START and STOP Condition when transferring command or display data through the 2-wire serial interface.

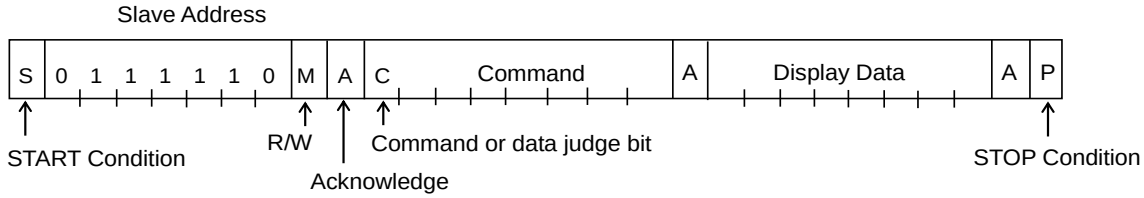


Figure 5. Interface Protcol

The following procedure shows how to transfer Command and Display Data.

(1) Generate “START Condition”.
(2) Issue Slave Address.
(3) Transfer Command and Display Data.
(4) Generate “STOP Condition”

Acknowledge (ACK)

Data format is comprised of 8 bits, Acknowledge bit is returned after sending 8-bit data.
After the transfer of 8-bit data (Slave Address, Command, Display Data), release the SDA line at the 8th falling edge of SCL. The SDA keeps “Low” output until the 9th falling edge of the SCL.
(Output cannot be pulled “High” because of open drain NMOS).
If acknowledge function is not required, keep SDA line at “Low” level from 8th falling edge to 9th falling edge of SCL.

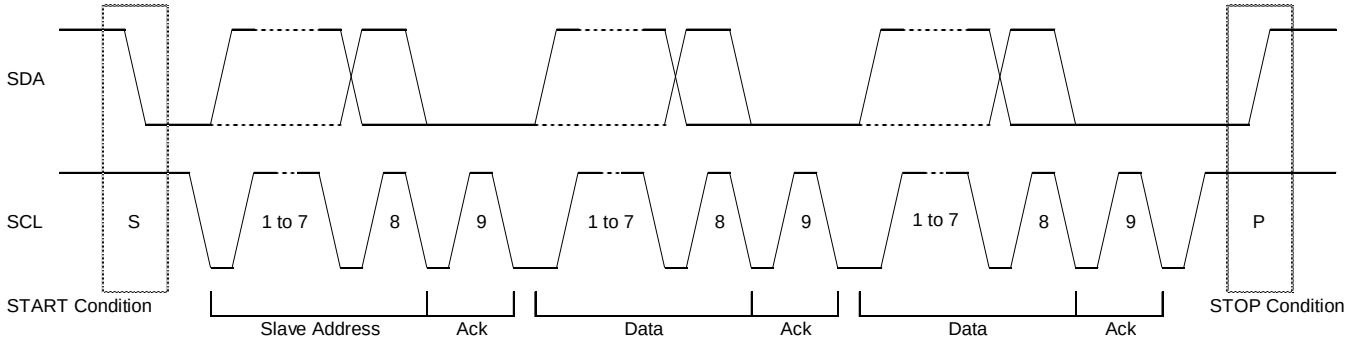
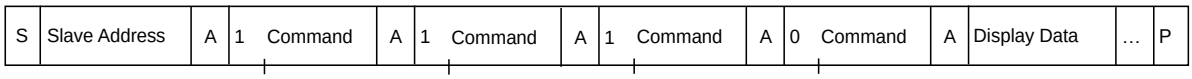


Figure 6. Acknowledge Timing

Functional Descriptions – continued

Command Transfer Method

Issue Slave Address (“01111100”) after generating “START Condition”.
After issuing Slave address (“01111100”), the first byte is always command input.
MSB (Most Significant Bit) of command is the judgment bit for Command or Display Data.
When set “command or data judge bit” = “1”, commands can be input continuously.
When set “command or data judge bit” = “0”, next byte data is Display Data.

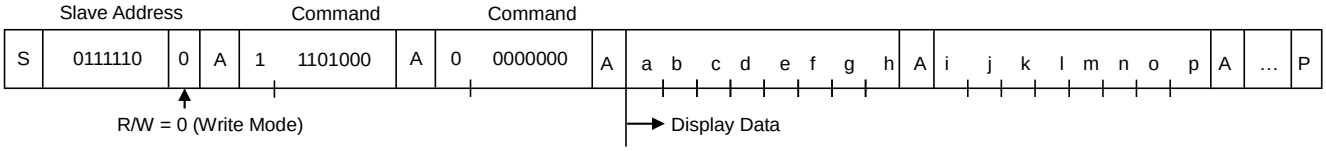


Command cannot be accepted in once input state of display data.
In order to input command again it is necessary to generate “START Condition”.
If “START Condition” or “STOP Condition” is generated during command transfer, the command being transferred is cancelled.
If Slave Address is issued continuously following “START Condition” during the transfer, it remains in command input state.
After generating “START Condition”, issue Slave Address at the first data transfer.
If Slave Address cannot be recognized in the first data transfer, Acknowledge bit is not returned and subsequent data transfer is not accepted. When data is in invalid status, it is restored by generating “START Condition” again.

Consider the MPU interface characteristics such as Input rise time and Setup/Hold time when transferring command and data (Refer to MPU Interface Characteristics).

Write Display Data and Transfer Method

For Write Mode set R/W bit to “0”.
BU91R63CH-M has Display Data RAM (DDRAM) of 44 x 4 = 176bit.
The relationship between data input and display data, DDRAM data and address are as follows.



8-bit data is stored in DDRAM. ADSET command specifies the address to be written, and address is automatically incremented in every 4-bit data.
Data can be continuously written in DDRAM by transmitting data continuously.
When DDRAM data is written successively, after writing DDRAM data to 2Bh (SEG43), the address is returned to 00h (SEG0) by the auto-increment function.

DDRAM address

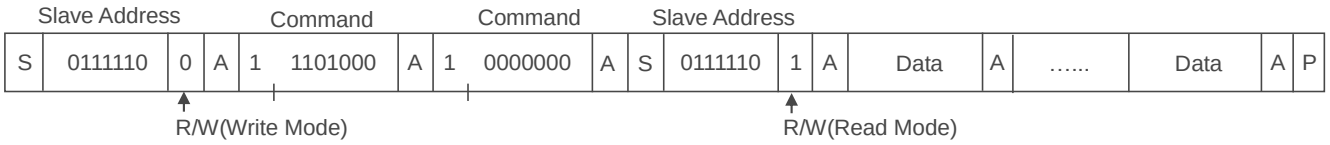
BIT	00h	01h	02h	03h	04h	05h	06h	07h	…	29h	2Ah	2Bh	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7		SEG 41	SEG 42	SEG 43	

Display data is written to DDRAM every 4-bit data.
No need to wait for ACK bit to complete data transfer.

Functional Descriptions – continued

Read Display and Transfer Method

For Read Mode set R/W bit to “1”.
The display data and command register value can be read during Read Mode.
The Read Mode sequence is shown below.



In Read Mode, the display data and the register data can be read from the DDRAM through the SDA line.
Output data is output in synchronization with the SCL signal.
In order to access the DDRAM, it is necessary to set the address at first using the ADSET command in Write Mode.
Note that if the address is not set before reading the display data, reading will start from the current address.
The address is automatically incremented by +2 for each 8-bit output data.
Master side should output ACK signal every 8bit data output.
BU91R63CH-M continues address increment and output data by receiving ACK. If ACK is not received, BU91R63CH-M does not continue the above read operation so that input “STOP Condition”.
When receiving “STOP Condition”, BU91R63CH-M ends Read Mode.
The address automatically returns to 00h after 2Bh. (Not incremented to 2Ch or 2Dh.)

An example of the display data read sequence is shown below.

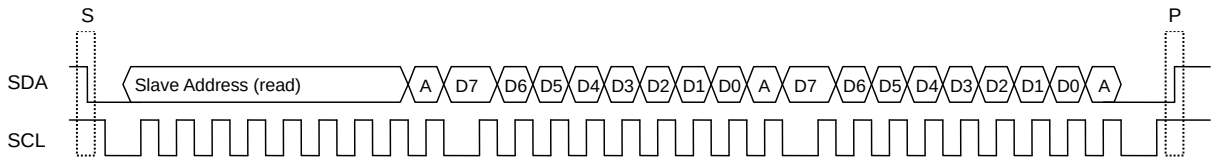
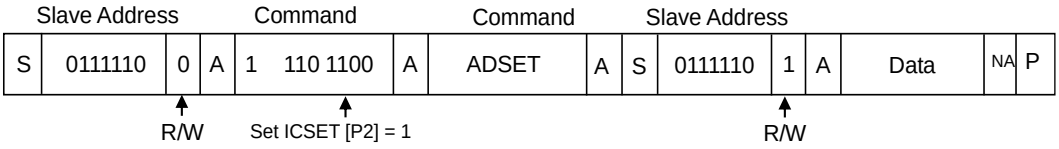


Figure 7. Read Sequence

Functional Descriptions – continued

Read Command Register and Transfer Method

The command registers can be read during Read Mode. The sequence for the command register read is shown below and is similar to the display data read sequence.



Regarding address setting, refer to Address Set (ADSET) command.
The following register settings can be read in this mode by setting address to 2Ch, 2Dh, and 2Eh.
Address does not increment automatically after read the command register value.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	P7	P6	P5	P4	P3	P2	P1	P0	2Ch
REG2	P7	P6	P5	P4	P3	P2	P1	P0	2Dh
REG3	0	0	0	0	P3	P2	P1	P0	2Eh

REG1: P7 = Duty setting
P6 = Duty setting
P5 = 1/2Bias / 1/3Bias setting
P4 = Internal clock / External clock setting
P3 = Software Reset setting
P2 to P0 = Blink setting

REG2: P7 to P6 = Frame Frequency setting
P5 to P4 = Power Save Mode setting
P3 = Frame/Line inversion setting
P2 = Display On/Off setting
P1 = All Pixels ON setting
P0 = All Pixels OFF setting

REG3: P3 = Contrast setting
P2 = Contrast setting
P1 = Contrast setting
P0 = Contrast setting

The ADSET and ICSET setting address map is shown below.

Write Mode	ADSET				ICSET							
RAM Address	D7	D6	D5	D[4:0]	*P7*	*P6*	*P5*	*P4*	*P3*	*P2*(Note)	*P1*	*P0*
0000 0000 to 0001 1111	0	0	0	*0 0000 to 1 1111*	*1*	*1*	*1*	*0*	*1*	*0*	*0*	*0*
0010 0000 to 0010 1011	0	0	0	*0 0000 to 0 1011*	*1*	*1*	*1*	*0*	*1*	*1*	*0*	*0*
Read Mode	ADSET				ICSET							
RAM Address	D7	D6	D5	D[4:0]	*P7*	*P6*	*P5*	*P4*	*P3*	*P2*(Note)	*P1*	*P0*
0000 0000 to 0001 1111	1	0	0	*0 0000 to 1 1111*	*1*	*1*	*1*	*0*	*1*	*0*	*0*	*0*
0010 0000 to 0010 1110	1	0	0	*0 0000 to 0 1110*	*1*	*1*	*1*	*0*	*1*	*1*	*0*	*0*

(Note) Please take care of ICSET [P2] setting.

OSC (Oscillator)

The clock required for internal operation and liquid crystal display operation is generated by an internal oscillation circuit or an external clock. If internal oscillator circuit is used, OSCIN must be connected to VSS level.
When using external clock mode, input external clock from OSCIN terminal after ICSET command setting.

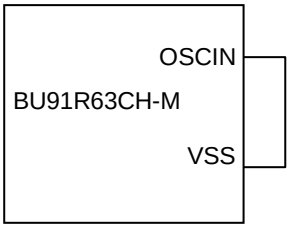


Figure 8. Internal Clock Mode

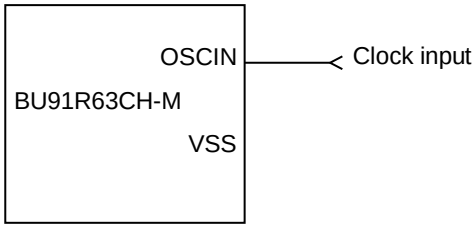


Figure 9. External Clock Mode

LCD Driver Bias Circuit

This circuit generates the liquid crystal drive voltage. It also has a built-in buffer amplifier that can be driven with low power consumption.
1/3 or 1/2 Bias can be set by MODESET command.
Line or frame inversion can be set by DISCTL command.
Refer to the LCD Driving Waveform for each LCD bias setting.

Blinker Timing Generator

BU91R63CH-M has Blink function.
Blink mode can be set by BLKCTL command.
The Blink frequency varies depending on f_{CLK} characteristics at internal clock mode.
Refer to Oscillation Characteristics for f_{CLK}.

Reset Initialize Condition

Initial condition after executing Software Reset is as follows.
- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).

Refer to Detailed Command Description for initial value of registers.

Command / Function List

Description List of Command / Function

No.	Command	Function
1	Set IC Operation (ICSET)	Software reset, internal/external clock setting (P2 is MSB data of DDRAM address)
2	Display Control (DISCTL)	Frame Frequency, Power Save Mode setting
3	Address Set (ADSET)	DDRAM address setting Register address setting
4	Mode Set (MODESET)	Display ON/OFF, Bias, Duty
5	Blink Control (BLKCTL)	Blink off/0.5 Hz/1 Hz/2 Hz/0.3 Hz/0.2 Hz Blink setting
6	All Pixels Control (APCTL)	All Pixels ON/OFF during DISPON
7	Contrast Setting (EVRSET)	Contrast Setting

Detailed Command Description

D7 (MSB) is a command or data judgment bit.
Refer to Command / Data Transfer Method.

C = 0: Next byte is RAM write data.
C = 1: Next byte is command.

Set IC Operation (ICSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2: MSB data of DDRAM address. Please refer to Address Set (ADSET) command.

Set software reset execution.

Setup	P1
No operation	0
Software Reset Execute	1

When “Software Reset” is executed, BU91R63CH-M is reset to initial condition.
(Refer to Reset Initialize Condition)
Don’t set Software Reset (P1) with P2, P0 at the same time.

Set oscillator mode.

Setup	P0	Reset initialize condition
Internal Clock（internal oscillation circuit used)	0	○
External Clock	1	-

Internal Clock Mode: OSCIN must be connected to VSS level.
External Clock Mode: Input external clock from OSCIN terminal.

<Frame frequency Calculation at external clock mode>
DISCTL 80 Hz setting: Frame frequency = external clock / 512 [Hz]
DISCTL 130 Hz setting: Frame frequency = external clock / 315 [Hz]
DISCTL 64 Hz setting: Frame frequency = external clock / 648 [Hz]
DISCTL 200 Hz setting: Frame frequency = external clock / 205 [Hz]

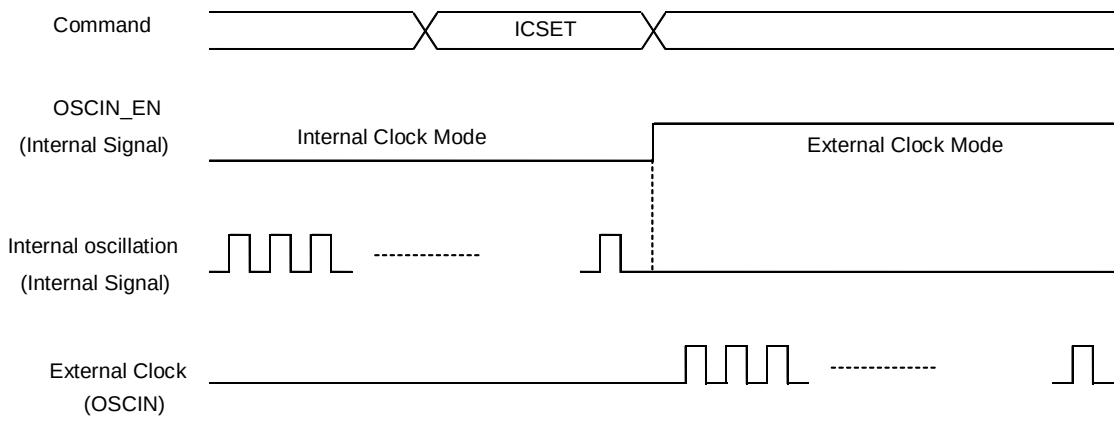


Figure 14. OSC MODE Switch Timing

Detailed Command Description – continued

Display Control (DISCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Frame Frequency.

Setup	P4	P3	Reset initialize condition
80 Hz	0	0	○
130 Hz	0	1	-
64 Hz	1	0	-
200 Hz	1	1	-

Set LCD Drive Waveform.

Setup	P2	Reset initialize condition
Line Inversion Mode	0	○
Frame Inversion Mode	1	-

Power consumption is reduced in the following order:
Line inversion > Frame inversion
Typically, when driving large capacitance LCD, Line inversion is more susceptible to crosstalk.
Regarding driving waveform, refer to LCD Driving Waveform.

Set Power Save Mode

Setup	P1	P0	Reset initialize condition
Power Save Mode 1	0	0	-
Power Save Mode 2	0	1	-
Normal Mode	1	0	○
High Power Mode	1	1	-

Power consumption is increased in the following order:
Power Save Mode 1 < Power Save Mode 2 < Normal Mode < High Power Mode

Address Set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

The range of address in the Write Mode can be set from 000000 to 101011(bin).
The range of address in the Read Mode can be set from 000000 to 101110(bin).

	MSB					LSB
Internal Register	Address [5]	Address [4]	Address [3]	Address [2]	Address [1]	Address [0]
Command	ICSET P2	ADSET P4	ADSET P3	ADSET P2	ADSET P1	ADSET P0

Address [5:0]: MSB bit is specified in ICSET P2 and [4:0] are specified as ADSET P4 - P0.
Don't set out of range address, otherwise address is set to 000000.

Detailed Command Description – continued

Mode Set (MODE SET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	0	P3	P2	P1	P0

Set Display On and Off

Setup	P3	Reset initialize condition
Display Off (DISPOFF)	0	○
Display On (DISPON)	1	-

Display Off: Regardless of DDRAM data, all SEGMENT and COMMON outputs stop after writing OFF data of 1frame. Display Off mode is disabled after Display On command.
Display On: SEGMENT and COMMON outputs become active, and reading operation from DDRAM to Display starts.

Set Bias Level

Setup	P2	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	-

Please refer to LCD Driving Waveform, for example of SEG and COM output waveform

Set Duty

Setup	P1	P0	Reset initialize condition
1/4 Duty	0	0	○
1/3 Duty	0	1	-
1/2 Duty	1	0	-
Static	1	1	-

Blink Control (BLKCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	P2	P1	P0

Set Blink condition.

Blink mode (Hz)	P2	P1	P0	Reset initialize condition
OFF	0	0	0	○
0.5	0	0	1	-
1	0	1	0	-
2	0	1	1	-
0.3	1	0	0	-
0.2	1	0	1	-

The Blink frequency varies depending on f_{CLK} characteristics at internal clock mode.
Refer to Oscillation Characteristics for f_{CLK}.

Detailed Command Description – continued

All Pixels Control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	P2	P1	P0

Set all pixels to be turned on and off simultaneously.

Setup	P1	Reset initialize condition
Normal	0	○
All Pixels ON	1	-

Setup	P0	Reset initialize condition
Normal	0	○
All Pixels OFF	1	-

All Pixels ON: All pixels are ON regardless of DDRAM data simultaneously.
All Pixels OFF: All pixels are OFF regardless of DDRAM data simultaneously.

This command is valid in Display On status. The data of DDRAM is not changed by this command.
If set both P1 and P0 = “1”, All Pixels OFF is selected.

P2 is used for P3 of Contrast Setting.

Detailed Command Description – continued

Contrast Setting (EVRSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	0	P2	P1	P0

BU91R63CH-M has an electronic volume of 16 gradations. This function allows setting the maximum potential (V0) of the gradation voltage for LCD driving. In the initial state after reset, the electronic volume setting is “0000”. At this time, the VLCD voltage becomes the V0 voltage. Set the electronic volume so that the V0 voltage is 2.7 V or higher. Refer to the table below for V0 output voltage.

Contrast Setting (V0 voltage)	P3(*Note*)	P2	P1	P0	Reset initialize condition
1.000 x VLCD	0	0	0	0	○
0.975 x VLCD	0	0	0	1	-
0.950 x VLCD	0	0	1	0	-
0.925 x VLCD	0	0	1	1	-
0.900 x VLCD	0	1	0	0	-
0.875 x VLCD	0	1	0	1	-
0.850 x VLCD	0	1	1	0	-
0.825 x VLCD	0	1	1	1	-
0.800 x VLCD	1	0	0	0	-
0.775 x VLCD	1	0	0	1	-
0.750 x VLCD	1	0	1	0	-
0.725 x VLCD	1	0	1	1	-
0.700 x VLCD	1	1	0	0	-
0.675 x VLCD	1	1	0	1	-
0.650 x VLCD	1	1	1	0	-
0.625 x VLCD	1	1	1	1	-

(*Note*) P3 setting uses P2 of APCTL.

The relationship of LCD display contrast setting and VLCD voltage

Formula	VLCD							Unit
	6.0	5.5	5.0	4.5	4.0	3.0	2.7	
1.000 x VDD	6.000	5.500	5.000	4.500	4.000	3.000	2.700	V
0.975 x VDD	5.850	5.363	4.875	4.388	3.900	2.925	2.632	V
0.950 x VDD	5.700	5.225	4.750	4.275	3.800	2.850	2.565	V
0.925 x VDD	5.550	5.088	4.625	4.163	3.700	2.775	2.497	V
0.900 x VDD	5.400	4.950	4.500	4.050	3.600	2.700	2.430	V
0.875 x VDD	5.250	4.813	4.375	3.938	3.500	2.625	2.362	V
0.850 x VDD	5.100	4.675	4.250	3.825	3.400	2.550	2.295	V
0.825 x VDD	4.950	4.538	4.125	3.713	3.300	2.475	2.227	V
0.800 x VDD	4.800	4.400	4.000	3.600	3.200	2.400	2.160	V
0.775 x VDD	4.650	4.263	3.875	3.488	3.100	2.325	2.092	V
0.750 x VDD	4.500	4.125	3.750	3.375	3.000	2.250	2.025	V
0.725 x VDD	4.350	3.988	3.625	3.263	2.900	2.175	1.957	V
0.700 x VDD	4.200	3.850	3.500	3.150	2.800	2.100	1.890	V
0.675 x VDD	4.050	3.713	3.375	3.038	2.700	2.025	1.822	V
0.650 x VDD	3.900	3.575	3.250	2.925	2.600	1.950	1.755	V
0.625 x VDD	3.750	3.438	3.125	2.813	2.500	1.875	1.687	V

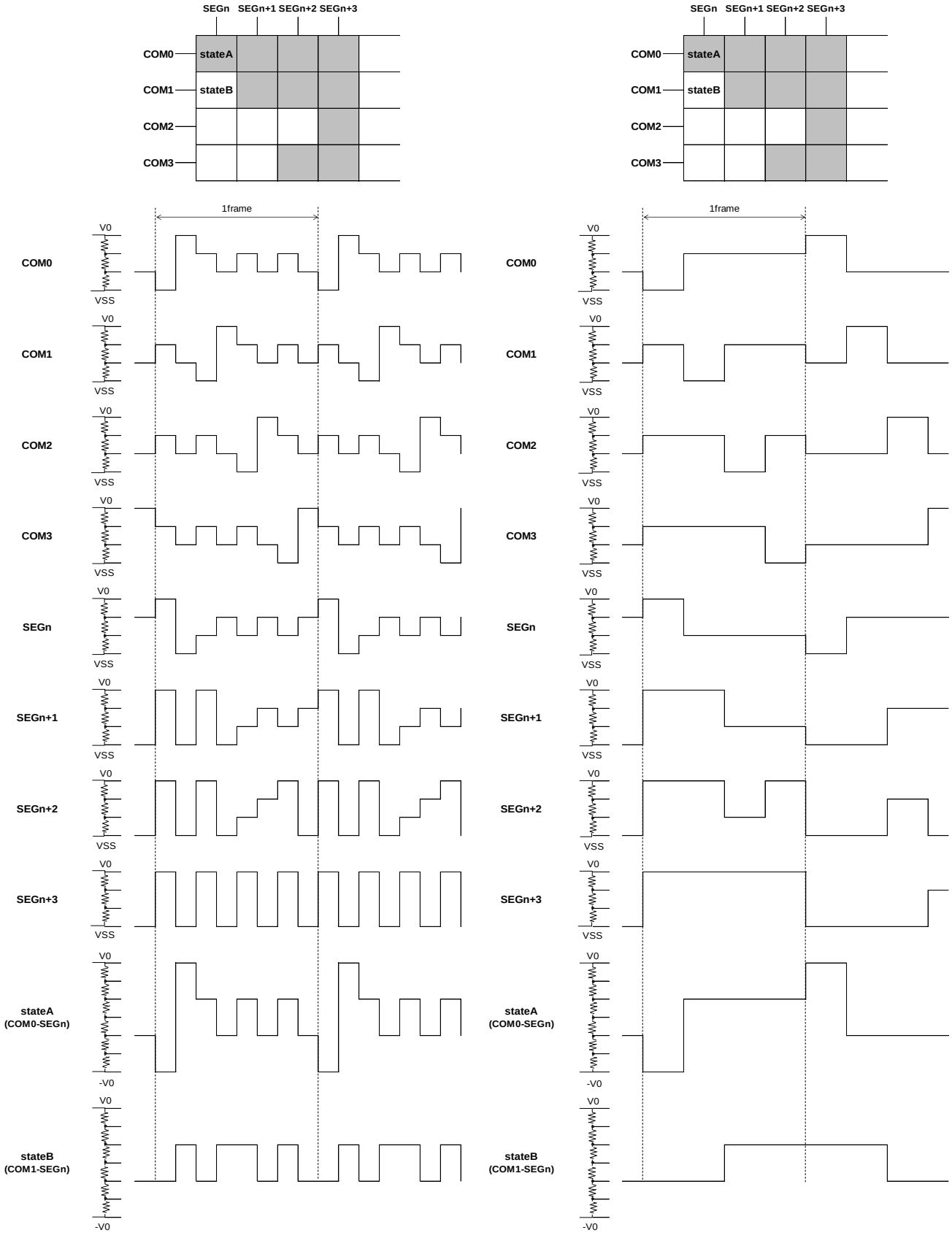
Prohibited Setting

In the case of using EVR function, ensure “VLCD – V0 > 0.6 V” condition is satisfied.
IC output may become unstable if the above conditions are not satisfied.

LCD Driving Waveform

(1/4duty, 1/3bias)

Line Inversion

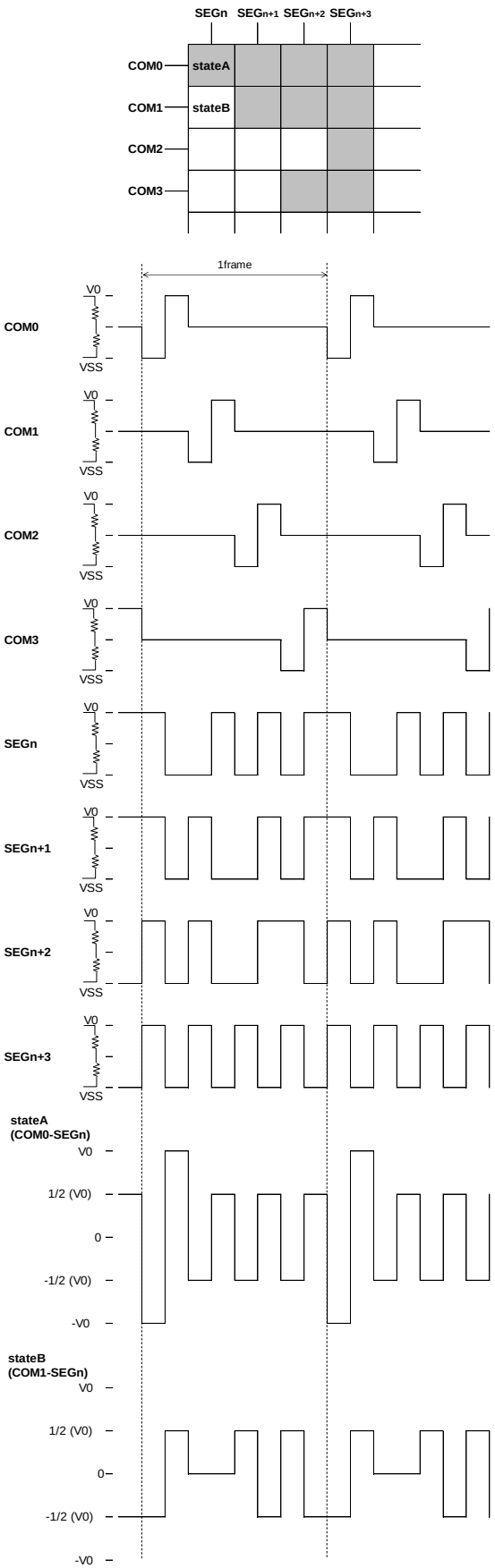


Frame Inversion

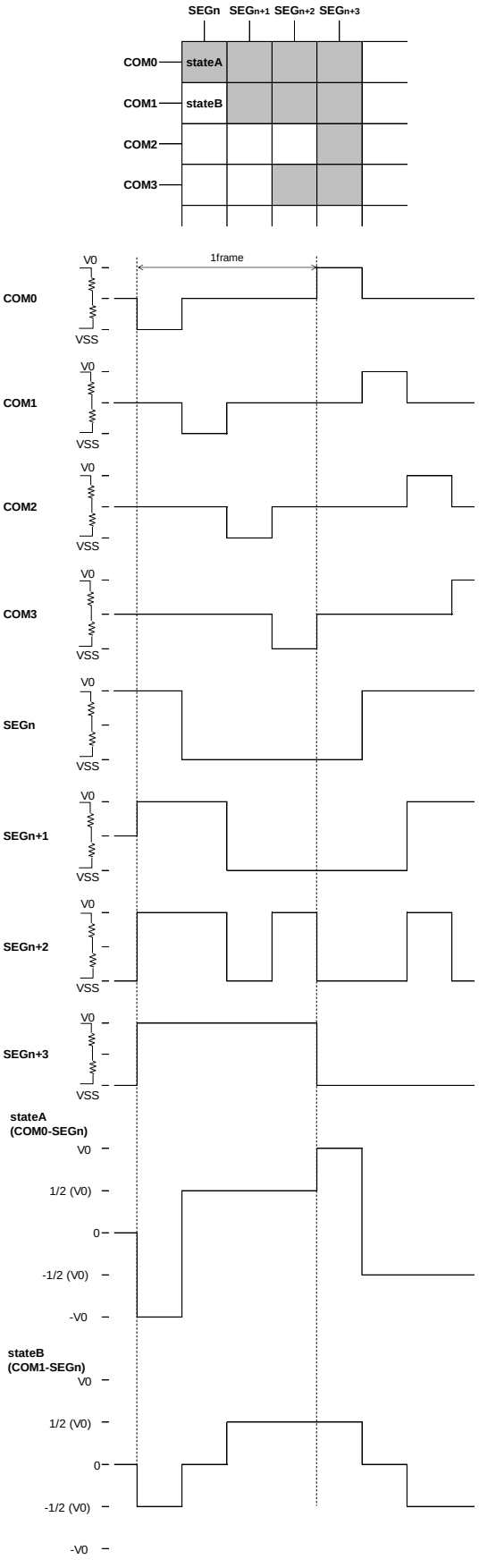
LCD Driving Waveform – continued

(1/4duty, 1/2bias)

Line Inversion



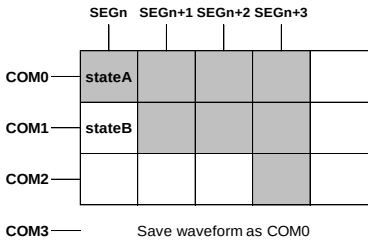
Frame Inversion

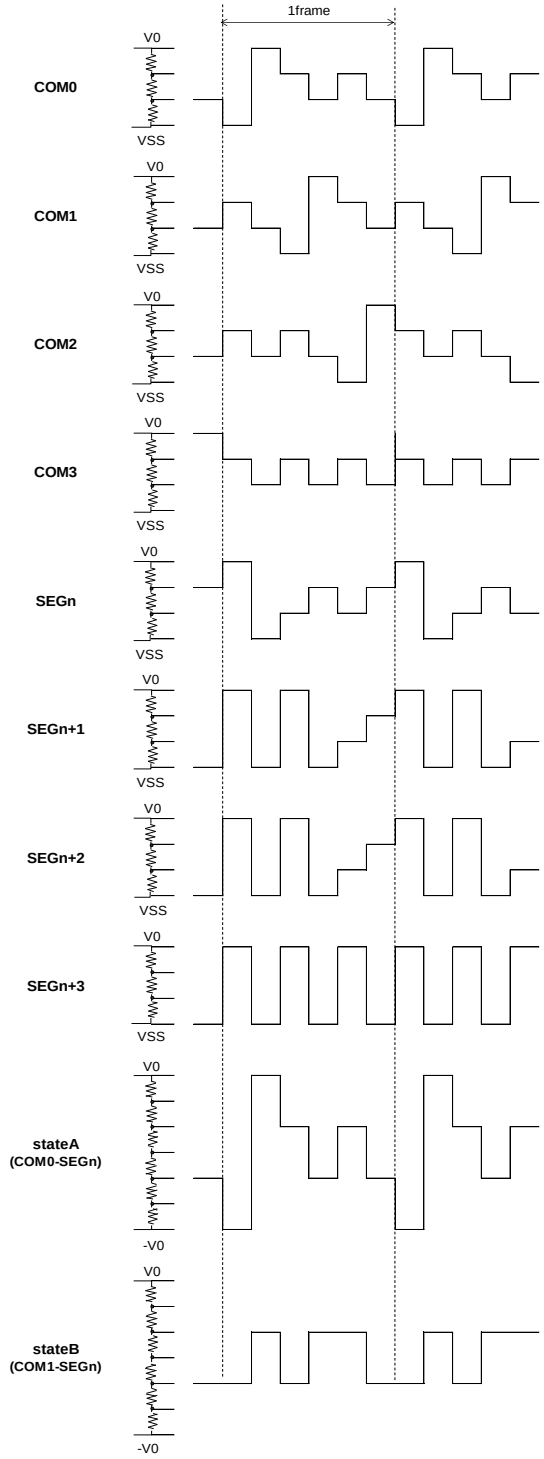


LCD Driving Waveform – continued

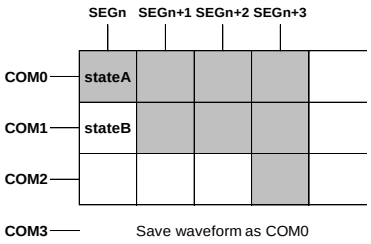
(1/3duty, 1/3bias)

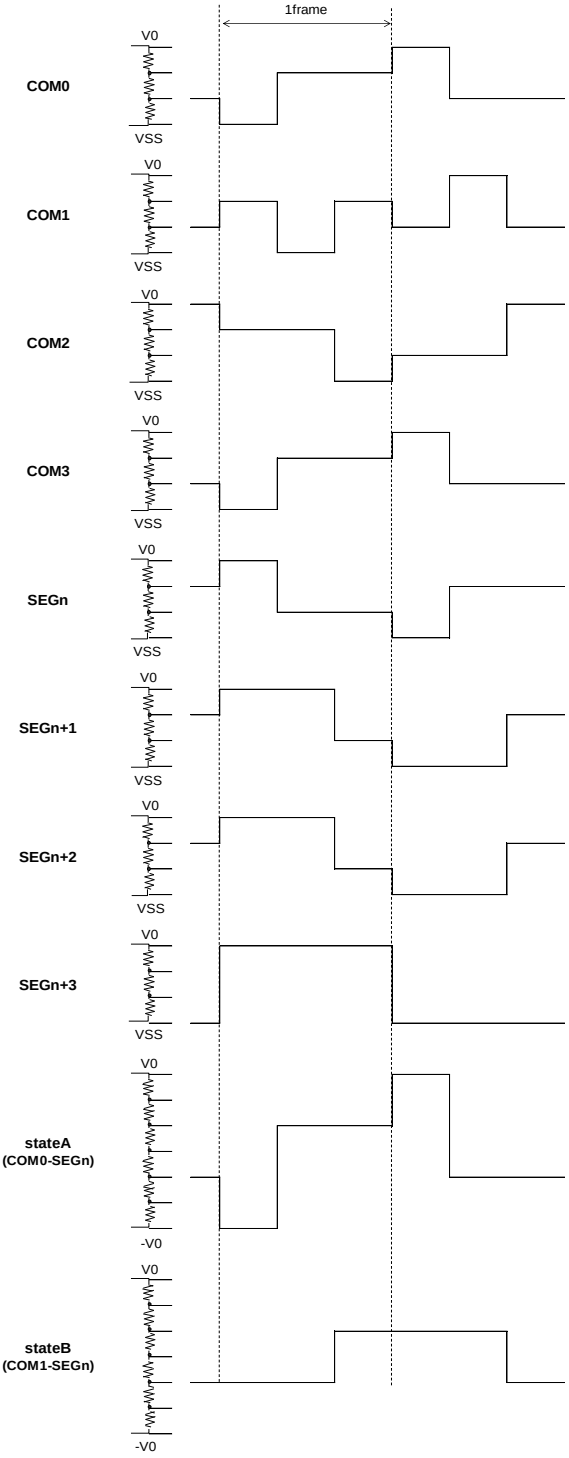
Line Inversion





Frame Inversion

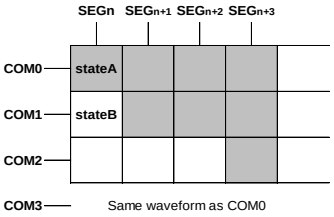


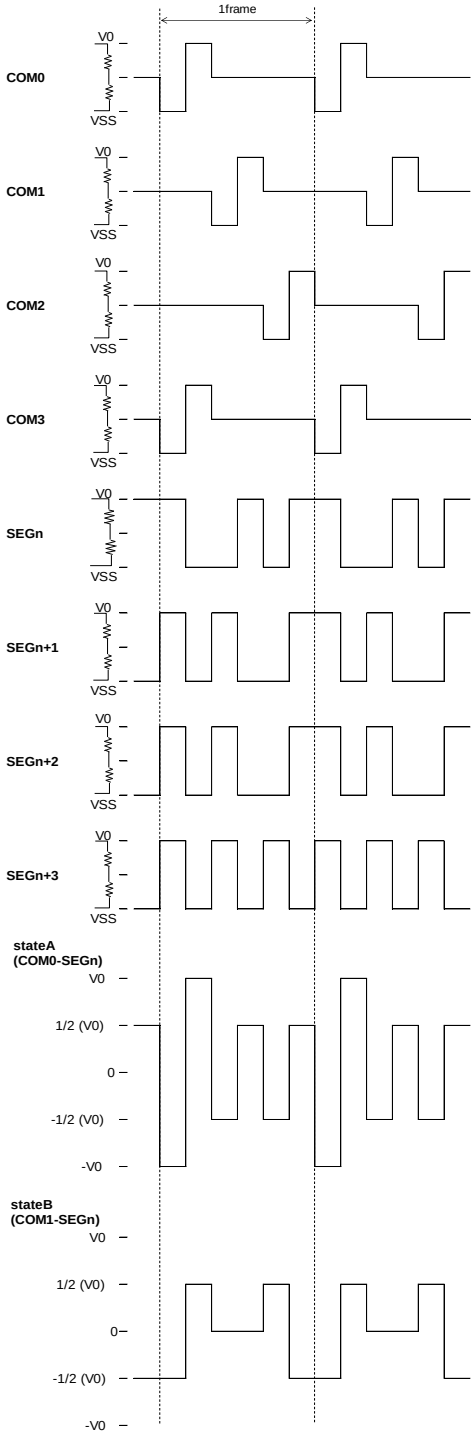


LCD Driving Waveform – continued

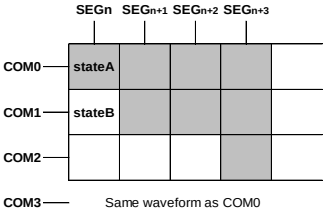
(1/3duty, 1/2bias)

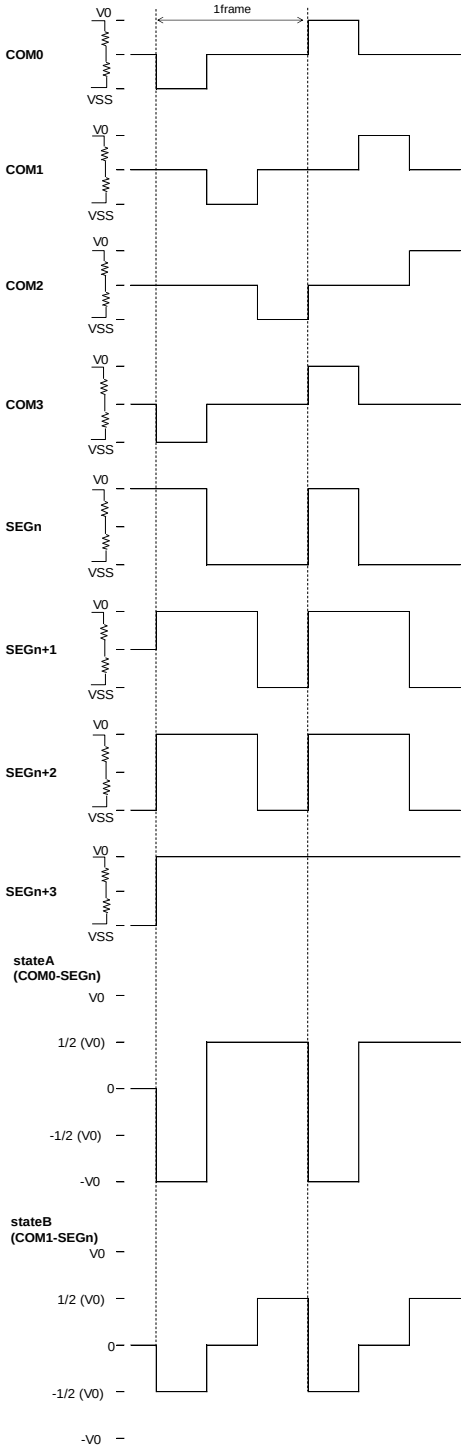
Line Inversion





Frame Inversion

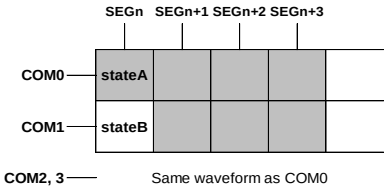




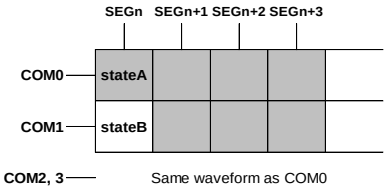
LCD Driving Waveform – continued

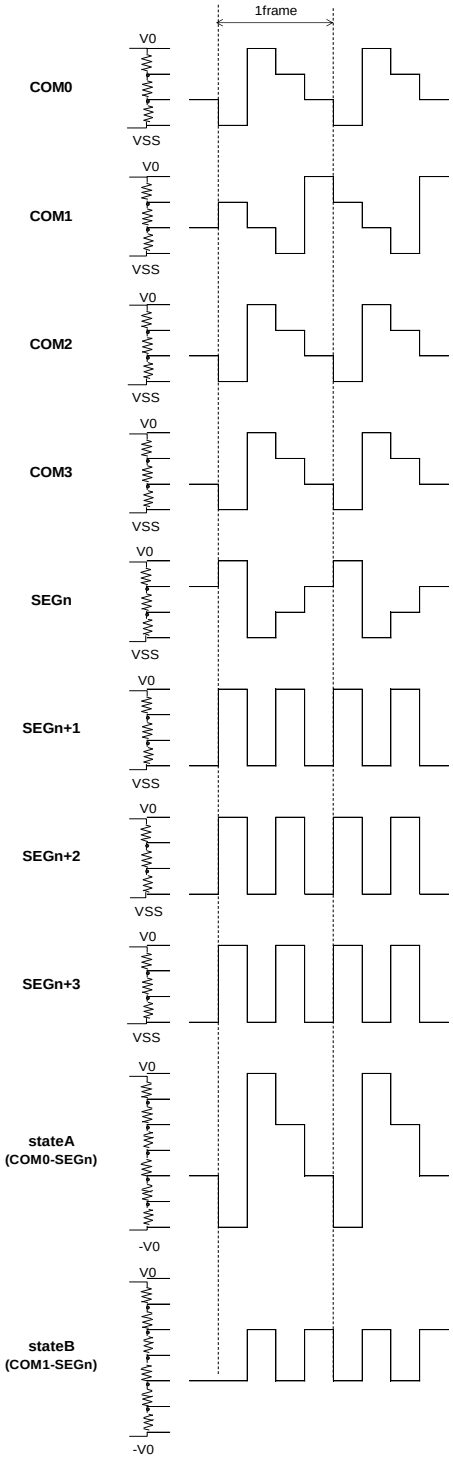
(1/2duty, 1/3bias)

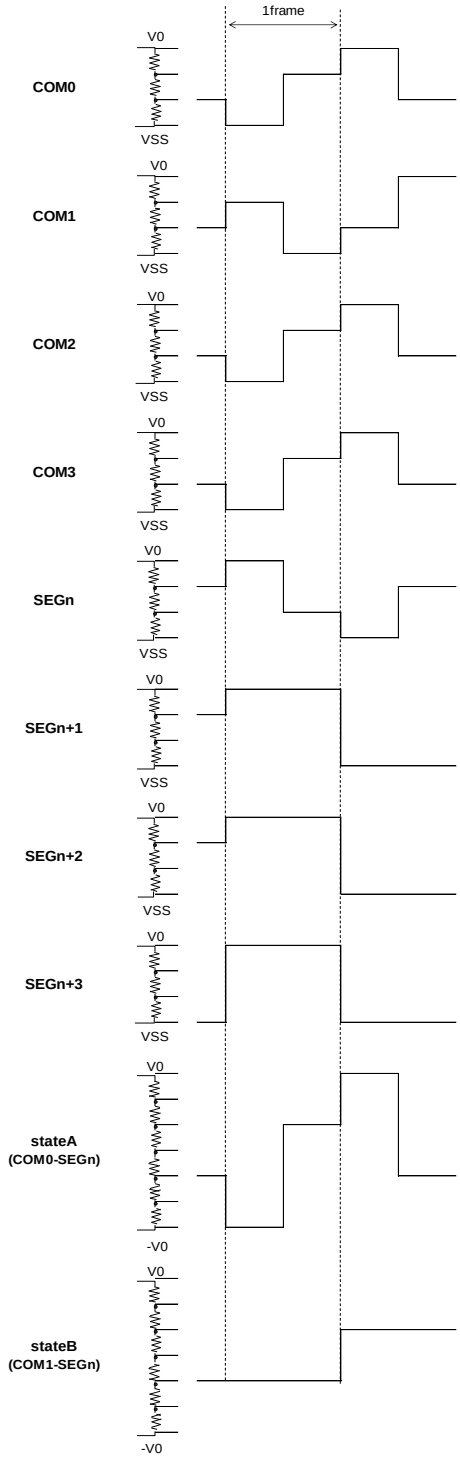
Line Inversion



Frame Inversion



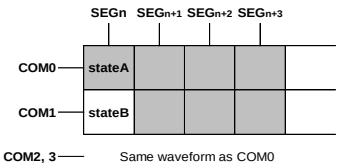




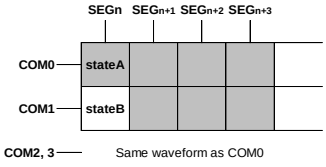
LCD Driving Waveform – continued

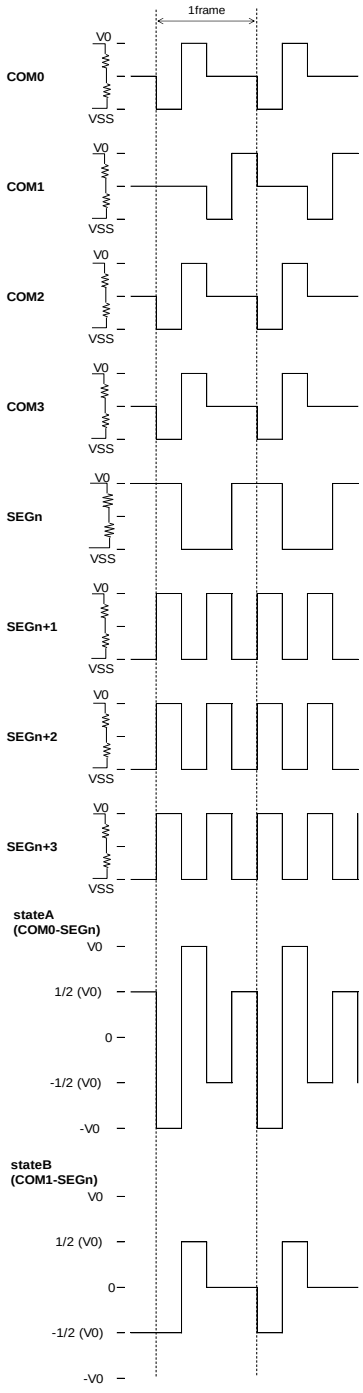
(1/2duty, 1/2bias)

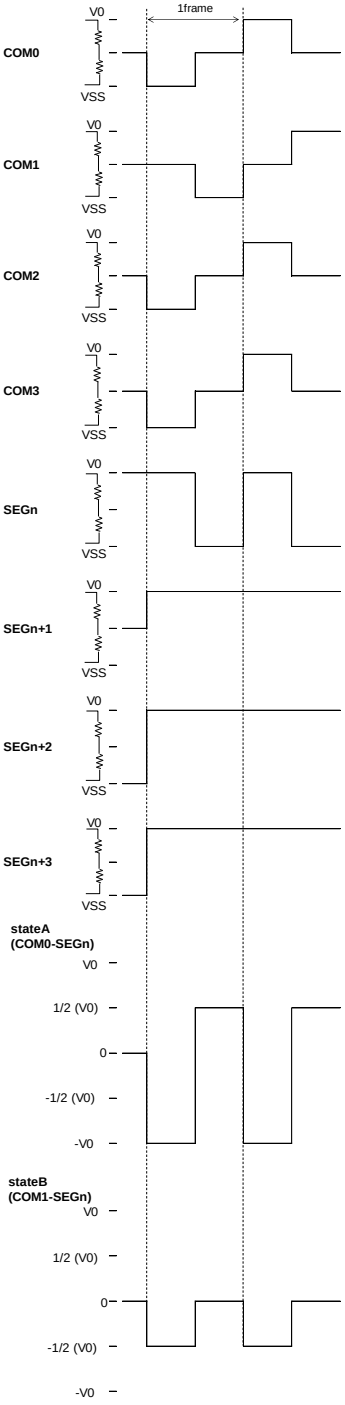
Line Inversion



Frame Inversion



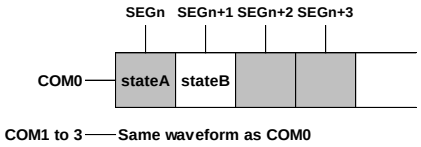




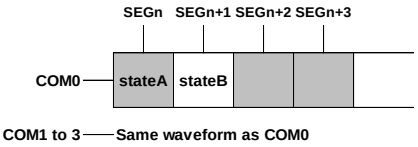
LCD Driving Waveform – continued

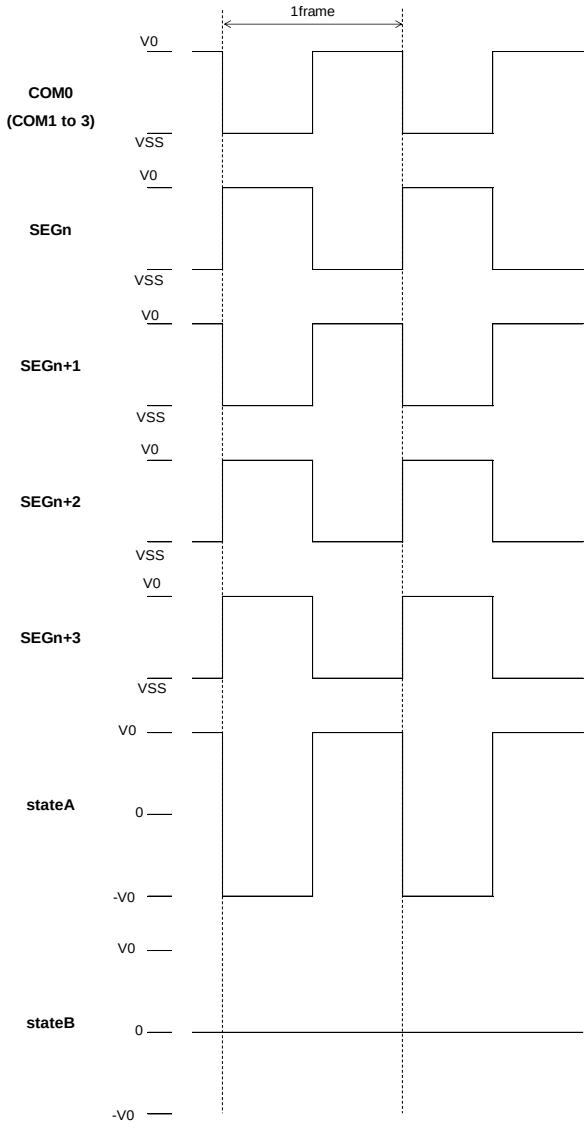
(Static)

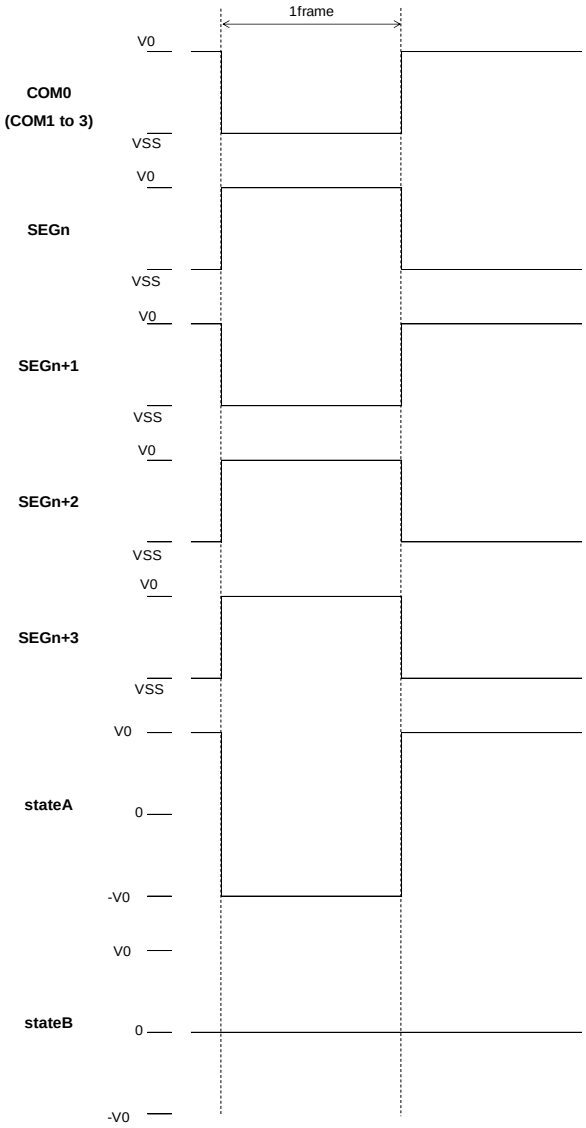
Line Inversion



Frame Inversion







Example of Display Data

When displaying a pattern as shown in Figure 12. Example Display Pattern on a panel with SEG / COM wiring patterns shown in Figure 10. Example COM Line Pattern and Figure 11. Example SEG Line Pattern, the following DDRAM data map is shown.

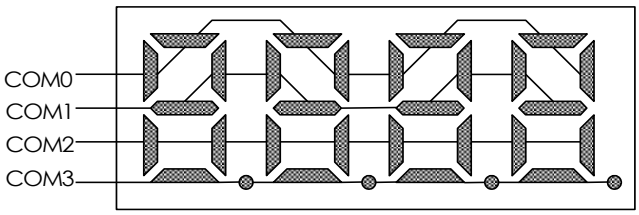


Figure 10. Example COM Line Pattern

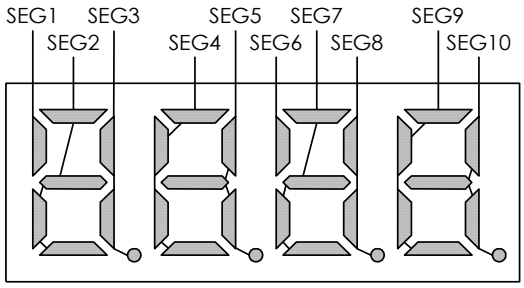


Figure 11. Example SEG Line Pattern

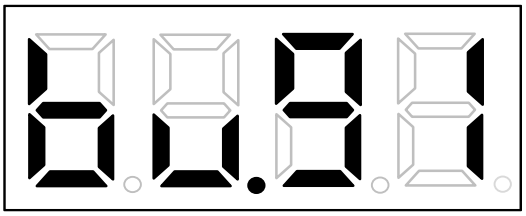


Figure 12. Example Display Pattern

<DDRAM data mapping in Figure 12 display pattern>

		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COM0	D0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
COM1	D1	0	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
COM2	D2	0	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0
COM3	D3	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Address		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h

Initialize Sequence

Follow the Power On sequence below to initialize condition.

Power On
↓
STOP Condition
↓
START Condition
↓
Issue Slave Address
↓
Execute Software Reset by sending ICSET command.

After Power On and before sending initialize sequence, each register value, DDRAM address and DDRAM data are random.

Start Sequence

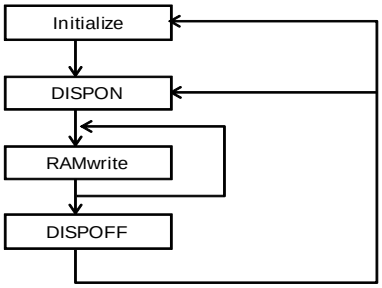
Start Sequence Example1

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power On	-	-	-	-	-	-	-	-	VDD = 0 → 3.3 V (tr = 1 ms) VLCD = 0 → 5.0 V
	↓	-	-	-	-	-	-	-	-	-
2	Wait 100 µs	-	-	-	-	-	-	-	-	Initialize
	↓	-	-	-	-	-	-	-	-	-
3	Stop	-	-	-	-	-	-	-	-	STOP Condition
	↓	-	-	-	-	-	-	-	-	-
4	Start	-	-	-	-	-	-	-	-	START Condition
	↓	-	-	-	-	-	-	-	-	-
5	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
	↓	-	-	-	-	-	-	-	-	-
6	ICSET	1	1	1	0	1	0	1	0	Software Reset
	↓	-	-	-	-	-	-	-	-	-
7	BLKCTL	1	1	1	1	0	*	0	0	Blink OFF
	↓	-	-	-	-	-	-	-	-	-
8	DISCTL	1	0	1	0	0	0	1	0	80 Hz, Line Inversion, Normal mode
	↓	-	-	-	-	-	-	-	-	-
9	APCTL	1	1	1	1	1	0	0	0	Set MSB of EVRSET
	↓	-	-	-	-	-	-	-	-	-
10	EVRSET	1	1	1	0	0	0	0	0	EVRSET V0 = 1.00 x VLCD
	↓	-	-	-	-	-	-	-	-	-
11	ICSET	1	1	1	0	1	*	0	0	RAM MSB address set
	↓	-	-	-	-	-	-	-	-	-
12	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓	-	-	-	-	-	-	-	-	-
13	Display Data	*	*	*	*	*	*	*	*	address 00h to 01h
	Display Data	*	*	*	*	*	*	*	*	address 02h to 03h
	⋮	-	-	-	-	-	-	-	-	⋮
	Display Data	*	*	*	*	*	*	*	*	address 2Ah to 2Bh
	↓	-	-	-	-	-	-	-	-	-
14	Stop	-	-	-	-	-	-	-	-	STOP Condition
	↓	-	-	-	-	-	-	-	-	-
15	Start	-	-	-	-	-	-	-	-	START Condition
	↓	-	-	-	-	-	-	-	-	-
16	Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
	↓	-	-	-	-	-	-	-	-	-
17	MODESET	1	1	0	0	1	0	0	0	Display On, 1/4 Duty, 1/3 Bias
	↓	-	-	-	-	-	-	-	-	-
18	Stop	-	-	-	-	-	-	-	-	STOP Condition

(*: don't care)

Start Sequence- continued

Start Sequence Example2



Initialize Sequence

DISPON Sequence

RAM w rite Sequence

DISPOFF Sequence

BU91R63CH-M is initialized with “Initialize Sequence”, starts to display with “DISPON Sequence”, updates Display data with “RAM Write Sequence” and stops the display with “DISPOFF Sequence”.
Execute “DISPON Sequence” in order to restart display.

Initialize Sequence (In case of VDD≠VLCD)

Input	DATE								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
VDD On									
Wait 100 µs									
STOP									
START									
Slave Adress	0	1	1	1	1	1	0	0	Issue Slave Address
ISECT	1	1	1	0	1	0	1	0	Execute Software Reset
VLCD ON									
STOP									
START									
Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
ICSET	1	1	1	0	1	0	1	0	Execute Software Reset
MODESET	1	1	0	0	0	0	0	0	Display Off
ICSET	1	1	1	0	1	0	0	0	Set MSB of RAM address
ADSET	0	0	0	0	0	0	0	0	Set RAM Address
Display Data	*	*	*	*	*	*	*	*	Display data
:									
STOP									

Initialize Sequence (In case of VDD=VLCD)

Input	DATE								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
VDD, VLCD On									
Wait 100 µs									
STOP									
START									
Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
ICSET	1	1	1	0	1	0	1	0	Execute Software Reset
MODESET	1	1	0	0	0	0	0	0	Display Off
ICSET	1	1	1	0	1	0	0	0	Set MSB of RAM address
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display Data	*	*	*	*	*	*	*	*	Display data
:									
STOP									

DISPON Sequence

Input	DATE								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
ICSET	1	1	1	0	1	0	0	0	Set Internal OSC mode
DISCTL	1	0	1	0	0	0	1	0	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
EVRSET	1	1	1	0	0	0	0	0	Set Contrast Setting
MODESET	1	1	0	0	1	0	0	0	Display On
STOP									

RAM Write Sequence

Input	DATE								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
DISCTL	1	0	1	0	0	0	1	0	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
EVRSET	1	1	1	0	0	0	0	0	Set Contrast Setting
MODESET	1	1	0	0	1	0	0	0	Display On
ICSET	1	1	1	0	1	0	0	0	Set MSB of RAM address
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display Data	*	*	*	*	*	*	*	*	Display data
:									
STOP									

DISPOFF Sequence

Input	DATE								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave Address	0	1	1	1	1	1	0	0	Issue Slave Address
MODESET	1	1	0	0	0	0	0	0	Display Off
STOP									

Abnormal operation may occur in BU91R63CH-M due to the effect of noise or other external factor.
To avoid this phenomenon, it is highly recommended to input command according to sequence described above during initialization, Display On/Off and refresh of RAM data.

Cautions in Power ON/OFF

To avoid unintended display errors, malfunctions and abnormal currents, use the following sequence when turning the power On and Off.
Be sure to turn on the VDD power supply first before turning on the VLCD power supply.
When turning off the power, be sure to turn off the VLCD power supply first, and then turn off the VDD power supply.
Also, satisfy the conditions of $t_1 > 0$ ns and $t_2 > 0$ ns. Data transmission / reception may fail, so do not transfer data while the power supply voltage is rising or falling.

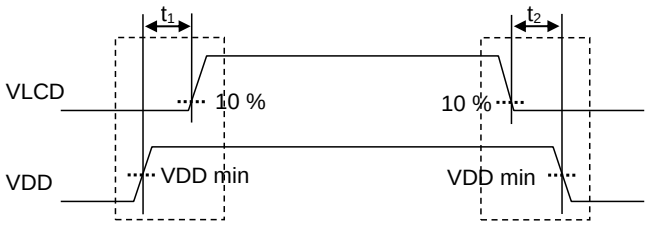


Figure 13. Recommended Power ON/OFF Sequence

BU91R63CH-M has a POR circuit (Power On Reset) and Software Reset function.
To ensure the operation, observe the following conditions when the power is turned on.
To operate the POR circuit, start up the VDD power supply so that the following recommended conditions for t_R, t_F, t_{OFF}, and V_{BOT} are satisfied.
To enable the POR circuit, T0 must be set to VSS.

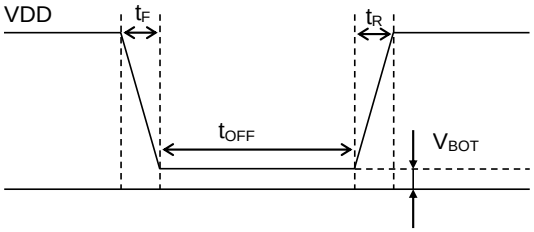


Figure 14. Power ON/OFF Waveform

Recommended condition of t_R, t_F, t_{OFF}, V_{BOT} (Ta = 25 °C)

t_R(*Note*)	t_F(*Note*)	t_{OFF}(*Note*)	V_{BOT}(*Note*)
1 ms to 500 ms	1 ms to 500 ms	Min 20 ms	Less than 0.1 V

(*Note*) Not 100 % tested.

If the above recommended conditions cannot be satisfied, execute the following sequence immediately after turning on the power. When T0 = VDD, this sequence must also be executed, since the POR circuit is disabled. However, since the command cannot be accepted when the power is turned off, Software Reset is not the same operation as POR.

1. Generate STOP Condition

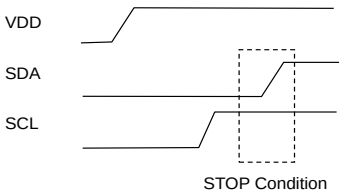


Figure 15. Stop Condition

2. Generate START Condition.

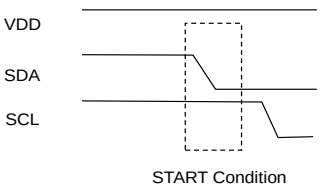


Figure 16. Start Condition

3. Issue Slave Address

4. Execute Software Reset (ICSET) Command

Display Off Operation in External Clock Mode

BU91R63CH-M enters the DISPOFF sequence in synchronization with the frame after receiving the MODESET (Display Off) command. All SEGMENT and COMMON outputs stop after writing 1 frame OFF level. Therefore, when using in external clock mode, input of an external clock according to each frame frequency setting is required after completion of MODESET (Display Off) transmission. The number of external clocks required for setting each frame frequency is as follows according to the frame frequency setting of the DISCTL command.

Input the external clock as below.

DISCTL 80 Hz setting (Frame frequency = external clock / 512 [Hz]) , 1024 clk or more
DISCTL 130 Hz setting (Frame frequency = external clock / 315 [Hz]) , 630 clk or more
DISCTL 64 Hz setting (Frame frequency = external clock / 648 [Hz]) , 1296 clk or more
DISCTL 200 Hz setting (Frame frequency = external clock / 205 [Hz]) , 410 clk or more

Refer to the timing chart below.

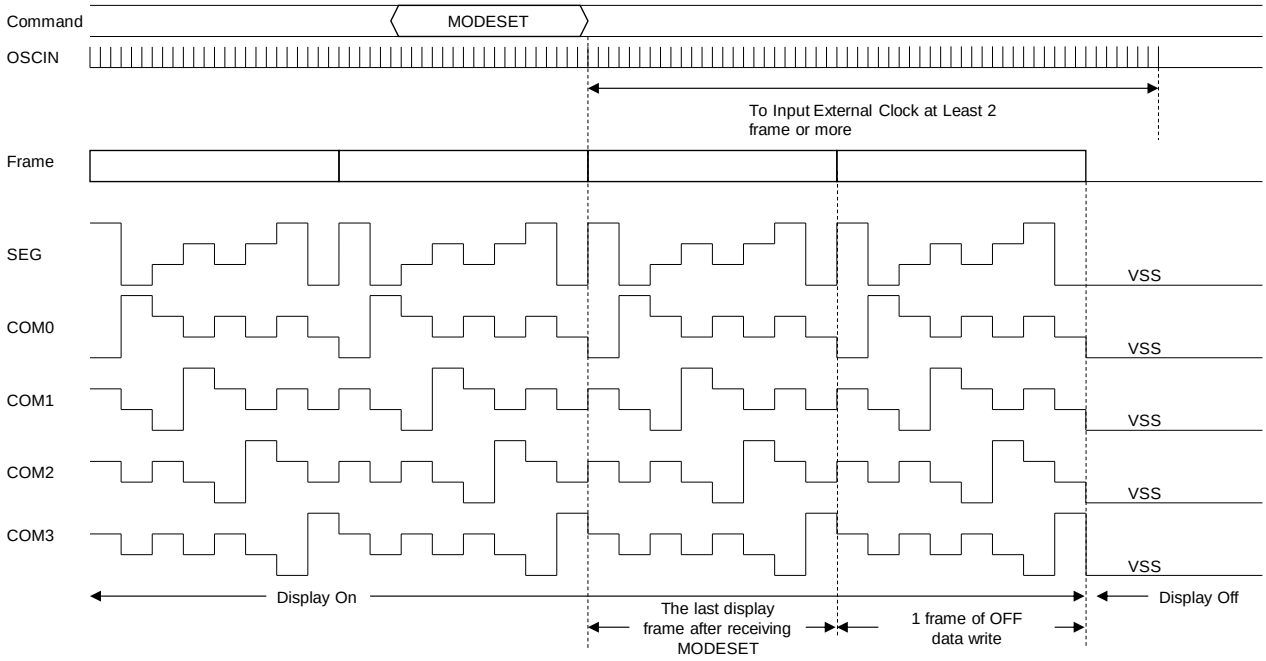


Figure 17. External Clock Stop Timing

In external clock mode, the clock signal must always be supplied to BU91R63CH-M. If the clock supply is stopped, the display may freeze in a DC state that is not suitable for the LCD.

Note on The Multiple Device Connection to 2-wire Serial Interface

Do not access other devices on the same bus with the BU91R63CH-M VDD Power Off.

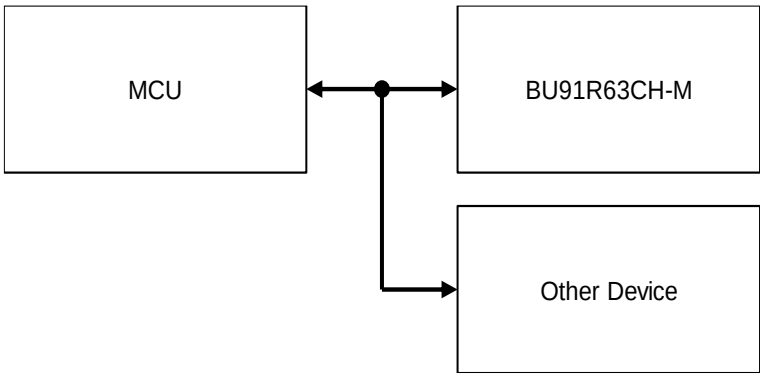


Figure 18. Example of BUS Connection

A capacitor is connected between the drain and gate of the SDA output NMOS transistor to control the slew rate (see the figure below). When power (VDD) is not applied, the gate is in a high impedance state.

When the SDA pin transitions from Low to High while in this state, current is supplied via the slew rate control capacitor, and the gate voltage (Vg) rises.

When this voltage (Vg) exceeds the threshold voltage (Vth), the output transistor is turned on and current (Ids) is drawn from the SDA pin.

The SDA signal maintains the power supply voltage (VDD) by the external resistor (R), but if the voltage drop (R x Ids) increases due to the current (Ids), is not possible to maintain “1” as the logical value of the SDA signal level.
Be sure to apply power (VDD) to BU91R63CH-M even when multiple devices are connected on the same bus.

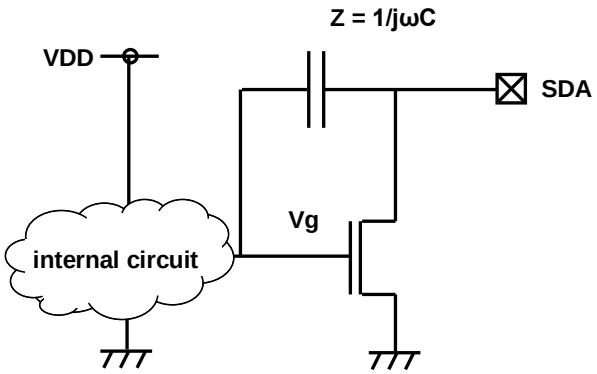


Figure 19. SDA Output Cell Structure

Note in Case that the SDA is Stuck LOW

Normally, the state of SDA is controlled by the MCU, and BU91R63CH-M controls SDA to the VSS level only when “0” is output during ACK and Read Mode. If the data line (SDA) is stuck at LOW unexpectedly, the MCU needs to send a dummy byte with START and STOP conditions twice as shown below (Please set SDA to High at this time). This sequence returns from the SDA stuck state.

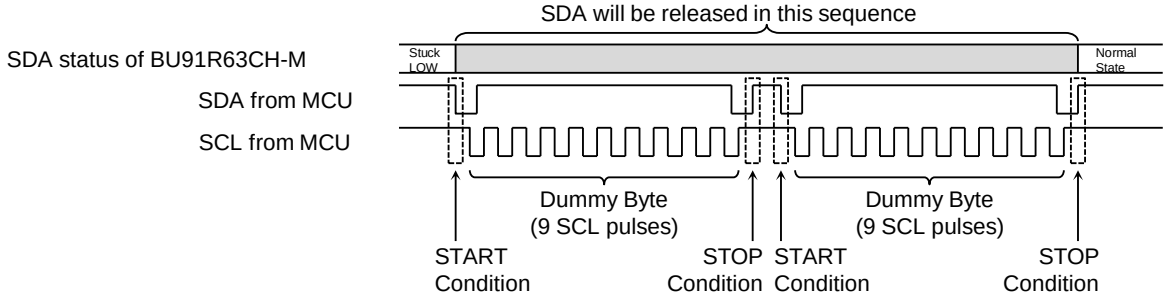


Figure 20. Recovery sequence from SDA stuck

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Operational Notes – continued

12. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

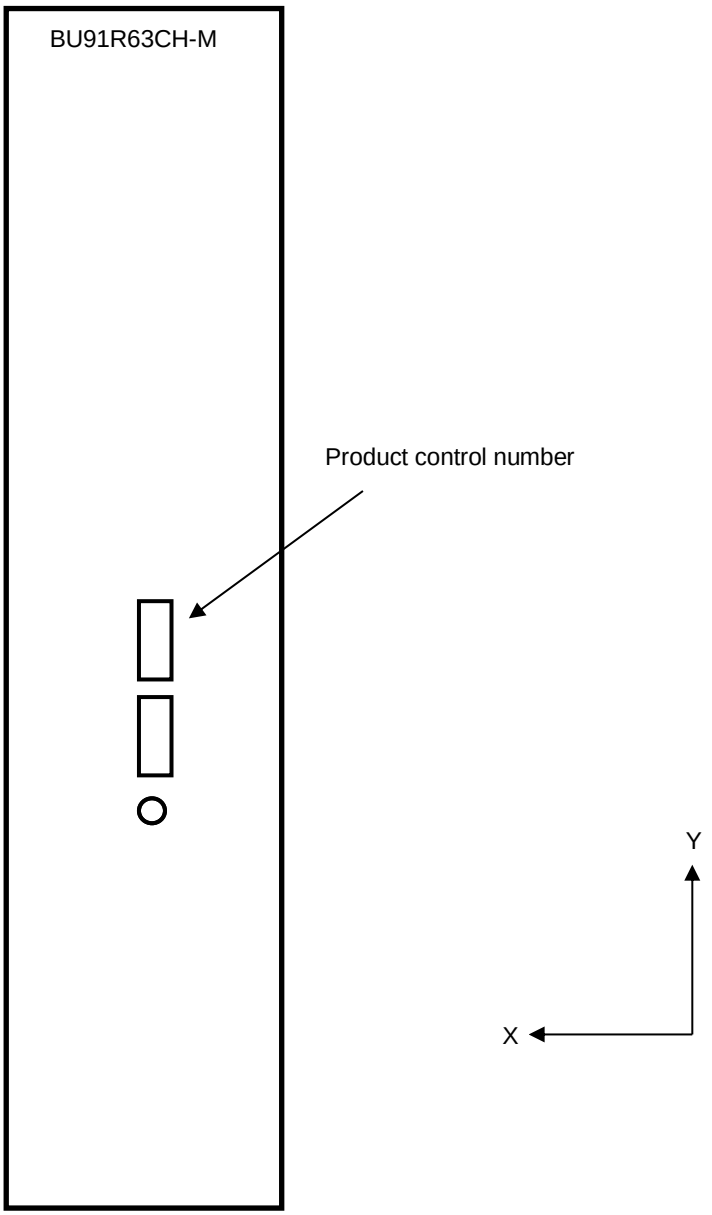
Ordering Information

B U 9 1 R 6 3 C H	-	M 3 B W
Part Number		Product Rank M: for Automotive

Minimum Order Quantity (MOQ)

Orderable Part Number	Minimum Order Quantity
BU91R63CH-M3BW	1,360 pcs

Back Marking Diagram



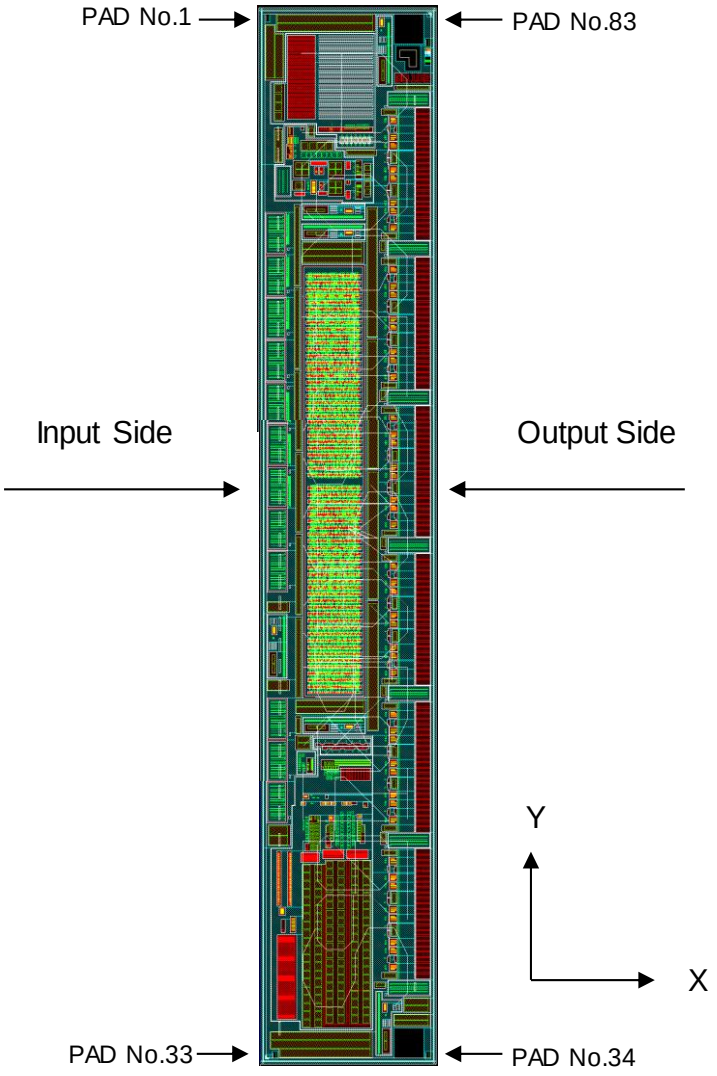
(Bump side down)

Refer to PAD Arrangement for the definition of X/Y coordinates.

Packing Quantity

Packing QTY. (Standard QTY)	Tray:	136	pcs / Tray
	Block:	680	pcs / Block (1 block = 5 trays)
	Vacuum Pack:	680	pcs / Vacuum pack (1 vacuum pack = 1 blocks)
	Inner Box	1,360	pcs / inner Box (1 inner box = 2 vacuum packs)
	Outer Box	2,720	pcs / outer Box (1 outer box = 2 inner boxes)

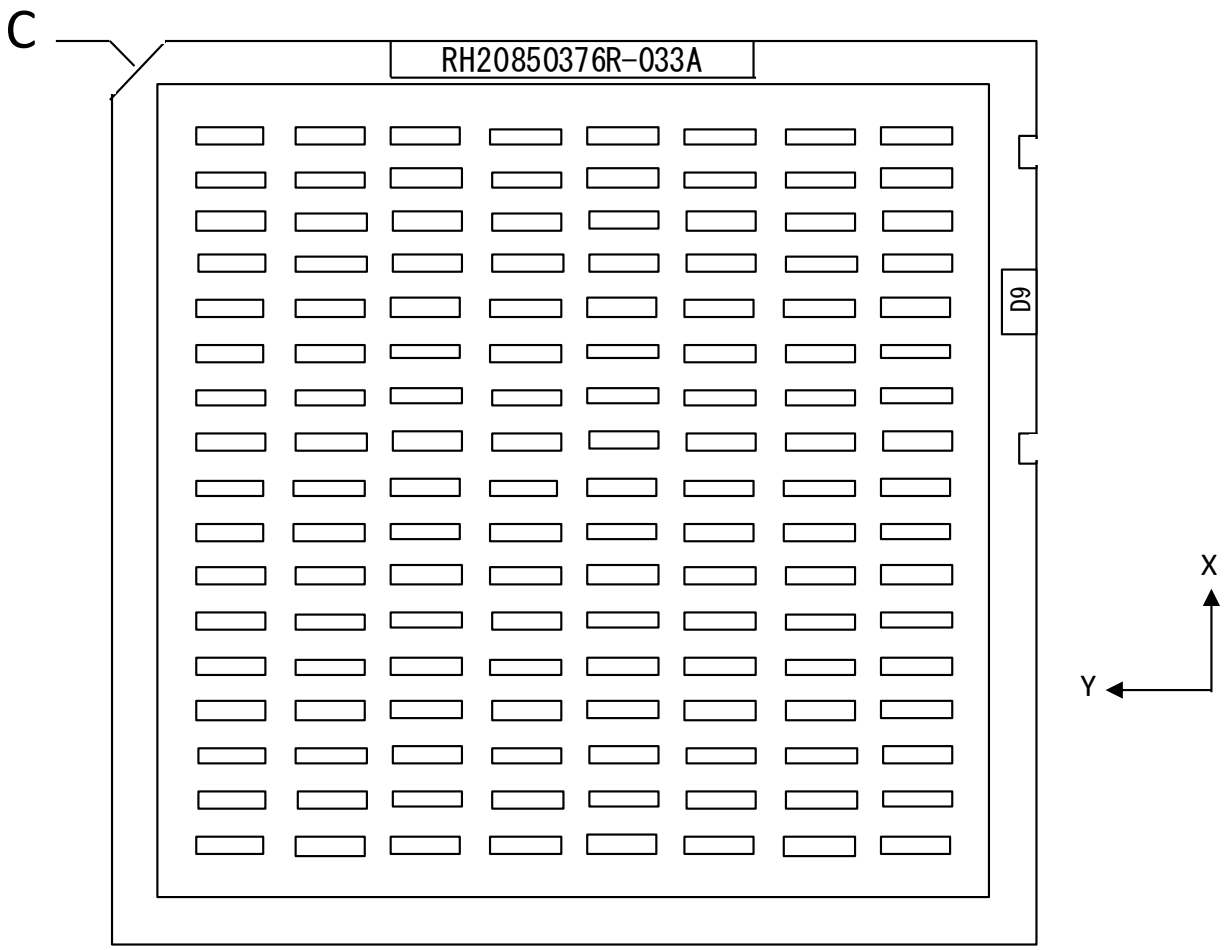
Pellet Drawing



(Bump side up)

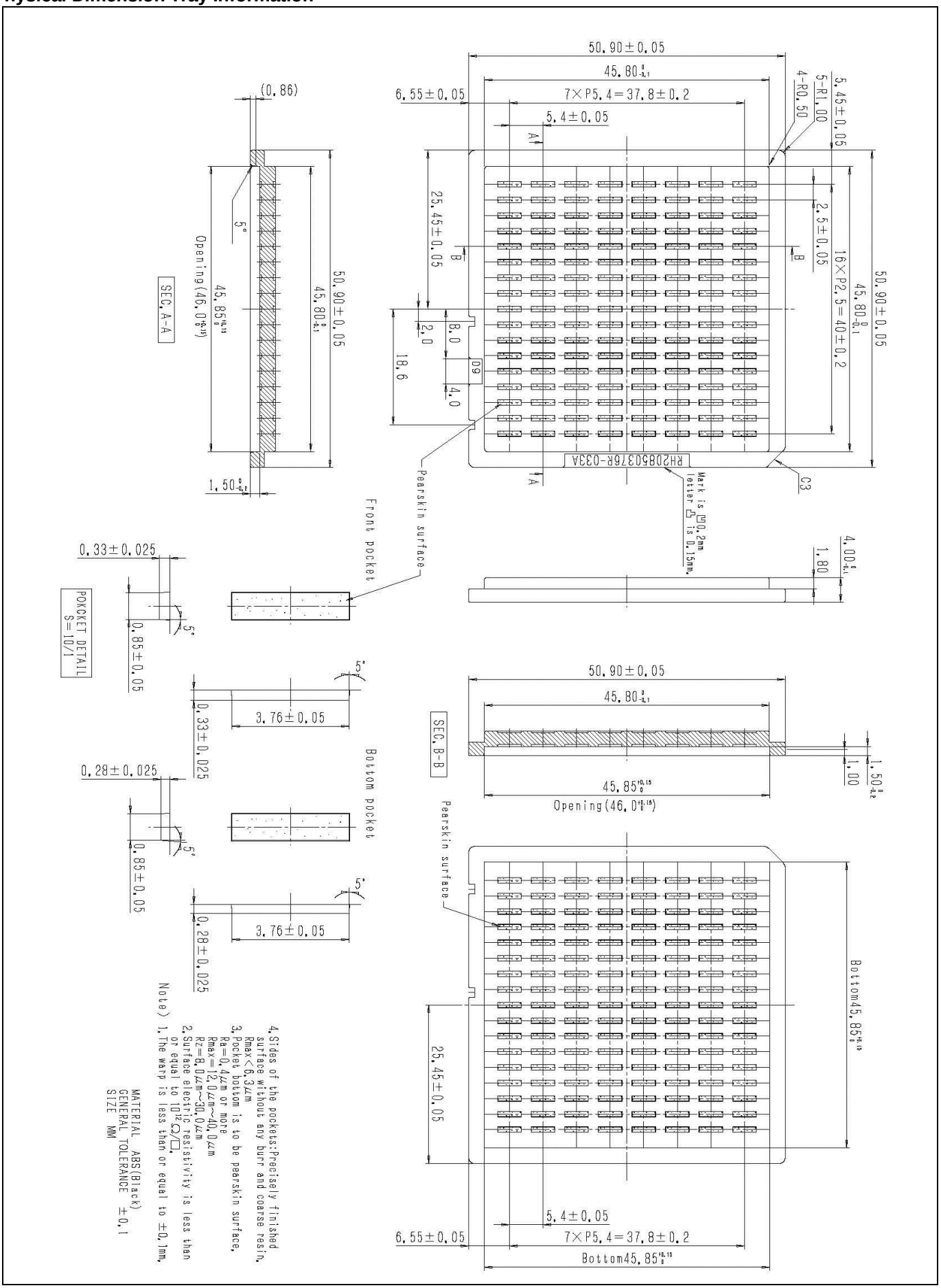
Package Condition

Products should be aligned to the same direction with Bump side up.
"Chamfering" side is aligned with X/Y direction of the chip as shown in the following drawing.



Refer to PAD Arrangement for the definition of X/Y coordinates.

Physical Dimension Tray Information



Revision History

Data	Revision	Changes
10 Feb. 2016	001	New Release
15 Oct. 2019	002	P5 Add Terminal Resistance P6 Add Dimension P8 Move Operational Temperature Range to Recommend Operating Conditions P8 Add Maximum Junction Temperature P20 Add The relationship of LCD display contrast setting and VLCD Voltage P31 Add the description in Cautions in Power ON/OFF (Transcription from Operational Notes) P32 Add Display Off Operation in External Clock Mode P33 Add Note on The Multiple Device Connection to 2-wire Serial Interface P33 Add Note in case that the SDA is stuck LOW P34 Delete Thermal Consideration P35 Move Data transmission to Cautions in Power ON/OFF P36 Change Minimum Order Quantity P37 to P38 Add Packing Quantity, Pellet Drawing, Package Condition - Change Figure number - Correction of errors.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

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2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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