A/D Converter Series for Automotive

Successive Approximation A/D Converter 12 bit, 8-channel, I²C Interface

BD79124MUF-C

General Description

The BD79124MUF-C is a general purpose, 12 bit 8-channel successive approximation A/D converter.

Features

- AEC-Q100 Qualified(Note 1)
- Low Power Consumption
- Small VQFN16FV3030 Package
- 2-wire Serial Bus Interface (Supports up to 3.4 MHz)
- Single-ended Inputs
- Alert Function

(Note 1) Grade 1

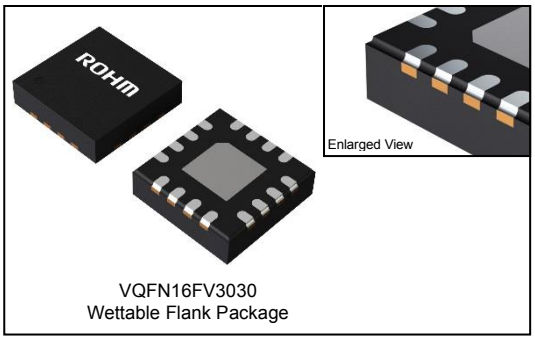
Applications

- Cluster Displays
- Infotainment
- Battery Management Systems (BMS)

Key Specifications

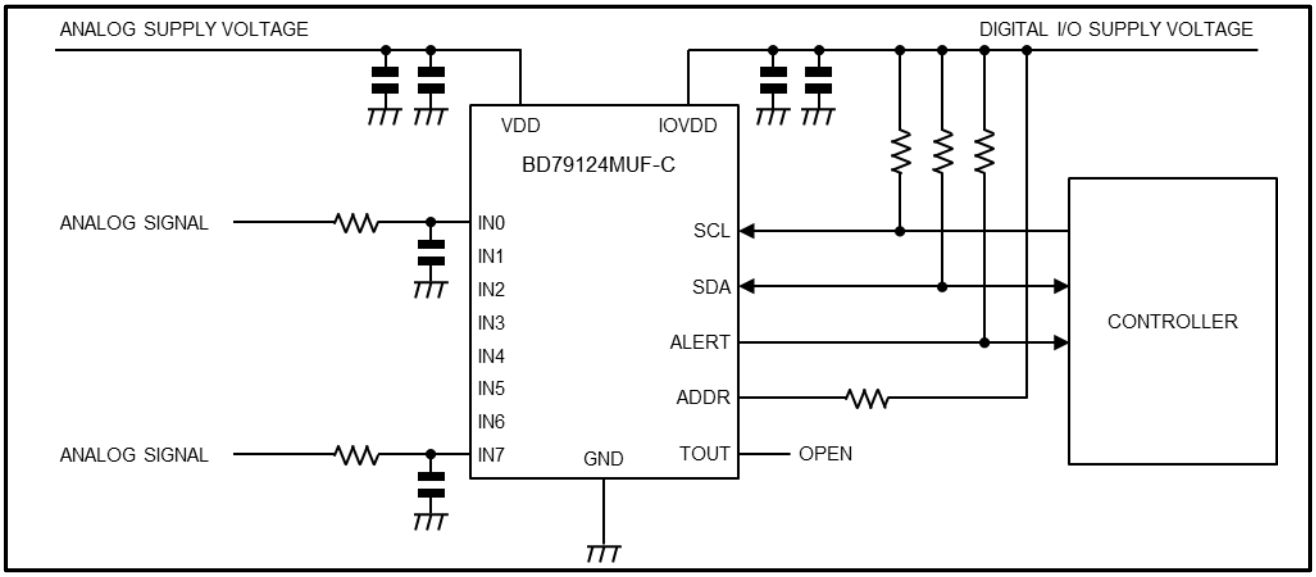
- Input Voltage Range (VDD): 2.70 V to 5.25 V
- Input Voltage Range (IOVDD): 1.65 V to 5.25 V
- Power Consumption:
  (In High-speed mode) 0.9 mW @ V_{DD} = 3.6 V (Typ)
  1.8 mW @ V_{DD} = 5.25 V (Typ)
- INL: ±1.0 LSB @ V_{DD} = 3 V (Typ)
- DNL: ±0.99 LSB @ V_{DD} = 3 V (Typ)
- SNR: 72 dB @ V_{DD} = 3 V (Typ)
- SINAD: 72 dB @ V_{DD} = 3 V (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package	W (Typ) x D (Typ) x H (Max)
VQFN16FV3030	3.0 mm x 3.0 mm x 1.0 mm



VQFN16FV3030
Wettable Flank Package

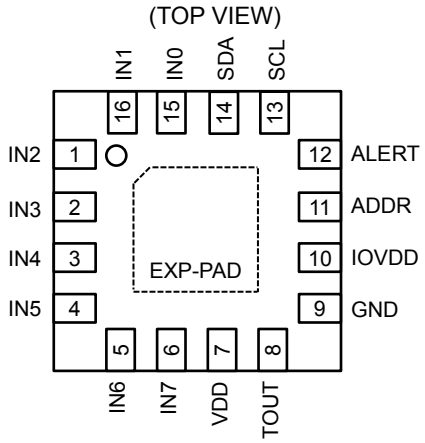
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

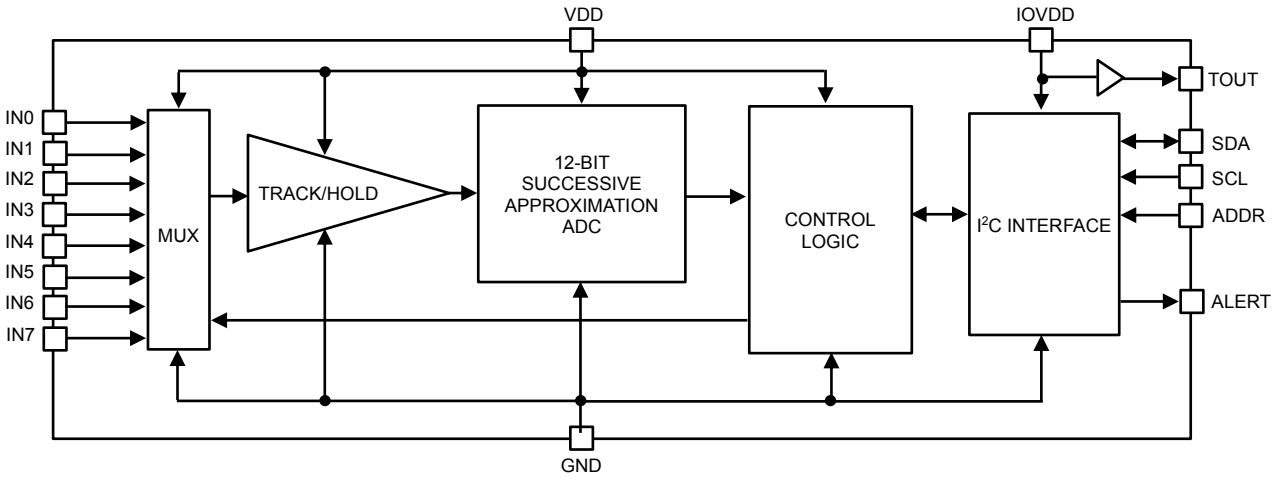
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	IN2	Analog input pin 2. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
2	IN3	Analog input pin 3. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
3	IN4	Analog input pin 4. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
4	IN5	Analog input pin 5. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
5	IN6	Analog input pin 6. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
6	IN7	Analog input pin 7. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
7	VDD	Analog/Digital power supply pin. This voltage is the full scale of the AD conversion.
8	TOUT	Output pin for IOVDD voltage. This pin can be used as an ADDR pin pull-up destination. If used, do not connect a bypass capacitor to this pin. If not used, leave this pin OPEN.
9	GND	Analog/Digital ground pin. This voltage is the zero scale of the AD conversion.
10	IOVDD	Digital I/O power supply pin.
11	ADDR	Input pin for selecting the device I^2C address.
12	ALERT	Output pin for Digital alert.
13	SCL	Input pin for serial clock.
14	SDA	Input/output pin for serial data.
15	IN0	Analog input pin 0. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
16	IN1	Analog input pin 1. The input voltage range must be between 0 V and V_{DD}. Or GPO pin.
-	EXP-PAD	The EXP-PAD is connected to GND.

Block Diagram



Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Analog/Digital Supply Voltage	V_{DD}	5.7	V
Digital I/O Supply Voltage	V_{IOVDD}	V_{DD}+0.3, max 5.7	V
Analog Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	-0.3 to V_{IOVDD}+0.3	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
VQFN16FV3030				
Junction to Ambient	θ_{JA}	189.0	57.5	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	23	10	°C/W

(Note 2) Based on JESD51-2A (Still-Air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 6)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 6) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog/Digital Supply Voltage	V_{DD}	2.70	-	5.25	V
Digital I/O Supply Voltage	V_{IOVDD}	1.65	-	V_{DD}	V
Analog Input Voltage	V_{IN}	0	-	V_{DD}	V
Digital Input Voltage	V_{DIN}	0	-	V_{IOVDD}	V
Operating Temperature	Topr	-40	+25	+125	°C
Clock Frequency	f_{SCL}	100	-	3400	kHz
Sampling Rate	f_S	-	-	140	kSPS

Electrical Characteristics

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V, f_{SCL} = 3.4 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Statistic Converter Characteristics						
Resolution with No Missing Codes	R_{ES}	-	12	-	bit	
Integral Non-linearity1	I_{NL1}	-1.2	-	+1.2	LSB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Integral Non-linearity2	I_{NL2}	-1.0	-	+1.0	LSB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Differential Non-linearity1	D_{NL1}	-0.99	-	+0.99	LSB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Differential Non-linearity2	D_{NL2}	-0.99	-	+0.99	LSB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Offset Error1	O_{E1}	-2.9	±1.1	+2.9	LSB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Offset Error2	O_{E2}	-2.3	±1.1	+2.3	LSB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Gain Error1	G_{E1}	-2.2	±0.8	+2.2	LSB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Gain Error2	G_{E2}	-2.0	±0.8	+2.0	LSB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Dynamic Converter Characteristics (f_{IN} = 2 kHz, V_{IN} = -0.02 dBFS)						
Signal to Noise and Distortion Ratio1	S_{INAD1}	70	72	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Signal to Noise and Distortion Ratio2	S_{INAD2}	70	72	-	dB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Signal to Noise Ratio1	S_{NR1}	70.8	72	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Signal to Noise Ratio2	S_{NR2}	70.8	72	-	dB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Total Harmonic Distortion	T_{HD}	-	-80	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Spurious-free Dynamic Range	S_{FDR}	-	82	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Effective Number of Bits1	E_{NOB1}	11.3	11.6	-	bit	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Effective Number of Bits2	E_{NOB2}	11.3	11.6	-	bit	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
Inter-channel Isolation1	I_{SO1}	-	-90	-	dB	Ta = 25 °C, V_{DD} = 5.0 V V_{IOVDD} = 3.0 V
Inter-channel Isolation2	I_{SO2}	-	-90	-	dB	Ta = 25 °C, V_{DD} = 3.0 V V_{IOVDD} = 3.0 V
AD Conversion Time1	t_{CONV1}	-	1.2	1.8	µs	BUSYTIME = 00
AD Conversion Time2	t_{CONV2}	-	6.0	10	µs	BUSYTIME = 11
Track/Hold Acquisition Time1	t_{HOLD1}	0.15	0.25	-	µs	BUSYTIME = 00
Track/Hold Acquisition Time2	t_{HOLD2}	0.6	1.0	-	µs	BUSYTIME = 11

Electrical Characteristics – continued

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V, f_{SCL} = 3.4 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Analog Input Characteristics						
Input Capacitance	C_{SH}	-	28	-	pF	V_{DD} = 5 V
Input Range	V_{IN}	0	-	V_{DD}	V	
Digital Input Characteristics (SCL,SDA)						
High Input Voltage	V_{IH}	0.7 x V_{IOVDD}	-	-	V	
Low Input Voltage	V_{IL}	-	-	0.3 x V_{IOVDD}	V	
Digital Output Characteristics (SDA)						
Output Low Voltage1	V_{OL1}	-	-	0.4	V	I_{SINK} = 2 mA, V_{IOVDD} > 2 V
Output Low Voltage2	V_{OL2}	-	-	V_{IOVDD} x 0.2	V	I_{SINK} = 2 mA, V_{IOVDD} ≤ 2 V
Output Low Current1	I_{OL1}	-	-	3	mA	V_{OL} = 0.4 V, Standard and Fast mode
Output Low Current2	I_{OL2}	-	-	6	mA	V_{OL} = 0.6 V, Fast mode
Output Low Current3	I_{OL3}	-	-	20	mA	V_{OL} = 0.4 V, Fast mode plus
Digital Output Characteristics (GPO)						
Output High Voltage	V_{OH}	0.8 x V_{DD}	-	V_{DD}	V	
Output Low Voltage	V_{OL}	0	-	V_{DD} x 0.2	V	
Digital Output Characteristics (ALERT)						
Output High Voltage1	V_{OH1}	V_{IOVDD} - 0.20	V_{IOVDD} - 0.03	-	V	I_{SOURCE} = 200 µA
Output High Voltage2	V_{OH2}	-	V_{IOVDD} - 0.1	-	V	I_{SOURCE} = 1 mA
Output Low Voltage1	V_{OL1}	-	0.02	0.40	V	I_{SINK} = 200 µA
Output Low Voltage2	V_{OL2}	-	0.1	-	V	I_{SINK} = 1 mA
Current Consumption						
Operational Current Consumption1	I_{A1}	-	340	500	µA	V_{DD} = V_{IOVDD} = 5.25 V, I^2C High-speed mode
Operational Current Consumption2	I_{A2}	-	260	320	µA	V_{DD} = V_{IOVDD} = 3.6 V, I^2C High-speed mode
Operational Current Consumption3	I_{A3}	-	140	185	µA	V_{DD} = V_{IOVDD} = 5.25 V, I^2C Fast mode plus
Operational Current Consumption4	I_{A4}	-	100	140	µA	V_{DD} = V_{IOVDD} = 3.6 V, I^2C Fast mode plus
Operational Current Consumption5	I_{A5}	-	76	104	µA	V_{DD} = V_{IOVDD} = 5.25 V, I^2C Fast mode
Operational Current Consumption6	I_{A6}	-	45	65	µA	V_{DD} = V_{IOVDD} = 3.6 V, I^2C Fast mode
Operational Current Consumption7	I_{A7}	-	49	63.5	µA	V_{DD} = V_{IOVDD} = 5.25 V, I^2C Standard mode
Operational Current Consumption8	I_{A8}	-	25.5	37.5	µA	V_{DD} = V_{IOVDD} = 3.6 V, I^2C Standard mode
Operational Current Consumption9	I_{A9}	-	40	50	µA	V_{DD} = V_{IOVDD} = 5.25 V, No conversion
Operational Current Consumption10	I_{A10}	-	20	30	µA	V_{DD} = V_{IOVDD} = 3.6 V, No conversion

Timing Specifications

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V

High-speed Mode

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCL clock frequency	f_{SCL}	-	-	3.4	MHz	
Setup time for a repeated START condition	t_{SU_STA}	160	-	-	ns	
Hold time for START condition	t_{HD_STA}	160	-	-	ns	
Low period of the SCL pin	t_{LOW}	160	-	-	ns	
High period for the SCL pin	t_{HIGH}	60	-	-	ns	
Data in hold time	t_{HD_DAT}	0	-	70	ns	
Data in setup time	t_{SU_DAT}	10	-	-	ns	
STOP condition setup time	t_{SU_STO}	160	-	-	ns	
SDA/SCL rise time	t_R	-	-	80	ns	
SDA/SCL fall time	t_F	-	-	80	ns	
Capacitive load for each bus line	C_B	-	-	15	pF	
Suppressible spike pulse width	t_{SP}	0	-	10	ns	

Standard Mode, Fast Mode, and Fast Mode Plus

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SCL clock frequency	f_{SCL}	-	-	1	MHz	
Setup time for a repeated START condition	t_{SU_STA}	260	-	-	ns	
Hold time for START condition	t_{HD_STA}	260	-	-	ns	
Low period of the SCL pin	t_{LOW}	500	-	-	ns	
High period for the SCL pin	t_{HIGH}	260	-	-	ns	
Data in hold time	t_{HD_DAT}	0	-	-	ns	
Data in setup time	t_{SU_DAT}	50	-	-	ns	
STOP condition setup time	t_{SU_STO}	260	-	-	ns	
SDA/SCL rise time	t_R	-	-	120	ns	
SDA/SCL fall time	t_F	-	-	120	ns	
Capacitive load for each bus line	C_B	-	-	60	pF	
Suppressible spike pulse width	t_{SP}	0	-	50	ns	

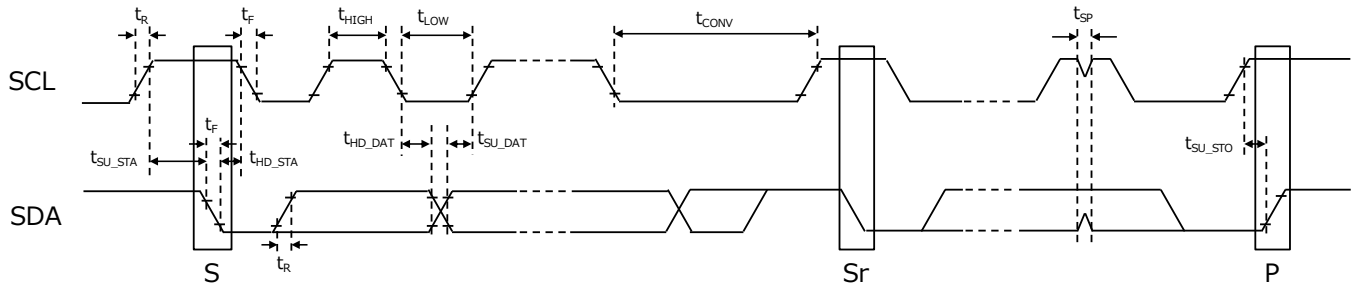


Figure 1. 2-wire Serial Bus Interface Timing Chart

Term Definitions

INTEGRAL NON-LINEARLITY (INL):
It is a measure of the deviation of each individual code from a line drawn from zero scale (0.5 LSB below the first code transition) through full scale (0.5 LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

DIFFERENTIAL NON-LINEARLITY (DNL):
It is the measure of the maximum deviation from the ideal step size of 1 LSB.

OFFSET ERROR (OE):
It is the deviation of the first code transition “(000…000) to (000…001)” from the ideal of 1.0 LSB.

FULL SCALE ERROR (FSE):
It is the deviation of the last code transition “(111…110) to (111…111)” from the ideal of “V_{DD}-1.0 LSB”.

GAIN ERROR (GE):
It is defined as full scale error minus offset error.

Ideal Transfer Characteristics
Figure 2 shows the ideal transfer characteristics of this product. Code transitions occur midway between successive integer LSB values, such as 1.0 LSB, 2.0 LSB, and so on. The LSB size for this product is V_{DD} / 4096. The output code format of the A/D converter is straight binary.

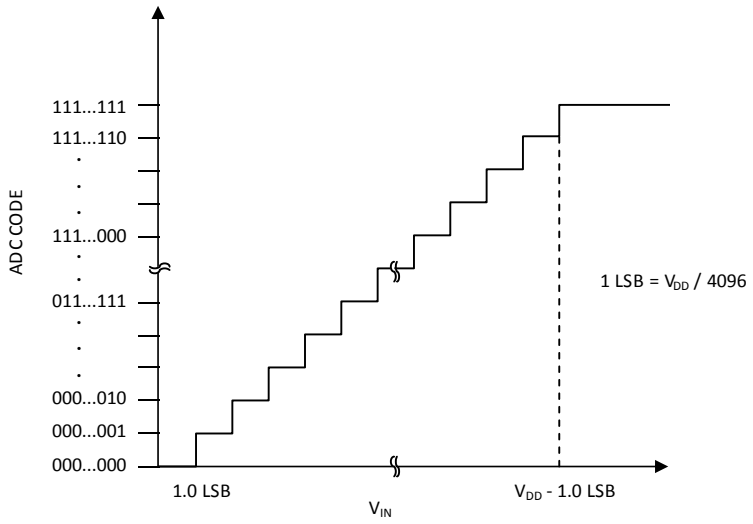


Figure 2. Ideal Transfer Characteristics

Term Definitions - continued

TOTAL HARMONIC DISTORTION (THD):

It is the ratio, expressed in dB or dBc, of the RMS total of the first 5 harmonic components at the output to the RMS level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

SIGNAL TO NOISE AND DISTORTION RATIO (SINAD):

It is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all other spectral components below half the sampling frequency, including harmonics but excluding DC component.

EFFECTIVE NUMBER OF BITS (ENOB):

It is another method of specifying Signal to Noise and Distortion Ratio. ENOB is defined as “(SINAD-1.76) / 6.02” and says that the converter is equivalent to a perfect A/D converter of this number of bits.

SIGNAL TO NOISE RATIO (SNR):

It is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all other spectral components below half the sampling frequency, not including harmonics and DC component.

SPURIOUS FREE DYNAMIC RANGE (SFDR):

It is the difference, expressed in dB, between the RMS value of the input signal to the RMS value of the peak spurious spectral component, where a peak spurious spectral component is any spurious signal present in the output spectrum that is not present at the input.

CONVERSION TIME:

It is the required time for the A/D converter to convert the input signal to the digital code.

Typical Performance Curves

(Reference Data)

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V

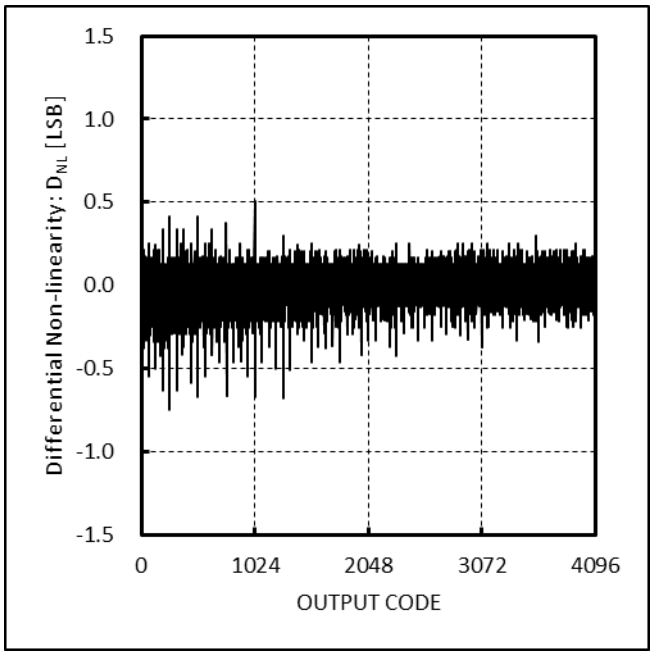


Figure 3. Differential Non-linearity vs OUTPUT CODE
(V_{IOVDD} = 3 V, V_{DD} = 5 V)

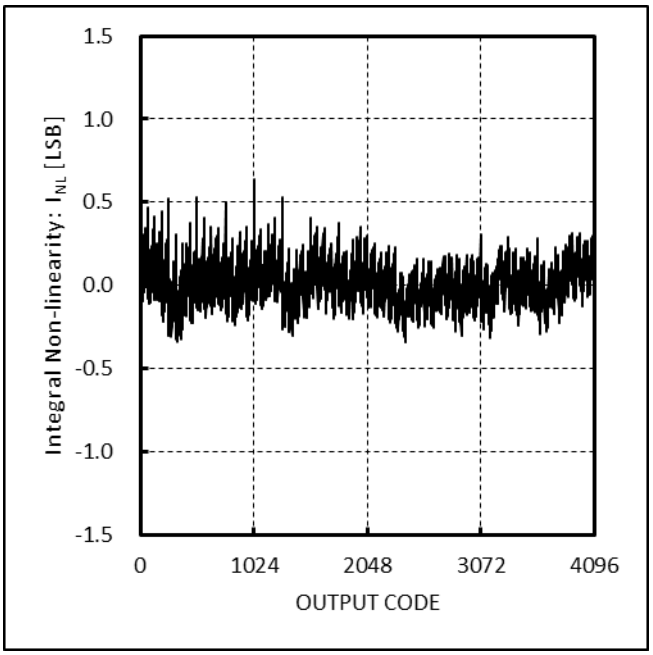


Figure 4. Integral Non-linearity vs OUTPUT CODE
(V_{IOVDD} = 3 V, V_{DD} = 5 V)

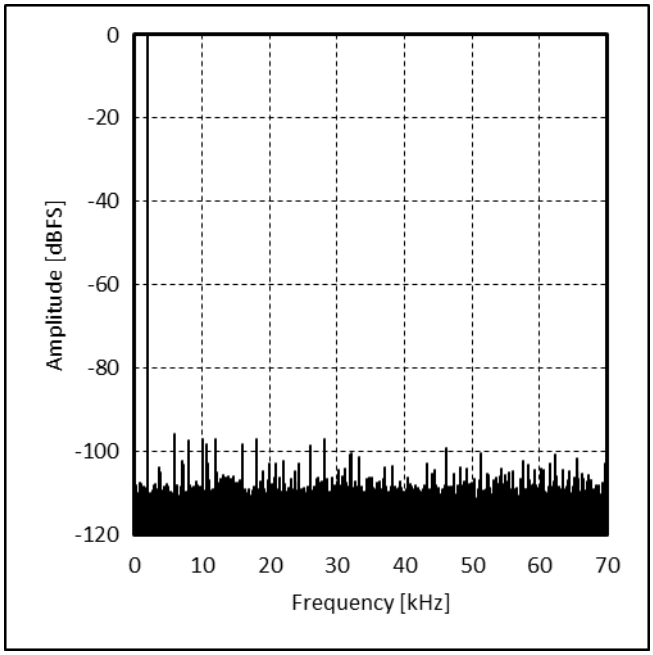


Figure 5. Amplitude vs Frequency
(V_{IOVDD} = 3 V, V_{DD} = 5 V, f_{IN} = 2 kHz)

Typical Performance Curves - continued

(Reference Data)

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V

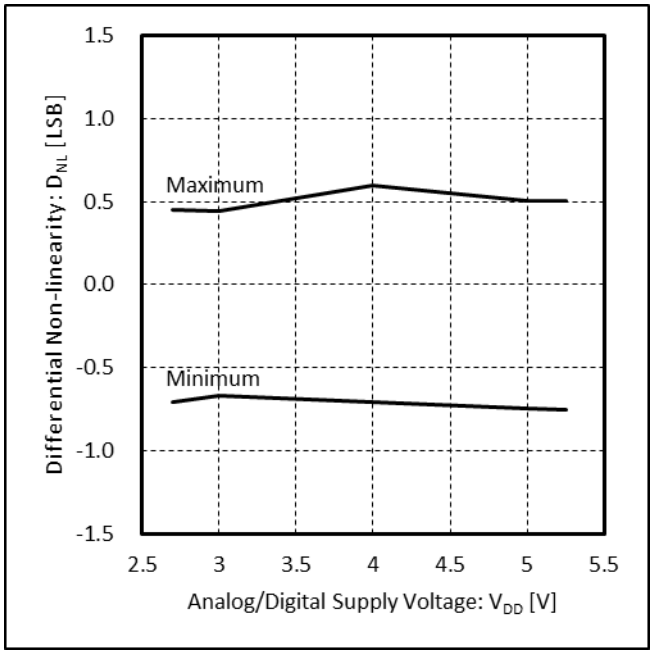


Figure 6.

Differential Non-linearity vs Analog/Digital Supply Voltage

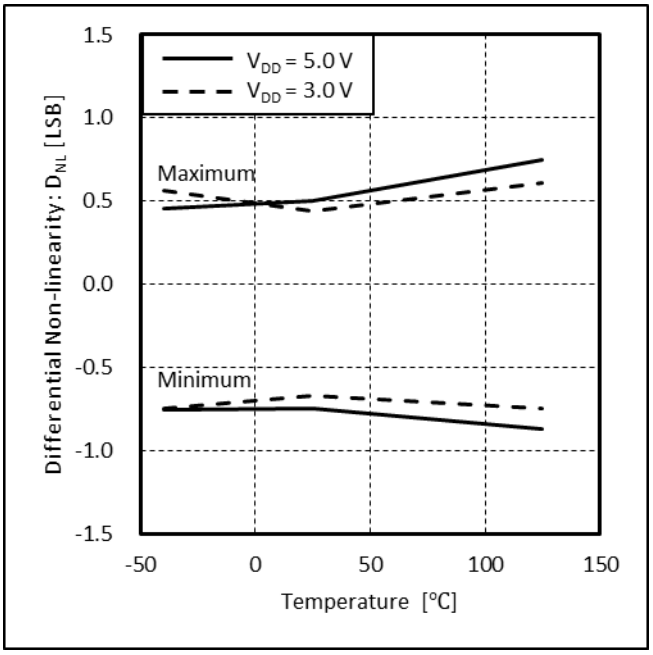


Figure 7. Differential Non-linearity vs Temperature

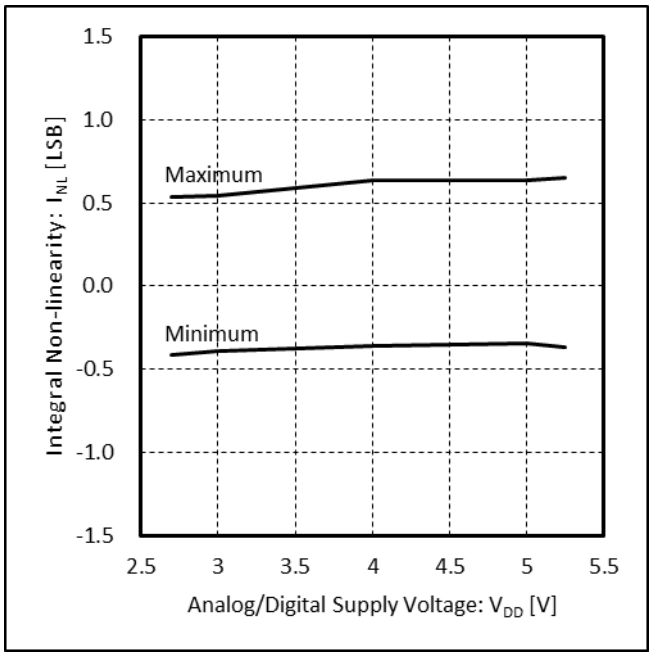


Figure 8.

Integral Non-linearity vs Analog/Digital Supply Voltage

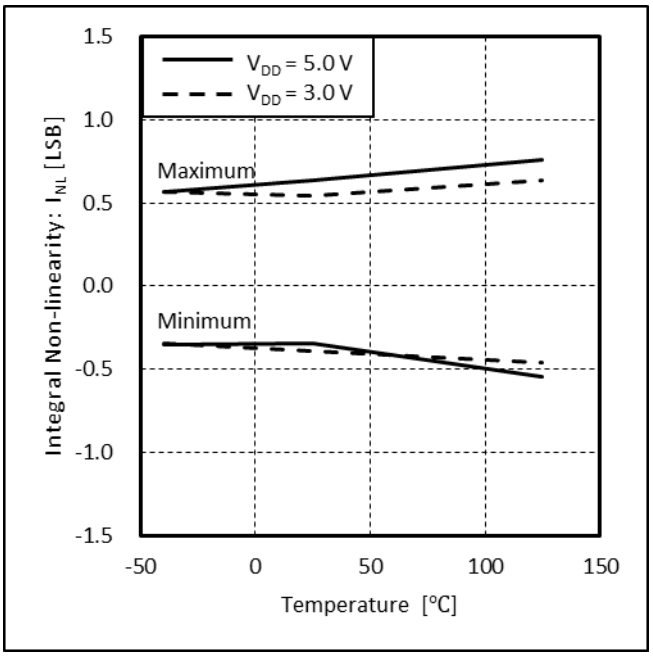


Figure 9. Integral Non-linearity vs Temperature

Typical Performance Curves - continued

(Reference Data)

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V

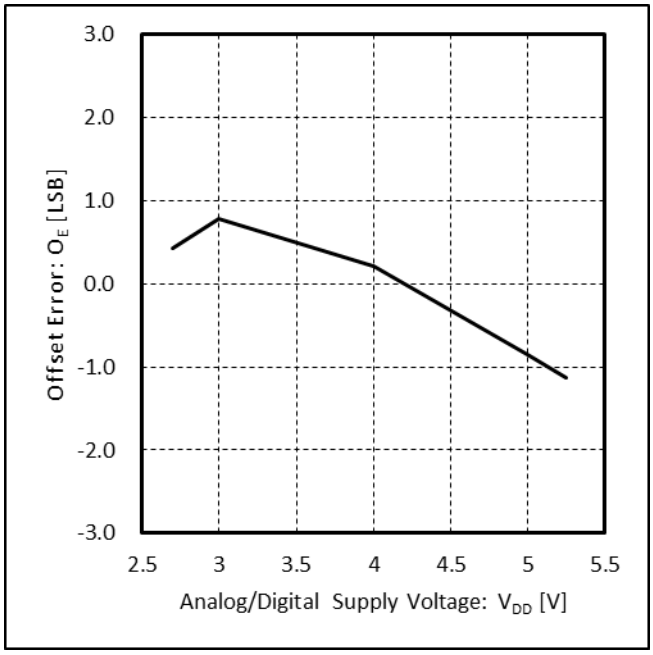


Figure 10. Offset Error vs Analog/Digital Supply Voltage

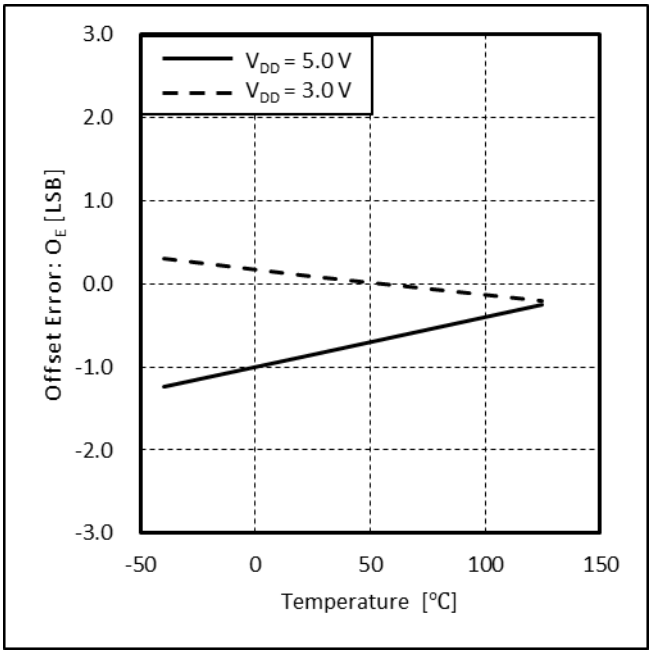


Figure 11. Offset Error vs Temperature

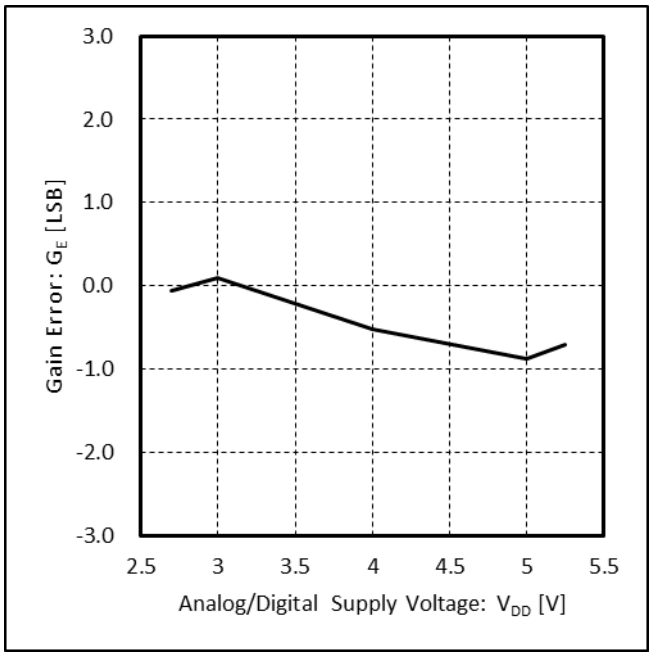


Figure 12. Gain Error vs Analog/Digital Supply Voltage

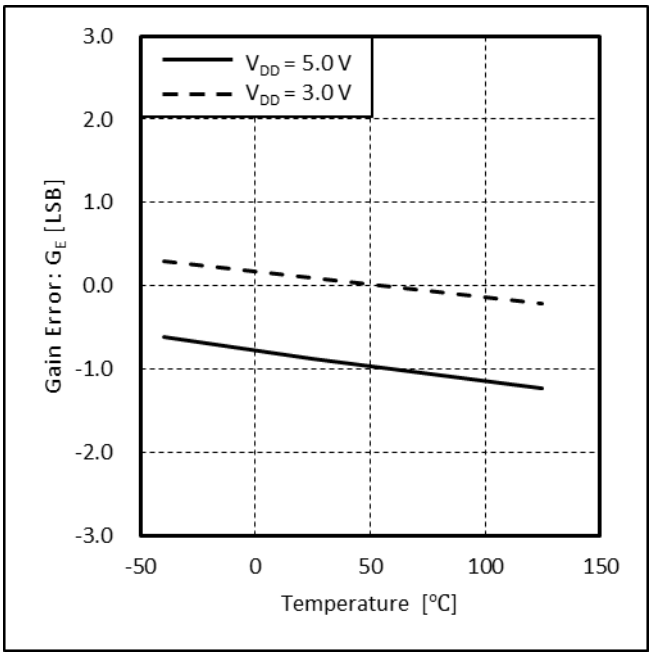


Figure 13. Gain Error vs Temperature

Typical Performance Curves - continued

(Reference Data)

Unless otherwise specified, Ta = -40 °C to +125 °C (typical: Ta = 25 °C), V_{DD} = 2.7 V to 5.25 V, V_{IOVDD} = 1.65 V to 5.25 V

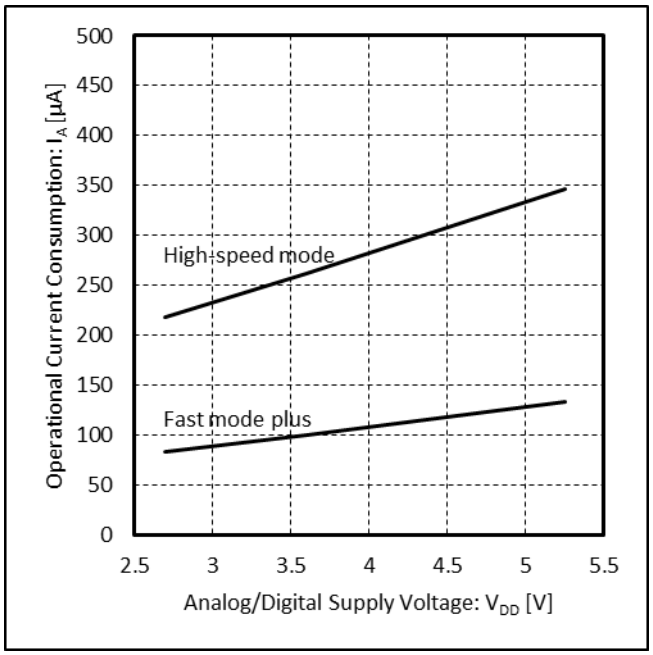


Figure 14. Operational Current Consumption vs Analog/Digital Supply Voltage

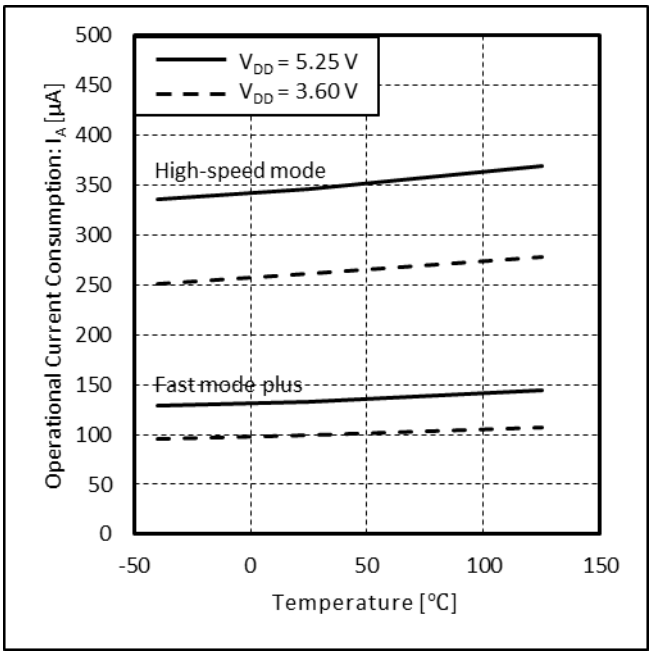


Figure 15.
Operational Current Consumption vs Temperature

I²C Communication Format

Protocol Features

Item	Send Data
General Call	0x00
General Call + Software Reset	0x00 + 0x06
General Call + Address Update	0x00 + 0x04
High-speed Mode Configuration	0x08 or 0x09 or 0x0A or 0x0B or 0x0C or 0x0D or 0x0E or 0x0F
Read ADC at Manual or Auto Sequence Mode	7-bit Target Address, 1 (Read)
Write or Read Register	7-bit Target Address, 1 (Write) + OPCODE

OPCODE for Commands

OPCODE	Command Description
0x10	Single Register Read
0x08	Single Register Write
0x18	Set bit
0x20	Clear bit
0x30	Reading a Continuous Block of Register
0x28	Writing a Continuous Block of Register

I²C Frame Acronyms

OPCODE	Command Description
S	Start condition for the I²C frame
Sr	Restart condition for the I²C frame
P	Stop condition for the I²C frame
A	ACK (Low)
R	Read bit (High)
W	Write bit (Low)

1. Reading ADC Result

In the Reading ADC result sequence, you can read the ADC results of Manual mode and Auto Sequence mode. When sending this sequence, insert t_{CONV} (SCL = Low) immediately before the data.

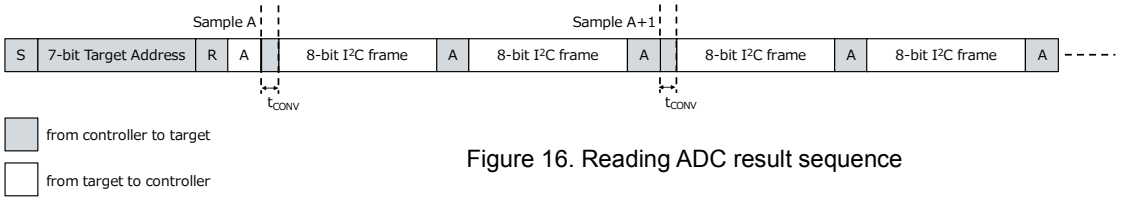


Figure 16. Reading ADC result sequence

I²C Communication Format - continued

2. Single Register Read

In the Single Register Read sequence, you can read 1 byte register data.

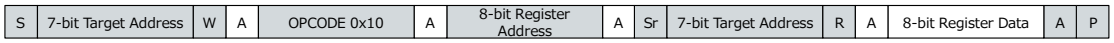


Figure 17. Single Register Read sequence

3. Single Register Write

In Single Register Write sequence, you can write 1 byte data to a register.

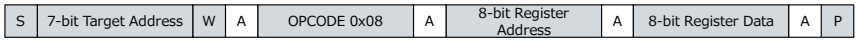


Figure 18. Single Register Write sequence

4. Set bit

In Set bit sequence, you can write 1 to the specified bit and the other bits can hold their values.
For example, if the data in the register is 0xF0 (0b11110000) and 0xCC (0b11001100) is specified, the data in the register is updated to 0xFC (0b11111100).

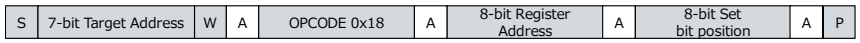


Figure 19. Set bit sequence

5. Clear bit

In Clear bit sequence, you can write 0 to the specified bit and the other bits can hold their values.
For example, if the data in the register is 0xF0 (0b11110000) and 0xCC (0b11001100) is specified, the data in the register is updated to 0x30 (0b00110000).

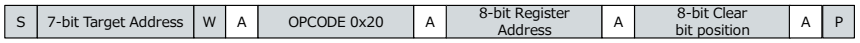


Figure 20. Clear bit sequence

6. Reading a Continuous Block of Register

In Reading a Continuous Block of Register sequence, you can read data from registers at continuous addresses in order.
In this case, the first data to be read is the data at the specified address, and the next data is the data in the register next one.

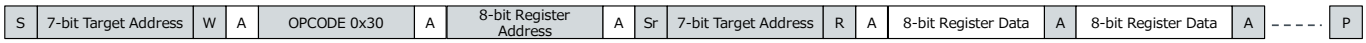


Figure 21. Reading a Continuous Block of Register sequence

7. Writing a Continuous Block of Register

In Writing a Continuous Block of Register sequence, you can write data to registers at continuous addresses in order.
In this case, the first data to be written is written to the specified address, and the next data is written to the register next one.

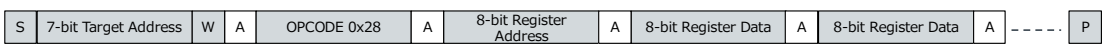


Figure 22. Writing a Continuous Block of Register sequence

I²C Target Address Selector

You can select the I²C target address according to the ADDR pin setting.
The I²C target address is updated by either power-on, software reset by the RST register, or address update by General Call.
I²C target addresses are shown in Figure 23 and Table 1.

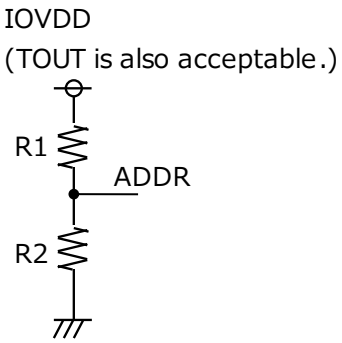


Figure 23. ADDR pin input circuit

Table 1. I²C Address Selection

R1*(Note 7)*	R2*(Note 7)*	I²C Address
0 Ω	OPEN	001 0111
100 kΩ	OPEN	001 0100
OPEN	0 Ω	001 0000
OPEN	100 kΩ	001 0011

(Note 7) Tolerance for R1, R2 ≤ ±5 %.

Register Map(Note 8)

Address	Register Name	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	SYSTEM_STATUS	R/W	0x81	RSVD	SEQ_STATUS	I2C_SPEED	0	0	0	0	BOR
0x01	GENERAL_CFG	R/W	0x00	0	0	STATS_EN	DWC_EN	0	0	0	RST
0x02	DATA_CFG	R/W	0x00	FIX_PAT	0	APPEND_STATUS [1:0]		0	0	0	0
0x03	BUSY_CFG	R/W	0x00	BUSY_TIME [1:0]		0	0	0	0	0	0
0x04	OPMODE_CFG	R/W	0x00	0	CONV_MODE [1:0]		0	0	0	CLK_DIV [1:0]	
0x05	PIN_CFG	R/W	0x00	PIN_CFG [7:0]							
0x0B	GPO_VALUE	R/W	0x00	GPO_VALUE [7:0]							
0x10	SEQUENCE_CFG	R/W	0x00	0	0	0	SEQ_START	0	0	SEQ_MODE [1:0]	
0x11	MANUAL_CH_SEL	R/W	0x00	0	0	0	0	MANUAL_CHID [3:0]			
0x12	AUTO_SEQ_CH_SEL	R/W	0x00	AUTO_SEQ_CH_SEL [7:0]							
0x14	ALERT_CH_SEL	R/W	0x00	ALERT_CH_SEL [7:0]							
0x18	EVENT_FLAG	R	0x00	EVENT_FLAG [7:0]							
0x1A	EVENT_HIGH_FLAG	R/W	0x00	EVENT_HIGH_FLAG [7:0]							
0x1C	EVENT_LOW_FLAG	R/W	0x00	EVENT_LOW_FLAG [7:0]							
0x1E	EVENT_RGN	R/W	0x00	EVENT_RGN [7:0]							
0x20	HYSTERESIS_CH0	R/W	0xF0	HIGH_THRESHOLD_CH0 [3:0]				HYSTERESIS_CH0 [3:0]			
0x21	HIGH_TH_CH0	R/W	0xFF	HIGH_THRESHOLD_CH0 [11:4]							
0x22	EVENT_COUNT_CH0	R/W	0x00	LOW_THRESHOLD_CH0 [3:0]				EVENT_COUNT_CH0 [3:0]			
0x23	LOW_TH_CH0	R/W	0x00	LOW_THRESHOLD_CH0 [11:4]							
0x24	HYSTERESIS_CH1	R/W	0xF0	HIGH_THRESHOLD_CH1 [3:0]				HYSTERESIS_CH1 [3:0]			
0x25	HIGH_TH_CH1	R/W	0xFF	HIGH_THRESHOLD_CH1 [11:4]							
0x26	EVENT_COUNT_CH1	R/W	0x00	LOW_THRESHOLD_CH1 [3:0]				EVENT_COUNT_CH1 [3:0]			
0x27	LOW_TH_CH1	R/W	0x00	LOW_THRESHOLD_CH1 [11:4]							
0x28	HYSTERESIS_CH2	R/W	0xF0	HIGH_THRESHOLD_CH2 [3:0]				HYSTERESIS_CH2 [3:0]			
0x29	HIGH_TH_CH2	R/W	0xFF	HIGH_THRESHOLD_CH2 [11:4]							
0x2A	EVENT_COUNT_CH2	R/W	0x00	LOW_THRESHOLD_CH2 [3:0]				EVENT_COUNT_CH2 [3:0]			
0x2B	LOW_TH_CH2	R/W	0x00	LOW_THRESHOLD_CH2 [11:4]							
0x2C	HYSTERESIS_CH3	R/W	0xF0	HIGH_THRESHOLD_CH3 [3:0]				HYSTERESIS_CH3 [3:0]			
0x2D	HIGH_TH_CH3	R/W	0xFF	HIGH_THRESHOLD_CH3 [11:4]							
0x2E	EVENT_COUNT_CH3	R/W	0x00	LOW_THRESHOLD_CH3 [3:0]				EVENT_COUNT_CH3 [3:0]			
0x2F	LOW_TH_CH3	R/W	0x00	LOW_THRESHOLD_CH3 [11:4]							

(Note 8) Do not write any commands to other addresses except above. Do not write '1' to the fields in which value is '0' in above table.

Register Map(Note 8) **– continued**

Address	Register Name	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x30	HYSTERESIS_CH4	R/W	0xF0	HIGH_THRESHOLD_CH4 [3:0]				HYSTERESIS_CH4 [3:0]			
0x31	HIGH_TH_CH4	R/W	0xFF	HIGH_THRESHOLD_CH4 [11:4]							
0x32	EVENT_COUNT_CH4	R/W	0x00	LOW_THRESHOLD_CH4 [3:0]				EVENT_COUNT_CH4 [3:0]			
0x33	LOW_TH_CH4	R/W	0x00	LOW_THRESHOLD_CH4 [11:4]							
0x34	HYSTERESIS_CH5	R/W	0xF0	HIGH_THRESHOLD_CH5 [3:0]				HYSTERESIS_CH5 [3:0]			
0x35	HIGH_TH_CH5	R/W	0xFF	HIGH_THRESHOLD_CH5 [11:4]							
0x36	EVENT_COUNT_CH5	R/W	0x00	LOW_THRESHOLD_CH5 [3:0]				EVENT_COUNT_CH5 [3:0]			
0x37	LOW_TH_CH5	R/W	0x00	LOW_THRESHOLD_CH5 [11:4]							
0x38	HYSTERESIS_CH6	R/W	0xF0	HIGH_THRESHOLD_CH6 [3:0]				HYSTERESIS_CH6 [3:0]			
0x39	HIGH_TH_CH6	R/W	0xFF	HIGH_THRESHOLD_CH6 [11:4]							
0x3A	EVENT_COUNT_CH6	R/W	0x00	LOW_THRESHOLD_CH6 [3:0]				EVENT_COUNT_CH6 [3:0]			
0x3B	LOW_TH_CH6	R/W	0x00	LOW_THRESHOLD_CH6 [11:4]							
0x3C	HYSTERESIS_CH7	R/W	0xF0	HIGH_THRESHOLD_CH7 [3:0]				HYSTERESIS_CH7 [3:0]			
0x3D	HIGH_TH_CH7	R/W	0xFF	HIGH_THRESHOLD_CH7 [11:4]							
0x3E	EVENT_COUNT_CH7	R/W	0x00	LOW_THRESHOLD_CH7 [3:0]				EVENT_COUNT_CH7 [3:0]			
0x3F	LOW_TH_CH7	R/W	0x00	LOW_THRESHOLD_CH7 [11:4]							
0xA0	RECENT_CH0_LSB	R	0x00	LAST_VALUE_CH0 [3:0]				0	0	0	0
0xA1	RECENT_CH0_MSB	R	0x00	LAST_VALUE_CH0 [11:4]							
0xA2	RECENT_CH1_LSB	R	0x00	LAST_VALUE_CH1 [3:0]				0	0	0	0
0xA3	RECENT_CH1_MSB	R	0x00	LAST_VALUE_CH1 [11:4]							
0xA4	RECENT_CH2_LSB	R	0x00	LAST_VALUE_CH2 [3:0]				0	0	0	0
0xA5	RECENT_CH2_MSB	R	0x00	LAST_VALUE_CH2 [11:4]							
0xA6	RECENT_CH3_LSB	R	0x00	LAST_VALUE_CH3 [3:0]				0	0	0	0
0xA7	RECENT_CH3_MSB	R	0x00	LAST_VALUE_CH3 [11:4]							
0xA8	RECENT_CH4_LSB	R	0x00	LAST_VALUE_CH4 [3:0]				0	0	0	0
0xA9	RECENT_CH4_MSB	R	0x00	LAST_VALUE_CH4 [11:4]							
0xAA	RECENT_CH5_LSB	R	0x00	LAST_VALUE_CH5 [3:0]				0	0	0	0
0xAB	RECENT_CH5_MSB	R	0x00	LAST_VALUE_CH5 [11:4]							
0xAC	RECENT_CH6_LSB	R	0x00	LAST_VALUE_CH6 [3:0]				0	0	0	0
0xAD	RECENT_CH6_MSB	R	0x00	LAST_VALUE_CH6 [11:4]							
0xAE	RECENT_CH7_LSB	R	0x00	LAST_VALUE_CH7 [3:0]				0	0	0	0
0xAF	RECENT_CH7_MSB	R	0x00	LAST_VALUE_CH7 [11:4]							

(Note 8) Do not write any commands to other addresses except above. Do not write '1' to the fields in which value is '0' in above table.

Register Map – continued

SYSTEM_STATUS

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	R/W	0x81	RSVD	SEQ_ STATUS	I2C_SPEED	0	0	0	0	BOR

RSVD (Read Only)
Fixed value, always 1

SEQ_STATUS (Read Only)
Status of the Channel Sequencer. When two or more CH are selected in AUTO_SEQ_CH_SEL and SEQ_START = 1, Channel Sequencer is in progress.
0: stop
1: in progress

I2C_SPEED (Read Only)
Status of I^2C
0: Except High-speed Mode
1: High-speed Mode

BOR
Brown out reset indicator. Writing 1 will set it to 0.
0: BOR is not detected.
1: BOR is detected.

GENERAL_CFG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x01	R/W	0x00	0	0	STATS_EN	DWC_EN	0	0	0	RST

STATS_EN
Enable LAST_VALUE update in Address A0 to AF
0: Do not update LAST_VALUE
1: Update LAST_VALUE

DWC_EN
Enable Digital Window Comparator
0: Disable
1: Enable

RST
Software Reset
0: Normal operation
1: Execute Software Reset and update I^2C address.

DATA_CFG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	R/W	0x00	FIX_PAT	0	APPEND_STATUS [1:0]		0	0	0	0

FIX_PAT
Fix the ADC result to 0xA5A.
0: Disable
1: Enable

APPEND_STATUS
Output data format in the Reading ADC result sequence
00: 12 bit Data output + 4'b0000
01: 12 bit Data output + 4 bit Channel ID
10: 12 bit Data output + 3'b100 + ALERT
11: Reserved

Register Map – continued

BUSY_CFG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	R/W	0x00	BUSY_TIME [1:0]		0	0	0	0	0	0

BUSY_TIME
AD conversion time
00: 1.2 µs
01: Reserved
10: Reserved
11: 6.0 µs

OPMODE_CFG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	R/W	0x00	0	CONV_MODE [1:0]		0	0	0	CLK_DIV [1:0]	

CONV_MODE
Select AD conversion mode
00: Manual Mode or Auto Sequence Mode
01: Autonomous Mode
10: Reserved
11: Reserved

CLK_DIV
Select interval time at Autonomous Mode
00: 0.75 ms
01: 1.5 ms
10: 3 ms
11: 6 ms

PIN_CFG

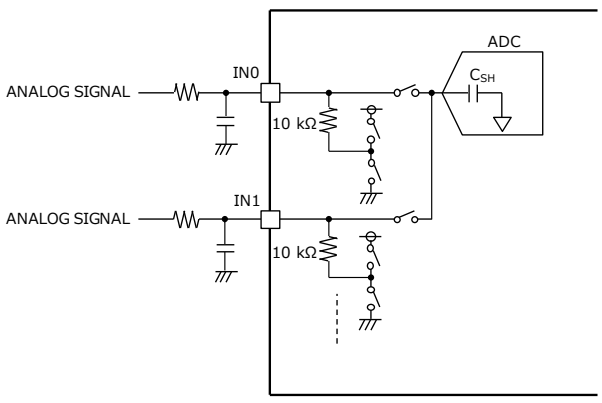
Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x05	R/W	0x00	PIN_CFG [7:0]							

PIN_CFG
Enable GPO for IN0 to IN7
Bit0 corresponds to IN0, Bit7 corresponds to IN7
0: Disable
1: Enable

GPO_VALUE

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0B	R/W	0x00	GPO_VALUE [7:0]							

GPO_VALUE
Select GPO output polarity for IN0 to IN7
Bit0 corresponds to IN0, Bit7 corresponds to IN7
0: Low
1: High



Register Map – continued

SEQUENCE_CFG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	R/W	0x00	0	0	0	SEQ_START	0	0	SEQ_MODE [1:0]	

SEQ_START
Start/Stop of Channel Sequencer
0: Stop
1: Start

SEQ_MODE
Select Sequence Mode
00: Manual Mode, select channel in MANUAL_CHID
01: Auto Sequence Mode or Autonomous Mode, select channel in AUTO_SEQ_CH_SEL
10: Reserved
11: Reserved

MANUAL_CH_SEL

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x11	R/W	0x00	0	0	0	0	MANUAL_CHID [3:0]			

MANUAL_CHID
Select channel at Manual Mode
0000: IN0
0001: IN1
0010: IN2
0011: IN3
0100: IN4
0101: IN5
0110: IN6
0111: IN7
1xxx: Reserved

AUTO_SEQ_CH_SEL

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x12	R/W	0x00	AUTO_SEQ_CH_SEL [7:0]							

AUTO_SEQ_CH_SEL
Select channel at Auto Sequence Mode and Autonomous Mode
Execute AD conversion in order by the selected channel.
Bit0 corresponds to IN0, Bit7 corresponds to IN7
0: Not selected
1: Selected

Register Map – continued

ALERT_CH_SEL

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	R/W	0x00	ALERT_CH_SEL [7:0]							

ALERT_CH_SEL

Select channel for ALERT flag to be output on ALERT pin, Bit0 corresponds to IN0, Bit7 corresponds to IN7

0: Not selected

1: Selected

EVENT_FLAG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x18	R	0x00	EVENT_FLAG [7:0]							

EVENT_FLAG

Indicate ALERT flag for each channel, Bit0 corresponds to IN0, Bit7 corresponds to IN7

0: Not flagged

1: Flagged

EVENT_HIGH_FLAG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1A	R/W	0x00	EVENT_HIGH_FLAG [7:0]							

EVENT_HIGH_FLAG

Indicate ALERT High flag for each channel. Writing 1 will clear the flag and set it to 0.

Bit0 corresponds to IN0, Bit7 corresponds to IN7

0: Not flagged

1: Flagged

EVENT_LOW_FLAG

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1C	R/W	0x00	EVENT_LOW_FLAG [7:0]							

EVENT_LOW_FLAG

Indicate ALERT Low flag for each channel. Writing 1 will clear the flag and set it to 0.

Bit0 corresponds to IN0, Bit7 corresponds to IN7

0: Not flagged

1: Flagged

EVENT_RGN

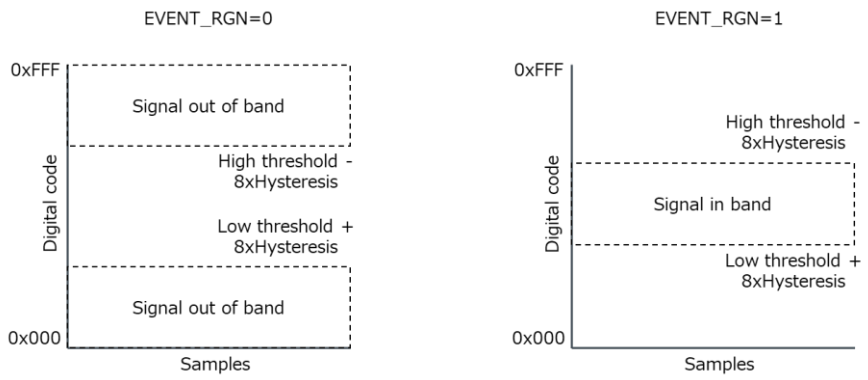
Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E	R/W	0x00	EVENT_RGN [7:0]							

EVENT_RGN

Select a region for Digital Window Comparator, Bit0 corresponds to IN0, Bit7 corresponds to IN7

0: Detecting outside

1: Detecting inside



Register Map – continued

HYSTERESIS_CH0, HIGH_TH_CH0

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x20	R/W	0xF0	HIGH_THRESHOLD_CH0 [3:0]				HYSTERESIS_CH0 [3:0]			
0x21	R/W	0xFF	HIGH_THRESHOLD_CH0 [11:4]							

EVENT_COUNT_CH0, LOW_TH_ CH0

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x22	R/W	0x00	LOW_THRESHOLD_CH0 [3:0]				EVENT_COUNT_CH0 [3:0]			
0x23	R/W	0x00	LOW_THRESHOLD_CH0 [11:4]							

HIGH_THRESHOLD_CH0
High threshold for CH0

HYSTERESIS_CH0
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH0
Low threshold for CH0

EVENT_COUNT_CH0
Configure the number of times the Event Counter for CH0.
Flagged when the AD conversion result exceeds the threshold n+1 times.

HYSTERESIS_CH1, HIGH_TH_CH1

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x24	R/W	0xF0	HIGH_THRESHOLD_CH1 [3:0]				HYSTERESIS_CH1 [3:0]			
0x25	R/W	0xFF	HIGH_THRESHOLD_CH1 [11:4]							

EVENT_COUNT_CH1, LOW_TH_ CH1

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x26	R/W	0x00	LOW_THRESHOLD_CH1 [3:0]				EVENT_COUNT_CH1 [3:0]			
0x27	R/W	0x00	LOW_THRESHOLD_CH1 [11:4]							

HIGH_THRESHOLD_CH1
High threshold for CH1

HYSTERESIS_CH1
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH1
Low threshold for CH1

EVENT_COUNT_CH1
Configure the number of times the Event Counter for CH1.
Flagged when the AD conversion result exceeds the threshold n+1 times.

Register Map – continued

HYSTERESIS_CH2, HIGH_TH_CH2

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x28	R/W	0xF0	HIGH_THRESHOLD_CH2 [3:0]				HYSTERESIS_CH2 [3:0]			
0x29	R/W	0xFF	HIGH_THRESHOLD_CH2 [11:4]							

EVENT_COUNT_CH2, LOW_TH_ CH2

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2A	R/W	0x00	LOW_THRESHOLD_CH2 [3:0]				EVENT_COUNT_CH2 [3:0]			
0x2B	R/W	0x00	LOW_THRESHOLD_CH2 [11:4]							

HIGH_THRESHOLD_CH2
High threshold for CH2

HYSTERESIS_CH2
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH2
Low threshold for CH2

EVENT_COUNT_CH2
Configure the number of times the Event Counter for CH2.
Flagged when the AD conversion result exceeds the threshold n+1 times.

HYSTERESIS_CH3, HIGH_TH_CH3

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2C	R/W	0xF0	HIGH_THRESHOLD_CH3 [3:0]				HYSTERESIS_CH3 [3:0]			
0x2D	R/W	0xFF	HIGH_THRESHOLD_CH3 [11:4]							

EVENT_COUNT_CH3, LOW_TH_ CH3

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x2E	R/W	0x00	LOW_THRESHOLD_CH3 [3:0]				EVENT_COUNT_CH3 [3:0]			
0x2F	R/W	0x00	LOW_THRESHOLD_CH3 [11:4]							

HIGH_THRESHOLD_CH3
High threshold for CH3

HYSTERESIS_CH3
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH3
Low threshold for CH3

EVENT_COUNT_CH3
Configure the number of times the Event Counter for CH3.
Flagged when the AD conversion result exceeds the threshold n+1 times.

Register Map – continued

HYSTERESIS_CH4, HIGH_TH_CH4

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x30	R/W	0xF0	HIGH_THRESHOLD_CH4 [3:0]				HYSTERESIS_CH4 [3:0]			
0x31	R/W	0xFF	HIGH_THRESHOLD_CH4 [11:4]							

EVENT_COUNT_CH4, LOW_TH_ CH4

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x32	R/W	0x00	LOW_THRESHOLD_CH4 [3:0]				EVENT_COUNT_CH4 [3:0]			
0x33	R/W	0x00	LOW_THRESHOLD_CH4 [11:4]							

HIGH_THRESHOLD_CH4
High threshold for CH4

HYSTERESIS_CH4
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH4
Low threshold for CH4

EVENT_COUNT_CH4
Configure the number of times the Event Counter for CH4.
Flagged when the AD conversion result exceeds the threshold n+1 times.

HYSTERESIS_CH5, HIGH_TH_CH5

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x34	R/W	0xF0	HIGH_THRESHOLD_CH5 [3:0]				HYSTERESIS_CH5 [3:0]			
0x35	R/W	0xFF	HIGH_THRESHOLD_CH5 [11:4]							

EVENT_COUNT_CH5, LOW_TH_ CH5

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x36	R/W	0x00	LOW_THRESHOLD_CH5 [3:0]				EVENT_COUNT_CH5 [3:0]			
0x37	R/W	0x00	LOW_THRESHOLD_CH5 [11:4]							

HIGH_THRESHOLD_CH5
High threshold for CH5

HYSTERESIS_CH5
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH5
Low threshold for CH5

EVENT_COUNT_CH5
Configure the number of times the Event Counter for CH5.
Flagged when the AD conversion result exceeds the threshold n+1 times.

Register Map – continued

HYSTERESIS_CH6, HIGH_TH_CH6

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x38	R/W	0xF0	HIGH_THRESHOLD_CH6 [3:0]				HYSTERESIS_CH6 [3:0]			
0x39	R/W	0xFF	HIGH_THRESHOLD_CH6 [11:4]							

EVENT_COUNT_CH6, LOW_TH_ CH6

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3A	R/W	0x00	LOW_THRESHOLD_CH6 [3:0]				EVENT_COUNT_CH6 [3:0]			
0x3B	R/W	0x00	LOW_THRESHOLD_CH6 [11:4]							

HIGH_THRESHOLD_CH6
High threshold for CH6

HYSTERESIS_CH6
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH6
Low threshold for CH6

EVENT_COUNT_CH6
Configure the number of times the Event Counter for CH6.
Flagged when the AD conversion result exceeds the threshold n+1 times.

HYSTERESIS_CH7, HIGH_TH_CH7

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3C	R/W	0xF0	HIGH_THRESHOLD_CH7 [3:0]				HYSTERESIS_CH7 [3:0]			
0x3D	R/W	0xFF	HIGH_THRESHOLD_CH7 [11:4]							

EVENT_COUNT_CH7, LOW_TH_ CH7

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x3E	R/W	0x00	LOW_THRESHOLD_CH7 [3:0]				EVENT_COUNT_CH7 [3:0]			
0x3F	R/W	0x00	LOW_THRESHOLD_CH7 [11:4]							

HIGH_THRESHOLD_CH7
High threshold for CH7

HYSTERESIS_CH7
Hysteresis for high and low thresholds. Apply a 4 bit setting with a 3 bit left shift.

LOW_THRESHOLD_CH7
Low threshold for CH7

EVENT_COUNT_CH7
Configure the number of times the Event Counter for CH7.
Flagged when the AD conversion result exceeds the threshold n+1 times.

Register Map – continued

RECENT_CH0_LSB, RECENT_CH0_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA0	R	0x00	LAST_VALUE_CH0 [3:0]				0	0	0	0
0xA1	R	0x00	LAST_VALUE_CH0 [11:4]							

LAST_VALUE_CH0
Recent ADC result at CH0

RECENT_CH1_LSB, RECENT_CH1_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA2	R	0x00	LAST_VALUE_CH1 [3:0]				0	0	0	0
0xA3	R	0x00	LAST_VALUE_CH1 [11:4]							

LAST_VALUE_CH1
Recent ADC result at CH1

RECENT_CH2_LSB, RECENT_CH2_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA4	R	0x00	LAST_VALUE_CH2 [3:0]				0	0	0	0
0xA5	R	0x00	LAST_VALUE_CH2 [11:4]							

LAST_VALUE_CH2
Recent ADC result at CH2

RECENT_CH3_LSB, RECENT_CH3_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA6	R	0x00	LAST_VALUE_CH3 [3:0]				0	0	0	0
0xA7	R	0x00	LAST_VALUE_CH3 [11:4]							

LAST_VALUE_CH3
Recent ADC result at CH3

Register Map – continued

RECENT_CH4_LSB, RECENT_CH4_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xA8	R	0x00	LAST_VALUE_CH4 [3:0]				0	0	0	0
0xA9	R	0x00	LAST_VALUE_CH4 [11:4]							

LAST_VALUE_CH4
Recent ADC result at CH4

RECENT_CH5_LSB, RECENT_CH5_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xAA	R	0x00	LAST_VALUE_CH5 [3:0]				0	0	0	0
0xAB	R	0x00	LAST_VALUE_CH5 [11:4]							

LAST_VALUE_CH5
Recent ADC result at CH5

RECENT_CH6_LSB, RECENT_CH6_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xAC	R	0x00	LAST_VALUE_CH6 [3:0]				0	0	0	0
0xAD	R	0x00	LAST_VALUE_CH6 [11:4]							

LAST_VALUE_CH6
Recent ADC result at CH6

RECENT_CH7_LSB, RECENT_CH7_MSB

Address	R/W	Initial	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xAE	R	0x00	LAST_VALUE_CH7 [3:0]				0	0	0	0
0xAF	R	0x00	LAST_VALUE_CH7 [11:4]							

LAST_VALUE_CH7
Recent ADC result at CH7

Control Sequence

1 Power-up Sequence

When VDD and IOVDD are supplied from separate power supplies, the power supply start-up order is arbitrary. Communication via I²C should be performed after t_{PU} after all power has been supplied.

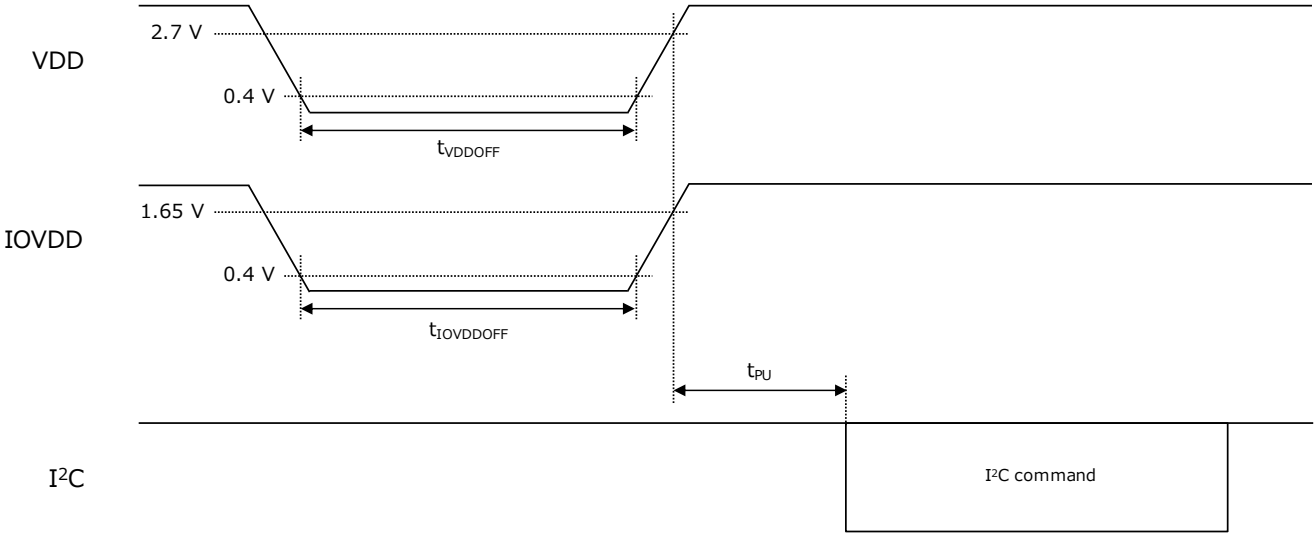


Figure 24. Power-up sequence

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
VDD off time	t_{VDDOFF}	1	-	-	ms	
IOVDD off time	$t_{IOVDDOFF}$	1	-	-	ms	
I²C command available time from Power-up	t_{PU}	0.1	-	-	ms	

Control Sequence - continued

2 AD Conversion

There are three AD conversion modes:

Manual Mode	Only one channel can be selected from IN0 to IN7. Each time the Reading ADC result sequence is transmitted, AD conversion is performed.
Auto Sequence Mode	Multiple channels can be selected from IN0 to IN7. Each time the Reading ADC result sequence is transmitted, AD conversion is performed on the next channel.
Autonomous Mode	One or multiple channels can be selected from IN0 to IN7. Each interval, AD conversion is automatically performed without Reading ADC result sequence.

2.1 Manual Mode

In this mode, each time the Reading ADC result sequence is transmitted, AD conversion is performed on only one selected channel from IN0 to IN7.
To change the channel, set it again in the MANUAL_CHID register.

Table 2. Manual Mode measurement flow example

	Register Name	Address	Data
Step1	CONV_MODE SEQ_MODE	0x04 0x10	0x00 0x00
Step2	MANUAL_CHID	0x11	0x00: IN0 Selected 0x01: IN1 Selected 0x02: IN2 Selected 0x03: IN3 Selected 0x04: IN4 Selected 0x05: IN5 Selected 0x06: IN6 Selected 0x07: IN7 Selected
Step3	Target Address + R (High)		Read

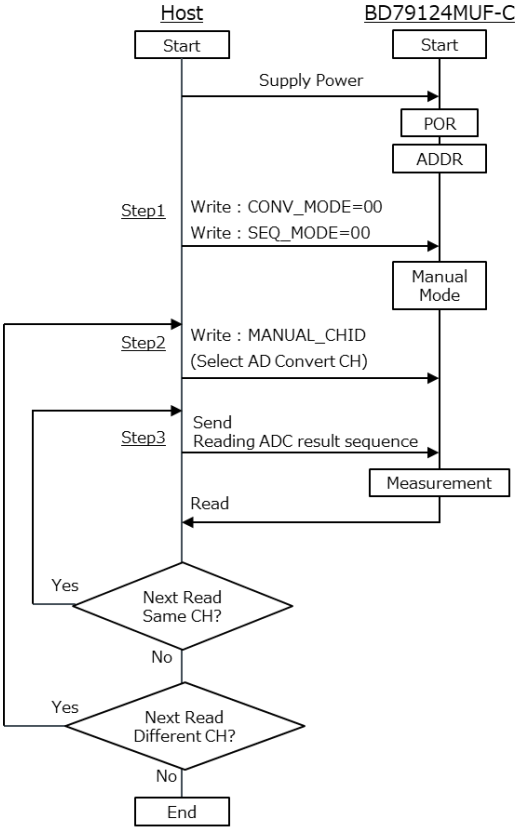


Figure 25.
Manual Mode measurement flow example

The Reading ADC result sequence is I²C commands as shown in the Figure 26.
The ADC result is MSB first, and the 4 bits after that are fixed to 0.
By setting the APPEND_STATUS register in the DATA_CFG register, you can output CHID or flag in the back 4 bits.

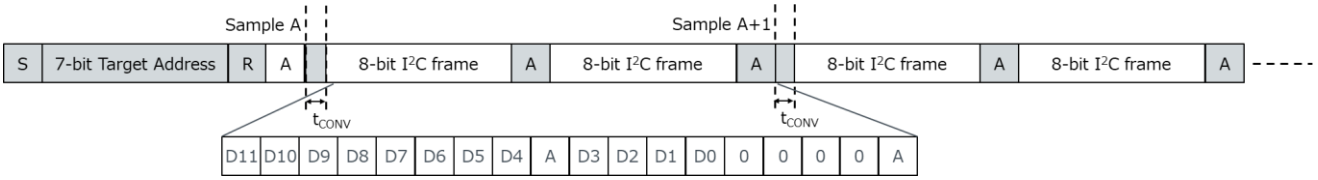


Figure 26. Reading ADC result sequence

2 AD Conversion – continued

2.2 Auto Sequence Mode

In this mode, each time the Reading ADC result sequence is transmitted, AD conversion is performed on the selected channels from IN0 to IN7 in order. When you change the selected channels, set SEQ_START register to 0 first, then reconfigure AUTO_SEQ_CH_SEL register, then set SEQ_START register to 1. Optionally, by setting the APPEND_STATUS register, you can know which CH has been AD converted.

Table 3. Auto Sequence Mode measurement flow example

	Register Name	Address	Data
Step1	CONV_MODE SEQ_MODE	0x04 0x10	0x00 0x01
Step2	AUTO_SEQ_CH_SEL	0x12	SELECT
(Option)	APPEND_STATUS	0x02	0x00: OFF 0x10: ON
Step3	SEQ_START	0x10	0x11
Step4	Target Address + R(High)		Read
Step5	Next Read Different CH SEL? = Yes		
	SEQ_START	0x10	0x10

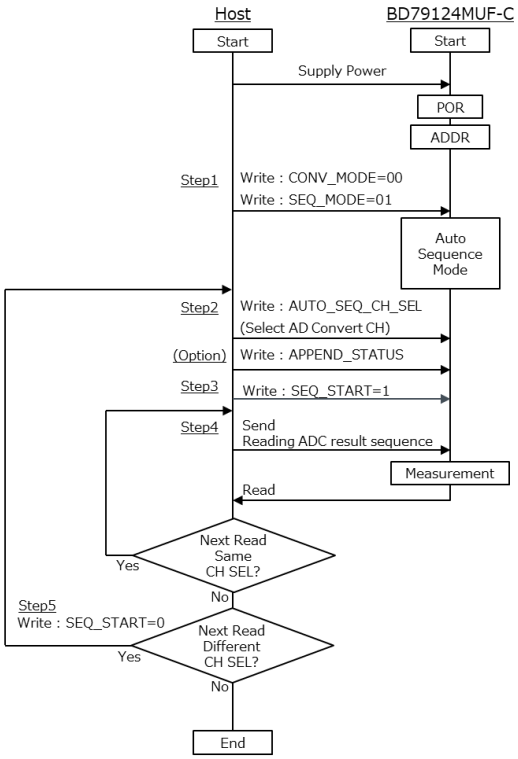


Figure 27.
Auto Sequence Mode measurement flow example

2.2.1 AUTO_SEQ_CH_SEL

For example, if the value of AUTO_SEQ_CH_SEL register is set to 0x96, i.e., CH1, 2, 4 and 7 are selected, after CH1 is AD converted and the result is read, CH2 is going to be AD converted. Next to CH7 AD conversion is CH1.

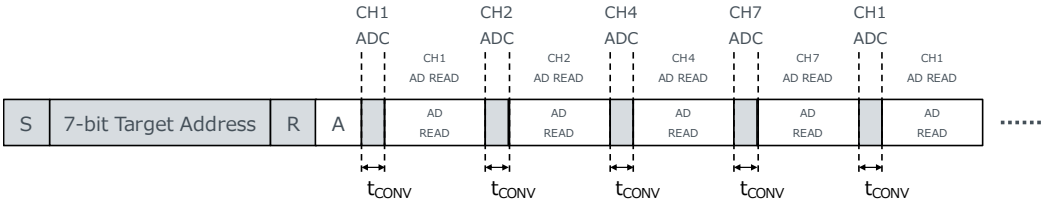


Figure 28. Auto Sequence Mode operation example

2.2.2 APPEND_STATUS

For example, if the value of APPEND_STATUS register is set to 0b10 and CH4 is AD converted, the 12 bit AD conversion result and 0b0100 which indicates the CH4 is converted are output. If it is CH0 that is AD converted, the output is 0b0000, and if it is CH7, the output is 0b0111.

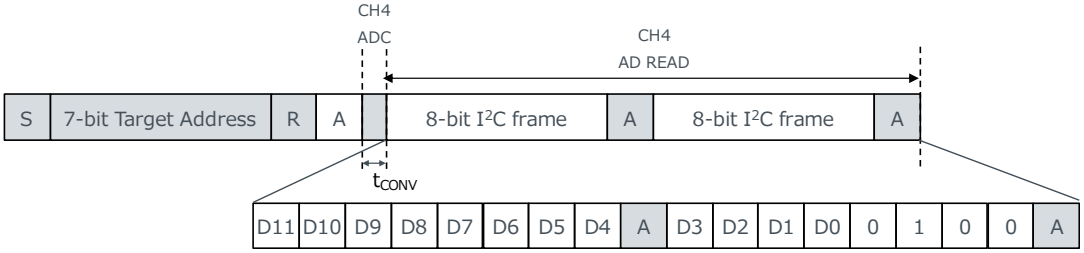


Figure 29. APPEND_STATUS output example

2 AD Conversion – continued

2.3 Autonomous Mode

In this mode, each interval, AD conversion is automatically performed without Reading ADC result sequence.
The AD conversion results are stored in LAST_VALUE_CHx (x = 0 to 7) register, If the STATS_EN register is set to 0, the value will not be updated.
If you use ALERT function (DWC, Digital Window Comparator), the ALERT pin outputs low level if the result exceeds threshold. ALERT function is available in Manual Mode and Auto Sequence Mode, too.

Table 4. Autonomous Mode measurement flow example

	Register Name	Address	Data
Step1	SEQ_MODE	0x10	0x01
Step2	AUTO_SEQ_CH_SEL	0x12	SELECT
Step3	CONV_MODE STATS_EN	0x04 0x01	0x01 0x20
Step4	DWC_EN SEQ_START	0x01 0x10	0x30 0x11
(Option)	EVENT_FLAG EVENT_HIGH_FLAG EVENT_LOW_FLAG	0x18 0x1A 0x1C	Read Only Read or Clear Read or Clear
(Option)	LAST_VALUE_CHx	0xA0 – 0xAF	Read Only
Step5	Stop Measurement? = Yes		
	SEQ_START DWC_EN	0x10 0x01	0x01 0x20

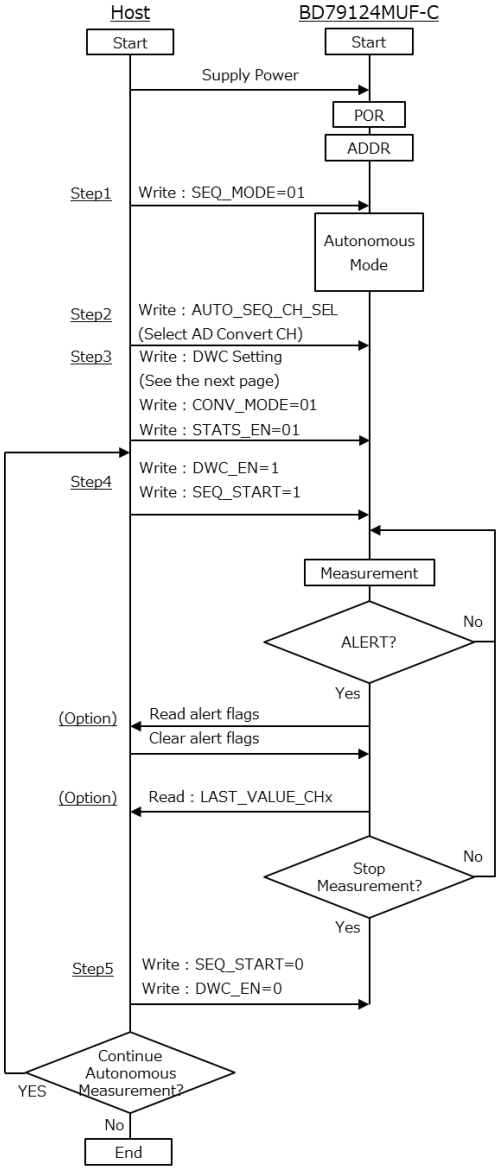


Figure 30.
Autonomous Mode measurement flow example

Control Sequence - continued

3 ALERT Function

3.1 Summary

Depending on the AD conversion result, the ALERT pin can output an interrupt.
The ALERT pin is an open drain (Low active) output. When using this pin, pull it up to IOVDD.

If the AD conversion result meets the set condition, it is stored as a flag.
Which CH flag causes an interrupt to be generated on the ALERT pin can be selected by setting the corresponding bit in the ALERT_CH_SEL register to 1. If a flag is stored on a CH that is not selected, the ALERT pin will not output an interrupt.

3.2 Flag Condition

Threshold, counts, hysteresis, and inside/outside detection can be set as conditions for the flag to be stored, all of which can be specified for each CH. The threshold can be set with the HIGH_THRESHOLD_CHx (x = 0 to 7) and LOW_THRESHOLD_CHx (x = 0 to 7) registers, the number of times with the EVENT_COUNT_CHx (x = 0 to 7) register, hysteresis with the HYSTERESIS_CHx (x = 0 to 7) register, and inside/outside detection with the EVENT_RGN register.

For example, in the case of the setting shown in Figure 31, EVENT_RGN=0, the counter is incremented when the AD conversion result exceeds the High threshold or falls below the Low threshold in the outside detection. Also, since EVENT_COUNT_CHx (x = 0 to 7) = 2, the flag is set when the AD conversion result exceeds the threshold value three times in a row. In this case, the flag is distinguished which threshold is exceeded.

In the case of Figure 31, the AD conversion result exceeds the threshold value from the fourth time, so the event counter is incremented, but the sixth time the AD conversion result is below the threshold value including hysteresis, so the event counter is reset and the counting starts again from the first time when the result exceeds the threshold value again.

Regarding hysteresis, the value set is shifted 3 bits to the left, so 8 times the value written to the register is applied.

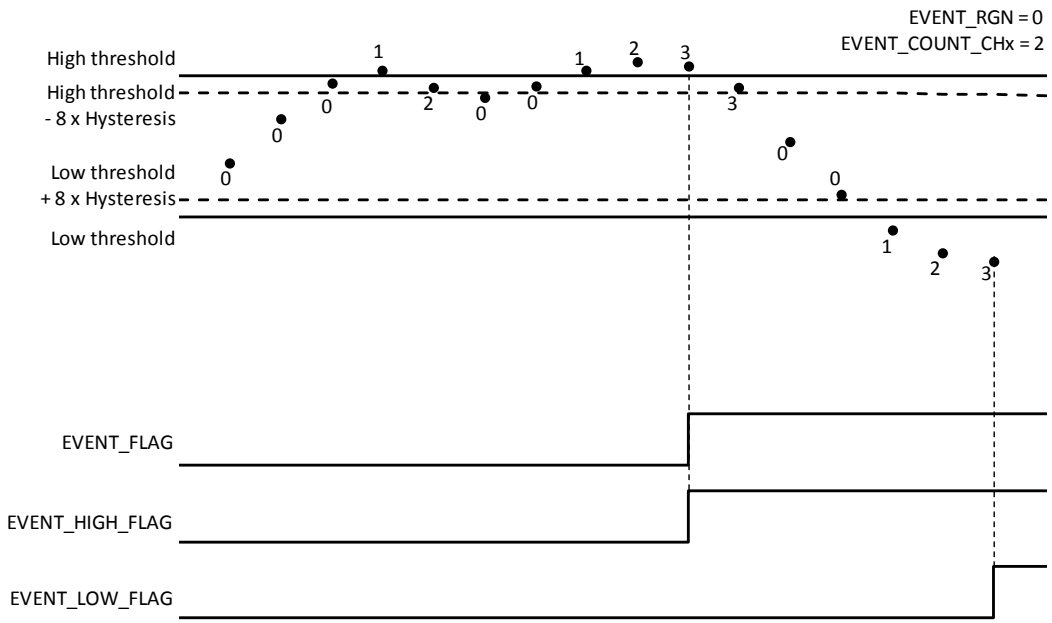


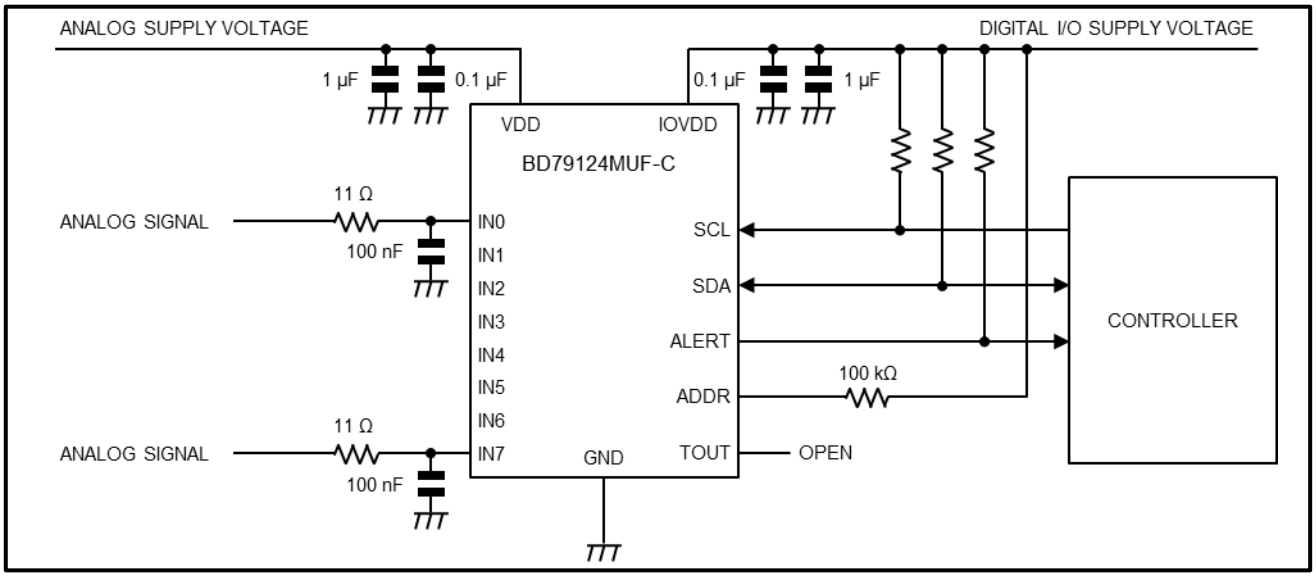
Figure 31. ALERT detection example

3.3 Flag Register

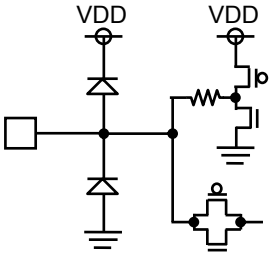
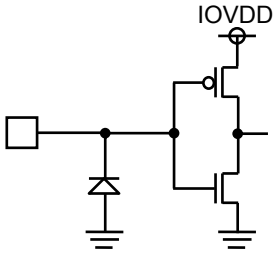
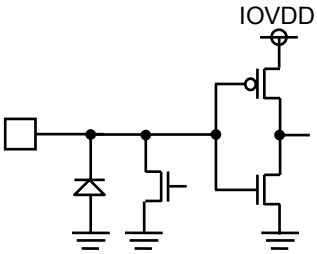
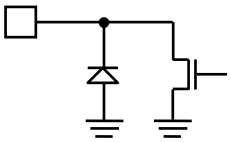
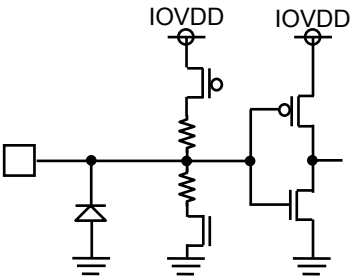
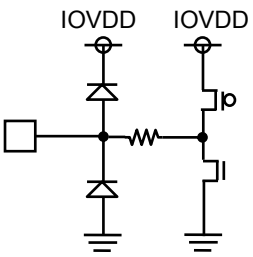
Whether or not each CH is flagged can be checked by reading the EVENT_FLAG register.
Each bit of the EVENT_FLAG register is the logical OR of each bit of the EVENT_HIGH_FLAG and EVENT_LOW_FLAG registers. Therefore, the value of the EVENT_FLAG register is 1 when either threshold is exceeded.

To clear the flag, write 1 to the bit of the EVENT_HIGH_FLAG or EVENT_LOW_FLAG register.

Application Example



I/O Equivalence Circuits

Pin Name	Equivalence Circuit	Pin Name	Equivalence Circuit
IN0 IN1 IN2 IN3 IN4 IN5 IN6 IN7		SCL	
SDA		ALERT	
ADDR		TOUT	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

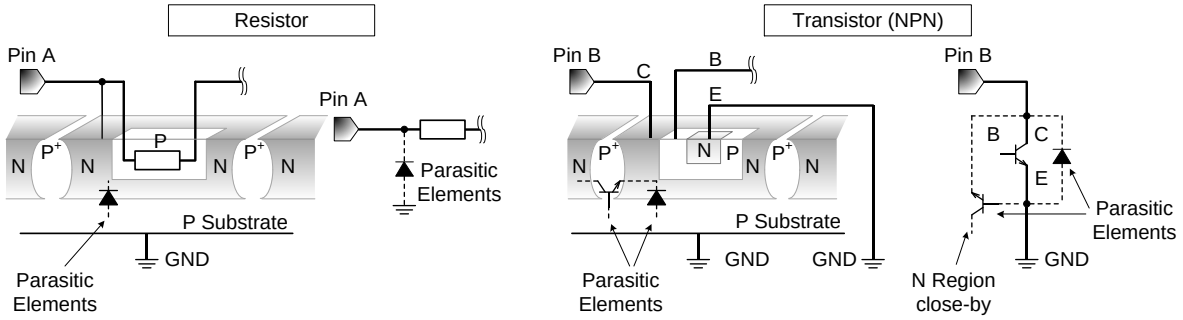


Figure 32. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

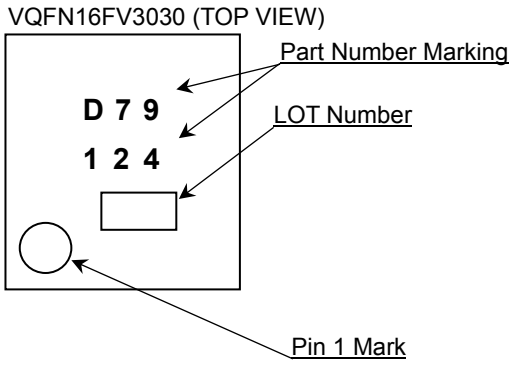
Ordering Information

B	D	7	9	1	2	4	M	U	F	-	C	E	2

Package
MUF: VQFN16FV3030

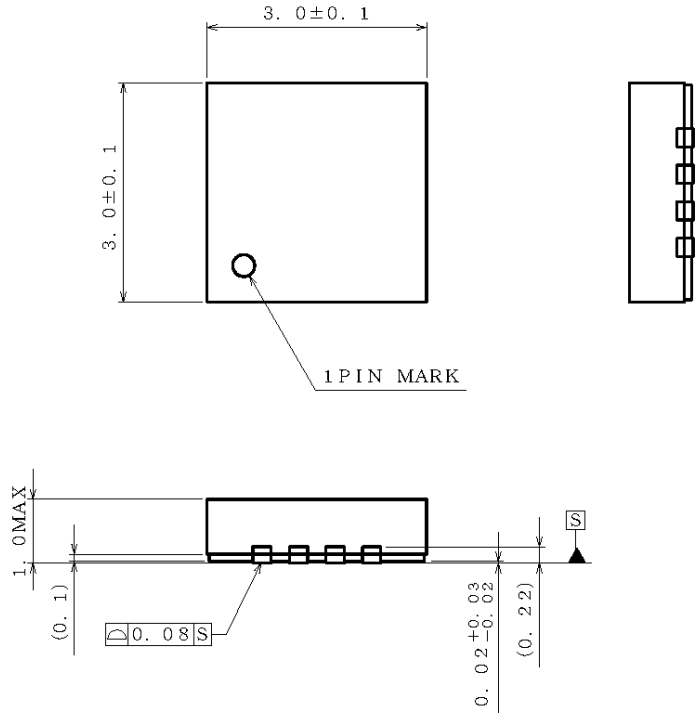
Product Rank
C: for Automotive
Packaging and forming Specification
E2: Embossed tape and reel

Marking Diagram



Physical Dimension and Packing Information

Package Name	VQFN16FV3030

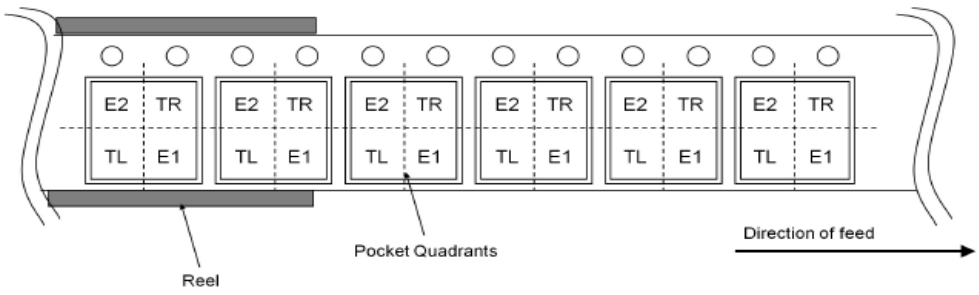


(UNIT : mm)
PKG : VQFN16FV3030
Drawing No. EX396−5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
23.Jul.2024	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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