Operational Amplifier

Low Noise High Output Drive Rail-to-Rail input/output CMOS Operational Amplifier

TLR2374FV-LB

General Description

This product is a rank product for the industrial equipment market.
This is the best product for use in these applications.
This product is a Rail-to-Rail input/output monolithic IC integrated quad independent CMOS operational amplifier features wide operating voltage range with 4 V to 16 V, low input offset voltage, low noise, low input bias current and high output drive. It is suitable for equipment operating from battery power and using sensors that an amplifier.

Features

- Low Noise
- Rail-to-Rail input/output
- Wide Operating Supply Voltage Range
- High Output Drive

Applications

- Industrial Equipment
- Battery-powered Equipment
- Current Monitoring Amplifier
- ADC Front Ends, Buffer Amplifier
- Photodiode Amplifiers
- Sensor Amplifiers

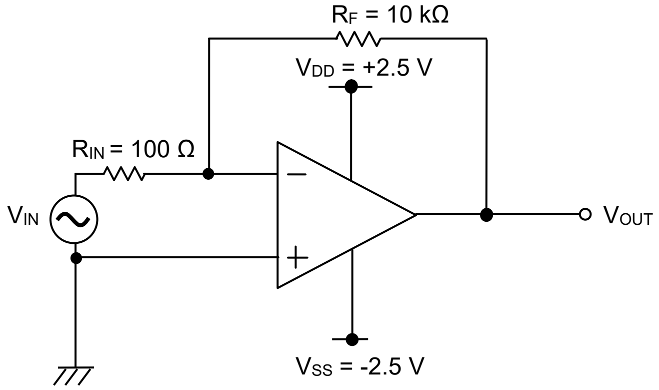
Key Specifications

- Input Offset Voltage: 1.5 mV (Max)
- Input-referred Noise Voltage Density
  - f = 1 kHz: 25 nV/√Hz (Typ)
  - f = 10 kHz: 12 nV/√Hz (Typ)
- Common-mode Input Voltage Range: V_{SS} to V_{DD}
- Input Bias Current: 2.5 pA (Typ)
- Output Current (V_{OUT} = 0.5 V): 22 mA (Typ)
- Operating Supply Voltage Range
  - Single Supply: 4.0 V to 16.0 V
  - Dual Supply: ±2.0 V to ±8.0 V
- Operating Temperature Range: -40 °C to +125 °C

Package

Package	W (Typ) x D (Typ) x H (Max)
SSOP-B14	5.0 mm x 6.4 mm x 1.35 mm

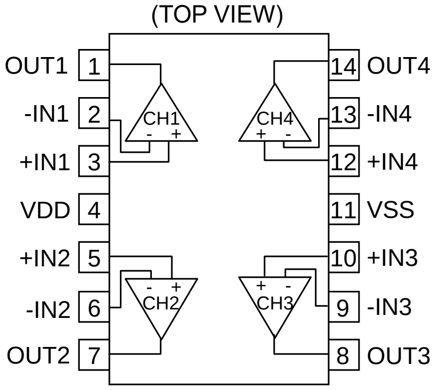
Typical Application Circuit



$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

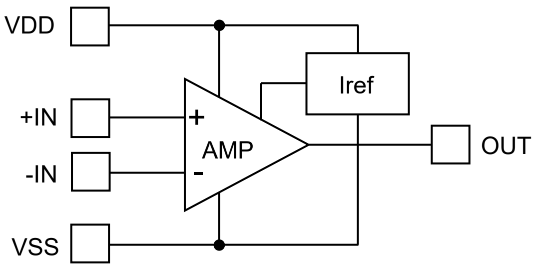
○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configurations



Pin No.	Pin Name	Function
1	OUT1	Output1
2	-IN1	Inverting input1
3	+IN1	Non-inverting input1
4	VDD	Positive power supply
5	+IN2	Non-inverting input2
6	-IN2	Inverting input2
7	OUT2	Output2
8	OUT3	Output3
9	-IN3	Inverting input3
10	+IN3	Non-inverting input3
11	VSS	Negative power supply / Ground
12	+IN4	Non-inverting input4
13	-IN4	Inverting input4
14	OUT4	Output4

Block Diagram



(Note) Each channel has the same configuration.

Description of Blocks

1. AMP:
   This block is a full-swing output operational amplifier with class-AB output circuit and high-precision-Rail-to-Rail differential input stage.

2. Iref:
   This block supplies reference current which is needed to operate AMP block.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage (V_{DD} - V_{SS})	V_S	18	V
Input Pin Voltage (+IN, -IN)	V_I	(V_{SS} - 0.3) to (V_{SS} + 18)	V
Input Pin Current (+IN, -IN)	I_I	10	mA
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operate over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSOP-B14				
Junction to Ambient	θ_{JA}	159.6	92.8	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	13	9	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{DD} - V_{SS})	Single Supply	V_S	4.0	5.0	16.0	V
	Dual Supply		±2.0	±2.5	±8.0	
Operating Temperature		Topr	-40	+25	+125	°C

Electrical Characteristics

(Unless otherwise specified V_S = 5 V, V_{SS} = 0 V, V_{ICM} = 2.5 V, R_L = 10 kΩ to V_{ICM}, Ta = 25 °C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Offset Voltage	V_{IO}	-	0.01	0.60	mV	No load, Absolute value
		-	-	1.50		No load, Absolute value, Ta = -40 °C to +125 °C
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	0.2	7.0	µV/°C	No load, Absolute value, Ta = -40 °C to +125 °C
Input Offset Current	I_{IO}	-	0	-	pA	Absolute value
Input Bias Current	I_B	-	2.5	-	pA	Absolute value
Common-mode Input Voltage Range	V_{ICMR}	0	-	5	V	V_{SS} to V_{DD}
Supply Current	I_{DD}	-	4.5	6.8	mA	No load, G = 0 dB
		-	-	7		No load, G = 0 dB, Ta = -40 °C to +125 °C
Output Voltage High	V_{OH}	-	20	100	mV	I_L = 1 mA, V_{OH} = V_{DD} - V_{OUT}
		-	-	150		I_L = 1 mA, V_{OH} = V_{DD} - V_{OUT}, Ta = -40 °C to +125 °C
Output Voltage Low	V_{OL}	-	20	100	mV	I_L = 1 mA,
		-	-	150		I_L = 1 mA, Ta = -40 °C to +125 °C
Output Source Current *(Note 1)*	I_{OH}	-	22	-	mA	V_{OUT} = V_{DD} - 0.5 V, Absolute value
Output Sink Current *(Note 1)*	I_{OL}	-	22	-	mA	V_{OUT} = V_{SS} + 0.5 V, Absolute value
Large Signal Voltage Gain	A_V	82	110	-	dB	-
		80	-	-		Ta = -40 °C to +125 °C
Gain Bandwidth Product	GBW	-	5	-	MHz	G = 40 dB, C_L = 25 pF
Phase Margin	θ	-	65	-	deg	G = 40 dB, C_L = 25 pF
Common-mode Rejection Ratio	CMRR	70	90	-	dB	-
Power Supply Rejection Ratio	PSRR	70	90	-	dB	-
Slew Rate	SR	-	3	-	V/µs	C_L = 50 pF
Input-referred Noise Voltage Density	Vn	-	25	-	nV/√Hz	f = 1 kHz
		-	12	-		f = 10 kHz
Total Harmonic Distortion + Noise	THD+N	-	0.001	-	%	V_{OUT} = 2.5 Vp-p, f = 1 kHz
Channel Separation	CS	-	100	-	dB	input referred

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Typical Performance Curves

V_{SS} = 0 V

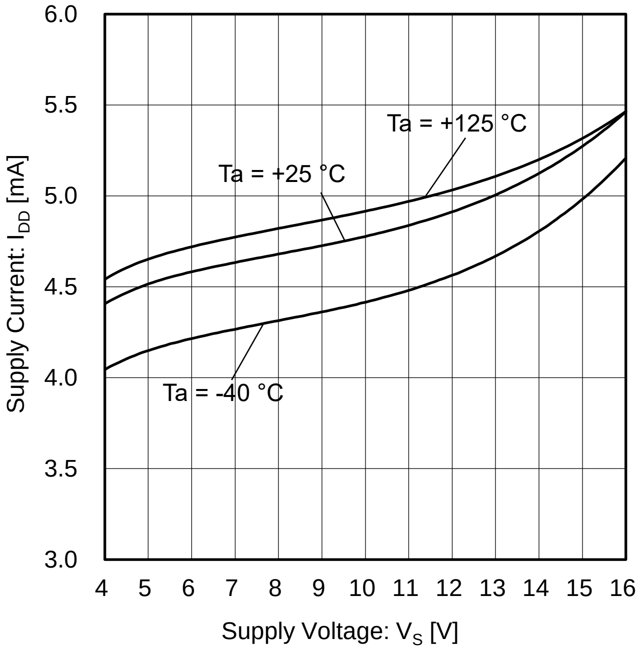


Figure 1. Supply Current vs Supply Voltage

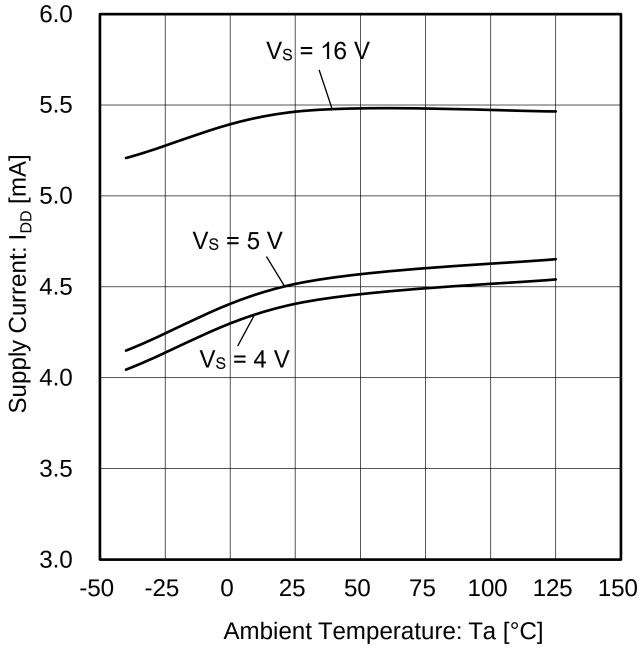


Figure 2. Supply Current vs Ambient Temperature

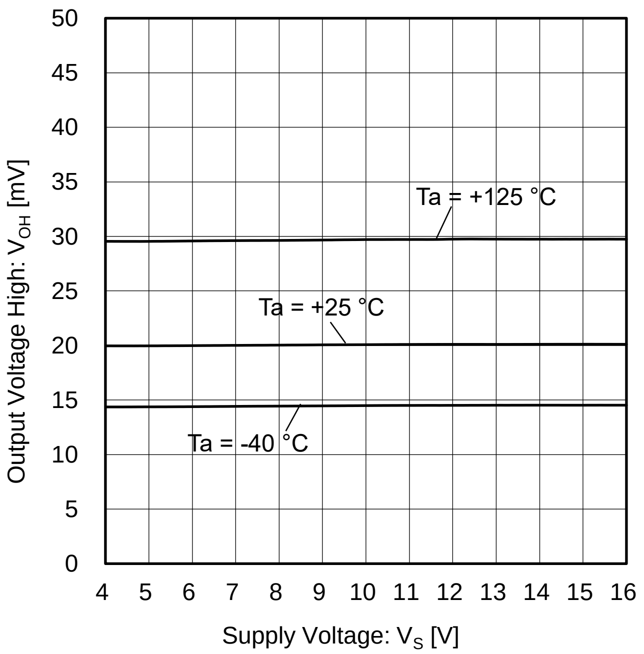


Figure 3. Output Voltage High vs Supply Voltage
(I_L = 1 mA)

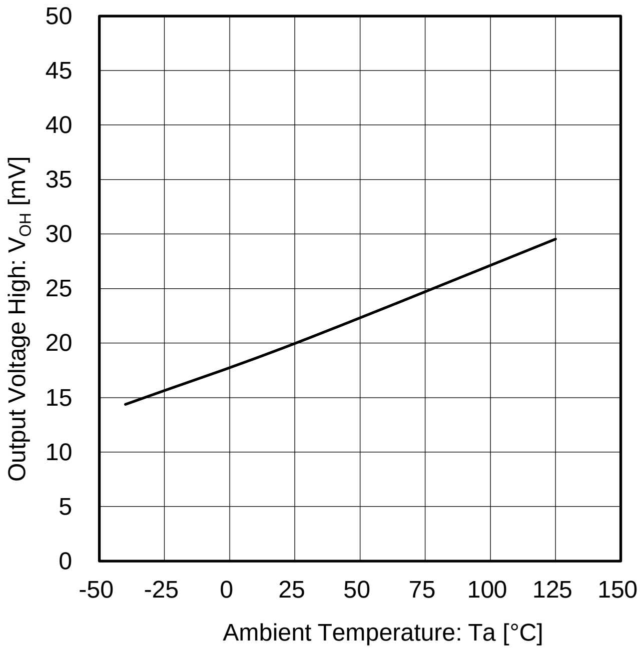


Figure 4. Output Voltage High vs Ambient Temperature
(V_S = 5 V, I_L = 1 mA)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

V_{SS} = 0 V

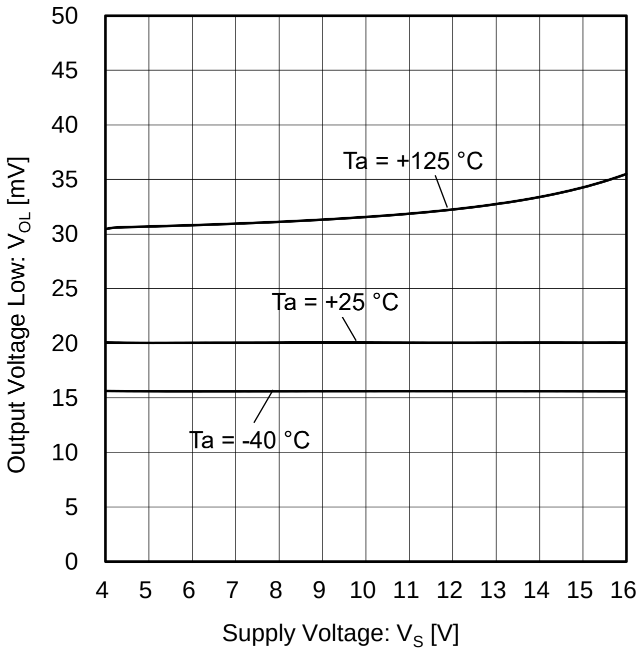


Figure 5. Output Voltage Low vs Supply Voltage
(I_L = 1 mA)

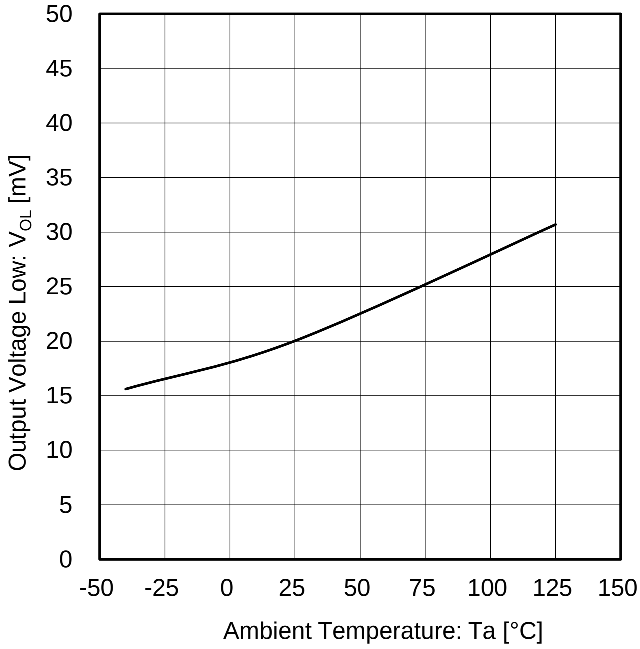


Figure 6. Output Voltage Low vs Ambient Temperature
(V_S = 5 V, I_L = 1 mA)

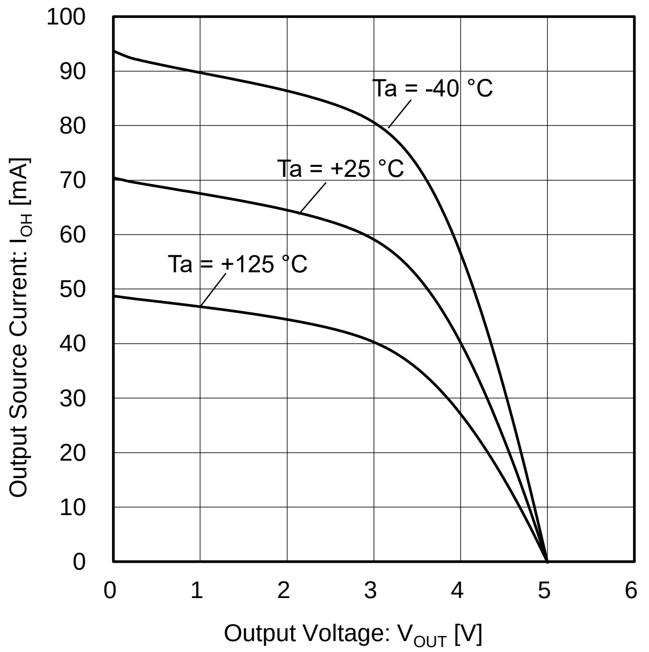


Figure 7. Output Source Current vs Output Voltage
(V_S = 5 V)

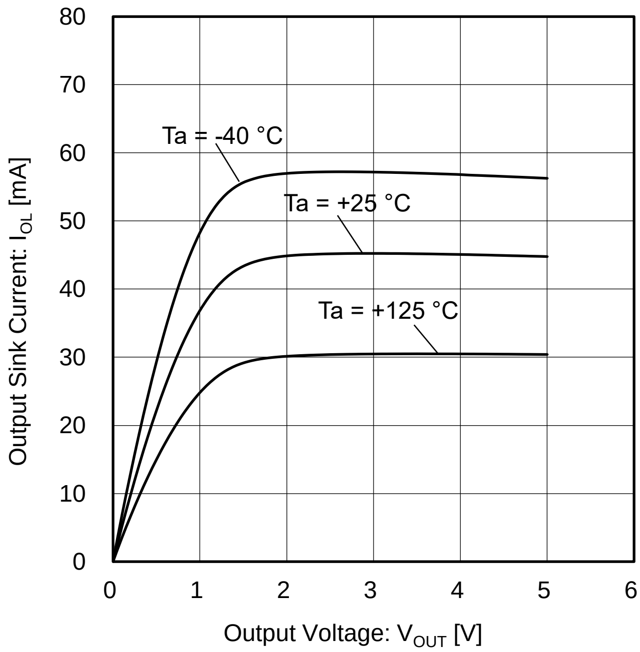


Figure 8. Output Sink Current vs Output Voltage
(V_S = 5 V)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

V_{SS} = 0 V

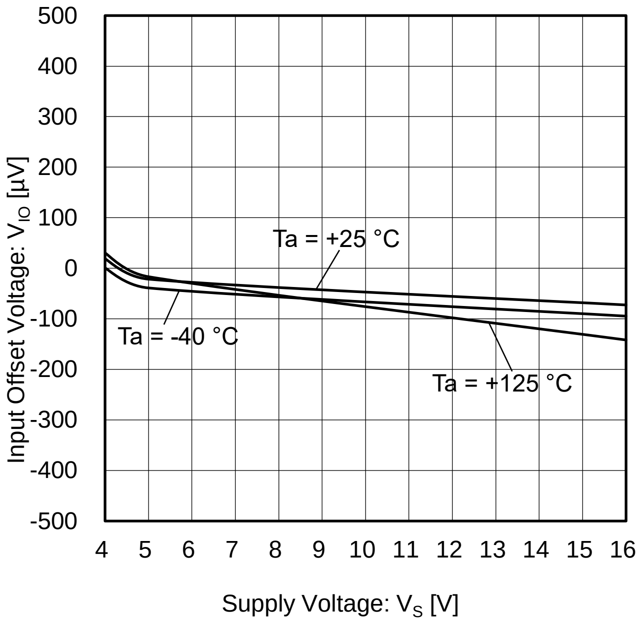


Figure 9. Input Offset Voltage vs Supply Voltage

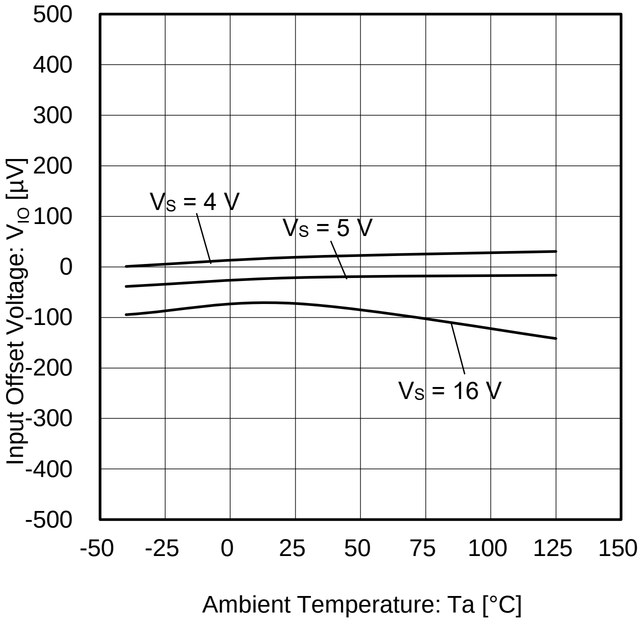


Figure 10. Input Offset Voltage vs Ambient Temperature

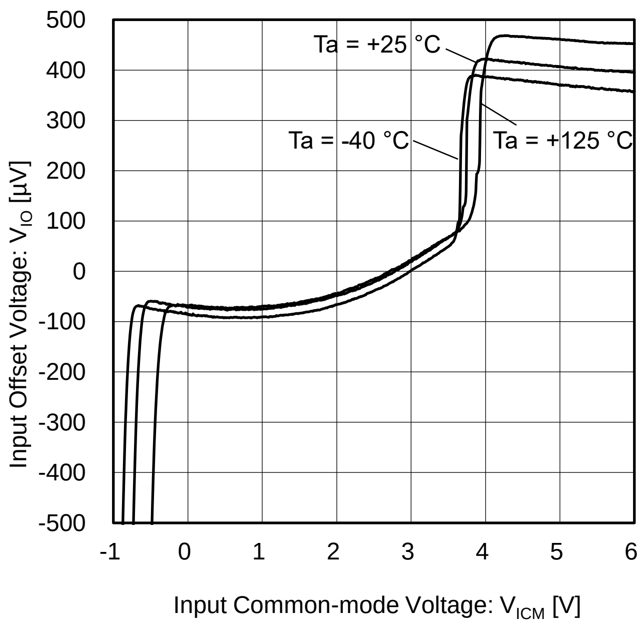


Figure 11. Input Offset Voltage vs Input Common-mode Voltage
(V_S = 5 V)

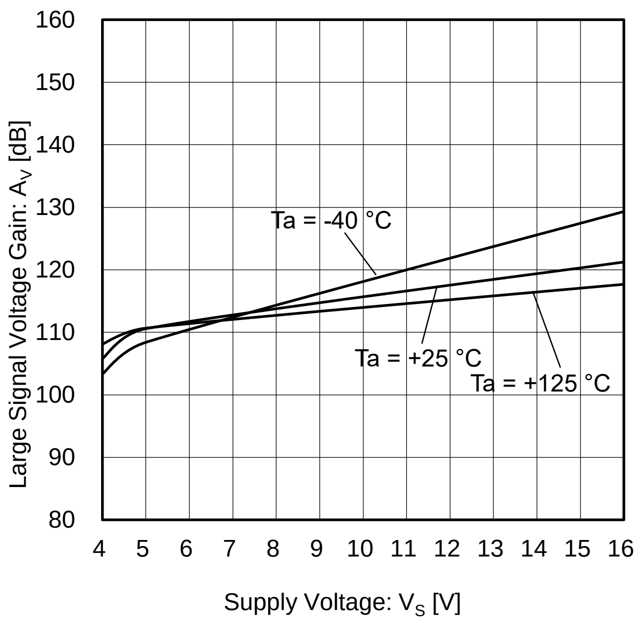


Figure 12. Large Signal Voltage Gain vs Supply Voltage
(R_L = 10 kΩ)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

V_{SS} = 0 V

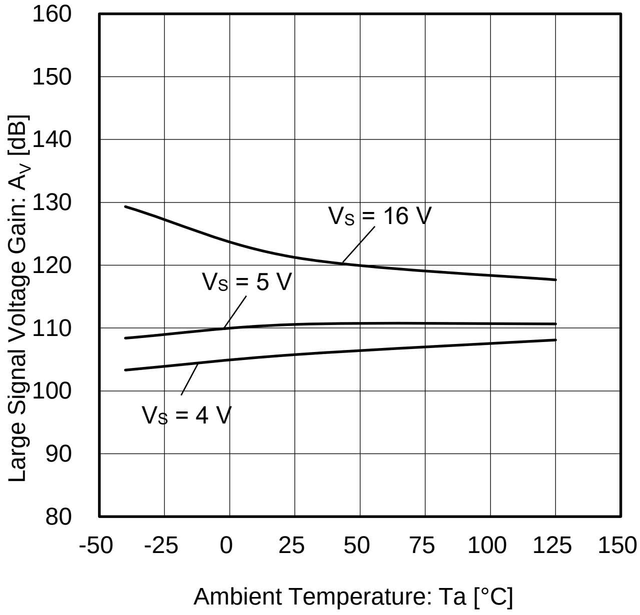


Figure 13. Large Signal Voltage Gain vs Ambient Temperature

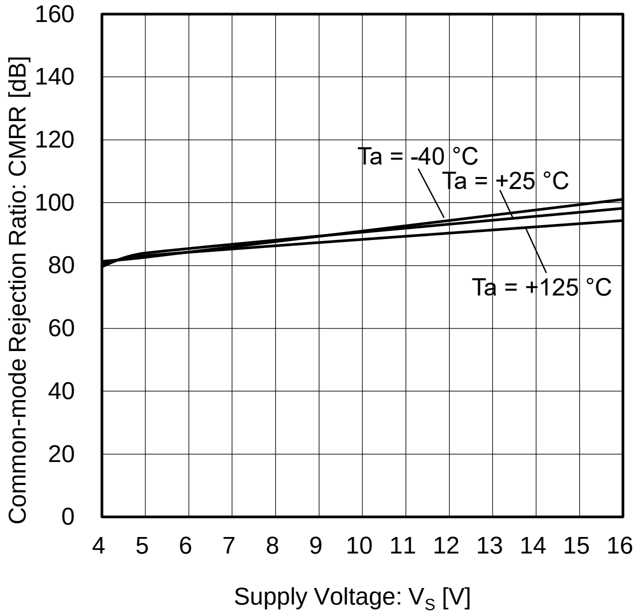


Figure 14. Common-mode Rejection Ratio vs Supply Voltage

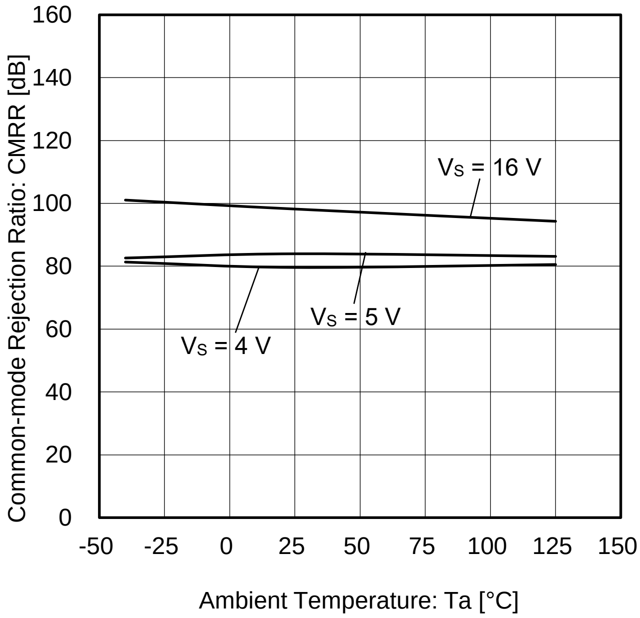


Figure 15. Common-mode Rejection Ratio vs Ambient Temperature

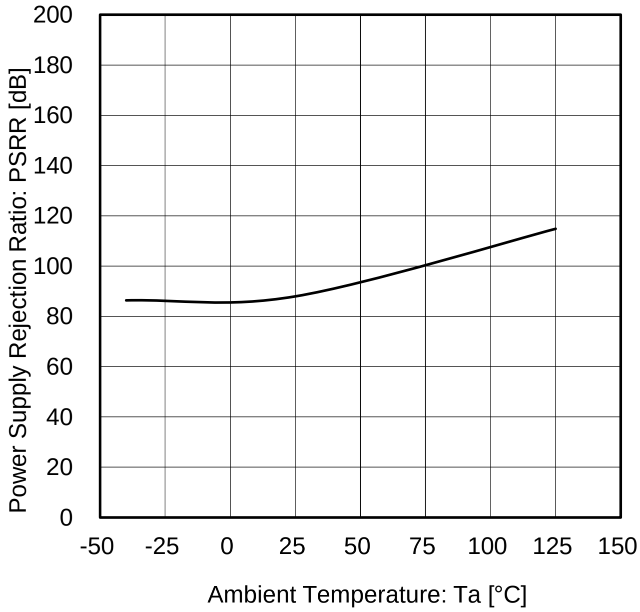


Figure 16. Power Supply Rejection Ratio vs Ambient Temperature

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

V_{SS} = 0 V

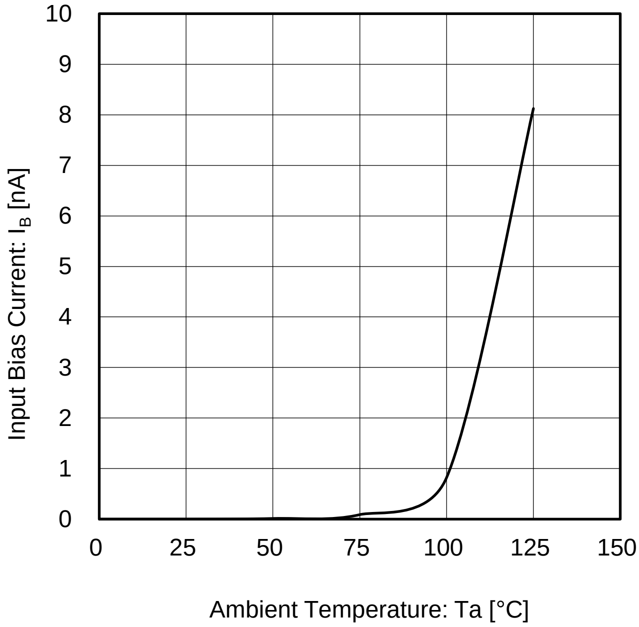


Figure 17. Input Bias Current vs Ambient Temperature
(V_S = 5 V)

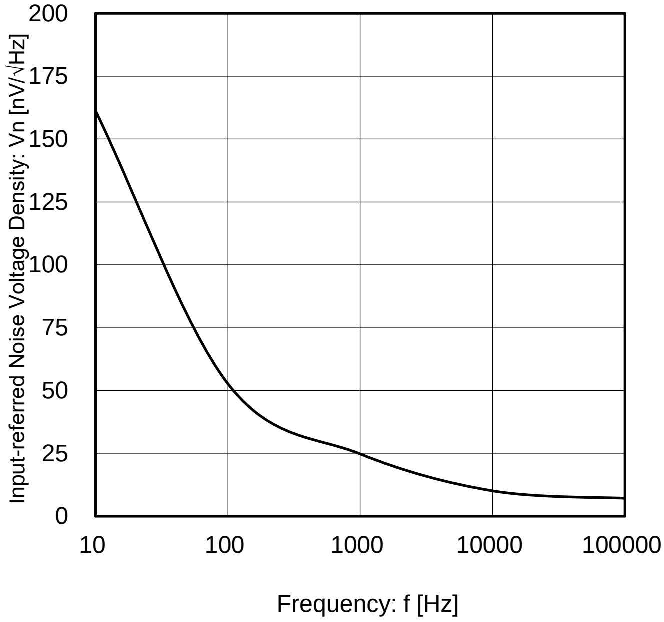


Figure 18. Input-referred Noise Voltage Density vs Frequency
(V_S = 5 V)

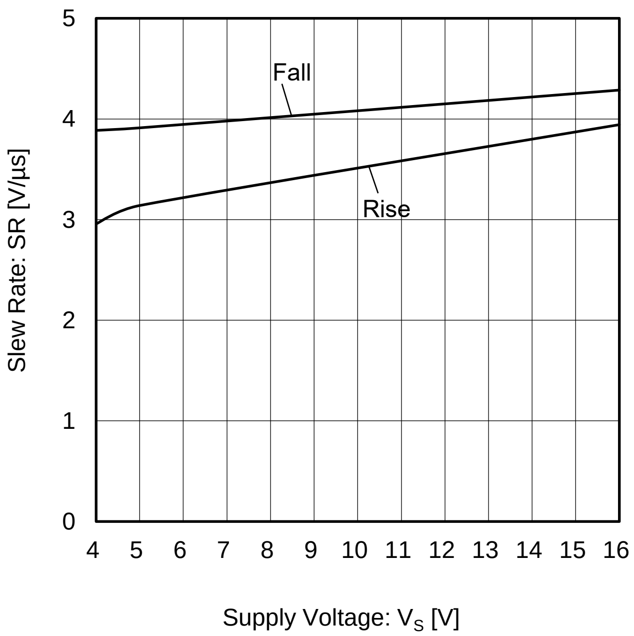


Figure 19. Slew Rate vs Supply Voltage

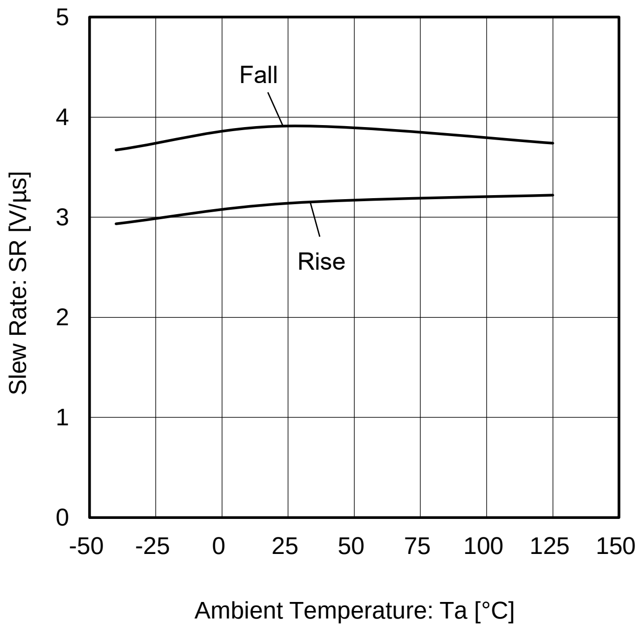


Figure 20. Slew Rate vs Ambient Temperature
(V_S = 5 V)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

V_{SS} = 0 V

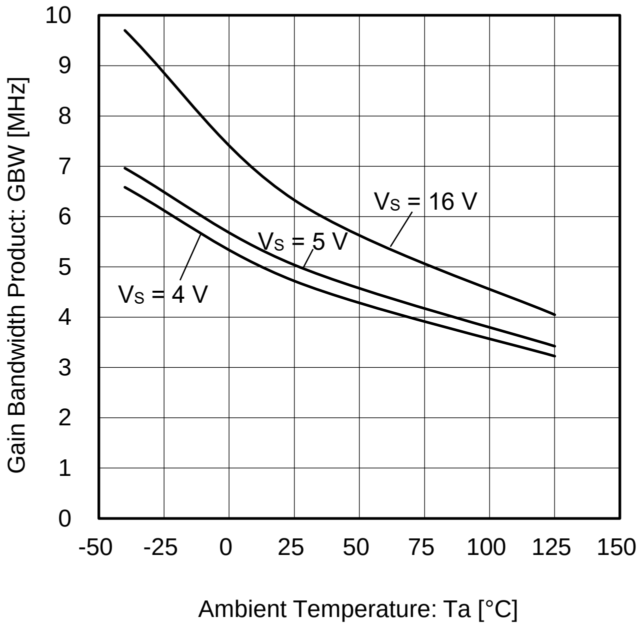


Figure 21. Gain Bandwidth Product vs Ambient Temperature

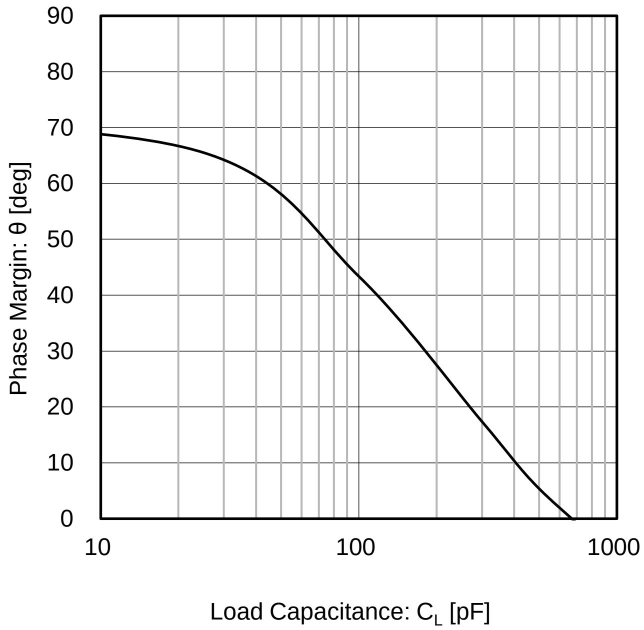


Figure 22. Phase Margin vs Load Capacitance
(V_S = 5 V, R_F = 10 kΩ, G = 40 dB)

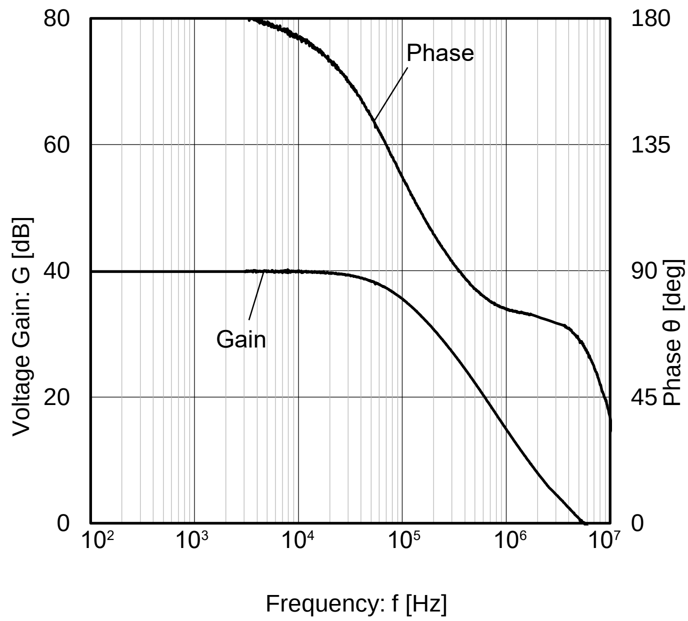


Figure 23. Voltage Gain vs Frequency
(V_S = 5 V)

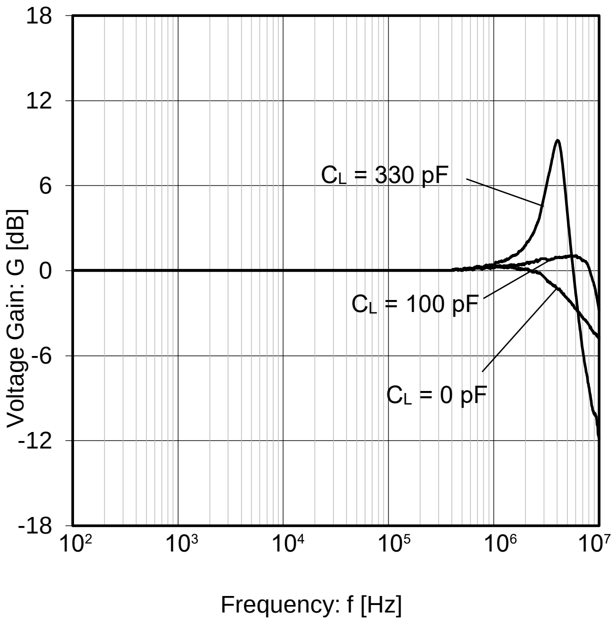


Figure 24. Voltage Gain vs Frequency
(V_S = 5 V, G = 0 dB, V_{IN} = 180 mV_{P-P})

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Application Examples

○Voltage Follower

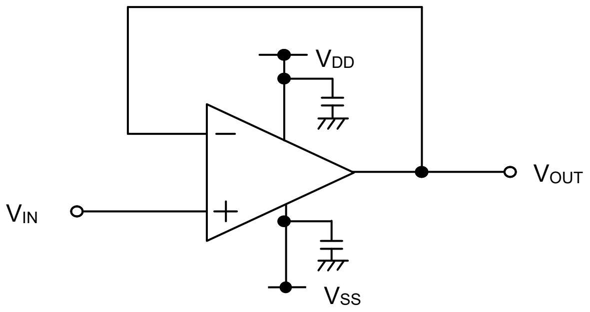


Figure 25. Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage due to high input impedance and low output impedance. Computation for output voltage is shown below.

$$V_{OUT} = V_{IN}$$

○Inverting Amplifier

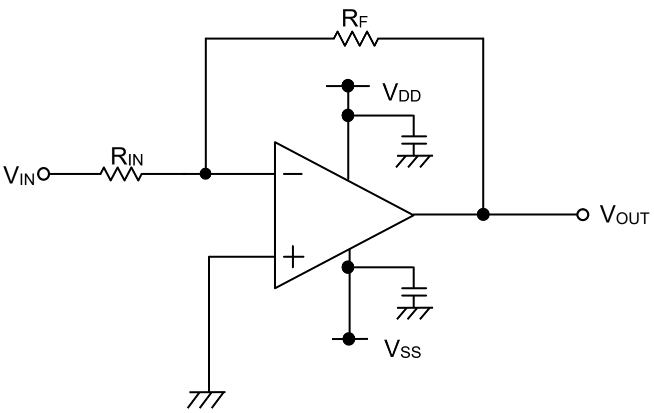


Figure 26. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain which depends on the ratio of R_{IN} and R_F, and then it outputs phase-inverted voltage. The output voltage is shown in the next expression.

$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

This circuit has input impedance equal to R_{IN}.

○Non-inverting Amplifier

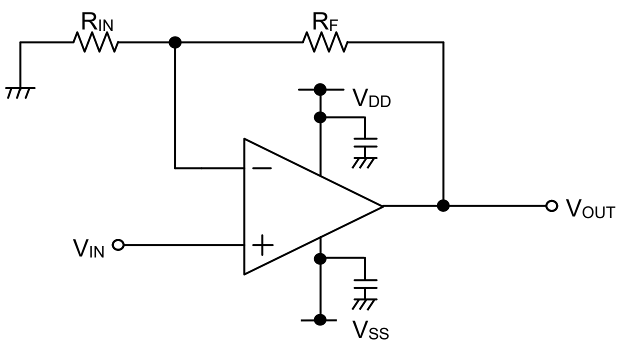


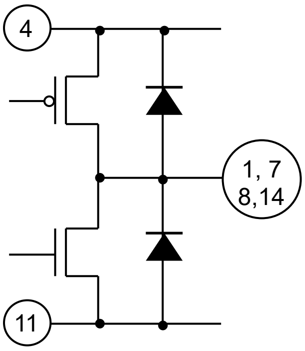
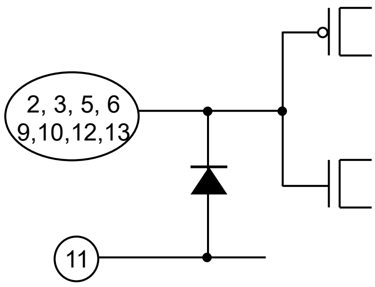
Figure 27. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_{IN} and R_F. The output voltage (V_{OUT}) is in-phase with the input voltage and is shown in the next expression.

$$V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Description	Equivalence Circuit
1 7 8 14	OUT1 OUT2 OUT3 OUT4	Output	
2 3 5 6 9 10 12 13	-IN1 +IN1 +IN2 -IN2 -IN3 +IN3 +IN4 -IN4	Input	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

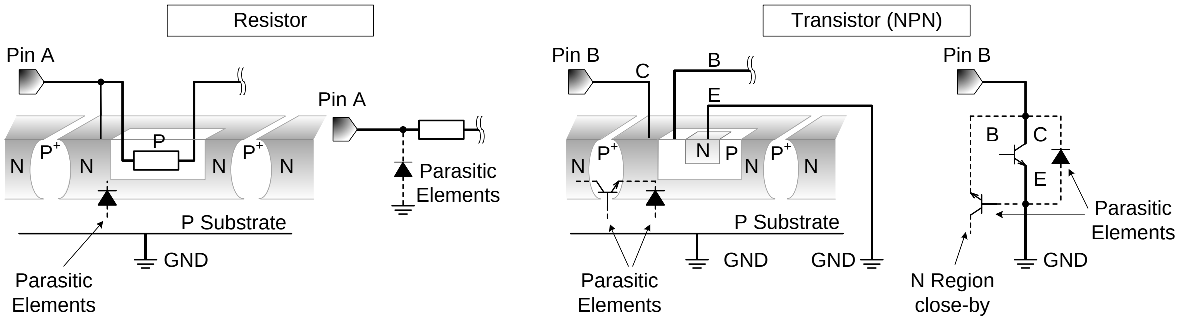


Figure 28. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

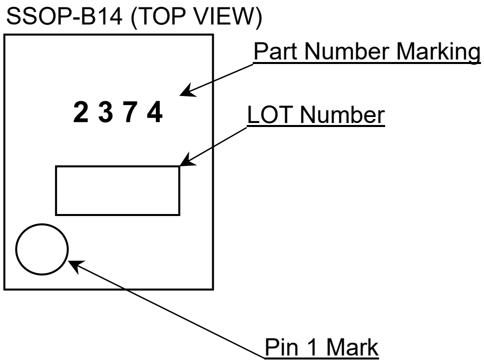
Ordering Information

T L R 2 3 7 4 F V - L B E 2

Package
FV: SSOP-B14

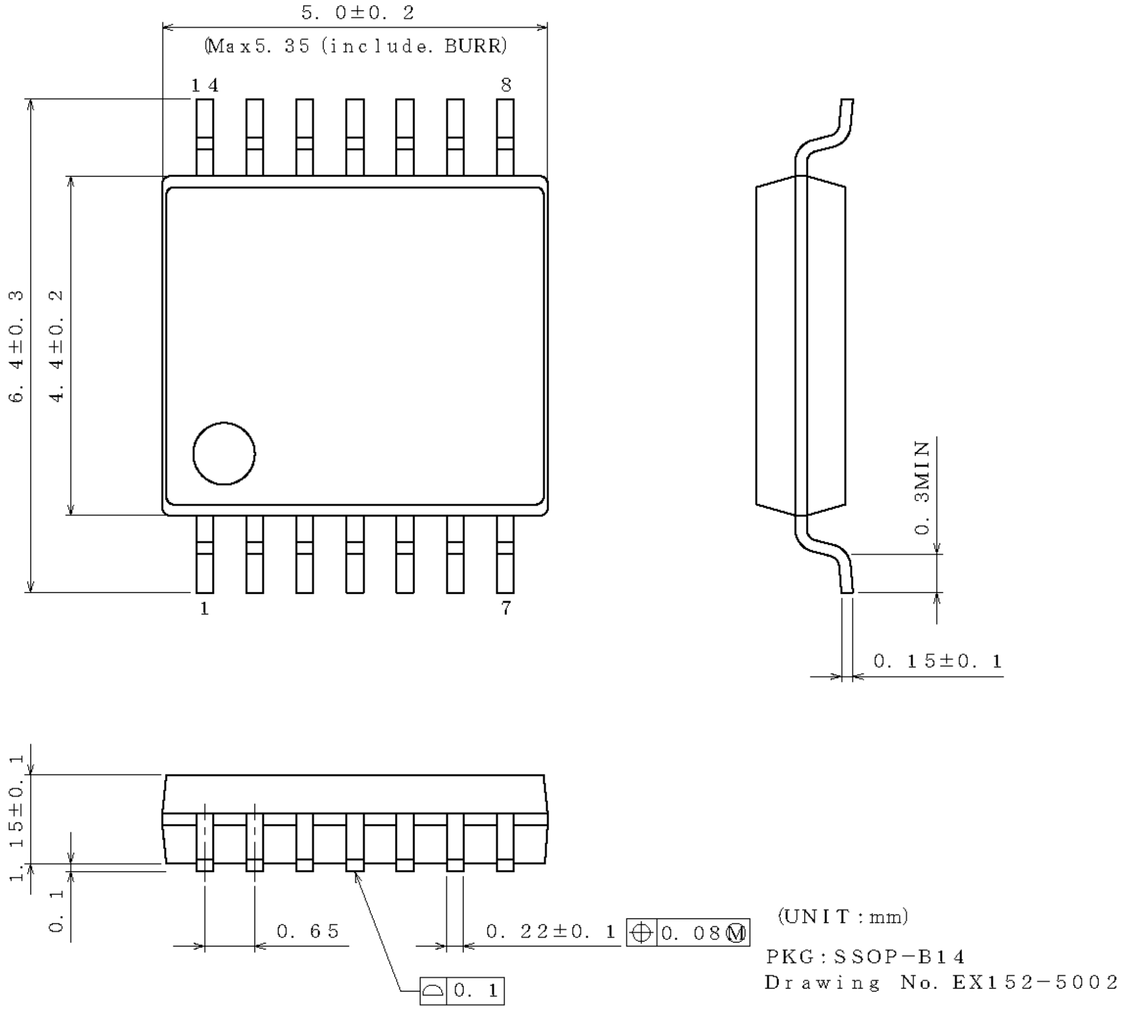
Product Rank
LB: for Industrial applications
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagrams



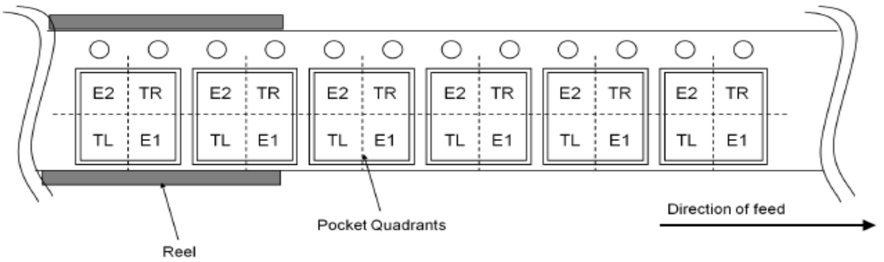
Physical Dimension and Packing Information

Package Name	SSOP-B14



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
31.Aug.2023	001	New Release