Operational Amplifier

Automotive Zero Drift Low Offset Voltage Rail-to-Rail input/output CMOS Operational Amplifier

LMR1001YF-C

General Description

LMR1001YF-C single CMOS operational amplifier features zero drift, low input offset voltage and Rail-to-Rail input/output that are suitable for sensor amplifiers, engine control unit, electric power steering, anti-lock braking system and all automotive application.

Features

- AEC-Q100 Qualified*(Note 1)*
- Low Input Offset Voltage Temperature Drift
- Low Input Offset Voltage
- Rail-to-Rail input/output

(Note 1) Grade 1

Applications

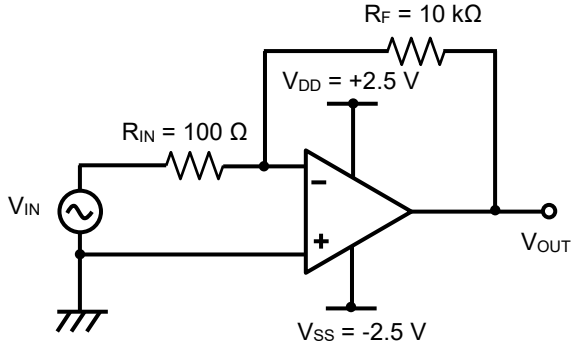
- Engine Control Unit
- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- All Automotive Application
- Battery-powered Equipment
- Current Sense Amplifiers
- Input, Output ADC, and DAC Buffers
- Photodiode Amplifiers
- Sensor Amplifiers

Key Specifications

- Input Offset Voltage Temperature Drift: 25 nV/°C (Typ)
- Input Offset Voltage: 12 µV (Max)
- Common-mode Input Voltage Range: V_{SS} to V_{DD}
- Input Bias Current: 150 pA (Typ)
- Operating Supply Voltage Range
  - Single Supply: 2.7 V to 5.5 V
  - Dual Supply: ±1.35 V to ±2.75 V
- Operating Temperature Range: -40 °C to +125 °C

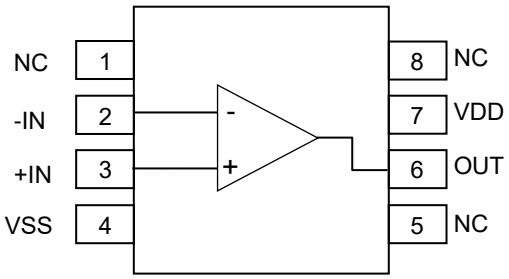
Package	**W (Typ) x D (Typ) x H (Max)**
SOP8	5.0 mm x 6.2 mm x 1.71 mm

Typical Application Circuit



$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

Pin Configuration



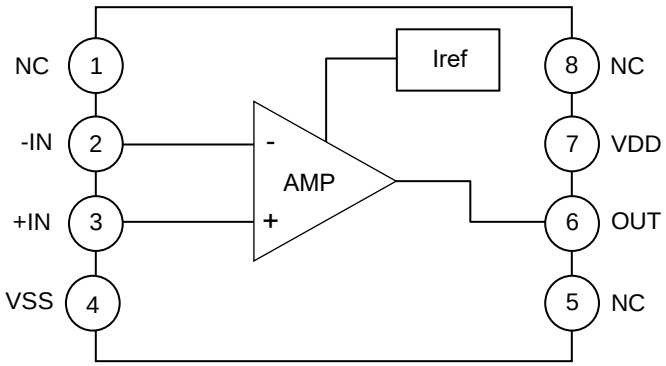
(TOP VIEW)

Pin Description

Pin No.	Pin Name	Function
1	NC	No connect*(Note 1)*
2	-IN	Inverting input
3	+IN	Non-inverting input
4	VSS	Negative power supply / Ground
5	NC	No connect*(Note 1)*
6	OUT	Output
7	VDD	Positive power supply
8	NC	No connect*(Note 1)*

(Note 1) Keep open on an application board.

Block Diagram



Description of Blocks

1. AMP:
   This block is a Rail-to-Rail input/output operational amplifier with class-AB output circuit and differential input stage.

2. Iref:
   This block supplies reference current which is needed to operate AMP block.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage (V_{DD} – V_{SS})	V_S	7.0	V
Differential Input Voltage*(Note 1)*	V_{ID}	V_S	V
Common-mode Input Voltage Range	V_{ICMR}	(V_{SS} - 0.3) to (V_{DD} + 0.3)	V
Input Current	I_I	±10	mA
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) The differential input voltage indicates the voltage difference between inverting input and non-inverting input. The input pin voltage is set to V_{SS} or more.

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
SOP8				
Junction to Ambient	θ_{JA}	197.4	109.8	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	21	19	°C/W

(Note 2) Based on JESD51-2A(Still-Air).

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (V_{DD} – V_{SS})	Single Supply	V_S	2.7	5.0	5.5	V
	Dual Supply		±1.35	±2.50	±2.75	
Operating Temperature		Topr	-40	+25	+125	°C

Electrical Characteristics (Unless otherwise specified V_S = 5 V, V_{SS} = 0 V)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage	V_{IO}	25 °C	-	1	12	µV	Absolute value
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-40 °C to +125 °C	-	25	500	nV/°C	Absolute value
Input Offset Current	I_{IO}	25 °C	-	10	-	pA	Absolute value
Input Bias Current	I_B	25 °C	-	150	-	pA	Absolute value
Supply Current	I_{DD}	25 °C	-	850	1250	µA	R_L = ∞, G = 0 dB
		-40 °C to +125 °C	-	-	1500		
Output Voltage High	V_{OH}	25 °C	-	20	50	mV	R_L = 10 kΩ, V_{OH} = V_{DD} - V_{OUT}
		-40 °C to +125 °C	-	-	100		
Output Voltage Low	V_{OL}	25 °C	-	10	50	mV	R_L = 10 kΩ V_{OL} = V_{OUT} - V_{SS}
		-40 °C to +125 °C	-	-	100		
Large Signal Voltage Gain	Av	25 °C	110	145	-	dB	R_L = 10 kΩ
		-40 °C to +125 °C	100	-	-		
Common-mode Input Voltage Range	V_{ICMR}	25 °C	0	-	5.0	V	V_{SS} to V_{DD}
Common-mode Rejection Ratio	CMRR	25 °C	110	130	-	dB	V_{ICM} = V_{SS} to V_{DD}
Power Supply Rejection Ratio	PSRR	25 °C	95	115	-	dB	V_{DD} = 2.7 V to 5.5 V
Output Source Current *(Note 1)*	I_{OH}	25 °C	25	35	-	mA	V_{OUT} = V_{SS} Absolute value
Output Sink Current *(Note 1)*	I_{OL}	25 °C	25	35	-	mA	V_{OUT} = V_{DD} Absolute value
Slew Rate	SR	25 °C	-	1.3	-	V/µs	R_L = 10 kΩ, G = 0 dB
Gain Bandwidth Product	GBW	25 °C	-	1.5	-	MHz	R_L = 10 kΩ, G = 40 dB
Phase Margin	θ	25 °C	-	70	-	deg	R_L = 10 kΩ, G = 40 dB
Input-referred Noise Voltage Density	Vn	25 °C	-	70	-	nV/√Hz	f = 1 kHz
Overload Recovery Time	t_{OR}	25 °C	-	0.13	-	ms	V_{IN} = (V_{DD}/2 + 0.2 V) to V_{DD}/2, G = 40 dB V_{IN} = (V_{DD}/2 - 0.2 V) to V_{DD}/2, G = 40 dB

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Typical Performance Curves

V_{SS} = 0 V

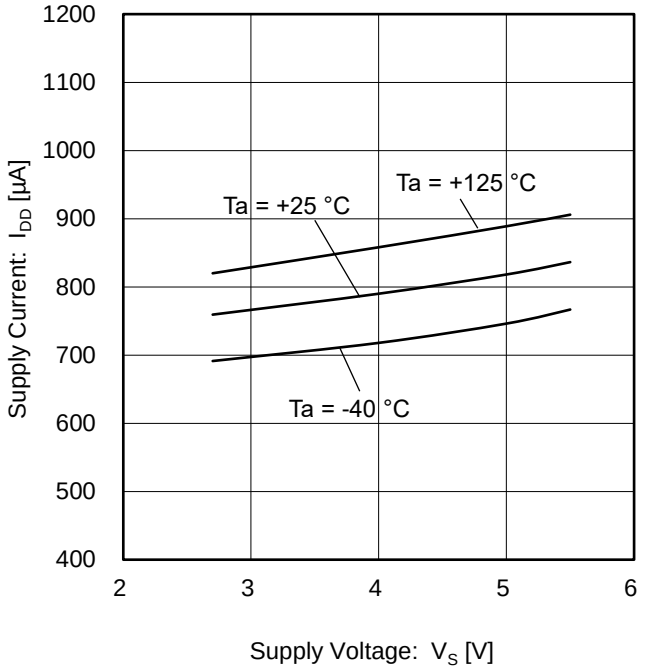


Figure 1. Supply Current vs Supply Voltage

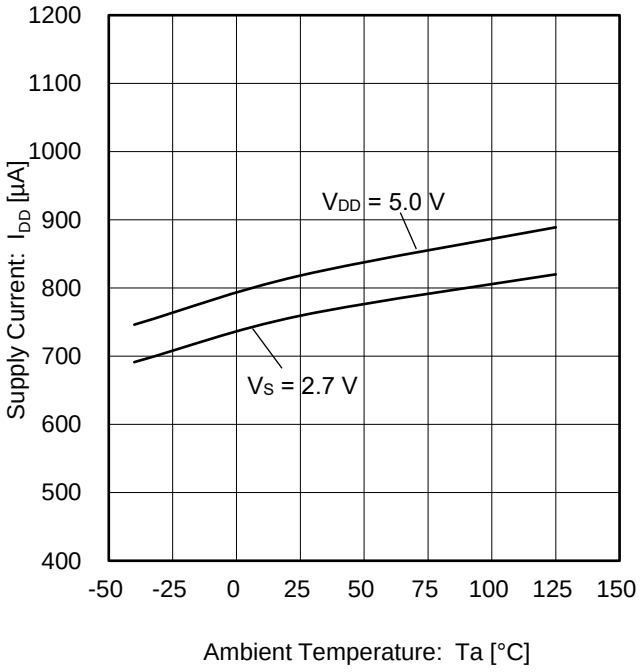


Figure 2. Supply Current vs Ambient Temperature

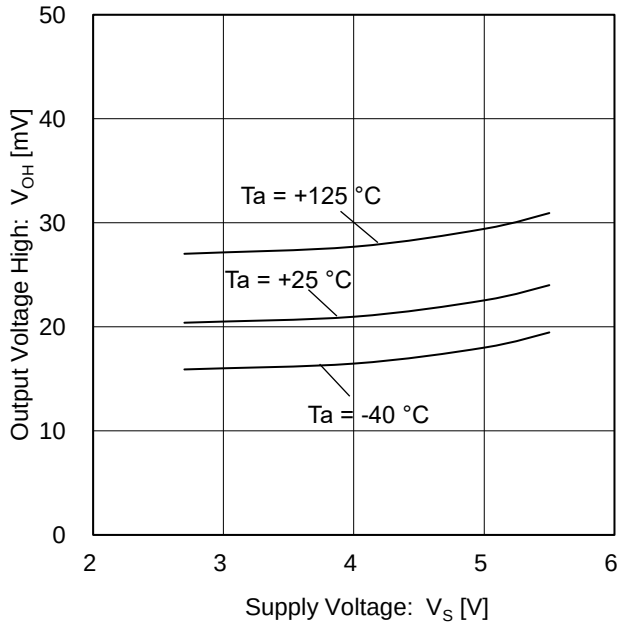


Figure 3. Output Voltage High vs Supply Voltage
(R_L = 10 kΩ)

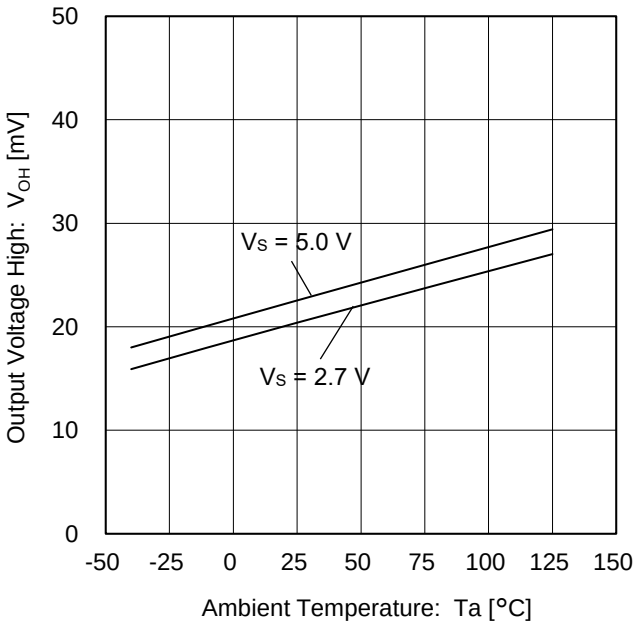


Figure 4. Output Voltage High vs Ambient Temperature
(R_L = 10 kΩ)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
V_{SS} = 0 V

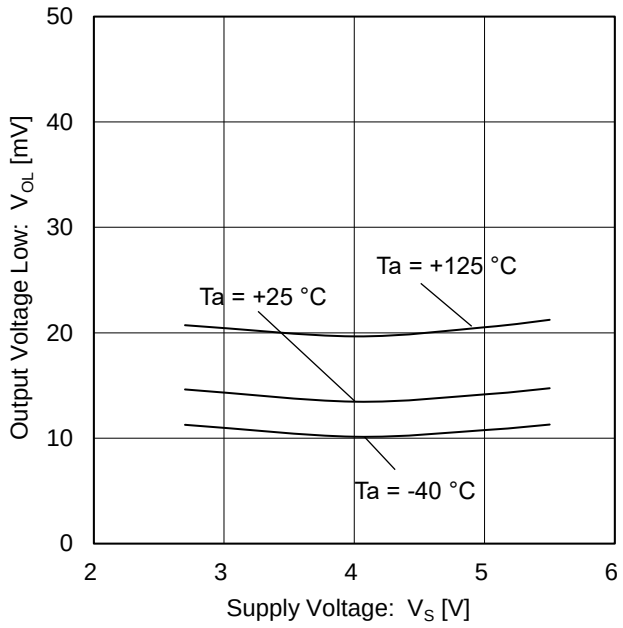


Figure 5. Output Voltage Low vs Supply Voltage
(R_L = 10 kΩ)

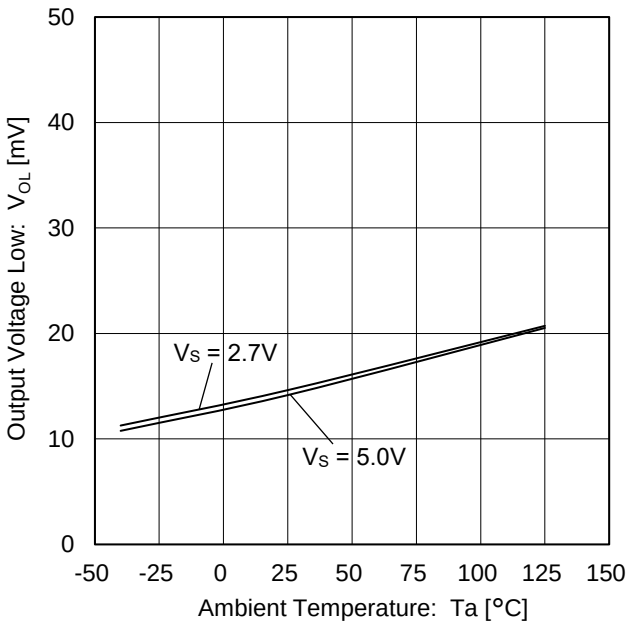


Figure 6. Output Voltage Low vs Ambient Temperature
(R_L = 10 kΩ)

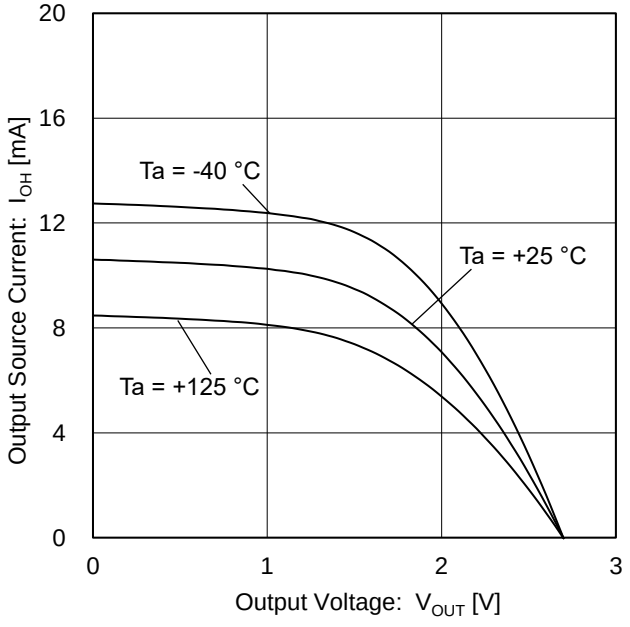


Figure 7. Output Source Current vs Output Voltage
(V_S = 2.7 V)

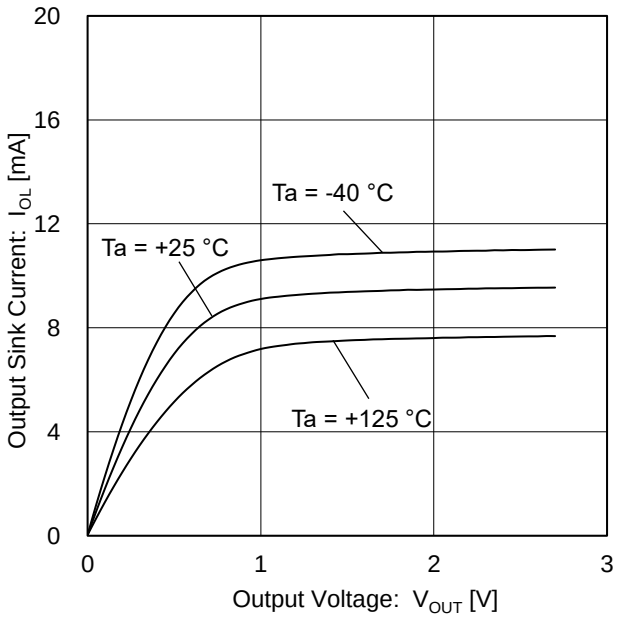


Figure 8. Output Sink Current vs Output Voltage
(V_S = 2.7 V)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
V_{SS} = 0 V

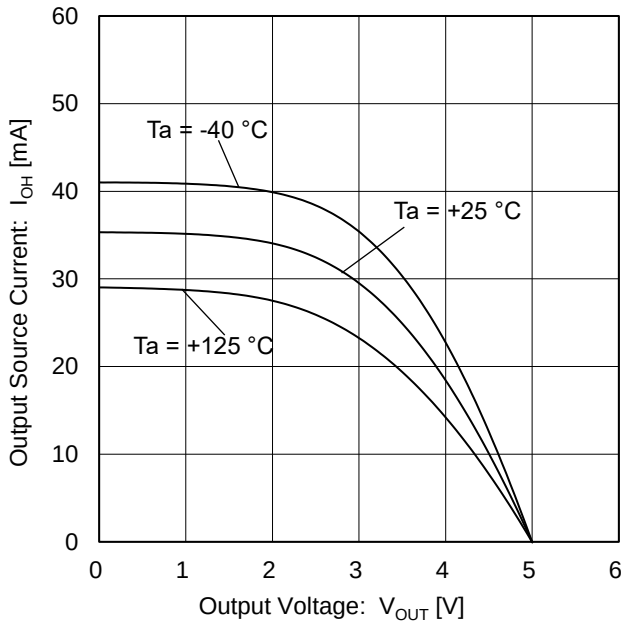


Figure 9. Output Source Current vs Output Voltage
(V_S = 5.0 V)

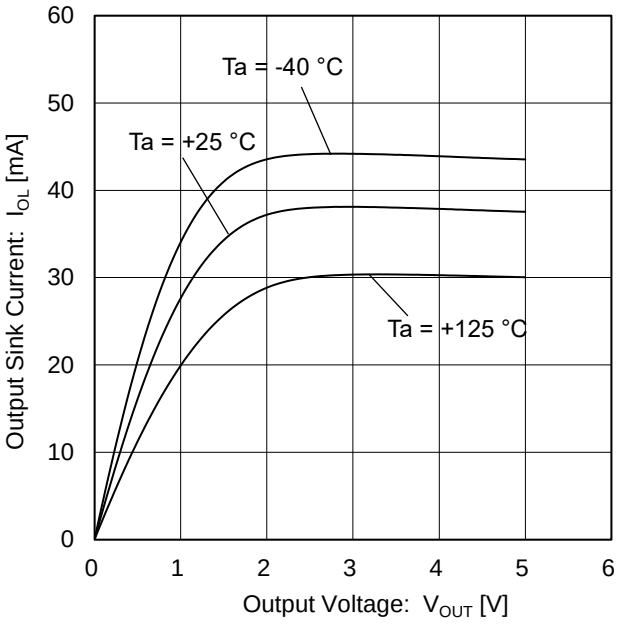


Figure 10. Output Sink Current vs Output Voltage
(V_S = 5.0 V)

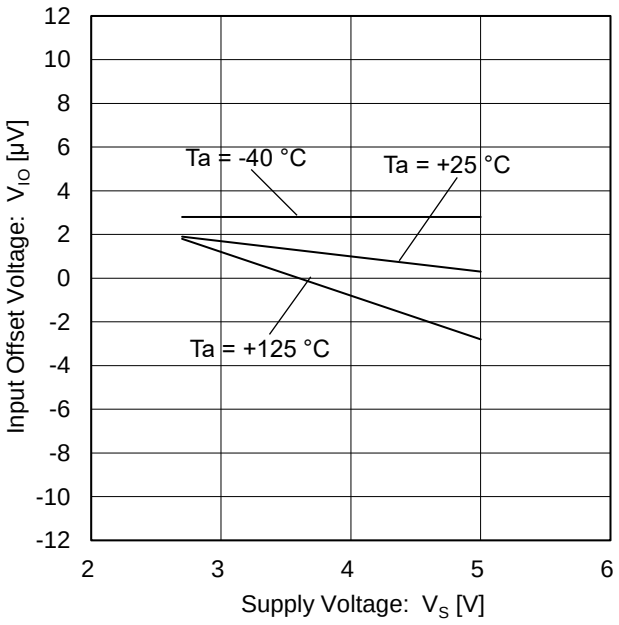


Figure 11. Input Offset Voltage vs Supply Voltage

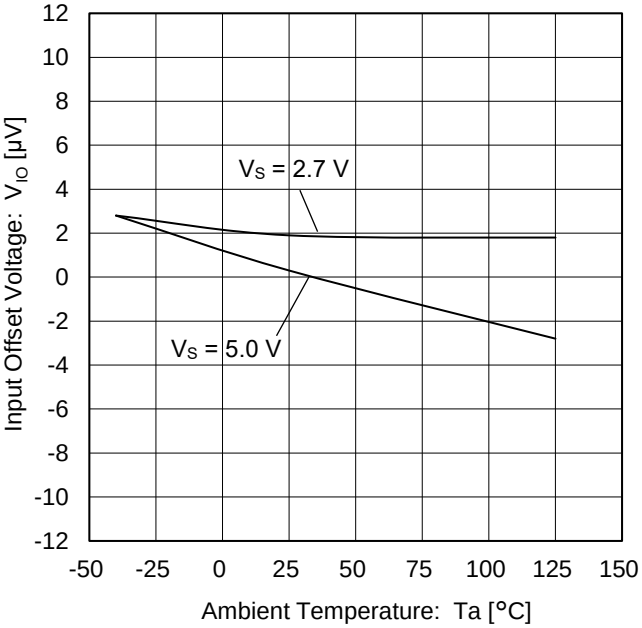


Figure 12. Input Offset Voltage vs Ambient Temperature

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
V_{SS} = 0 V

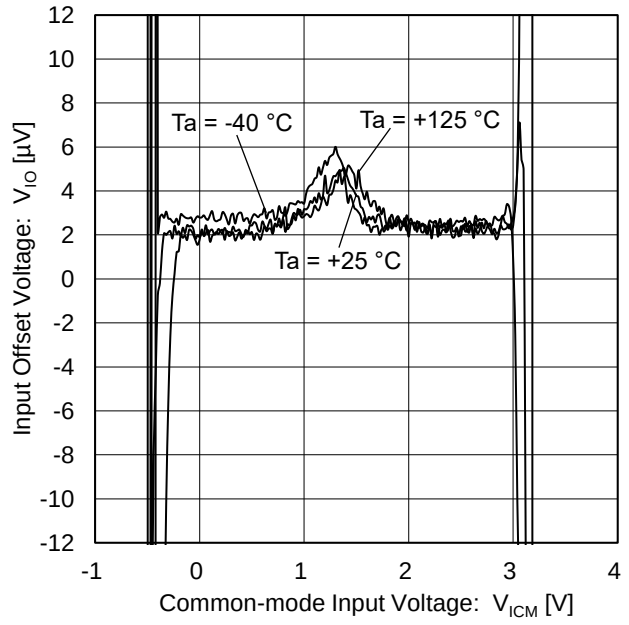


Figure 13. Input Offset Voltage vs Common-mode Input Voltage (V_S = 2.7 V)

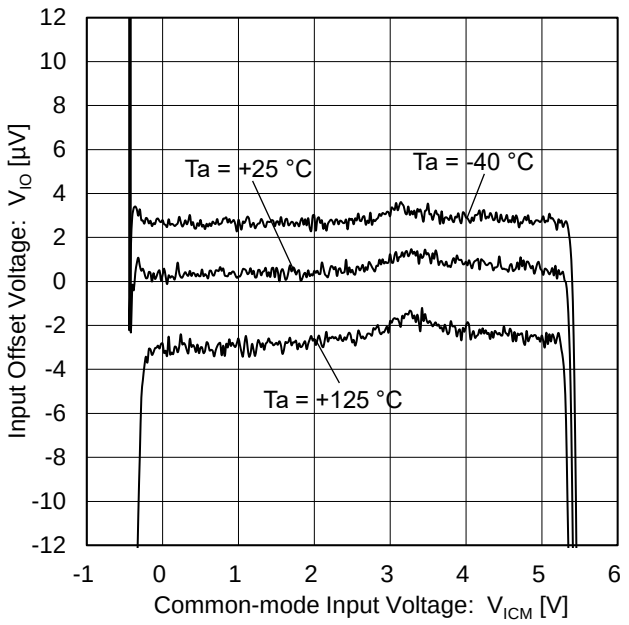


Figure 14. Input Offset Voltage vs Common-mode Input Voltage (V_S = 5.0 V)

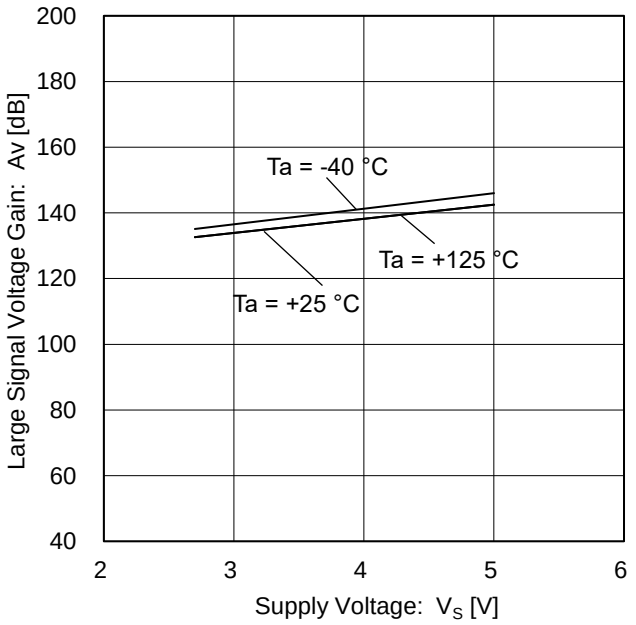


Figure 15. Large Signal Voltage Gain vs Supply Voltage (R_L = 10 kΩ)

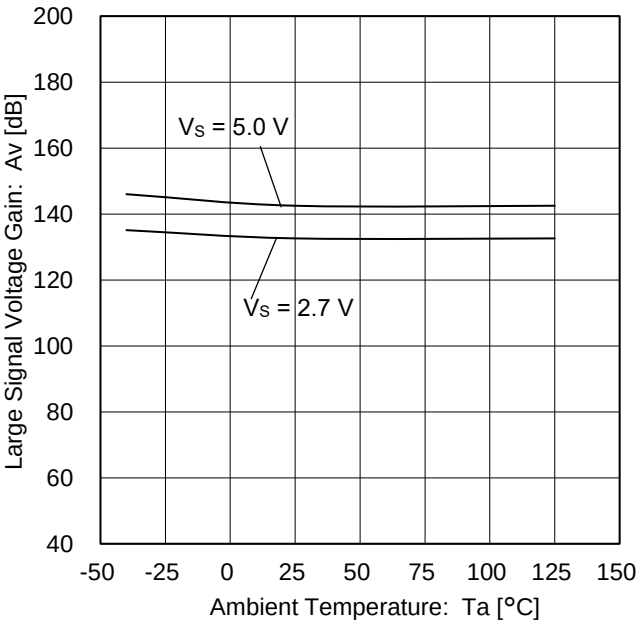


Figure 16. Large Signal Voltage Gain vs Ambient Temperature (R_L = 10 kΩ)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
V_{SS} = 0 V

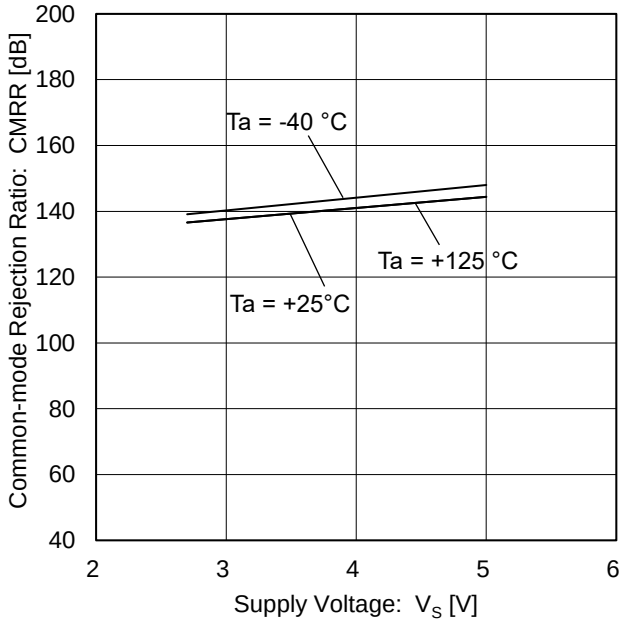


Figure 17. Common-mode Rejection Ratio vs Supply Voltage

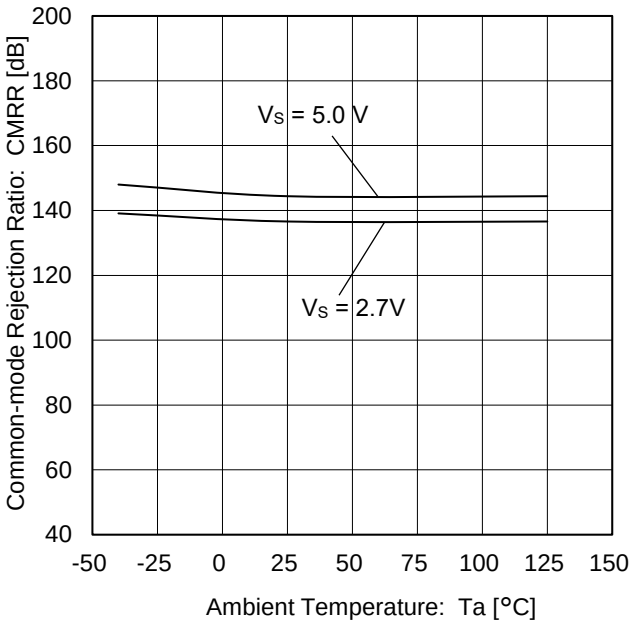


Figure 18. Common-mode Rejection Ratio vs Ambient Temperature

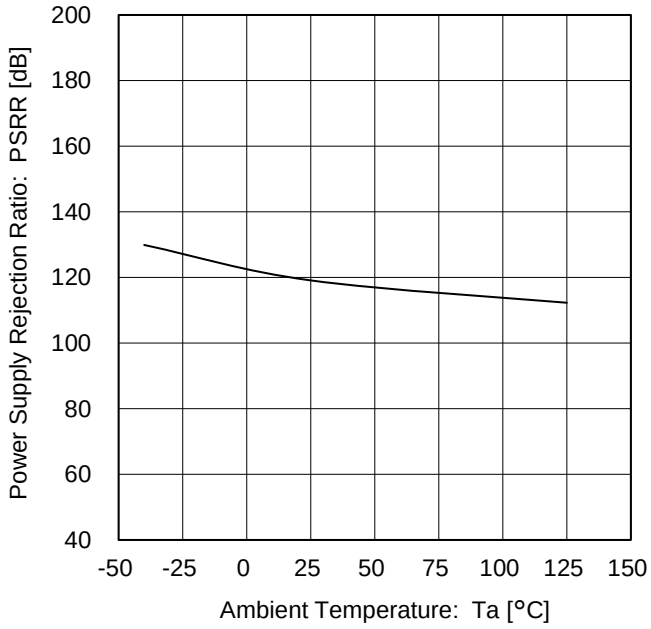


Figure 19. Power Supply Rejection Ratio vs Ambient Temperature

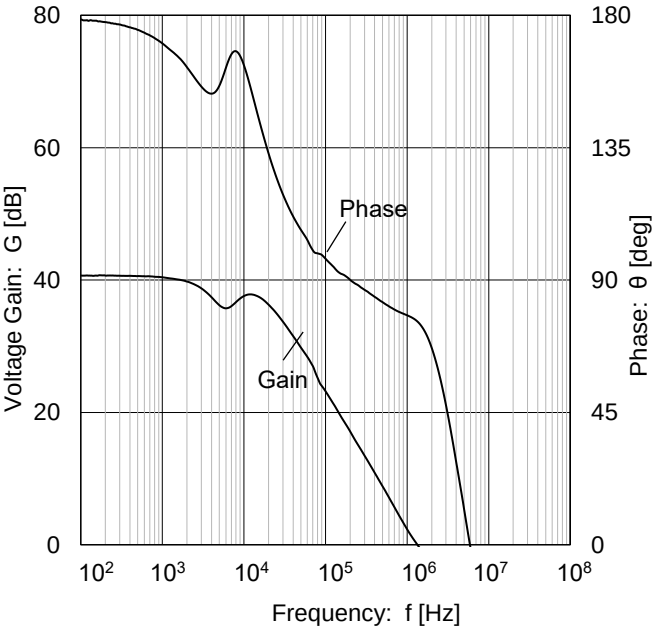


Figure 20. Voltage Gain, Phase vs Frequency (V_S = 5.0 V)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Typical Performance Curves - continued
V_{SS} = 0 V

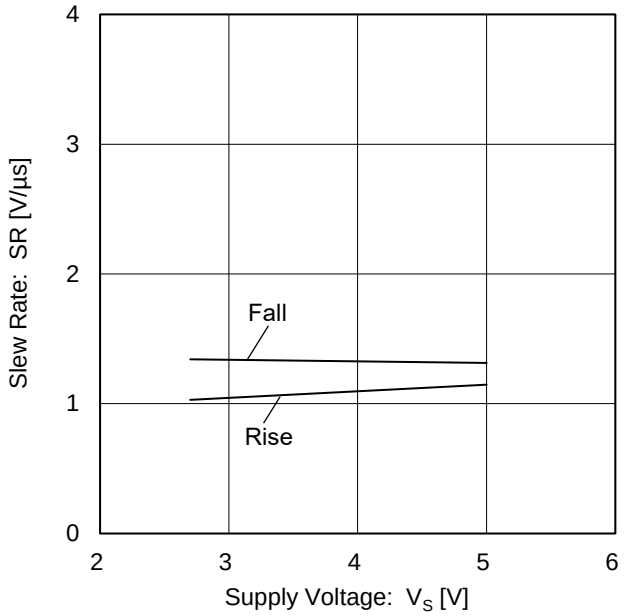


Figure 21. Slew Rate vs Supply Voltage

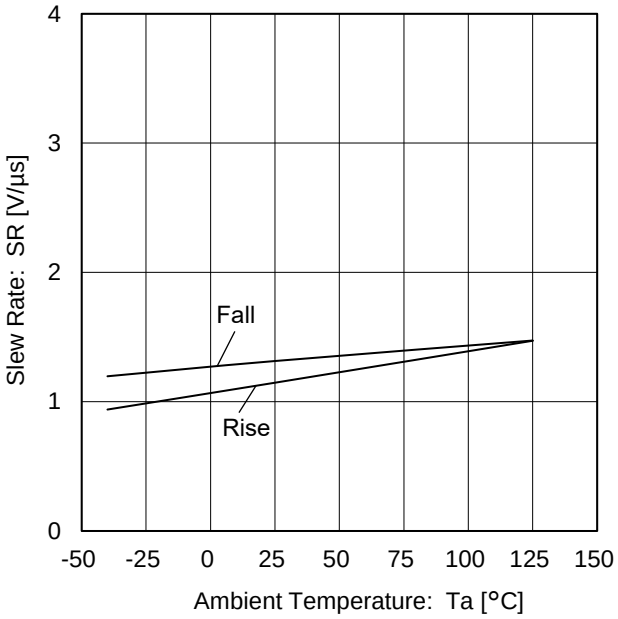


Figure 22. Slew Rate vs Ambient Temperature
(V_S = 5.0 V)

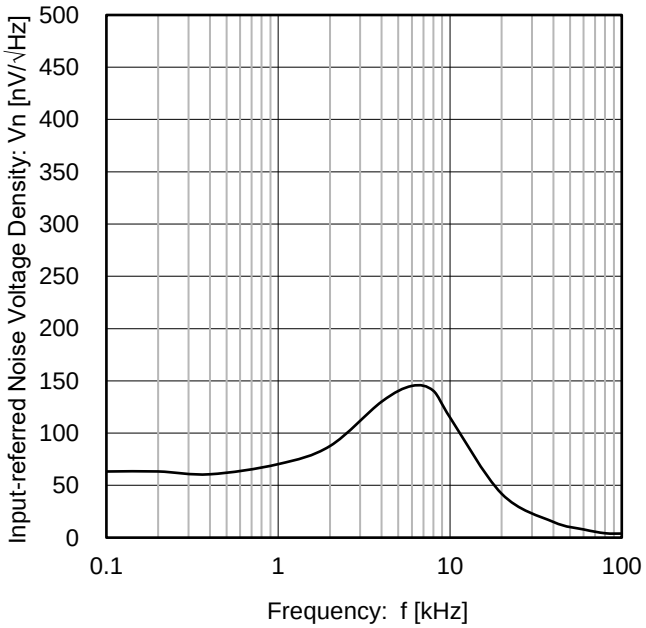


Figure 23. Input-referred Noise Voltage Density vs Frequency
(V_S = 5.0 V)

(Note) The above data are measurement value of typical sample; it is not guaranteed.

Application Examples

○Voltage Follower

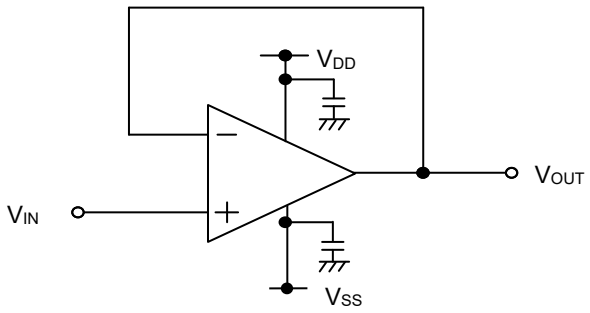


Figure 24. Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage due to high input impedance and low output impedance. Computation for output voltage is shown below.

$$V_{OUT} = V_{IN}$$

○Inverting Amplifier

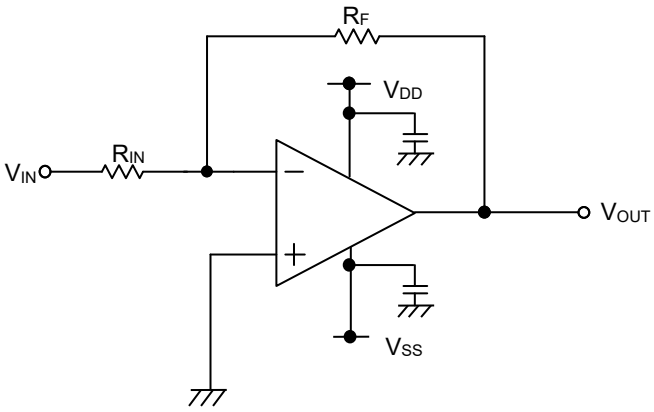


Figure 25. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain which depends on the ratio of R_{IN} and R_F, and then it outputs phase-inverted voltage (V_{OUT}). The output voltage is shown in the next expression.

$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

This circuit has input impedance equal to R_{IN}.

○Non-inverting Amplifier

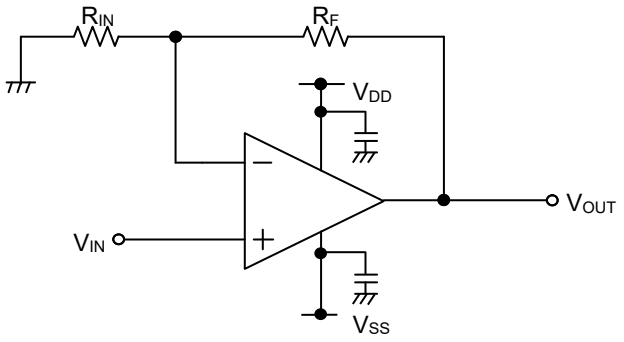


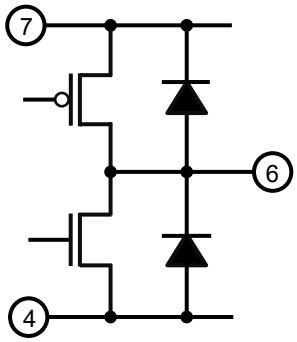
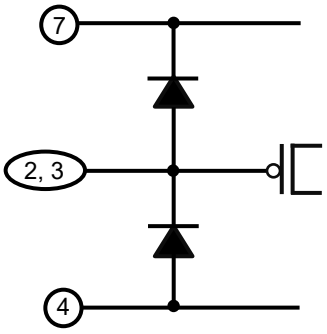
Figure 26. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_{IN} and R_F. The output voltage (V_{OUT}) is in-phase with the input voltage and is shown in the next expression.

$$V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Description	Equivalence Circuit
6	OUT	Output	
2 3	-IN +IN	Input	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

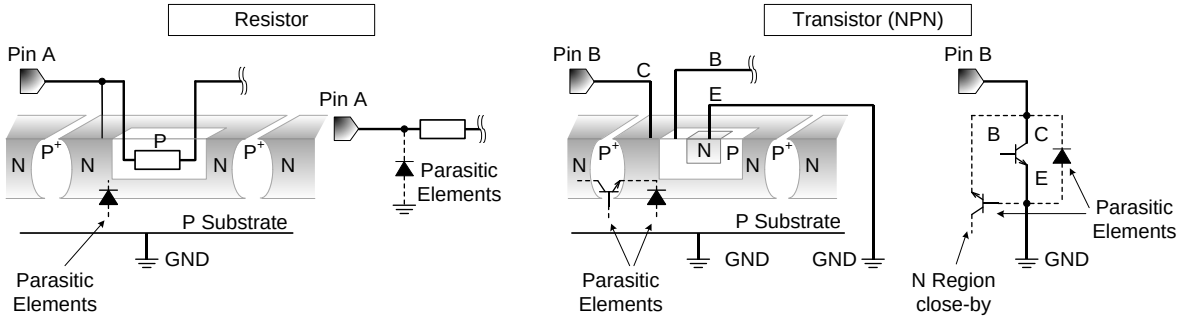
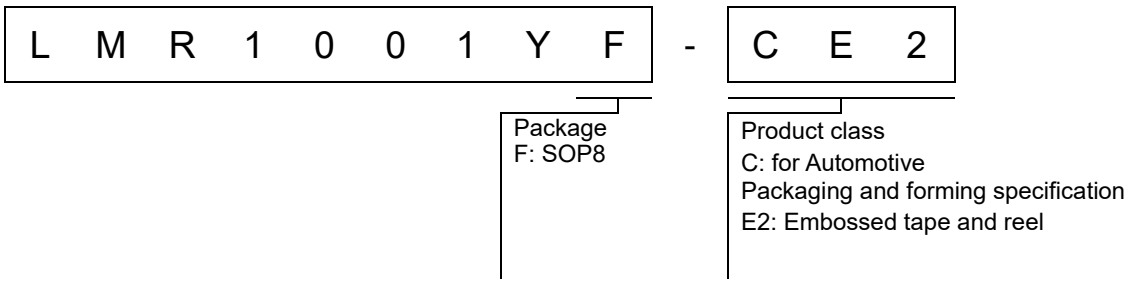


Figure 27. Example of monolithic IC structure

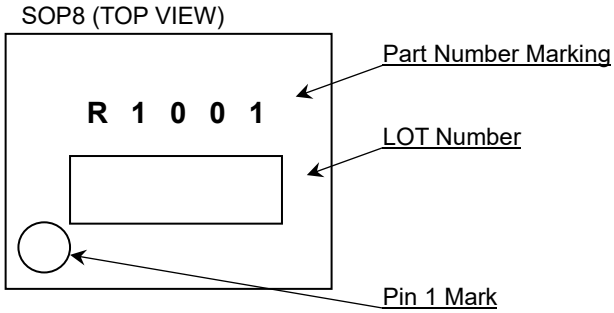
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

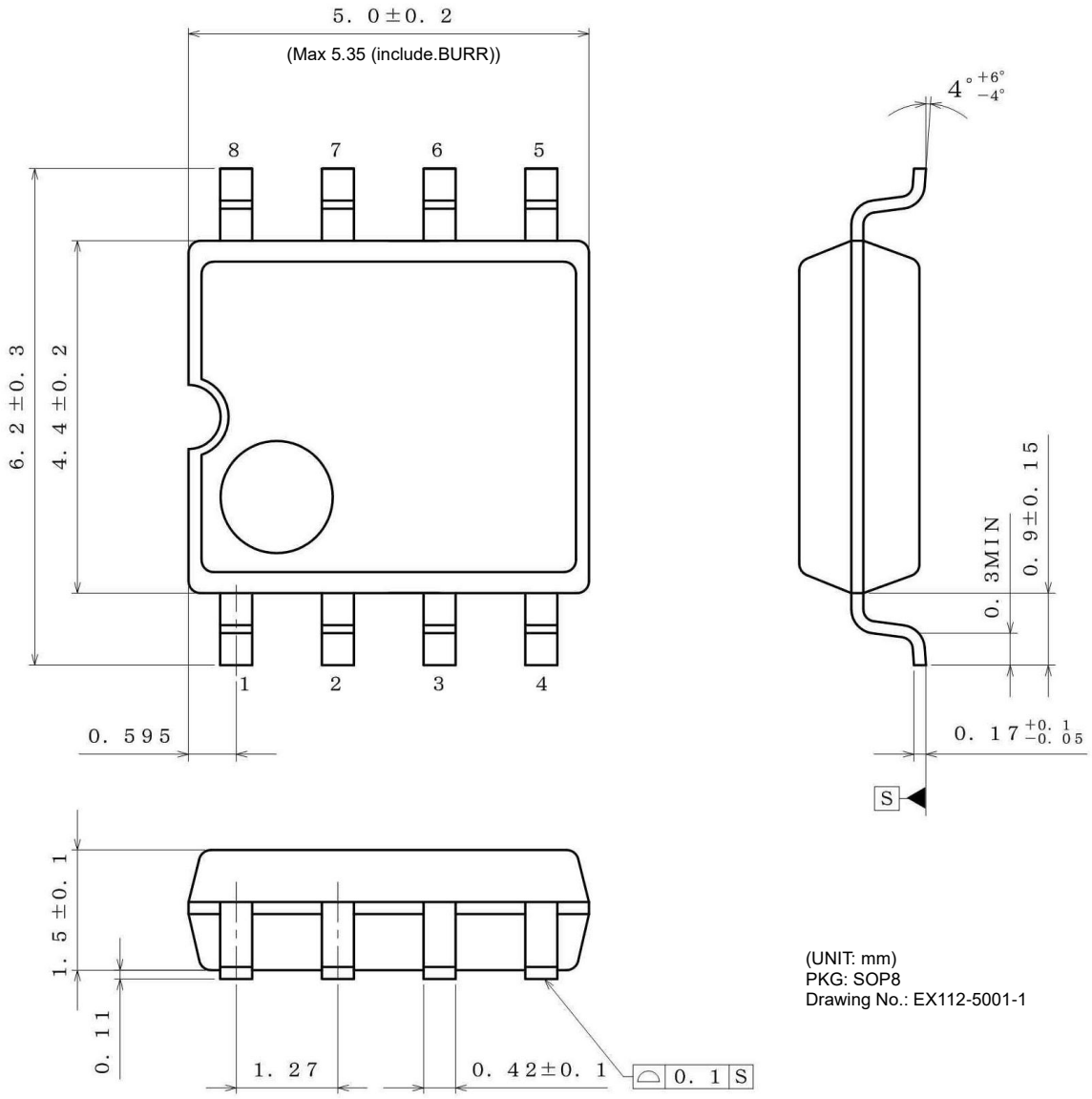


Marking Diagram



Physical Dimension and Packing Information

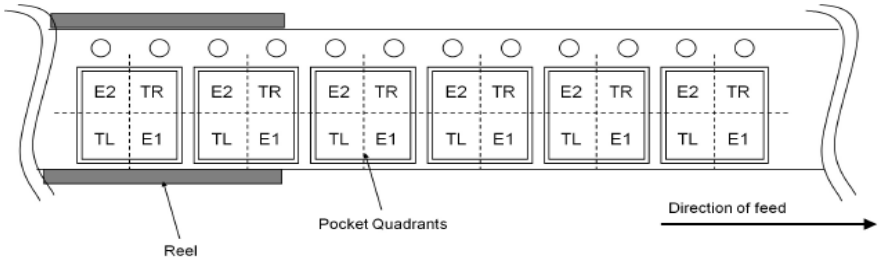
Package Name	SOP8



(UNIT: mm)
PKG: SOP8
Drawing No.: EX112-5001-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
16.Jan.2023	001	New Release