

# **Application Note**

# SPICE Models: ROHM Voltage Detector ICs



BD48 G/FVE, BD49 G/FVE, BD52 G/FVE, BD53 G/FVE, BD45 G, BD46 G G, BU48 G/FVE/F, BU49 G/FVE/F, BU42 G/FVE/F, BU43 G/FVE/F, BD47 G

No.10006EAY01

### 1. INTRODUCTION

#### 1.1 SPICE

SPICE is a general-purpose circuit-simulation program for nonlinear DC, nonlinear transient, and linear AC analysis. It solves network equations for node voltages and was designed to solve both linear and nonlinear electrical circuits. SPICE models simulate a variety of circuits with high accuracy, from switching power supplies to RAM cells and sense amplifiers. A variety of circuit components are supported, including resistors, capacitors, inductors, mutual inductors, dependent/independent voltage/current sources, transmission lines, and common semiconductor devices such as diodes, bipolar junction transistors (BITs), junction field effect transistors (JFETs), metal-oxide-semiconductor field effect transistors (MOSFETs), and metal-semiconductor FETs (MESFETs).

#### 1.2 PSpice®

PSpice® is a SPICE analog circuit and digital logic simulation software that runs on personal computers.

#### 1.3 OrCAD® PSpice 9.1

OrCAD® PSpice simulates analog-only circuits. After preparing a design for simulation, OrCAD Capture generates a circuit file set, which contains the circuit netlist and analysis commands. The circuit file set is read by PSpice A/D for simulation. PSpice A/D formulates these into meaningful graphical plots, which can be marked for display directly from the schematic page.

OrCAD PSpice 9.1 (Student Version) is PSpice simulation software that is available for free but with certain limitations imposed on the libraries and functionality. A fully functional version can be purchased from Cadence Design Systems, Inc.

#### 1.4 SPICE Models: ROHM Voltage Detector ICs

ROHM SPICE model is made by typical data, and the manufacturing dispersions are not included.

Moreover, it does not guarantee all of the simulation result of execution by using this.

This model is being supplied as a aid to confirm the validity of a design approach and help to select surrounding component values.

While it reflects reasonably close to similarity to the actual device in terms of performance, it is not suggested as a replacement for breadboarding.

Simulation should be used as a forerunner or a supplement to a traditional lab testing.

Note:

OrCAD is a registered trademark of Cadence Design Systems, Inc. PSpice is a registered trademark of Cadence Design Systems, Inc.

### 2. SIMULATION CIRCUIT SETUP

### 2.1 Model File

A model defines the electrical behavior of a part. On a schematic page, this correspondence is defined by a part's implementation property, which is assigned the model name.

Depending on the device type that it describes, a model is defined as one of the following:

- · a model parameter set
- a subcircuit netlist

Both ways of defining a model are text-based, with specific rules of syntax.

### 2.2 Model Libraries

Device model and subcircuit definitions are organized into model libraries. Model libraries are text files that contain one or more model definitions. Typically, model library names have a .LIB extension.

Most model libraries contain models of similar type. For vendor-supplied models, libraries are also partitioned by manufacturer.

Two files are used, the LIB file and the OLB file. The LIB file holds the characteristics of the model while the OLB file contains the model symbols.

Although the LIB file alone is enough, circuits cannot be generated using OrCAD Capture. Instead, the netlist file must be used in PSpice A/D.

In contrast, having an OLB file of the model enables the user to make circuits in the OrCAD Capture, resulting in greater convenience and better circuit conceptualization.

The sample LIB and OLB model files used in the setup, simulation, and evaluation examples with OrCAD PSpice are BU4229.LIB and BU4229.OLB. These are PSpice models of a voltage detector IC manufactured by ROHM.

### 2.3 Simulation Setup

To start simulation setup, select the OrCAD Capture application.



### 2.3.1 Starting the Design Project

GrCAD Capture	
File View Edit Options V	
New Deen	Project
Save Ctrl+S Save As	Library VHDL File Text File
Print Preview Print Ctrl+P Print Setup	
Import Design Export Design	
Exit	
Create new project.	Session Log

Create a new project and enter the necessary parameters such as project name, project type, and project directory. In this example, the project name is BU4229\_SIM\_test and the type of project is Analog or Mixed A/D.

New Project		X
Name BU4229_SIM Create a New Project Using Analog or Mixed A/D Analog or Mixed A/D PC Board Wizard PC Board Wizard Programmable Logic Wizard Construction	Mixed A/D new project	OK Cancel Help w Users wew Analog or 0 project. The ct may be blank from an existing
ENBU4229_SIM	>	Browse

Next, create a blank project

Create PSpice Project	
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<b></b>	Browse
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	Help

### 2.3.2 Project Directory

Select the target directory for saving the project. In this example we will be saving our project on drive E:

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	2
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Create a project folder, such as BU4229\_SIM.

Select Directory	
Directories: e:\	ОК
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Drives:	Click this button
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#### BD48□G/FVE,BD49□G/FVE,BD52□G/FVE,BD53□G/FVE, BD45□□G,BD46□□G,BU48□G/FVE/F,BU49□G/FVE/F, BU42□G/FVE/F,BU43□G/FVE/F,BD47□G

Create Directory	×
Current Directory: E:\	ОК
Name: BU4229_SIM	Cancel
	Help

After creating the folder, select that folder then press OK

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BU4229_SIM	Help
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### 2.3.3 The OrCAD Capture Environment

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This is how OrCAD Capture will look like after successfully setting the project directory. The next step is to add parts to the circuit for simulation.

### 2.3.4 Adding Parts to the Schematic

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Parts may be added as shown or by simply pressing Shift+P. Parts can also be added by clicking on the Place Part button on the right tool bar.

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This is the Place Part window. Initially no libraries are included. Libraries need to be added for setup (i.e. the PSpice models for the BU4229).

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Place Part			X
Part:		_	ОК
, Part List:			Cancel
			Add Library
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Libraries: Design Cache	Graphic G flormal Convert		
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### 2.3.5 Adding Libraries

Place Part		
Part:		 ОК
Part List:		Cancel Add Library Remove Library Part Search Help
Libraries: Design Cache	Graphic Convert Packaging Parts per Pkg: 1 Part: Type:	nep

To add Libraries, click on the Add Library button as shown above.

Select the OLB files required for simulation. Normally, sources.OLB and analog.OLB are necessary, which are a shared OLB file of OrCAD containing voltage/current sources and analog devices such as resistors and capacitors. Go to the Capture/Library/PSpice folder (default) in the OrCAD PSpice directory or to the relevant folder.

#### BD48□G/FVE,BD49□G/FVE,BD52□G/FVE,BD53□G/FVE, BD45□□G,BD46□□G,BU48□G/FVE/F,BU49□G/FVE/F, BU42□G/FVE/F,BU43□G/FVE/F,BD47□G

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From the Capture/Library/PSpice folder, select analog.OLB and source.OLB then press the Open button. (Press Ctrl and click on the files to select them both)

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File name:	"source.olb" "analog.olb"
Files of type:	Capture Library(*.olb)
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This is what the Place Part window will look like after adding the libraries. You may see a list of parts from each library.

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Next, add the model library of the PSpice model for simulation. It is easier if the model files are located in the Project Folder. (E.g. BU4229.LIB and BU4229.OLB in E:¥BU4229\_SIM) Then add the BU4229.OLB library.

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The parts list of the BU4229 library should now be displayed, along with (possibly) other associated parts.

Place Part			
Part: BU4229			ОК
Part List:			Cancel
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		- 1	Part Search
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Simulation setup can now begin.

### 2.3.6 Simulation Setup

Add parts in the OrCAD Capture Environment.

Place Part			×
Part: BU4229		-	ОК
Part List: BU4229 COMP1 COMP2			Cancel Add Library Remove Library Part Search
Libraries: ANALOG BU4229 Design Cache SOURCE	Graphic Normal Convert Packaging Parts per Pkg: 1 Part: Type: Homogeneous		Help

#### BD48□G/FVE,BD49□G/FVE,BD52□G/FVE,BD53□G/FVE, BD45□□G,BD46□□G,BU48□G/FVE/F,BU49□G/FVE/F, BU42□G/FVE/F,BU43□G/FVE/F,BD47□G

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Next, add voltage sources and other components like resistors and capacitors. DC Voltage (VDC) and DC Current (IDC) sources can be found in the Sources library while passive devices like resistors (R) and capacitors (C) are located in the Analog library.

Place the parts. To rotate the device, right-click on the device and select Rotate.

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Complete the necessary wiring as shown below. In this case the simulation will be run to determine the detection voltage. (Detection Voltage Parameter)

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Place a ground by clicking on the GND button in the right tool box.



To set the values of the external components (i.e. resistor, capacitor, DC voltage source), click on the device then right-click and choose Edit Properties. For this example, R2 will be set to 470Kohms, C1 to 100nF, and V1 to 5V.

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The Property Editor window will appear. Change the value of the part by typing the value with the proper prefix unit (i.e. k for kilo and p for pico).

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Return to the schematic page by clicking on Window tab in the main pull-down menu.

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The values can also be changed by double-clicking on the value displayed.

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Enter the value in the popup box, then press OK.

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Display Format Do Not Display Value Only Name and Value Name Only Both if Value Exists	Color
ОК	Cancel Help

### 2.3.7 Creating a Simulation Profile

To create a simulation profile, click on the PSpice tab in the main menu and select New Simulation Profile.

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Enter a name for the simulation profile. In this example the name is BU4229\_Vdet.

New Simulation	
Name:	Create
BU4229_Vdet	
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Inherit From:	
none	
Root Schematic: SCHEMATIC1	

In the Simulation Settings window, select DC Sweep under Analysis type in order to evaluate Vdet.

Simulation Settings - BU4229	P_Vdet 🛛 🔀
	Libraries Stimulus Options Data Collection Probe Window Run to time: 1000ns seconds (TSTOP) Start saving data after: 0 seconds Transient options Maximum step size: seconds Skip the initial transient bias point calculation (SKIPBP) Output File Options
	OK Cancel Apply Help



Enter the required settings. In this case the DC voltage source V1 will be swept linearly from 5V to 0V with a stepping voltage of 0.1mV.

Simulation Settings - BU4	229_V det 🛛 🔀
General Analysis Include F	iles   Libraries   Stimulus   Options   Data Collection   Probe Window
Analysis type: DC Sweep Options: Primary Sweep Secondary Sweep Monte Carlo/Worst Case Parametric Sweep	Sweep voriable       Name:       V1         Voltage source       Name:       V1         Current source       Model type:       Image: Comparent type:         Global parameter       Model name:       Image: Comparent type: Comparent t
☐ Temperature (Sweep) ☐ Save Bias Point ☐ Load Bias Point	Sweep type Linear C Logarithmic Decade Increment: 0.1m
	C Value list
	OK Cancel Apply Help

Simulation Settings - BU4229_Vdet			
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Library files			
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	Add to Design		
	Edit		
	Change		
Library Path			
"d:\OrCAD_Demo\PSpice\UserLib";"d:\OrCAD_Demo\C Browse			
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Locate the model file BU4229.LIB

Open			? 🗙
Look in: 🗀	BU4229_SIM		* 🎫 🕶
BU4229			
File name:			Open
Files of type:	Library Files (*.lib)	•	Cancel

Add the library to the design then press OK.

Simulation Settings - BU4229_Vdet			
General Analysis Include Files Libraries Stimulus Options Data Collection Probe Window			
Filename:			
E:\BU4229_SIM\BU4229.lib Browse			
Library files			
.\bu4229.lib nom.lib* Add as Global			
Add to Design			
Edit			
Change			
Library Path			
"d:\OrCAD_Demo\PSpice\UserLib";"d:\OrCAD_Demo\C Browse			
OK Cancel Apply Help			

Simulation is now ready to begin.

### 2.3.8 Running the Simulation

To run the simulation, go to PSpice tab in the main menu and select Run.

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Place Optimizer Parameters Run Optimizer	<u>U1</u> 470К — <u>Т</u>
Markers 1 Bias Points	VDD VOUT 0 + 1 BU4229
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Run PSpice simulation for active profile.	0 items selected   5cale=200% X=3.20 Y=0.00 // 🖳

OrCAD PSpice A/D will automatically load and run the simulation.

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Simulation running		
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** Profile: "SCHEMATICI-BU4229_Vdet" [E:\BU4229_SIM\bu4229_sim-SC Reading and checking circuit Start = 5 V_V1 = 2.661	End = 0	Progress of simulation
Circuit read in and checked, no errors DC Analysis		
Analysis (Watch ) Devices /		
For Help, press F1	V_V1 = 2.661	46%

### 3. EVALUATION OF RESULTS

A completed simulation will look like this. Note the 100% shown on the progress bar.

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Image: Second	🖹 🔻 🚅 🎥 🎒 🐰 🖻 💼 🗠 🗠 🛛 SCHEMATICI-BU4229_Vdet	t II	
Image: State and Checking circuit       Image: State and Checking circuit         Image: State and Checking circuit       State = 5       V_VI = 100.0E-06       End = 0	� � � �   Ⅲ 蚯 ♥ 目    ☆ 寥 ▽ ♂    杰 孝 孝 埣 オ	<b>养蒜晶蛋苷</b> 型	
Image: State and Checking circuit       Image: State and Checking Circuit         Image: State and Checking Circuit       State = 5       V_VI = 100.0E-06       End = 0			
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B       00       0.50       1.60       1.50       2.60       2.50       3.60       3.50       4.60       4.50       5.60         U       0.50       1.60       1.50       2.60       2.50       3.60       3.50       4.60       4.50       5.60         U       0.01       0.01       0.00 <td></td> <td></td> <td></td>			
Bud223_sim         Image: Scheme and Decked, no errors         DC Analysis         D C Analysis         D C Analysis         D C Analysis			
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■       UU1         ■       No recognized product configuration selected.         ■       Pro-Roline "SOHEMATIC1-8U4229_Vdet" [E:\8U4229_SIM\bu4229_sim         Reading and checking circuit       Image: Sole Charles and checked, no errors         DC Analysis       DC Analysis         DC Analysis       Finished			
■       UU1         ■       No recognized product configuration selected.         ■       Pro-Roline "SOHEMATIC1-8U4229_Vdet" [E:\8U4229_SIM\bu4229_sim         Reading and checking circuit       Image: Sole Charles and checked, no errors         DC Analysis       DC Analysis         DC Analysis       Finished			
■       UU1         ■       No recognized product configuration selected.         ■       Pro-Roline "SOHEMATIC1-8U4229_Vdet" [E:\8U4229_SIM\bu4229_sim         Reading and checking circuit       Image: Sole Charles and checked, no errors         DC Analysis       DC Analysis         DC Analysis       Finished			
Image: Start and Start an	0V 0.5V 1.0V 1.5V 2	2.00 2.50 3.00 3.50 4.00 4	+.50 5.00
No recognized product configuration selected.     ** Profile: "SCHEMATICI-BU4229_Vdet" [E:\8U4229_SIM\bu4229_sim Reading and checking circuit Circuit read in and checked, no errors DC Analysis DC Analysis finished     Image: Start = 5     V_V1 = 100.0E-06     End = 0		V_V1	
Image: SCHEMATICI-BU4229_Vdet" [E:\BU4229_SIM\bu4229_sim         Reading and checking circuit         Circuit read in and checked, no errors         DC Analysis         DC Analysis finished    Start = 5 V_V1 = 100.0E-06 End = 0	💆 bu4229_sim		
Reading and checking circuit       Circuit read in and checked, no errors       DC Analysis       DC Analysis finished	No recognized product configuration selected.		
DC Analysis DC Analysis finished	Reading and checking circuit		
	DC Analysis St	tart = 5 V_V1 = 100.0E-06 End = 0	
	Simulation complete	B Andria (Wester) During (	
	For Help, press F1		

### 3.1 Adding a Trace or Output

SCHEMATIC1-BU4229_Vdet - OrCAD PS	Spice A/D Demo - [b	u4229_sim-SCH	IEMATIC1-B (	_ 🗆 🔀
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	V_V1			
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No recognized product configuration sele ** Profile: "SCHEMATIC1-BU4229 Vdet"	×			
Reading and checking circuit				
Circuit read in and checked, no errors DC Analysis	Start = 5	V_V1 = 10	0.0E-06	Enc
DC Analysis finished Simulation complete	<			>
		Watch \ Devices /		
Add trace[s] to the selected plot	V_V1 = 100.0E-06	100%		

Select the pin, node, or branch for monitoring/measurement. In this case the VOUT pin is selected [V(U1:VOUT)].

#### BD48□G/FVE,BD49□G/FVE,BD52□G/FVE,BD53□G/FVE, BD45□□G,BD46□□G,BU48□G/FVE/F,BU49□G/FVE/F, BU42□G/FVE/F,BU43□G/FVE/F,BD47□G

Simulation Output Variables	35	Functions or Macros	
×		Analog Operators and Fun	ctions 💌
IS(X_U1.Mdrv) IS(X_U1.Mout) IS(X_U1.X1.M6) IS(X_U1.X1.M7) IS(X_U1.X52.M4) V(0) V(C1:1) V(C1:2) V(GND) V(N00014) V(N00017) V(N00055) V(R1:1) V(R1:2) V(U1:CT) V(U1:GND) V(U1:GND) V(U1:YDD) V(V1:+) V(V1:-)	<ul> <li>Analog</li> <li>Digital</li> <li>Voltages</li> <li>Currents</li> <li>Noise (V<sup>2</sup>/Hz)</li> <li>Alias Names</li> <li>Subcircuit Nodes</li> </ul>	# () * + - / @ ABS() ARCTAN() ATAN() AVG() AVG() AVG() AVG() D() D() DB() ENVMAX(,) ENVMIN(,) EXP() G() IMG()	
V(X_U1.10) V(X_U1.11) V(X_U1.14) V(X_U1.15) Full List	171 variables listed	LOG() LOG10() M() MAX()	~

The OrCAD PSpice A/D should look like this.





### 3.2 Alternate Display

Enlarge the graph to full screen by clicking on the Alternate Display button.



It should look like this.



### 3.3 Measurement

To begin measurement, first enable the Cursor by clicking on the Toggle cursor button (shown below).



The cursor will appear, with the coordinates shown in a small window. Navigate to the desired point. In this example we will measure the threshold voltage.



Zooming is possible by selecting the area and pressing Ctrl+A. For this measurement the cursor is placed midway on the VOUT drop (VDD sweep from 5V to 0V).



The threshold voltage can be found by looking at the coordinates of the cursor. In this example the threshold voltage is at 2.9001V of VDD.

### 3.4 Annotate Measurement Values



To add an annotation of the measurement, click on the Mark Label button shown above. Ensure that the cursor is at the desired measurement point before making the annotation. Otherwise, the annotation will be incorrect. The annotation will display the coordinates of the cursor.



To fit the graph for viewing, go to View tab then select Fit under Zoom.

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Zoom to show all	traces and labels	V_V1 = 100.0E-06	100%



A fit view of the graph is shown below.



From the simulation results, VDET of the BU4229 is verified to be 2.9V with VOUT=470k $\Omega$  pulled up to VDD, CT=100pF, with a VDD sweep from 5V to 0V.

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