

Power Management IC designed for “NXP® i.MX 8M Mini”

BD71847AMWV Frequently Asked Questions

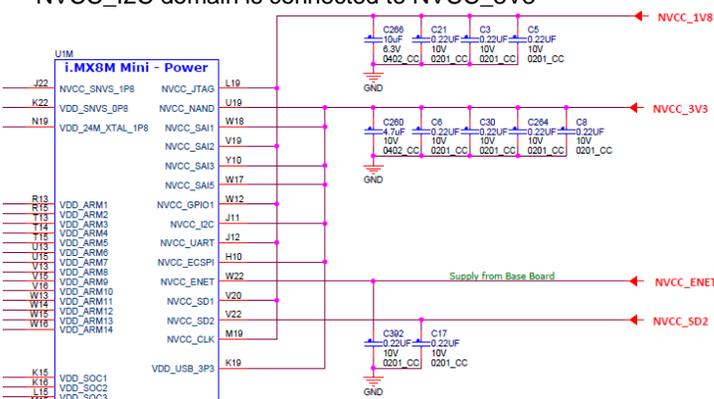
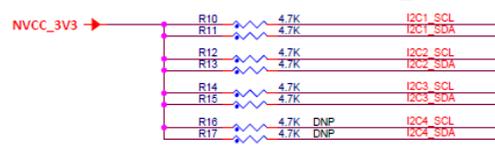
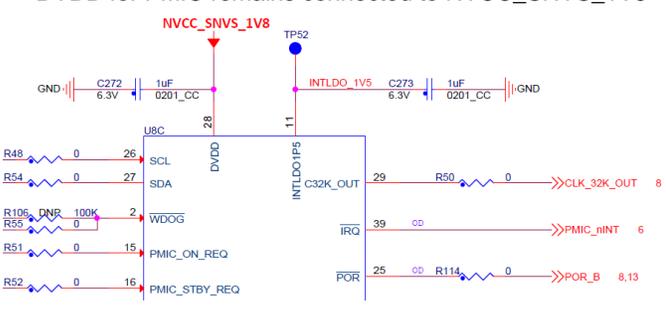
1. Introduction

This document question-and-answer format for BD71847AMWV which is a Power Management IC for NXP i.MX 8M Mini System-on-Chip (SoC) platform.

2. Terminologies

Term	Definition
DCR	DC Resistance
DDR	Double Data Rate
I2C	Inter-Integrated Circuit
LDO	Low Dropout
PFM	Pulse-Frequency Modulation
PMIC	Power Management Integrate Circuit
PWM	Pulse-Width Modulation
RTC	Real-Time Clock
PWM	Pulse-Width Modulation
SoC	System-on-Chip
UVLO	Under Voltage Lock Out
VR	Voltage Regulator

3. Frequently Asked Questions

#	Category	Question	Answer
1	BUCK	Can the BUCK6 inductor be reduced from 1uH to 0.47uH? Is it for efficiency?	PMIC was designed under 1uH condition for the best ripple and transient response. If the degradations in ripple and transient response are acceptable, 0.47uH can be an option.
2	I2C	What is the I2C device/slave address of PMIC?	The device address is 0x4B. Please refer to Figure4-3 of I2C Device Addressing of the datasheet.
3	Package	What is the preferred connection for 4 corner pads?	4 corner pads are shorted to EXP-PAD internally. It is recommended to solder such corner pads to ground.
4	Product	What is the difference between BD71847MWV and BD71847AMWV?	Please refer to the technical document of "Errata information on product BD71847MWV" on the web site. BD71847MWV is no more available in mass production process.
5	I2C	May I need a 3.3V level shifter for the I2C interface if 3.3V components are requested to be connected to the SoC?	<p>3.3V as the pull up source is acceptable even if DVDD is 1.8V. But NVCC_I2C of the I2C domain in SoC should be 3.3V (the same voltage as the pull up source for PMIC) and DVDD in PMIC always needs to be 1.8V.</p> <ul style="list-style-type: none"> NVCC_I2C domain is connected to NVCC_3V3  <ul style="list-style-type: none"> I2C interface is pulled up to NVCC_3V3  <ul style="list-style-type: none"> DVDD for PMIC remains connected to NVCC_SNVs_1V8 

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6	IO	Can we apply 3.3V on power control signals: PWRON_B, PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, RTC_RESET_B, POR_B if DVDD=1.8V?	Yes. 3.3V is acceptable for driving the control signals.
7	BUCK	Why does the discharging of BUCK7 happen later than the discharging of the others power rails?	BUCK8 needs to be de-asserted earlier than BUCK7 for the memory requirement.
8	I2C	Is there any mechanism protecting not allowed I2C access to the PMIC registers?	As the secure I2C access function, PMIC prepares the REGLOCK register which prohibits the unexpected I2C access during the operation. I2C access is locked by the register as the default setting.
9	BUCK	Could BUCK5 support 0.95V for VDD_GPU/VDD_VPU and VDD_DRAM? According to the NXP datasheet, it defined 0.85V/0.9V/0.95V for VDD_GPU/VDD_VPU and VDD_DRAM.	BUCK5 supports 0.975V and not for 0.95V. But this situation is approved by NXP and addressed under the SoC datasheet.
10	BUCK Memory	How to I implement the different DDR memory application?	The output voltage for BUCK8 can be adjusted by U-Boot in the initial startup depending on the memory type in use. The voltage change handled by U-Boot is acceptable for PMIC because the validity in the power sequence is confirmed by NXP and no other sideband effects are found during their validation.
11	BUCK	How do I disable BUCK6 in hardware terms?	BUCK6 is initially ON as the default setting and its output voltage is monitored during the power sequence as an one of the triggers to de-assert POR_B, the power good signal to SoC. So it is not recommended to turn off BUCK6.
12	BUCK	Could BUCK6 act as a switch? Could it work in 100% duty cycle?	BUCK6 supports 100% max duty but there is the limitation for input range described as "headroom" in the datasheet. Please refer to the section in the datasheet for details.
13	Sequence	How can the start-up behavior be modified?	The way of the power state transition can be modified through the register of TRANS_COND0/1.
14	UVLO	Is it possible to modify the ULVO value?	No, it is the fixed value.
15	BUCK	According to the datasheet, BUCK7 requests only 22μF whereas all the other BUCKs will need 2x 22μF.	The difference comes from the I _{omax} requirements. 1.5A for BUCK7 is lower than 3A for others.
16	BUCK	Could output capacitor of each BUCK reduce to 1x22μF?	One output capacitor for cost saving is acceptable if BUCK work in forced PWM mode. After confirmation, BUCK output voltage accuracy is within SoC requirements under the PWM mode. However if higher efficiency in light load region is needed in the system, it is recommended to use 22uF x 2pcs to support PFM mode.
17	BUCK	Could BUCK6 inductor be removed when VSYS is 3.3V application?	To avoid the emergency shutdown in PMIC, 3.3V should be externally supplied to BUCK6_FB pin. But leakage current through the discharge resistor around 33mA will flow if 3.3V is directly supplied. This leakage current can be suppressed to add the series resistor to BUCK6_FB line. The maximum value is up to 60kohm.

#	Category	Question	Answer
18	System	How to power down the system via software?	<p>This depends on the operating system you are using. For Linux and Android, there are shell commands like “power off” or “shutdown” which will call several routines to store content and finally power down the system.</p> <p>One possibility for a power-down is to de-assert the PMIC_ON_REQ line. This will cause the PMIC to power down the rails according to the sequencing requirements. Such de-assertion can be achieved while writing to the SNVS_LPCR register, bit TOP and DP_EN, according to the NXP i.MX 8M Mini Reference Manual.</p> <p>For precise description of “power-down function” of the board support package including low-level driver, please contact the SoC manufacturer.</p>

4. Revision History

Date	Revision Number	Description
6 th .Sep.2019	001	First Release
26 th .Nov.2019	002	The answers for #1, 2, 3, and 5 are changed.
6 th .Dec.2019	003	Added #16.
7 th .Jan.2020	004	Added #17.
19 th .Mar.2020	005	Added #18.

Notes

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