Power Management / Power Supply IC

Power Supply Sequence Circuit with General Purpose Power Supply IC

When supplying an LSI or electrical equipment such as an FPGA or DSP with multiple power supply systems, the order of turning ON/OFF the power supplies may be specified. If this order is not followed, the equipment may not be turned ON normally or devices may be damaged. The order of turning ON/OFF the multiple power supply systems is referred to as a power supply sequence. A power supply sequence IC may be used as a dedicated device to control the power supply sequence. This application note proposes a circuit that accomplishes the power supply sequence without using any dedicated power supply sequence IC, by using general purpose power supply ICs that do not have the Power Good output or an output discharge function required for the sequence control.

Power supply sequence specification 1

In this example, we introduce the circuit design for the power supply sequence of 3 systems.
The specifications of the input and output voltages are shown below.

V_{IN}: 5.0V
V_{OUT1}: 1.2V
V_{OUT2}: 3.3V
V_{OUT3}: 1.5V

Figure 1-1 shows the power tree diagram. In this example, the circuit is configured with 3 power supply ICs. The power supply ICs are assumed to be switching regulators (DC/DC converters) or linear regulators (LDO). As a function of the power supply IC, an enable pin that can control the ON/OFF of the output is required.

The power shall be turned ON in the order of V_{OUT}1, 2, and 3, and be turned OFF in the order of V_{OUT}3, 2, and 1. Figure 1-2 shows the schematic diagram.

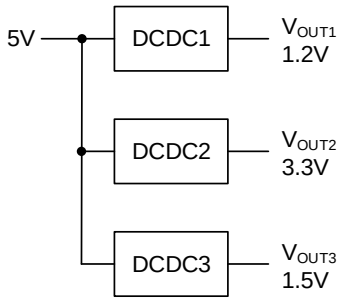

Figure 1-1. Power tree

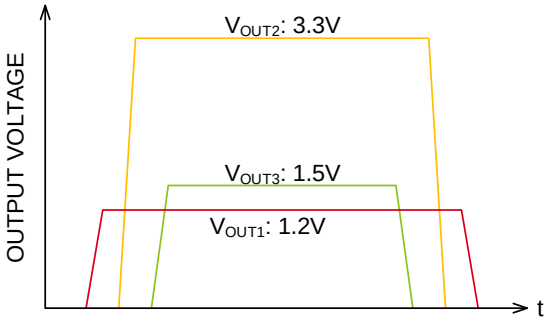

Figure 1-2. Schematic diagram of the power supply sequence

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Control block diagram 1

Figure 1-3 shows the control block diagram. DCDC 1, DCDC 2, and DCDC 3 are the power supply ICs of 3 systems. Each output is controlled by the enable (EN) pin. Power Good 1 and 2 monitor the output voltage of the DCDCs when the power is turned ON, and output the “High” signal to the DCDC to be turned ON next when the output voltage reaches the target voltage. Power Good 3 and 4 monitor the output voltage of the DCDCs when the power is turned OFF, and output the “Low” signal to the DCDC to be turned OFF next when the output voltage reaches the target voltage. The Discharge blocks ensure the normal operation of the power supply sequence by rapidly discharging the electric charges stored in the output capacitor of the DCDCs to decrease the voltage when the power is turned OFF. Note that, in this block diagram, the logic is designed as Active High between EN and VOUT of the DCDC blocks, between IN and PGOOD of the Power Good blocks, and between IN and OUT of the Discharge blocks. In addition, the PGOOD pin (output) of the Power Good blocks and the OUT pin of the Discharge blocks are of the open-collector or open-drain type.

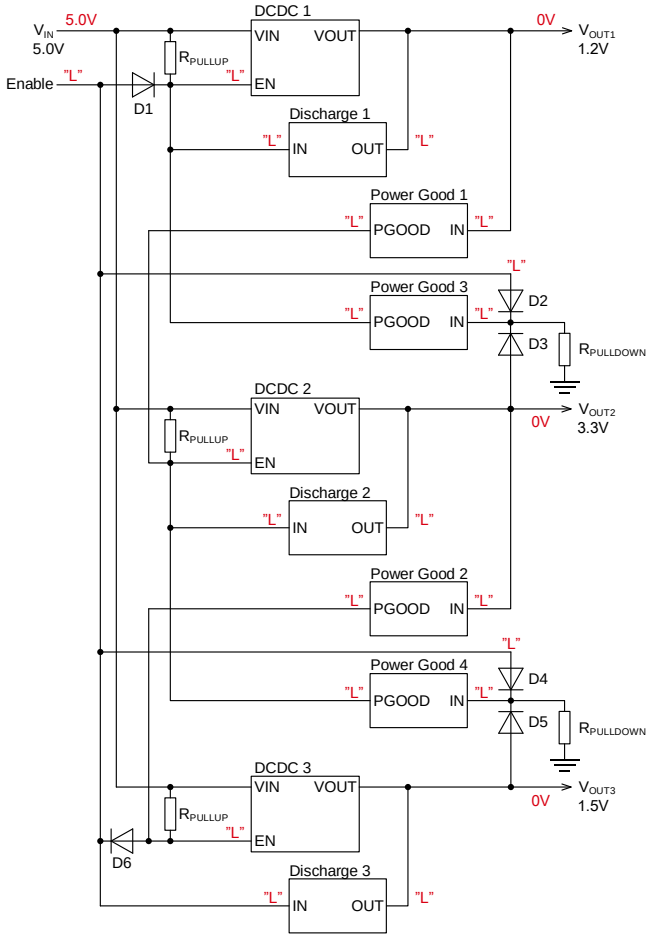

Figure 1-3. Control block diagram

Let’s follow the sequence operation in order. For the initial values, the Enable terminal is at the “Low” level and the outputs of the 3 DCDCs are zero. Figure 1-4 shows the operation in the first step when the power is turned ON. First, the “High” voltage is applied to the Enable terminal to turn ON the power supplies. The “High” voltage is applied to the EN pin of DCDC 1 via diode D1 and DCDC 1 is turned ON. When the output voltage of DCDC 1 increases from 0 V to 1.2 V, the output voltage of Power Good 1 switches from “Low” to “High”. Then, the voltage is applied to the EN pin of DCDC 2 on the next stage. In addition, since the “High” voltage is applied to the IN pins of Power Good 3 and Power Good 4 via diodes D2 and D4, the PGOOD pins (output) are maintained at high impedance.

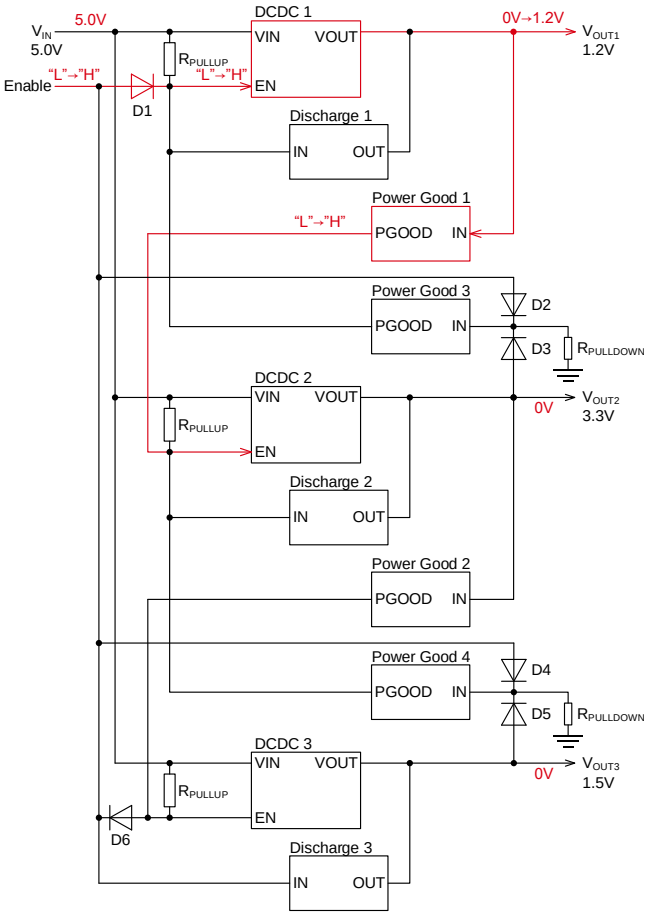

Figure 1-4. Operation when the power is turned ON: First step

Figure 1-5 shows the operation in the second step when the power is turned ON. The “High” voltage is applied to the EN pin of DCDC 2 and DCDC 2 is turned ON. When the output voltage of DCDC 2 increases from 0 V to 3.3 V, the output voltage of Power Good 2 switches from “Low” to “High”. Then, the voltage is applied to the EN pin of DCDC 3 on the next stage.

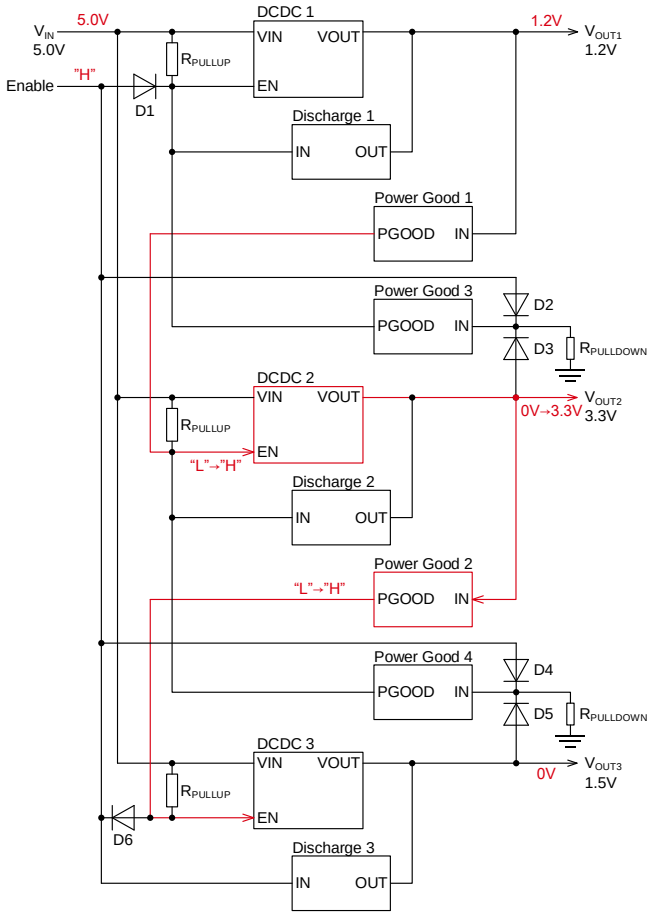

Figure 1-5. Operation when the power is turned ON: Second step

Figure 1-6 shows the operation in the third step when the power is turned ON. The “High” voltage is applied to the EN pin of DCDC 3 and DCDC 3 is turned ON. The output voltage of DCDC 3 increases from 0 V to 1.5 V and all of the 3 power supply systems are now operating.

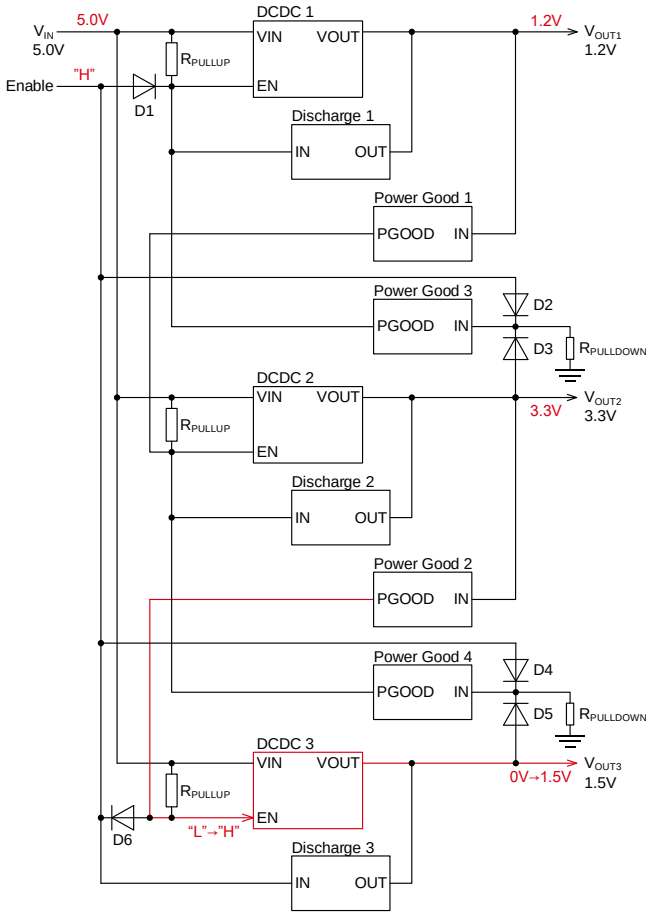

Figure 1-6. Operation when the power is turned ON: Third step

Figure 1-7 shows the state of the main nodes when the power supplies are operating.

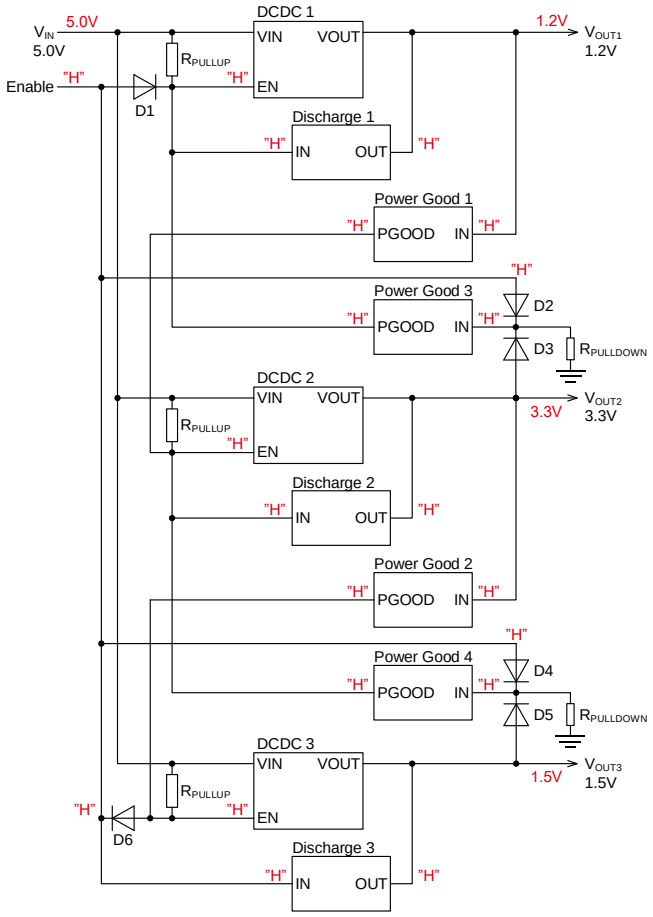

Figure 1-7. State of main nodes when the power supplies are operating

Next, we follow the sequence operation when the power is turned OFF in order. Figure 1-8 shows the operation in the first step when the power is turned OFF. First, the “Low” voltage is applied to the Enable terminal to turn OFF the power supplies. The “Low” voltage is applied to the EN pin of DCDC 3 via diode D6 and DCDC 3 is turned OFF. At the same time, the “Low” voltage is applied to the IN pin of Discharge 3 and the OUT pin switches to low impedance. This causes a rapid transition of the output voltage of DCDC 3 to 0 V. When the output voltage of DCDC 3 decreases, the output voltage of Power Good 4 switches from “High” to “Low”. Then, the voltage is applied to the EN pin of DCDC 2 and the IN pin of Discharge 2 on the previous stage.

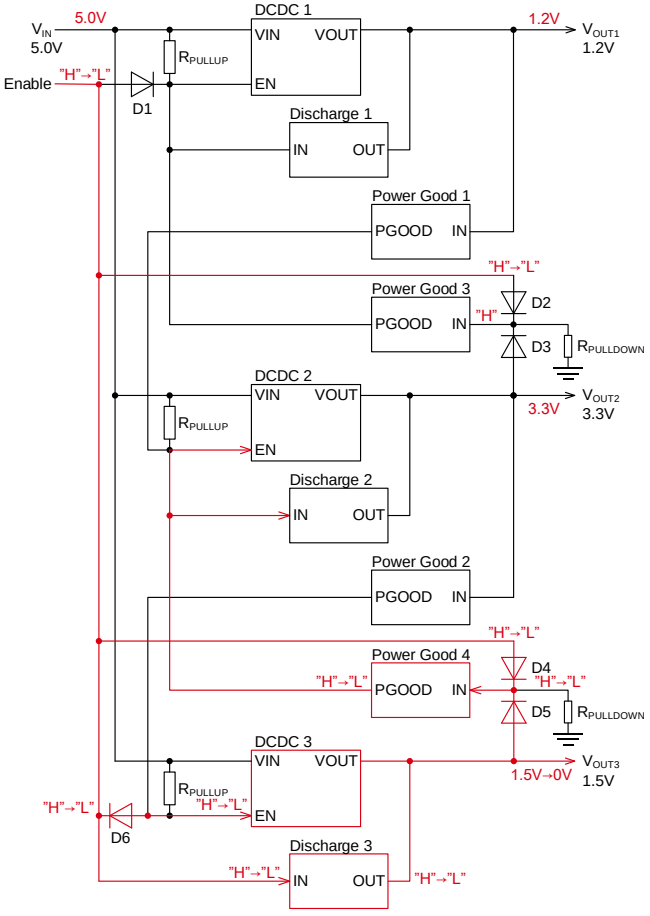

Figure 1-8. Operation when the power is turned OFF: First step

Figure 1-9 shows the operation in the second step when the power is turned OFF. The “Low” voltage is applied to the EN pin of DCDC 2 and DCDC 2 is turned OFF. At the same time, the “Low” voltage is applied to the IN pin of Discharge 2 and the OUT pin switches to low impedance. This causes a rapid transition of the output voltage of DCDC 2 to 0 V. When the output voltage of DCDC 2 decreases, the output voltage of Power Good 3 switches from “High” to “Low”. Then, the voltage is applied to the EN pin of DCDC 1 and the IN pin of Discharge 1 on the previous stage.

Figure 1-10 shows the operation in the third step when the power is turned OFF. The “Low” voltage is applied to the EN pin of DCDC 1 and DCDC 1 is turned OFF. At the same time, the “Low” voltage is applied to the IN pin of Discharge 1 and the OUT pin switches to low impedance. This causes a rapid transition of the output voltage of DCDC 1 to 0 V. All of the 3 power supply systems are now turned OFF.

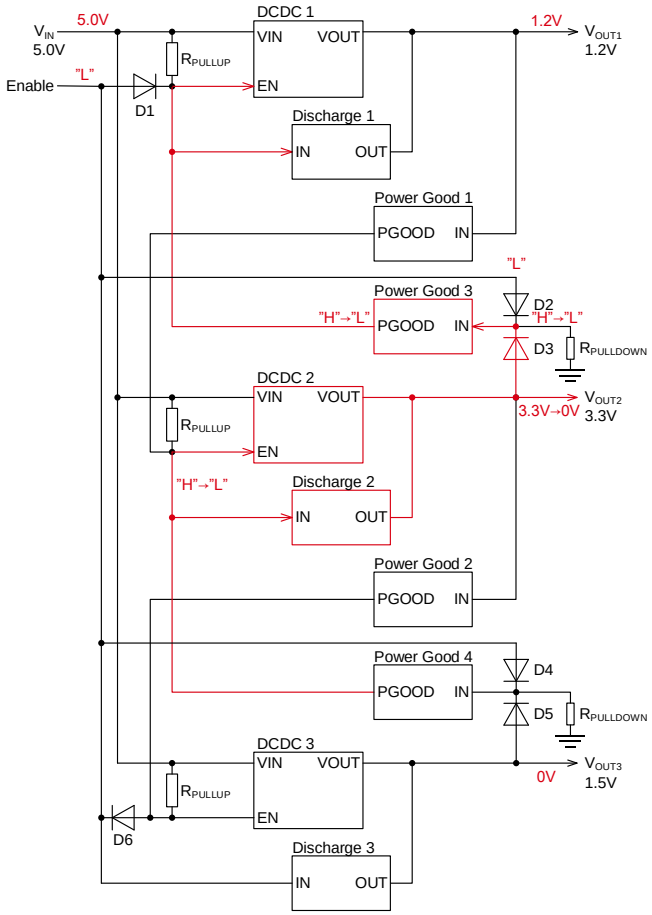

Figure 1-9. Operation when the power is turned OFF: Second step

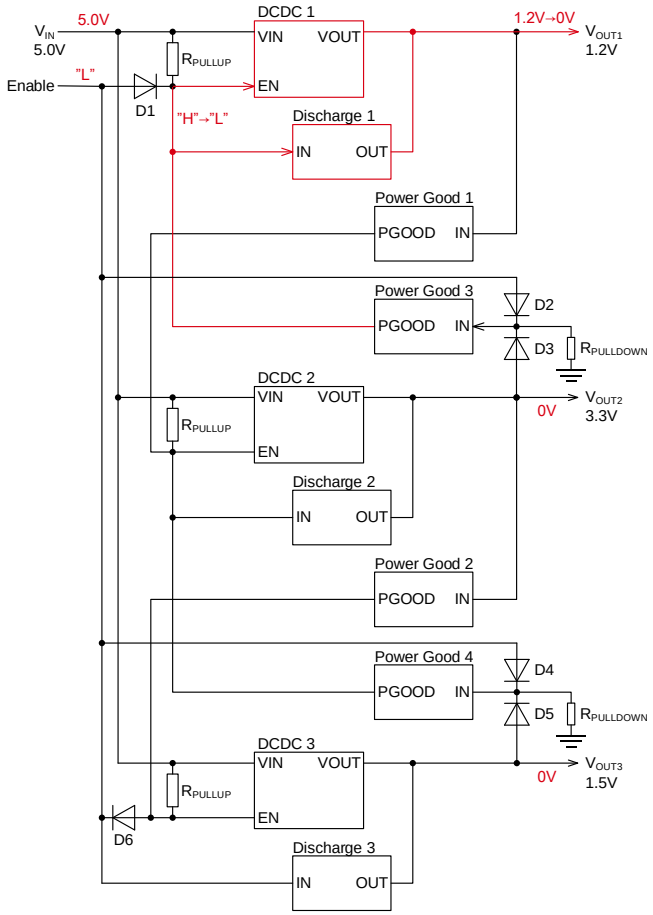

Figure 1-10. Operation when the power supply is turned OFF: Third step

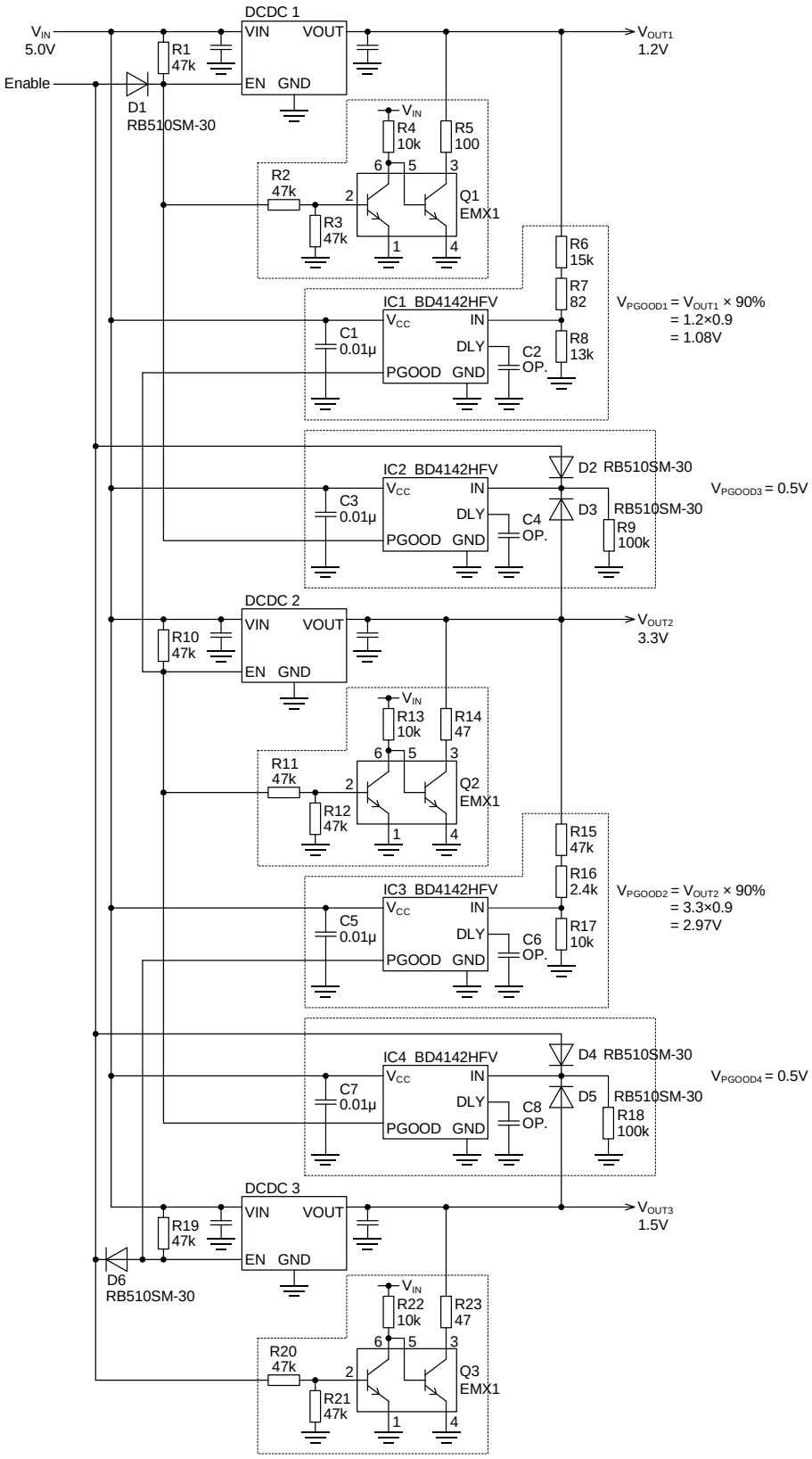

Figure 1-11. Example of a circuit that accomplishes the power supply sequence

Example of circuit 1

Figure 1-11 shows an example of a circuit that accomplishes the power supply sequence. The DCDCs in the 3 systems are assumed to be switching regulators (DC/DC converters) or linear regulators (LDO). The DCDCs feature an enable (EN) pin that can control the ON/OFF of the output.

The Power Good blocks use voltage detector IC BD4142HFV to perform the Power Good function. Figure 1-12 features the main part. This IC is equipped with a built-in hysteresis comparator with the detection voltage of 0.5 V. The detection voltage can be set using an external resistor. The detection voltage V_{PGOOD} can be calculated with Equation 1-1.

$$V_{PGOOD} = \frac{R_2 + R_3}{R_3} \times 0.5 \quad [V] \qquad (1\text{-}1)$$

In the example shown in Figure 1-11, V_{OUT1} is 1.2 V and the PGOOD of IC1 is set to output the flag when 90% of the output voltage is reached. If the detection voltage is set to a higher value such as 95%, the PGOOD output switches to “Low” when the output voltage momentarily drops due to fluctuations in the load, disadvantageously causing momentary interruptions to the DCDCs in the subsequent stages. The detection voltage should be determined after understanding the specifications of the fluctuations in the load and the voltage drop. The detection voltage at 90% is 1.2 V × 0.9 = 1.08 V. The resistor values can be calculated from Equation 1 as follows.

$$V_{PGOOD} = \frac{(15\ k\Omega + 82\ \Omega) + 13\ K\Omega}{13\ k\Omega} \times 0.5\ \mathrm{V} = 1.08 \quad [V]$$

Therefore, R2 is a series connection of 15kΩ and 82Ω and R3 is 13kΩ.

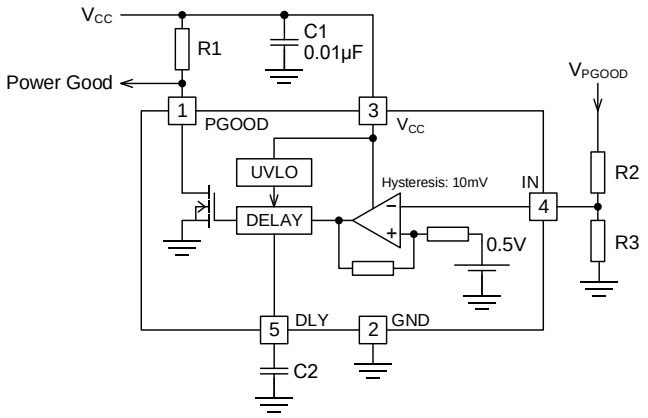

Figure 1-12. Power Good function configured with BD4142HFV

Since the tolerance is ±1.8% for the detection voltage of BD4142HFV, the range of PGOOD is from 88.4% (= 90% × 0.982) to 91.6% (= 90% × 1.018). In addition, since the hysteresis is 10 mV, the detection release voltage is 88.2% (= 90% × (0.5 V - 10 mV)/0.5 V) and the range is from 86.6% (= 88.2% × 0.982) to 89.8% (= 88.2% × 1.018).

To delay the PGOOD flag, connect a capacitor to the DLY pin. The delay time and the capacitance can be calculated with Equation 1-2.

$$C_2 = \frac{t_{DELAY}}{2 \times 10^6} \quad [F] \qquad (1\text{-}2)$$

On the other hand, the PGOOD IC2 and IC4 operate when the power is turned OFF. The detection is released (the output of the PGOOD switches from “High” → “Low”) when the output voltage of the DCDCs decreases to approximately 0.5 V or lower.

The Discharge block is configured with transistors and resistors as shown in Figure 1-13. The transistor in the first stage is a simple inverter circuit, and the transistor in the second stage is a switch of an open-collector. The resistance connected in series to the collector is varied to adjust the fall time of the output voltage.

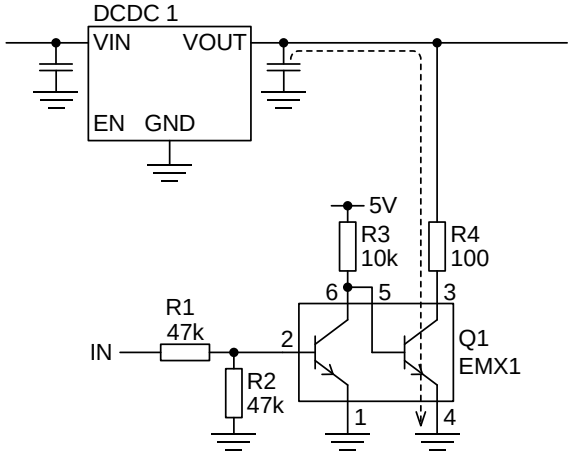

Figure 1-13. Discharge circuit

The diodes at various locations are components for creating logic operations. Since the “Low” voltage needs to be maintained low, Schottky barrier diodes with low forward voltages are used.

Example of operation 1

Figure 1-14 shows an example of the operation of the circuit in Figure 1-11. The voltage from the main power supply (V_{IN} 5.0 V) is always applied. To turn ON the power, switch the Enable pin from “Low” to “High”. Then, the output is turned ON in the order of V_{OUT}1, 2, and 3 according to the specification initially created. Next, to turn OFF the power, switch the Enable pin from “High” to “Low”. The output is turned OFF in the order of V_{OUT}3, 2, and 1.

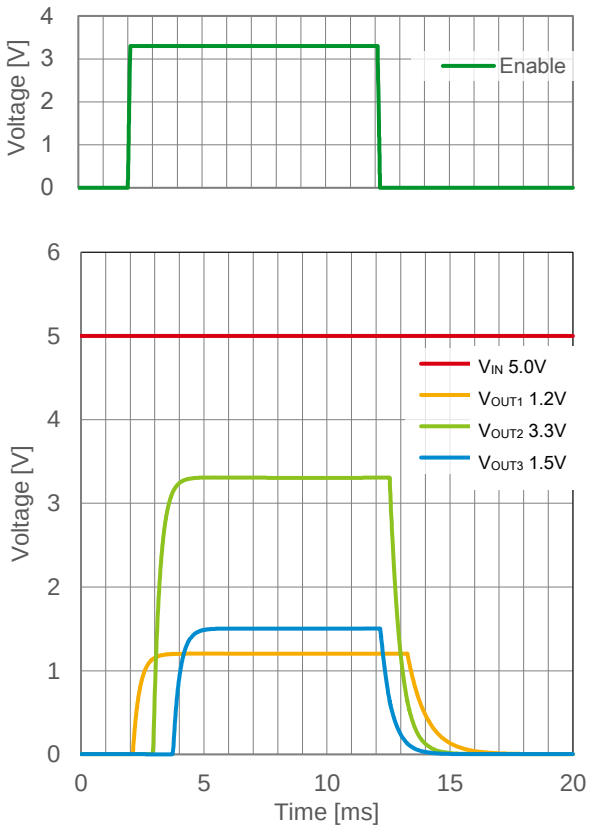

Figure 1-14. Operation waveforms of the power supply sequence

In this way, the power supply sequence can be accomplished without using any dedicated power supply sequence IC, by using general purpose power supply ICs that do not have the Power Good output or an output discharge function required for the sequence control.

Power supply sequence specification 2

In this example, we introduce the circuit design for the power supply sequence of 3 systems.
The specifications of the input and output voltages are shown below.

V_{IN}: 5.0V
V_{OUT1}: 1.2V
V_{OUT2}: 1.5V
V_{OUT3}: 3.3V

Figure 2-1 shows the power supply tree diagram. In this example, the circuit is configured with 3 power supply ICs. The power supply ICs are assumed to be switching regulators (DC/DC converters) or linear regulators (LDO). As a function of the power supply IC, an enable pin that can control the ON/OFF of the output is required.

The power shall be turned ON in the order of V_{OUT}1, 2, and 3, and be turned OFF in the order of V_{OUT}1, 2, and 3 as well. Figure 2-2 shows the schematic diagram.

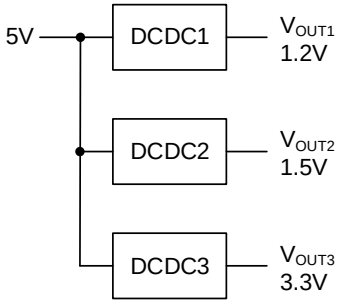

Figure 2-1. Power tree

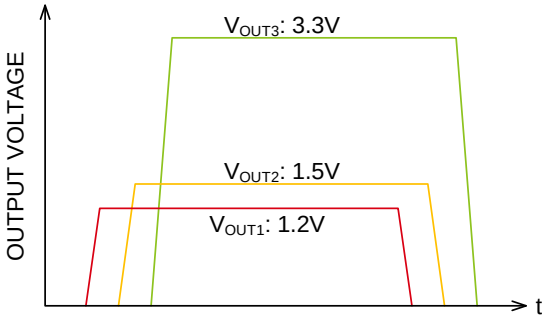

Figure 2-2. Schematic diagram of the power supply sequence

Control block diagram 2

Figure 2-3 shows the control block diagram. DCDC 1, DCDC 2, and DCDC 3 are the power supply ICs of 3 systems. Each output is controlled by the enable (EN) pin. Power Good 1 and 2 monitor the output voltage of the DCDCs when the power is turned ON, and output the “High” signal to the DCDC to be turned ON next when the output voltage reaches the target voltage. In addition, when turning the power OFF, the “LOW” signal is output to the DCDC to be turned OFF next when the target dropped voltage is reached. The Discharge blocks ensure the normal operation of the power supply sequence by rapidly discharging the electric charges stored in the output capacitor of the DCDCs to decrease the voltage when the power is turned OFF. Note that, in this block diagram, the logic is designed as Active High between EN and VOUT of the DCDC blocks, between IN and PGOOD of the Power Good blocks, and between IN and OUT of the Discharge blocks. In addition, the PGOOD pin (output) of the Power Good blocks and the OUT pin of the Discharge blocks are of the open-collector or open-drain type.

Let’s follow the sequence operation in order. For the initial values, the Enable terminal is at the “Low” level and the outputs of the 3 DCDCs are zero. Figure 2-4 shows the operation in the first step when the power is turned ON. First, the “High” voltage is applied to the Enable terminal to turn ON the power supplies. The “High” voltage is applied to the EN pin of DCDC 1 and DCDC 1 is turned ON. When the output voltage of DCDC 1 increases from 0 V to 1.2 V, the output voltage of Power Good 1 switches from “Low” to “High”. Then, the voltage is applied to the EN pin of DCDC 2 on the next stage.

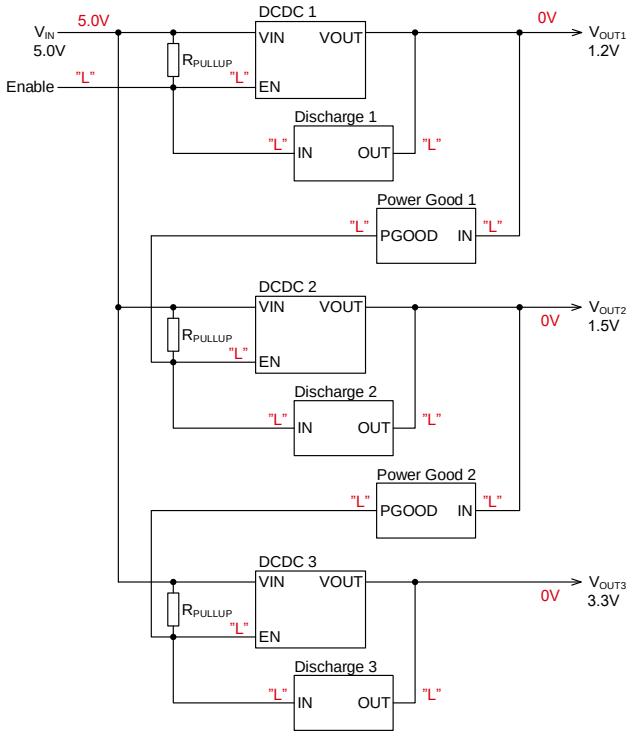

Figure 2-3. Control block diagram

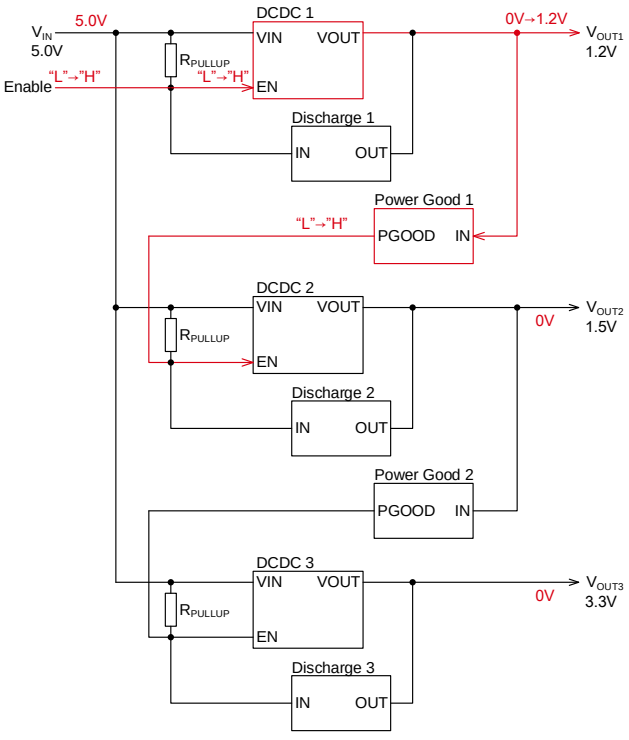

Figure 2-4. Operation when the power is turned ON: First step

Figure 2-5 shows the operation in the second step when the power is turned ON. The “High” voltage is applied to the EN pin of DCDC 2 and DCDC 2 is turned ON. When the output voltage of DCDC 2 increases from 0 V to 1.5 V, the output voltage of Power Good 2 switches from “Low” to “High”. Then, the voltage is applied to the EN pin of DCDC 3 on the next stage.

Figure 2-6 shows the operation in the third step when the power is turned ON. The “High” voltage is applied to the EN pin of DCDC 3 and DCDC 3 is turned ON. The output voltage of DCDC 3 increases from 0 V to 3.3 V and all of the 3 power supply systems are now operating.

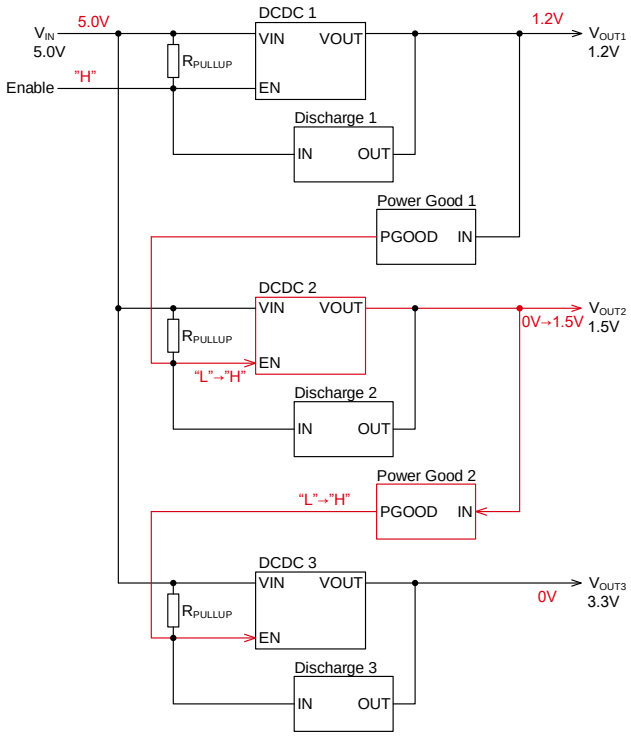

Figure 2-5. Operation when the power is turned ON: Second step

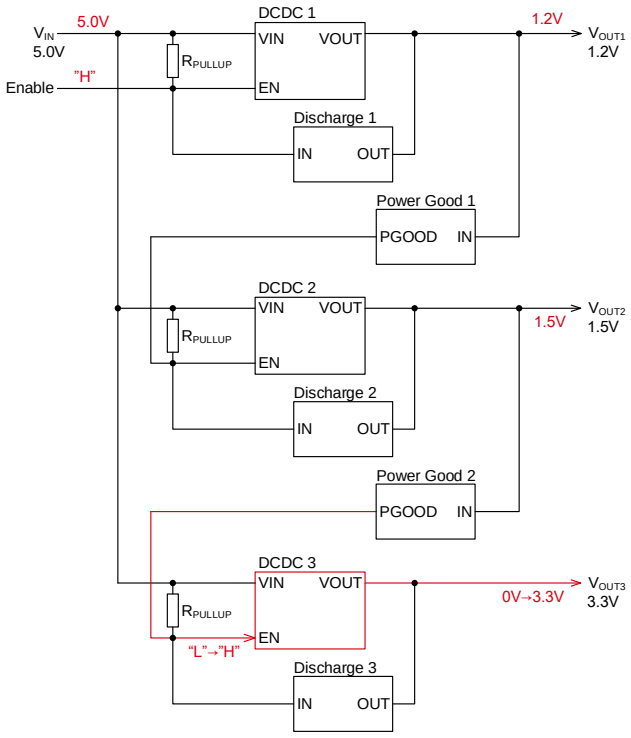

Figure 2-6. Operation when the power is turned ON: Third step

Figure 2-7 shows the state of the main nodes when the power supplies are operating.

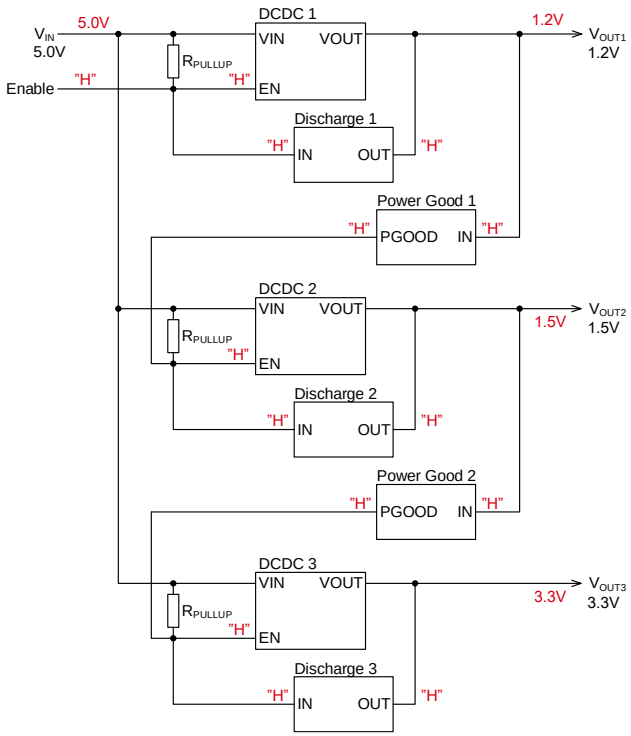

Figure 2-7. State of main nodes when the power supplies are operating

Next, we follow the sequence operation when the power is turned OFF in order. Figure 2-8 shows the operation in the first step when the power is turned OFF. First, the “Low” voltage is applied to the Enable terminal to turn OFF the power supplies. The “Low” voltage is applied to the EN pin of DCDC 1 and DCDC 1 is turned OFF. At the same time, the “Low” voltage is applied to the IN pin of Discharge 1 and the OUT pin switches to low impedance. This causes a rapid transition of the output voltage of DCDC 1 to 0 V. When the output voltage of DCDC 1 decreases, the output voltage of Power Good 1 switches from “High” to “Low”. Then, the voltage is applied to the EN pin of DCDC 2 and the IN pin of Discharge 2 on the next stage.

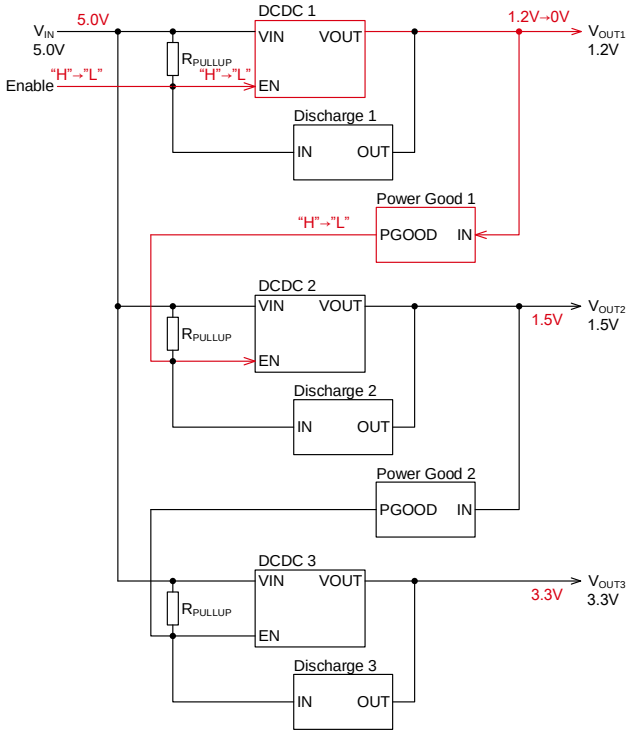

Figure 2-8. Operation when the power is turned OFF: First step

Figure 2-9 shows the operation in the second step when the power is turned OFF. The “Low” voltage is applied to the EN pin of DCDC 2 and DCDC 2 is turned OFF. At the same time, the “Low” voltage is applied to the IN pin of Discharge 2 and the OUT pin switches to low impedance. This causes a rapid transition of the output voltage of DCDC 2 to 0 V. When the output voltage of DCDC 2 decreases, the output voltage of Power Good 2 switches from “High” to “Low”. Then, the voltage is applied to the EN pin of DCDC 3 and the IN pin of Discharge 3 on the next stage.

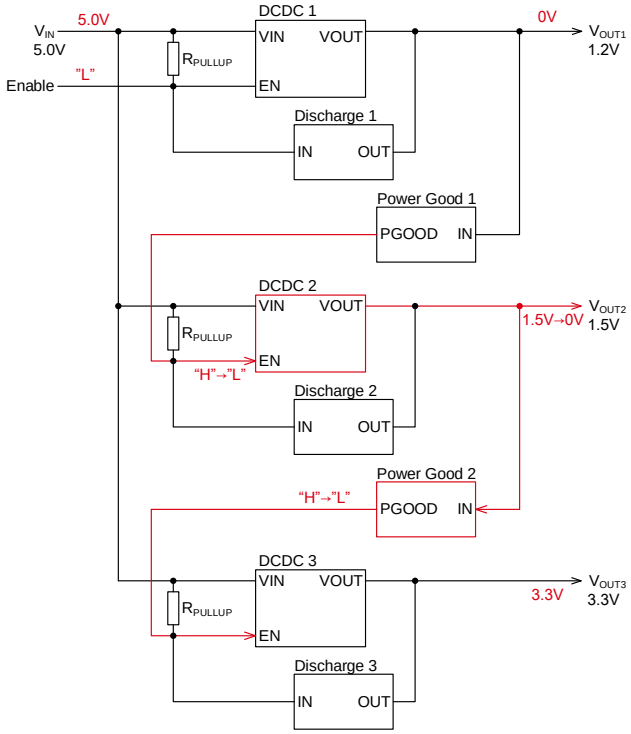

Figure 2-9. Operation when the power is turned OFF: Second step

Figure 2-10 shows the operation in the third step when the power is turned OFF. The “Low” voltage is applied to the EN pin of DCDC 3 and DCDC 3 is turned OFF. At the same time, the “Low” voltage is applied to the IN pin of Discharge 3 and the OUT pin switches to low impedance. This causes a rapid transition of the output voltage of DCDC 3 to 0 V. All of the 3 power supply systems are now turned OFF.

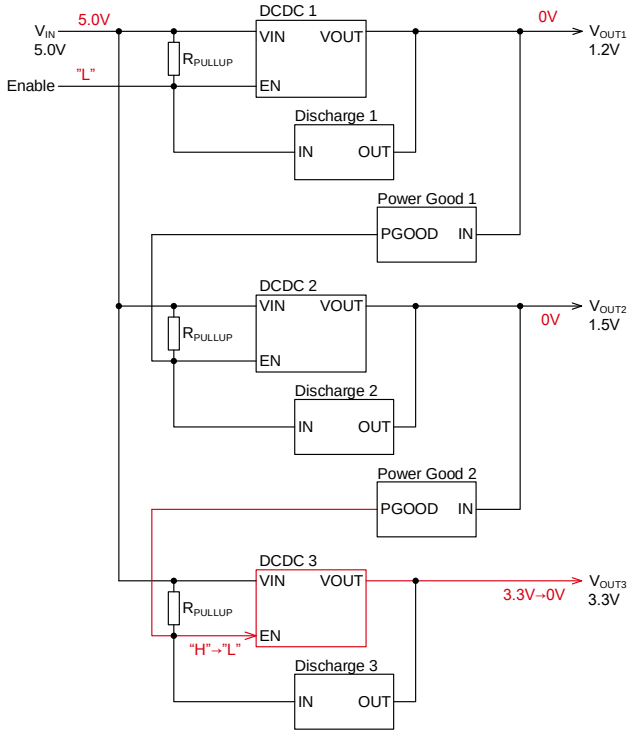

Figure 2-10. Operation when the power is turned OFF: Third step

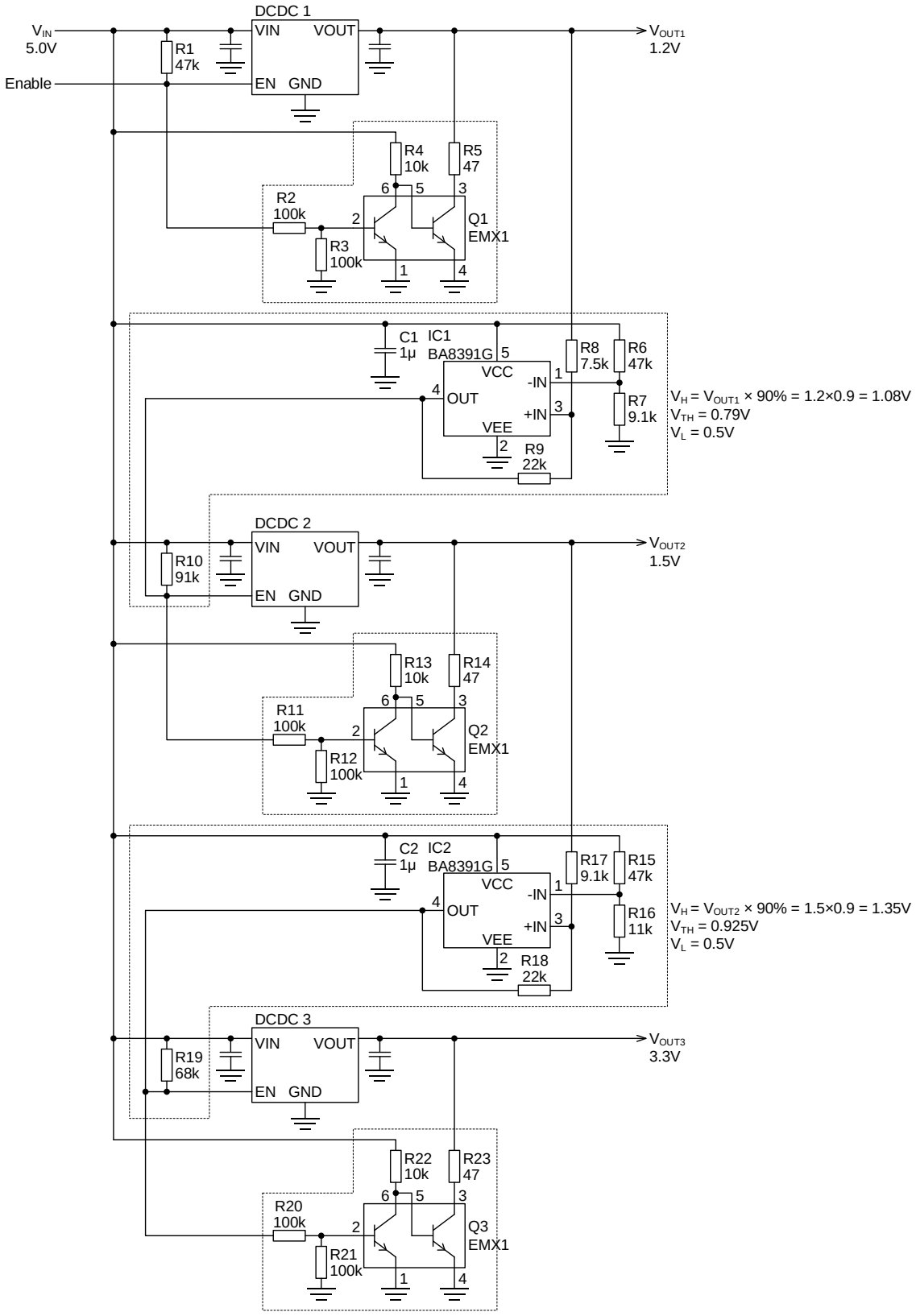

Figure 2-11. Example of a circuit that accomplishes the power supply sequence

Example of circuit 2

Figure 2-11 shows an example of a circuit that accomplishes the power supply sequence. The DCDCs in the 3 systems are assumed to be switching regulators (DC/DC converters) or linear regulators (LDO). The DCDCs feature an enable (EN) pin that can control the ON/OFF of the output.

The Power Good block is configured with a non-inverting hysteresis comparator as shown in Figure 2-12, and the comparator IC BA8391G is used for the device. A large hysteresis voltage is provided between the detection voltage when turning ON the power (V_H) and the detection voltage when turning OFF the power (V_L). This enables a single device to detect both voltages when turning the power ON and OFF to output the control signals.

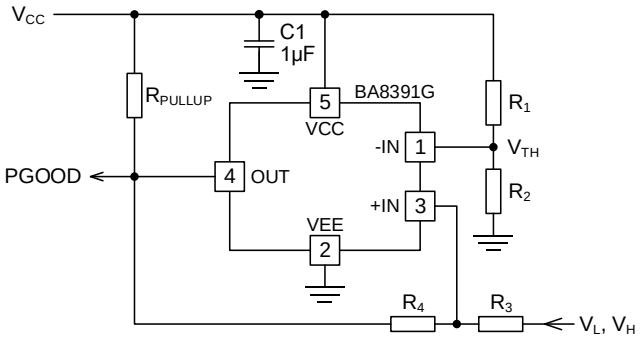

Figure 2-12. Power Good function configured with a non-inverting hysteresis comparator

First, we look at V_H, the detection voltage when turning ON the power. In the example shown in Figure 2-11, V_{OUT1} is 1.2 V and the PGOOD IC1 is set to output the flag when 90% of the output voltage is reached. The detection voltage V_H is 1.2 V × 0.9 = 1.08 V. Next, V_L, which is the detection voltage when turning OFF the power, is set to 0.5 V. At this voltage, parasitic elements generally will not be turned ON even if reverse voltage is applied between the power supplies.

The threshold voltage of the comparator (V_{TH}) is set to the midpoint between V_H and V_L as shown in Figure 2-13. The value can be calculated with Equation 2-1.

$$V_{TH} = \frac{(V_H - V_L)}{2} + V_L \quad [V] \qquad (2\text{-}1)$$

$$= \frac{(1.08 - 0.5)}{2} + 0.5 = 0.79\ V$$

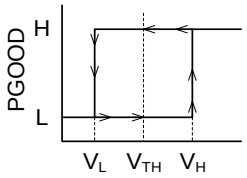

Figure 2-13. Hysteresis voltage

In the circuit diagram shown in Figure 2-12, V_{TH} is expressed by Equation 2-2. Converting this to the equation for R_2 gives Equation 2-3.

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad [V] \qquad (2\text{-}2)$$

$$R_2 = \frac{R_1 \times V_{TH}}{V_{CC} - V_{TH}} \quad [\Omega] \qquad (2\text{-}3)$$

When R_1 is 47kΩ and V_{CC} is 5 V, R_2 is 8.8kΩ according to the following equation. Select the nominal resistor value of 9.1kΩ from the E24 series.

$$R_2 = \frac{47k\Omega \times 0.79V}{5V - 0.79V} = 8.8k\Omega \cong 9.1\text{k}\Omega$$

To cancel the input bias current, select R3 so as to have the same impedance as the inverting pin. The value is 7.6kΩ according to Equation 2-4, so select the nominal resistor value of 7.5kΩ from the E24 series.

$$R_3 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} = \frac{1}{\frac{1}{47k\Omega} + \frac{1}{9.1k\Omega}} 7.6k\Omega \cong 7.5k\Omega \qquad (2\text{-}4)$$

The general calculations for obtaining V_H and V_L of a non-inverting hysteresis comparator are described by Equations 2-5 and 2-6. Converting these to the equations for R_4 and R_{PULLUP} gives Equations 2-7 and 2-8.

$$V_H = \frac{(R_3 + R_4) \times R_2}{R_4 \times (R_1 + R_2)} \times V_{CC} \quad [V] \qquad (2\text{-}5)$$

$$V_L = \frac{(R_3 + R_4 + R_{PULLUP}) \times V_{TH} - R_3 \times V_{CC}}{R_4 + R_{PULLUP}} \quad [V] \qquad (2\text{-}6)$$

$$R_4 = \frac{R_2 \times R_3 \times V_{CC}}{(R_1 + R_2) \times V_H - R_2 \times V_{CC}} \quad [\Omega] \qquad (2\text{-}7)$$

$$R_{PULLUP} = \frac{R_3 \times (V_{TH} - V_{CC}) + R_4 \times (V_{TH} - V_L)}{V_L - V_{TH}} \ [V] \qquad (2\text{-}8)$$

Substitute the constants obtained above into Equations 2-7 and 2-8 to determine the remaining values.

$$R_4 = \frac{9.1k\Omega \times 7.5k\Omega \times 5V}{(47k\Omega + 9.1k\Omega) \times 1.08V - 9.1k\Omega \times 5V}$$

$$= 22.6k\Omega \cong 22k\Omega \qquad (2\text{-}9)$$

$$R_{PULLUP} = \frac{7.5k\Omega \times (0.79V - 5V) + 22k\Omega \times (0.79V - 0.5V)}{0.5V - 0.79V}$$

$$= 86.9k\Omega \cong 91\text{k}\Omega \qquad (2\text{-}10)$$

The Discharge block is configured with transistors and resistors as shown in Figure 2-14. The transistor in the first stage is a simple inverter circuit, and the transistor in the second stage is a switch of an open-collector. The resistance connected in series to the collector is varied to adjust the fall time of the output voltage.

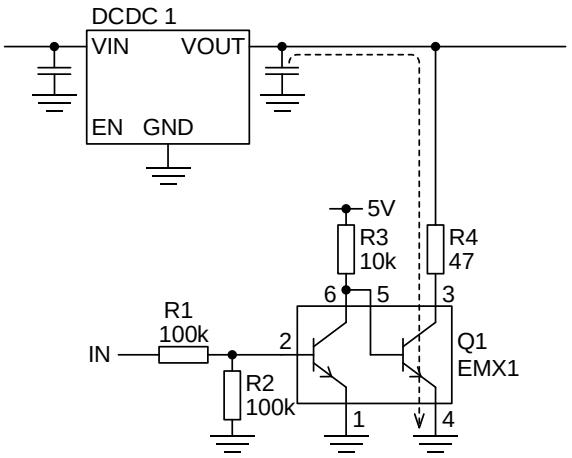

Figure 2-14. Discharge circuit

Example of operation 2

Figure 2-15 shows an example of the operation of the circuit in Figure 2-11. The voltage from the main power supply (V_{IN} 5.0 V) is always applied. To turn ON the power, switch the Enable pin from “Low” to “High”. Then, the output is turned ON in the order of $V_{OUT}1$, 2, and 3 according to the specification initially created. Next, to turn OFF the power, switch the Enable pin from “High” to “Low”. The output is turned OFF in the order of $V_{OUT}1$, 2, and 3.

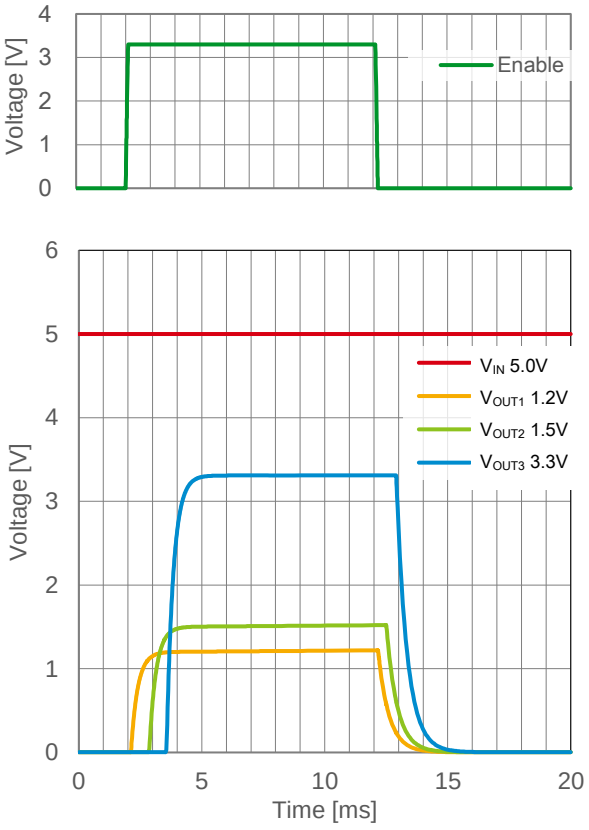

Figure 2-15. Operation waveforms of the power supply sequence

In this way, the power supply sequence can be accomplished without using any dedicated power supply sequence IC, by using general purpose power supply ICs that do not have the Power Good output or an output discharge function required for the sequence control.

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