

## Linear Regulator Series

# Thermal Resistance Data: SSOP5

## BD9xxN1G-C Series

This application note provides the thermal resistance data of the SSOP5 package used for the thermal design of the BD9xxN1G-C series linear regulator IC.

### Product Summary

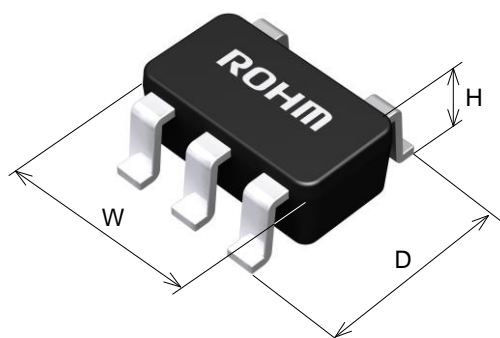
Model name: BD9xxN1G-C series

Package name: SSOP5

Function: Linear regulator (LDO) IC

See Datasheet for more details.

### Package



SSOP5

W (typ) D (typ) H (max)  
2.9 mm × 2.8 mm × 1.25 mm

### Measurement environment

Content	Standard
Measurement environment	JEDEC STANDARD JESD51-2A (Still Air)
Measurement board standard	JEDEC STANDARD JESD51-3 JESD51-7

### Thermal resistance

Configuration	$\theta_{JA}$ (°C/W)	$\Psi_{JT}$ (°C/W)
1-layer	271.3	46
2-layers	194.2	39
4-layers	146.7	37

$\theta_{JA}$ : Thermal resistance between  
junction temperature  $T_J$  -  
ambient temperature  $T_A$

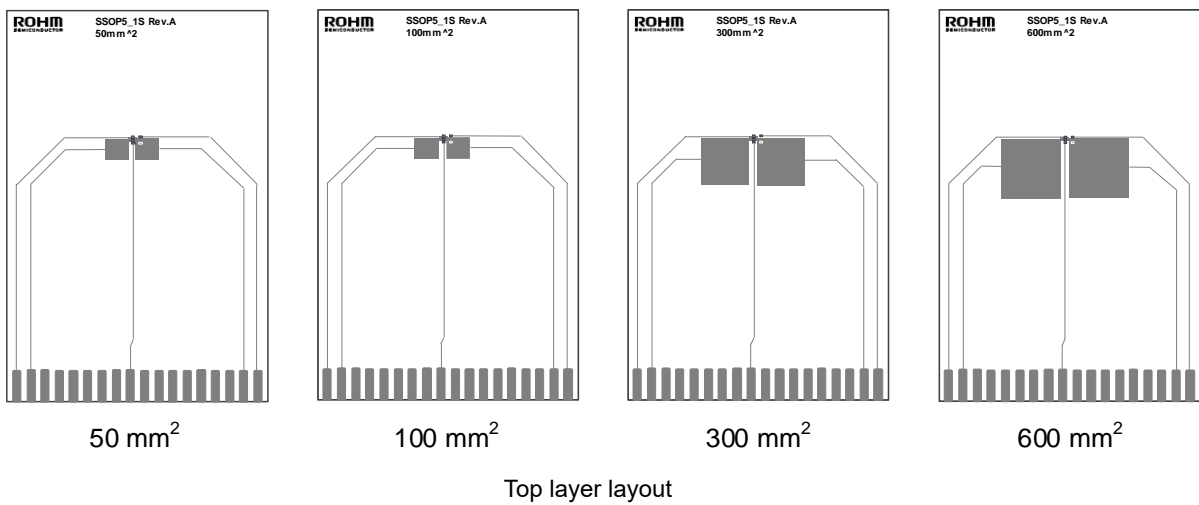
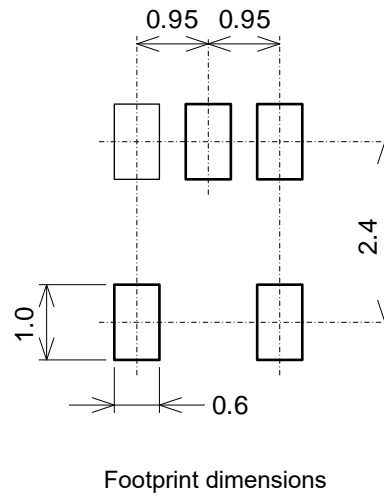
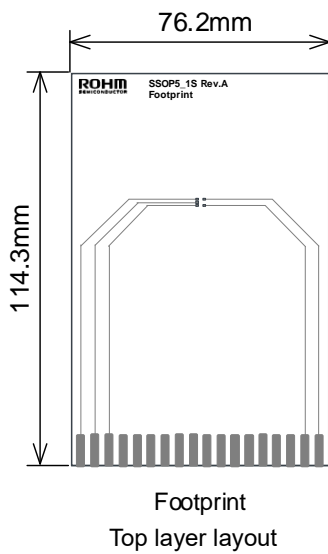
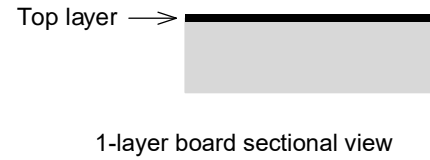
$\Psi_{JT}$ : Thermal characterization parameter between  
Junction temperature  $T_J$  -  
package surface center temperature  $T_T$

Note: The thermal resistances and thermal characterization parameters in this application note are based on measurement under a JEDEC environment and may not always be consistent with the values for actual equipment. It is necessary to consider variations in the values due to the PCB characteristics, PCB layout, parts layout, chassis shape, surrounding environment, and so on.

PCB specification, 1 layer (1s)

Conforms to JEDEC standard JESD51-3

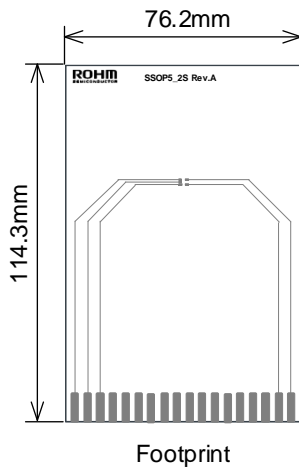
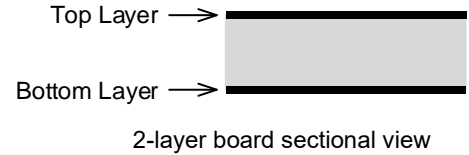
Item	Value
Board thickness	1.57 mm
Board outline dimensions	76.2 mm × 114.3 mm
Board material	FR-4
Trace thickness (Finished thickness)	70 μm (2 oz)
Lead width	0.254 mm
Copper foil area	Footprint [ 50 mm <sup>2</sup> to 600 mm <sup>2</sup> ]



PCB specification, 2-layers

Conforms to JEDEC standard JESD51-7

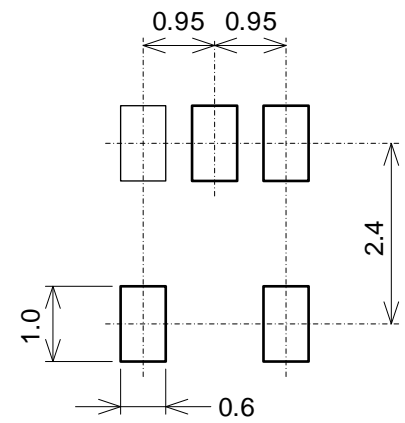
Item		Value
Board thickness		1.60 mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (Finished thickness)	Top	70 μm (2 oz)
	Bottom	70 μm (2 oz)
Lead width		0.254 mm
Copper foil area	Top	Footprint 5505 mm <sup>2</sup> (74.2 mm × 74.2 mm) [ 50 mm <sup>2</sup> to 3000 mm <sup>2</sup> ]
	Bottom	



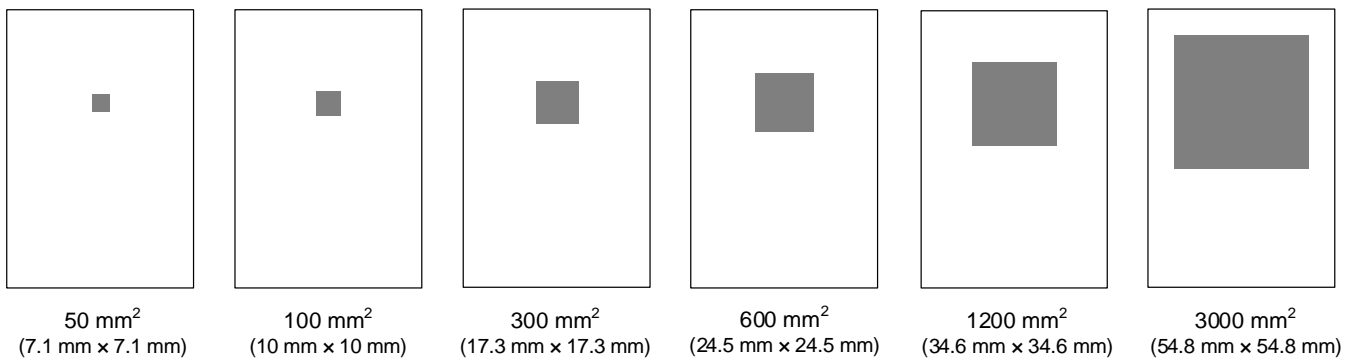
Top layer layout



Bottom layer layout



Footprint dimensions

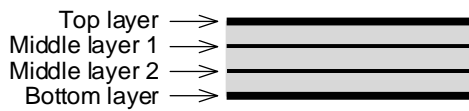


Bottom layer layout

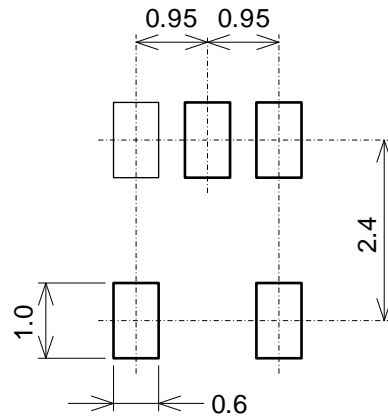
**PCB specification, 4-layers (2s2p)**

Conforms to JEDEC standard JESD51-7

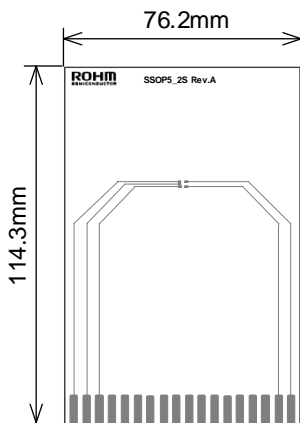
Item		Value
Board thickness		1.60 mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (Finished thickness)	Top	70 μm (2 oz)
	Middle 1	35 μm (1 oz)
	Middle 2	35 μm (1 oz)
	Bottom	70 μm (2 oz)
Lead width		0.254 mm
Copper foil area	Top	Footprint
	Middle 1	5505 mm <sup>2</sup> (74.2 mm × 74.2 mm)
	Middle 2	5505 mm <sup>2</sup> (74.2 mm × 74.2 mm)
	Bottom	5505 mm <sup>2</sup> (74.2 mm × 74.2 mm)



4-layer board sectional view



Footprint dimensions



Footprint

Top layer layout



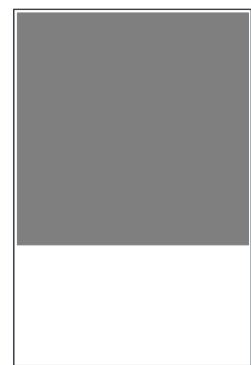
5505 mm<sup>2</sup>  
(74.2 mm × 74.2 mm)

Middle 1 layer layout



5505 mm<sup>2</sup>  
(74.2 mm × 74.2 mm)

Middle 2 layer layout



5505 mm<sup>2</sup>  
(74.2 mm × 74.2 mm)

Bottom layer layout

Thermal resistance data, 1-layer (1s)

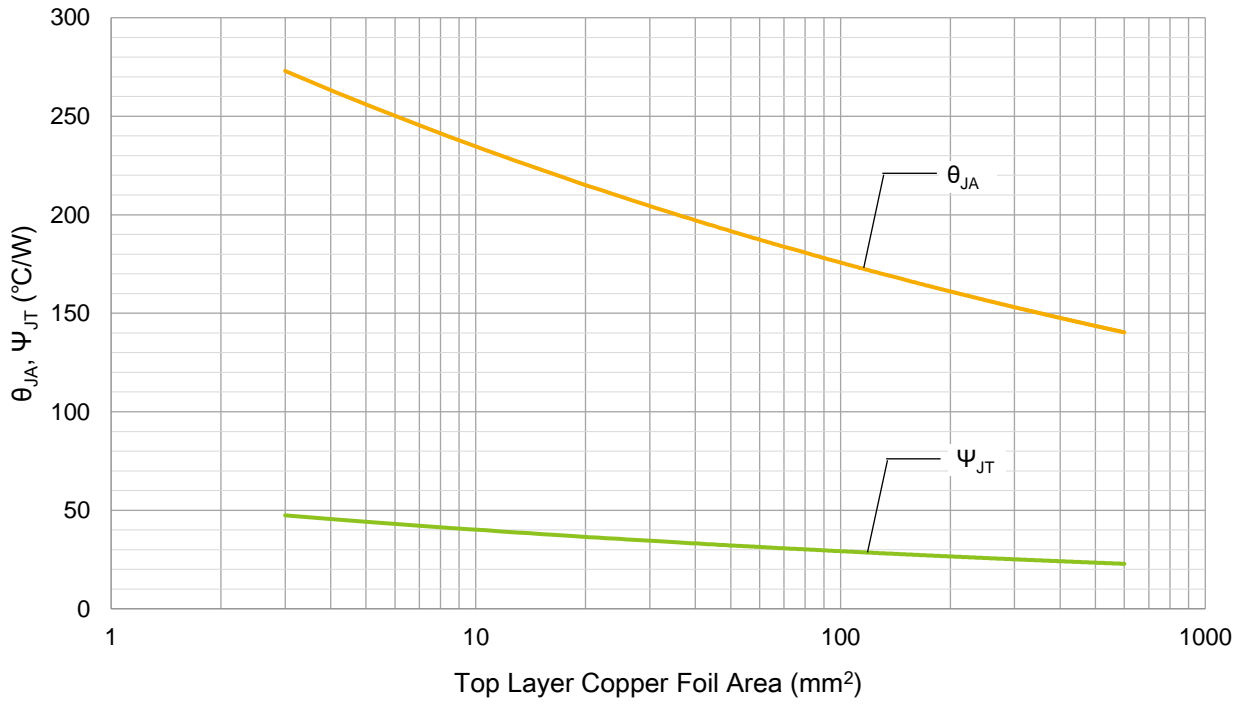


Figure 1.  $\theta_{JA}$ ,  $\psi_{JT}$  vs. Top Layer Copper Foil Area

Thermal resistance data, 2-layers

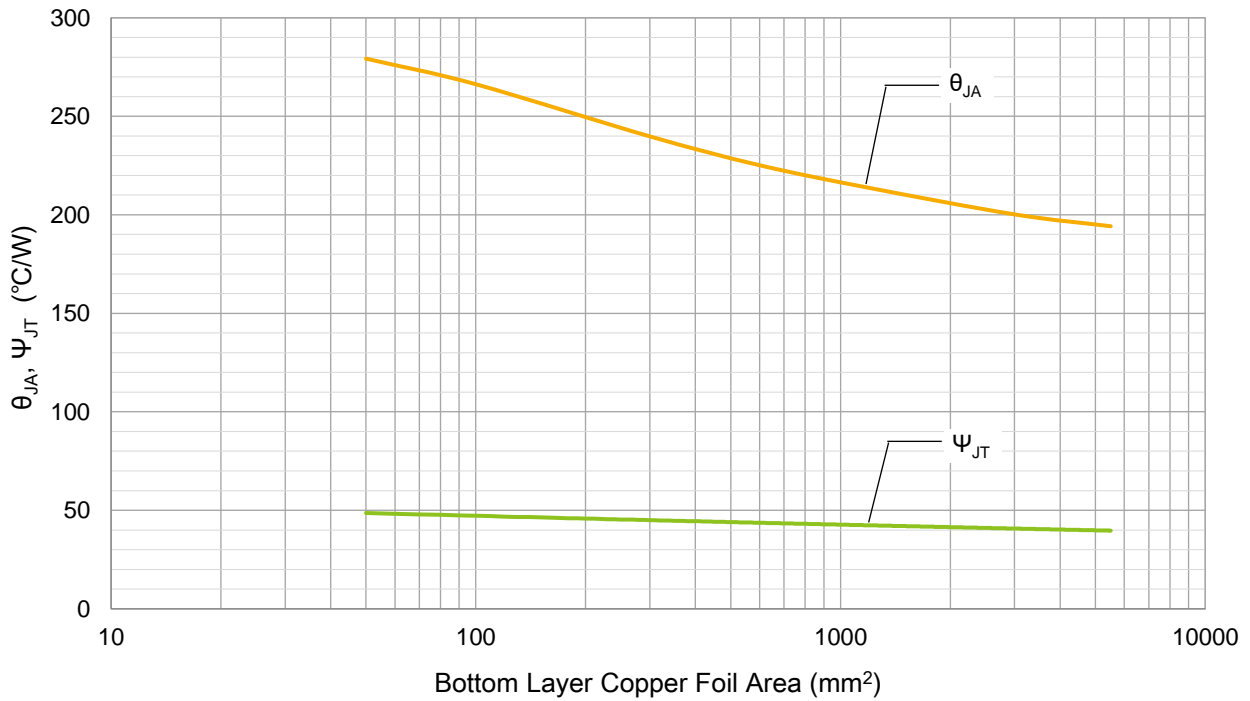
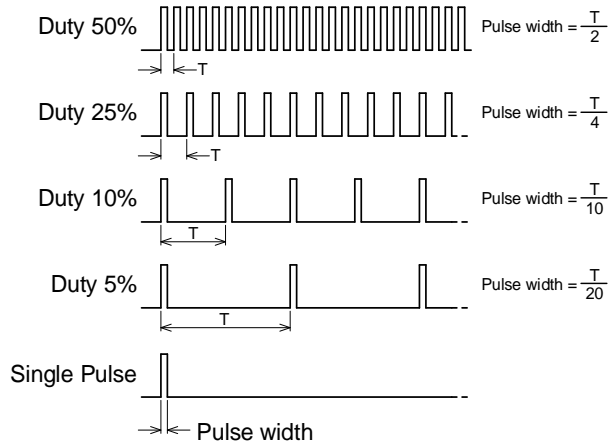


Figure 2.  $\theta_{JA}$ ,  $\psi_{JT}$  vs. Bottom Layer Copper Foil Area

### Transient thermal resistance

Conforms to JEDEC standard JESD51

X axis: The length of time electrical power is applied to the device-under-test



Y axis: Transient thermal resistance

### Transient thermal resistance data, 1-layer (1s)

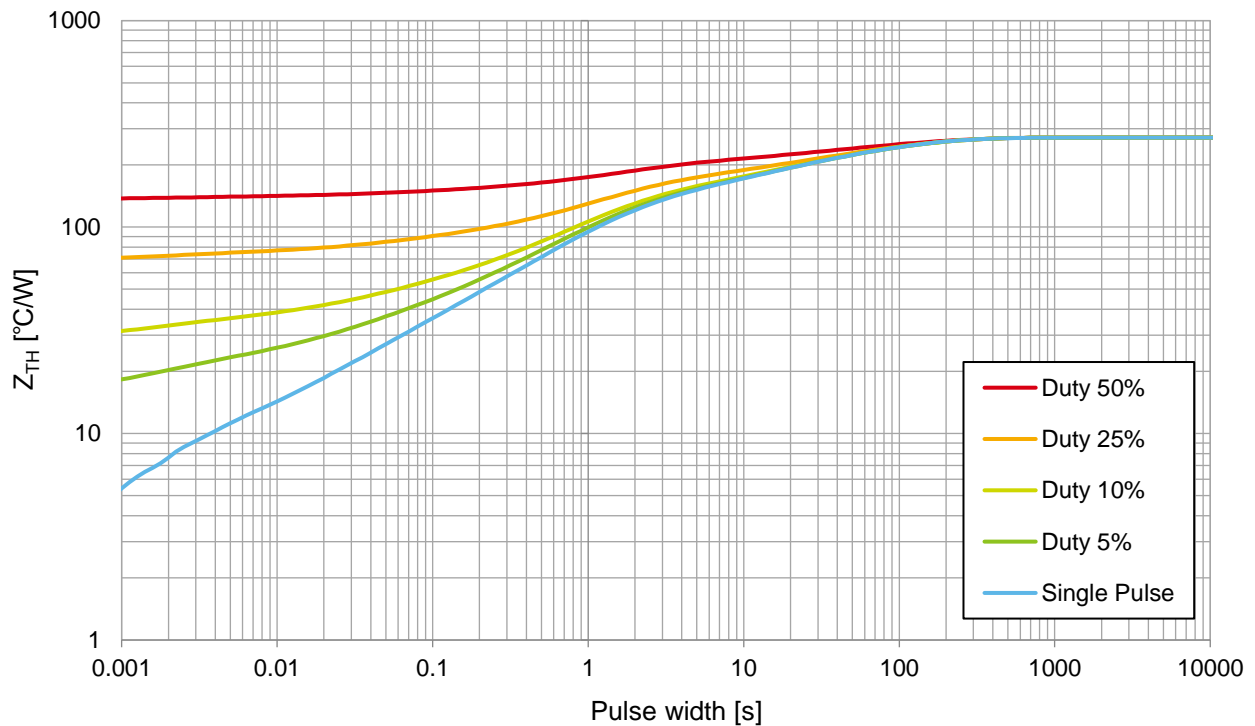


Figure 3. Transient thermal resistance, 1 layer, Copper foil surface area Footprint

Transient thermal resistance data, 1-layer (1s), continued

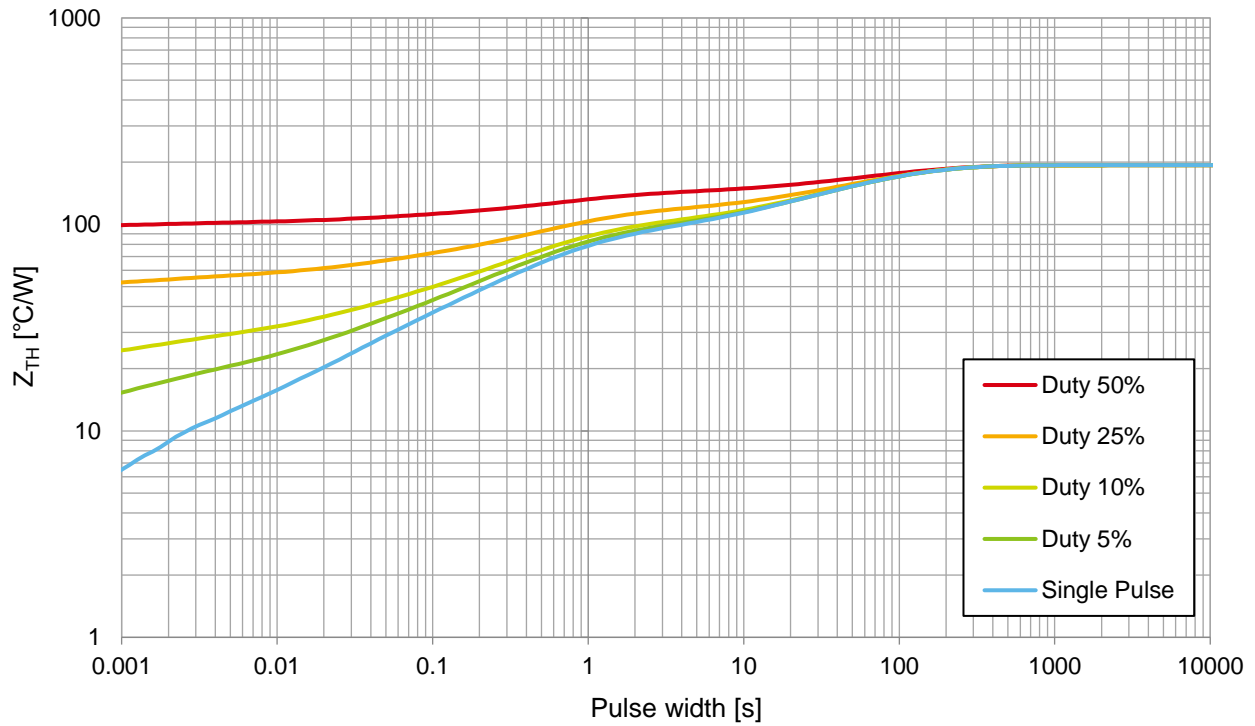


Figure 4. Transient thermal resistance, 1-layer, Copper foil surface area 50 mm<sup>2</sup>

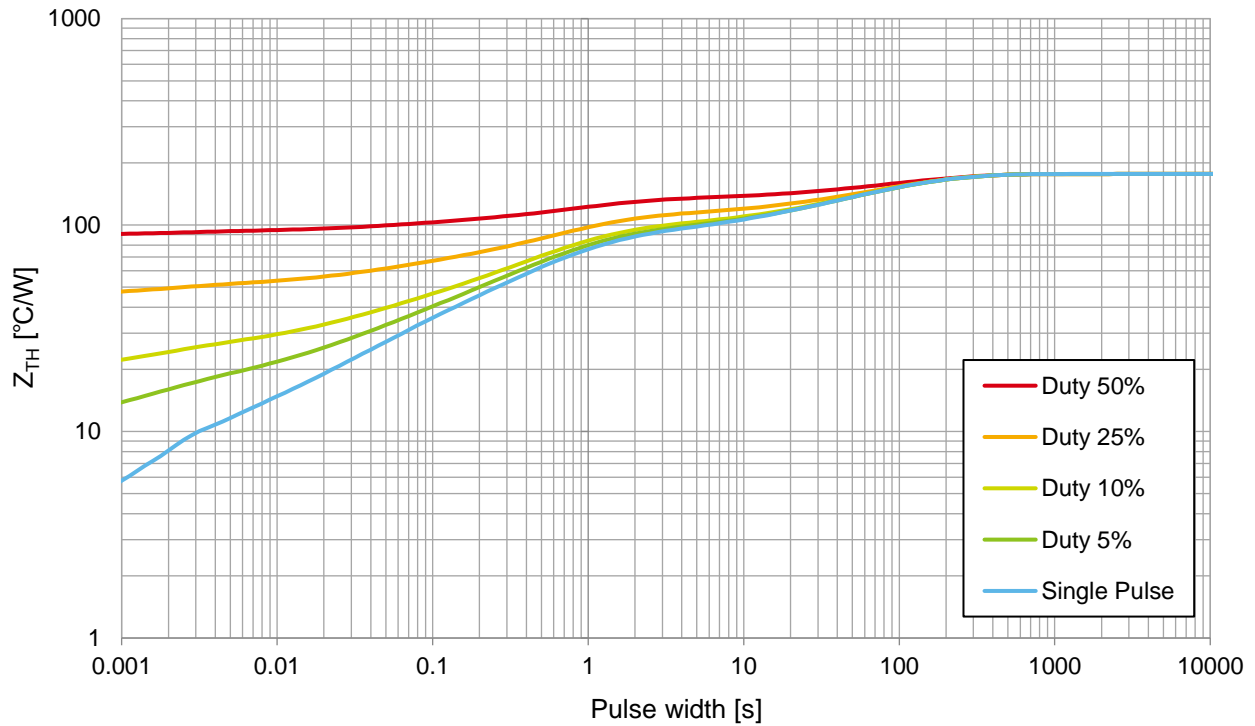


Figure 5. Transient thermal resistance, 1-layer, Copper foil surface area 100 mm<sup>2</sup>

Transient thermal resistance data, 1-layer (1s), continued

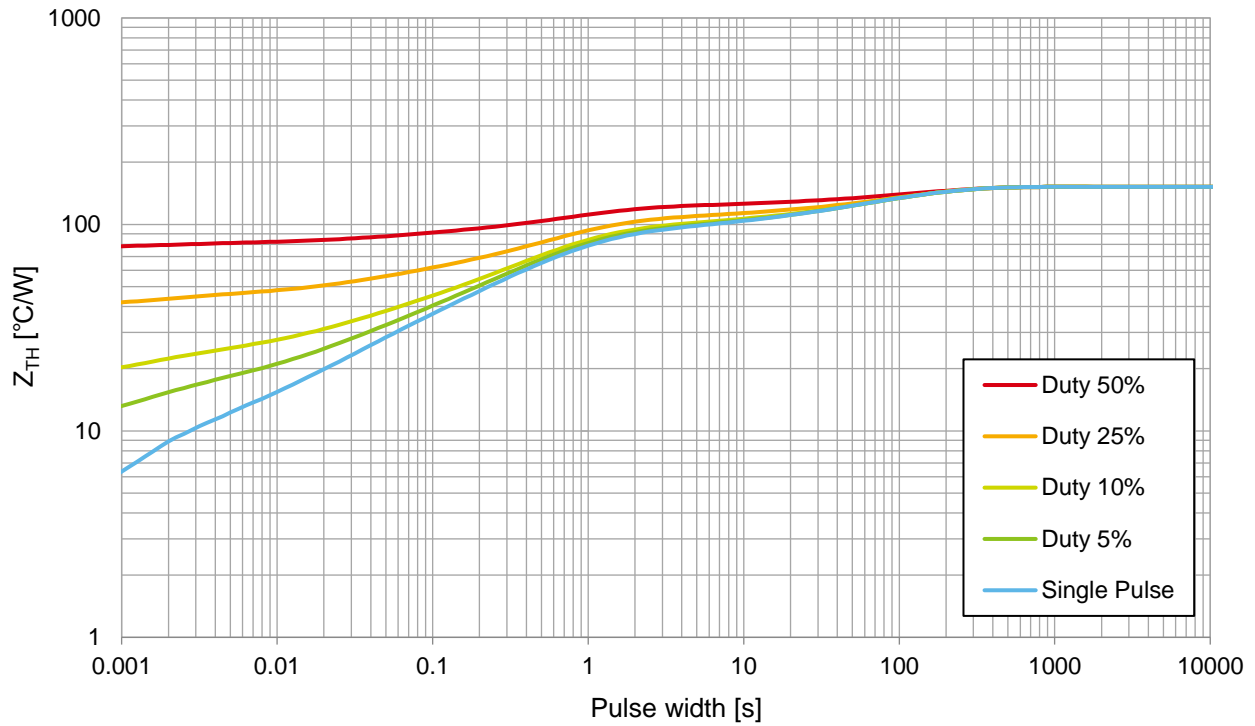


Figure 6. Transient thermal resistance, 1-layer, Copper foil surface area 300 mm²

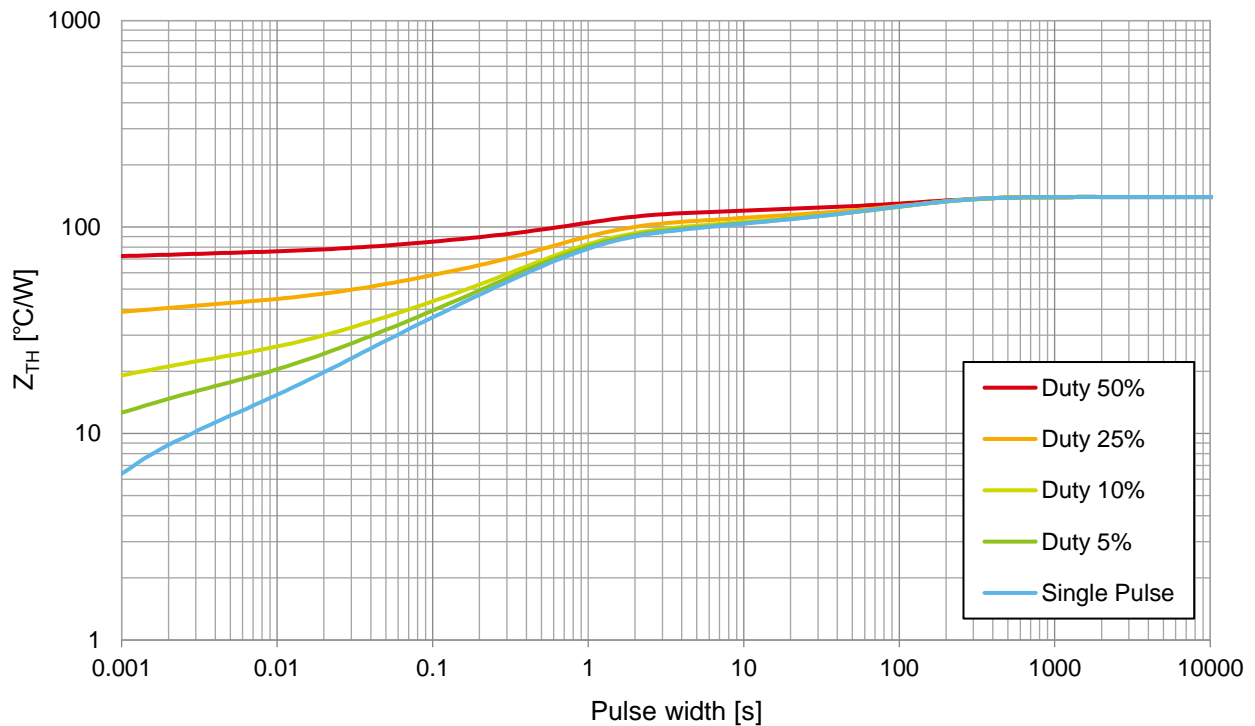


Figure 7. Transient thermal resistance, 1-layer, Copper foil surface area 600 mm²



Transient thermal resistance data, 2-layers

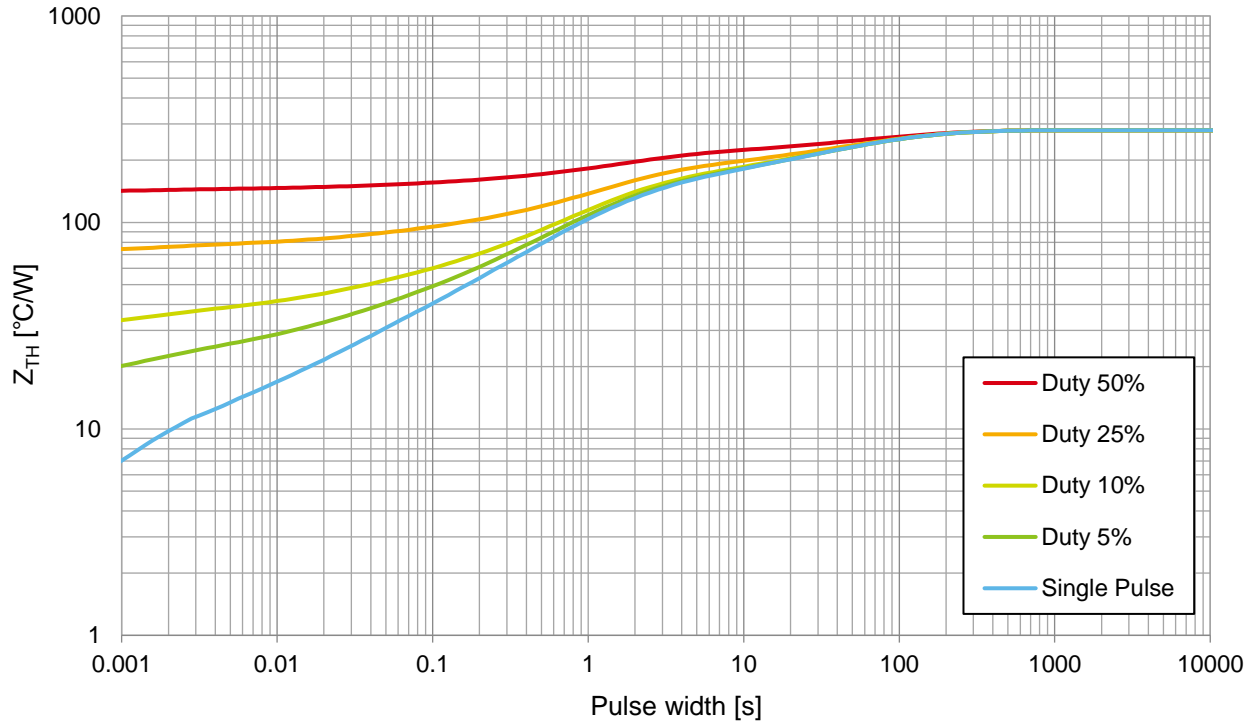


Figure 8. Transient thermal resistance, 2-layers, Copper foil bottom area 50 mm<sup>2</sup>

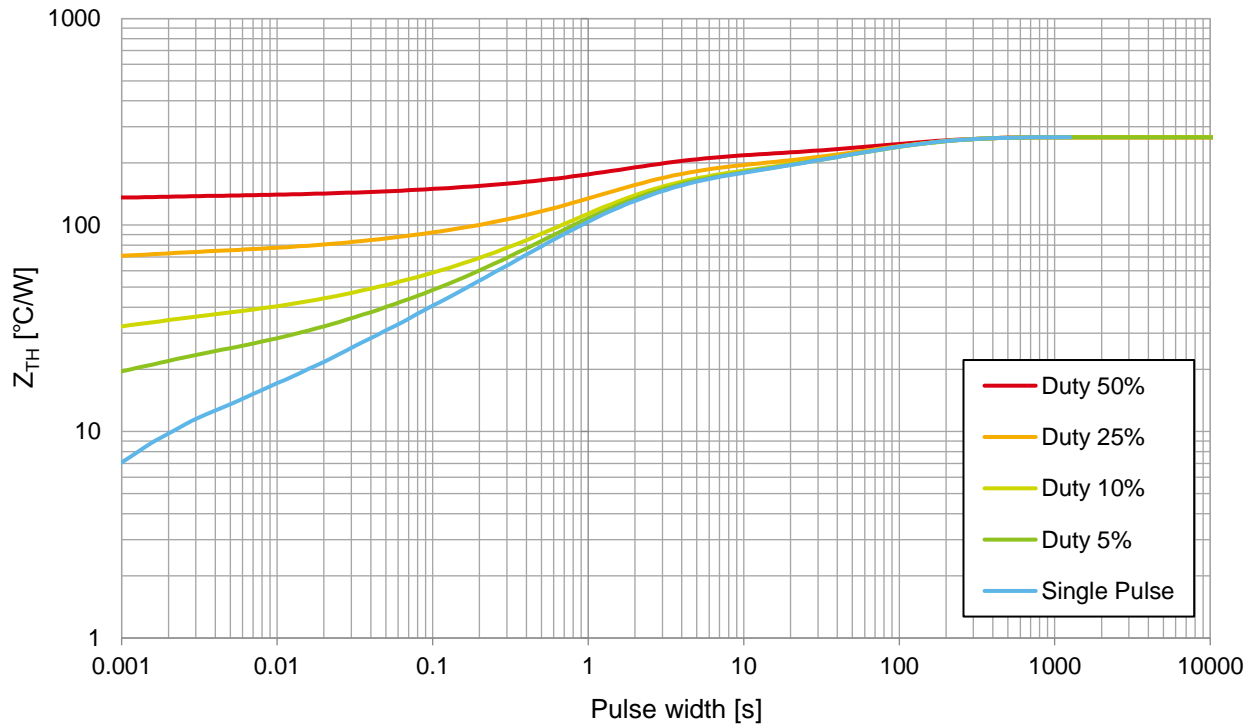


Figure 9. Transient thermal resistance, 2-layers, Copper foil bottom area 100 mm<sup>2</sup>

Transient thermal resistance data, 2 layers, continued

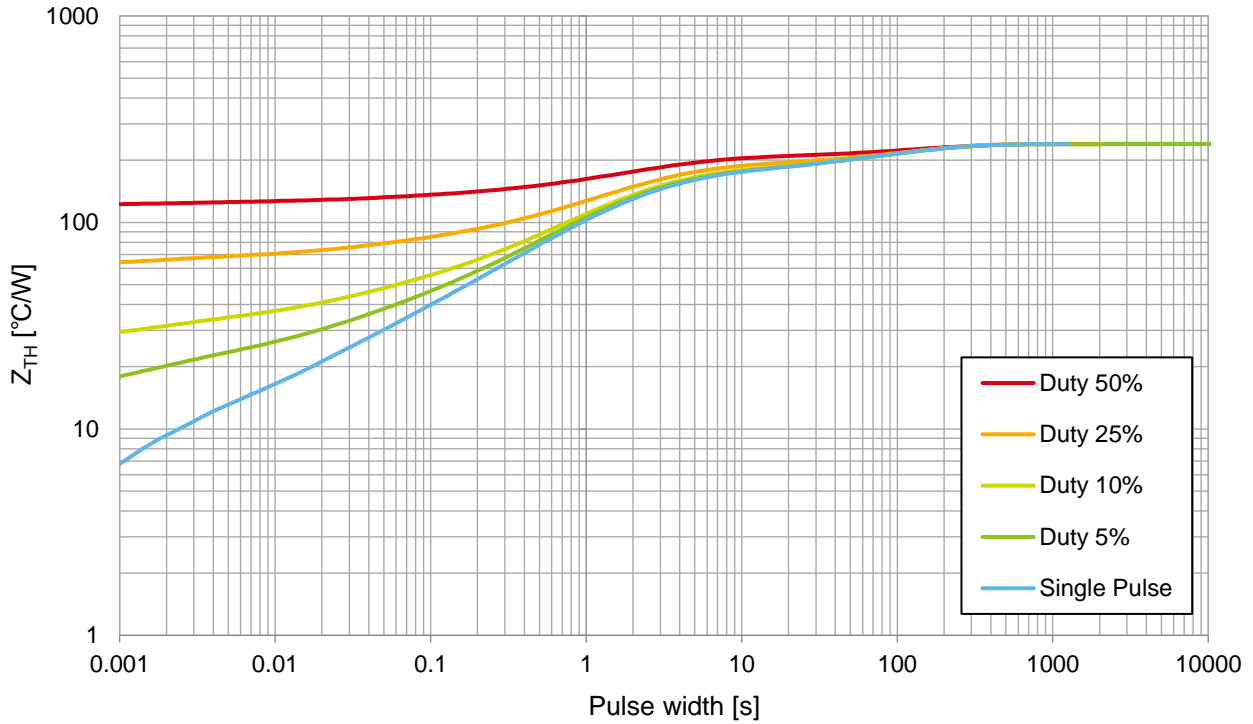


Figure 10. Transient thermal resistance, 2-layers, Copper foil bottom area 300 mm<sup>2</sup>

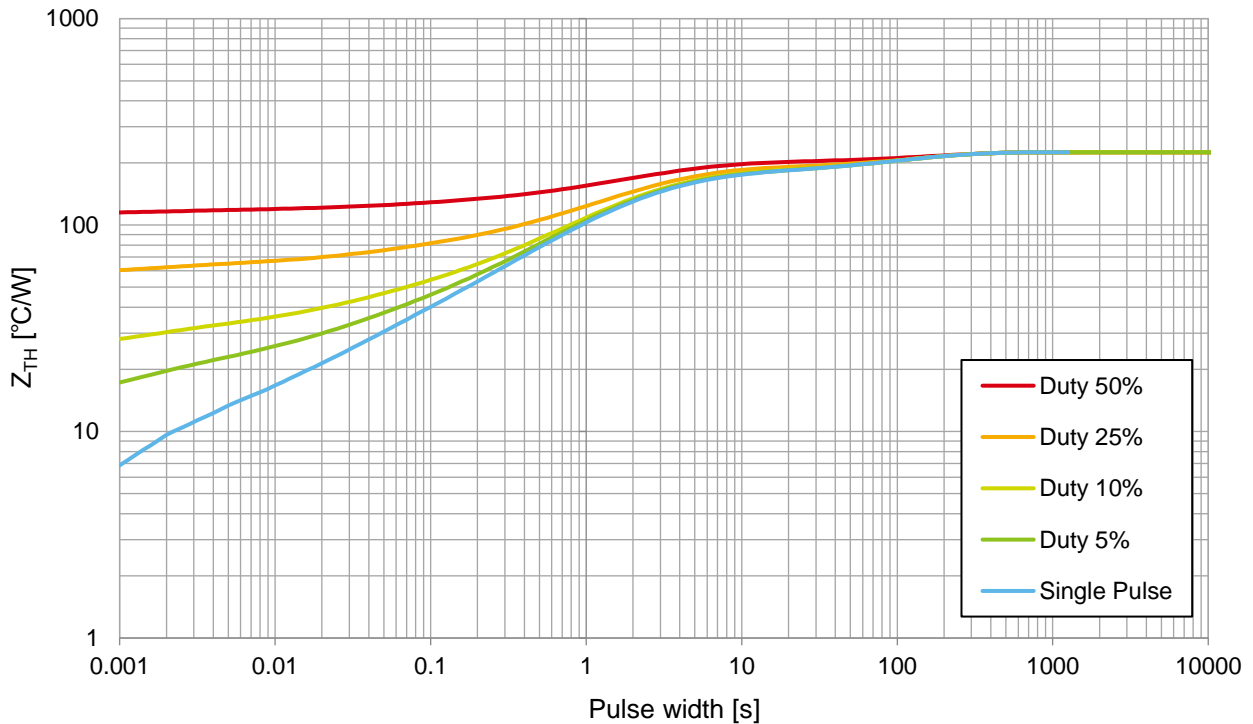


Figure 11. Transient thermal resistance, 2-layers, Copper foil bottom area 600 mm<sup>2</sup>

Transient thermal resistance data, 2-layers, continued

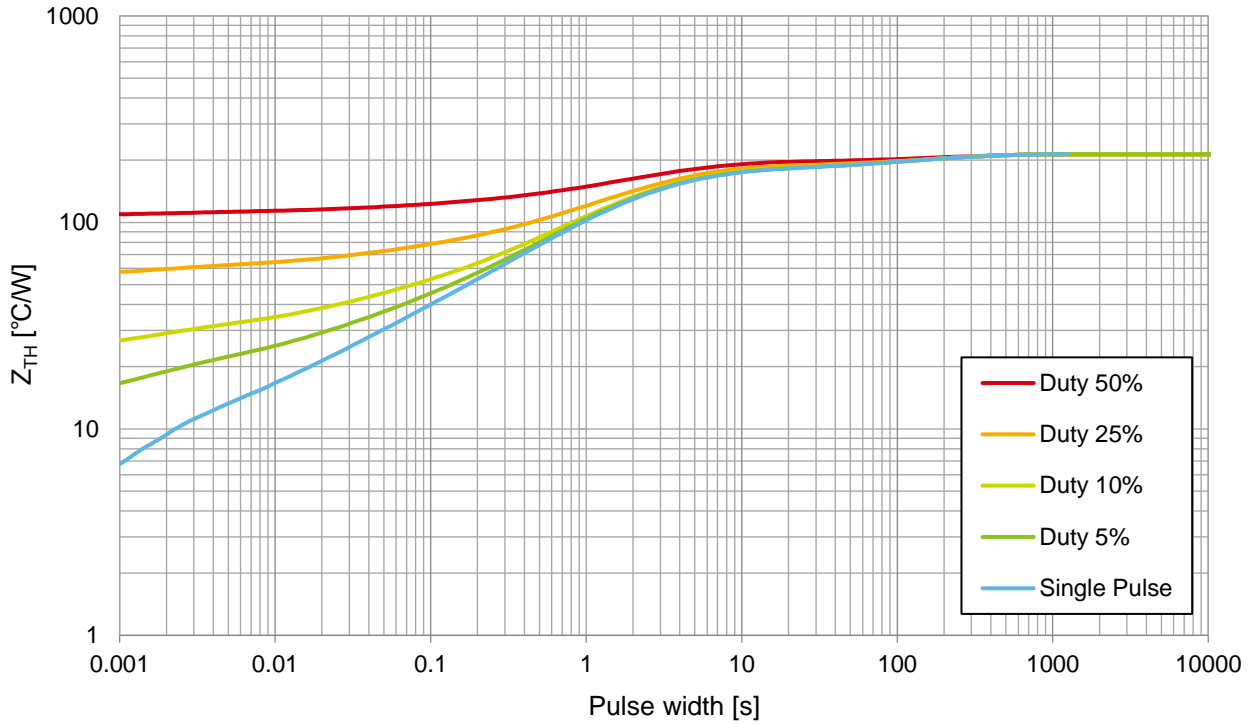


Figure 12. Transient thermal resistance, 2-layers, Copper foil bottom area 1200 mm<sup>2</sup>

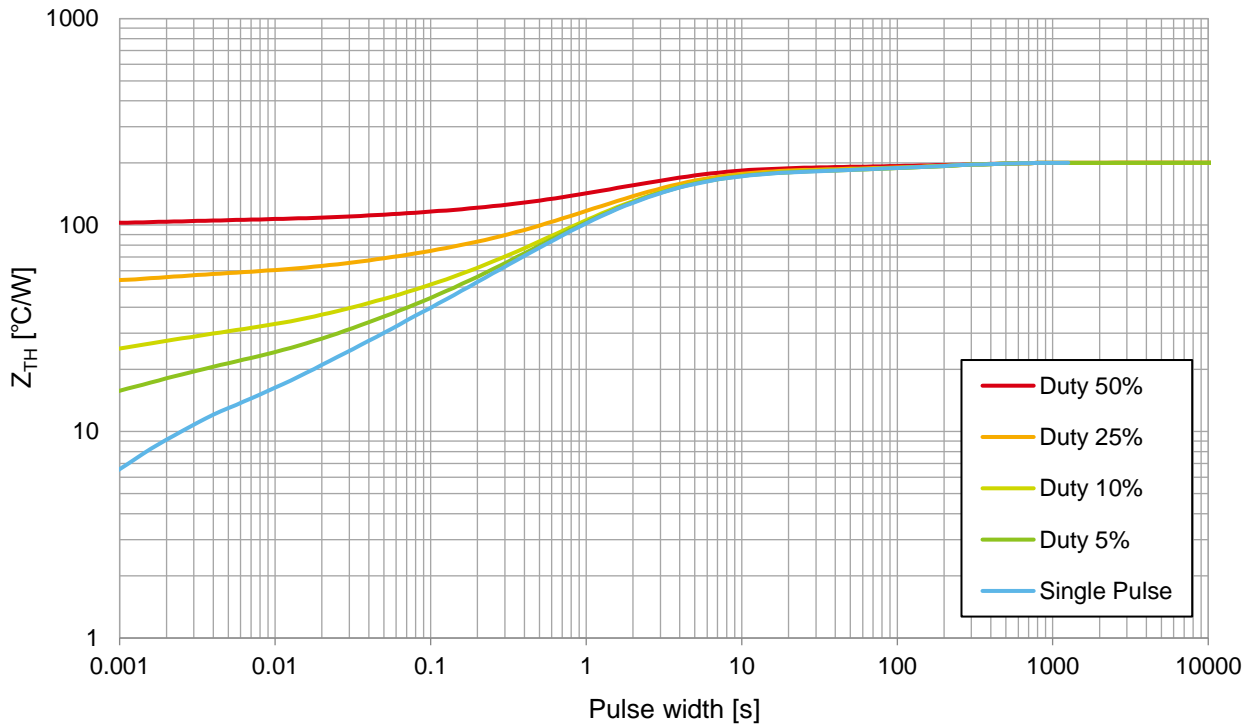


Figure 13. Transient thermal resistance, 2-layers, Copper foil bottom area 3000 mm<sup>2</sup>

Transient thermal resistance data, 2-layers, continued

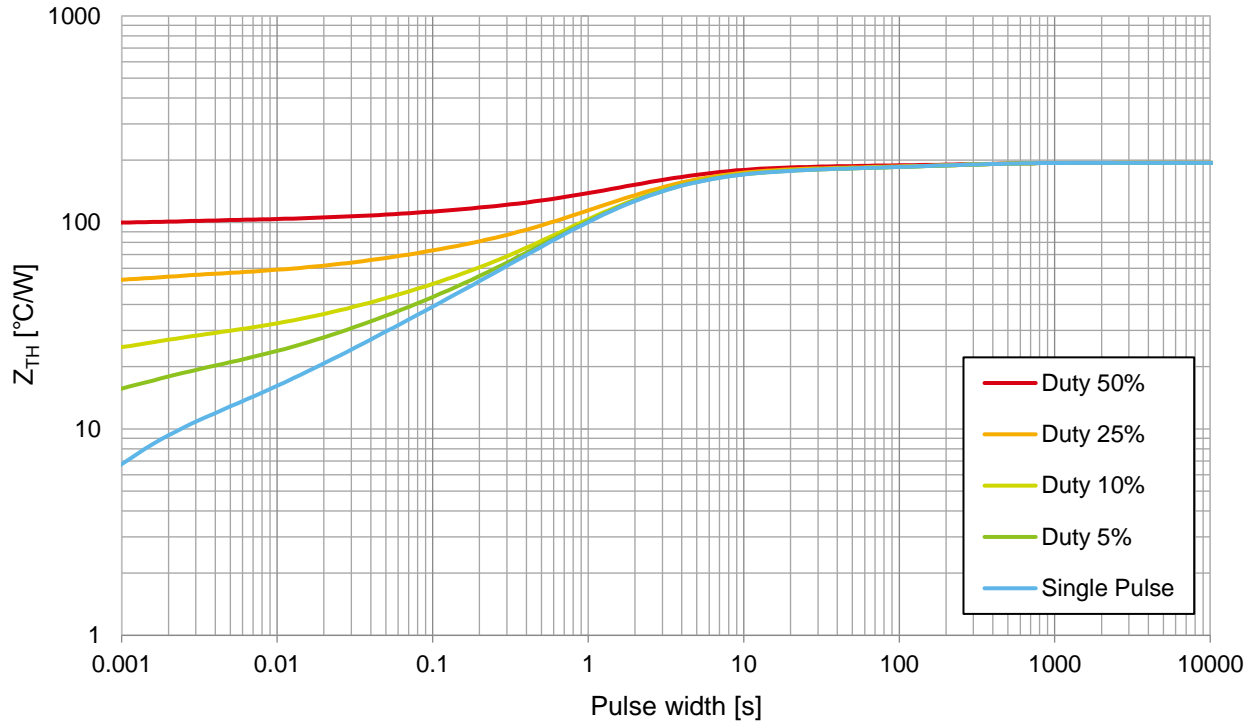


Figure 14. Transient thermal resistance, 2-layers, Copper foil bottom area 5505 mm<sup>2</sup>

Transient thermal resistance data, 4-layers (2s2p)

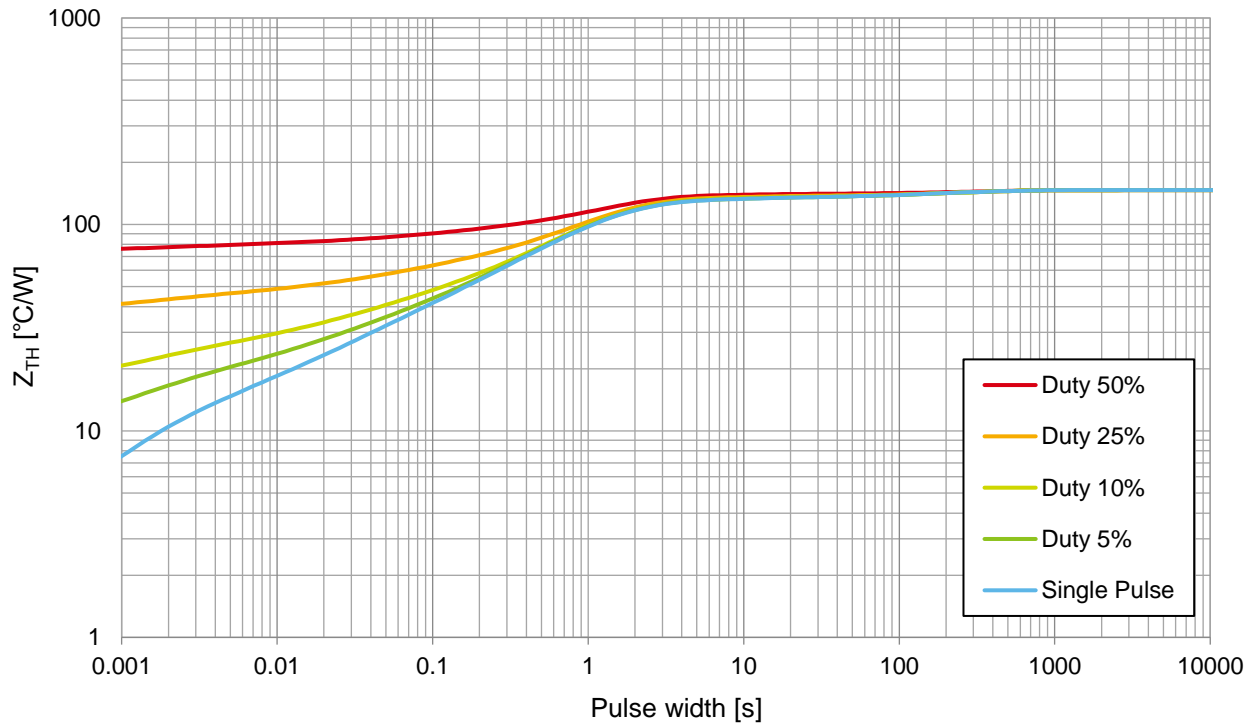


Figure 15. Transient thermal resistance, 4-layers

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