Linear Regulator Series

Power Source ON/OFF Characteristics for Linear Regulator

When a linear regulator IC is turned ON, the electric charge is stored in the output capacitor and the output voltage increases up to the specified value. At this time, an inrush current flows from the input to output of the IC. The output voltage drops when the input power source is disconnected. This application note explains the series of operations when the power source is turned ON/OFF.

Evaluation circuit

Figure 1 shows the typical circuit of a linear regulator to which an evaluation circuit of the startup characteristics is added. An inrush current is defined as a current flowing from the input to output of a linear regulator during the increase of voltage when the power is turned ON. The inrush current is primarily the total of the charging current and the load current to the output capacitor. As another external factor, the charging current to the input capacitor is also observed at the same time, making the separation of the waveforms difficult. For the IC with the enable control as shown in Figure 1, the input capacitor can be charged by applying the input voltage in advance. Then, the enable terminal voltage can turn ON the output, facilitating the measurement. For the IC without the enable control, it is necessary to reduce the inrush current to the input capacitor. This can be achieved either by changing the capacitance of the input capacitor to the minimum value that allows normal operation or replacing the input capacitor with a electrolytic capacitor that has a higher ESR value.

The waveforms of the enable control voltage and the output voltage are monitored at the voltage probes 1 and 2, respectively. The output current is measured on the input side with the current probe. The waveform is then observed using the channel of the voltage probe 1 on the oscilloscope as a trigger. For the IC without the enable control, the input voltage is measured instead of the enable control voltage with the voltage probe 1.

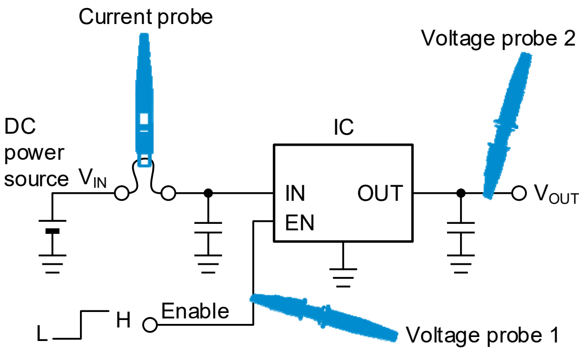


Figure 1. Evaluation circuit of the startup characteristics

When the current is measured between the IC output terminal and the output capacitor (phase compensation capacitor) as shown in Figure 2, the inductance component is added because of the wire for monitoring using the current probe gets longer. If the over current protection operates and suspends the output in this situation, resonance occurs to release the energy stored in the inductor and an oscillation-like waveform might be observed (Figure 3).

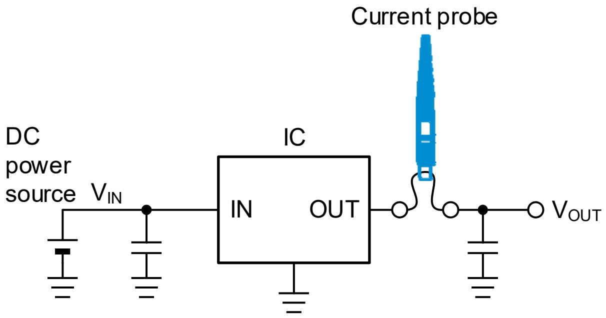


Figure 2. Evaluation circuit with the current monitored on the output side

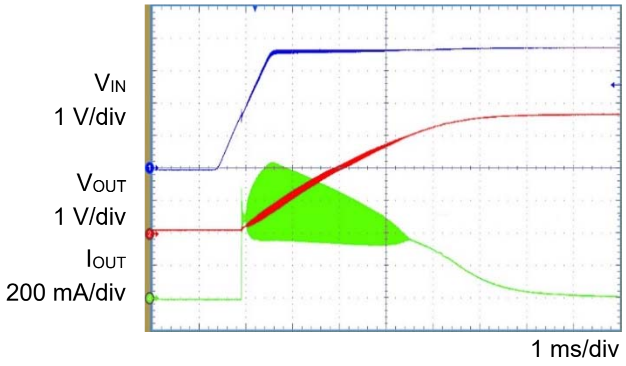


Figure 3. Resonance waveform caused by the measurement system

C_{OUT}=700 pF

Power source ON characteristics

Figure 4 shows the startup characteristics of a linear regulator IC with the over current protection having the shape of the letter “7” (top horizontal line connected with a diagonal line from lower left to upper right). The waveforms are the enable terminal voltage, the output voltage, and the output current from top to bottom. The enable voltage serves as a trigger. These characteristics are obtained when the output capacitance is 100 μF. Figure 5 shows the characteristic of the over current protection of the same linear regulator IC, drawing a curve in the shape of the letter “7” (fold back).

As the output voltage and current are both zero at the point (A) immediately before the IC is started up, the “7” curve starts from the lower left. The IC is started up when the enable terminal transits from low to high. Then, an inrush current flows to charge the output capacitor of the IC. The inrush current activates the over current protection circuit of the IC and the current is regulated to approximately 900 mA.

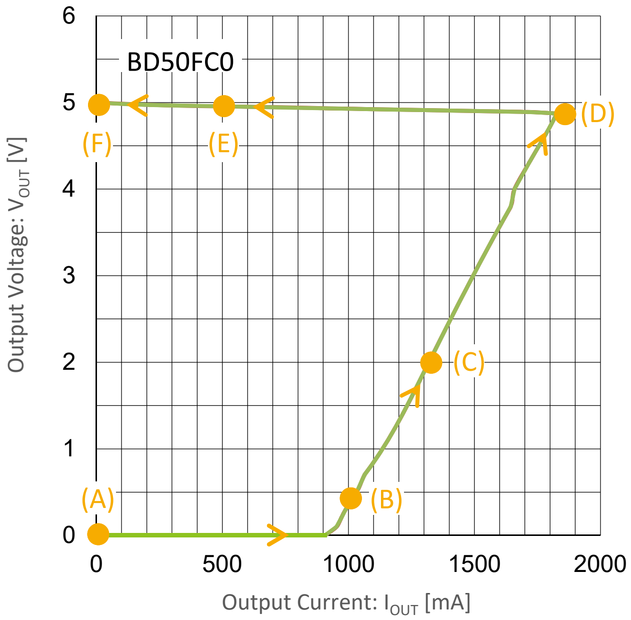


Figure 5. Characteristic of over current protection and the track of inrush current

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=100 μF

Then, the output voltage increases to the point (B). This accompanies the increase of the inrush current along the “7” curve. The output voltage and the inrush current further increase along the “7” curve to the points (C) and (D). At the point (D), it reaches the current limit value during the normal operation. When the output voltage approaches the specified value, the charging current to the output capacitor decreases to the points (E) and (F).

If the over current protection circuit of the linear regulator IC has such startup characteristics described as the letter “7”, the IC starts up while the output current is regulated to transit from the zero point along the “7” curve.

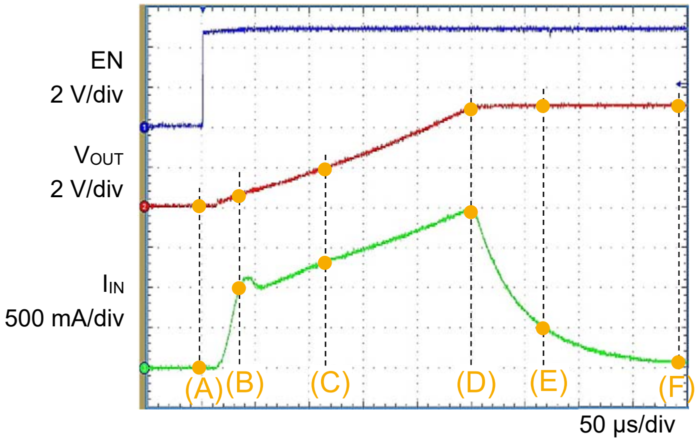


Figure 4. Startup characteristics

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=100 μF

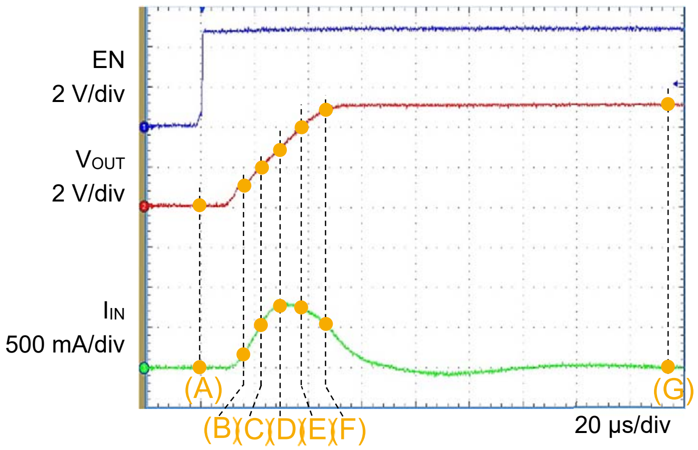


Figure 6. Startup characteristics

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=4.7 μF

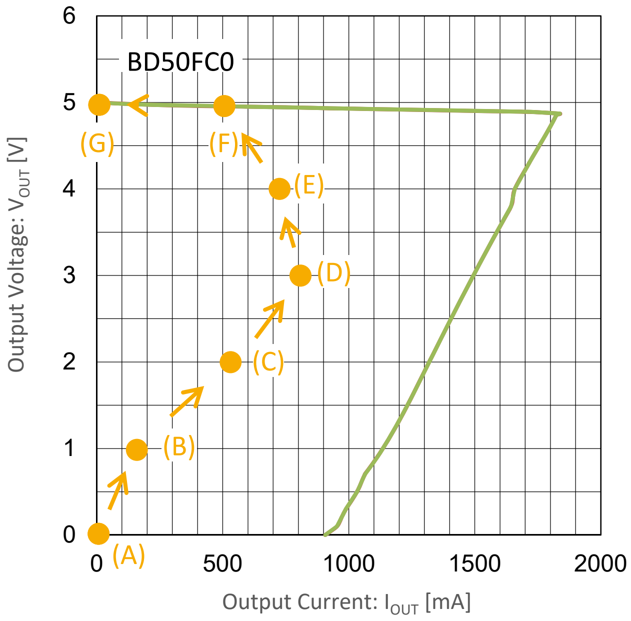


Figure 7. Characteristic of over current protection and the track of inrush current

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=4.7 μF

Figure 6 shows the startup characteristics when the output capacitance is decreased from 100 μF to 4.7 μF. By overlaying the characteristic of the over current protection and the track of the inrush current as shown in Figure 7, you can see that the IC with a lower output capacitance starts up without activating the over current protection to apply the current limit.

Next, we explain the startup time. From Figures 8 to 13, the startup waveforms are shown when the capacitance of the output capacitor is varied from 1 μF to 1,000 μF. When the capacitance of the output capacitor is between 1 μF and 10 μF, the inrush current during startup remains lower than the value that will activate the over current protection circuit and the current limit is not applied. Therefore, the output voltage increases with the rise time of the internal reference-voltage of the IC. Since the startup times are the same, it is clear that the values of inrush current depend on the output capacitance values. When the capacitance of the output capacitor is between 47 μF and 1,000 μF, the current limit is applied on the inrush current by the over current protection circuit. When the over current protection circuit is activated, the current limit is applied along the “7” curve as previously shown in Figure 5. The charging current to the capacitor is then limited accordingly, making the startup time longer. In summary, if the inrush current during startup is smaller than the value that will activate the over current protection circuit, the startup time depends on the startup time of the internal reference-voltage of the IC, but not on the capacitance value of the output capacitor. On the other hand, if the inrush current during startup is large enough to activate the over current protection circuit, the startup time becomes longer as the capacitance value of the output capacitor becomes larger.

So far, we have explained the startup characteristics when the enable terminal is controlled. However, the power source of the input rises during startup if the enable control function is not available. In this case, the inrush current flows into the input capacitor as well. When the power source is tuned ON, the capacitor is short-circuited as it is being charged from 0 V to the specified voltage. Therefore, the peak current is given as [Input voltage/Capacitor ESR], causing a larger current for the capacitor with a lower ESR (Figure 14).

Figure 15 shows the startup waveforms when a ceramic capacitor is used for the input. The 10 μF ceramic capacitor used in the experiment has an ESR of approximately 3mΩ. Therefore, the peak current is calculated to be 4,000 A when the power source voltage of 12 V is applied, creating a short circuit between the power source and the ground. In the actual waveform, the peak current value reaches 12 A at the power source voltage of 5 V and then drops sharply. The peak current is determined by the maximum value of the power source capability on the supply side. The current suddenly disappears as soon as the charging to the input capacitor is completed, resulting in a large ringing. It is followed by the inrush current to the output capacitor. Thus, if the power source line with a low ESR capacitor is raised rapidly, a large inrush current flows, which may cause damage to the power source on the supply side or activate the over current protection circuit to suspend the supply. To reduce the peak value of the inrush current, it is necessary to reduce the voltage rise rate through design.

Figure 16 shows the startup waveforms when an aluminum electrolytic capacitor is used for the input. The 10 μF aluminum electrolytic capacitor used in the experiment has an ESR of approximately 1Ω. Therefore, the peak current is calculated to be 12 A when a voltage of 12 V is applied. In the actual waveform, the peak current value reaches 9 A at the power source voltage of 9 V and the charging of the capacitor is completed. The following waveform continues to the inrush current to the output capacitor. Although the peak current can be reduced compared with the ceramic capacitor, the same problem as described above may occur if the current capability of the supply side is insufficient. Therefore, it is necessary to consider the design that addresses the issues related to the rise rate of the power source.

In either case, the charging currents to the input and output capacitors can be observed at the same time for the IC without the enable control, making the separation difficult. It is necessary to change the value of the input capacitor to the minimum value that allows normal operation or monitor the current on the output side (Figure 2).

Power source ON characteristics with soft start function

The soft start function can reduce the peak value of the charging current to the output capacitor by increasing the output voltage slowly. In the IC where the soft start time is fixed inside (e.g., BDxxGC0, BDxxGA5, BDxxGA3, BDxxHC5, BDxxHC0, BDxxHA5, BDxxHA3, BDxxIC0, and BDxxIA5), the charging may not be completed within the soft start time if a larger value of the output capacitor results in a larger charging current and the over current protection circuit is activated to apply the current limit. Now we will explain these characteristics.

From Figures 17 to 22, the startup waveforms are shown when the output capacitor is varied from 10 µF to 1,000 µF.

First, the startup sequence is explained for the capacitor with a capacitance of 10 µF as shown in Figure 17. The output voltage starts increasing slowly with a constant slope under the enable control. This slope is set by the soft start control, and the rise rate is designed to be 800 µs for this IC (the time for the voltage to reach 95% of the specified voltage). After the output voltage has risen by 0.1 V, an inrush current of 116 mA is observed. This inrush current is caused by the operation delay of the soft start circuit and the current is reduced after it become possible to control the output (section (A)). Then, the output voltage increases with time at a constant slope while the output current remains constant (section (B)). Namely, the peak current is regulated to 42 mA. As the output voltage approaches the specified value, the rise rate of the soft start circuit is decreased and the output current starts to decrease (section (C)).

Figure 18 shows the waveforms when the capacitance of the output capacitor is increased to 100 µF. Compared with the case of 10 µF, the output current is increased since it requires more electric charge to charge the capacitor. However, the peak current is regulated to 350 mA. The inrush current seen in Figure 17 is not observed immediately after the enable control since the inrush current is masked by a larger peak current that flows after the enable control.

Figure 19 shows the waveforms when the capacitance of the output capacitor is increased to 220 µF. Compared with the case of 100 µF, the output current is increased since it requires further electric charge to charge the capacitor. However, the peak current is regulated to 840 mA.

Under the conditions for Figures 17 to 19, by overlaying the characteristic of the over current protection and the track of the inrush current, you can see that the IC starts up without activating the over current protection to apply the current limit as shown in Figure 23. In addition, the output voltage increases with the soft start time of approximately 800 µs, which is the specified value, since the current limit is not applied.

Figure 20 shows the startup waveforms when the capacitance of the output capacitor is increased to 330 µF. Compared with the case of 220 µF, the output current is further increased since it requires more electric charge to charge the capacitor. As a result, the over current protection circuit is activated and the output voltage is increased while the output current is regulated (section (A)). As the output voltage approaches the specified value, it is still within the soft start rise time (800 µs). Therefore, the soft start circuit continues to operate and the output current starts to decrease (section (B)).

Under the conditions of Figure 20, overlaying the characteristic of the over current protection and the track of the inrush current gives Figure 24. In the section (A) of Figure 20, the output voltage increases along the “7” curve while the current limit is applied. In the section (B), the current limit is lifted and it enters the final stage of the soft start operation.

Figures 21 and 22 show the startup waveforms when the capacitance of the output capacitor is 470 µF and 1,000 µF, respectively. Compared with the case of 330 µF, the charging current is further increased in both cases. Therefore, the current limit is constantly applied by the over current protection circuit during the startup. This situation is similar to the operation without the soft start function described above, and the startup time becomes longer as the capacitor value is increased (Figure 5, Figures 11 to 13).

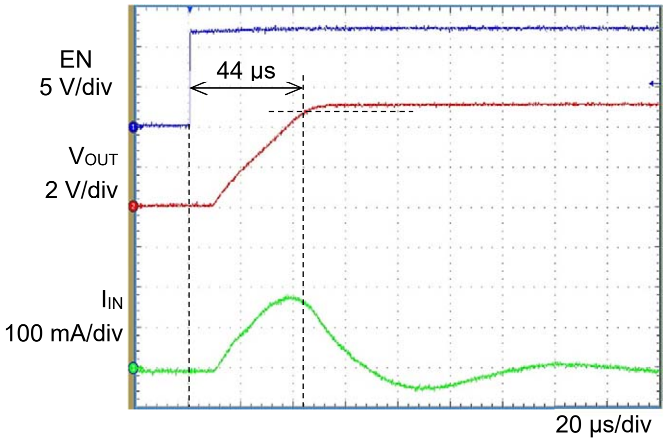


Figure 8. Startup waveforms

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=1 µF

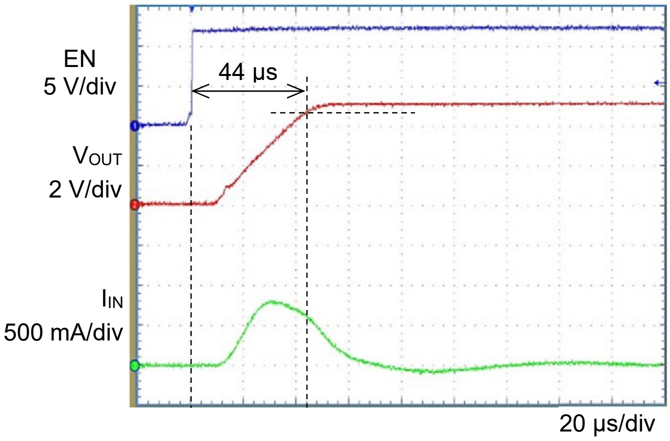


Figure 9. Startup waveforms

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=4.7 µF

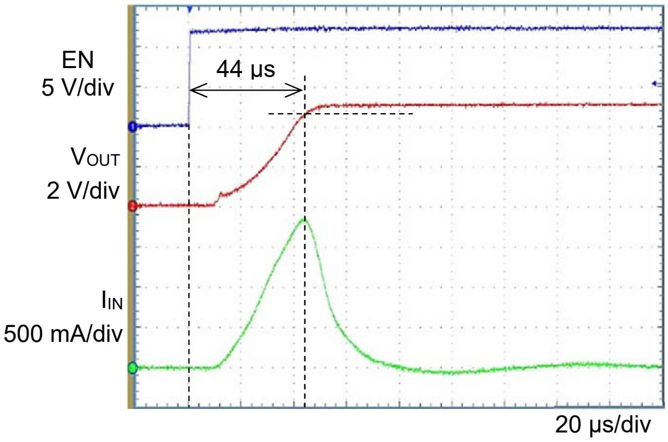


Figure 10. Startup waveforms

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=10 µF

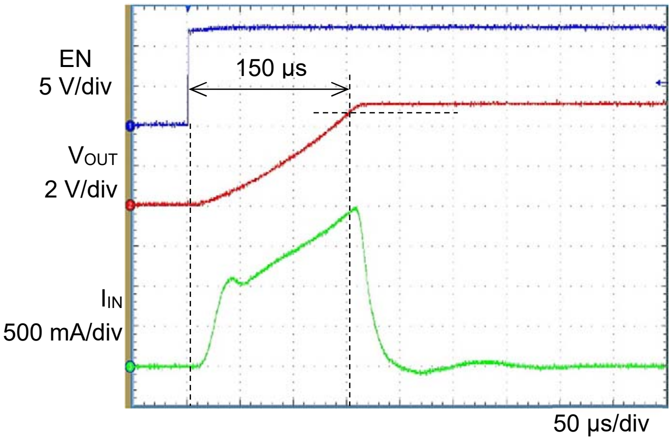


Figure 11. Startup waveforms

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=47 µF

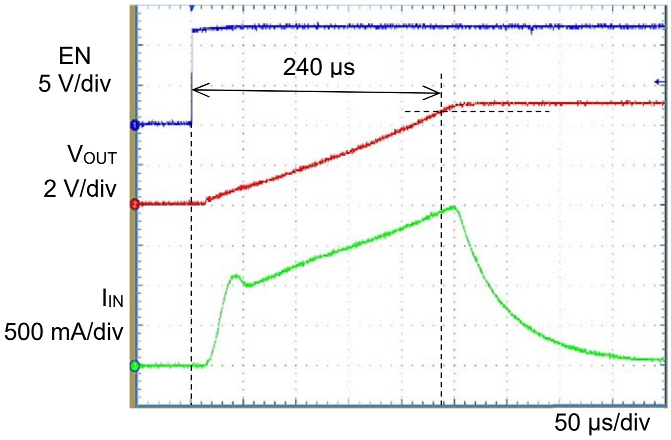


Figure 12. Startup waveforms

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=100 µF

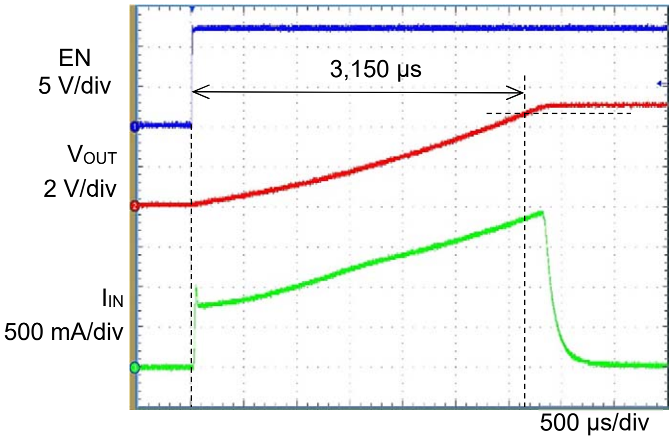
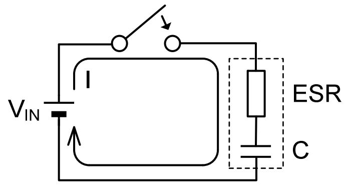


Figure 13. Startup waveforms

V_{IN}=12 V, V_{OUT}=5 V, C_{OUT}=1,000 µF



$$I = \frac{V_{IN}}{ESR}$$

Figure 14. Inrush current to the capacitor

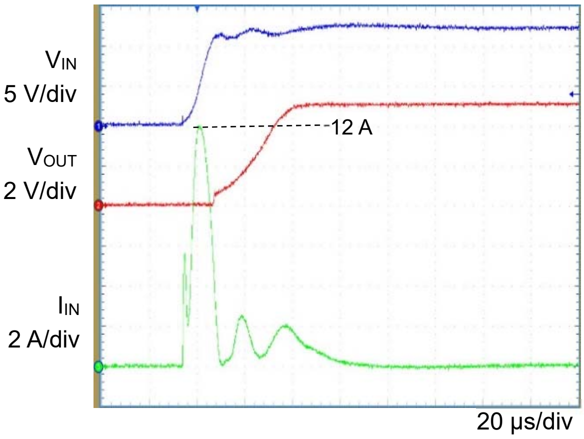


Figure 15. Startup waveforms when a ceramic capacitor is used for the input

V_{IN}=12 V, V_{OUT}=5 V, C_{IN}=10 µF, C_{OUT}=10 µF

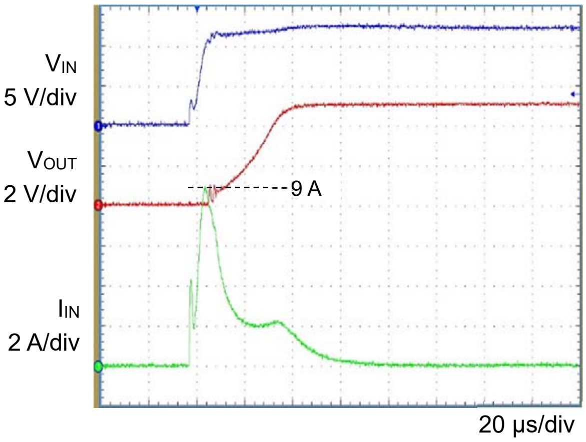


Figure 16. Startup waveforms when an aluminum electrolytic capacitor is used for the input

V_{IN}=12 V, V_{OUT}=5 V, C_{IN}=10 µF, C_{OUT}=10 µF

So far, we have explained the soft start characteristics with the enable control. Next, the startup waveforms when the rise time of the input power source (V_{IN}) is longer than that of the soft start (800 µs) are shown in Figures 25 and 26. As for the measurement conditions, the enable terminal of the IC is connected to the input voltage. Since the enable threshold voltage for the IC is approximately 1.6 V, the output is OFF when the input voltage is below 1.6 V. In the section (A), the input voltage starts increasing, but the output is still zero since the voltage is below 1.6 V. An inrush current to the input capacitor is also observed. In the section (B), the input voltage exceeds 1.6 V and the output is turned ON. Since the output increases rapidly, an inrush current of 680 mA is observed. As the increase of the output voltage becomes slower, the current decreases. In the section (C), the output voltage increase slowly following the increase of the input voltage. Therefore, the inrush current to the output capacitor becomes small, ranging between 10 mA and 30 mA. In summary, when the rise time of the input power source is longer than that of the soft start (800 µs), the rise time of the input power source determines the rise time of the output.

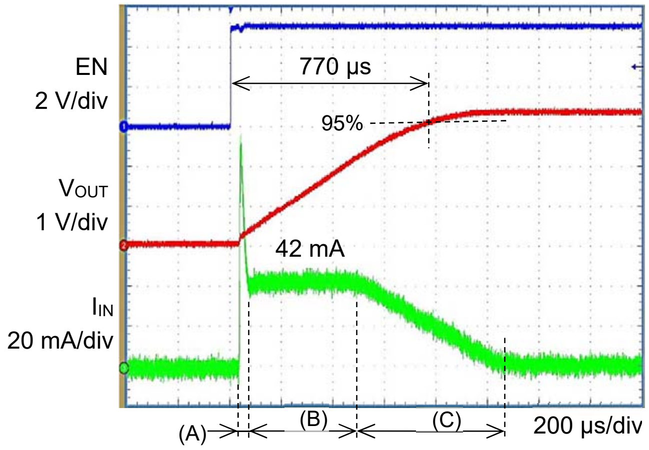


Figure 17. Startup waveforms

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=10 µF

(BD33IC0WEFJ)

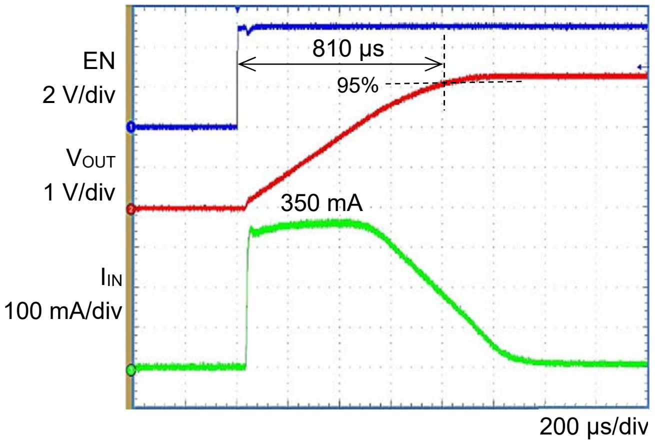


Figure 18. Startup waveforms

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=100 µF

(BD33IC0WEFJ)

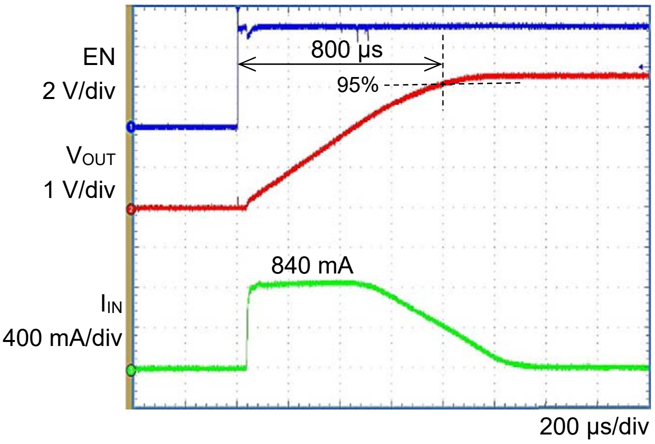


Figure 19. Startup waveforms

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=220 µF

(BD33IC0WEFJ)

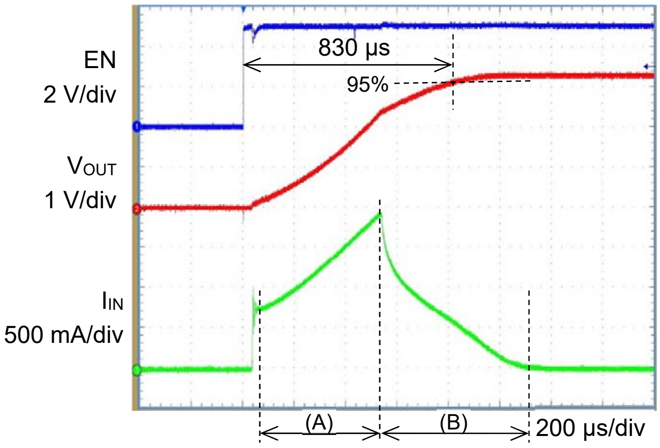


Figure 20. Startup waveforms

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=330 µF

(BD33IC0WEFJ)

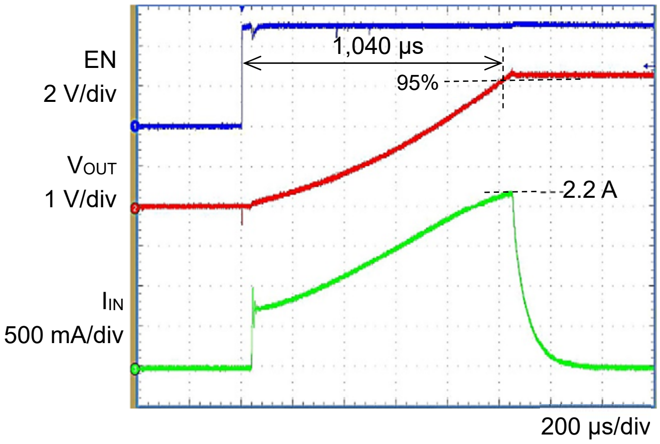


Figure 21. Startup waveforms

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=470 µF

(BD33IC0WEFJ)

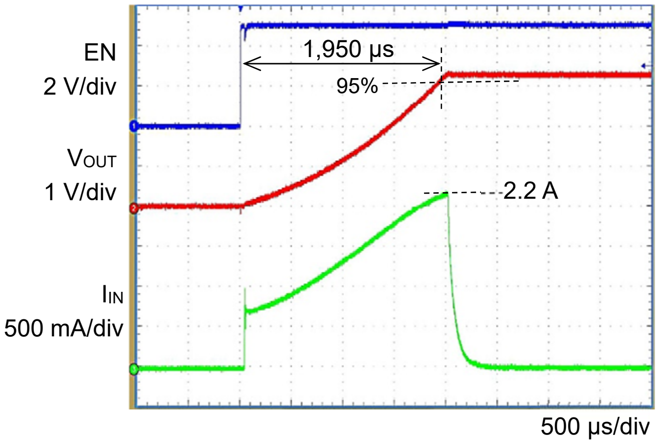


Figure 22. Startup waveforms

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=1,000 µF

(BD33IC0WEFJ)

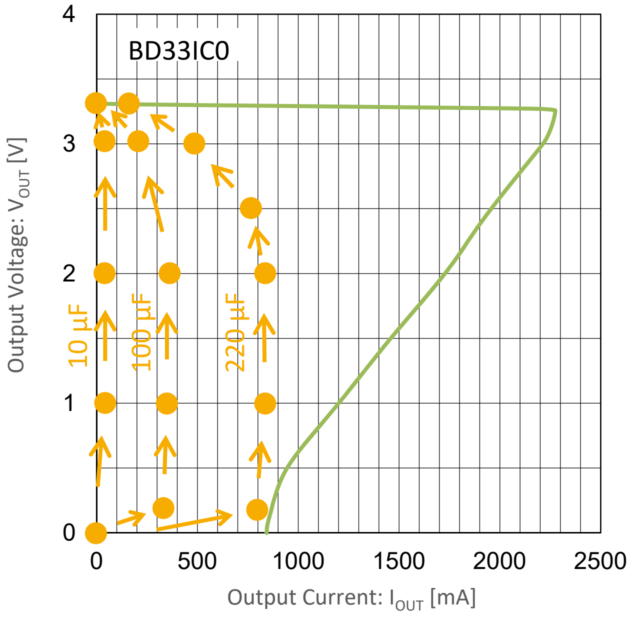


Figure 23. Characteristic of over current protection and the track of inrush current

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=10 μF, 100 μF, 220 μF

(BD33IC0WEFJ)

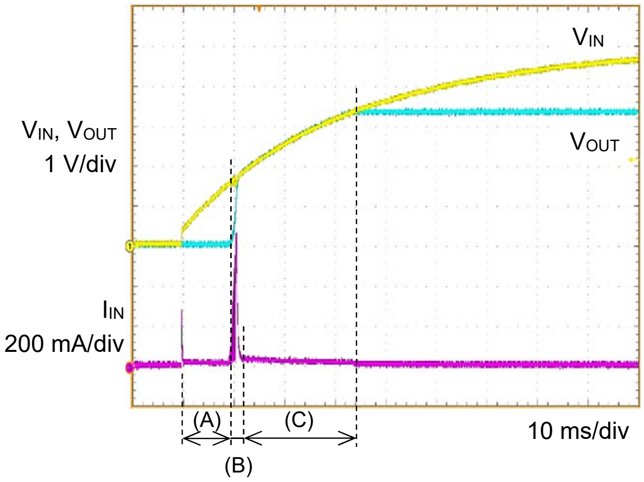


Figure 25. Startup waveforms

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=220 μF

(BD33IC0WEFJ, EN=V_{IN})

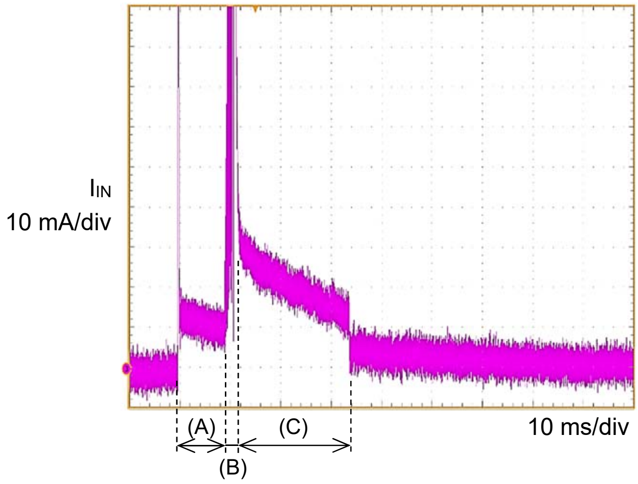


Figure 26. Startup waveform of I_{OUT}, the vertical axis magnified

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=220 μF

(BD33IC0WEFJ, EN=V_{IN})

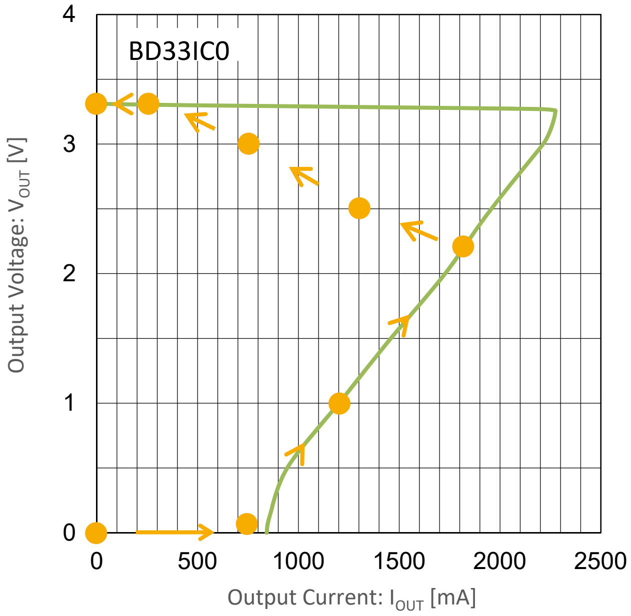


Figure 24. Characteristic of over current protection and the track of inrush current

V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=330 μF

(BD33IC0WEFJ)

Power source OFF characteristics

Figure 27 shows the waveforms when the output is turned OFF under the enable control. This is a non-load situation where the electric charge in the output capacitor is discharged through the feedback resistor between the output terminal and the ground. If there is a load, the discharge time is reduced according to the load resistance. For a simple resistance, the discharge time can be calculated with the following equation.

$$t = -CR \times \ln\frac{V_C}{V_O} \quad [sec] \tag{1}$$

C : Capacitance of the output capacitor $[F]$
R : Load resistance $[\Omega]$
V_O : Output voltage $[V]$
V_C : Voltage after discharge $[V]$

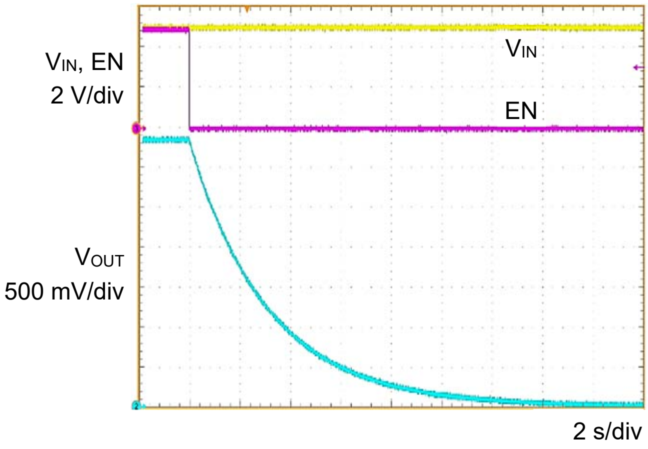


Figure 27. Waveforms when the power source is turned OFF under EN control
V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=220 μF, no load
(BD33IC0WEFJ)

Figure 28 shows the output waveforms when the input voltage is decreased steeply. The LDO used in this example has the MOS-type output Tr, and the parasitic diode exists in parallel to the Tr. The polarity of the diode sets the output and input sides as the anode and cathode, respectively. Therefore, when the input voltage is decreased, the output voltage decreases following the input voltage. When the input voltage is decreased to 0 V, the output voltage remains at the forward direction voltage of the parasitic diode and decreases slowly. Then, the voltage decreases in time constant with the load resistance.

Figure 29 shows the output waveforms when the input voltage is decreased slowly. Since the output Tr is saturated when the input voltage decreases to the same value as the output voltage, the output voltage decreases following the input voltage. The decrease of the output voltage becomes rather slow temporarily when the input voltage reaches 1.6 V. This is because the enable threshold voltage of the LDO used in this example is 1.6 V, and the LDO output becomes high impedance at this point. The rest is the same as shown in Figure 28: when the input voltage is decreased, the output voltage decreases following the input voltage due to the parasitic diode of the output Tr. When the input voltage is decreased to 0 V, the output voltage remains at the forward direction voltage of the parasitic diode and decreases more slowly. Then, the voltage decreases in time constant with the load resistance.

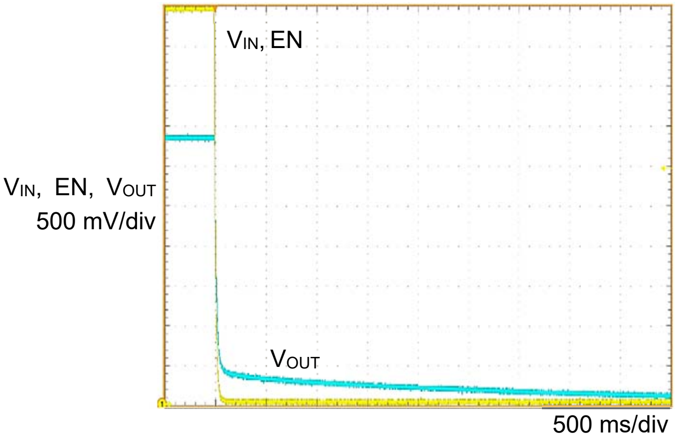


Figure 28. Waveforms when the power source is turned OFF and the input is decreased steeply
V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=220 μF, no load
(BD33IC0WEFJ, EN=V_{IN})

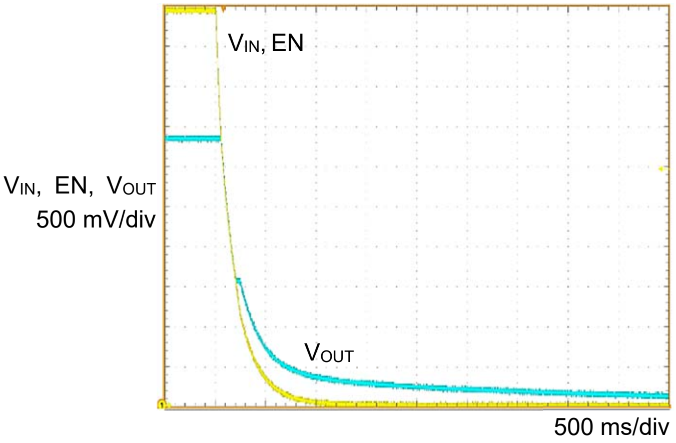


Figure 29. Waveforms when the power source is turned OFF and the input is decreased slowly
V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=220 μF, no load
(BD33IC0WEFJ, EN=V_{IN})

Figure 30 shows the waveforms when the supply from the power source is suspended with the input being in an open state. Since the electric charge in the input capacitor is consumed by the operation current of the IC, the input voltage is decreased. Since the output Tr is saturated when the input voltage decreases to the same value as the output voltage, the output voltage decreases following the input voltage. When the input voltage reaches 1.6 V, which is the enable threshold voltage, the current consumption by the IC becomes zero. Then, the decrease of the input voltage becomes slow and the electric charge in the input capacitor is discharged naturally. As for the output voltage, this is a non-load situation where the electric charge in the output capacitor is discharged through the feedback resistor between the output terminal and the ground.

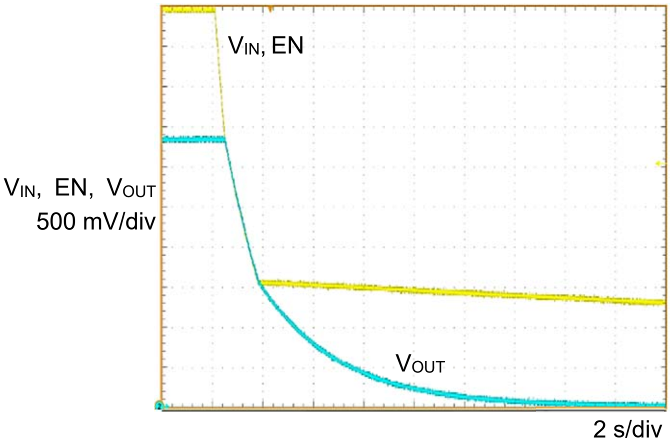


Figure 30. Waveforms when the power source is turned OFF with the open input
V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=220 μF, no load
(BD33IC0WEFJ, EN=V_{IN})

Power source OFF characteristics with output discharge function

Figure 31 shows the waveforms when the power source is turned OFF for the LDO equipped with the output discharge function. When the enable control is turned OFF, the output Tr is turned OFF and the low resistance resistor between the output terminal and the ground is switched ON at the same time to rapidly discharge the electric charge in the output capacitor (Figure 32). The discharge time can be calculated with Equation 1 described above. The output discharge circuit operates when the enable control is activated with the IC being supplied with the power source (input voltage). The discharge circuit does not operate when the input voltage drops, thus providing the normal characteristics when the power source is turned OFF as shown in Figures 28 and 29.

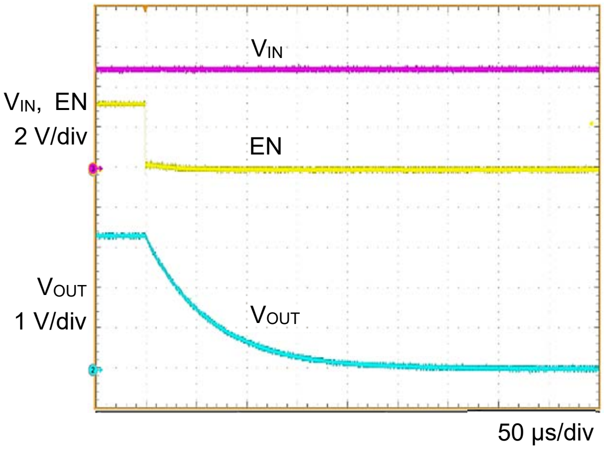


Figure 31. Waveforms when the power source is turned OFF for the LDO equipped with the output discharge function.
V_{IN}=5 V, V_{OUT}=3.3 V, C_{OUT}=2.2 μF, no load
(BU33TD3WG)

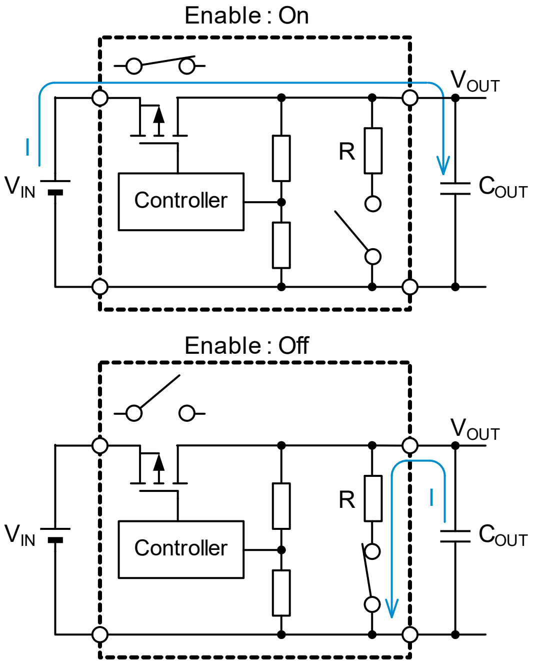


Figure 32. Output discharge function

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
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4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

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6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

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