Linear Regulator Series

BAxxCC0 Series Circuit Using a Ceramic Output Capacitor

The BAxxCC0 series are IC that were designed in an era when large capacitance multilayer ceramic capacitors (MLCC) or low ESR aluminum electrolytic capacitors were not common. These IC utilize the ESR (equivalent series resistance) value of the output capacitor to perform the phase compensation of the loop. The ESR value of the output capacitor has a range in which the operation is stable. Therefore, if an ultra-low ESR ceramic capacitor or low ESR aluminum electrolytic capacitor is used as the output capacitor, the phase compensation cannot be performed properly, causing an abnormal oscillation. Standard aluminum electrolytic capacitors generally show a characteristic that causes the capacitance to decrease and the ESR to increase at low temperature. In addition, it is difficult to select parts since the ESR increases over time due to the drying up of the electrolyte. On the other hand, ceramic capacitors show excellent properties with respect to the variation in capacitance and the ESR, allowing stable use if the ESR issue is resolved. This application note proposes a circuit using an output ceramic capacitor that allows a stable phase compensation.

Phase compensation in BAxxCC0 series

Regulators with the NPN-type output mode have a low output impedance due to their collector-grounded structure. Therefore, the pole by the power step that exists in the loop gain (referred to as the second pole P_2 or the power pole P_{PWR}) occurs at a high frequency. Since this type of LDO has no pole at a low frequency, the phase compensation is performed by generating a pole inside the IC (the first pole P_1) at a low frequency (Figure 1).

In Figure 1, the first pole P_1 is at 100 Hz and the gain decreases at a rate of −20 dB/dec as the frequency increases. The second pole P_2 is at 1 MHz and the gain decreases at a rate of −40 dB/dec above this frequency. Next, as for the phase change, a phase delay of −90° occurs at the first pole P_1, and another phase delay of −90° occurs at the second pole P_2. The phase margin at 0 dB is checked for judging the stability. The 0 dB crossover frequency f_C is 95 kHz, giving the phase margin of 84°. Also, since the frequency of the second pole P_2 is high at 1 MHz, the phase delay by this pole does not affect the crossover frequency f_C significantly. Therefore, the loop can be judged to be stable.

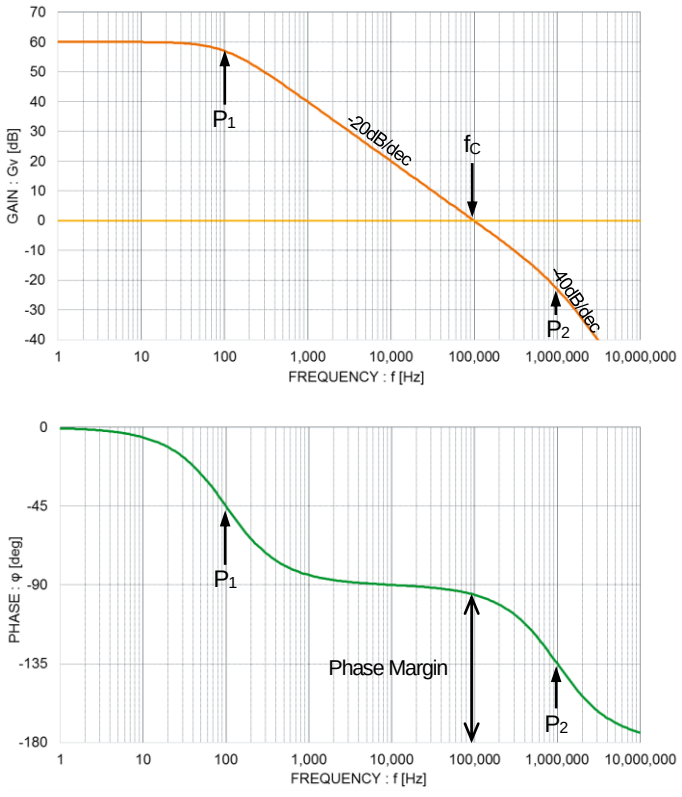

Figure 1. Bode plot for NPN-type LDO

Since the output mode of the BAxxCC0 series is composed of the emitter-grounding of the PNP transistor, the output impedance is high at several tens of kΩ (Figure 2).

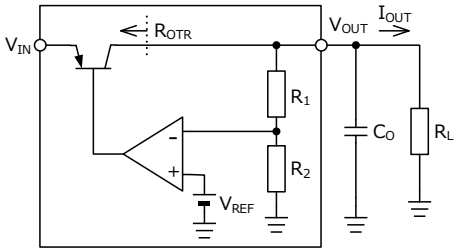

Figure 2. Circuit diagram of BAxxCC0 series LDO

Therefore, the load pole P_L is formed at a low frequency that depends on the load resistance and the output capacitance. The frequency of this pole can be calculated with the following equations.

$$P_L = \frac{1}{2\pi \cdot R_O \cdot C_O} \quad [Hz]$$

C_O : Output capacitor $[F]$

R_O : Impedance of the output node $[\Omega]$

$$R_0 = \frac{1}{\frac{1}{R_L} + \frac{1}{R_1 + R_2} + \frac{1}{R_{OTR}}} \quad [\Omega]$$

R_L : Load resistance $[\Omega]$

R_1, R_2 : Resistor divider circuit $[\Omega]$

R_{OTR} : Output impedance of the transistor $[\Omega]$

When $R_L \ll (R_1, R_2, R_{OTR})$,
the pole frequency can be calculated with the following equation.

$$P_L = \frac{1}{2\pi \cdot R_L \cdot C_O} \quad [Hz]$$

Figure 3 is a Bode plot showing that the load pole P_L appears at a lower frequency according to the equation above in addition to the first pole P_1. Since these two poles produce a secondary phase delay, the phase delay reaches −180° at the crossover frequency f_C to cause an oscillation in the loop. Therefore, it is necessary to compensate for the phase advance of +90° by adding a zero point to the loop in order to operate this type of LDO stably.

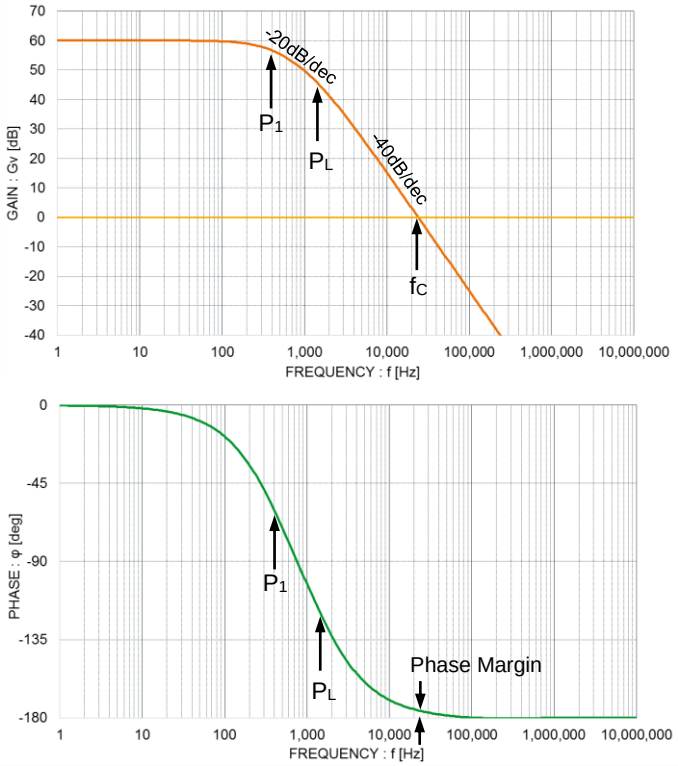

Figure 3. Bode plot for PNP-type LDO
Without phase compensation

Phase compensation using the ESR of the output capacitor

The zero point is added to reduce the phase delay by using the ESR of the output capacitor. Figure 4 shows a simple equivalent circuit of a capacitor. Standard aluminum electrolytic capacitors have ESR values of a few Ω to several tens of Ω. On the other hand, ceramic capacitors have ultra-low ESR values of a few mΩ. ESL is an equivalent series inductance that represents the inductance components of the capacitor lead and the electrode wiring. Since the value is small, between a few nH and a few μH, it does not affect the phase compensation below 1 MHz.

Figure 4. Simple equivalent circuit of a capacitor

Since the phase compensation by the ESR is a parasitic element of the output capacitor as shown in Figure 5, it is usually omitted from the circuit diagram. The zero frequency can be calculated with the following equation. Since the constants (capacitance and ESR) are directly involved in determining the zero frequency, the characteristics of the output capacitor become particularly important factors.

$$ZERO = \frac{1}{2\pi \cdot C_O \cdot ESR} \quad [Hz]$$

C_O : Output capacitor $[F]$

ESR : ESR of the output capacitor $[\Omega]$

A zero point is added to the Bode plot in Figure 3. Assuming C_O = 22 µF and ESR = 1Ω, a zero frequency of 7.2 kHz is obtained. The Bode plot to which this zero point is added is shown in Figure 6. Similar to Figure 3, the two poles, the first pole P_1 and the load pole P_L, at low frequencies produce the secondary phase delay. By placing a zero point at 7.2 kHz, a phase advance of +90° is inserted to reduce the phase delays that occur at the first pole P_1 and the load pole P_L. As a result, the bandwidth of the loop is broadened, the 0 dB crossover frequency shifts from 23 kHz to 64 kHz, and a phase margin of 52° is secured. In addition, since the power pole P_{PWR} is at a higher frequency than the crossover frequency, its influence on the phase delay is limited. Since the frequencies of each of the poles and the zero point are close, the gain plot does not have exact straight lines, for example, with a slope of −20 dB/dec or −40 dB/dec. Instead, the plot presents a curve that combines each of the slopes.

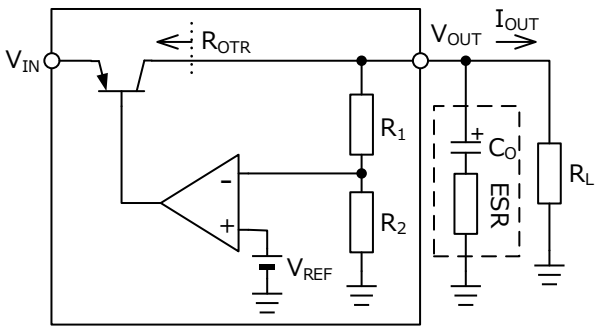

Figure 5. Phase compensation by ESR

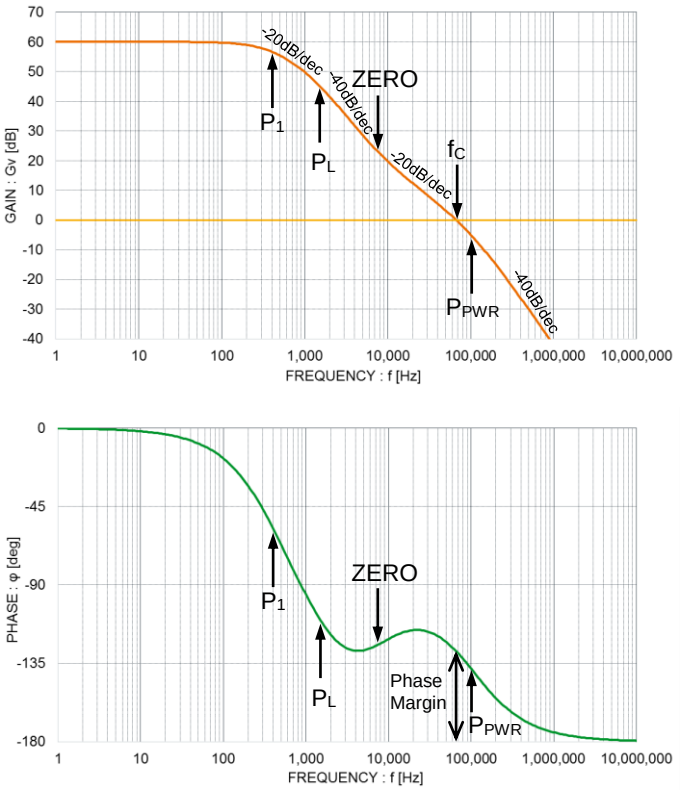

Figure 6. Bode plot for PNP-type LDO
Phase compensation by ESR, C_O = 22 µF, ESR = 1Ω

ESR and stability

When an aluminum electrolytic capacitor is used in practice, the important parameters relevant to the zero frequency are varied. For example, different series of capacitors may have different values of ESR or the temperature characteristics may change the ESR. Since the phase margin may be decreased and cause an abnormal oscillation if the ESR is varied too widely, the IC data sheet provides the plot of the safe operation range for the ESR. Next, it will be explained why the phase compensation cannot be achieved when the ESR is too low or too high beyond the safe operation range.

Low ESR

In Figure 6, the phase compensation is performed using an output capacitor with an ESR of 1Ω. In Figure 7, the Bode plot is shown when the phase compensation is performed using a capacitor with an ESR of 0.1Ω. As the ESR is reduced, the zero frequency increases to 72 kHz. The phase compensation with a zero point is performed after the phase delay of −180° is produced by the two poles, the first pole P_1 and the load pole P_L. Therefore, the phase is not recovered sufficiently and the phase margin is lost, making the loop unstable.

This condition is observed when low ESR aluminum electrolytic capacitors are used. Also, the zero frequency further increases when ultra-low ESR ceramic capacitors are used, resulting in a condition where no phase compensation is achieved as in Figure 3.

High ESR

Next, the Bode plot when the ESR is increased to 20Ω is shown in Figure 8. Compared with the case when the ESR is 1Ω (Figure 6), the zero frequency is reduced from 7.2 kHz to 360 Hz. As a result, the 0 dB crossover frequency increases from 64 kHz to 374 kHz. The phase delay produced by the two poles, the first pole P_1 and the load pole P_L, is compensated for by the phase advance at the zero point. However, since the 0 dB crossover frequency exceeds the frequency of the power pole P_{PWR}, the pole produces a phase delay. As a result, the phase margin is decreased to 15°, making the operation unstable.

Aluminum electrolytic capacitors have a characteristic that causes the ESR to increase at low temperature. In addition, the electrolyte dries up over time and increases the ESR. In such condition, it is expected that the zero frequency will decrease and make the operation unstable.

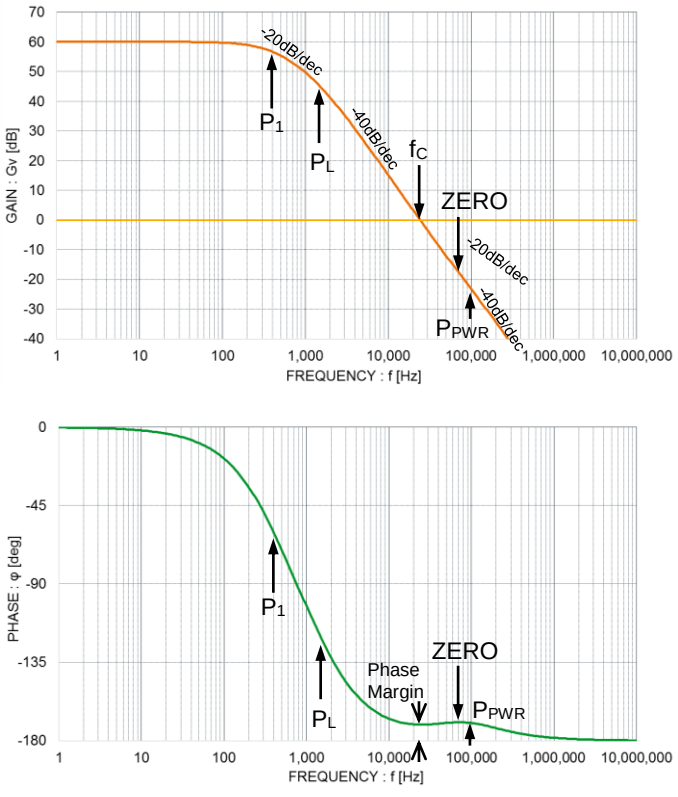

Figure 7. Compensation by low ESR

C_O=22μF、ESR=0.1Ω

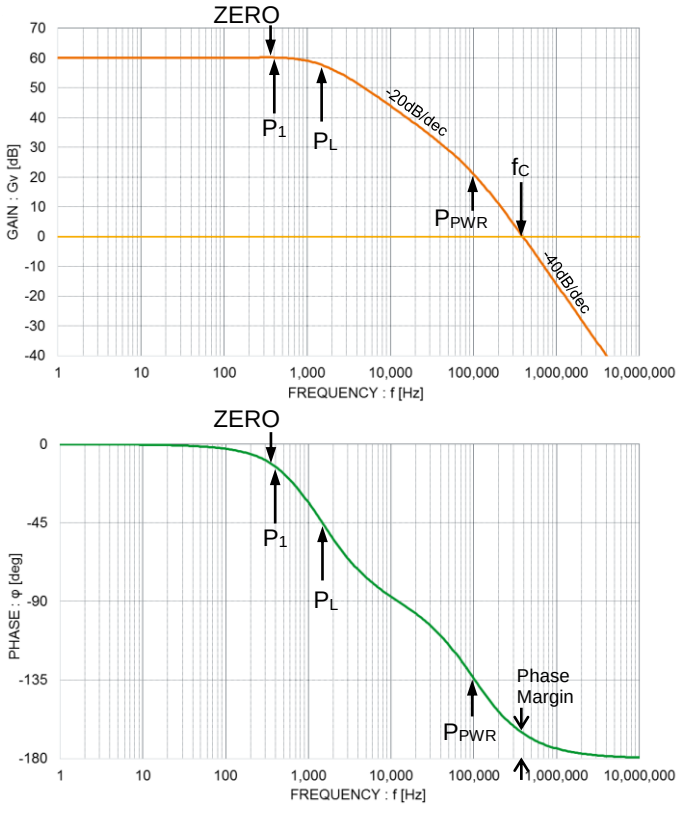

Figure 8. Compensation by high ESR

C_O=22μF、ESR=20Ω

Circuit using a ceramic capacitor

The ceramic capacitors with X5R and X7R characteristics are superior to aluminum electrolytic capacitors in both temperature characteristics and aging. Therefore, such a ceramic capacitor is a good choice for the IC if the stability of its operation depends on the characteristics of the output capacitor. Since the ESR of ceramic capacitors is extremely low at several tens of mΩ or below, the phase compensation cannot be achieved and an oscillation occurs if it is used as is. Connecting an external resistor to the ceramic capacitor in series allows it to be used as a capacitor with a stable ESR.

An FRA (frequency response analyzer) is used to measure the Bode plot while varying the output resistance R_O, which corresponds to the ESR, on the evaluation circuit with BA00CC0WFP as shown in Figure 9. The phase and gain margins are read from the Bode plot and presented in Figures 10 and 11, respectively, while the output current is used as the variable. In addition, Figure 12 shows the plot of the output resistance when the phase margin is over 30° and the gain margin is over 10 dB at the same time. This plot demonstrates that stable operation is achieved using an output ceramic capacitor by setting the output resistance R_O to 1Ω.

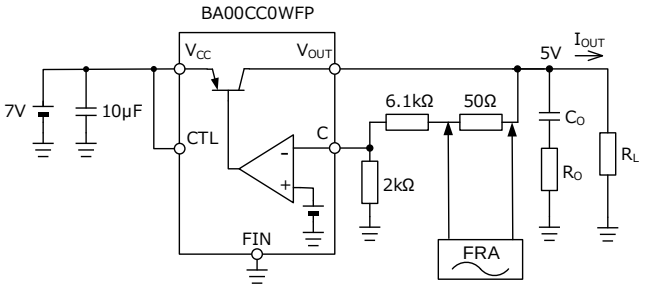

Figure 9. Evaluation circuit for stable operation

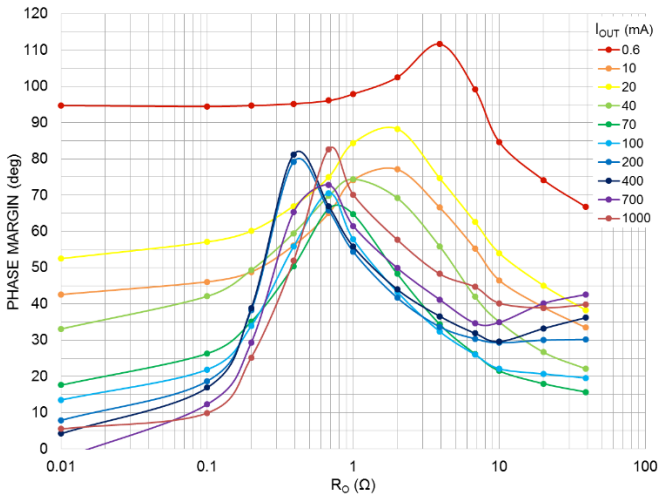

Figure 10. Phase margin vs. R_O

C_O = 22 μF (effective capacitance 19.5 μF)

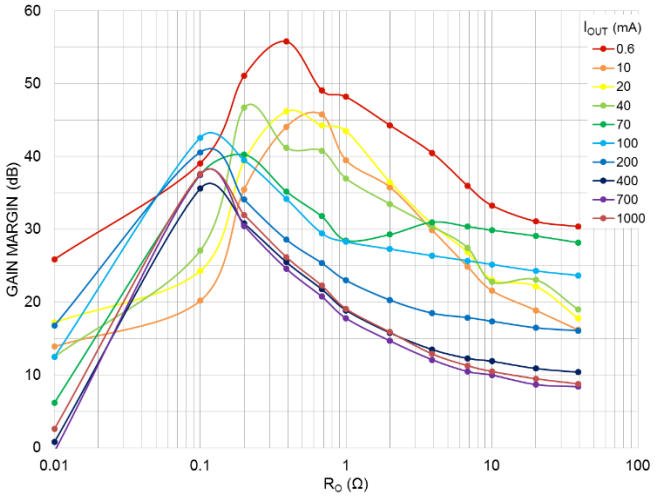

Figure 11. Gain margin vs. R_O

C_O = 22 μF (effective capacitance 19.5 μF)

Figures 13 and 14 show the same characteristics when the output capacitance is increased from 22 μF to 44 μF (22 μF × 2) and to 94 μF (47 μF × 2), respectively. The stable operation is achieved with a resistance of 1Ω in these cases as well.

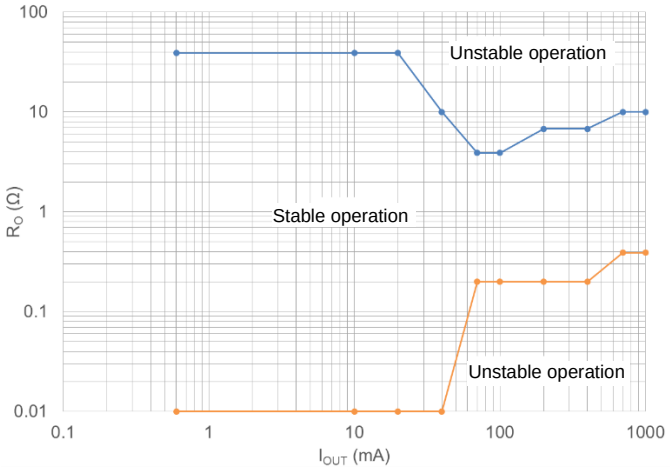

Figure 12. R_O vs I_{OUT}

C_O = 22 µF (effective capacitance 19.5 µF)

Phase margin over 30°, gain margin over 10 dB

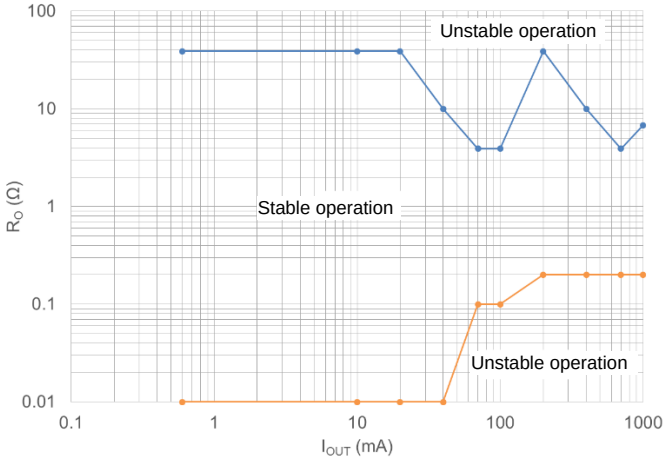

Figure 13. R_O vs I_{OUT}

C_O = 22 µF × 2 (effective capacitance of 39 µF)

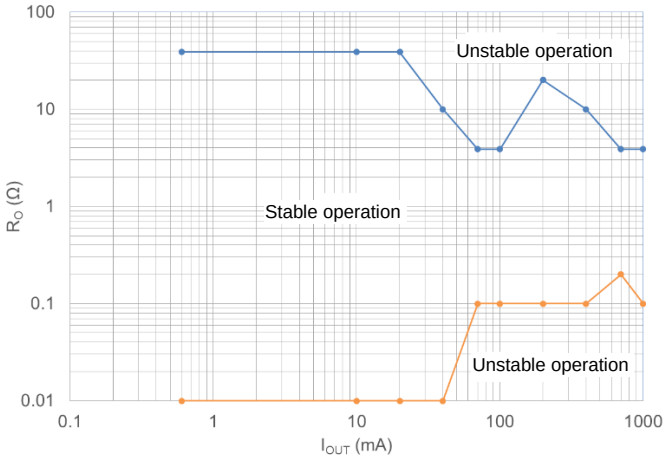

Figure 14. R_O vs I_{OUT}

C_O = 47 µF × 2 (effective capacitance of 68.1 µF)

The above evaluation for the stable operation is the result when the impedance is reduced sufficiently low by using a stabilized DC power supply for the supply side power source and the load is applied with a pure resistance. In practice, there are cases where the impedance of the supply side power source is high or the load includes an inductance component. In such cases, the operation may be unstable with the constants from this evaluation. Always check thoroughly that any unstable operation such as oscillation would not occur on the actual equipment. When the supply side impedance is high, it is useful to compensate for the high impedance by increasing the capacitance of the IC input capacitor in order to achieve the stable operation.

The circuit using an output ceramic capacitor is shown in Figure 15. A single output resistor R_O is sufficient for multiple output capacitors. When the load current is quiet without any ripples, the rated power of 0.1 W (1608 size) is sufficient for the resistor. When there is a ripple load current regularly, the rated power P_{RO} of the output resistor R_O is determined by using the average value of the ripple load current and is calculated with the following equations.

$$P = I_{RIPPLE}^2 \times R_O \quad [W]$$

P : Power loss in the resistor $[W]$

I_{RIPPLE} : Average value of the ripple load current $[A]$

R_O : Output resistance $[\Omega]$

$$P_{RO} \geq P \times 2 \quad [W]$$

Select a resistor of which the rated power P_{RO} is larger than the power loss P in the resistor by a factor of 2 or greater.

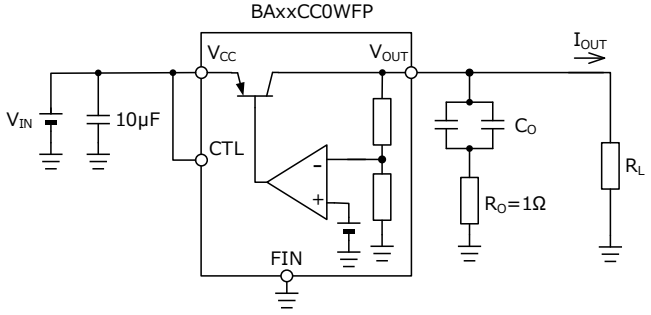

Figure 15. Circuit using an output ceramic capacitor

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) ROHM shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) ROHM has used reasonable care to ensure the accuracy of the information contained in this document. However, ROHM does not warrants that such information is error-free, and ROHM shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of ROHM.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/