Constant Current LED Driver

Thermal Resistance Data: HRP7

50 V 500 mA 1-Channel LED Source Driver for Automotive Applications
BD8374HFP-M, BD83732HFP-M, BD83733HFP-M

The BD837xx Series is an LED source driver IC with the capability of withstanding a high input voltage of 50 V. This can be used for exterior lamps such as rear lamps, turn lamps, DRL/position lamps, and fog lamps. This application note summarizes thermal resistance data used for thermal design, which is most crucial for the source driver.

IC features

- ■ AEC-Q100 Qualified
- ■ Variable-Form Constant-Current Source Driver
- ■ PWM Dimming Function
- ■ CR Timer for PWM Dimming Function Integrated
- ■ LED Open/Short Detection Circuit Function Integrated
- ■ Over-voltage Mute Function Integrated (BD8374HFP-M)
- ■ Temperature Derating Function Integrated (BD83732HFP-M / BD83733HFP-M)
- ■ Abnormal Output Detection and Output Function (PBUS)
- ■ HRP7 package

Package

Figure1. HRP7 package

Measurement environment

Description	Standards
Measurement environment	JEDEC STANDARD JESD51-2A (Still Air)
Measurement substrate standards	JEDEC STANDARD JESD51-3 JESD51-5 JESD51-7

Table1. Measurement standards

Thermal resistance data

PCB	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)
1-layer	73.5	6
2-layer	27.2	3
4-layer	20.7	2

θ_{JA}: Thermal resistance between junction T_J and ambient temperature T_A

Ψ_{JT}: Thermal characteristic parameter between junction T_J and package surface central temperature T_T

* The values of θ_{JA}, Ψ_{JT}, and Z_{TH} indicated in this application note are measured values in the JEDEC environment, and therefore, do not necessarily match with the given environment; extra care must be taken as these values are affected by PCB characteristics, PCB layout, parts arrangement, casing shape, and ambient environment

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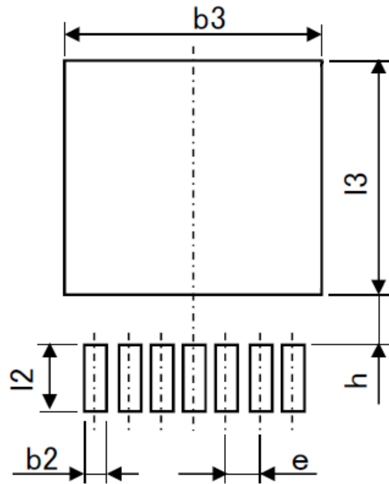
1-layer PCB specification (1s)



Unit: mm

Land pitch	Land interval	Land length		Land width	
e	h	l2	L3	b2	b3
1.27	0.94	1.37	9.00	0.93	10.00

Figure 2. Footprint dimension

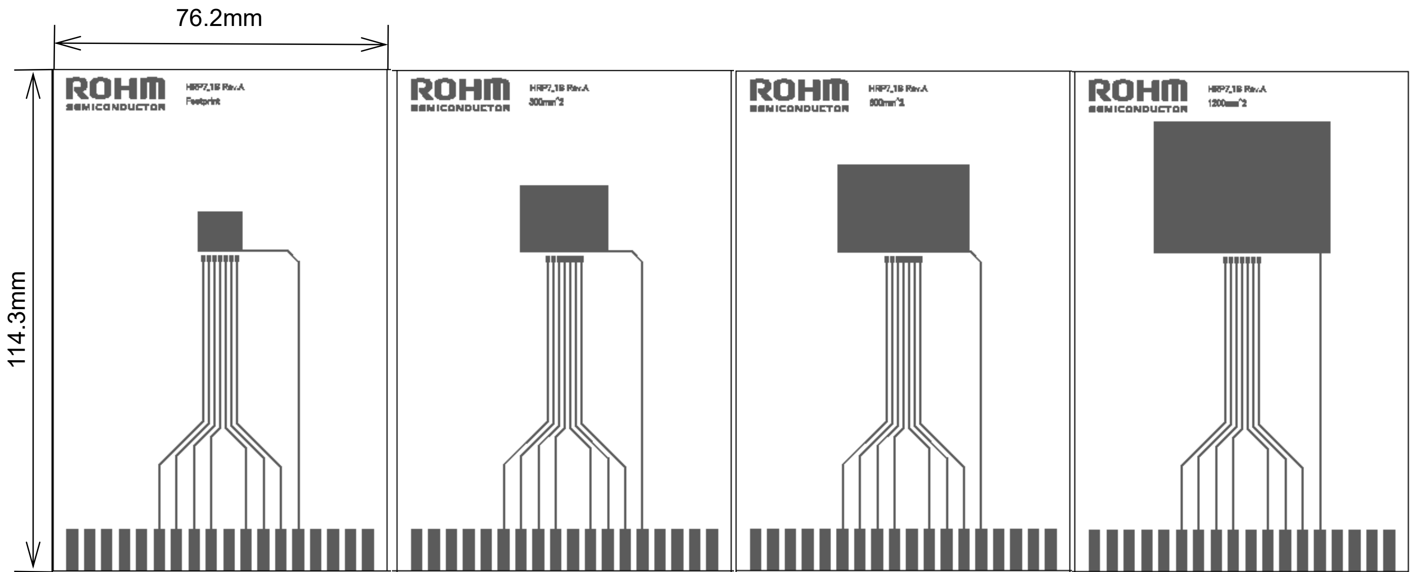


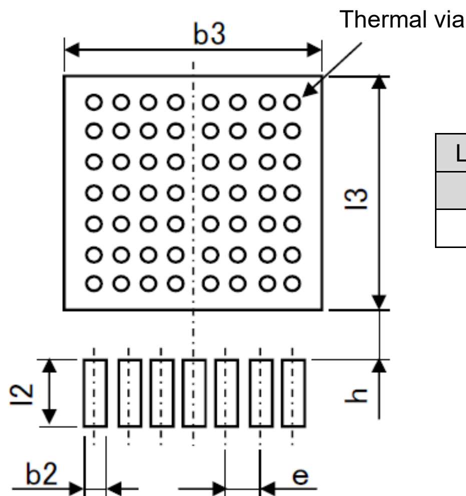
Figure 3. Footprint Figure 4. 300 mm^2 Figure 5. 600 mm^2 Figure 6. 1200 mm^2

Dimension	Value
Substrate thickness	1.57 mm
Substrate external dimension	76.2 mm × 114.3 mm
Substrate material	FR4
Copper foil thickness (surface layer)	70 µm (2 oz)
Copper foil area	Footprint, 300 mm^2, 600 mm^2, 1200 mm^2

Table 2. PCB specification

Figure 7. Substrate cross-section diagram

2-layer PCB specification



Unit: mm

Land pitch	Land interval	Land length		Land width		Thermal via	
e	h	l2	L3	b2	b3	Pitch	Diameter
1.27	0.94	1.37	9.00	0.93	10.00	1.20	φ0.30

Figure 8. Footprint dimension

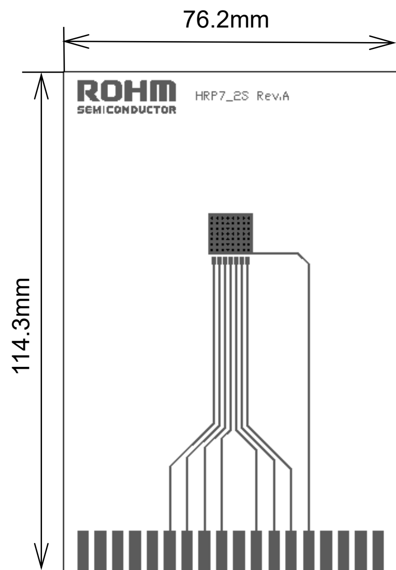


Figure 9. Surface layer

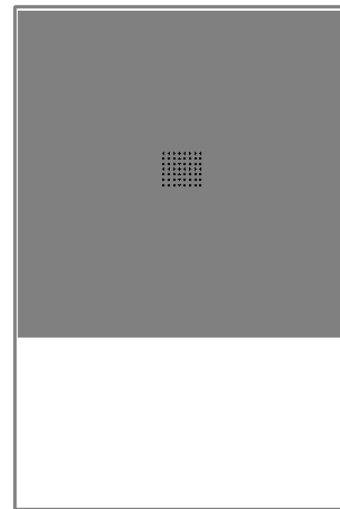


Figure 10. Back layer

Dimension	Value
Substrate thickness	1.60 mm
Substrate external dimension	76.2 mm × 114.3 mm
Substrate material	FR4
Copper foil thickness (surface layer, back layer)	70 µm (2 oz)
Copper foil area (surface layer / back layer)	Footprint / 5505mm^2 (74.2 mm × 74.2 mm)

Table 3. PCB specification

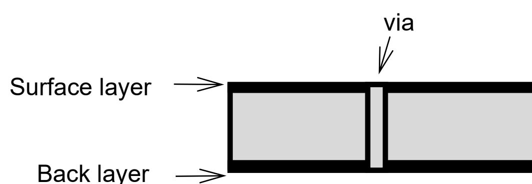
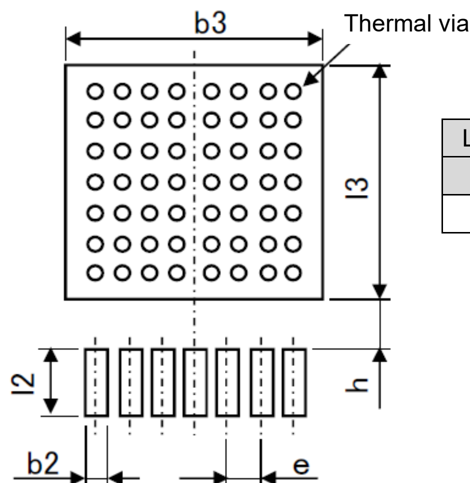


Figure 11. Substrate cross-section diagram

4-layer PCB specification (2s2p)



Unit: mm

Land pitch	Land interval	Land length		Land width		Thermal via	
e	h	l2	L3	b2	b3	Pitch	Diameter
1.27	0.94	1.37	9.00	0.93	10.00	1.20	φ0.30

Figure 12. Footprint dimension

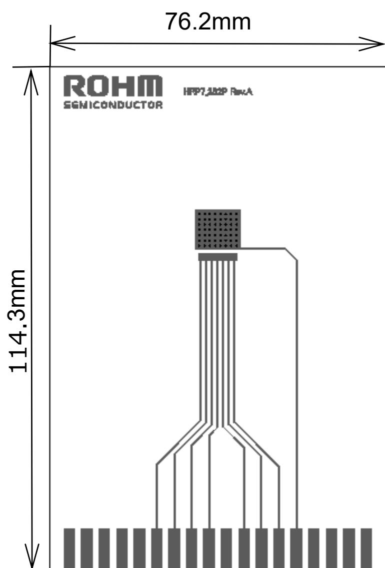


Figure 13. Surface layer

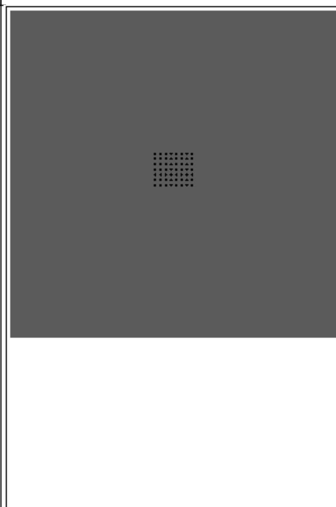


Figure 14. GND layer

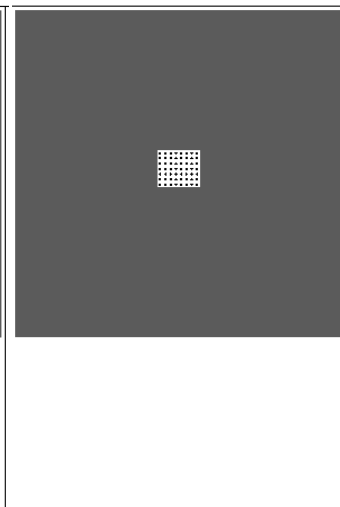


Figure 15. Power supply layer

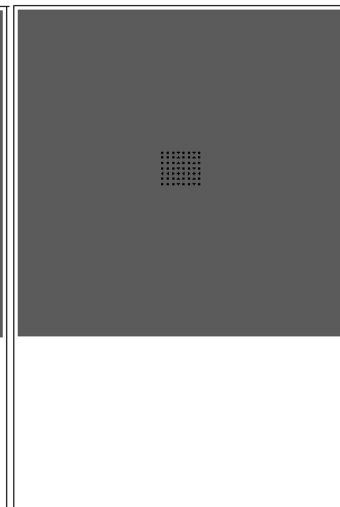


Figure 16. Back layer

Dimension	Value
Substrate thickness	1.60 mm
Substrate external dimension	76.2 mm × 114.3 mm
Substrate material	FR4
Copper foil thickness (surface layer, back layer)	70 µm (2 oz)
Copper foil thickness (GND layer, power supply layer)	35 µm (1 oz)
Copper foil area (surface layer / other)	Footprint / 5505mm² (74.2 mm × 74.2 mm)

Table 4. PCB 仕様

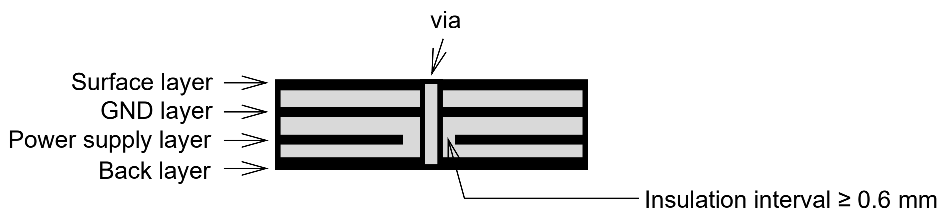


Figure 17. Substrate cross-section diagram

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1-layer Thermal resistance data

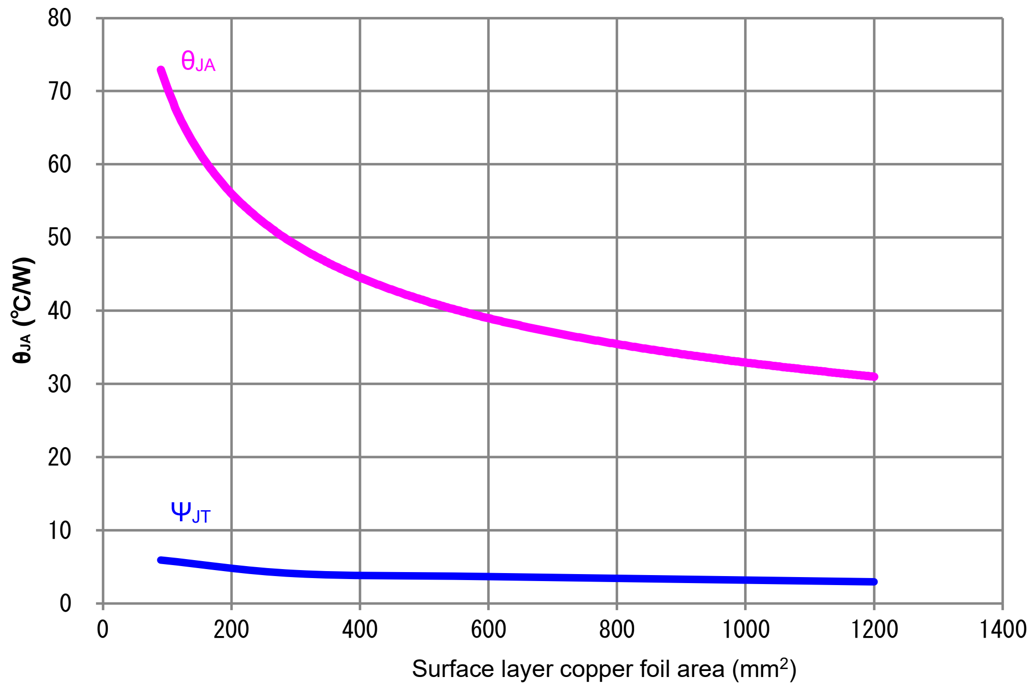
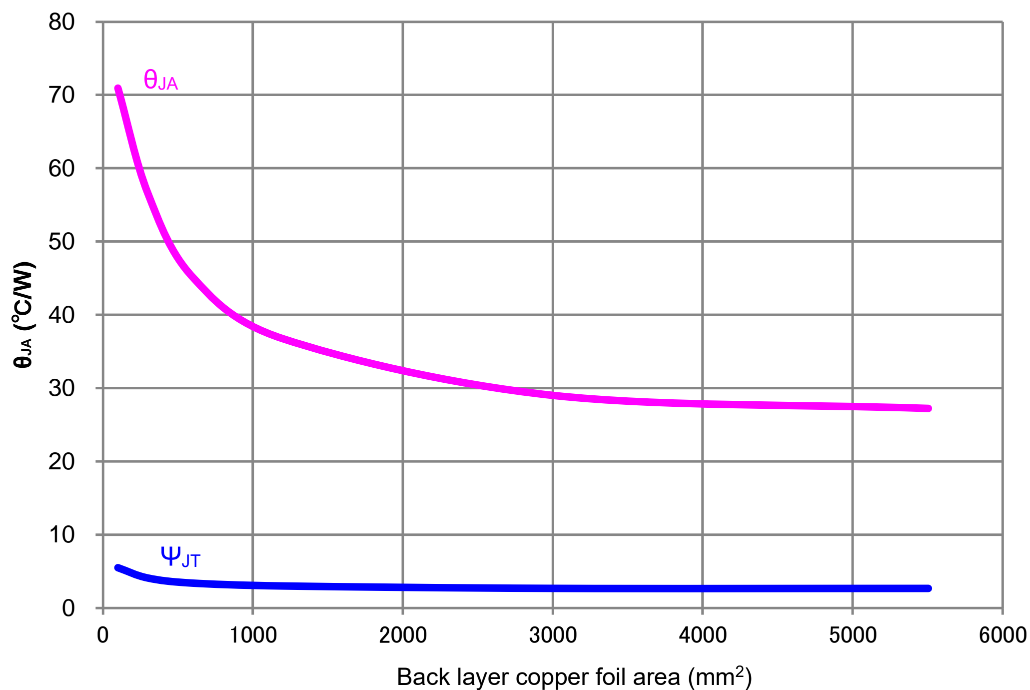


Figure 18. θ_{JA} / Ψ_{JT} vs Copper foil area (1-layer)

2-layer Thermal resistance data



* The copper foil of the back layer is used as parameter.

Figure 19. θ_{JA} / Ψ_{JT} vs Copper foil area (2-layer)

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1-layer Transient thermal resistance data

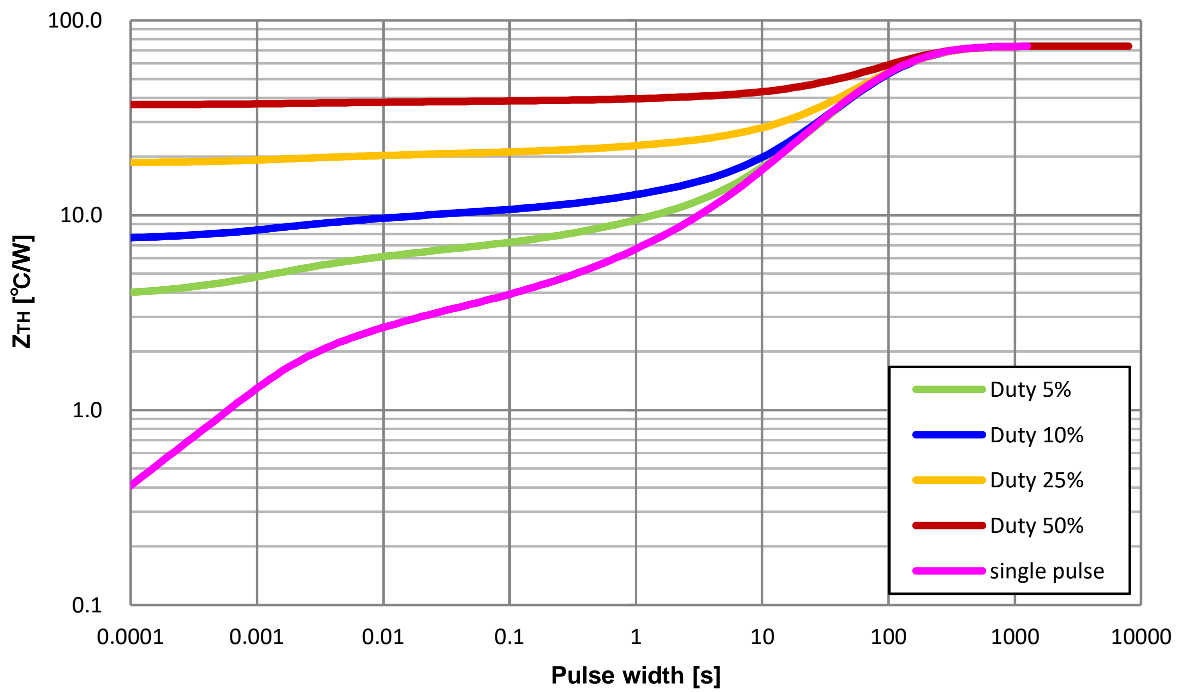

Figure 20. Transient thermal resistance footprint (1-layer)

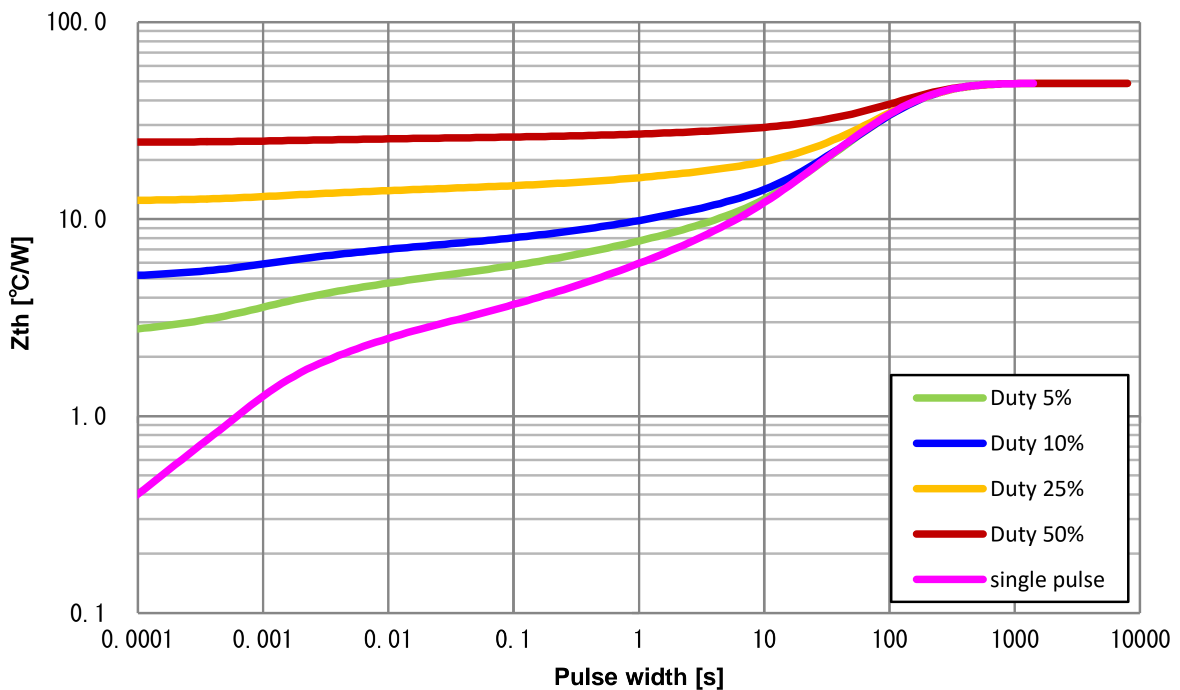

Figure 21. Transient thermal resistance 300 mm² (1-layer)

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1-layer Transient thermal resistance data (continued)

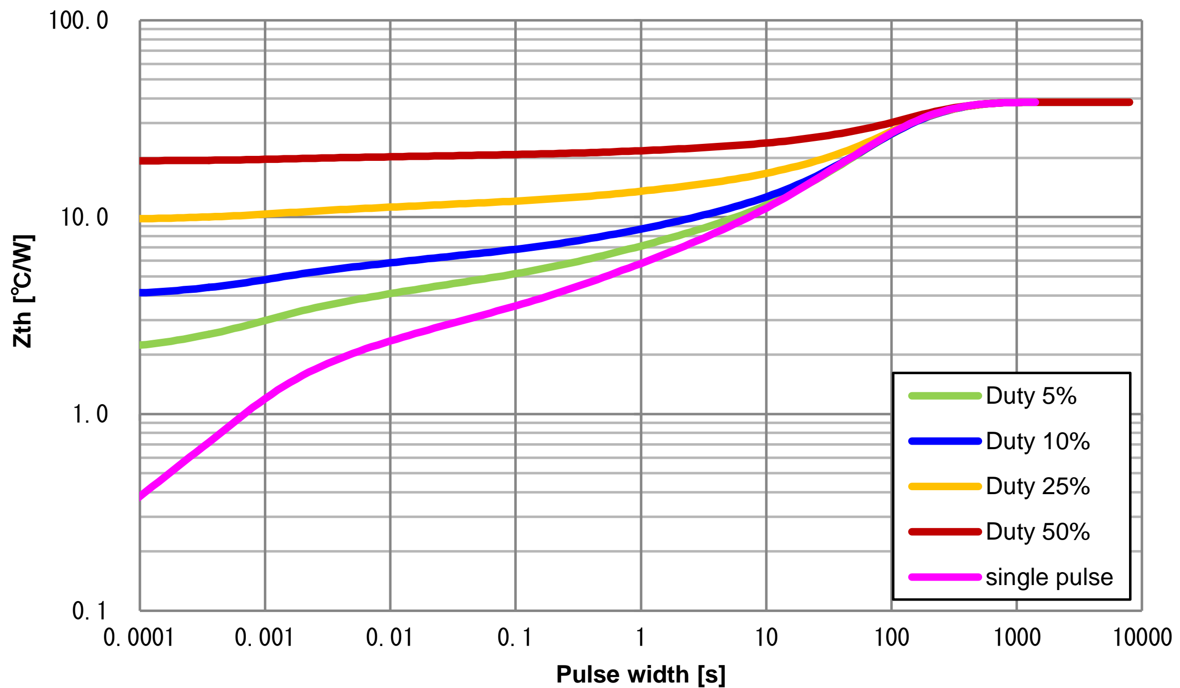

Figure 22. Transient thermal resistance 600 mm² (1-layer)

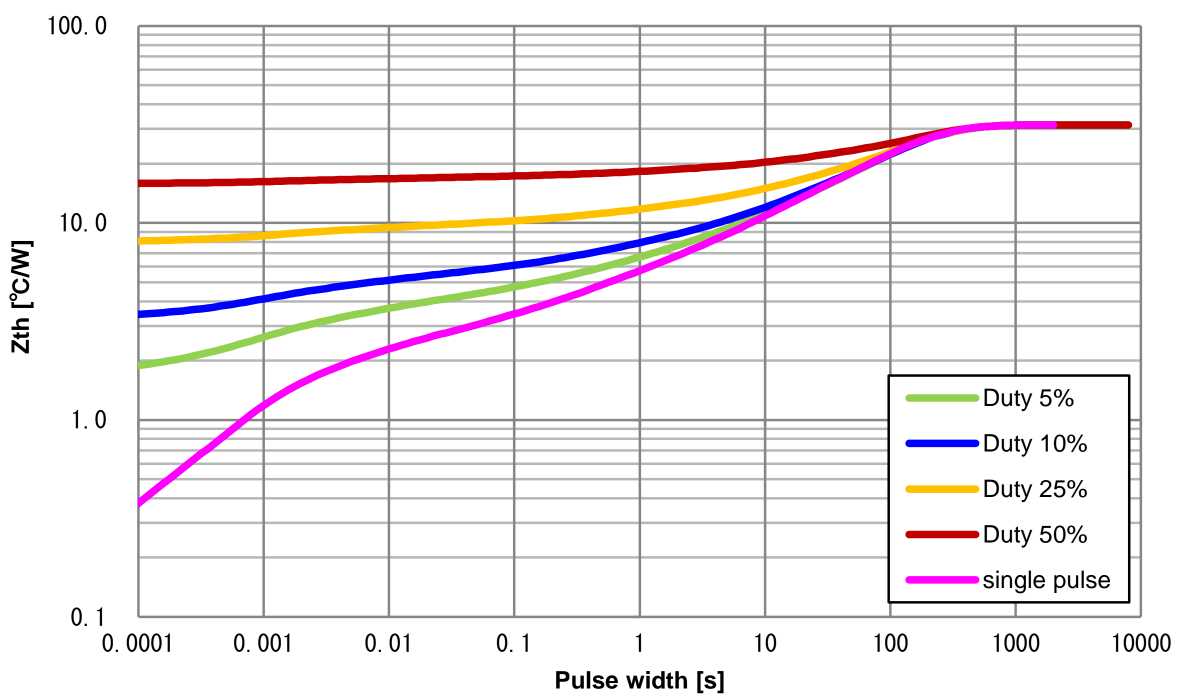

Figure 23. Transient thermal resistance 1200 mm² (1-layer)

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2-layer Transient thermal resistance data

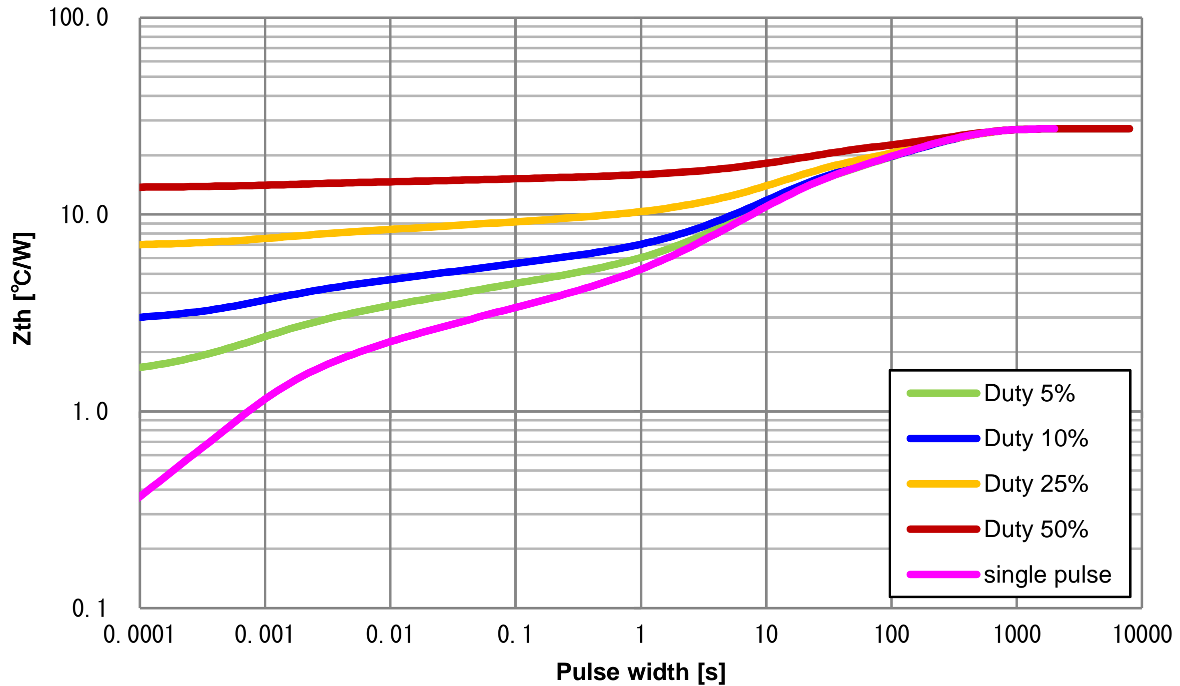

Figure 24. Transient thermal resistance (2-layer)

4-layer Transient thermal resistance data

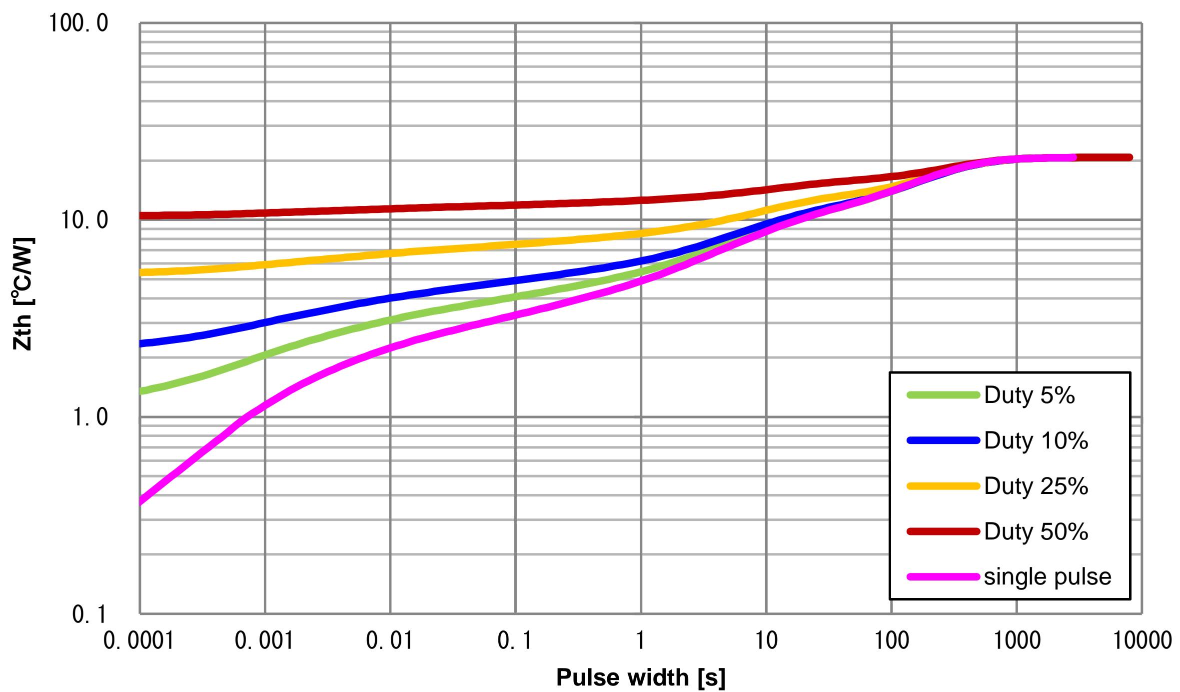

Figure 25. Transient thermal resistance (4-layer)

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Calculation example (in case of BD8374HFP-M)

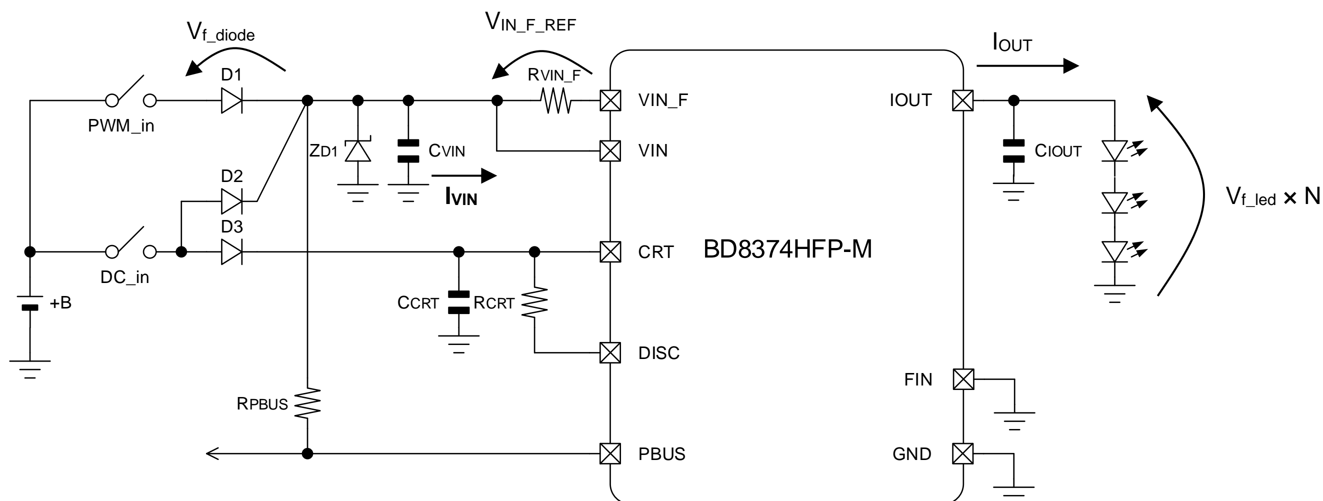


Figure 26. Application circuit diagram

1. Calculate the thermal loss. (See the data sheet for details)

The thermal loss Pc generated in the LSI can be calculated using the following formula:

$Pc = (+B - V_{f_diode} - V_{IN_F_REF} - V_{f_led} \times N) \times I_{OUT} + I_{VIN} \times (+B - V_{f_diode})$

Pc : Thermal loss

+B : Battery voltage

V_{f_diode} : Reverse connection preventing diode Vf

$V_{IN_F_REF}$: VIN_F terminal voltage (VIN − VIN_F)

V_{f_led} : LED Vf

N : LED line number

I_{OUT} : Output current

I_{VIN} : Circuit current

If +B = 13.5 V, V_{f_diode} = 1.0 V, $V_{IN_F_REF}$ = 0.18 V(typ), V_{f_led}= 2.3 V, N = 3, I_{OUT} = 200 mA, and I_{VIN} = 2.1 mA(typ), then the thermal loss Pc is calculated as follows:

$Pc = (+B - V_{f_diode} - V_{IN_F_REF} - V_{f_led} \times N) \times I_{OUT} + I_{VIN} \times (+B - V_{f_diode})$

$= (13.5V - 1.0V - 0.18V - 2.3V \times 3) \times 200mA + 2.1mA \times (13.5V - 1.0V)$

$= 1.11$ [W]

2. Calculate the junction temperature T_J from the ambient temperature T_A

The following formula can be used to estimate T_J.

$T_J = T_A + \theta_{JA} \times P_c$

θ_{JA}: Thermal resistance between T_J and T_A

Here, the specification of the substrate on which the LSI is mounted is defined as follows:

Number of layers: 1-layer

Substrate material: FR4

Copper foil area: 30 mm × 40 mm = 1200 mm^2

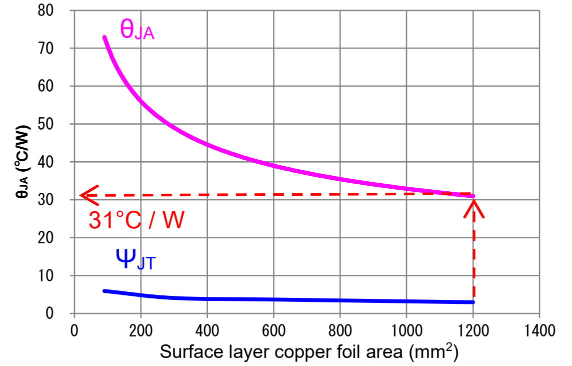


Figure 27. θ_{JA} / Ψ_{JT} vs copper foil area (1-layer)

Calculation with θ_{JA} = 31°C/W read out from “Figure 27. θ_{JA}/ Ψ_{JT} vs Copper foil area (1-layer)” and Ta = 85°C gives the following result:

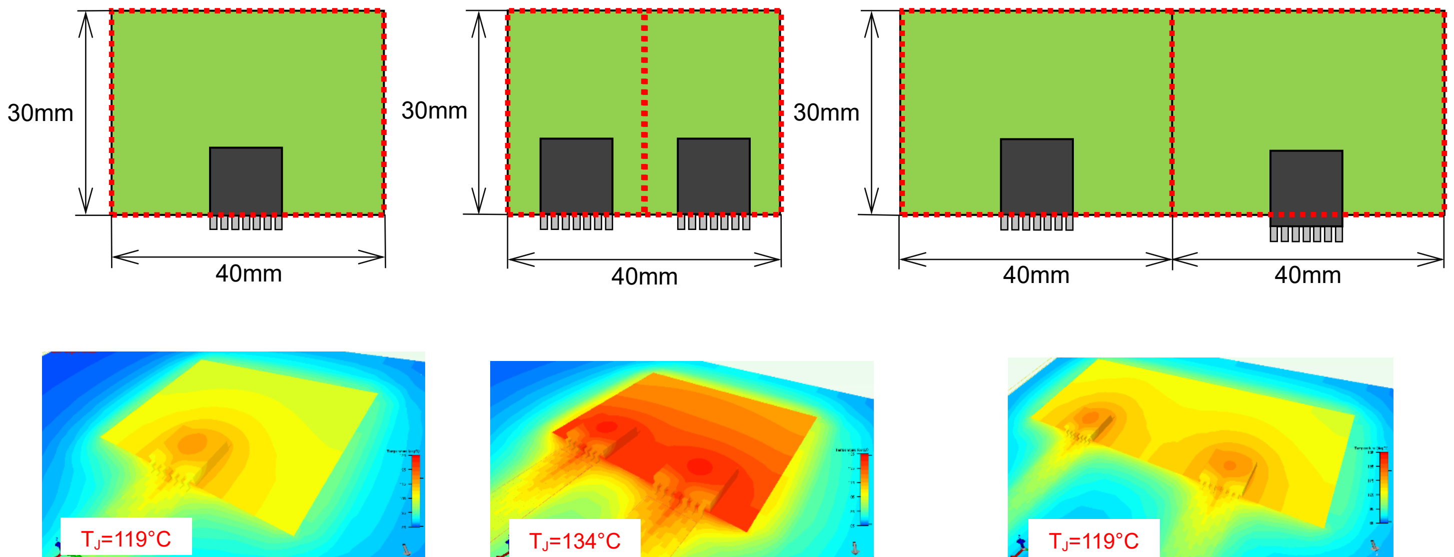
$T_J = T_A + \theta_{JA} \times Pc$

= 85 °C + 31 °C / W × 1.11W

= 119.4 [°C]

* The above calculation provides an estimated value of Tj using θ_{JA} measured in the JEDEC environment. Please use it as a rough estimate as these values are affected by PCB characteristics, PCB layout, parts arrangement, casing shape, and ambient environment.

* θ_{JA} indicated above is the value under the condition that one LSI as a thermal-generating source is mounted on the substrate. When multiple LSIs are used, care must be taken as these can interfere with each other (see Figure 28).



* The temperature monitoring point is in the center of the chip's surface.
* This is the analytical result from simulation using FloTHERM (by Mentor Graphics).

Figure 28. Effective thermal release range

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3. Calculate the junction temperature T_J from the surface temperature T_T

The following formula can be used to estimate T_J.

$T_J = T_T + \Psi_{JT} \times P_c$

T_T: Surface temperature (mold center temperature. See Figure 29)

Ψ_{JT}: Thermal characteristic parameter between T_J -and T_T

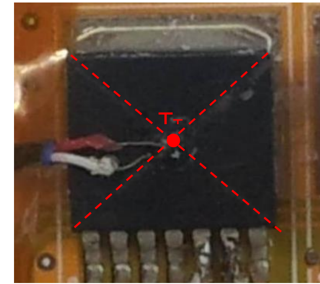

Figure 29. Reference picture of T_T measurement position

Here, the specification of the substrate on which LSI is mounted is defined as follows.

Number of layers: 2-layer
Substrate material: FR4
Copper foil area: 50 mm × 50 mm = 2500 mm^2

Calculation with Ψ_{JT} = 3°C/W read out from "Figure 30. θ_{JA}/ Ψ_{JT} vs Copper foil area (2-layer)" and T_T = 115°C measured in an actual operating state gives the following result:

$T_J = T_T + \Psi_{JT} \times Pc$
= 115°C + 3°C / W × 1.11W
= 118.3 [°C]

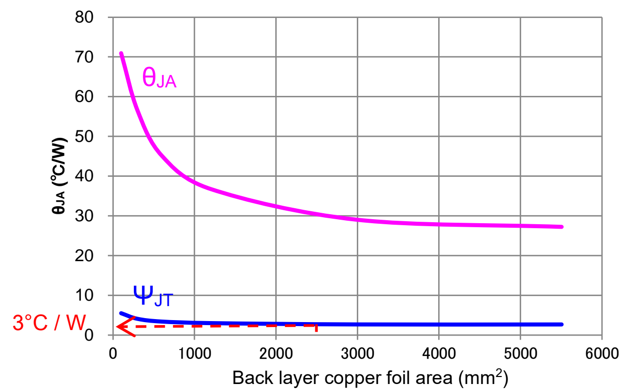

Figure 30. θ_{JA}/ Ψ_{JT} vs. copper foil area (2-layer)

* In the above calculation, the thermal loss Pc calculated in Step 1 is used. However, the use of an actual measurement value can provide a more accurate estimated value of T_J.

* The above calculation provides an estimated value of T_J using Ψ_{JT} measured in the JEDEC environment. Please use it as a rough estimate as these values are affected by PCB characteristics, PCB layout, parts arrangement, casing shape, and ambient environment.

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4. Calculate the junction temperature T_J from the transient thermal resistance data

In a case where thermal loss increases transiently (such as due to transient variations in input voltage), the transient thermal resistance should be used for calculation. One of such examples is shown below.

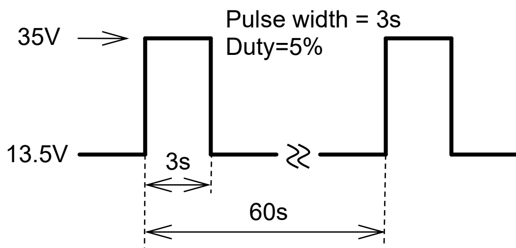

Figure 31. Example of +B voltage waveform

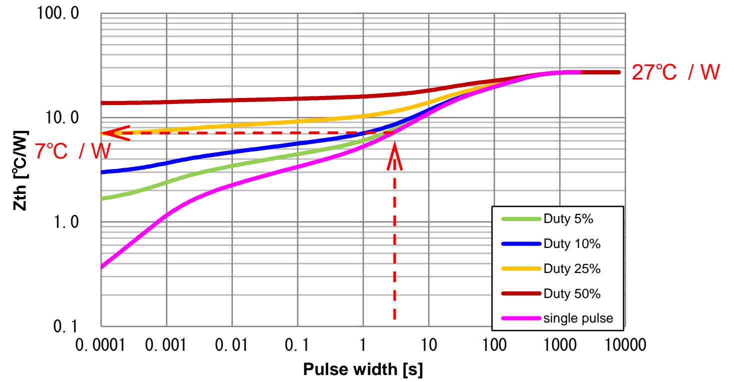

Figure 32. Transient thermal resistance (2-layer)

As shown in Figure 31, when repeated application of +B voltage occurs transiently, adding up the temperature rises at constant voltage (+B = 13.5 V) and at transient voltage (+B = 35 V) can compute the total value of ΔT_J.

If V_{f_diode}= 1.0 V, $V_{IN_F_REF}$ = 0.18 V(TYP), V_{f_led} = 2.3V, N = 3, I_{OUT} = 200 mA, I_{VIN} = 2.1 mA(TYP), then the thermal loss P_C is calculated as follows:

At constant voltage (+B = 13.5V)

$$P_{C1} = (+B - V_{f_diode} - V_{IN_F_REF} - V_{f_led} \times N) \times I_{OUT} + I_{VIN} \times (+B - V_{f_diode})$$
$$= (13.5V - 1.0V - 0.18V - 2.3V \times 3) \times 200mA + 2.1mA \times (13.5V - 1.0V)$$
$$= 1.11\ [W]$$

At transient voltage (+B = 35V)

$$P_{C2} = (+B - V_{f_diode} - V_{IN_F_REF} - V_{f_led} \times N) \times I_{OUT} + I_{VIN} \times (+B - V_{f_diode})$$
$$= (35V - 1.0V - 0.18V - 2.3V \times 3) \times 200mA + 2.1mA \times (35V - 1.0V)$$
$$= 5.46\ [W]$$

In 2-layer substrate implementation, each temperature rise is calculated as follows:

At constant voltage (+B = 13.5V)

$$\Delta T = \theta_{JA} \times P_{C1}$$
$$= 27\ °C/W \times 1.11W$$
$$= 30.0\ [°C]$$

θ_{JA}: Thermal resistance between T_J and T_A

At transient voltage (+B = 35V)

$$\Delta T = Z_{TH}(3s) \times (P_{C2} - P_{C1})$$
$$= 7\ °C/W \times (5.46W - 1.11W)$$
$$= 30.5\ [°C]$$

Z_{TH} (3s): Transient thermal resistance with pulse width 3 s, duty 5%

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The total temperature rise ΔT_J is as follows:

$$\Delta T_J = 30.0\ °C + 30.5\ °C = 60.5\ °C$$

When the ambient temperature Ta during application of transient voltage is 65 °C, the following formula is established:

$$T_J = T_A + \Delta T_J = 65\ °C + 60.5\ °C = 125.5\ °C$$

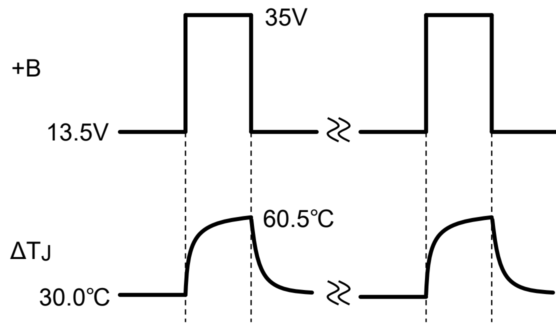

Figure 33. Image of temperature rise

* The above calculation provides an estimated value of T_J using Z_{TH} measured in the JEDEC environment. Please use it as a rough estimate as these values are affected by PCB characteristics, PCB layout, parts arrangement, casing shape and ambient environment.

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