Charge protection ICs with Buit-in FET

Negative Voltage Protection type

BD6046GUL

Pb Free ROHM Electronic Components RoHS Directive Compliance

●Descriptions

BD6046GUL protects the devices from the abnormal input voltage at the USB port.
Addition to the conventinal charge protection IC, it prevents the negative voltage happened by the USB reverse insertion without any additional compornents.
ROHM's original charge protection IC series enables to protect the abnormal input voltage from -30V to +30V.

●Features

1) Overvoltage Protection up to 28V
2) Negative Voltage Protection
3) Internal Low Ron (250mΩ) FET
4) Over voltage Lockout (OVLO)
5) Under voltage Lockout(UVLO)
6) Internal 2.5msec Startup Delay
7) Over Current Protect
8) Thermal Shut Down
9) Small package: VCSP50L2(2.5mm x 2.5mm, height=0.55mm)

●Applications

Mobile phones, MP3 players, Digital Still Camera, PDA, IC recorder, Electronic Dictionary, Handheld Game, Game Controller, Camcorder, Bluetooth Headsets, etc

Status of this document.
The Japanese version of this document is the formal specification.
A customer may use this translation version only for reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intended to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

Sep. 2008

●Absolute maximum ratings (Ta=25℃)

Contents	Symbol	Rating	Unit	Conditions
Input supply voltage 1	Vmax1	-30～30	V	IN
Input supply voltage 2	Vmax2	-0.3～7	V	other
Power dissipation	Pd	975	mW	
Operating temperature range	Topr	-40～+85	℃	
Storage temperature range	Tstr	-55～+150	℃	

※1 When using more than at Ta=25℃, it is reduced 7.8mW per 1℃.
ROHM specification board 50mm× 58mm mounting.

●Recommended operating range (Ta=-40～+85℃)

Parameter	Symbol	Range	Unit	Usage
Input voltage range	V_{in}	2.2～28	V	

※ This product is not especially designed to be protected from radioactivity.

- **Typical Application Circuit**

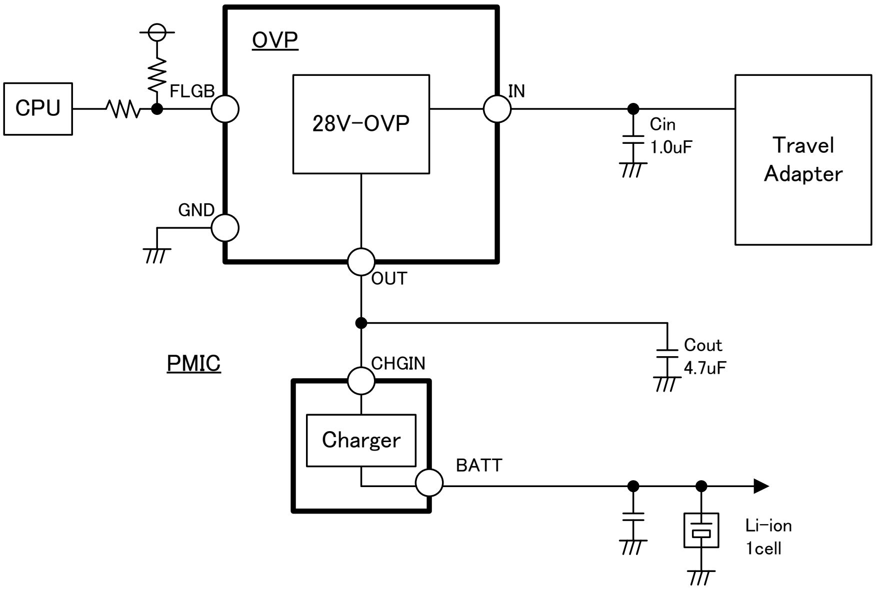


Figure1. Application Circuit

・Safety is high because it detects, and it protects it for an abnormal voltage up to 28V.
・It contributes to the miniaturization because all external is built into.

- **Ball Configuration**

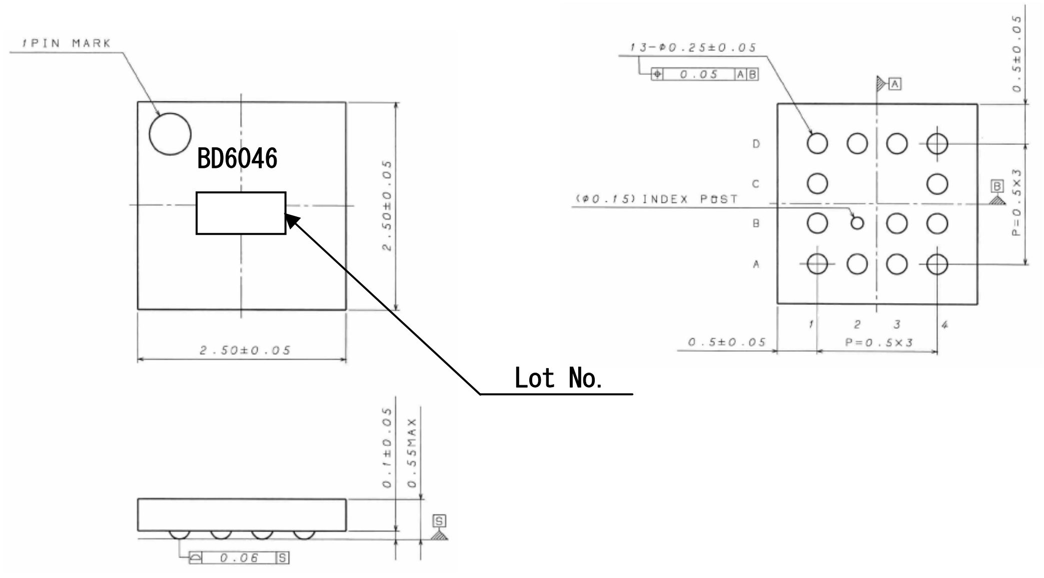
Top View

A	OUT	FLGB	IN	IN
B	OUT	index	IN	IN
C	OUT			IN
D	OUT	GND	IN	IN
	1	2	3	4

Bottom View

D	OUT	GND	IN	IN
C	OUT			IN
B	OUT	index	IN	IN
A	OUT	FLGB	IN	IN
	1	2	3	4

● Package Dimensions (VCSP50L2)



● PIN DESCRIPTIONS

PIN	NAME	FUNCTION
A3, A4, B3, B4, C4, D3, D4	IN	Input voltage Pin. A 1□F low ESR capacitor, or larger must be connected between this pin and GND
A1, B1, C1, D1	OUT	Output Voltage Pin
A2	FLGB	Open-drain output pin that turns low when any protection event occurs. (overvoltage protection, thermal shut down)
D2	GND	Ground Pin

● Electrical Characteristics

(Unless otherwise noted, Ta = 25°C, IN=5V)

Parameter	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
● ELECTRICAL						
Input Voltage Range	VIN	-	-	28	V	
Supply Quiescent Current	ICC		35	70	μA	
Under Voltage Lockout	UVLO	3.42	3.6	3.78	V	IN=decreasing
Under Voltage Lockout Hysteresis	UVLOh	50	100	150	mV	IN=increasing
Over Voltage Lockout	OVLO	6.5	6.7	6.9	V	IN=increasing
Over Voltage Lockout Hysteresis	OVLOh	50	100	150	mV	IN=decreasing
Current limit	ILM	1.2	-	-	A	
Vin vs. Vout Res.	RON	-	250	300	mΩ	
FLGB Output Low Voltage	FLGBVO	-	-	400	mV	SINK=1mA
FLGB Leakage Current	FLGBleak	-	-	1	μA	
● TIMINGS (FLGB pull up resistance 100kΩ)						
Start Up Delay	Ton	-	2.5	5	msec	
Output Turn Off Time	Toff	-	2	10	μsec	
Alert Delay	Tovp	-	1.5	10	μsec	

* This product is not especially designed to be protected from radioactivity.

- **Timing Diagram**

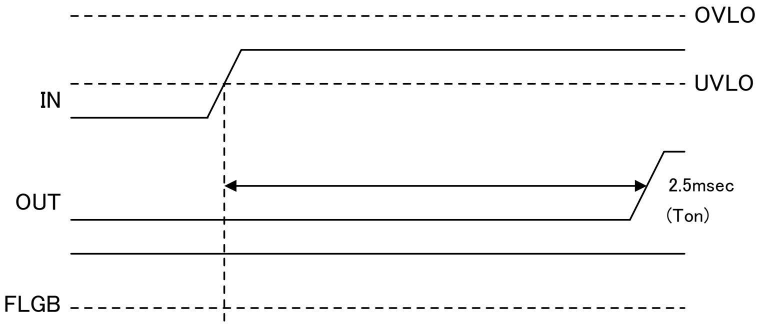


Figure2. Start up sequence

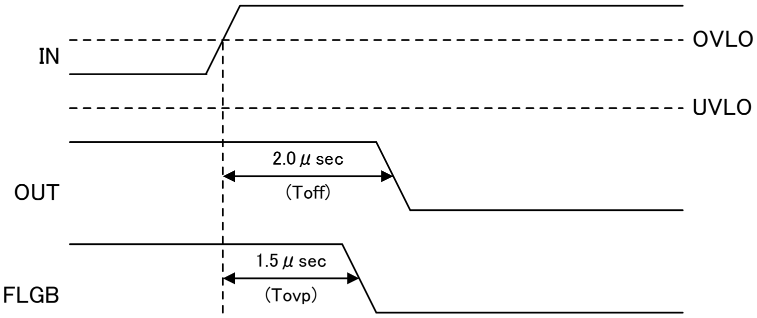


Figure3. Shutdown by over voltage detection

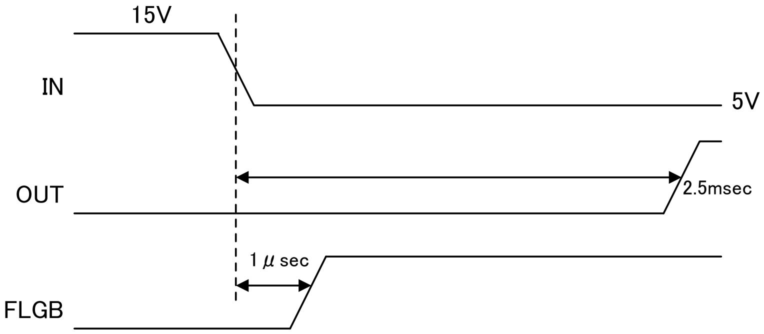


Figure4. Recovery from overvoltage protection

● Block Diagram

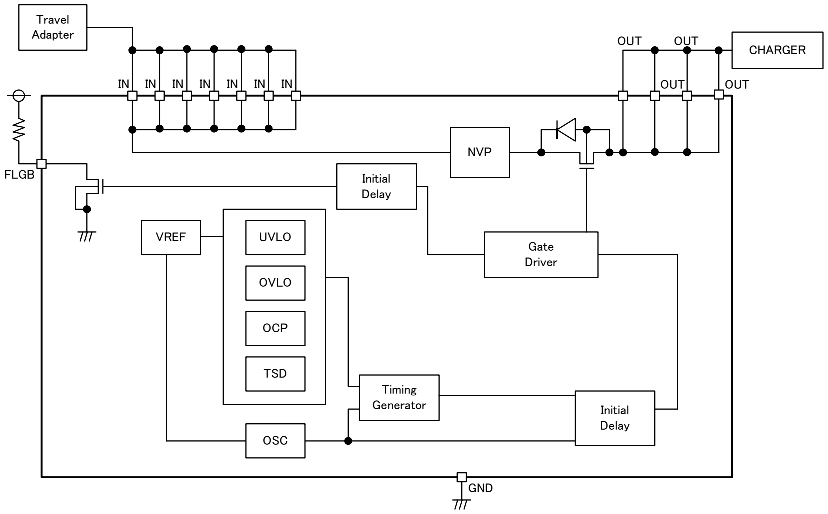


Figure5. Block Diagram

● PIN number/PIN name

Pin number	Pin name
A3, A4, B3, B4, C4, D3, D4	IN
A1, B1, C1, D1	OUT
D2	GND
A2	FLGB

●Use-related Cautions

(1) Absolute maximum ratings
If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range
This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector
There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines
In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage
Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation
When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields
Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board
When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins
Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(10) Ground wiring pattern
When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors
When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)
When the junction temperature reaches the defined value, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

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Published by
KTC LSI Development Headquarters
LSI Business Pomotion Group

Catalog No.08Y280A '08.9 ROHM ©