

## SiC MOSFET

# 800 V Three-Phase Output LLC DC/DC Resonant Converter

In this application note, we will introduce a 5 kW LLC resonance-type DC/DC converter with three-phase output. The converter employs silicon carbide (SiC) MOSFETs for the switching elements and uses isolated transformers. Since the SiC MOSFETs have a breakdown voltage characteristic of 1,200 V, the input voltage can be increased up to 800 V. Employing switching frequencies of the transistors of approximately 200 kHz and 160 kHz for an input voltage of 600 V and 800 V, respectively, enables the isolated transformers and the input and output capacitors to be significantly downsized. However, their conduction loss in on-resistance  $R_{DS(on)}$  is not sufficiently small, unlike that of silicon (Si) MOSFETs. To improve this conduction loss, the currents in the individual phases are reduced by employing the three-phase circuit topology. As a result, an output power as high as 5 kW is achieved. Furthermore, an additional technology is implemented to minimize the capacitance of the input and output capacitors. Employing transformers with a current balancing function among the three phases effectively reduced the differences between the maximum peak currents generated in the individual phases. In this application note, we will introduce an example of these novel LLC converters that achieved a conversion efficiency of 97.6% at 5 kW by using these technologies.

These novel inverter circuits have been developed jointly with Power Assist Technology Ltd. (<https://www.power-assist-tech.co.jp/>) [29].

## Features of LLC resonant converters and three-phase output circuit topology

An LLC resonant DC/DC converter (hereafter referred to as an “LLC dc/dc”) is an attractive candidate as a circuit design for utilizing the zero-voltage switching (hereafter referred to as “ZVS”) and pulse width modulation (hereafter referred to as “PWM”) technologies to avoid the switching-loss problem unique to switching power supplies [1]-[7]. An LLC dc/dc equipped with the ZVS utilizes a spontaneous resonance produced by the series connection of an inductor and a capacitor (LC resonance). The current generated by this resonance takes the form of a pseudo sine wave, preventing unexpected voltage spikes. In other words, since an LLC dc/dc equipped with the ZVS and the zero-current-switching (ZCS) requires no additional circuit, it can simplify the circuit design and solve problems, including the voltage spikes due to the reverse recovery current in the rectifier diode for the ZVS PWM converters [8].

However, the spontaneous current resonance limits the operation range of switching devices. The transistors of the LLC dc/dc can generate a high resonance frequency by switching at a high frequency and extend the applicable range of the output voltage [9]. This enables the passive components to be further downsized. Therefore, high frequency switching devices, including SiC MOSFETs, GaN devices, and Si MOSFETs, can be considered suitable for the LLC dc/dc [10].

In addition, a high performance LLC dc/dc should achieve a power conversion efficiency as high as possible. A power conversion at a low voltage and a large current generally reduces the conversion efficiency because of Joule heat loss. Accordingly, the Joule heat loss is reduced by parallelizing the output circuit and employing a high input voltage to disperse a large current. The three-phase output circuit topology employed here can reduce the current in the single-phase circuit to 1/3 of the total current. Therefore, although the current ripple in the input and output can be absorbed with capacitors, an LC filter is required to reduce the current ripple in the ZVS PWM [11].

Meanwhile, the Si MOSFETs or GaN devices are not suitable for the switching devices when the input voltage is high. This is because the allowable voltage range is lower compared with IGBTs, although the switching characteristics are superior. The breakdown voltage (VB) of mass-produced Si MOSFETs and GaN devices is generally less than 650 V. When the BV of these devices exceeds 650 V, their  $R_{DS(on)}$  usually exceeds several hundred milliohms [12]-[13]. Furthermore, for the safe operation of the power supply system, the allowable voltage range of the power supply must cover the input voltage. Therefore, if the input voltage exceeds 600 V, it does not satisfy the general allowable voltage range of the Si MOSFETs or GaN devices. Accordingly, it is necessary to select a multi-level converter in order to enable a high input voltage with these devices. However, since many switching devices are required, the control system is complicated and the production cost is drastically increased [14]-[18].

In contrast, the SiC MOSFETs can satisfy the requirements of the fast switching speed and the high BV [19] simultaneously. These advantageous device characteristics of the SiC MOSFETs allow application of the high input voltage achieved with the high switching speed and the high BV. As a result, since a smaller power transformer can be used, an LLC dc/dc with a high power conversion efficiency can be effectively downsized.

This application note explains the advantages of configuring a three-phase output circuit LLC dc/dc equipped with isolated transformers (Figure 1) and employing SiC MOSFETs with the BV of 1,200 V. Isolated transformers generally make up a large volume of the power supply and with a maximum switching frequency exceeding 200 kHz, they can be significantly downsized. The high BV allows an input voltage as high as 600 V to 800 V. The three-phase output circuit configuration reduces the maximum current in the circuit, enabling improvement in the power conversion efficiency. Furthermore, a technology to balance these three-phase circuit currents is added to the transformers, reducing the maximum peak current in the circuit. As a result, the input and output capacitors are downsized. In the following chapters, we explain the circuit operation in detail and introduce the verification result of the actual equipment.



Figure 1. A view of the 5-kW LLC dc/dc using SiC MOSFETs.

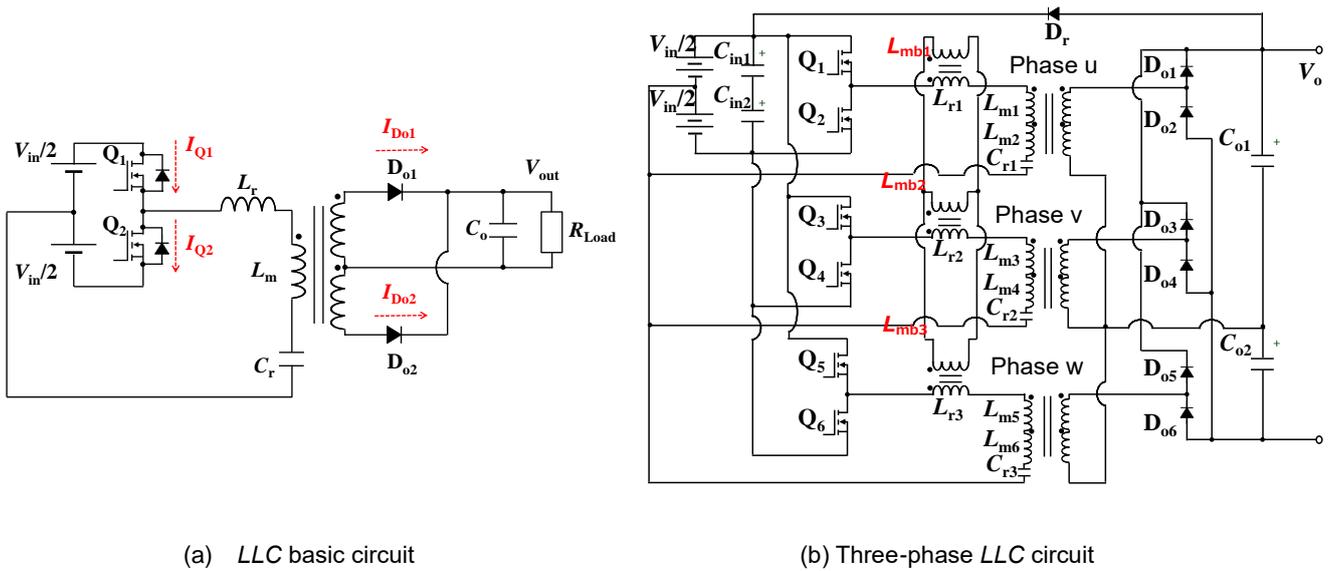


Figure 2. Circuit diagram of LLC dc/dc converter

## Operation principle and circuit configuration

Figure 2 (a) shows the basic circuit of the LLC dc/dc. The LLC circuit is basically configured with a half bridge having two switches,  $Q_1$  and  $Q_2$ . These switches are connected with resonance inductance  $L_r$ , magnetizing inductance of the isolated transformer  $L_m$ , and resonance capacitor  $C_r$  in series. The diagram shows the interleaved type circuit configuration composed of these passive components as a resonance tank.

$Q_1$  and  $Q_2$  are alternately switching with a duty cycle of approximately 50%. Dead time for the period while both  $Q_1$  and  $Q_2$  are turned OFF is provided to avoid short circuiting between  $Q_1$  and  $Q_2$ . The soft switching operation is performed during this dead time period.

Figure 3 shows the voltage and current waveforms in  $Q_1$  and  $Q_2$  of the LLC dc/dc. The figure shows gate-source voltage  $V_{gk}$ , drain-source voltage  $V_{Qk}$ , and drain current  $I_{Qk}$  on  $Q_k$ , as well as forward current  $I_{Dok}$  of secondary side diode  $D_{ok}$  ( $k = 1, 2$ ).

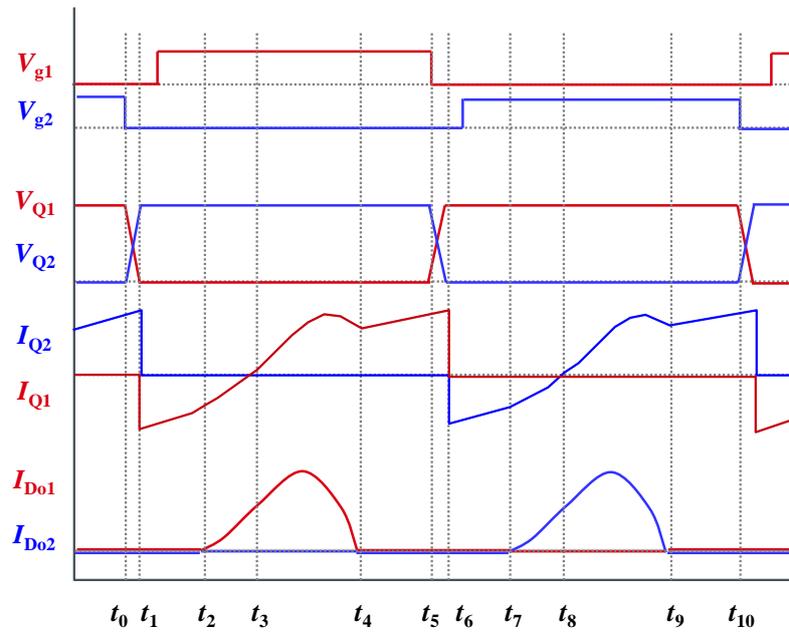


Figure 3. Voltage and current waveforms in  $Q_1$  and  $Q_2$

The operation method of the circuit is explained below.

Term 1 ( $t_0 - t_1$ ): This period starts when  $Q_2$  is turned OFF.  $V_{Q2}$  is increased with the resonance of  $(L_m + L_r)$  and  $C_r$ . The period continues until  $V_{Q1}$  reaches 0.

Term 2 ( $t_1 - t_2$ ): This period starts when  $V_{Q1}$  reaches 0. The reverse current starts flowing to body diode  $D_{o1}$  of  $Q_1$ . The ZVS is achieved with  $Q_1$  being turned ON while this reverse current is flowing. The resonance of  $(L_m + L_r)$  and  $C_r$  generates voltage on  $L_m$  in such a manner that the voltage is applied to  $D_{o1}$  in the forward direction.

Term 3 ( $t_2 - t_3$ ):  $I_{D_{o1}}$  starts flowing resonantly between  $L_r$  and  $C_r$ . This resonance increases  $I_{D_{o1}}$  and supplies the power.

Term 4 ( $t_3 - t_4$ ): This period starts when the value of  $I_{Q1}$  changes from negative to positive. During this period,  $I_{D_{o1}}$  spontaneously decreases due to the  $L_r$ - $C_r$  resonance. The period continues until  $I_{D_{o1}}$  reaches 0.

Term 5 ( $t_4 - t_5$ ): During this period, the resonance continues between  $(L_m + L_r)$  and  $C_r$ . The period continues until  $Q_1$  is turned OFF.

Term 6 ( $t_6 - t_{10}$ ):  $Q_1$  and  $Q_2$  switch their roles in the circuit and Terms 1 to 5 are repeated.

To improve the efficiency, the three-phase LLC configuration is employed as shown in Figure 2 (b). The phases are switching with a phase difference of 120 degrees [20]-[22]. In this three-phase LLC dc/dc,  $Q_j$ ,  $D_{oj}$ , and  $L_{mj}$  ( $j = 1$  to 6) as well as  $L_{ri}$  and  $C_{ri}$  ( $i = 1$  to 3) are operated in the same way as in Figure 2 (a).

It is practically impossible to manufacture transformers with exactly identical characteristics. Therefore, unbalanced transformers generate unbalanced currents in the individual phases, resulting in a larger current ripple in the output capacitor. Mitigation measures for this problem of unbalance are shown in [21] and [22] for example, but they require additional components. To avoid such additional components,  $L_{mbi}$  is placed adjacent to the transformers connected in parallel as shown in Figure 3 (b). These additional transformers are hereafter referred to as the current balance transformers, which equalize the currents in the individual phases and contribute to the downsizing of input and output capacitors  $C_{ink}$  and  $C_{ok}$ . In addition, the reduction in the peak current provides a method to avoid deterioration in the reliability of the output capacitor [23].

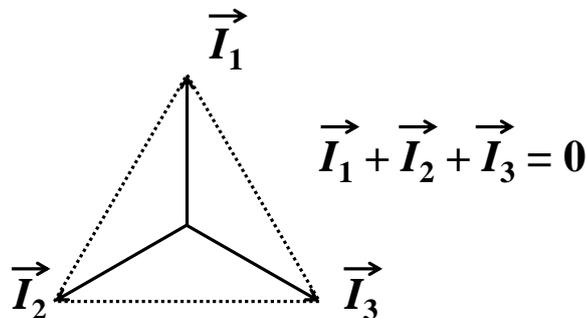


Figure 4. Three-phase current balance topology

The phase shift of 120 degrees between the phases means that the total current is always zero as shown in Figure 4. As a result,  $L_{mbi}$  generates no effective magnetic flux. Therefore,  $L_{mbi}$  has no effect on how  $L_{mj}$ ,  $L_{ri}$ , and  $C_{ri}$  resonate.

Diode  $D_r$  shown in Figure 3 returns the output power to the input side, and the input power supply provides only the power corresponding to the power loss in the system. This allows an accurate measurement of the power conversion efficiency [24].

In this design example, since output voltage  $V_o$  and input voltage  $V_{in}$  are approximately the same, the gain defined as  $V_o/V_{in}$  is approximately 1. If the gain = 1, according to the gain equation for the LLC dc/dc considering the secondary leakage inductance and the resistance component, the expected output power can be obtained by adjusting the switching frequency ( $f_{sw}$ ). Therefore,  $f_{sw}$  of  $Q_j$  is adjusted to set the output voltage.

## Design of transformers

To design the transformers as small as possible, it is necessary to pay attention to the following.

- Operate the transformers below the saturated magnetic flux density
- To reduce core loss  $P_{core}$  as much as possible, keep the maximum magnetic flux density during operation as low as possible
- To downsize the power supply unit, keep primary side winding number  $N_p$ , secondary side winding number  $N_s$ , and effective core area  $A_e$  small

Since the magnetic flux density during operation is directly related to core loss  $P_{core}$ , it must be decreased to design suitable transformers. Maximum magnetic flux density  $B_m$  with the duty of 50% is generally expressed with Equation (1) [25].

$$B_m = \frac{V_{in}}{8f_{sw}N_pA_e} \quad (1)$$

Equation (1) indicates that at least one of  $f_{sw}$ ,  $N_p$ , or  $A_e$  must be increased to decrease  $B_m$  under constant  $V_{in}$ . However, since increasing  $N_p$  or  $A_e$  leads to increase in the transformer size, increasing  $N_p$  or  $A_e$  is not an appropriate option to downsize the power supply. In contrast, increasing  $f_{sw}$  can decrease  $B_m$  without increasing the transformer size, and the SiC MOSFETs can satisfy this requirement.

Here,  $f_{sw}$  is set to approximately 200 kHz and 160 kHz at 600 V and 800 V, respectively, which could not be realized with the Si IGBTs. Furthermore, power ferrite PC40 (manufactured by TDK) [35] is selected as the core material of the transformers. It provides a high resistivity and a small eddy current loss and is suitable for high  $f_{sw}$ . For this PC40 core material, saturated flux density  $B_s$  is 380 mT at 100°C. To reduce  $P_{core}$  and prevent  $B_m$  from reaching  $B_s$  during the 200 kHz operation,  $B_m$  is set to 150 mT. As a result, effective volume  $V_e$  of the selected core component PC40EER28L-Z (manufactured by TDK) is 6.15 cm<sup>3</sup>.

Here, we will provide a practical explanation of the design of the transformer for 600 V. The parameters required for the design are as follows.

- 1)  $V_{in} = 600$  V
- 2)  $V_o = 600$  V
- 3) Maximum  $B_m = 150$  mT
- 4)  $f_{sw} = 200$  kHz
- 5)  $A_e = 0.814$  cm<sup>2</sup>

From these specifications and Equation (1),  $N_p$  is calculated to be 30.71 turns. To disperse heat generation from the core material, two transformers are connected in series and each  $N_p$  is set to 16 turns. Since  $N_s/N_p$  is equal to  $V_o/V_{in}$  (= 1),  $N_s$  is the same as  $N_p$ , namely 16 turns.  $C_{ri}$  is set to a value less than 100 nF in order to keep the capacitor size small. Therefore, if  $f_{sw}$  is set

to approximately 200 kHz, the  $L_{ri}$  value of 6  $\mu\text{H}$  or more is sufficient. After the transformer was manufactured, the measured  $L_r$  value was approximately 12  $\mu\text{H}$ . Therefore, the  $C_r$  value required for creating resonance  $f_{sw}$  of 200 kHz is calculated to be approximately 60 nF.  $S$  defined as  $L_r/L_m$  is set to 0.1 [26]. Therefore, the two  $L_{mj}$  values connected in series are set to approximately 120  $\mu\text{H}$ .

It has been shown that the Si IGBTs can be operated at a maximum of 50 kHz [27]. At  $f_{sw}$  of 50 kHz, if the core material considered above (PC40EEE57/47-Z) is used,  $A_e$  and  $V_e$  of the transformer are 3.44  $\text{cm}^2$  and 35.1  $\text{cm}^3$ , respectively. At the switching frequency of 200 kHz,  $V_e$  can be reduced by 82%.

Table 1 summarizes the design specifications of the LLC dc/dc for 600 V and 800 V.

Table 1. Design specifications of LLC dc/dc

Item	Condition	
	600 V	800 V
Input Voltage ( $V_{in}$ )	600 V	800 V
Input capacitances ( $C_{in1}, C_{in2}$ )	2200 $\mu\text{F}$	150 $\mu\text{F}$
Switching transistors ( $Q_i$ $i=1\sim6$ )	SiC MOSFET (SCT2080KE) ( $BV=1200$ V, $R_{on}=80$ m $\Omega$ )	←
Magnetic inductances ( $L_{mi}$ $i=1\sim6$ )	55.6 $\mu\text{H}$ , 55.1 $\mu\text{H}$ , 64.3 $\mu\text{H}$ 51.8 $\mu\text{H}$ , 56.2 $\mu\text{H}$ , 57.5 $\mu\text{H}$	94.6 $\mu\text{H}$ , 93.3 $\mu\text{H}$ , 94.0 $\mu\text{H}$ , 94.0 $\mu\text{H}$ , 93.1 $\mu\text{H}$ , 95.4 $\mu\text{H}$
Resonant inductances ( $L_{ri}$ $i=1\sim3$ )	12.0 $\mu\text{H}$ , 11.6 $\mu\text{H}$ , 11.6 $\mu\text{H}$	19.4 $\mu\text{H}$ , 21.2 $\mu\text{H}$ , 20.2 $\mu\text{H}$
Resonant capacitances ( $C_{ri}$ $i=1\sim3$ )	60 nF	30 nF
Secondary diodes ( $D_{oi}$ $i=1\sim6$ )	SiC SBD (SCS210KG) ( $BV=1200$ V)	←
Output capacitances ( $C_{oi}$ $i=1,2$ )	270 $\mu\text{F}$	150 $\mu\text{F}$
Output Voltage ( $V_o$ )	600 V	800 V

## Efficiency and loss

Figure 5 shows the power conversion efficiency as a function of the output power of the LLC dc/dc designed for 600 V. The power conversion efficiency is calculated from the energy usage provided by the input power supply during operation. In the circuit system proposed here, since the output power is directly regenerated to the input side (via diode  $D_r$  as shown in Figure 3),  $V_o$  is equal to  $V_{in}$  and the provided amount of energy can be regarded as the power loss in the LLC dc/dc.

The achieved maximum value of the power conversion efficiency is 97.6% at 5 kW. Switching frequency  $f_{sw}$  reaches 182 kHz to 217 kHz because of the high speed switching characteristics of the SiC MOSFETs.

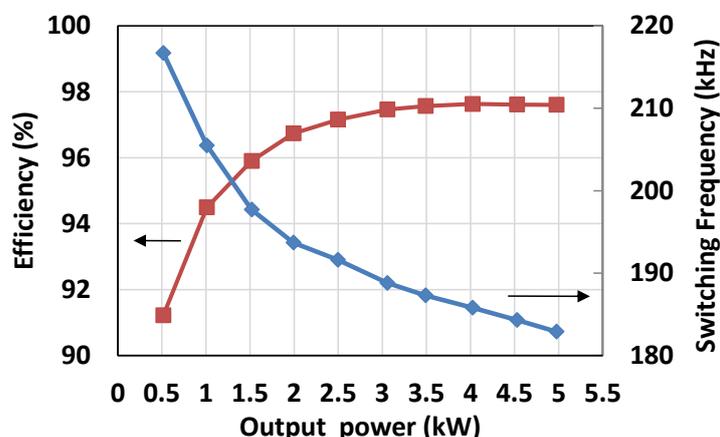


Figure 5. Efficiency and switching frequency for 600 V design

Figures 6 (a) and (b) show, respectively, the power loss ( $P_{loss}$ ) and power conversion efficiency  $\eta_p$  as functions of the output power with different  $V_{in}$  for the 800 V design. As shown in Figure 6 (a), a higher  $V_{in}$  reduces the increase rate of  $P_{loss}$ . Above 3 kW for  $V_{in} = 600$  V and 4 kW for  $V_{in} = 700$  V, the  $P_{loss}$  value is increased so much that the power cannot be supplied.

As shown in Figure 6 (b), it is difficult for the conversion efficiency to reach 97% and the output power is up to 3 kW for 600 V. However, the conversion efficiency can reach 98.1% at the output of 5 kW for 800 V, making the power loss practical.

Note that the conversion efficiency for 600 V shown here is based on a case where the transformers used are designed with the design specifications for 800 V. If the transformers designed with the design specifications for 600 V are used, the power conversion efficiency is 97.6% at 5 kW.

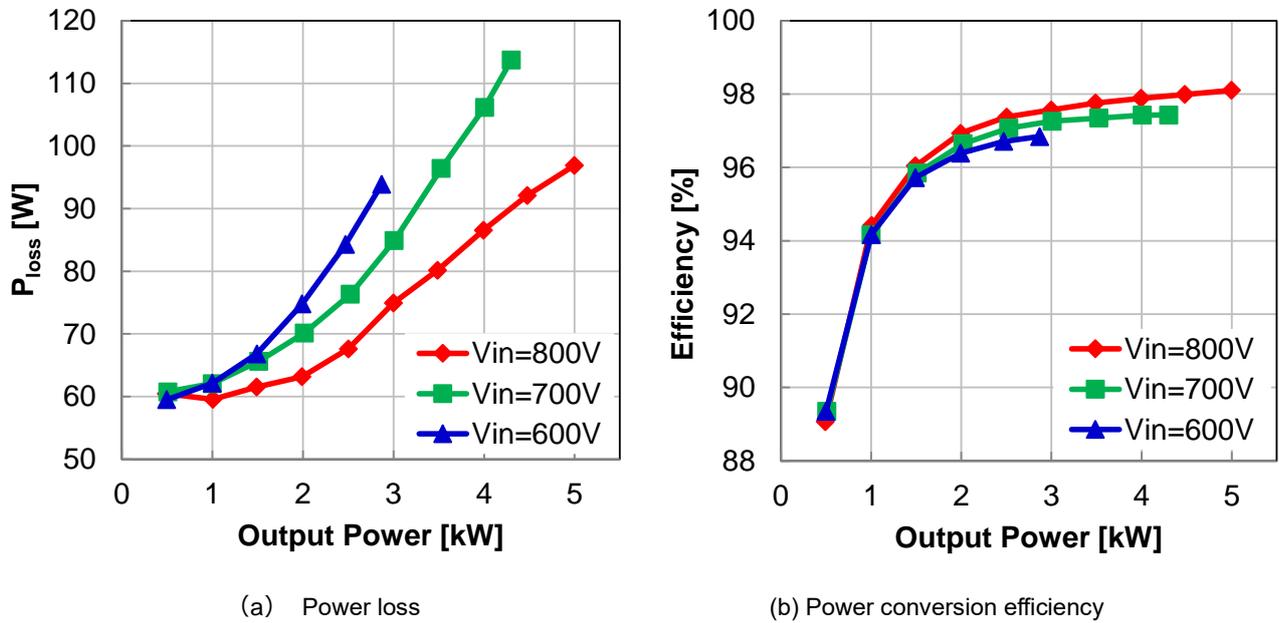


Figure 6. Efficiency characteristics for 800 V design

### Switching waveforms in components

Figure 7 shows the measured waveforms of drain-source voltage  $V_{DS}$  and drain current  $I_D$  for SiC MOSFET  $Q_1$ . The figures (a) and (b) show the waveforms for the 600 V and 800 V designs, respectively. The switching frequencies are approximately 200 kHz and 160 kHz for (a) and (b), respectively. The change in  $V_{DS}$  is completed within a very short period while  $I_D$  is flowing to the negative side. The ZVS operation can be easily confirmed from either of the waveforms.

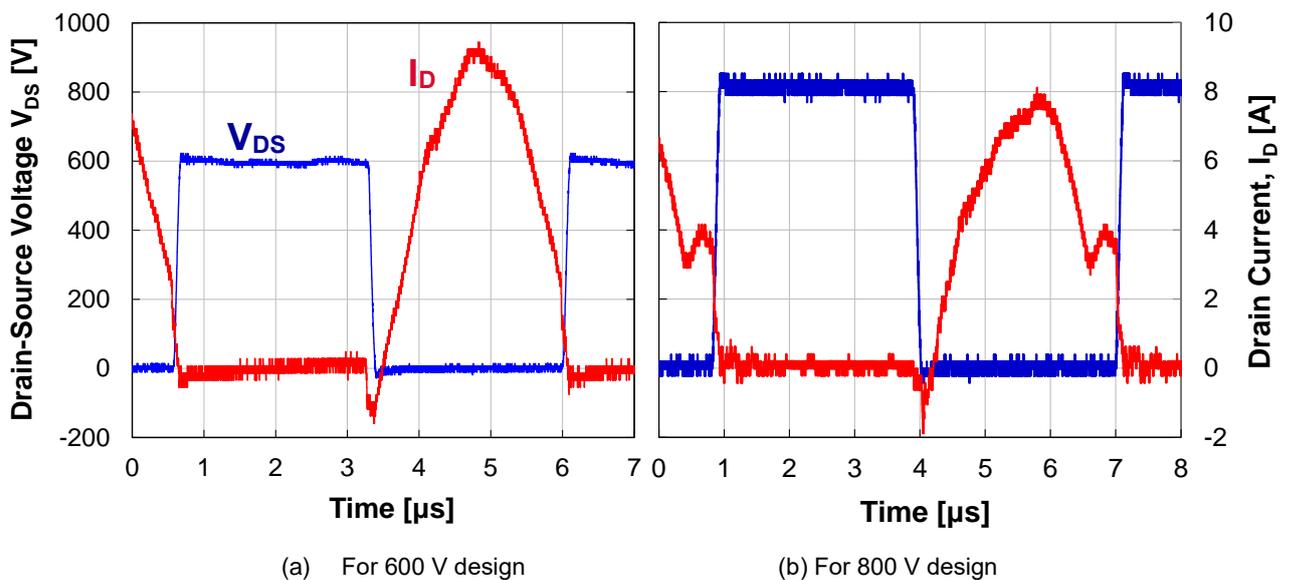


Figure 7.  $V_{DS}$  and  $I_D$  waveforms

Figures 8 and 9 show differences in the output diode currents with or without the current balance circuit. Figures 8 (a) and (b) summarize the currents in the secondary side diodes in the individual phases for the 600 V design. While (a) shows the currents without the current balance circuit, (b) shows the currents with the addition of the current balance circuit. Figures (c) and (d) show the total sum of the diode currents in the individual phases. The total sum represents the ripple current flowing in output capacitors  $C_{o1}$  and  $C_{o2}$ . Figure 9 shows the waveforms for the 800 V design and its details are the same as those of Figure 8.

In either case, if there is no current balance circuit, the current in only one of the phases is decreased or increased, indicating that unbalanced currents are supplied. In contrast, with the addition of the current balance circuit, nearly equal currents are flowing in all phases. The peak-to-peak value of ripple current  $\Delta I_{ripple}$  is, respectively, 6.45 Ap-p at maximum and 6.46 Ap-p at maximum in the unbalanced cases shown in Figures 8 (c) and 9 (c). With the additional current balance circuit, the value is 4.31 Ap-p and 3.75 Ap-p as shown in Figures 8 (d) and 9 (d), respectively, being reduced to 2/3 or less for both voltages.

Equation (2) shows the minimum value of input capacitance  $C_{in}$  or output capacitance  $C_o$  defined as  $C_m$ . This equation also shows that, with a smaller value for  $\Delta I_{ripple}$ , it is possible to set  $C_{in}$  or  $C_o$  to a smaller value, leading to the downsizing.

$$C_m = \frac{\Delta I_{ripple} \times T_{on}}{\Delta V_{ripple}} \quad (2)$$

In Equation (2),  $\Delta V_{ripple}$  is the maximum of the peak-to-peak value of the capacitor voltage, and  $T_{on}$  is the ON time of  $Q_i$ .  $\Delta V_{ripple}$  is usually set relative to the applied voltage. For example, if it is set to 0.1%, the value is 0.6 V and 0.8 V for 600 V and 800 V, respectively. Using the above values of  $\Delta I_{ripple}$ ,  $C_m$  is calculated to be 29.5  $\mu$ F for 600 V and 25.5  $\mu$ F for 800 V when the currents are not balanced, and 19.7  $\mu$ F for 600 V and 14.8  $\mu$ F for 800 V when the currents are balanced. For either voltage, the capacitance of the output capacitor is reduced to a half by balancing the currents.

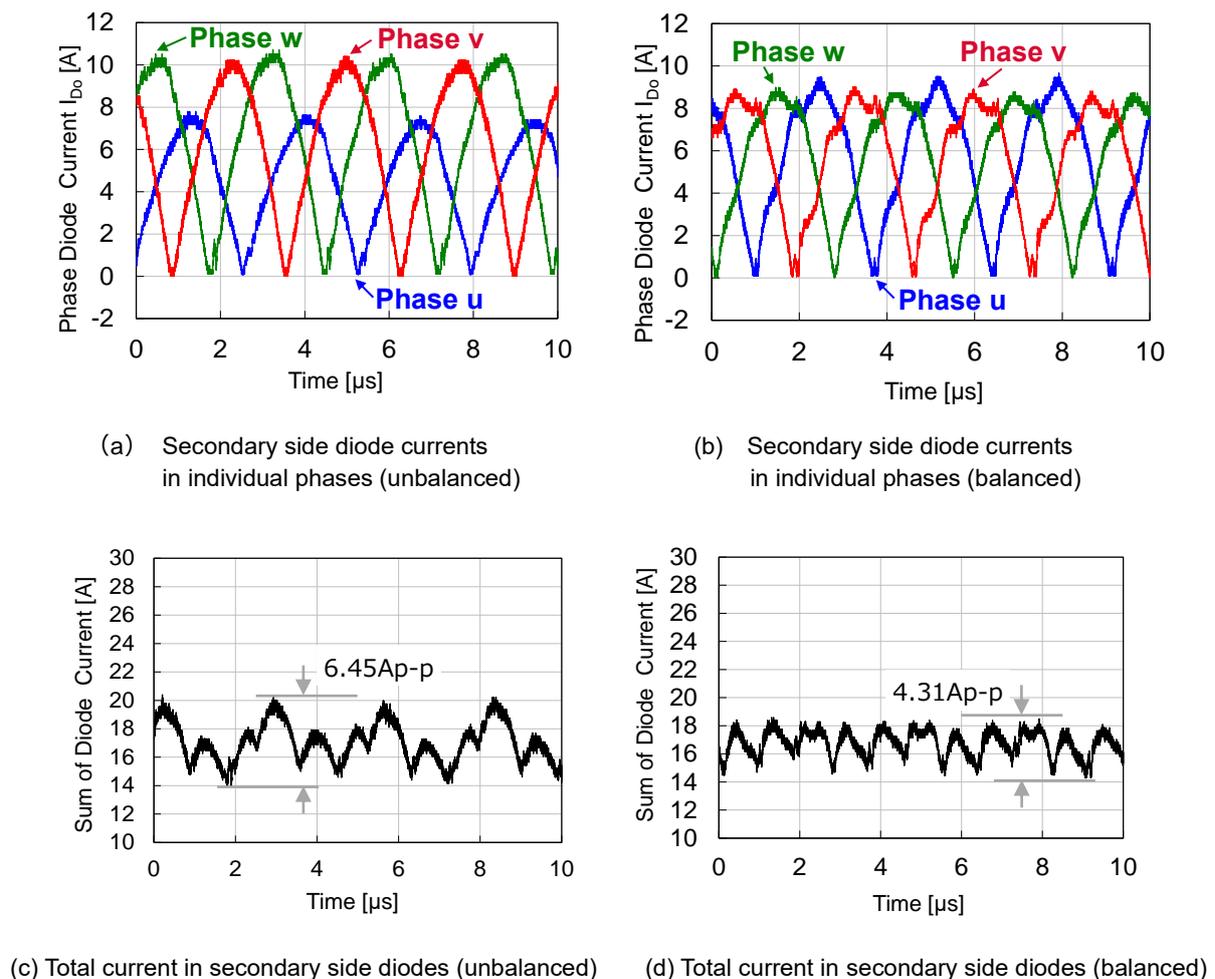
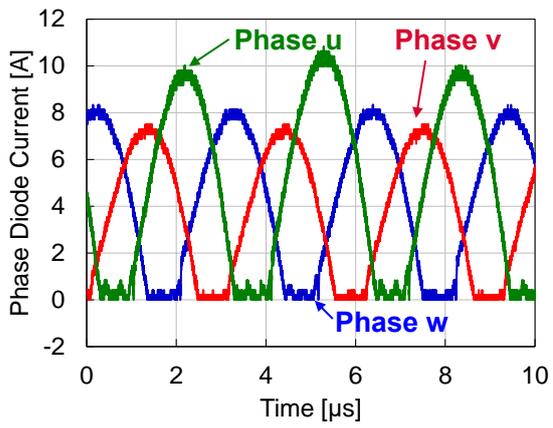
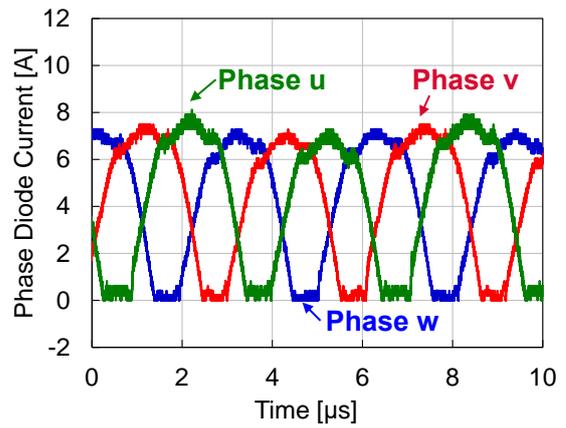


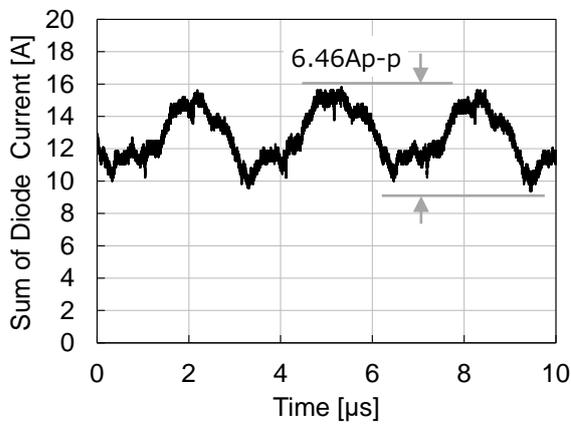
Figure 8. Waveforms of output ripple current (for 600 V)



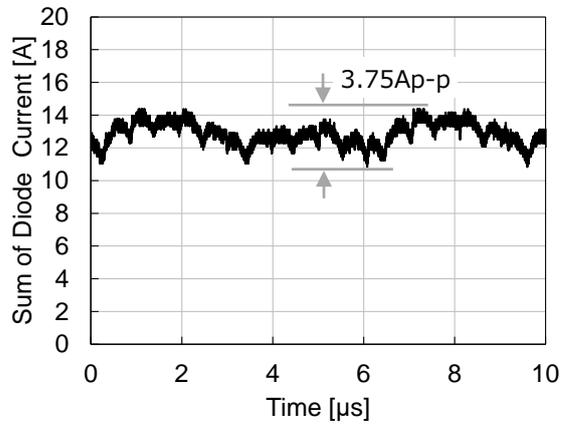
(a) Secondary side diode currents in individual phases (unbalanced)



(b) Secondary side diode currents in individual phases (balanced)



(c) Total current in secondary side diodes (unbalanced)



(d) Total current in secondary side diodes (balanced)

Figure 9. Waveforms of output ripple current (for 800 V)

## Loss analysis

Figure 10 shows breakdowns of losses in the LLC dc/dc using the SiC MOSFETs when the output power is 5 kW. The figures (a) and (b) show the breakdowns for 600 V and 800 V, respectively.

First, for the conduction loss in the transistors ( $I_D^2 * R_{DS(ON)}$ ), on-resistance  $R_{DS(ON)}$  of the SiC MOSFETs used depends on junction temperature  $T_j$ . For this evaluation, a heat sink was installed on the MOSFET and the heat was powerfully dissipated with a cooling fan. As a result,  $T_j$  is kept around 50°C. At  $T_j = 50^\circ\text{C}$ ,  $R_{DS(ON)}$  is approximately 90mΩ [28]. The drain current of the SiC MOSFET  $I_D$  is 4.5 A and 3.75 A for  $V_{in} = 600$  V and 800 V, respectively. Therefore, the total loss in the SiC MOSFETs used can be calculated by multiplying the conduction loss in the transistor ( $I_D^2 * R_{DS(ON)}$ ) by the number of transistors used (6 units), resulting in 10.9 W and 7.59 W for 600 V and 800 V, respectively. For the conduction loss in the secondary side diodes, the average current and the forward voltage are 2.94 A and 1.1 V for 600 V, and 2.62 A and 1.05 V for 800 V. Therefore, by multiplying the loss by the number of transistors used (6 units), the total loss is calculated to be 19.4 W and 16.5 W for 600 V and 800 V, respectively.

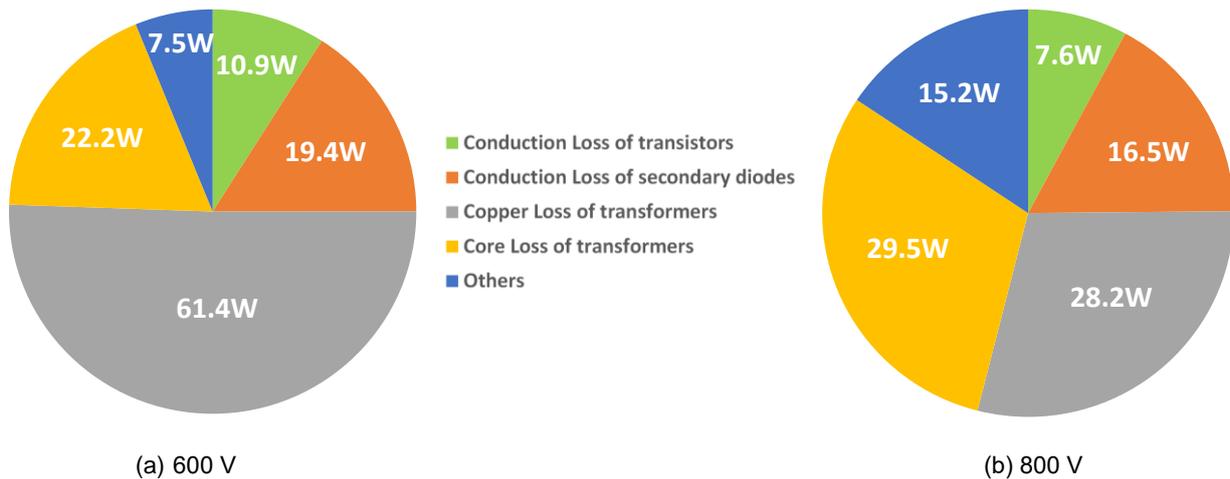


Figure 10. Loss analysis (power value)

Next, for the conduction loss (copper loss) in the transformers used, the total resistance of the winding copper wire shows frequency characteristics. The total resistance is 1.66Ω at the switching frequency of 183 kHz for 600 V, and 1.21Ω at 160 kHz for 800 V. Since the effective value of the current flowing in the transformers is 6.08 Arms for 600 V and 4.83 Arms for 800 V, the copper loss in the transformers is 61.4 W and 28.2 W for 600 V and 800 V, respectively. Needless to say, the significant reduction in the copper loss for 800 V can be attributed to the smaller output current for 800 V because of the higher output voltage at the same output power.

Furthermore, the core loss, another major loss in the transformers, is calculated as follows. First, for 600 V, using Equation (1) with  $A_e = 0.814 \text{ cm}^3$ ,  $N_p = 16$  turns,  $f_{sw} = 182.9 \text{ kHz}$ , and the input voltage of 300 V on each of the transformers connected in series,  $B_m$  is calculated to be 157 mT. From this value of  $B_m$ , based on the  $B_m$ -core loss characteristics described in the data sheet of TDK PC40EER28L-Z, the core loss is calculated to be 22.2 W. Similarly,  $B_m$  and the core loss are calculated to be 181 mT and 29.5 W for 800 V, respectively.

There still remains a difference between these losses and the total loss that is actually measured. The difference is 3.2 W and 12.2 W for 600 V and 800 V, respectively. It mainly represents the switching loss in the SiC MOSFETs, the core loss in the current balance transformers, and the ESR loss in the input and output capacitors.

Finally, Figure 11 shows the composition ratio of the losses for 600 V and 800 V. The use of the SiC MOSFETs reduces the conduction loss in the transistors to approximately 10% of the entire loss. However, the total loss in the transformers (copper loss + core loss) accounts for as much as approximately 58% and 83% of the entire loss for 600 V and 800 V, respectively. Therefore, how to reduce the losses in the transformers can be regarded as a future challenge.



Figure 11. Loss analysis (ratio)

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## Summary

With the three-phase 5 kW LLC dc/dc converter using the SiC MOSFETs, the switching frequency reached approximately 200 kHz for 600 V and enabled the downsizing of the isolated transformers. Such downsizing is impossible to achieve with the Si IGBTs. The high BV of the SiC MOSFETs allowed a  $V_{in}$  value as high as 800 V.

Meanwhile, the three-phase configuration reduced the current in each phase, maintained the high power conversion efficiency of the LLC dc/dc, and avoided increase in the switching loss at high frequencies. Furthermore, the additional current balance transformers for balancing the total currents in the individual phases reduced the current ripple by reducing the circuit peak current. These findings allowed us to further propose a circuit system that can minimize  $C_{in}$  and  $C_o$ .

We hope you find these circuit examples informative.







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